MICROGRID POWER QUALITY ENHANCEMENT USING A THREE-PHASE FOUR-WIRE GRID INTERFACING COMPENSATOR

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BONAFIDE CERTIFICATE

Certified that this project report entitled **"MICROGRID POWER QUALITY ENHANCEMENT USING A THREE PHASE FOUR WIRE GRID INTERFACING COMPENSATOR"** is the bonafide work of

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ABSTRACT

This report presents a three-phase four-wire grid-interfacing power quality compensator for micro grid applications. The compensator is proposed for use with each individual Distributed Generation (DG) system in the microgrid. It consists of two four-phase-leg inverters (a shunt and a series), optimally controlled to achieve an enhancement of both the quality of power within the micro grid and the quality of currents flowing between the micro grid and the utility system. During utility grid voltage unbalance, the compensator can compensate all the unwanted positive-, negative-, and zero-sequence voltage–current components found within the unbalanced utility. Specifically, the shunt four-leg inverter is controlled to ensure balanced voltages within the micro grid and to regulate power sharing among the parallel-connected DG systems.The series inverter is controlled complementarily to inject negative- and zero-sequence voltages in series to balance the line currents, while generating zero real and reactive power. The proposed system along with its controller is modeled and simulated in **MATLAB** using **simulink** and power system block-set tool boxes.

The performance of the proposed compensator has been verified in simulations. A laboratory hardware prototype model is designed, fabricated and tested.

ACKNOWLEDEGEMENT

I humbly submit all the glory and thanks to the almighty for showering the blessings and giving the necessary wisdom for accomplishing this project.

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LIST OF SYMBOLS AND ABBREVIATIONS

Symbols	Abbreviations
VSI	Voltage Source Inverter
DG	Distributed Generation
PCC	Point of Common Coupling
PV	Photo Voltaic
MGCC	Micro Grid Central Control
MV	Medium Voltage
LV	Low Voltage
MC	Microgrid Control
DMS	Distributed Management System
PI	Proportional Integral
PWM	Pulse Width Modulation
PLL	Phase Locked Loop
LPF	Low Pass Filter
DC	Direct Current
AC	Alternate Current
LOH	Lower Order Harmonics
THD	Total Harmonics Distortion
ph.	Phase
PIC	Peripheral Interface Con
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

IC	Integrated Circuit
LED	Light Emitting Diode
I/O	Input/ Output
A/D	Analog/Digital
ADC	Analog to Digital
Vc	Capacitor Voltage
w	Fundamental Frequency of the System

CHAPTER- I

INTRODUCTION

The interconnection of small, modular generation sources to low voltage distribution systems can form a new type of power system, the Micro Grid (Fig.1.1). Such systems can be operated in a non-autonomous way, if interconnected to the grid, or in an autonomous way, if disconnected from the main grid. The operation of micro-sources in the network can provide distinct benefits to the overall system performance, if managed and coordinated efficiently. The output from the power sources are typically not suited for direct connection to the micro grid, which will operate at standard frequency and voltage. For this reason a power electronic interface is required.

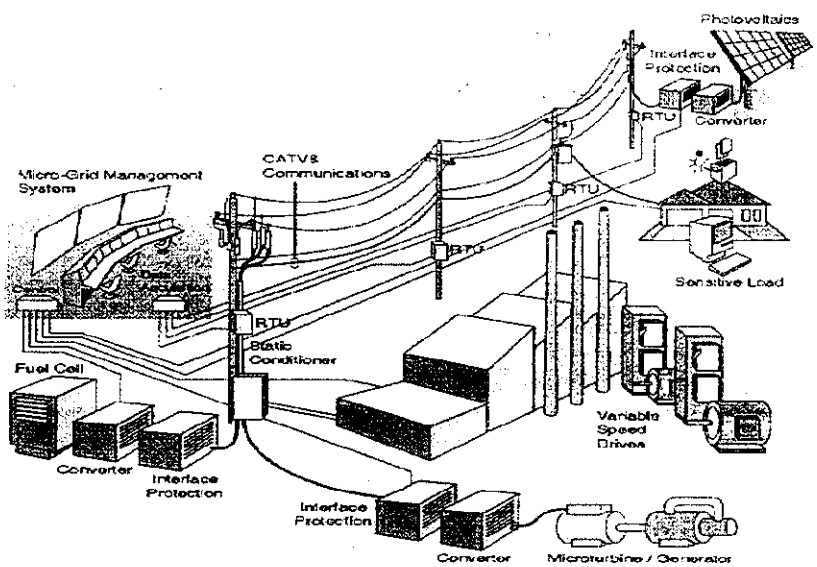


Figure 1.1 Concept of Microgrid

1.1 DEFINITIONS

1.1.1 **Micro Grids** are defined as low-voltage networks with micro-generation sources (PV, micro turbines, fuel-cells, micro-wind generators), together with local storage devices and controllable loads (e.g. water heaters and air conditioning) Fig.1.2

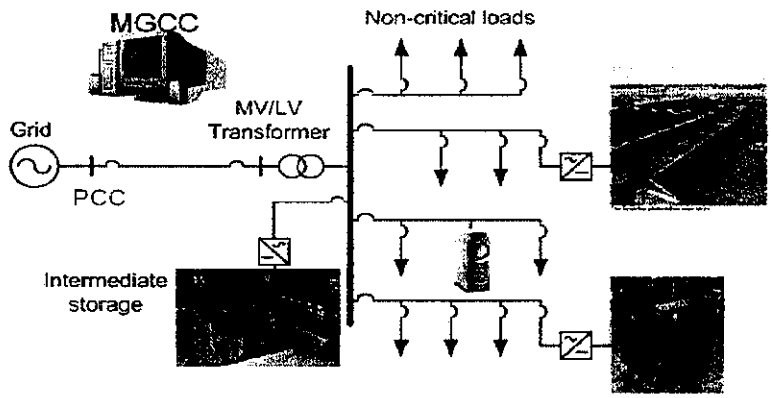


Figure 1.2 General Layout of microgrid

The total installed capacity in these MicroGrids is around a few hundred kilowatts. The unique feature of MicroGrids is that, although they operate mostly connected to the distribution network, they can be automatically transferred to islanded mode, in case of faults in the upstream network and can be resynchronized after restoration of the upstream network voltage. These LV grids are no three phase balanced systems, mainly because there is a large share of single phase loads. If micro-generation is added, an additional phase unbalance can be added since some of the micro sources are single phase grid connected (PV panels). Effective solutions are needed to allow for islanded operation of these Micro Grids (4 wires) in order to balance load / generation in these small modular systems.

• **Micro Grids can operate:**

– Normal Interconnected Mode

– Island Mode

Normal Interconnected Mode

• Connection with the main MV grid;

• Supply, at least partially, the loads or injecting in the MV grid;

• In this case, the MGCC:

– Interfaces with MC, LC and DMS;

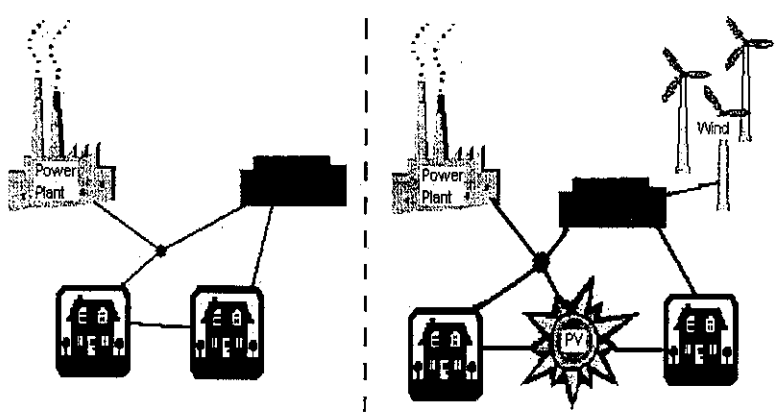
– Perform studies (forecasting, economic scheduling, DSM functions, etc)

Islanding Operation

- In case of failure of the MV grid (improved reliability)
- Possible operation in an isolated mode as in physical islands;

1.1.2 Distributed Generation:

Is the interconnection of alternative energy-producing resources to the utility grid system close to the load sites or at a Point of Common Connection/Coupling (PCC) to alleviate the demand for and expansion of the electric transmission system .DG is meant to shift the structure of the utility system from a centralized, radial system to that of a network of loads and sources that are distributed throughout the system Figure 1.3



(a) (b)

Fig.1.3 (a) Centralized Power System, (b) Distributed Power System

1.1.3 Power Quality:

It is the physical characteristics of the electrical supply provided under normal operating conditions that do not disrupt or disturb the customer's process

Maintain Specified voltage limit

Specified current limit

Specified frequency limit

1.1.4 Voltage Unbalance:

In three-phase power systems, the generated voltages are sinusoidal and equal in magnitude, with the individual phases 120 degrees apart. Nevertheless, electrical systems naturally have some degree of unbalance. Voltage unbalance can be defined as unequal voltage magnitudes at fundamental system frequency (under-voltages and over-voltages), fundamental phase angle deviation and unequal levels of harmonic distortion between the phases.

$$\% \text{ Unbalance} = \frac{\text{Maximum Deviation from Average}}{\text{Average of Phase - to - Phase voltages}} \times 100$$

The main cause of unbalanced voltages on distribution circuits are unbalanced loads.

1.1.5 Voltage Balancing:

Maintaining an exact voltage balance on all three phases at the point of use is virtually impossible for the following reasons:

- Single-phase loads are continually connected to, and disconnected from, the Power system
- Single-phase loads are not evenly distributed between the three phases
- Power systems may be inherently asymmetrical

Therefore, some voltage unbalance will be present in any type of low-voltage three-phase three-wire or three-phase four-wire system

1.1.6 Balanced & Unbalanced loads

In single phase (two wire systems) a load takes current under the application of voltage from one source. In three phase, it's actually three sources, each shifted 120 degrees from the prior, so for three phase loads have three voltages and three currents. Now in healthy conditions, that is balanced loads, the currents and voltages of each phase will equal the others of phases in magnitude, while 120 degree shifting is maintained. This way the voltages will sum to zero, add magnitudes of: first with 0 shifts, second with 120 degree shift and third with 240 shifts. But in unbalanced load, these sums will not equal zero. This can occur due to unequal impedances of the three phases, or in other words difference in currents magnitudes or angles. Unbalanced loads will cause back flow of current in neutral phase.

1.2 OVERVIEW OF THIS PROJECT:

Micro generators connected to the mains utility grid, usually through some voltage-source inverter (VSI)-based interfaces. Concerning the interfacing of a microgrid to the utility system, an important area of study is to investigate the impact of unbalanced utility grid voltages and utility voltage sags, which are two most common utility voltage quality problems, on the overall system performance. As a common practice, if the utility grid voltages are seriously unbalanced, a separation device, connected between the microgrid and the mains grid to provide isolation in the event of mains faults as in Fig. 1.2 will open and isolate the microgrid. However, when the utility voltages are not so seriously unbalanced, the separation device will remain closed, subjecting the microgrid to sustained unbalanced voltages at the Point of Common Coupling (PCC), if no compensating action is taken. Such an unbalance in voltages can cause increased losses in motor loads and abnormal operation of sensitive equipment. An obvious solution is to balance the voltages within the microgrid using some voltage regulation techniques. However, large unbalanced currents can flow between the unbalanced utility grid and microgrid due to the very low line impedance interfacing both grids, if only the microgrid voltages are

regulated. This flow of large currents can overstress semiconductor devices within the interfacing inverters and the distribution lines, and is expected to worsen during utility voltage sags when the voltage differences between the utility grid and the microgrid increase. For low voltage distribution, where microgrids are usually constructed with a four-wire configuration to supply both single-phase and three-phase loads, the problem is further complicated by the flow of zero-sequence currents through the line and neutral conductors.

To mitigate the above-mentioned complications, proposed a grid-interfacing power quality compensator for three-phase four-wire microgrid applications. The proposed compensator is to be used with each individual distributed generator (DG), and it consists of two optimally controlled four-phase-leg inverters (a shunt and a series as in Fig. 1.4). Operating together, the two four-leg inverters can compensate for all the unwanted positive-, negative-, and zero-sequence voltages/currents within the system, enhancing both the quality of power within the microgrid and the quality of current flowing between the microgrid and the utility. The proposed system has been tested in simulations and experimentally using a laboratory hardware prototype

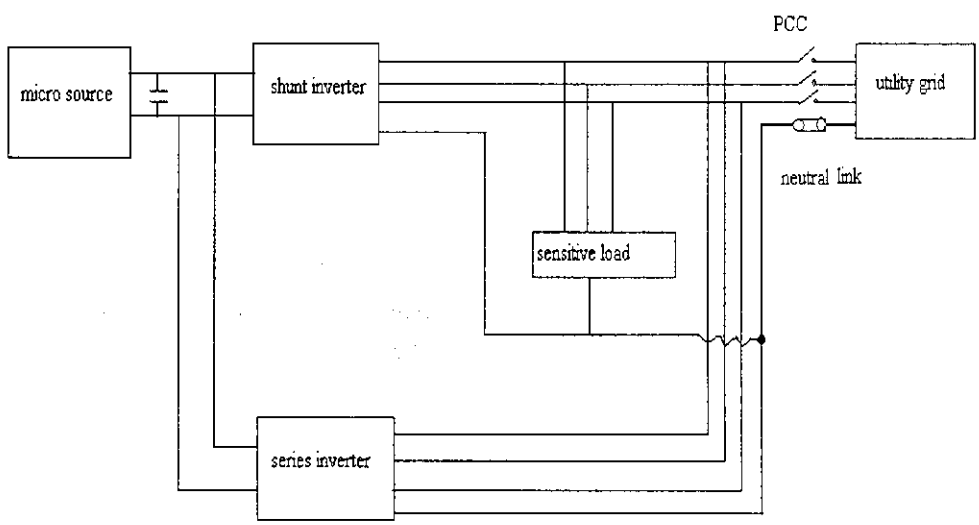


Figure 1.4 General Layout of proposed system

Fig. 1.4 shows the general layout of the proposed grid-interfacing power quality compensator. The compensator consists of two four-phase-leg inverters, namely inverter A (shunt) and inverter B (series). The main functions of inverter A are to maintain a set of balanced sensitive load voltages within the microgrid even under unbalanced load and grid voltage conditions, generate and dispatch power, share the power demand optimally with the other parallel-connected DG systems when the microgrid islands, and synchronize the microgrid with the utility system at the instant of connection. The main functions of inverter B are to maintain a set of balanced line currents by introducing negative- and zero-sequence voltages to compensate for the grid voltage unbalance, and to limit the flow of large fault currents during utility voltage sags.

1.3 OBJECTIVES:

- Maintain balanced microgrid voltages even under unbalanced load and grid voltage conditions.

- Eliminates negative sequence line currents flow with no active power consumption during grid voltage unbalance.

1.4 ORGANIZATION OF THE THESIS:

CHAPTER-1:

Gives an over view of conducted project in the area of Micro grids and voltage balancing strategies.

CHAPTER-2:

Includes the explanation of control strategies used in the two inverters and the main subsystems.

CHAPTER-3:

Presents the final simulation models of three phase three wire compensator both in island and grid connected mode. Results are shown.

CHAPTER-4:

Presents the final simulation models of proposed three phase four wire compensator both in island and grid connected mode. Results are shown and discussed with the results.

CHAPTER-5:

Includes description of all blocks used in hard ware prototype and pin connection diagrams of PIC controller, driver circuits for relay, PIC, power circuits are shown. Photographs of prototype model and wave forms are shown.

CHAPTER-6:

Included conclusion and Discussed with the future scope of the work.

CHAPTER II

CONTROL STRATEGIES FOR PROPOSED COMPENSATOR

The system has two inverters namely shunt and series. The control strategies for these inverters are discussed in this chapter.

2.1 CONTROL SRATEGIES OF SHUNT INVERTER A

2.1.1 Description of Control Algorithm

Figure 2.1 shows the voltage–current regulation scheme for inverter A, which contains an inner filter inductor current control loop and an outer load voltage control loop. For the outer voltage loop, the theoretical analysis is first presented in the synchronous *d*- *q*- 0 reference frames to assist in understanding the control principles. The developed voltage controllers are subsequently converted back to the stationary frame to allow for easier physical implementation. As illustrated in Fig. 2.1, the three-phase load voltages are first transformed from the stationary *a*- *b*- *c* frame to the stationary a- *ß*- 0 frame using the following quad transformation matrices.

$$U_{\alpha\beta 0} = \sqrt{\frac{2}{3}} T_{\alpha\beta 0} U_{abcn} \tag{1}$$

$$U_{\alpha\beta 0} = [U_\alpha \quad U_\beta \quad U_0]^T \tag{2}$$

$$U_{abcn} = [U_{an} \quad U_{bn} \quad U_{cn} \quad U_n]^T \tag{3}$$

$$T_{\alpha\beta 0} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \end{bmatrix} \tag{4}$$

Where *Un* is a placeholder quantity, usually chosen to be 0. The *a*- *ß*- 0 voltages are subsequently transformed to the forward-rotating positive-sequence synchronous frame (Indicated with superscript "+") and reverse-rotating negative sequence frame (indicated with superscript "- ") using the following transformation matrices.

$$U_{dq0}^{+} = \begin{bmatrix} U_d^{+} & U_q^{+} & U_0^{+} \end{bmatrix}^T = T_{dq0}^{+} U_{\alpha\beta 0} \tag{5}$$

$$T_{dq0}^{+} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{6}$$

$$U_{dq0}^{-} = \begin{bmatrix} U_d^{-} & U_q^{-} & U_0^{-} \end{bmatrix}^T = T_{dq0}^{-} U_{\alpha\beta 0} \tag{7}$$

$$T_{dq0}^{-} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 0 \\ -\sin(\omega t) & -\cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{8}$$

Note that the first two rows of *Taß*0, *T*+ *dq*0, and *T dq*0 resemble the commonly used three-phase "*a- b- c* to *a- ß to d- q*" transformation. Equations (1)–(8) can therefore be viewed simply as an extension from the three-phase "*a- b- c to a- ß* to *d- q*" transformation with only an independent zero-sequence row added. It would therefore be convenient to control the *d- q* voltages independently from the zero-sequence voltages, as indicated in Fig. 2.1 with the zero-sequence control path drawn external to the dotted box enclosing the *d- q* control paths.

To achieve zero steady-state errors when controlling the positive- and negative-sequence *d- q* voltages, two PI controllers are used along the positive- and negative-sequence *d- q* control paths. Practically, the implementation of these *d- q* controllers can be computationally inefficient due to the numerous coordinate frame transformations needed. A more efficient form of the voltage controllers can be derived by transforming both the positive- and negative-sequence PI controllers to the stationary *a- ß* frame using either the state-space or frequency domain technique.Performing this inverse transformation $k_p^{+} = k_p^{-} = k_p$ and $k_i^{+} = k_i^{-} = k_i$,

The a- *ß* frame voltage controllers can be expressed as

$$\begin{bmatrix} 2k_p + \frac{2k_i s}{s^2+\omega^2} & 0 \\ 0 & 2k_p - \frac{2k_i s}{s^2+\omega^2} \end{bmatrix}. \tag{9}$$

Effectively, these voltage (P + resonant) controllers introduce an infinite gain at the positive (50 Hz) and negative (- 50 Hz) fundamental frequencies to force the positive- and negative-sequence voltage errors to zero [see Fig. 3(a) for an example bode plot of (9) using a positive resonant frequency of 50 Hz], and can conveniently be implemented in the stationary a-β frame with minimum computational requirements. The same P + resonant compensator with the resonant frequency set at 50 Hz can also be used for controlling the zero sequence voltage, again with zero steady-state error, as shown in Fig. 2.1. Note that for this work, the resonant frequency is set by inverter A "real power versus supply frequency" droop controller and not the utility grid frequency. A mechanism to track the grid frequency for determining resonant condition (or transformation phase for synchronous PI implementation) is therefore not required. The outputs of the individual voltage controllers when added together give the demanded reference currents I^* a, I^* β, and I^* 0 for the inner filter inductor current loop. This inner loop is implemented using only proportional controllers with peak current limiting in the stationary a- β- 0 frame as any steady state error in this loop would not affect the outer voltage loop accuracy substantially. The outputs of the current controllers are then transformed back to the a- b- c frame and sent to a four-phase-leg pulse width-modulation (PWM) modulator for switching shunt inverter A.

2.1.2 Shunt Inverter A Control Structure

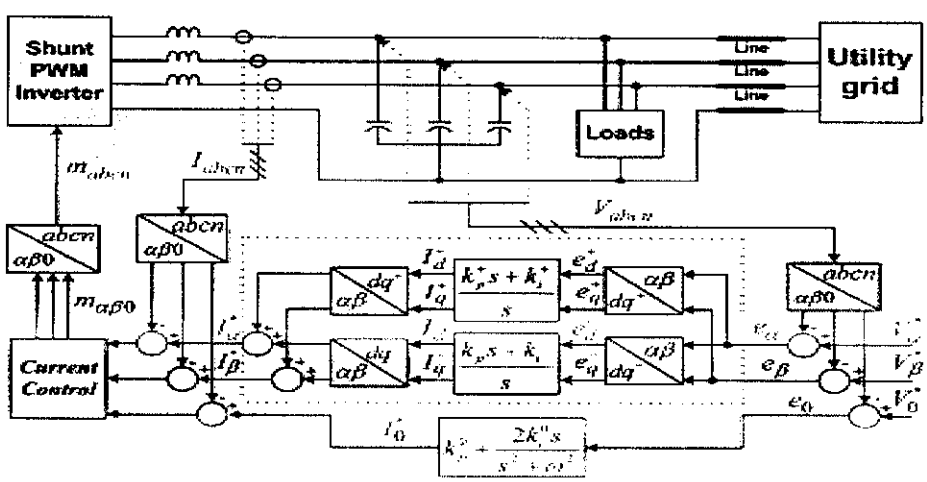


Figure 2.1 Control of shunt inverter A

2.1.3 Simulation Circuit of Shunt Inverter Controller

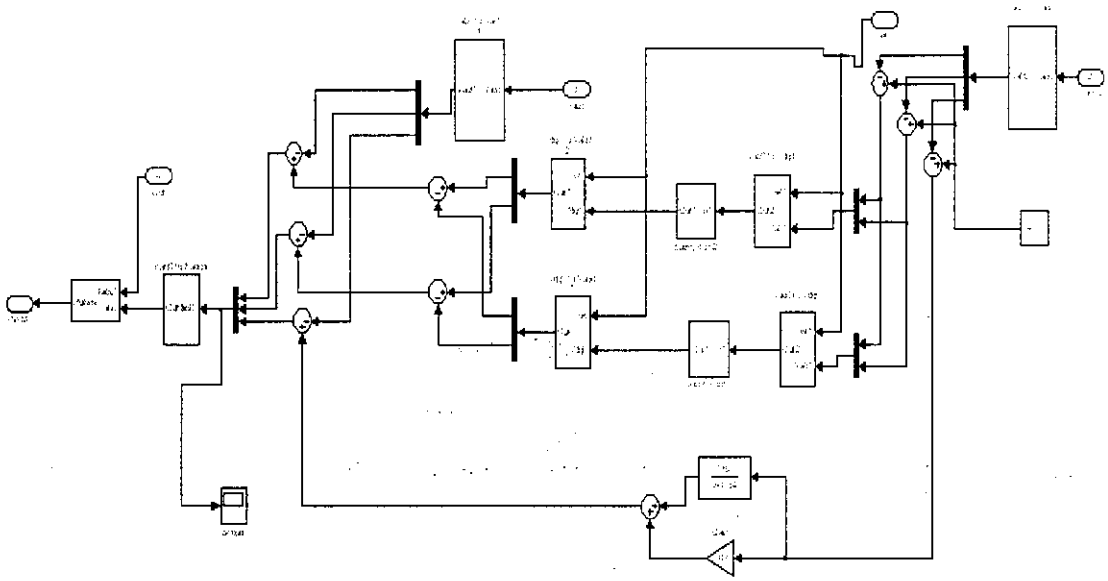


Figure 2.2 Simulation circuit of shunt inverter controller

2.2 CONTROL OF SERIES INVERTER B

2.2.1 Description of Control Algorithm

The circuit connection of series inverter B is shown in Fig. 2.3, where a four-leg inverter is again adopted for the control of zero-sequence component. The main function of the series inverter is to maintain a set of balanced line currents; i.e., to force the negative- and zero-sequence currents to zero in the three-phase four-wire system. Note that this inverter is not designed to control the positive-sequence currents, which are already (directly) regulated by shunt inverter A.Fig.2.2 shows the control scheme for series inverter B, where an inner voltage loop is shown embedded within an outer current loop. The outer current loop (also referred to as the reference voltage generator) functions to generate reference voltages for the inner voltage loop using the negative- and zero-sequence line currents as inputs. As

seen, the measured line currents are first transformed to the negative synchronous d- q- 0 reference frame using (1) and (7), and regulated with zero reference values using PI controllers for the negative sequence d- q currents and a resonant controller for the zero sequence component (see Fig.24). Note that the a- β resonant controllers described in Section compensate for both positive- and negative-sequence components and therefore cannot be used here for solely compensating the negative sequence component.

Before feeding into the PI controllers, the current signals should be filtered to remove positive-sequence currents, which appear as ac signals at twice the fundamental frequency, leaving only dc negative-sequence currents for compensation. This filtering is needed for enhancing the robustness of the control loop and is performed by averaging the d- q currents over half a fundamental cycle in the negative synchronous frame. Quite obviously, a degradation associate with this "half fundamental cycle" filtering would be the overall poorer controller transient response. Also shown in Fig (2.4) are measures taken to decouple the d- and q-control paths (indicated by dotted lines in the figure) to arrive at three decoupled d-, q-, and 0-axis control paths, which can be tuned independently. The outputs of this outer reference voltage generator, consisting only of negative- and zero-sequence components, are then transformed back to the a- β- 0 frame and fed into the inner voltage control loop.

2.2.2 Control of Series Inverter B, Structure

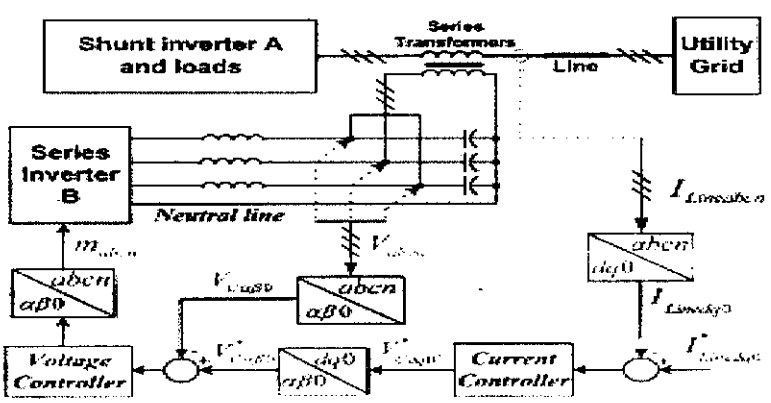


Figure 2.3 Control of series Inverter B

The block representation of the inner voltage loop is shown in Fig.2.4, where P + resonant controllers are used along the *a*- *ß*- 0 control paths. The use of P + resonant controllers in the inner control loop will force the filtered capacitor voltages VC of the series inverter to track the demanded negative and zero-sequence reference voltages V * C with zero steady state errors and eliminate any positive-sequence component since its reference value is kept at zero for the series inverter. The series inverter therefore injects only negative- and zero sequence voltages into the system to maintain a set of balanced line currents with no real and reactive power generation (or absorption) in the steady state. Note that an inner filter inductor current loop can be added to the voltage control loop to give a better dynamic response. However, due to the slow response of the outer reference voltage generation loop, a single inner voltage loop is considered sufficient, and this loop can reasonably be represented by a unity gain when designing the control scheme.

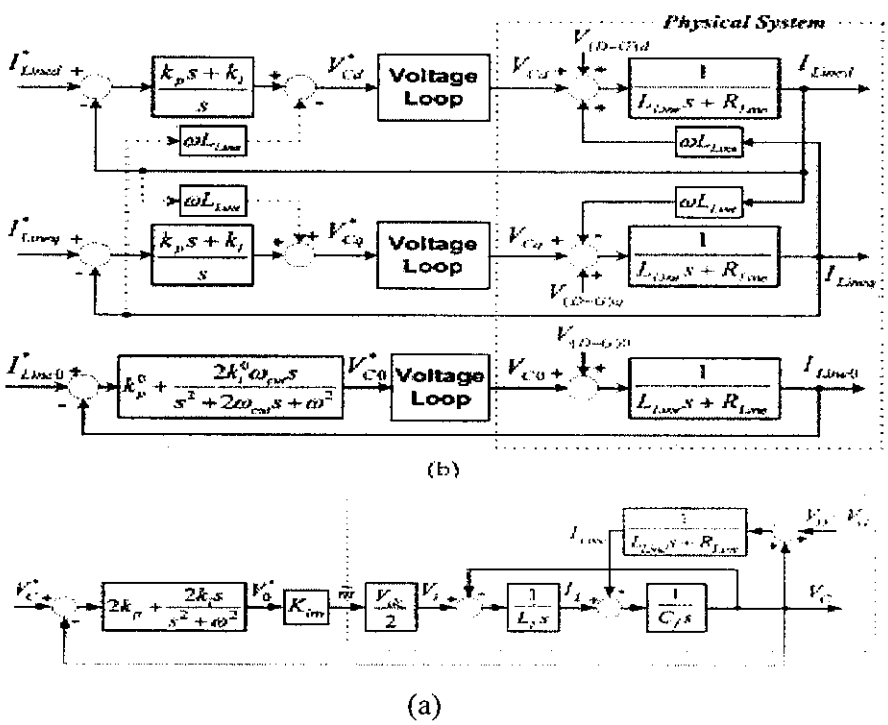


Figure 2.4 (a) Inner Voltage control loop (b) Outer Current loop

2.2.3 Simulation Circuit of Series Inverter Controller

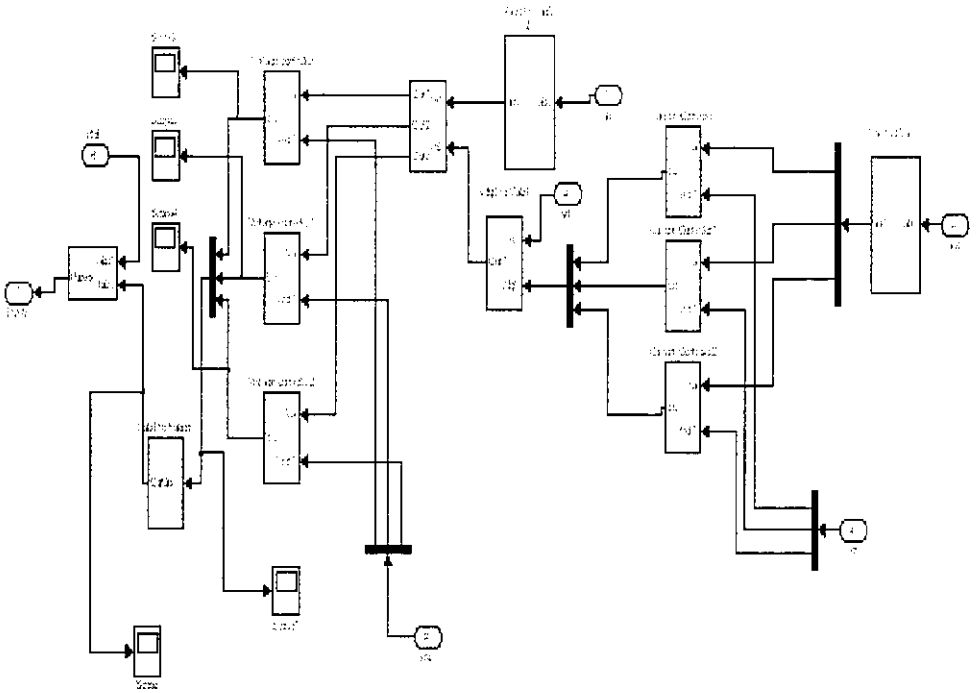


Figure 2.5 Simulation circuits of series Inverter Controller

2.3 IMPORTANT SUBSYSTEMS USED IN THE CONTROLLERS

2.3.1 Voltage controller

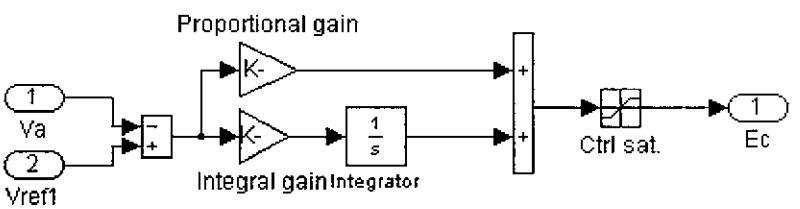


Figure 2.6 Voltage Controller

Each phase, PI controller is placed in the voltage controller.

2.3.2 PLL Block

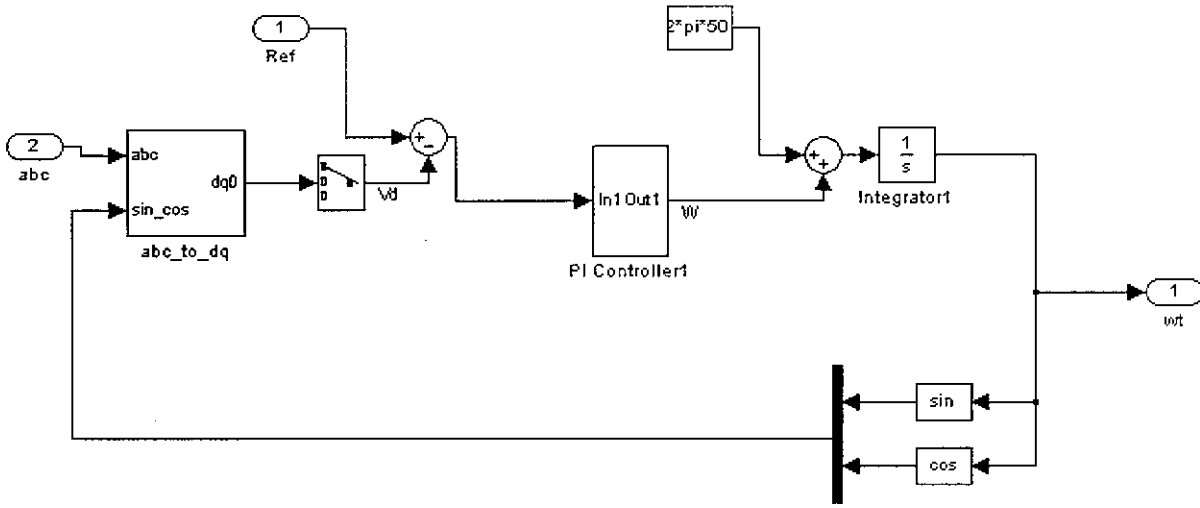
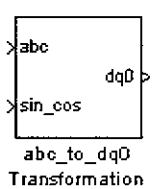


Figure 2.7 PLL Block

(a) abc_to_dq0 Transformation



This block performs abc-dq0 transformation on a set of three phase signals. It computes the direct axis V_d, quadratic axis V_q and zero sequence V0 quantities in a two-axis rotating reference frame according to the following transformation.

$V_d=2/3[V_a* \sin(? t)+V_b* \sin(? t-2p/3)+V_c* \sin(? t+2p/3]$

$V_q=2/3[V_a* \cos(? t)+V_b* \cos(? t-2p/3)+V_c* \cos(? t+2p/3]$

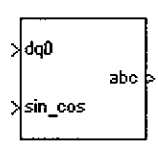
$V0=1/3[V_a+V_b+V_c]$

Where ? is the speed of the rotating frame in rad/sec. In addition, this transformation is known as Park transformation.

After doing the transformation, the direct axis component is compared with the DC error signal. It then given to the PI controller and added with the reference signal. Then it is given to the integrator for calculating the phase angle.

The load current is transformed in to dq0 quantities. By using a LPF and a comparator block, the harmonic content in the load current is calculated. The output signal then compared with the actual shunt active feedback current and the error signal is given to a PI controller for to avoid the fluctuations. The reverse transformation is by using the following equations to get the reference abc signal for PWM pulse generation of shunt inverter.

(b) dq0_to_abc Transformation



$$V_a = V_d * \sin(? t) + V_q * \cos(? t) + V0$$

$$V_b = V_d * \sin(? t - 2p/3) + V_q * \cos(? t - 2p/3) + V0$$

$$V_c = V_d * \sin(? t + 2p/3) + V_q * \cos(? t + 2p/3) + V0$$

The load voltage and feedback shunt controller voltage get compared and then given through the current and voltage controllers to produce the actual voltage signal. The reference current signal and the actual signal compare and produce the pulses for the shunt inverter.

2.3.3 Utility Grid

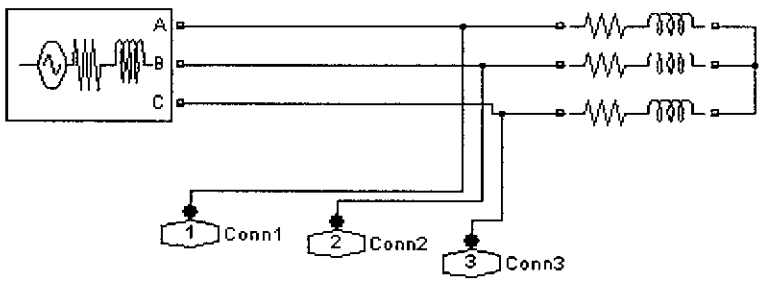


Figure 2.8 Utility Grid.

2.3.4 Four Leg Inverter

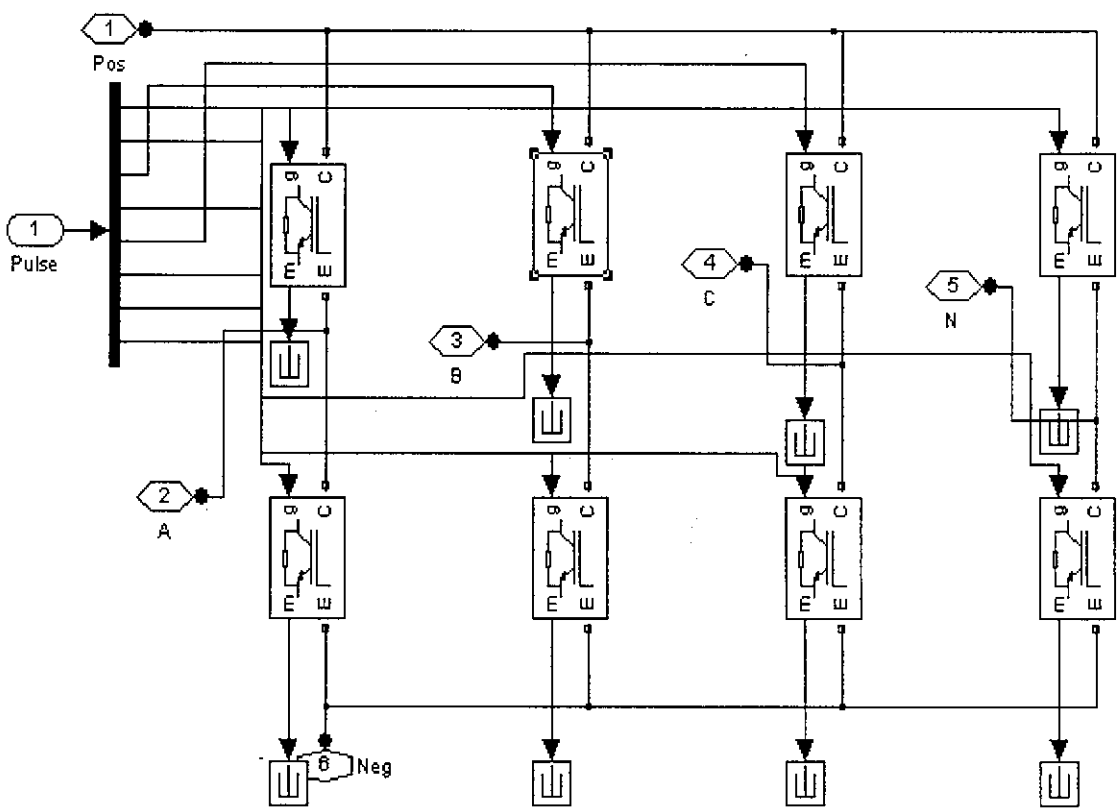


Figure 2.9 Four Leg Inverter Topology.

CHAPTER III

SIMULATION BY USING THREE LEG INVERTER TOPOLOGY AND RESULTS

This chapter includes the simulation model of three-phase three-wire compensator. It is simulated in island and grid interfacing mode. In island mode balanced and unbalanced loads are connected compensator, results are obtained. The results are plotted from grid interfacing model also.

3.1 THREE-LEG VOLTAGE SOURCE INVERTER

The topology of a three-leg voltage source inverter is shown in Fig. 3.1. Because of the constraint that the input lines must never be shorted and the output current must always be continuous a voltage source inverter can assume only eight distinct topologies. Six out of these eight topologies produce a nonzero output voltage and are known as non-zero switching states and the remaining two topologies produce zero output voltage and are known as zero switching states.

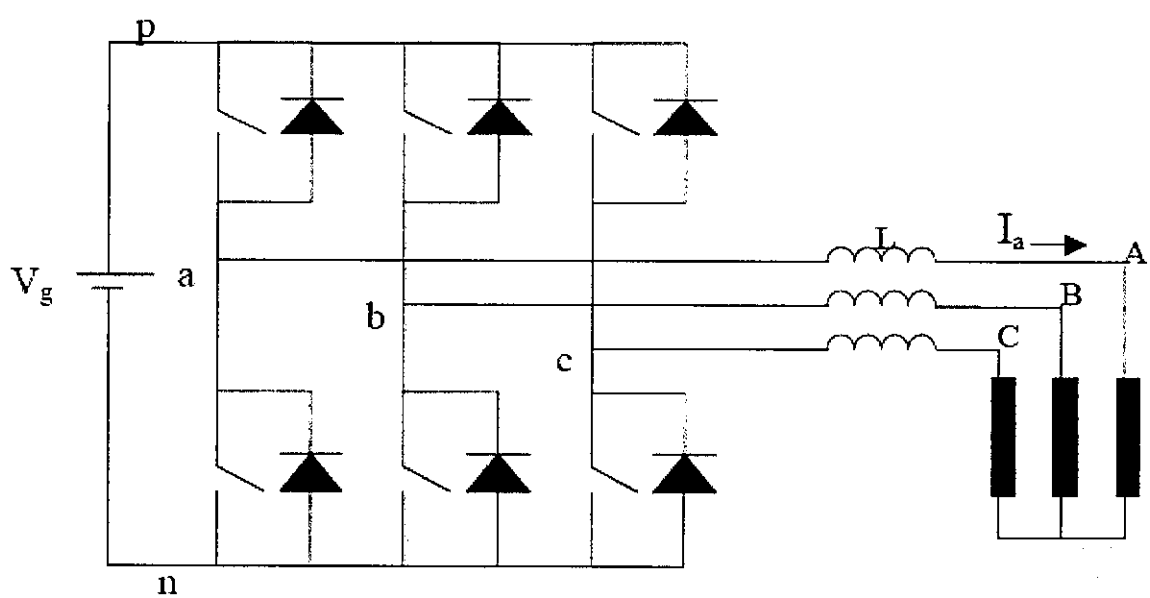


Figure 3.1 Topology of a three-leg voltage source inverter

The function of the Inverter is to convert DC input voltage to a 3-Phase AC output voltage of desired magnitude and frequency. In this chapter, 3-Phase Inverter consists of three–legs one for each phase. Each phase has 2 switches and a total of 6 switches. This Inverter is also called six-step Inverter. For one cycle of 360° each step (change of firing angle from one switch to another

switch) has a 60° interval. The output of each phase is shifted by 120°. The diodes are connected anti parallel to the switches in order to accommodate the phase relationship between current and voltage when we are using inductive Loads. Here 180° Conduction mode is performed since its Utility factor is more when compared to 120° Conduction Mode.

Along with the simulation of 3-Phase PWM Inverter Sinusoidal PWM Technique is performed. To perform Sinusoidal PWM a triangular reference signal along with a sinusoidal reference signal is used to determine the switching times for the Power MOSFET. These inputs are compared and will control the ON/OFF states of the power MOSFET. The main advantage of this sinusoidal PWM Technique is to have reduced value of Total Harmonic Distortion (THD) and the Lower Order Harmonics (LOH) .The following diagram depicts the two inputs of the comparator.

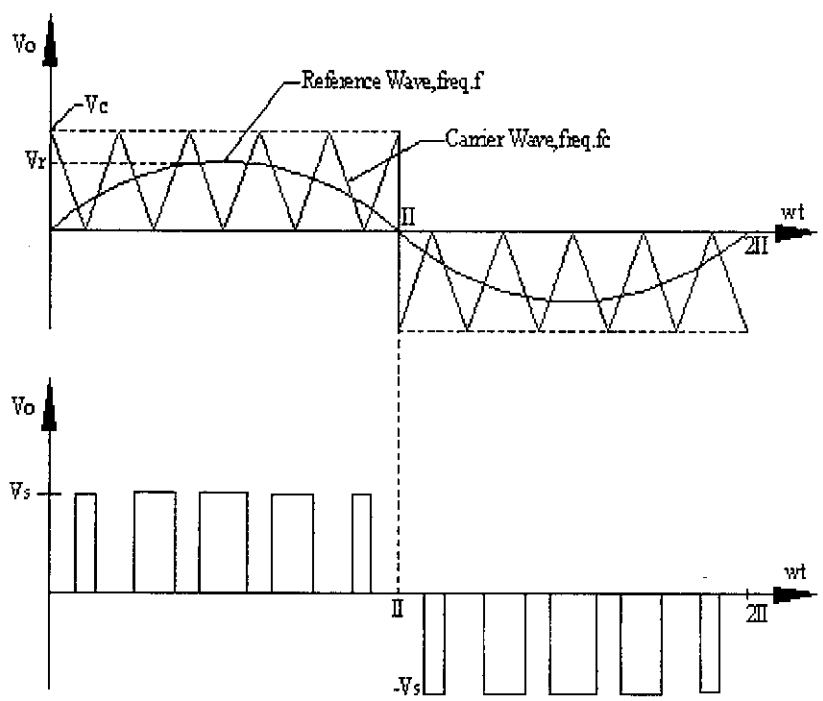


Figure 3.2 Sinusoidal PWM wave form

3.2 OVERALL SYSTEM STRUCTURE (THREE- PHASE THREE WIRE SYSTEM)

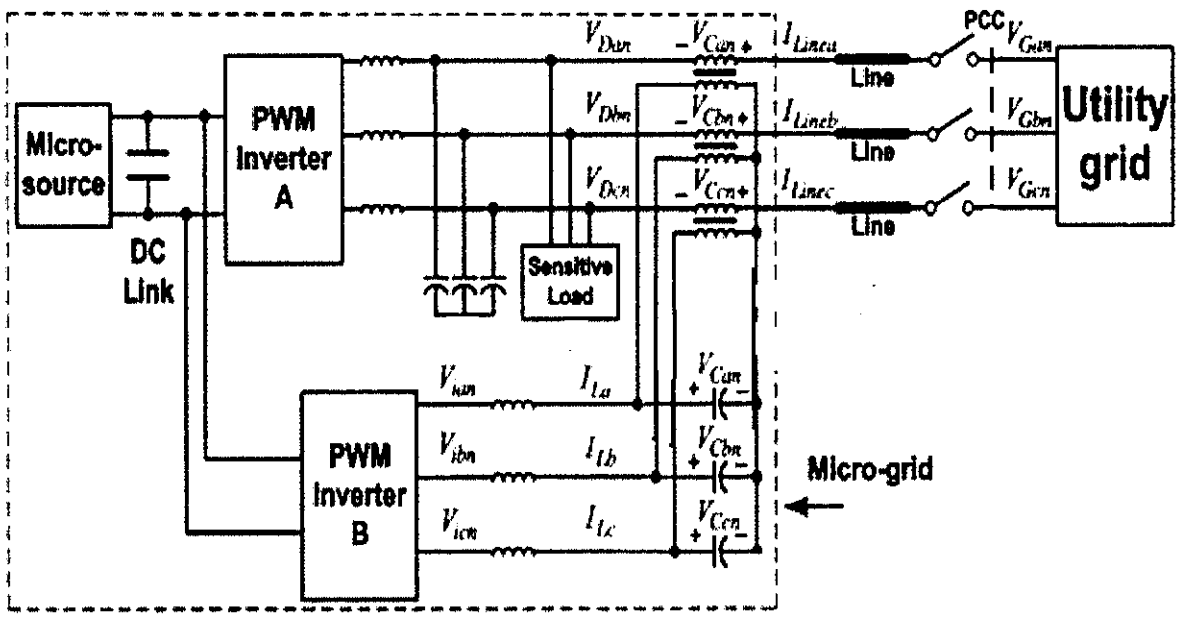


Figure 3.3 Overall System Structure (3ph.3 wire)

Fig.3.3 shows the general layout of the proposed grid-interfacing power quality compensator. The compensator consists of two four-phase-leg inverters, namely inverter A (shunt) and inverter B (series). The main functions of inverter A are to maintain a set of balanced sensitive load voltages within the microgrid even under unbalanced load and grid voltage conditions, generate and dispatch power, share the power demand optimally with the other parallel-connected DG systems when the microgrid islands, and synchronize the microgrid with the utility system at the instant of connection. The main functions of inverter B are to maintain a set of balanced line currents by introducing negative- and zero-sequence voltages to compensate for the grid voltage unbalance, and to limit the flow of large fault currents during utility voltage sags.

3.3 SIMULATION CIRCUIT WITH THREE PHASE –THREE WIRE COMPENSATOR (ISLAND MODE)

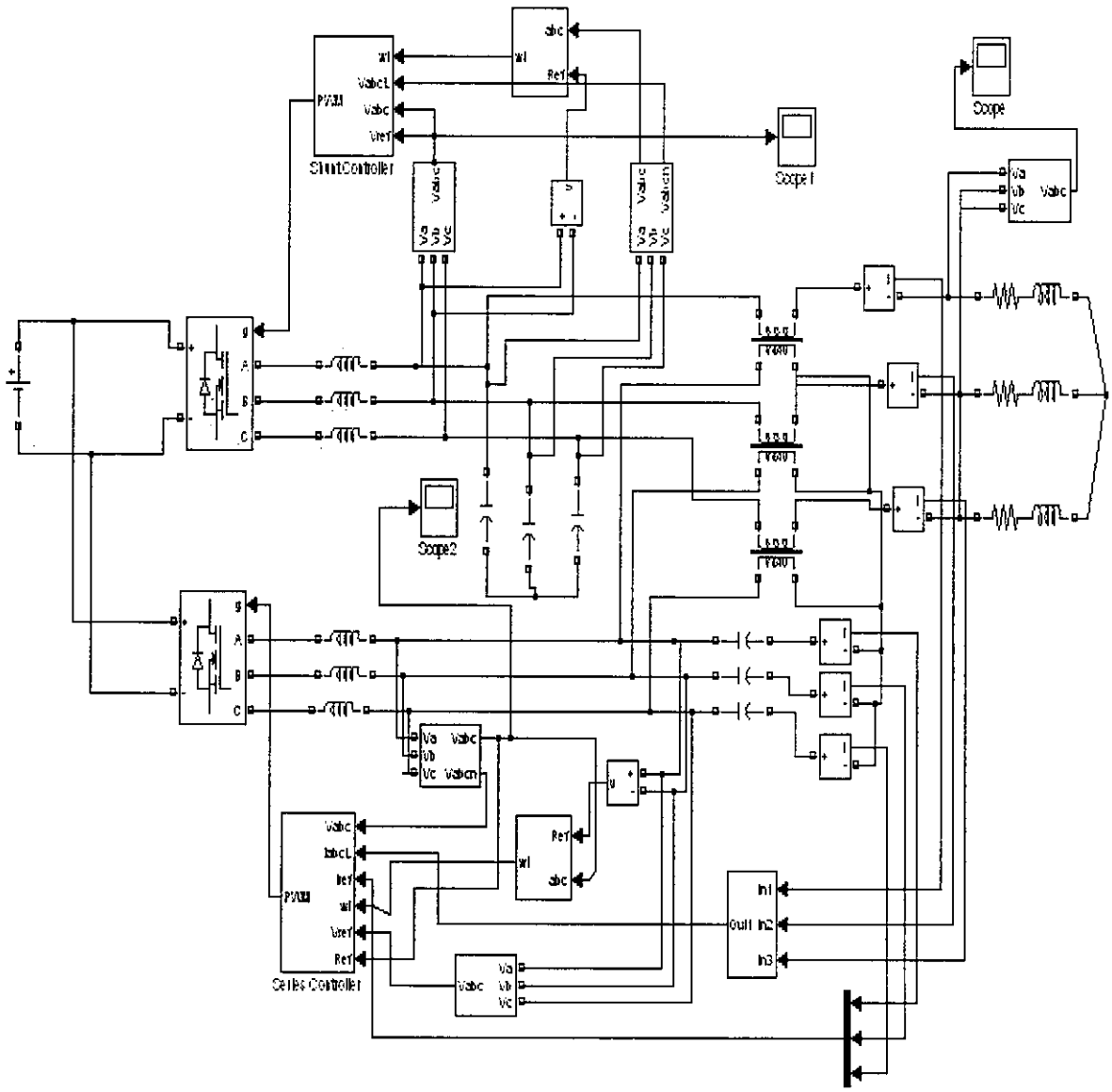


Figure 3.4 3ph. 3wire (island mode)

3.3.1 Microgrid Voltage with Balanced Load

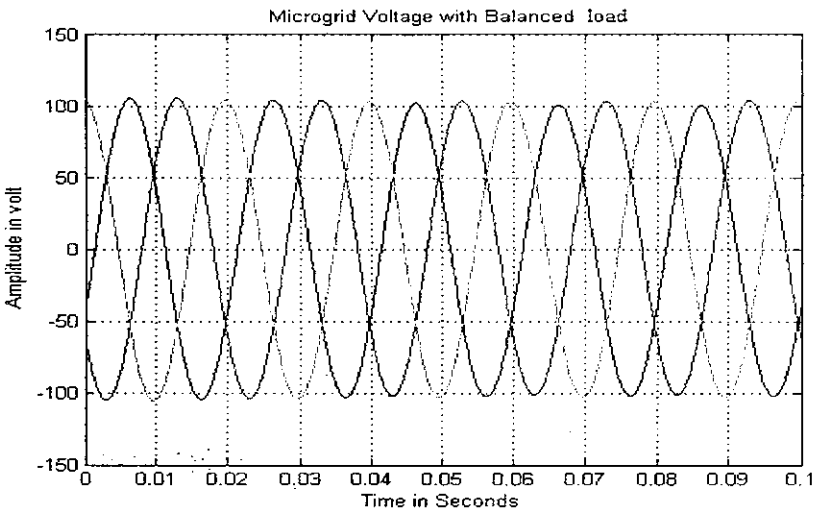


Figure 3.5 Microgrid voltages with balanced load in 3ph.3wire system

3.3.2 Microgrid Voltage with Unbalanced Load

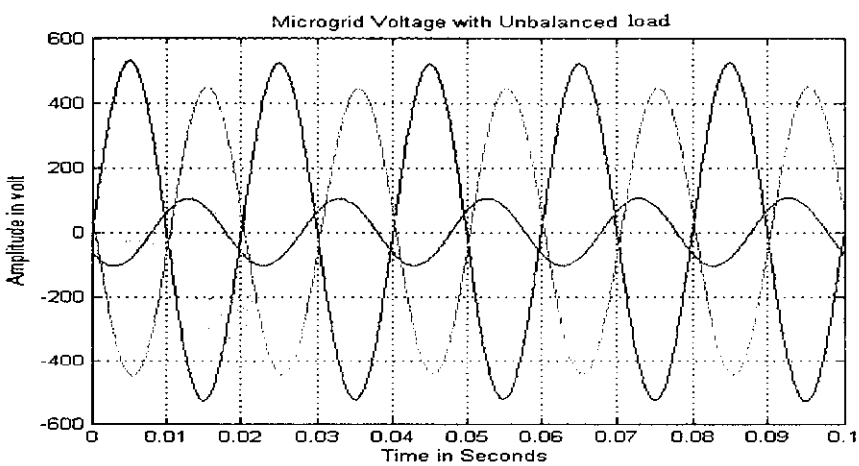


Figure 3.6.Microgrid voltage with unbalanced load in 3ph.3wire

3.4 SIMULATION CIRCUIT WITH THREE –PHASE THREE -WIRE MODEL (GRID INTERFACING)

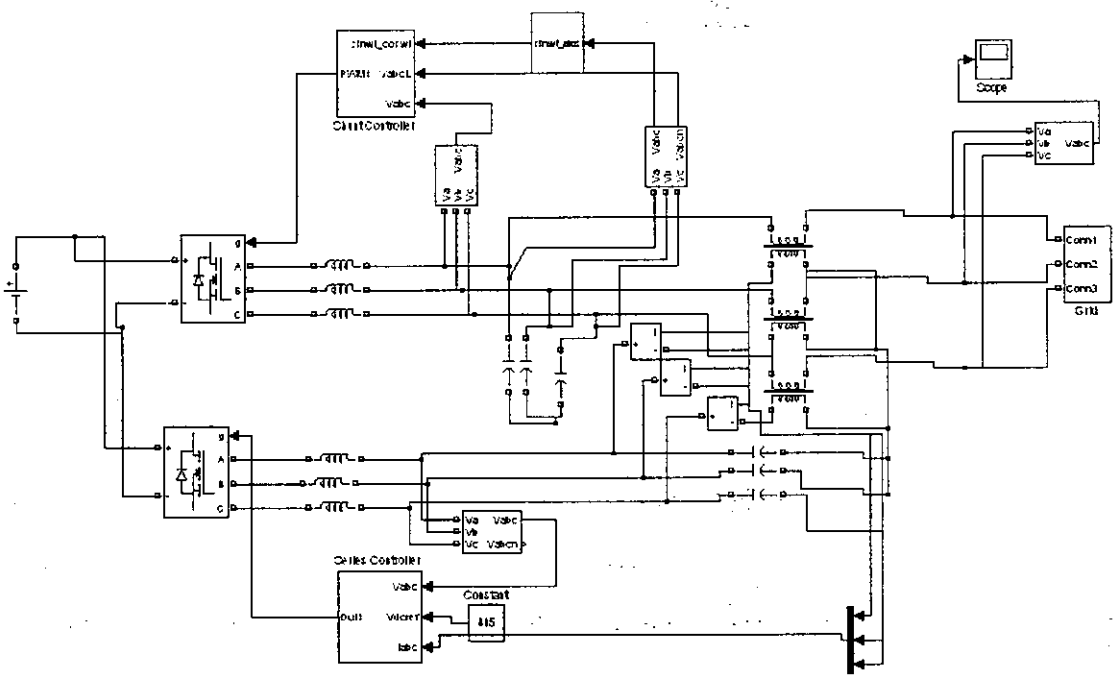


Figure 3.7 3ph.3 wires (grid interfacing)

3.5 THD of 3ph. 3wire system

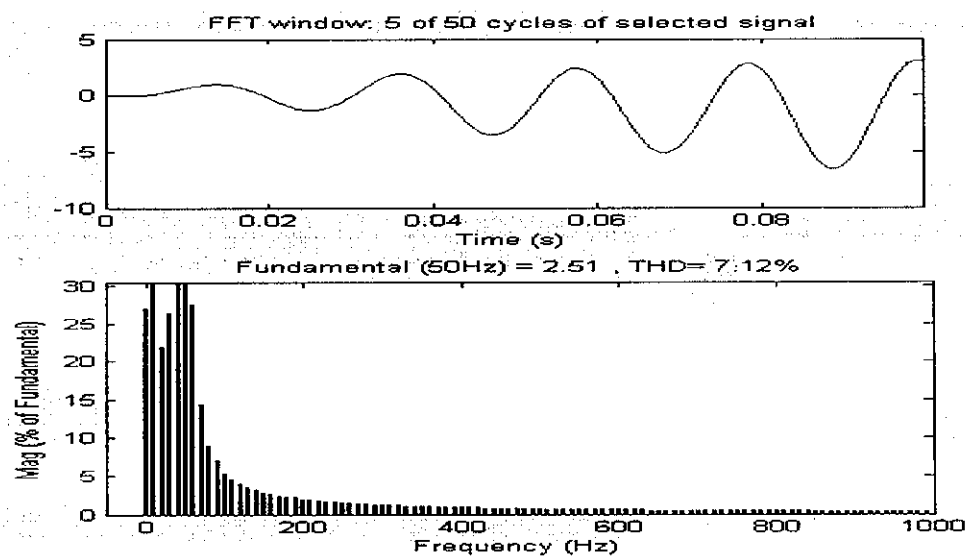


Figure 3.8 THD of 3ph.3wire

CHAPTER IV

SIMULATION OF PROPOSED SYSTEM BY FOUR LEG INVERTER TOPOLOGY AND RESULTS

4.1 FOUR-LEG VOLTAGE SOURCE INVERTER

A voltage source inverter based on the well known three-leg topology can only produce two independent output voltages. For example, if Vab and Vbc are both known, then Vca is implicitly defined. Thus, three-leg inverters can produce completely balanced three-phase voltages only if the Y-connected loads and filters are balanced. For sourcing power to unbalance and non-linear three-phase loads, four leg inverters have been developed. The fourth leg controls the neutral phase voltage and does not conduct any neutral currents. Through this, the four-leg inverter can produce three independent output voltages, regardless of loading. The topology of this approach is shown in Figure 4.1

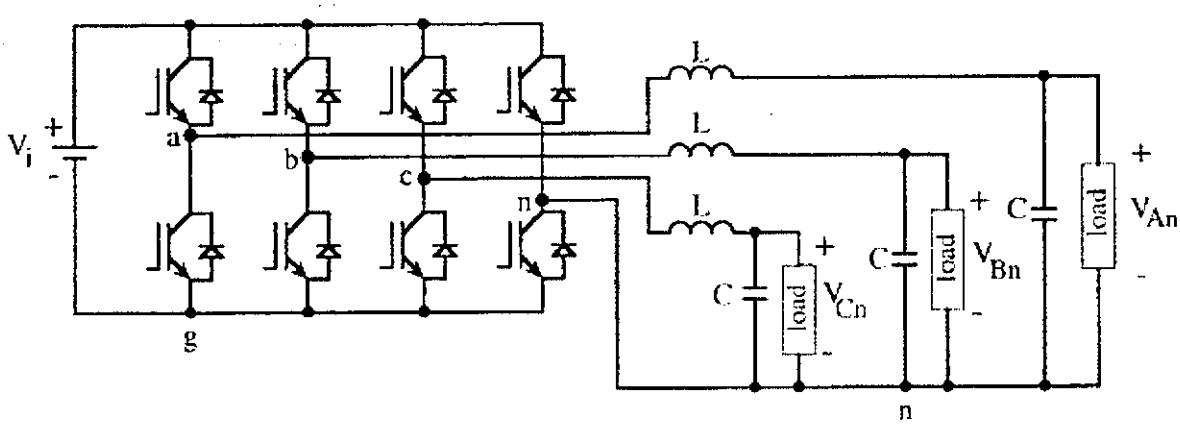


Figure 4.1 Four Leg VSI Topology

Li et al.[2] presented a power quality compensator for MicroGrid applications which employs a four-leg inverter [18]. The design and modeling of a balancing unit for this master thesis was based on that paper. Li et al. use both shunt and series connected inverters to overcome unbalanced utility grid voltages. Thus, they are enhancing both the quality of power within the MicroGrid and the quality of current flowing between the MicroGrid and the utility grid.

4.2 OVERALL SYSTEM STRUCTURE (THREE –PHASE FOUR WIRE SYSTEM)

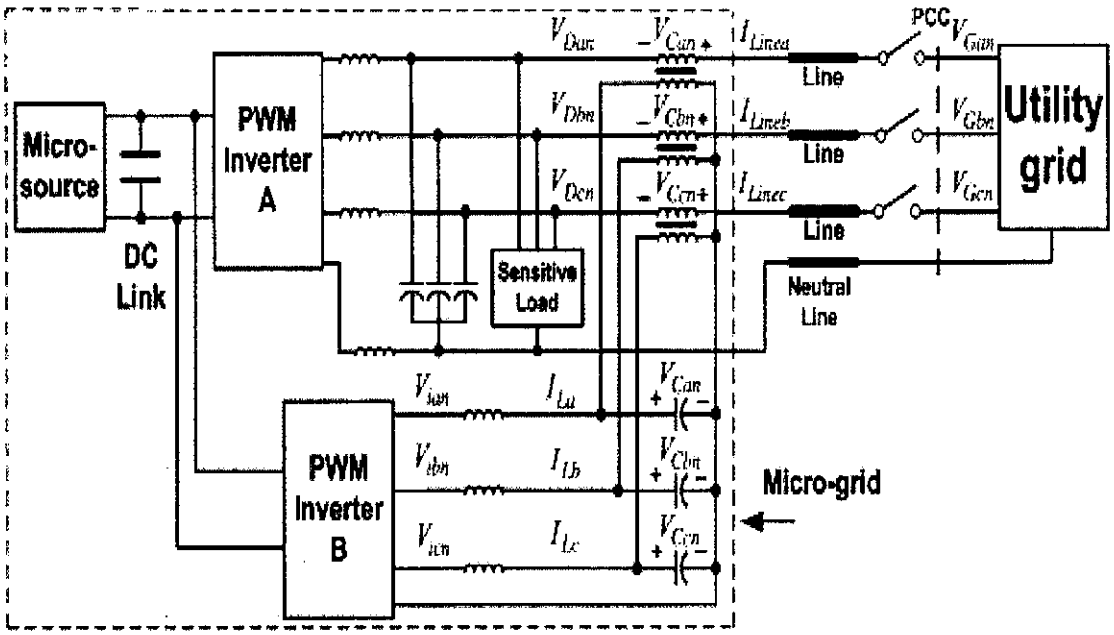


Figure 4.2 Overall system structure 3ph.4 wires

Fig. 4.2 shows the general layout of the proposed grid-interfacing power quality compensator. The compensator consists of two four-phase-leg inverters, namely inverter A (shunt) and inverter B (series). The main functions of inverter A are to maintain a set of balanced sensitive load voltages within the microgrid even under unbalanced load and grid voltage conditions, generate and dispatch power, share the power demand optimally with the other parallel-connected DG systems when the microgrid islands, and synchronize the microgrid with the utility system at the instant of connection. The main functions of inverter B are to maintain a set of balanced line currents by introducing negative- and zero-sequence voltages to compensate for the grid voltage unbalance, and to limit the flow of large fault currents during utility voltage sags.

4.3 FINAL SIMULATION CIRCUIT WITH THREE- PHASE FOUR-WIRE COMPENSATOR (ISLAND MODE)

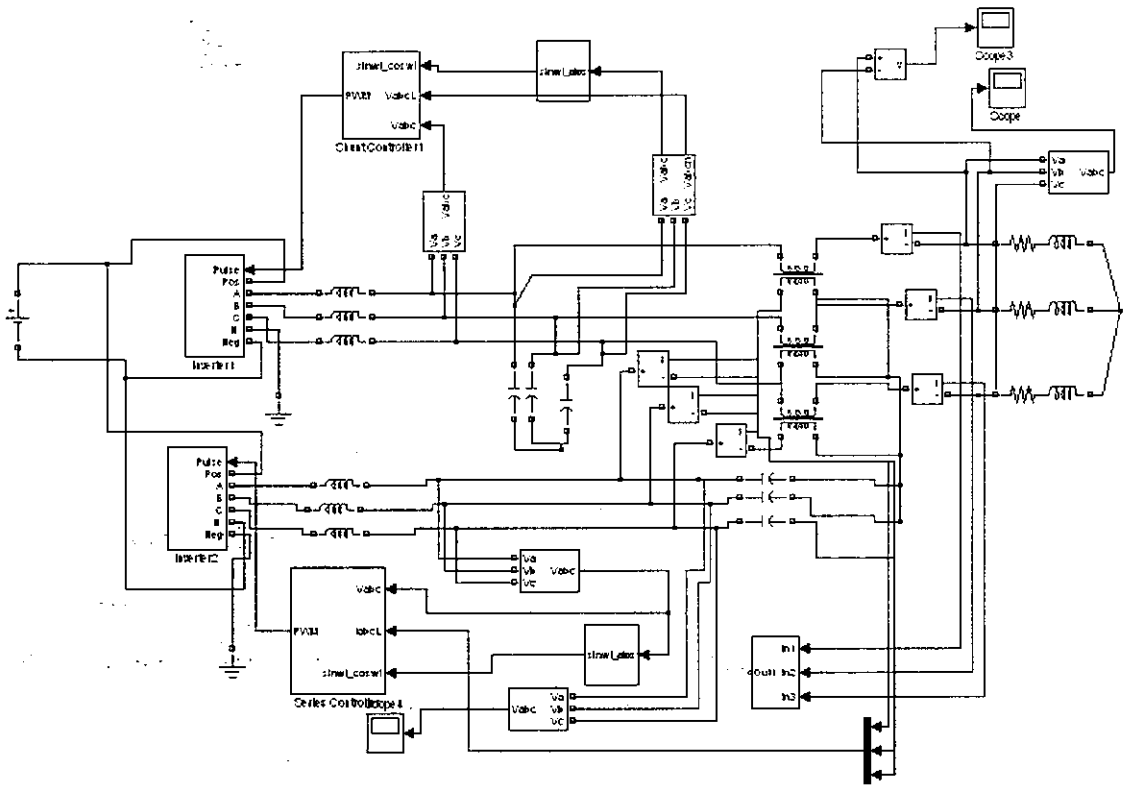


Figure 4.3 3ph. 4wire (island mode)

4.3.1 Microgrid Voltage with Balanced Load

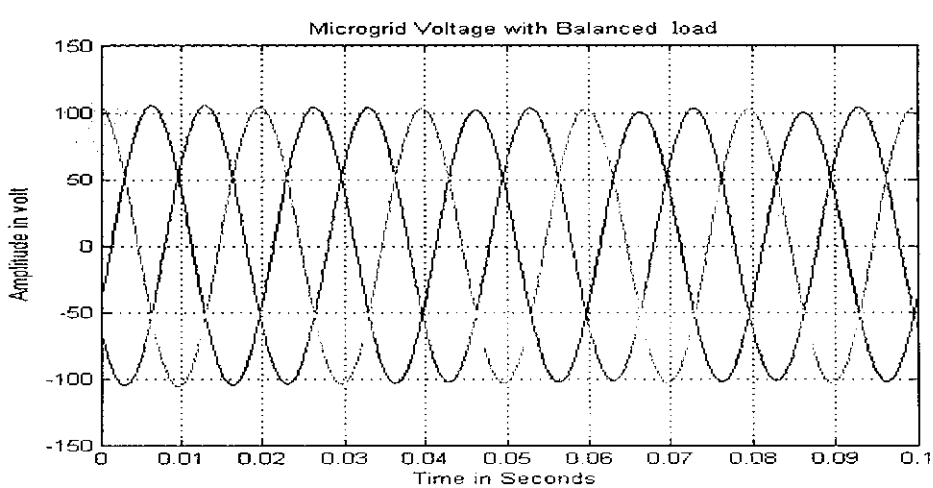


Figure 4.4 micro grid voltages with balanced load in 3ph.4 wire

4.3.2 Microgrid Voltage with Unbalanced Grid

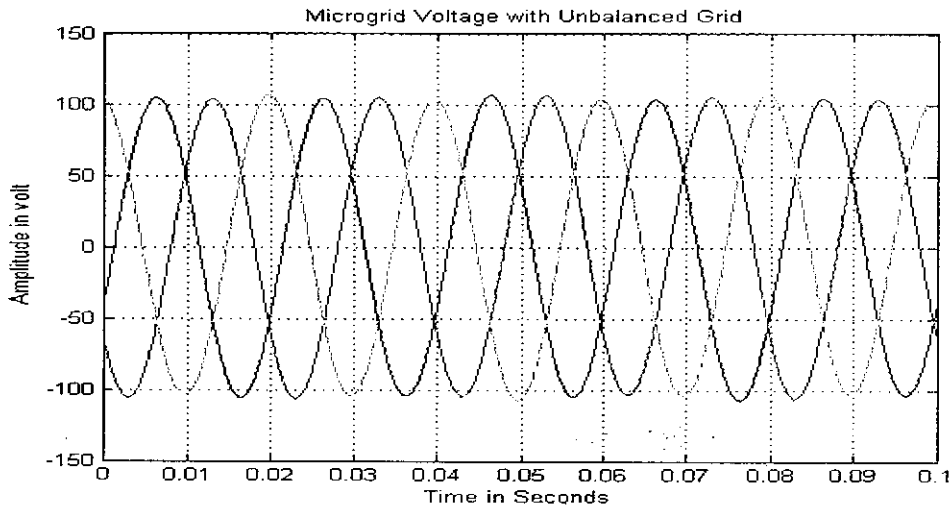


Figure 4.5 Microgrid voltages with unbalanced load in 3ph.4wire

4.4 FINAL SIMULATION CIRCUIT WITH THREE-PHASE FOUR-WIRE COMPENSATOR (GRID INTERFACING)

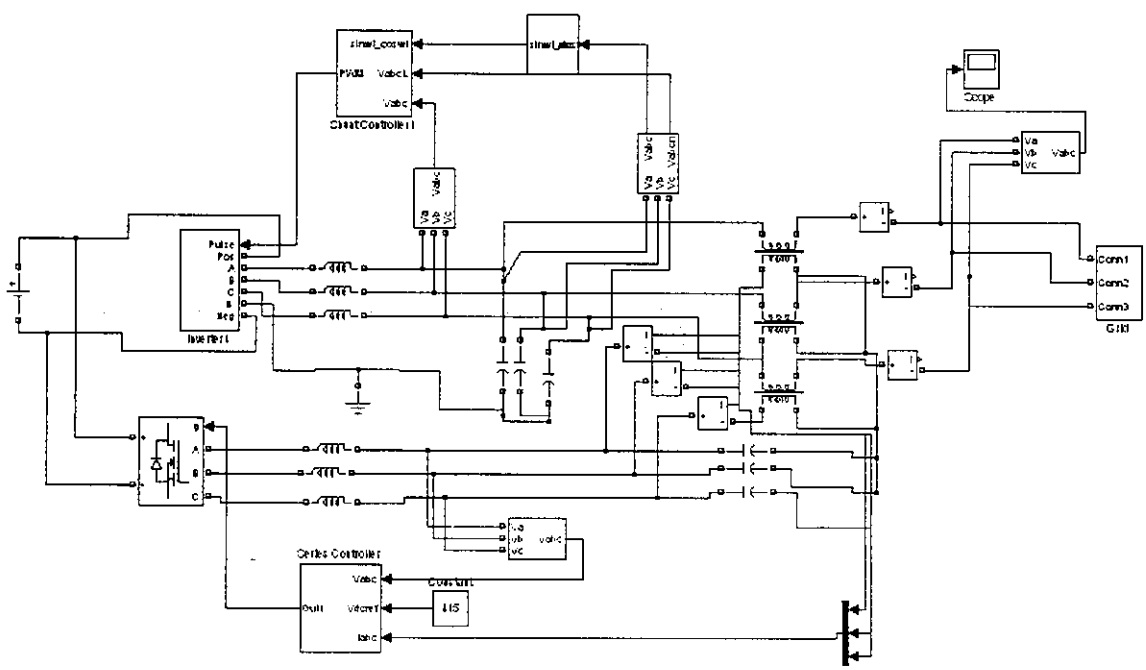


Figure 4.6 3ph.4 wires (grid interfacing)

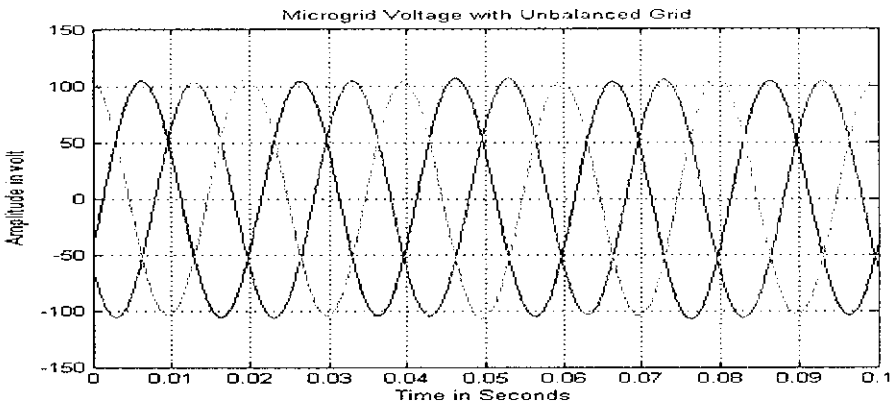


Figure 4.7 Microgrid voltage Unbalanced grid 3ph.4wire grid interfacing

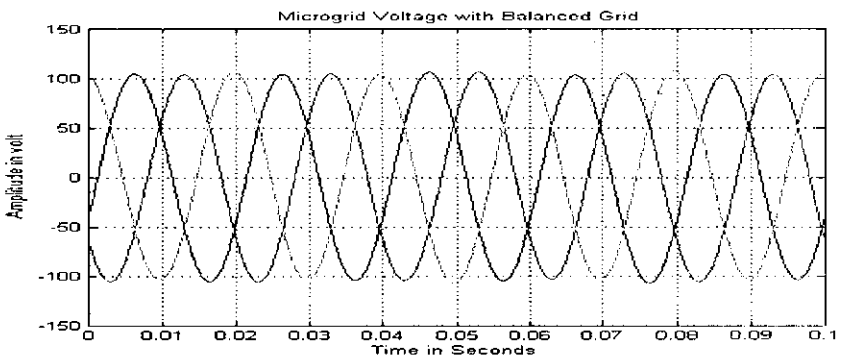


Figure 4.8 Microgrid voltages with balanced grid 3ph.4wire grid interfacing

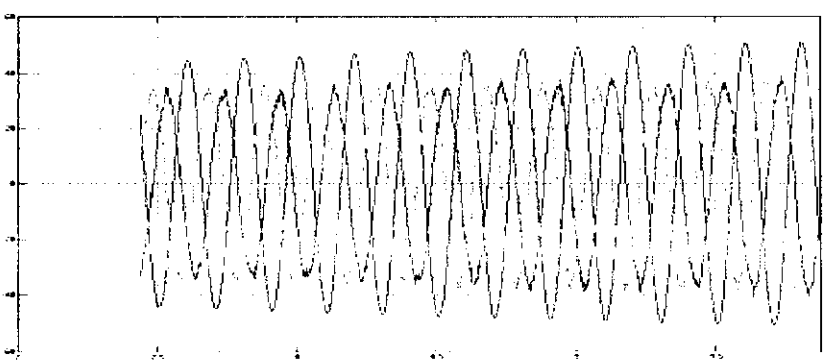


Figure 4.9 Microgrid voltages without series inverter

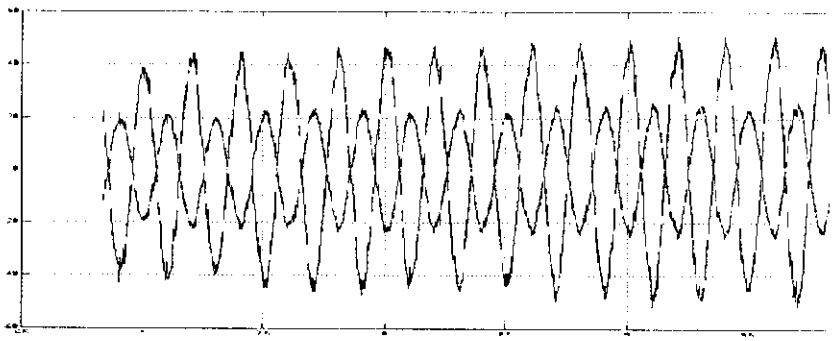


Figure 4.10 Microgrid voltages without shunt inverter

4.5 THD of 3ph.4wire

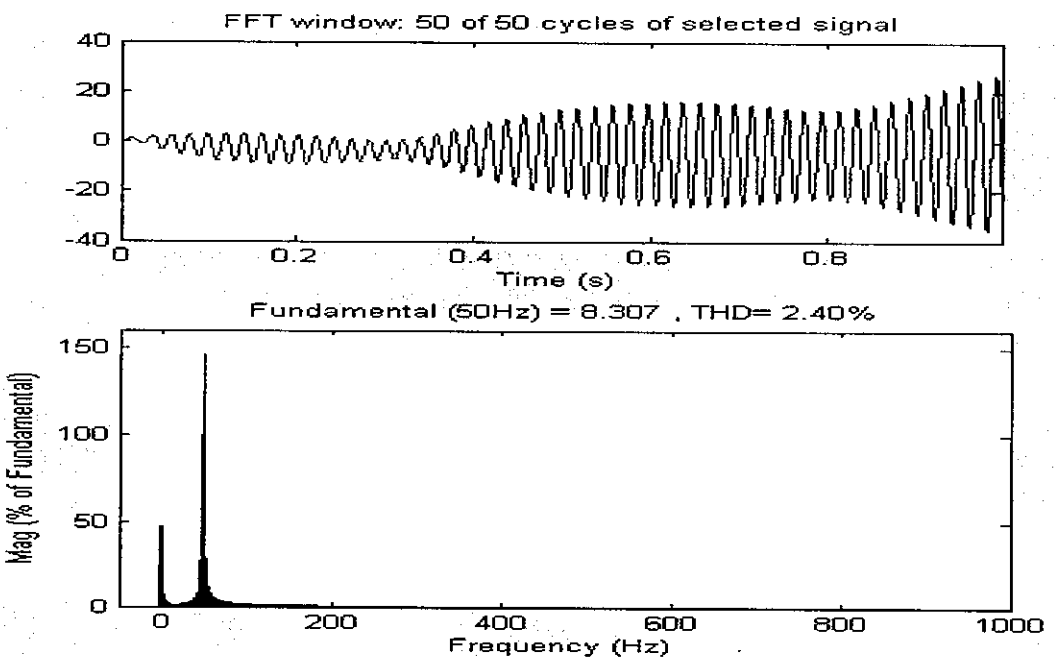


Figure 4.11 THD of 3ph.4wire

4.6 REAL AND REACTIVE POWER FROM INVERTERS

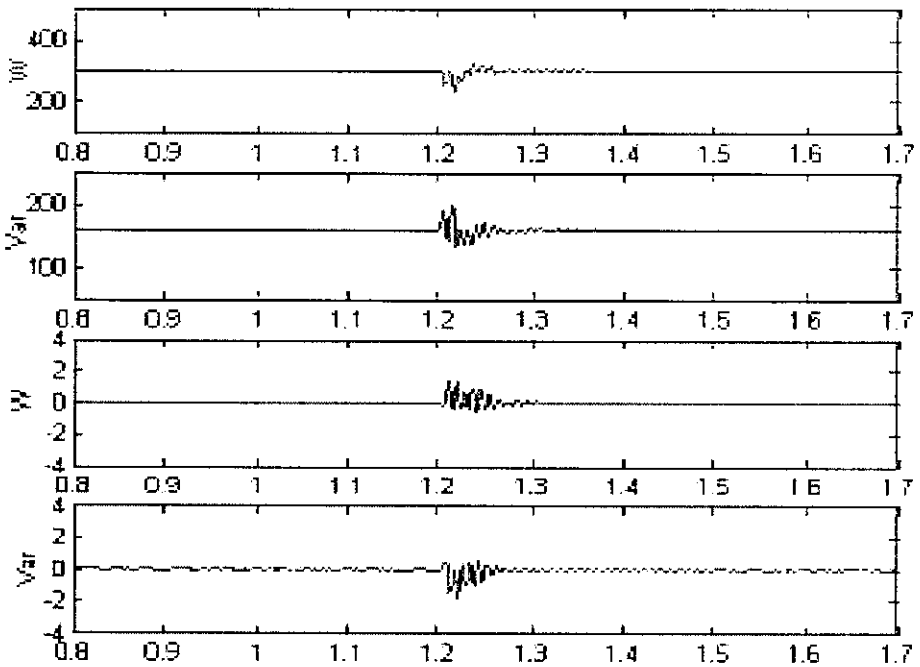


Fig..12. (a) Real power supplied by shunt inverter A, (b) reactive power supplied by shunt inverter A, (c) real power supplied by series inverter B and (d) reactive power supplied by series inverter B.

4.6 DISCUSSION ABOUT RESULT

Three-leg inverters can produce completely balanced three-phase voltages only if the Y-connected loads and filters are balanced. For sourcing power to unbalance and non-linear three-phase loads, four leg inverters have been developed. The fourth leg controls the neutral phase voltage and does not conduct any neutral currents. Through this, the four-leg inverter can produce three independent output voltages, regardless of loading.

Control goals – voltage control

Low steady state error

Low THD

Robust to load disturbances

Unbalanced load can connect

CHAPTER V

HARDWARE SYSTEM

This chapter explains the block diagram and components used for the hardware prototype of the proposed system. It includes the photographs of the fabricated model and wave forms.

5.1 GENERAL LAYOUT OF PROPOSED SYSTEM

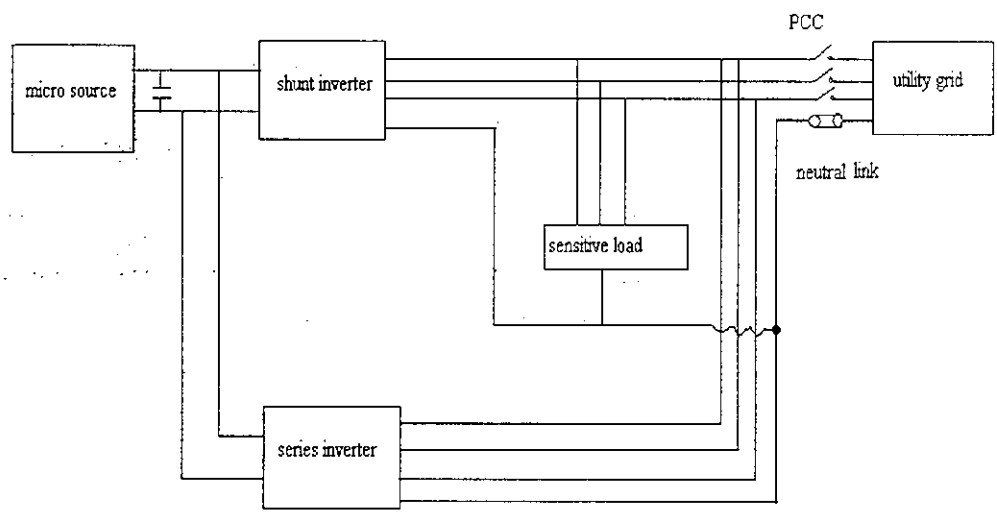


Fig 5.1 General Layout of proposed system

Instead of utility grid where variable voltage occuares due to load change, a 230V autotransformer is used to varying the depended on load.

5.2 OBJECTIVES OF HARDWARE

- Generate the same amount of AC voltage at the RELAY output ,how much reduction is occurred in the auto transformer output (grid)

5.3 BLOCK DIAGRAM OF THE PROPOSED HARDW

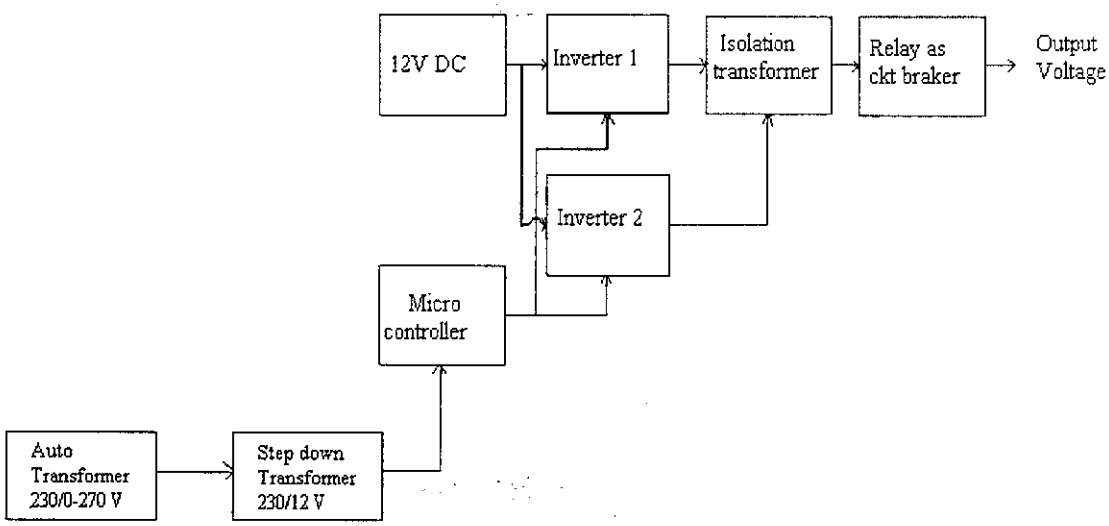


Fig 5.2 Hardware Block Diagram

5.4 BLOCK DIAGRAM DESCRIPTION:

The entire system can be divided into the following sub-systems for the easiness of understanding.

- 12V DC source
- 230 1ph AC supply
- Series inverter (inverter 1)
- Shunt inverter (inverter2)
- Isolation transformer
- Autotransformer (230/0-270 V)
- PIC micro controller
- Relays
- Optocoupler

The Figure 5.2 shows the experimental setup used in this project. The 1-ph supply is given through an auto transformer 230/0-270 V to a step down transformer 230/12 V. This 12 V ac voltage represents grid supply. It is directly given to the

microcontroller.If the autotransformer output varies; the step down voltage also varies. This variation sensed by the microcontroller .According to this variation the generating pulse width also varies. The conduction angle of MOSFETS in the inverters varied by this pulse width. Thus the inverter output changed. The two inverters are connected to the load through isolation transformer and relay. One inverter as shunt and one as series. The output of two inverters are added and get at relay output..The 12V DC source, which represents microsource (windmill, PV...etc) output is connected to the load through inverter 1.The microsource voltage is here considering as fixed ie12V DC.

5.5 PRINCIPLE OF OPERATION

The microcontroller checks the autotransformer output value to a fixed value, here that constant is 230.IF the supply is 230, then difference is zero. This time relay becomes open and two inverters are open. Now the relay output voltage is zero. If the supply voltage reduces below 230 the difference is positive and PWM duty cycle varies. If the difference is negative or zero the relay become open .Thus the PIC micro controller is generating pulses for the inverters according to the feedback signals from grid voltage.

Relay Operation

1	Grid Voltage	> =230V	No relay operation Inverter 1,2 OFF
2	Grid Voltage	< 230V	Relay circuit close Inverter 1,2 ON
3	Grid Voltage	<230V and decreases	Inverter output voltage increases
4	Grid Voltage	< 230 V and increases	inverter output voltage decreases

Table 5.1

5.6 DESIGN OF REGULATED POWER SUPPLY CIRCUIT:

This section introduces the operation of power supply circuits built using filters,

rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig. The ac voltage, typically 230V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

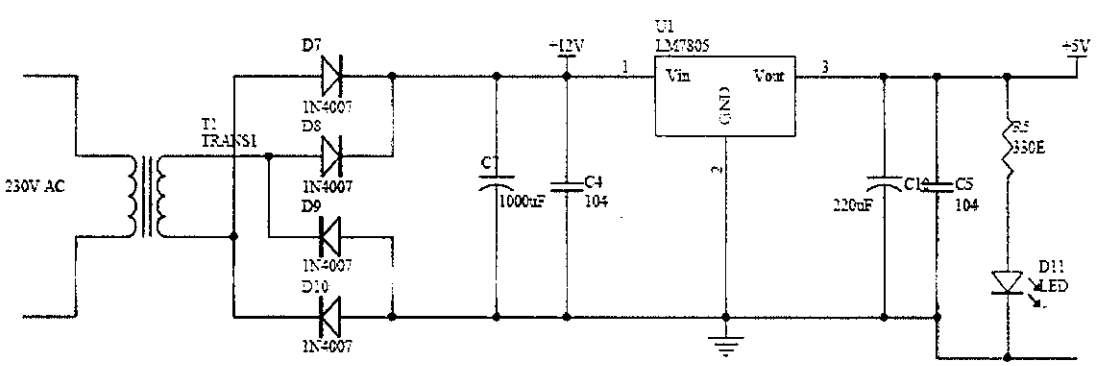


Figure 5.3 +5 V Power supply for PIC controller.

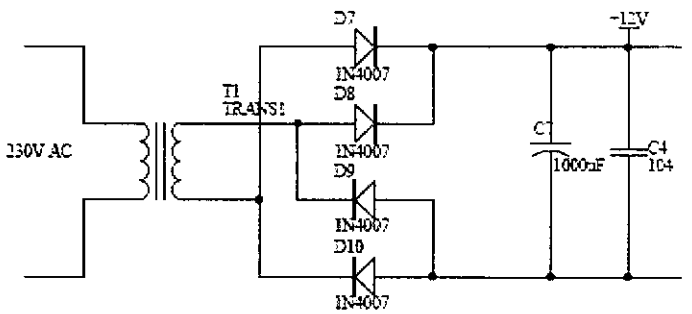


Figure 5.4 +12 V Power supply for Relay.

The 78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid-state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents. The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating. Considerable effort was expanded to make the 78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply. For output voltage other than 5V, 12V and 15V the 117 series provides an output voltage range from 1.2V to 57V. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output

current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

5.6.1. Step down transformer:

Alternating current of 230V, 50 Hz supply is given to the primary side of the step down transformer of 230V/ 0-12V type to perform step down operation. The current rating of the transformer is 1A. Now this can be used for rectification purpose.

5.6.2. Rectifier unit:

Rectification is achieved using a full bridge rectifier circuit, which comprises of four 1N 4007 solid-state diodes. Two diodes will conduct during the positive cycle and the other two will conduct during the negative half cycle. The output obtained is not a pure DC and therefore filtration has to be done.

5.6.3. Filtering unit:

Filter circuits usually consist of a capacitor, which smoothens the pulsating DC. It is helpful in reduction of the ripples from pulsating (1000μF/ 25V) and it maintains stability at the load side (10μF/ 25V).

5.6.4. Voltage regulators:

Voltage regulators play an important role in any power supply unit. The primary purpose of a regulator is to aid the rectifier and filter circuit in providing a constant DC voltage to the device. Power supplies without regulators have an inherent problem of changing DC voltage values due to variations in the load or due to fluctuations in the AC line voltage. MC 7805 and MC 7812 are used to provide +5V and +12V regulated DC supply respectively.

Features

- Output current in excess of 1A
- Internal thermal overload protection

- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

5.7. MOSFET-FULL BRIDGE INVERTER:

Here three phase full bridge inverter is used for both shunt and series inverters. Each inverter needs six MOSFET. The circuit connection of the full -Bridge inverter is shown in figure.

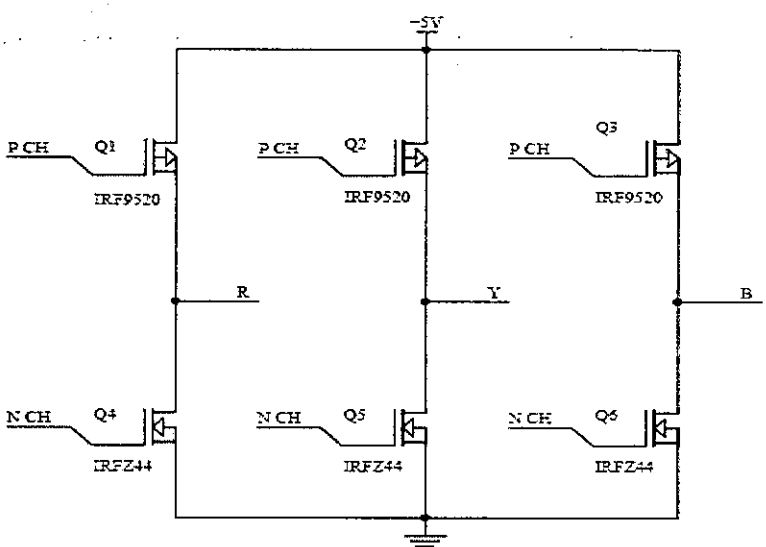


Figure 5.5 3ph full bridge inverter using MOSFET

5.7.1 Advantages of MOSFET:

MOSFETs provide much better system reliability.

- Driver circuitry is simple and cheaper.
- MOSFET's fast switching speeds permit much higher switching frequencies and there by the efficiency are increased.

- Overload and peak current handling capacity is high.
- MOSFETs have better temperature stability.
- MOSFET's leakage current is low.
- Drain-source conduction threshold voltage is absent which eliminates electrical noise.

MOSFETs are able to operate in hazardous radiation environments. Here three P channel IRF9520 MOSFET and three N channel IRFZ44 MOSFETs are used to construct the 3ph full bridge inverter. A power supply of +5 V DC supplied through a voltage regulator.

5.8 PHOTOTRANSISTOR OPTOCOUPLER:

A phototransistor optocoupler is a combination of a light source and a photosensitive detector. In the optocoupler, or photon coupled pair, the coupling is achieved by light being generated on one side of a transparent insulating gap and being detected on the other side of the gap without an electrical connection between the two sides (except for minor amount of coupling capacitance). In the optocoupler, an infrared light emitting background generates the light, and the photo-detector is a silicon diode, which drives and amplifies, example transistor. The sensitivity of the silicon material peaks at the wavelength emitted by the LED, giving maximum signal coupling.

5.8.1. Phototransistor optocoupler MCT2E:

These high-speed optocouplers are designed for use in analog or digital interface applications that require high voltage isolation between the input and output. The MCT2XXX series opto isolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in –line package. Applications include line receivers that require high common mode transient immunity and analog or logic circuits that require input-to-output electrical isolation. The MCT2E each

consist of light emitting diode and an integrated photon detector composed of a photodiode and an open-collector output transistor. Separate connections are provided for the photodiode bias and the transistor collect output. This feature reduces the transistor base to collector capacitance, result in speed up to one hundred times that of a conventional phototransistor optocoupler. The MCT2E is designed for wide-band analog applications. The optocoupler schematic diagram is shown the figure.

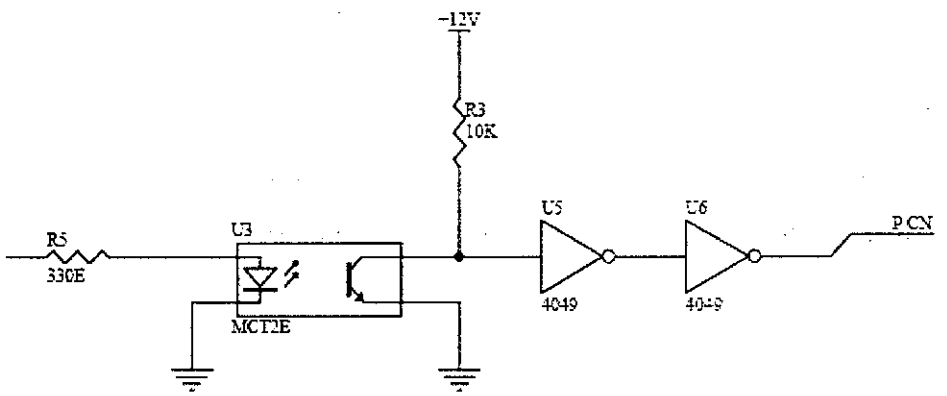


Figure 5.6 Driver Circuit for P-channel MOSFET

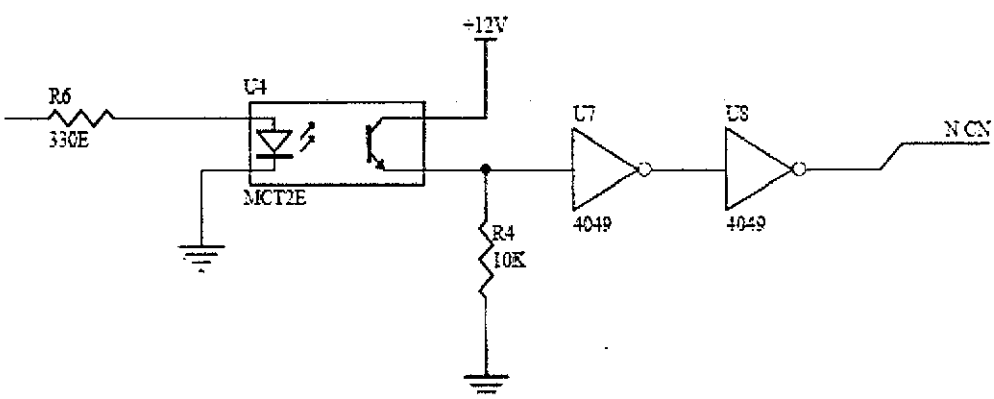


Figure 5.7 Driver Circuit for N-channel

5.9 PULSE GENERATING CIRCUIT:

PIC16F877A micro controller is used as the pulse generating circuit. PIC16F877A is a 40pin; CMOS flash micro controller with A/D controller. It has five I/O ports and has fifteen interrupts. In addition, it has eight A/D channels and the parallel port is implemented in it.

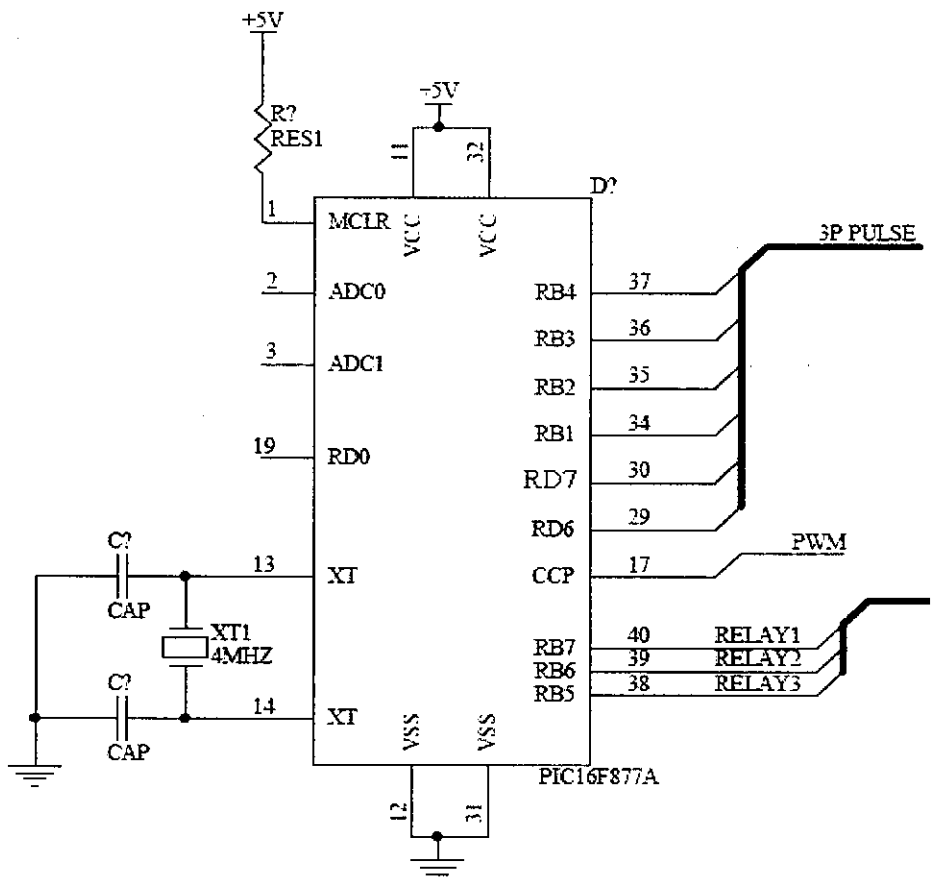


Figure 5.8 Pin configuration used for pulse generation in PIC controller

Pin number 1 is master clear. It is given by +5V supply. Port A is a bi-directional I/O port. Here we configure it as input channel. The potential transformer feedback signals are given as inputs. Port D is also a bi-directional I/O port and configures it as input pin. Here we use a crystal oscillator is connected; whose frequency is 4MHz. Pin number 13 and 14 is used for this purpose. Pin numbers 12 and 31 are the ground reference for logic and I/O pins. So we ground those pins. Pin

numbers 11 and 32 are the positive supply for logic and I/O pins. Therefore, we connect +5 V across it. Port B is also a bi-directional port and we configure it as output port. RB1-RB3 configured as output pins to output the PWM pluses. Port D is also a bi-directional port and we use RD6 and RD7 as output pins for PWM pulses. Pins RB5-RB7 used as output pins for the controlling pulses for the relay circuit. Pin number 17 is RC2 which is a bi-directional pin used here as PWM output enable.

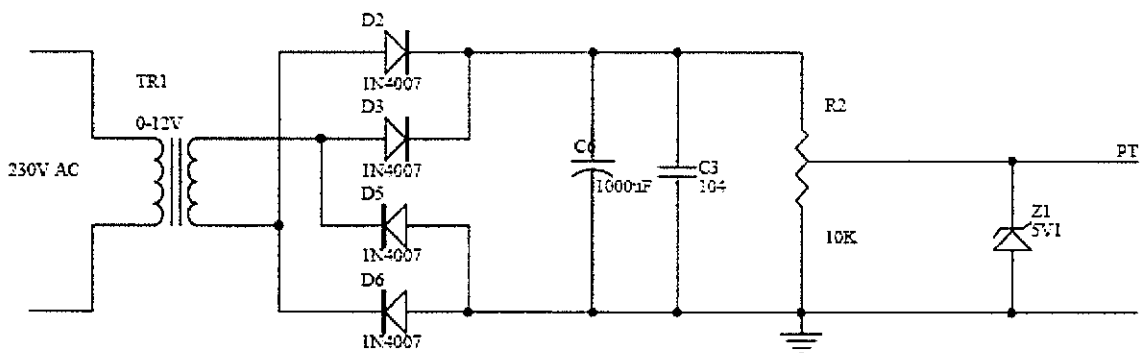


Figure 5.9 Feedback Signal for PIC controller

5.9.1 PWM MODE:

In pulse width modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORT C data latch, the TRISC 2 bit must be cleared to make the CCP1 pin an output. The Block Diagram of the PWM Mode and the PWM output is given below:

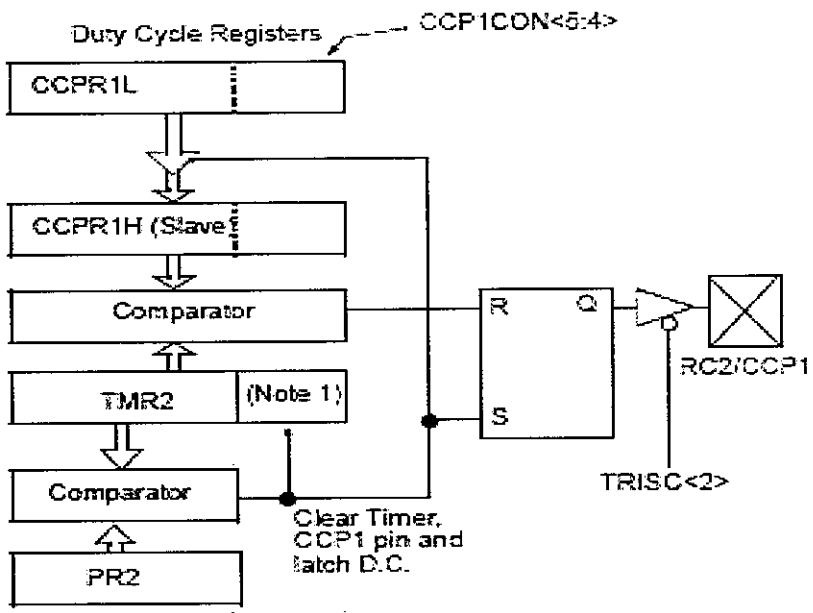


Figure 5.10 Functional Block Diagram of PWM operation

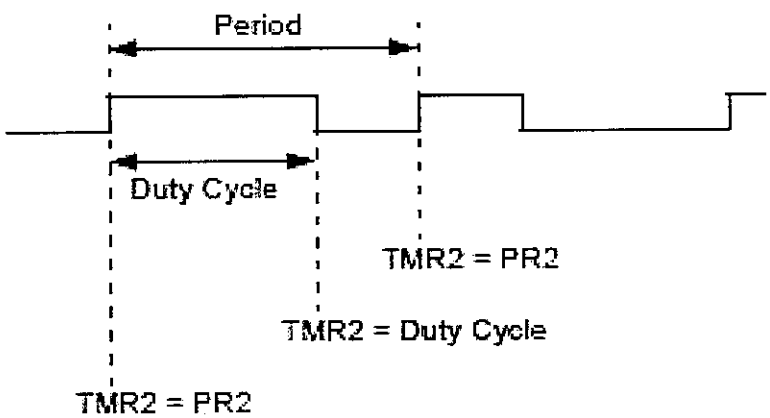


Figure 5.11 PWM output

A PWM output has a time-base (period) and a time that the output has high (duty cycle). The frequency of the PWM is the inverse of the period (1/period). The PWM period is specified by writing to the PR2 register. The PWM period is calculated using the following formula:

PWM period = [(PR2) + 1] * 4 *TOSC

5.9.2 PWM DUTY CYCLE:

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON 5, 4 bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSBs and the CCP1CON5, 4 contains the two LSBs. This 10-bit value is represented by CCPR1L: CCP1CON 5, 4. The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L: CCP1CON 5, 4) * Tosc * (TMR2 prescale value)

CCPR1L and CCP1CON 5,4 can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register. The following steps should be taken when configuring the CCP module for PWM operatio:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON 5, 4 bits
3. Make the CCP1 pin an output by clearing the TRISC 2 bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

5.10 RELAY:

The relay circuit used in this hardware implementation is as shown in figure. There are four relays used, on which two are single pole and other two are double pole. Relays are remote control electrical switches that are controlled by another switch such as computer as in a power train control module. They allow a small current flow circuit to control a higher current circuit. Relay has two circuits, a control circuit and a load circuit. Control circuit has a small control coil while the load circuit has a switch. The coil controls the operation of the switch. When current passes through control coil, an electromagnetic field produce and switch is close.

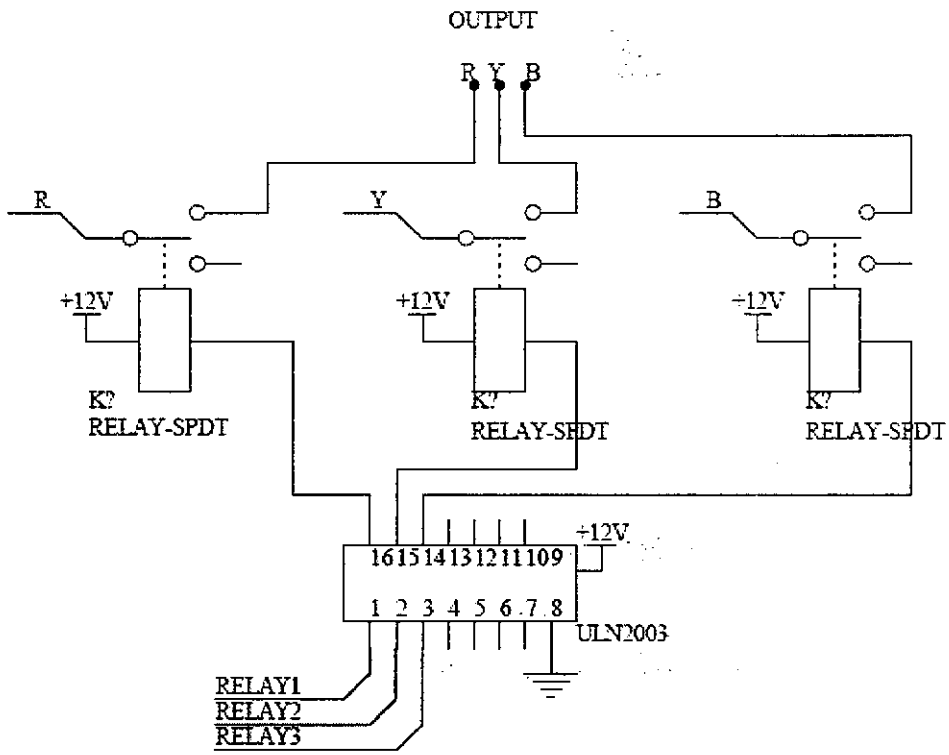


Figure 5.12 Circuit diagram for the relay operation

Decision Table

Normal	All Relay OFF
Decision 1	Relay1,2,3 ON

Table 5.2 Relay operation Decision

5.10.1 Driver circuit for Relay operation:

In order to amplify the pulses from the PIC controller to the power level, we are using driver circuit for relay. Here we are using ULN2003A Darlington pair for this purpose. It is seven Darlington per pack. The output current is 500mA per driver and output voltage is 50 they are 16-pin pack with copper lead frame to reduce the thermal resistance. The connection diagram of relay with the driver circuit is as shown in fig 5.13

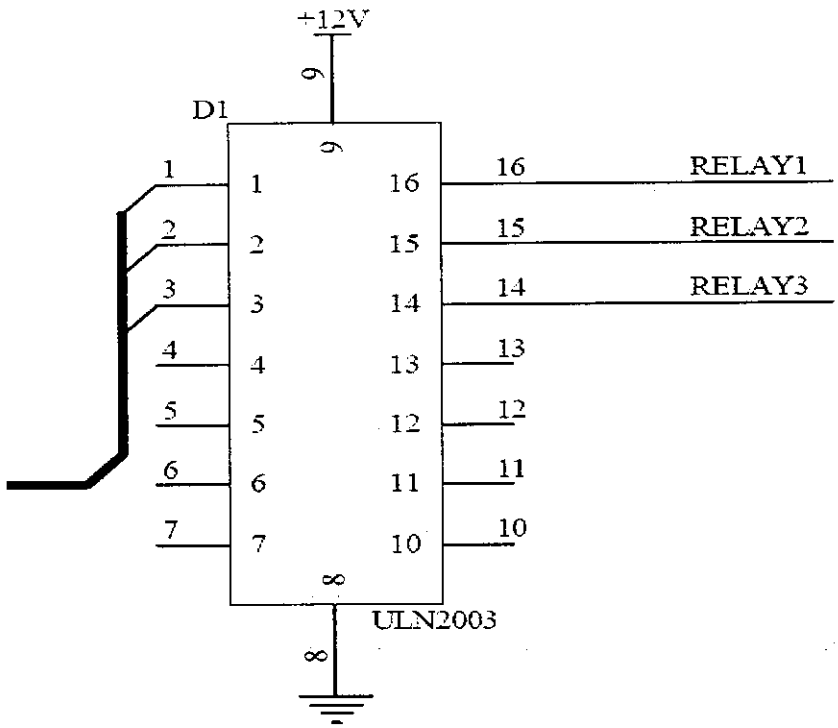


Figure 5.13 Driver circuit for relay operation

Here pins 1-3 are input pins which are connected to the PIC output pins. Pin 14-16 are output pins which are connected to the relay coil. Pin 8 is logic ground for the circuit. Pin 9 is positive power supply for the ULN2003 which is connected by a +12 V DC supply.

5. 11 MOSFET DRIVE

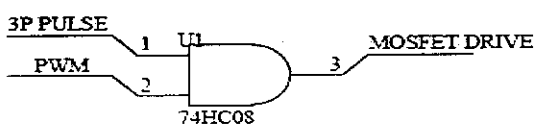


Figure 5.14 MOSFET Drive

The AND gate(7408) is used for multiplexing the three phase pulses generated by PIC controller and the internal PWM .Its inputs are 3ph. Pulses and PWM pulses. Output is to the MOSFET drive.

5.12 FLOW CHART OF THE MICROCONTROLLER OPERATION IN PWM INVERTER AND RELAYS

Circuit diagram for the relay operation

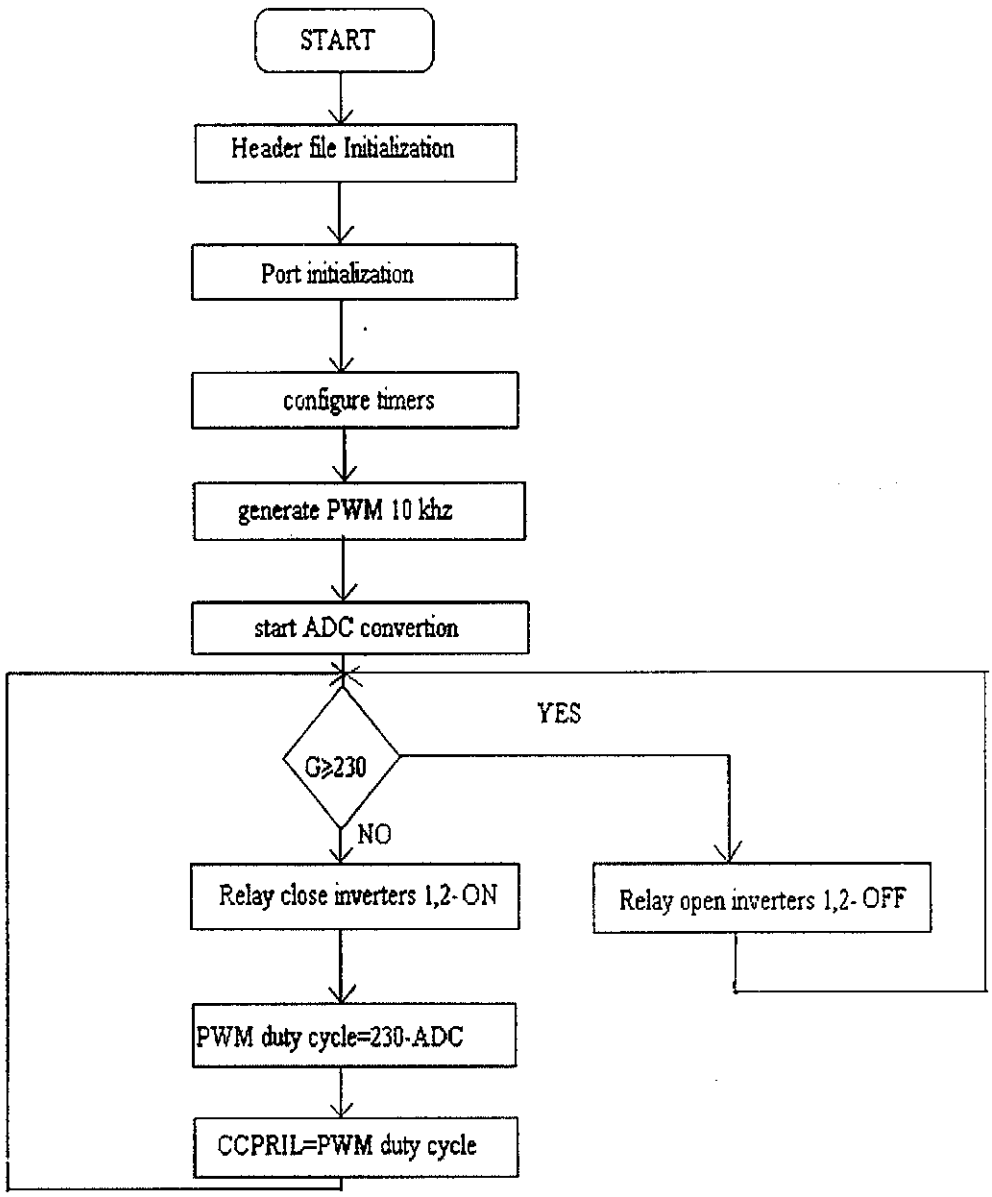


Figure 5.15 Flow chart of Microcontroller operation

5.13 HARDWARE TESTING RESULTS:

The hardware is fabricated and tested. The following table shows the test result.

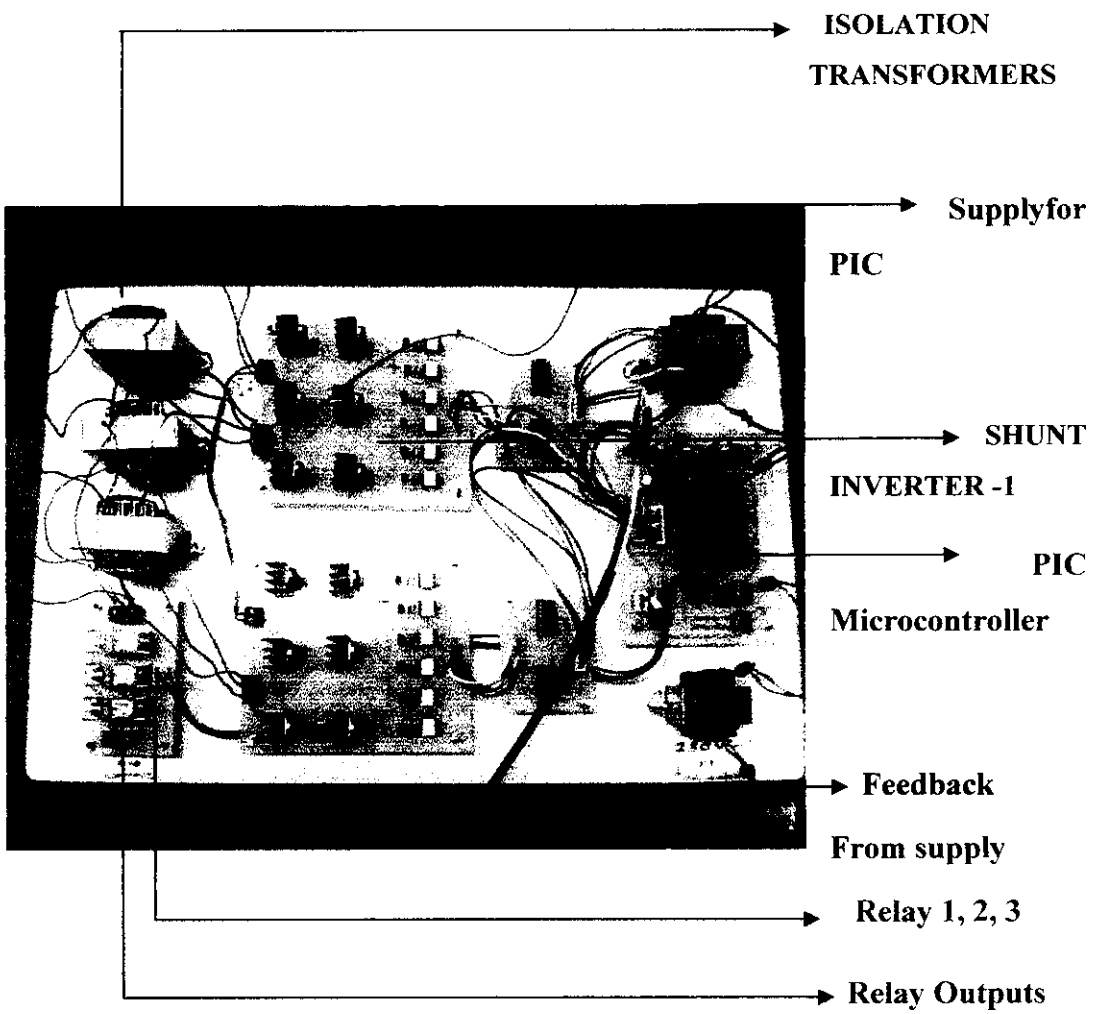


Figure 5.16 Hardware board

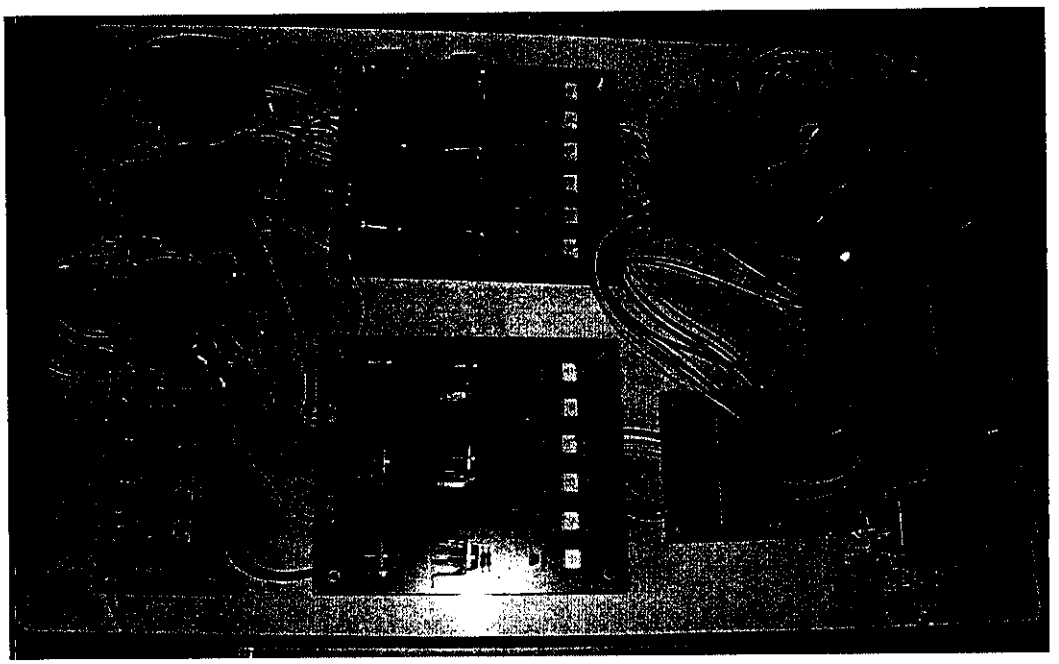


Figure: 5.17. Hardware board

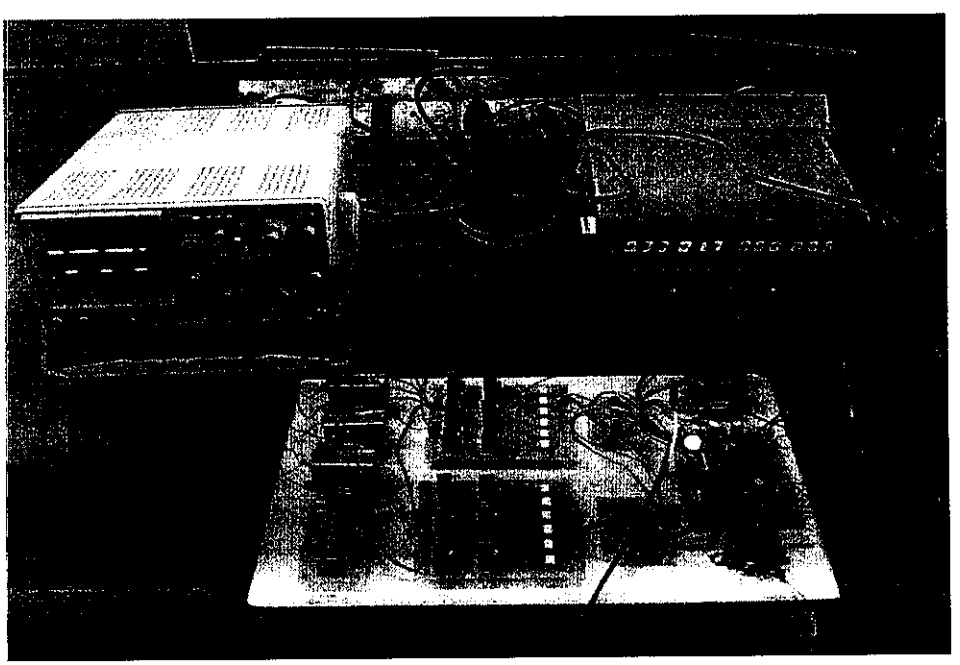
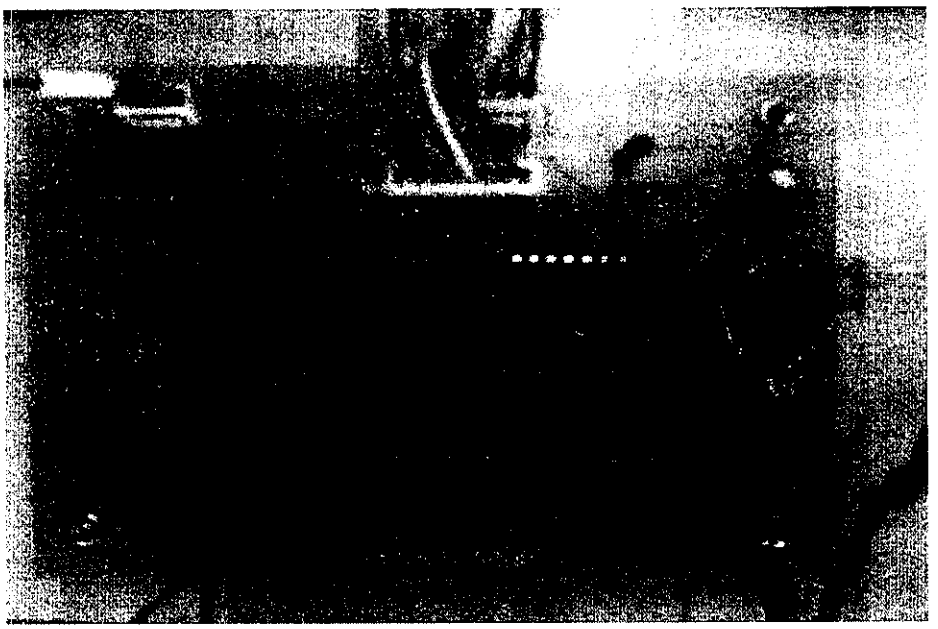


Fig 5.18 Hardware full setup



5.19Pic micro controller board

Fig 5.20 Inverter

Figure: 5.21 Relay

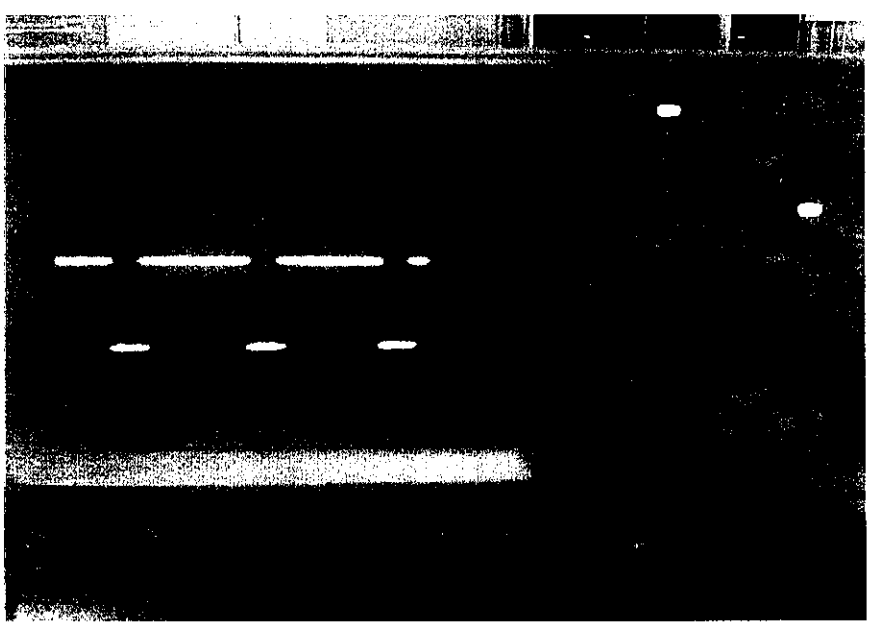


Fig 5.22generated triggering pulses 1

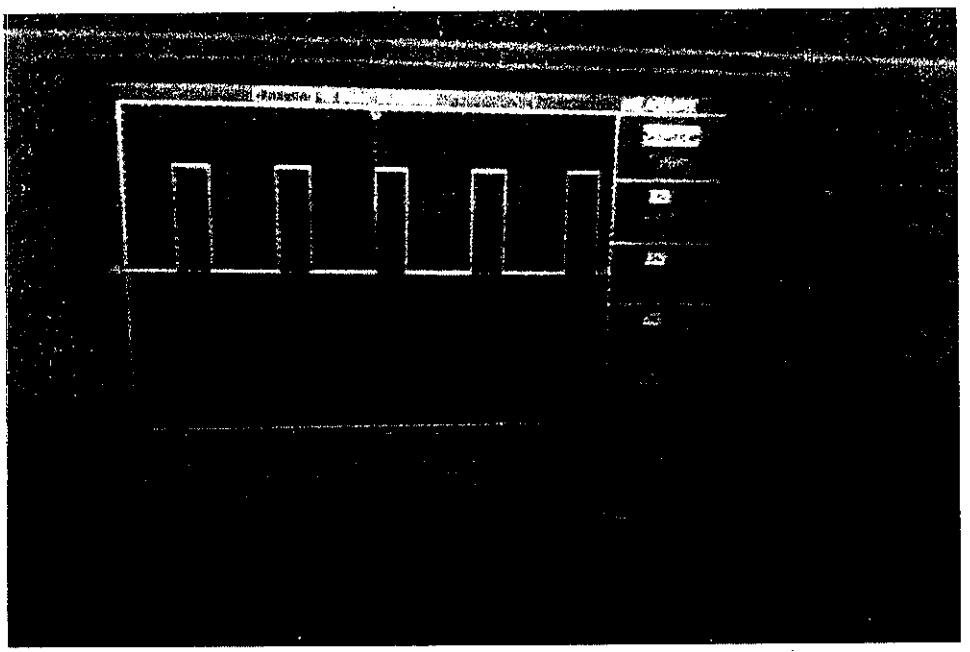


Fig 5.23 Generated triggering pulses 2

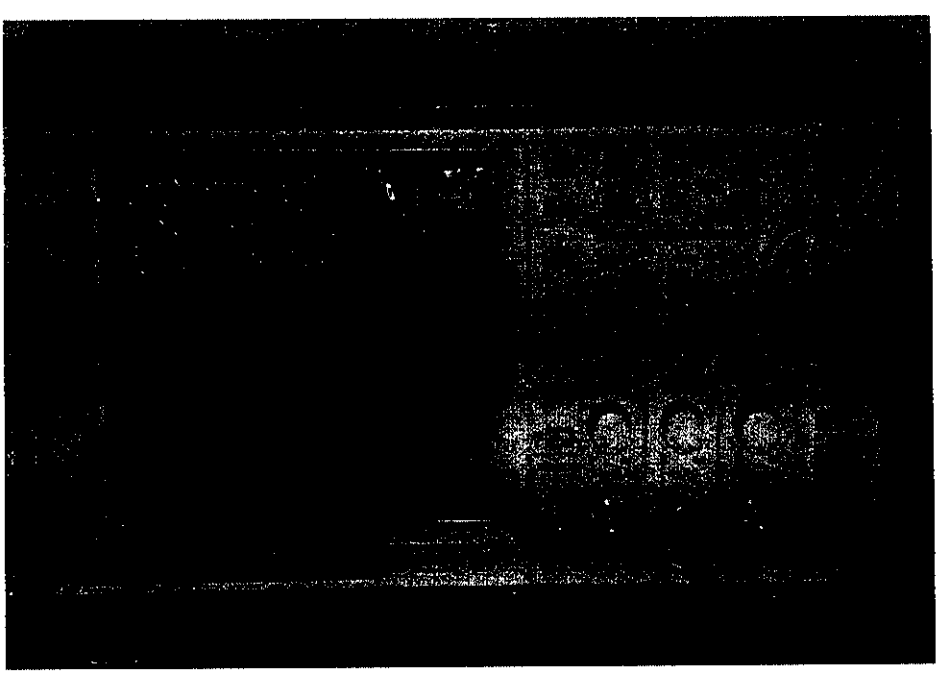


Figure 5.24 Inverter Output

CHAPTER VI

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

This project presents a three-phase four-wire grid-interfacing power quality compensator for compensating the most common voltage quality problem namely voltage unbalance in a microgrid. During grid voltage unbalance, the proposed compensator, using a shunt and a series four phase- leg inverter, can enhance both the quality of power within the microgrid and the quality of currents flowing between the microgrid and utility system. Functionally, the shunt four-leg inverter is controlled to maintain a set of balanced distortion free voltages within the microgrid and to regulate power sharing among the parallel-connected distributed generation (DG) systems. To complement, the series four-leg inverter is controlled to inject negative- and zero-sequence voltage in series to balance the line currents, generating zero real and reactive power during compensation. The proposed system has been tested in simulations and compared with the simulation result of three phase three ware system. A laboratory prototype developed and tested.

6.2 FUTURE SCOPE

With slight modification in control strategy of the pulse modulation of the inverter it can becomes a power conditioner for reducing harmonics thus improving the power quality. To assess the steady state behavior of different three phase voltage source inverters for microgrid, that work either off grid or grid connected with the main focus being on how this converters handle.

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APPENDIX

APPENDIX A: PIC16F877A

FEATURES OF PIC16F877A

High-Performance RISC CPU:

- Only 35 single word instructions to learn.
- All instructions are 1μs (@4MHz) except for program branches, which are 2 cycles.
- Operating speed: DC - 20MHz clock input.

Peripheral Features:

- Two 8-bit timer/counter (TMR0, TMR2) with 8-bit programmable prescaler.
- One 16-bit timer/counter (TMR1)
- High source/sink current: 25ma
- 12.5 ns resolution for PWM mode.
- Two Capture/Compare PWM (CCP) Modules.
- Brown-out detection circuitry for brown-out Reset (BOR).
- Synchronous serial port (SSP) with SPI (Master mode) and I2C (Master/slave mode).
- Universal synchronous asynchronous receiver/transmitter (USART/SCI) with 9-bit address detection.

Special Micro controller Features

- Power-On Reset Power-up Timer (PWRT) and Oscillator
- Selectable oscillator options.
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation.
- Self-reprogrammable under software control.
- Power saving Sleep mode.

CMOS Technology

- Fully static design
- Low power, high speed CMOS FLASH technology
- Wide operating voltage range: 2.0V to 5.0V

- < 0.6 mA typical @ 3V, 4MHz.

Timing diagram for the generation of pulse by using micro-controller, PIC 16F877A

- For generating the pulse, timer 1 of PIC16F877A is used.
- The first two sequences are repeated for every 10m
- The last sequence is repeated for every 20ms.
- Whenever the timer 1 is overflow, an interrupt is generated.
- That time, a count variable is increased.
- This count value will be compared with the predefined variable.
- If the present count value is greater than the predefined one, then the pulse will be generated.
- The timer1 is set to overflow for every 0.5ms.

PIN CONFIGURATION OF PIC16F877:

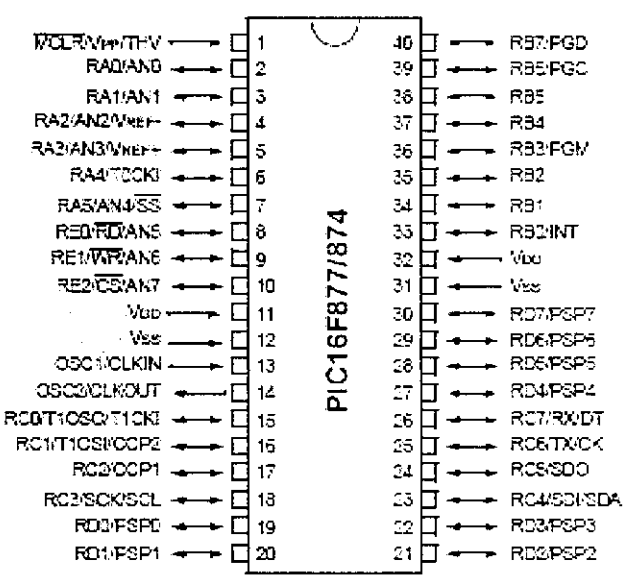


Fig 5.5 Pin diagram of PIC 16F877

MEMORY ORGANIZATION:

The PIC16F877 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F877 devices have 8K x 14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h

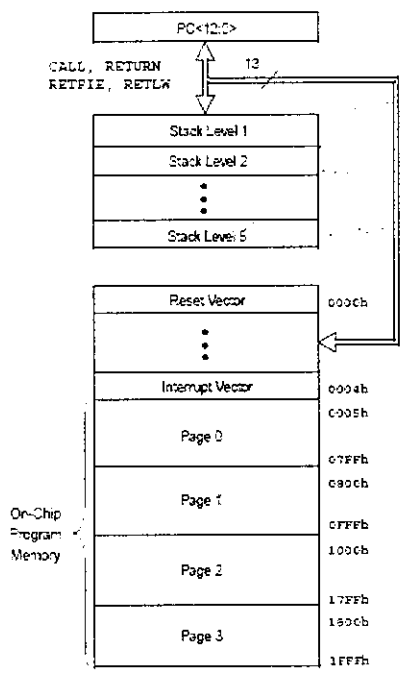


Fig 5.6 Memory Organization of PIC 16F877

FLASH PROGRAM MEMORY:

The Data EEPROM and FLASH Program Memory are readable and writable during normal operation over the entire VDD range. The data memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (SFR). There are six SFRs used to read and write the program and data EEPROM memory.

These registers are:

- EECON1
- EECON2

- EEDATA
- EEDATH
- EEADR
- EEADRH

The PIC 16F877 also has three timers namely:

- Timer 0 Module
- Timer 1 Module
- Timer 2 Module

TIMER 0 MODE:

Timer mode is selected by clearing bit T0CS (OPTION_REG 5). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler).Counter mode is selected by setting bit T0CS (OPTION_REG 5). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE of (OPTION_REG 4). Clearing bit T0SE selects the rising edge. The prescaler is mutually exclusively shared between the Timer0 module and the watchdog timer.

TIMER 1 MODE:

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L), which are readable and writable. The TMR1 Register pair (TMR1H: TMR1L) increments from 0000h to FFFFh and rolls over to 0000h.Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON 1).In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON 0).

TIMER 2 MODE:

Timer 2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device reset. The Timer2 module has an

8-bit period register PR2.Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

CAPTURE/COMPARE/PWM MODES:

Each Capture/Compare/PWM (CCP) mode contains a 16-bit register, which can operate as, a :• 16-bit Capture register

- 16-bit Compare register
- PWM master/slave Duty Cycle register

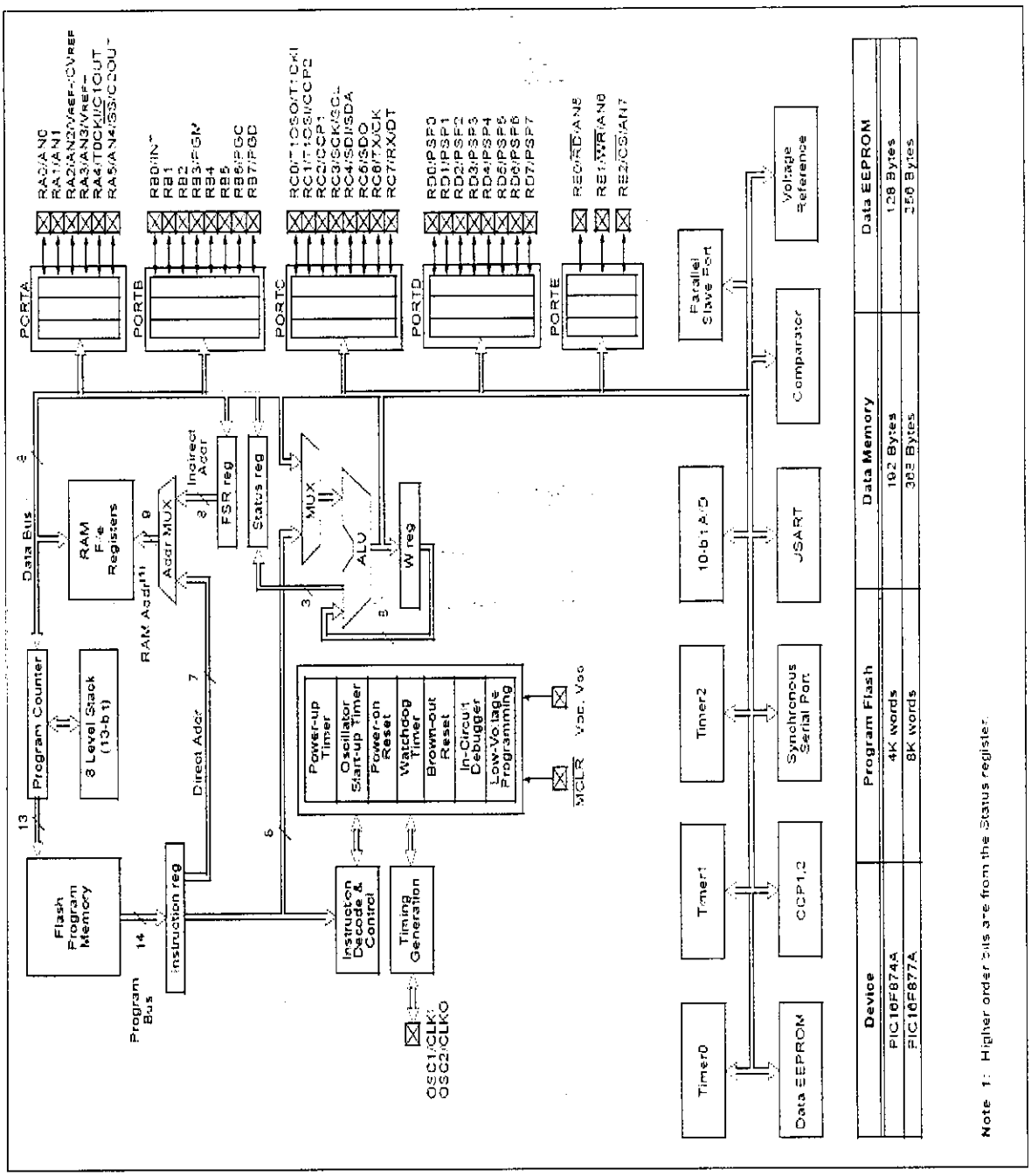
Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger.

CCP 1 MODE:

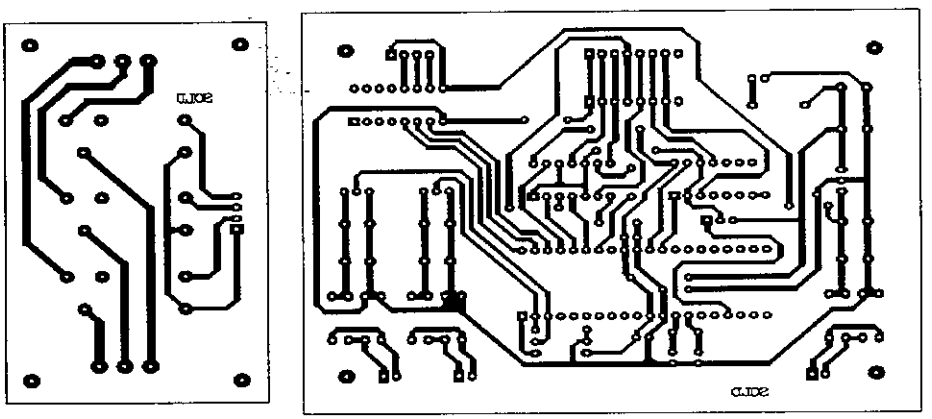
Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

CCP 2 MODE:

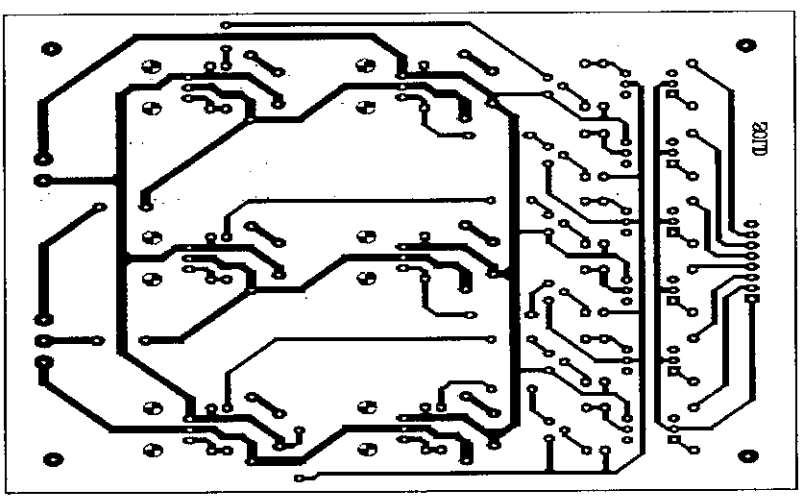
Capture/Compare/PWM Register 2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer 2 and start an A/D conversion.



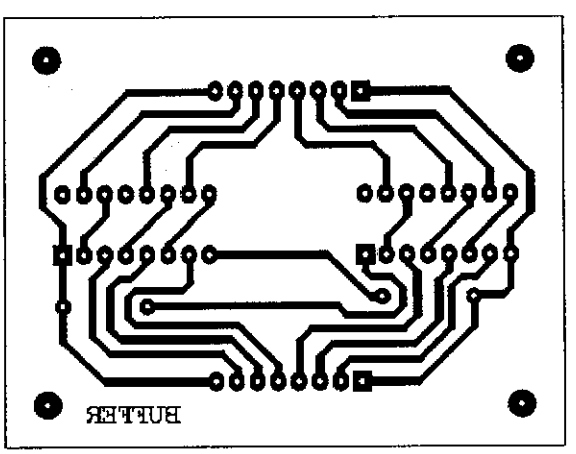
Block diagram of 16F877A



Controller PCB



Inverter PCB



Buffer PCB

APPENDIX B: PIC PROGRAMMING:

```
#include<pic.h>

unsigned char count=0,d_cycle,set_f[5]={0};

unsigned int ADRES=0;


#define RELAY1 RB5

#define RELAY2 RB6

#define RELAY3 RB7


#define S1 RB1

#define S2 RD7

#define S3 RB2

#define S4 RB4

#define S5 RD6

#define S6 RB3

__CONFIG(WDTDIS & XT & PWRTEN & BOREN & LVPDIS);

void main()

{

        ADCON1=0X8E;

        TRISA=0x01;

        TRISB=0;

        TRISD=0;

        TRISC=0;
```

```
        PORTB=0;
        PORTD=0;
        PORTA=0;
        PORTC=0;

        T1CON=0X01;                 //timer1
        TMR1H=0XF2;
        TMR1L=0XFB;

//      TMR1H=0XFF;
//      TMR1L=0XC8;

        T2CON=0X04;                 //pwm
        PR2=99;
        CCP1CON=0X0C;
        CCPR1L=d_cycle=80;

        S1=0;
        S6=1;

        GIE=PEIE=TMR1IE=1;

        while(1)
        {
                ADCON0=0X81;
```

```
delay();
ADGO=1;
delay();
while(ADGO);
ADRES=ADRESH*256+ADRESL;

ADRES=ADRES/2;



if(ADRES<230)
{
        RELAY1=RELAY2=RELAY3=1;
        d_cycle=230-ADRES;
        if(d_cycle>100)
                d_cycle=100;



}
else
{
        RELAY1=RELAY2=RELAY3=1;
        d_cycle=0;
}
CCPR1L=d_cycle;
```

```
                delay1();
        }

}
delay()
{
        unsigned char i;
        for(i=0;i<=100;i++);
}
delay1()
{
        unsigned int i;
        for(i=0;i<50000;i++);
}

void interrupt isr()
{
        if(TMR1IF==1)
        {
                TMR1IF=0;
                TMR1H=0XF2;
                TMR1L=0XFB;
//              TMR1H=0XFF;
//              TMR1L=0XC8;
```

```
count++;
if(count==1)
{
        S2=1;
        S6=0;
}
if(count==2)
{
        S1=1;
        S3=0;
}
if(count==3)
{
        S2=0;
        S4=1;
}
if(count==4)
{
        S3=1;
        S5=0;
}
if(count==5)
{
        S6=1;
```

```
                S4=0;
            }
            if(count==6)
            {
                count=0;
                S5=1;
                S1=0;
            }
        }
    }
```

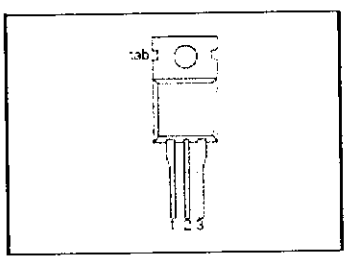
APPENDIX C:

N-channel enhancement mode TrenchMOS™ transistor

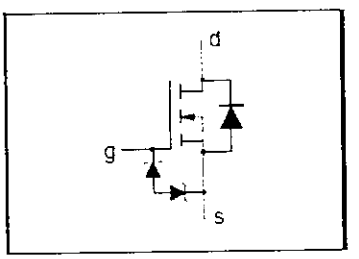
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	49	A
P_{tot}	Total power dissipation	110	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	22	mΩ

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	49	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	35	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	110	W
T_{stg}, T_j	Storage & operating temperature	-	-55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

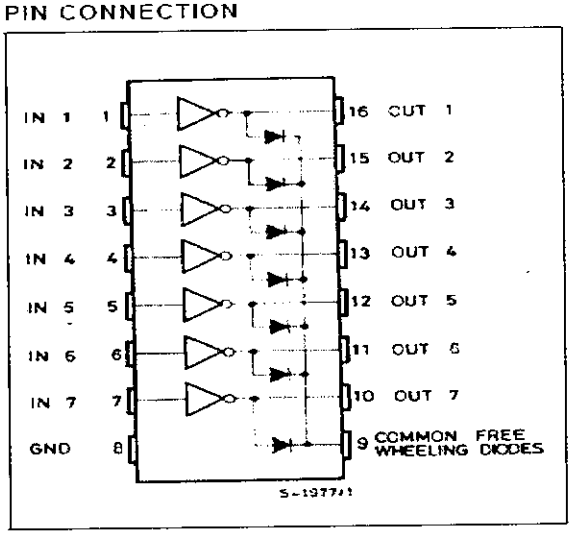
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\,j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.4	K/W
$R_{th\,j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

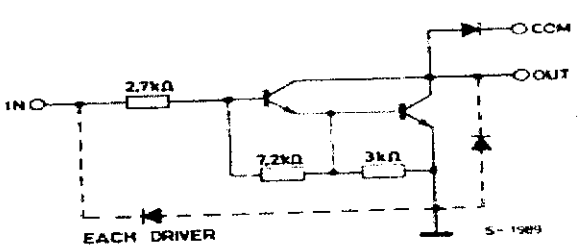
ULN2003A

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRATED SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

PIN CONNECTION





Series ULN-2003A
(each driver)

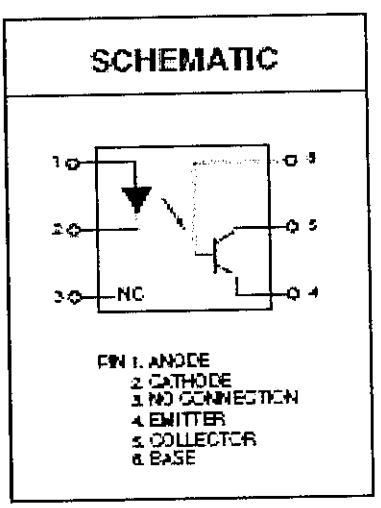
PHOTOTRANSISTOR OPTOCOUPLERS MCT2E

DESCRIPTION

The MCT2XXX series optoisolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package.

FEATURES

- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  - -Add option V for white package (e.g., MCT2V-M)
  - -Add option 300 for black package (e.g., MCT2.300)
- MCT2 and MCT2E are also available in white package by specifying -M suffix, eg. MCT2-M



APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

June 1989

National Semiconductor

54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

General Description

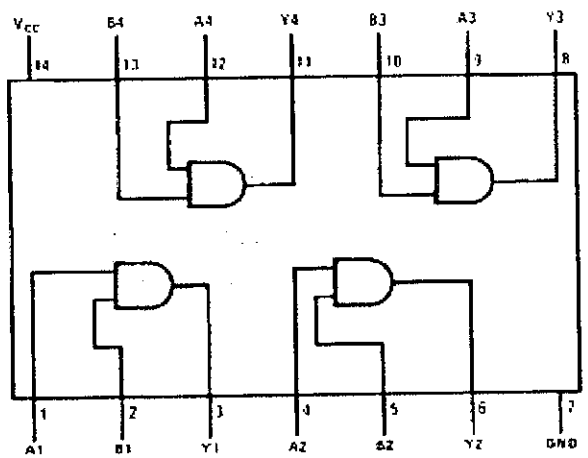
This device contains four independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6847–1

Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

MC78XX/LM78XX/MC78XXA

3-Terminal 1A Positive Voltage Regulator

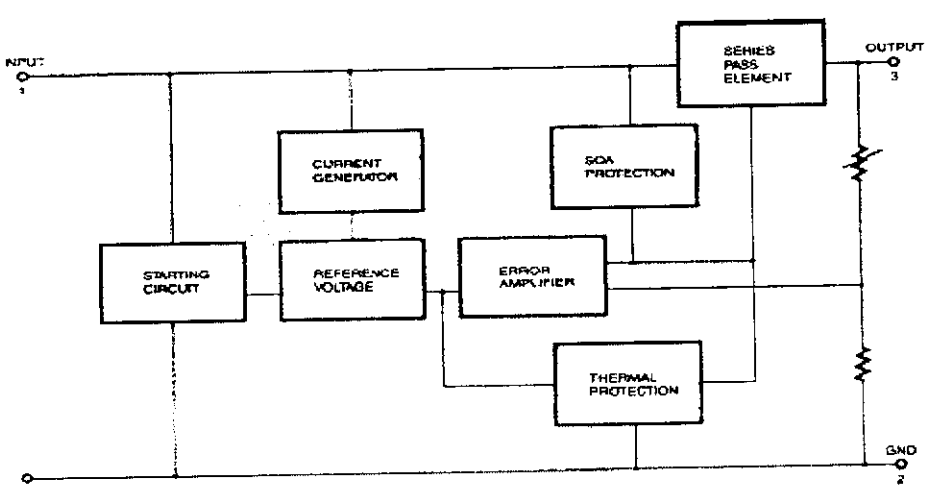
Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Internal Block Digram



CD4049UBC • CD4050BC
Hex Inverting Buffer • Hex Non-Inverting Buffer

General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

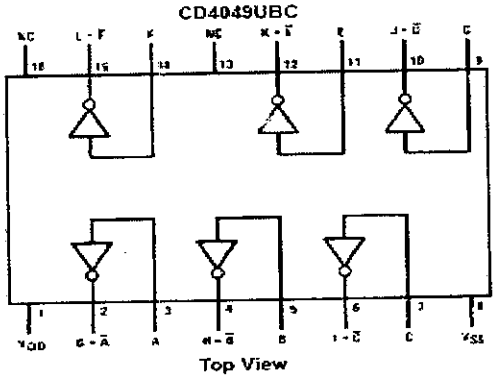
Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS HIGH-to-LOW logic level converter

Connection Diagrams

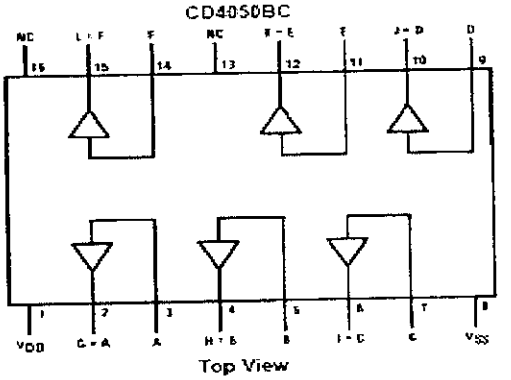
Pin Assignments for DIP

CD4049UBC



Top View

CD4050BC



Top View

6A, 100V, 0.600 Ohm, P-Channel Power MOSFET

IRF9520

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17501.

Features

- 6A, 100V
- $r_{DS(ON)} = 0.600\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol