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# IMPROVING POWER QUALITY IN WIND FARMS BY SUPPRESSING HARMONICS


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# BONAFIDE CERTIFICATE

Certified that this project report entitled **"Improving power quality in wind farms by suppressing harmonics"** is the bonafide work of

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Who carried out the project work under my supervision

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# ABSTRACT

The utility service providers will be required to maintain strict quality control by adhering to power factor and harmonic standards. Therefore, efforts are being made for systems that are drawing reactive volt-amperes to appear as linear load drawing current in-phase with the utility voltage. In this report, focus is on suppressing harmonics in the utility grid by a combined operation of Unified Power Quality Conditioner (UPQC) and Wind Energy Generation System (WEGS) at distribution level. An energy conditioner like UPQC can function as active series and shunt filter to compensate load current harmonics and supply voltage fluctuations simultaneously. The UPQC has two inverters that share a common DC link, consisting of a WEGS, compensating the voltage interruption. PWM pulses to these inverters play an important role. The aim of the project is to suppress harmonics due to non-linearity in the load by control strategies for the pulse modulation in the inverters. The validity of the proposed system is verified by simulating the model using MATLAB/SIMULINK. The prototype model is also designed, fabricated and tested.

# ACKNOWLEDEGEMENT

I humbly submit all the glory and thanks to the almighty for showering the blessings and giving the necessary wisdom for accomplishing this project.

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## ABBREVIATIONS

| | | |
|---|---|---|
| THD | - | Total harmonic distortion |
| UPQC | - | Unified Power Quality Conditioner |
| PWM | - | Pulse width modulation |
| AC | - | Alternating current |
| DC | - | Direct current |
| WEGS | - | Wind Energy Generating System |
| TMR0 | - | timer0 |
| TMR1 | - | timer1 |
| TMR2 | - | timer2 |
| CCP | - | compare capture |
| PQ | - | Power Quality |
| ASD | - | Adjustable speed drive |
| PCC | - | Point of common coupling |
| VSD | - | Variable speed drive |
| SMPS | - | Switch mode power supply |
| UPS | - | Uninterruptible power supply |
| TDD | - | Total demand distortion |
| RCCB | - | Residual current circuit breaker |
| APF | - | Active power filter |
| VAR | - | Volt-ampere reactive |
| DG | - | Distributed generation |
| SSB | - | Solid state breaker |
| LPF | - | Low pass filter |
| PLL | - | Phase lock loop |
| IGBT | - | Insulated gate bipolar transistor |
| PI | - | Proportional integral |
| MOSFET | - | Metal oxide semiconductor field effect transistor |
| PIC | - | Peripheral interface controller |
| LED | - | Light emitting diode |

## LIST OF SYMBOLS

$I_L$ - Load current

$I_{SC}$ - Short circuit current

$T_r$ - Transformer

$V_S$ - Source current

$I_S$ - Source current

$Vdc$ - DC voltage source

$L_r$ - filter inductance

$C_r$ - filter capacitance

$V_L$ - Load voltage

$I_L$ - Load current

$V_{inj}$ - Injected voltage

$I_d$ - Direct current

$I_q$ - Quadratic current

$\omega$ - Speed of rotating frame in rad/sec

$\mu F$ - microfarad

$mH$ - milli Henry

$V_0$ - Zero sequence voltage

# CHAPTER 1

# INTRODUCTION

It is well known that the development of renewable energy sources is strongly encouraged now a day due to fast depletion of traditional energy sources and the environmental pollution caused by them. The wind power generating system is one of the most useful generating systems, which harnesses the natural energy. Wind energy, which is the clean energy source and infinite natural resources, is one of the available non-conventional energy sources. It is a renewable energy source used in commercial and industrial applications Wind is a variable and random source of energy. Directly interfacing the wind energy systems to the utility gives rise to problems such as voltage fluctuations and harmonics. This problem is overcome by using a power electronic interface between Wind Energy Generating System (WEGS) and the utility.

## 1.1 NEED OF POWER QUALITY IMPROVEMENT:

In recent years, the applications of power electronics have grown tremendously. The power quality (PQ) problems in power distribution systems are not new, but only recently the effects of these problems have gained public awareness. Advances in semiconductor device technology have fuelled a revolution in power electronics over the past decade and there are indications that this trend will continue. However these power equipments which include Adjustable Speed motor Drives (ASDs), electronic power supplies, direct current (DC) motor drives, battery chargers, electronic ballasts are responsible for the rise in related PQ problems. These non-linear loads are constructed by nonlinear devices, in which the current is not proportional to the applied voltage. Non-linear loads appear to be prime sources of harmonic distortion in a power distribution system. Harmonic currents produced by non-linear loads are injected back into power distribution systems through the Point of Common Coupling (PCC). These harmonic currents can interact adversely with a wide range of power system equipments causing additional losses, overheating and overloading.

Traditionally, current harmonics caused by non-linear loads have been dealt using passive filters consisting of capacitors, inductors and damping resistors. They provide simple solutions but, very often, have large size and weight; hence, they cannot provide flexible compensation. Moreover, the passive filters are known to cause resonance, thus affecting the stability of the power distribution systems.

## 1.2 POWER QUALITY-DEFINITION AND PROBLEMS:

In the past, equipment used to control industrial process was mechanical in nature, being rather tolerant of voltage disturbances, such as voltage sags, spikes, harmonics etc. In order to improve the efficiency and to minimize costs, modern industrial equipment typically uses a large amount of electronic components. Such pieces of equipments are more susceptible to malfunction in the case of power system disturbances than traditional techniques based on electromechanical parts. As a result, minor power disturbances may completely interrupt whole automated factories because of sensitive electronic controllers. It is thus natural that electric utilities and end- users of electrical power are becoming increasingly concerned about the quality of electric power in distribution systems. The term power quality has become one of the most common expressions in the power industry during the current decade.

The term Power Quality has been used to describe the extent of variation of the voltage, current and frequency on the power system. In utility perspective, power quality is the concepts of providing electrical service with steady voltage and frequency and in customer perspective, it is the concept of receiving electrical service that does not hinder the operation of equipment. The electrical energy is consumed and required as a continuous flow as it cannot be conveniently stored and hence cannot be put through quality assurance checks before it is used. There are five basic types of power deficiencies, each with different causes and effects and, of course, different cost implications. The estimated power quality problem costs industry and commerce about 10 Billion Euro in European Union per annum, while expenditure on preventive measure is less than 5% of this value.

The basic power quality problems are:

- Voltage Sag
- Voltage Swell
- Voltage Interruption
- Under/ Over Voltage
- Voltage Flicker
- Harmonic Distortion
- Voltage Notching
- Transient Disturbance
- Outage and frequency variation

## 1.3 HARMONICS (WAVEFORM DISTORTION):

Distortion of the sine waveform of an AC Voltage or current can happen because of two conditions 1. Magnetic saturation of transformer cores and 2. Presence of large non-linear loads Magnetic saturation causes sudden change in the inductive reactance of a coil and results both in distortion of the magnetizing input current in a transformer as well as the output waveform.

### 1.3.1 Linear loads:

Loads that are resistances, capacitances or inductances (operating in the linear, unsaturated zone) or a combination of these circuit elements have the same wave shapes for voltage and current with or without a phase shift. Both are normally pure sinusoids and such loads are said to be linear. Most induction motors fed directly from AC mains also behave as a combination of resistance and inductive reactance and therefore can be considered as linear loads.

### 1.3.2 Non- linear loads:

Loads that draw distorted currents when supplied with sinusoidal voltage are called nonlinear. The current waveform is being distorted when the power electronic devices are introduced in the system to control the speed of AC (or DC) motors. These devices chop off part of the AC waveform using thyristors or power transistors, which are used as static switches. These are called non-linear loads.

### 1.3.3 Harmonic distortion:

Harmonic distortion is one of the major power quality issues in modern power systems. Today, the most common sources of Harmonics are power electronic loads such as semiconductor rectifiers in AC and DC variable-speed drives (VSD), Electronic lamp ballasts, Switch-Mode Power Supplies (SMPS) and Uninterruptible Power Systems (UPS). The distorted waveforms may be mathematically analyzed using Fourier transforms as a combination of vectors of the power frequency (50 Hz) and others whose frequency is a multiple of the power frequency. The power frequency component is called the Fundamental frequency component and higher multiples are called Harmonic frequency components or simply as harmonics.

### 1.3.4 Current sources of harmonics:

All electrical generators produce only voltage at fundamental frequency. However, there has to be a source of harmonic frequency voltage if a harmonic current has to flow. It is therefore construed theoretically that all harmonic producing loads are current sources of harmonics. These sources drive harmonic currents through the rest of the system consisting of the fundamental frequency sources as well as other loads connected to it. These current flowing through the different impedance of the system appears as harmonic voltages. It is usual for the voltage waveform of such a system to appear distorted. In addition, the harmonic currents flowing through the other loads of the system give rise to several abnormalities. The figure 1.1 shows one of the distorted voltage waveform due to non-linearity in load.

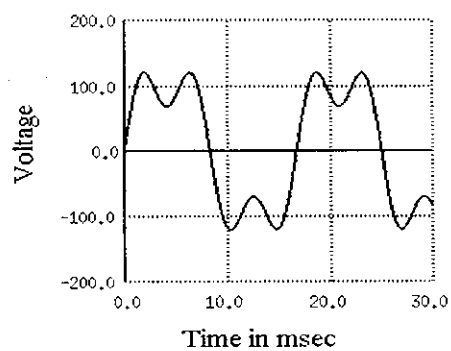



Figure 1.1 Distorted waveform

## 1.4 INDICES AND LIMITS FOR HARMONICS:

Two important indices, Total Harmonic Distortion in voltage (THD) and Total Demand Distortion in currents (TDD), are used to measure the amount of harmonics in power systems. These indices are used to measure the deviation of a periodic waveform containing harmonics from a perfect sine wave.

### 1.4.1 Limits for Harmonics -IEEE Standard:

The allowable limits for voltage and current distortion as specified by IEEE 519 – 1992 are given in Tables 1 and 2. Harmonics are measured at the Point of Common Coupling (PCC). PCC can be either the primary or secondary of a utility transformer or at the service entrance of the facility or between the non-linear loads and other loads of an industrial plant.

Table 1.1
Supply Voltage Distortion (THD) Limits as per IEEE 519 -1992

| Voltage at PCC / Point of supply | Individual harmonic Voltage distortion (%) | Total voltage Distortion THD (%) |
|---|---|---|
| ≤ 69 kV | 3.0 | 5.0 |
| 69.0001 - 161 kV | 1.5 | 2.5 |
| > 161.001 kV | 1.0 | 1.5 |

Table 1.2
Load Current Distortion (TDD) Limits as per IEEE 519-1992

| Isc / $I_L$ | Maximum Harmonic current Distortion in % of $I_L$ | | | | | |
|---|---|---|---|---|---|---|
| | Individual Harmonic order (Odd Harmonics) | | | | | |
| | <11th | 11-17 | 17-23 | 23-25 | >35 | TDD |
| <20 | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |

## 1.5 SOURCES OF HARMONICS:

The following types of electrical equipment generate considerable amount of harmonics:

- Variable speed drives (VSD)
- Uninterruptible power supplies (UPS) and SMPS
- Fluorescent lamps with electronic ballasts
- Power electronic equipment (drives, rectifier, computer etc)
- Arcing devices (welders, arc furnace)
- Iron saturating devices (transformers)

## 1.6 EFFECTS OF HARMONICS:

### 1.6.1 Overloading of neutrals:

The current flow in the neutral is zero in a balanced linear load condition. But in a balanced non-linear load condition, it may give rise to the 3rd harmonic currents. While the fundamental components cancel out in the neutral, the 3rd harmonic currents of all the three phases are co-phasal and the neutral has to carry 3 times the value of the third harmonic current. In a load where the third harmonic content is 70% of the fundamental, the neutral will carry 3 times this current, viz., 210% of the fundamental current value. A neutral conductor designed with half the cross section of phase conductors will therefore get heated resulting in conductor/termination failure. The same is also true for all triple-N harmonics (3, 9, 15 etc.) The remedy is to install a double sized neutral conductor when single-cored cables are used. The cables carrying triple-N harmonic currents must be de-rated where multi-cored cables are used.

### 1.6.2 Overheating of Transformers:

Transformers supplying to non-linear loads usually get overheated as a result of increased eddy current losses. In a transformer, eddy current loss at full load is about 10% of the total losses. The eddy current loss is proportional to the square of the frequency. The third harmonic component of eddy current will cause 9 times the

loss of the same magnitude of fundamental component. The higher loss in the core because of eddy current will cause overheating and eventual failure of the transformer. To overcome this, the transformer must be suitably de-rated considering the harmonic content of the load.

**1.6.3 False tripping of circuit breakers:**

Circuit breakers can mal-operate when used in circuits carrying harmonic currents, since the setting for tripping is done based on the fundamental component of the load current, leaving the harmonic currents.

**1.6.4 Residual Current Circuit Breakers (RCCB):**

RCCB is installed for the safety of the human beings and equipment and it can maloperate due to the earth leakage detection circuit detects the harmonic currents. Suitable filters are to be provided to mitigate this problem.

**1.6.5 Capacitor failures due to harmonics:**

Capacitors in circuits with high harmonic loads can fail due to two reasons, 1) Increased current flow 2) Resonance causing excessive voltage / current. Capacitors have lower impedance at higher frequencies. The harmonic current through branches containing capacitances (such as filters / power factor compensating circuits etc.) is therefore much higher. This increased current leads to failure of capacitors. The other problem is that of resonance. This can happen between the capacitors and inductances present in the system, which can either from a series resonant or parallel resonant combination. Since the reactance of a capacitor decreases with frequency and that of an inductor increases with frequency, a given combination of inductor and capacitor will have equal inductive and capacitive reactance at a particular value of frequency. This combination is set to be resonant at that frequency. A common method adopted to avoid failures due to resonance is by adding an inductance in series with the capacitor such that the combination is just inductive at the lowest significant harmonic. This solution also limits the harmonic current that can flow in the capacitor.

**1.6.6 Skin effect:**

Alternating current always tends to flow on the outer surface of a conductor. This is known as skin effect and is even noticeable at normal system frequency,

particularly in the larger cross-section conductors and results in the reduction of the effective area of the conductor. This is the reason for assuming a higher conductor resistance when AC currents are carried. The effect is more pronounced at high frequencies, particularly at 350 Hz, i.e. the 7th harmonic and above causing additional loss and heating. Where harmonic currents are present, designers should consider skin effect and de-rate cables accordingly.

**1.6.7 Electromagnetic interference:**

Harmonic currents flowing in conductors can set up magnetic fields around them which will link with the conductors of other circuits running nearby, resulting in interference. The interference with communication circuits is an example, but similar effect is possible in signal and data circuits as well and will result in the introduction of noise in these circuits. Filters may be provided to over come this effect.

**1.6.8 Operation of rotating machines:**

Harmonic currents affect rotating machines such as motors and generators in the same manner as transformers; by causing higher eddy current losses. Apart from this effect, harmonic voltages present in the system set up magnetic fields at harmonic frequencies, whose interaction with the rotor causes increased rotor heating. The phase sequence of harmonics is also different with some of them producing magnetic fields trying to rotate the machine in a direction opposite to the normal direction of rotation produced by the fundamental component. Others tend to rotate the machine in the same direction faster than the actual speed of rotation. In the case of induction motors, this causes interference with the motor torque. Filters may be provided to overcome this effect.

## 1.7 METHODS OF HARMONIC CONTROL:

Harmonic control in a power system is done using one of the following approaches.

### 1.7.1 Reduction harmonic currents generated by a load by suitable reconfiguration:

Mitigation is possible segregating the linear and non-linear loads by feeding them through separate feeders so that the cable impedance separating the two can soften the voltage distortion effect. In addition, 12-pulse controlled rectifier is used in place of 6-pulse controlled rectifier

### 1.7.2 By using passive filters:

Divert the harmonic currents away from other loads by shunt filters or block the flow of harmonic current using series inductive reactive filters Harmonic filters, as applied to electrical power systems, comprise power capacitors in series with inductors forming one or more circuits or arms. Each of which is tuned to accept a particular order of harmonic current. The function of the harmonic filter is to contain the harmonic currents generated in a particular circuit or factory system and to prevent circulation of such currents in the electrical supply system with consequent adverse effects on system operation. In effect, the capacitor banks are providing a sink for harmonic currents.

### 1.7.3 Isolation by a transformer:

The third harmonic currents as well as the multiples of third harmonics (6th, 9th, 12th etc.) behave like zero sequence currents. When these harmonic currents encounter a delta winding, they circulate within the delta and are trapped from flowing back beyond this winding. Thus, systems that encounter triple-N harmonic generation can use a delta-connected transformer to isolate the harmonics from the supply source.

### 1.7.4 Active filters:

In some installation, the harmonic content is not predictable. In many IT installations, for example, the equipment mix and location is constantly changing so that the harmonic content is also constantly changing. A convenient solution is the active filter or active conditioner. Active filters use waveform synthesis methods to read the load current and generate a current waveform equal to the distortion component but with the opposite polarity. With the harmonic components thus cancelled, the current drawn from the mains become perfectly sinusoidal. They offer

several advantages over passive filters but are much more expensive for comparable capacities.

Over the past 20 years the introduction of the power thyristor and its subsequent development has made it possible to cheapen and broaden the application of ac / dc conversion in the form of frequency converters to provide accurate speed control of direct-current motors or to provide dc supplies for large electrolytic processes, particularly in the chemical industry. Consequent upon the increased use of motor drives with thyristor control for both large and small projects, expansion of electrolytic processes and the rise in ratings of electric arc furnaces, the percentage of harmonic currents flowing in power systems in all highly industrialized countries is growing. In the UK, it is estimated that the increased flow of harmonic currents in electricity board networks will cause voltage distortion of up to 10% in certain areas- a very serious situation if allowed to happen.

## 1.8 OBJECTIVE:

An energy conditioner like UPQC can function as active series and shunt filter to compensate load current harmonics and supply voltage fluctuations simultaneously. In this paper, focus is on suppressing harmonics in the utility grid by a combined operation of Unified Power Quality Conditioner (UPQC) and Wind Energy Generation System (WEGS) at distribution level.

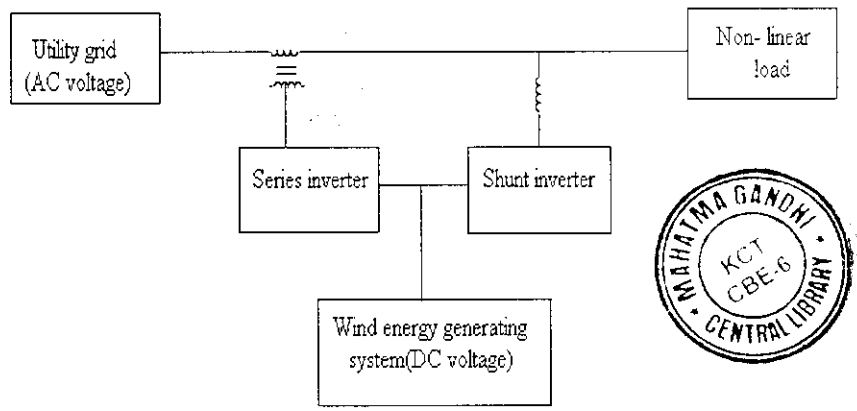





Figure 1.2 The proposed system

The purpose of this project is to study the combined operation of the Unified Power Quality Conditioner with wind energy generating system and design a UPQC to suppress the effect of harmonics and hence to improve the power quality. Also to investigate the performance of the proposed system by calculating THD values both in voltage and in current using MATLAB/ Simulink software. The figure 1.2 shows the block diagram of proposed system.

## 1.9 LITERATURE SURVEY:

The problems caused by the harmonic currents have led some researchers to study them. Luis F.C. Monteiro has proposed a new control strategy for UPQC in his paper "A control strategy for Unified Power Quality Conditioner" which is used in three phase three wire systems. In that paper, they presented an integration principle of shunt current compensation and series voltage compensation, both based on instantaneous active and reactive powers, directly calculated from a-b-c phase voltages and line currents.

E.H.Watanabe, in his paper "Power quality considerations on Shunt/Series Current and Voltage Conditioners" presents the basic concept of power quality considerations, especially when the current and voltage or both present non-sinusoidal waveforms. The use of compensator for current harmonic or unbalance compensation or the use of series compensator for voltage harmonic or unbalance compensations is discussed in his paper.

Hideaki Fujita, in his paper "The Unified Power Quality Conditioner: The integration of Series Active Filters and Shunt Active Filters" presented the capability of UPQC to improve the power quality at the point of Installation on power distribution systems and industrial power systems.

An experimental set up was discussed by Malabika Basu in his paper "Experimental Investigation of Performance of a Single Phase UPQC for Voltage Sensitive and Non-linear Loads". A PC-based closed loop control scheme is proposed and experimental investigation is carried out in laboratory. Many papers have been

published in international journals for the new advanced control algorithms used for investigating the performance of UPQC.

M.Hosseinpour, in his paper "Design and simulation of UPQC to improve Power Quality and Transfer Wind Energy to Grid" proposed a new scheme, a combined operation of UPQC with WEGS for power quality improvement. This paper also compares the investment cost of separate use of UPQC and WEGS with the new combined system.

## 1.10 ORGANIZATION OF THE THESIS:

This report presents about the combined operation of UPQC with WEGS for power quality improvement by suppressing harmonics. Chapter 1 tells about the importance of renewable energy resources and the need of power quality improvement. It also explains what are power quality and causes, effects and remedies of harmonics. Chapter 2 details the overview of the proposed system. Chapter 3 deals with the control strategies of PWM pulses for series and shunt inverters. Chapter 4 describes the modeling of proposed system in MATLAB/Simulink and simulation results of proposed system and comparison of THD. Chapter 5 deals with the modeling of hardware of the proposed system, the results of hardware testing and the process flow chart for PIC programming. In Chapter 6, the conclusion and the future scope of the project is discussed.

# CHAPTER 2

# UPQC WITH WIND ENERGY GENERATING SYSTEM

In this chapter, the concept of UPQC is discussed along with the phasor diagram. The proposed system i.e. is UPQC with Wind Energy Generating System connected to the DC link through the rectifier is also discussed in detailed.

## 2.1 SYSTEM CONFIGURATION OF UPQC:

The schematic diagram of the UPQC system is shown in figure 2.1. Power electronic based power processing offers higher efficiency, compact size and better controllability. However, due to switching actions, these systems behave as non-linear loads, so they draw non-sinusoidal and/or lagging current from the source. Hence, they draw considerable reactive power from the utility and inject harmonics in the power network.

The voltage injected in series with the load by series active power filter (APF) is made to follow through an isolation transformer $T_r$ as shown in figure, such that the sum of this injected voltage and the input voltage ($V_S$) is sinusoidal. Thus if the utility voltages are non-sinusoidal, or unbalanced, proper selection of magnitude and phase for the injected voltage will make the voltages at the load end to be balanced and sinusoidal. The shunt APF as a current source and inject a compensating harmonic current in order to have sinusoidal, in- phase input current ($I_S$) and the series APF acts as a voltage source and inject a compensating voltage in order to have sinusoidal load voltage. This combination of series and shunt APF is called as UPQC.

The voltage at point of common coupling (PCC) may be or may not be distorted depending on the other non-linear loads connected at PCC. Two voltage source inverters (shunt APF and series APF) are connected back to back, sharing a common DC link. $C_d$ represents the coupling capacitor. One inverter is connected parallel with the load. It acts as shunt APF, helps in compensating current as well as to maintain DC link voltage at constant level. The second inverter is connected in series with the utility voltage by using series transformers and helps in maintaining the load voltage sinusoidal. Passive elements $L_r$ and $C_r$ connected to the circuit to

remove the high frequency harmonics in order to eliminate the higher order harmonics caused by the converter switching.

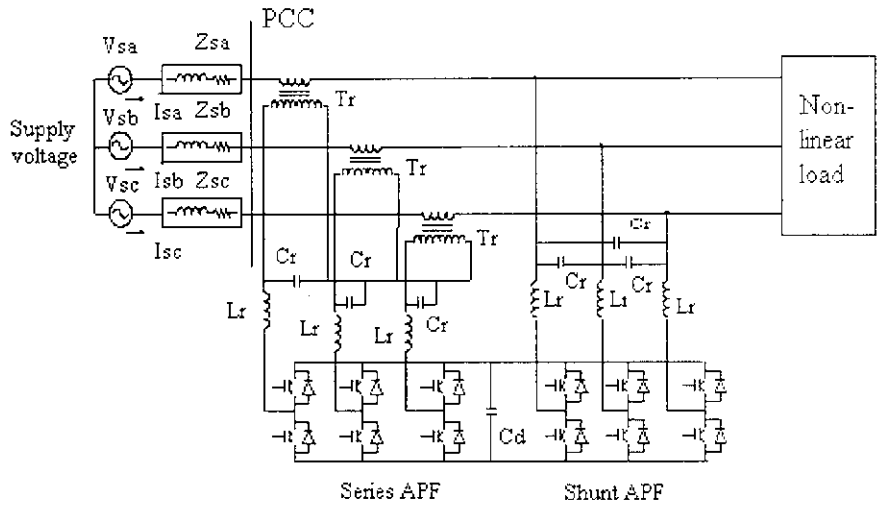



Figure 2.1 Schematic diagram of UPQC

## 2.2 PHASOR DIAGRAM OF UPQC:

The phasor diagram shown in figure 2.2 explains the operation of the UPQC. When the supply voltage, $V_{S1}$ is at rated value|, the load voltage $V_1$($|V_1|=|V_{L1}|=|V_{S1}|$) is also at the rated level. The load current is $I_{L1}$ ($|I_{L1}| =|I_1|$) and the shunt inverter compensate the reactive component $I_{C1}$ of load resulting in unity power factor, hence the load appear to draw only in-phase component $I_{S1}$ from the supply.

Now, if there is any sag in the supply, such that the supply voltage falls to $V_{S2}$($|V_{S2}|<|V_{S1}|$), the series compensator injects a voltage, $V_{inj}$, such that the magnitude of resultant voltage at the load end($V_{L2}$) is maintained at $|V_L|$. The load current changes to $I_{L2}$. Now the shunt inverter injects $I_{C2}$ in such a fashion that the utility current is $I_{S2}$ ($I_{S2}=I_{L2}$ ($\cos\Phi/\cos\theta$)) which is in phase with supply voltage. Between the control loops, the analog hysteresis current control loop used with the shunt is much faster than the voltage control loop of the series converter. For non-linear loads, harmonic elimination and VAR, compensation are first done by the shunt compensator, so the utility sees the load to be always linear and of u.p.f. A slower

digital controller simultaneously corrects the voltage sag. The series voltage compensator always sees the supply current to be in phase with the voltage due to the faster compensation by the shunt controller. The two loop speeds are chosen such that in no case these two controllers can interfere with each other and cause instability.

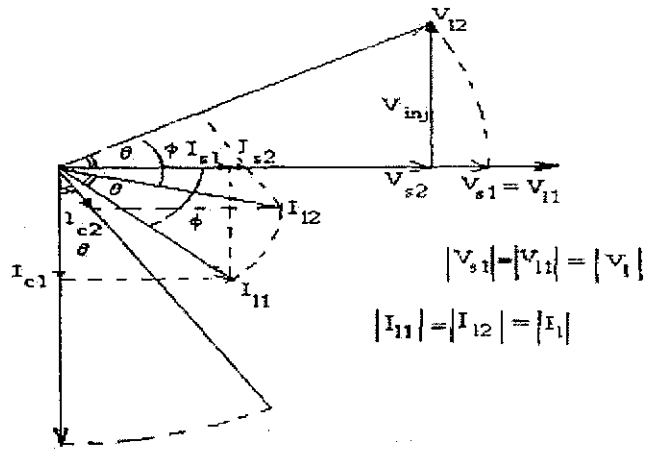



Figure 2.2 Phasor diagram of UPQC

## 2.3 CONFIGURATION OF PROPOSED SYSTEM:

The proposed system considers a combined operation of UPQC with Wind Energy Generation of electricity from renewable has improved very much. Utilizing of wind energy as a renewable source to generate electricity is being developed extremely rapidly and many commercial wind energy generating units are now available.

Here a new configuration of UPQC is proposed that has a Wind Energy Generation System connected to the DC link through the rectifier as shown in figure 2.3. The economic analysis of the separate linking of UPQC and Distributed Generation (DG) to distribution network and combined operation of UPQC with WEGS is done. In combined operation of UPQC and DG, an inverter is used less compared to the separate operation of them. On the other hand, there is no need for DG converter and its duty is done by shunt inverter. The shunt inverter transmits the

active power of DG to grid besides compensating the reactive power and harmonics of load current without increase of shunt inverter rating.

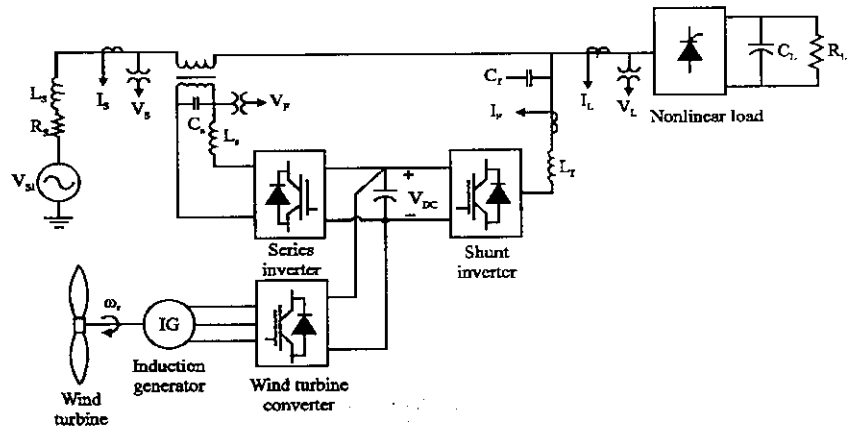



Figure 2.3 The proposed system

There are two operation modes in the proposed system. (i) Interconnected mode and (ii) Islanding mode.

### 2.3.1 Interconnected mode:

The first is interconnected mode, in which the WEGS provides power to the source and load. It compensates the current harmonics generated by the non-linear load and reactive power and to inject the active power of WEGS to grid. This mode is also known as normal mode or parallel mode.

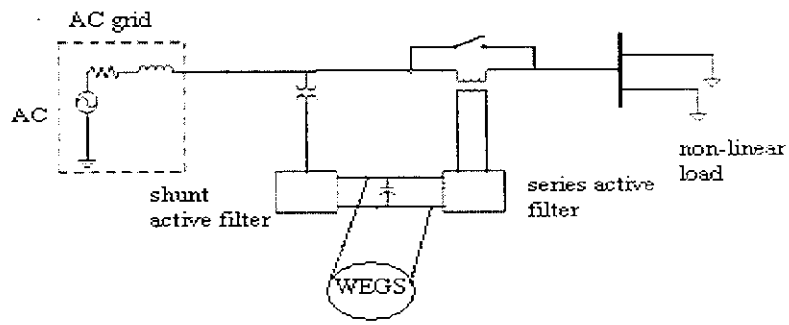



Figure 2.4 Combined operation of UPQC with WEGS in interconnected mode

### 2.3.2 Islanding mode:

The second is islanding mode, in which the WEGS provides power to the load only within its power rating when the voltage interruption occurs. The system operation transverse from the islanding mode to the interconnected mode when the voltage interruption is removed. This mode is also known as interruption mode.

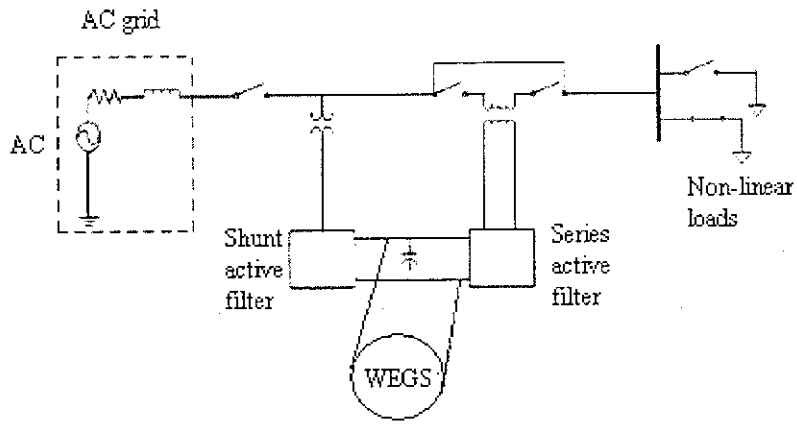



Figure 2.5 Combined operation of UPQC with WEGS in islanding mode

The control mode is determined by the state of Solid State Breaker (SSB). The figure 2.4 shows combined operation of UPQC and DG in islanding mode. This mode is the most challenging situation for power quality issues. I f the grid voltage drops below the certain threshold voltage level beyond the certain fixed duration, SSB should disconnect customer's network from the utility lines. Then the proposed configuration changes its operation mode from interconnected mode to islanding mode. If there are several DGs in the islanded network, all of the DG units should have proper control strategy to share loads

# CHAPTER 3

# CONTROL STRATEGIES FOR INVERTERS

In this chapter, complete control strategy used for the UPQC series and shunt inverters are discussed. The shunt controller determines the compensating current reference for PWM control of the UPQC shunt inverter, and series controller generates the compensating voltage reference for PWM series inverter.

## 3.1 SHUNT INVERTER CONTROL STRATEGY:

This method is derived from the space vector transformation of the input signals in the a-b-c coordinates (stationary reference frame) from the input sensors and the transformed into the orthogonal d-q coordinates (rotating reference frame with fundamental frequency) by means of Park's transformation. The d-q frame rotates with fundamental angular frequency that makes the fundamental signal to appear as DC components and the harmonic components are represented as AC signals.

Using this method current harmonics of all orders can be separated from the fundamental by using a low-pass-filter. The output signal is purely DC signal. which can be transformed back to a-b-c co-ordinates to obtain the fundamental current signal.

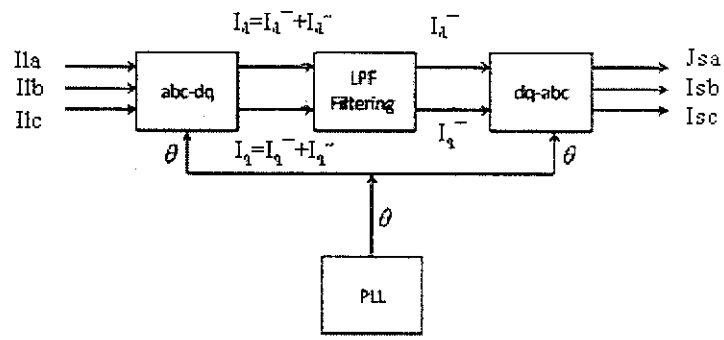



Figure 3.1 Block diagram of Synchronous Fundamental d-q Frame Model

The above diagram demonstrates the model. The d-q components of current signal both DC and AC signals and using Low Pass Filter (LPF) the signal is filtered

and applying reverse transformation we can obtain the fundamental value of the given input current signal. The generation of the reference compensation is same as in previous case. To maintain a constant frequency a virtual PLL circuit is used in simulation.

In this method the a-b-c to d-q transformation or Park's Transformation is obtained by using the following transformation matrix followed by the inverse transformation.

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \frac{2}{3}\begin{pmatrix} \cos\theta & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta-\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) \end{pmatrix}\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix}$$

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) \\ \cos\left(\theta+\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right) \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix}$$

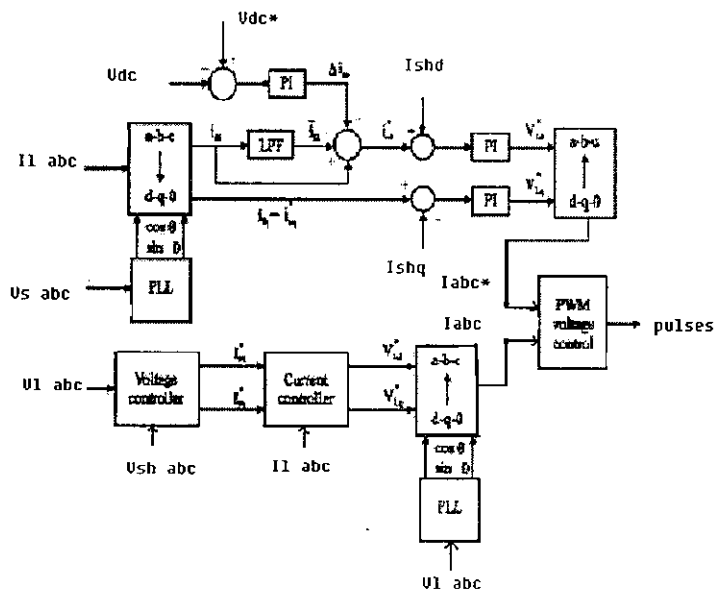



Figure 3.2 Shunt Inverter Control Block Diagram

## 3.2 SERIES INVERTER CONTROL STRATEGY:

The function of series inverter is to compensate the voltage disturbance in the source side, which is due to the fault in the distribution line. The series inverter control calculates the reference value to be injected by the series inverter as shown in figure. The system voltages are detected and then transformed into synchronous d-q-o reference frame using the equation

$$V_{sdqo}=T^{dqo}{}_{abc}V_{sabc}$$

The load bus voltage should be kept sinusoidal with constant amplitude even if the voltage on system side is disturbed. Therefore, the expected load bus voltage in d-q-o reference frame has only one value.

$$V^{*}_{ldq0} = T^{dq0}_{abc}.V^{*}_{labc} = \begin{bmatrix} V_m \\ 0 \\ 0 \end{bmatrix}$$

where,

$$V^{*}_{labc} = \begin{bmatrix} V_m \cos(\omega t + \theta) \\ V_m \cos(\omega t + \theta - 120^{\circ}) \\ V_m \cos(\omega t + \theta + 120^{\circ}) \end{bmatrix}$$

where, $V_m$ is the peak value of desired load voltage and $\theta$ is the phase angle of load voltage, which is determined by PLL (phase locked- loop).

This means d-axis of load reference voltage equals $V_m$ while q-axis and zero axis of load reference voltage equals zero. The compensation reference voltage is:

$$V^{*}_{fdqo}=V^{*}_{ldqo}-V_{sdqo}$$

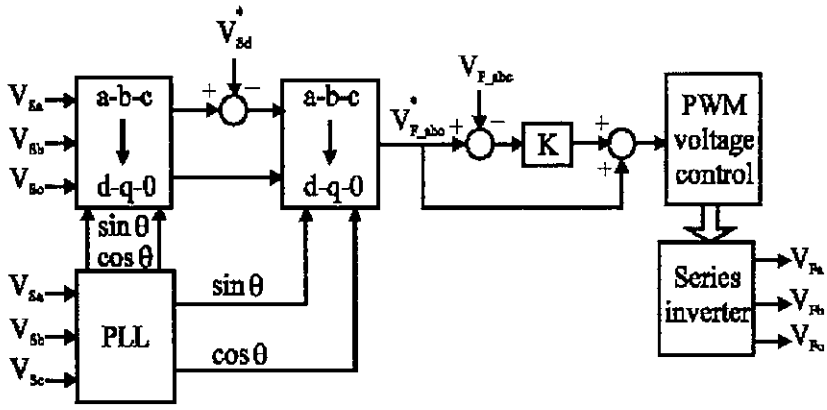



Fig 3.3 Series Inverter Control Block Diagram

The compensation reference voltage in above equation is then inversely transformed into a-b-c reference frame. Comparing the compensation reference voltage with a triangular wave, the output compensation voltage of the series compensator can be obtained by PWM voltage control.

# CHAPTER 4

# SIMULATION OF UPQC WITH WEGS USING MATLAB 7.0.4

In this chapter, the modeling of the proposed system for simulation study i.e. UPQC combined with WEGS is discussed. This modeling consisting of control blocks for series and shunt PWM inverter. The model is simulated using Matlab/Simulink blocks.

## 4.1 MATLAB/SIMULINK BLOCK FOR THE PROPOSED SYSTEM:

### 4.1.1 Overall system structure:

The Matlab/Simulink based simulation model of proposed system is shown in figure. The load is realized by using a thyristor bridge rectifier followed by a RL load. The distortion in supply voltage is introduced by the non-linearity in the load. Both the series and shunt active power filters are realized by six IGBT switches each, sharing a common DC link, in which wind mill is connected.

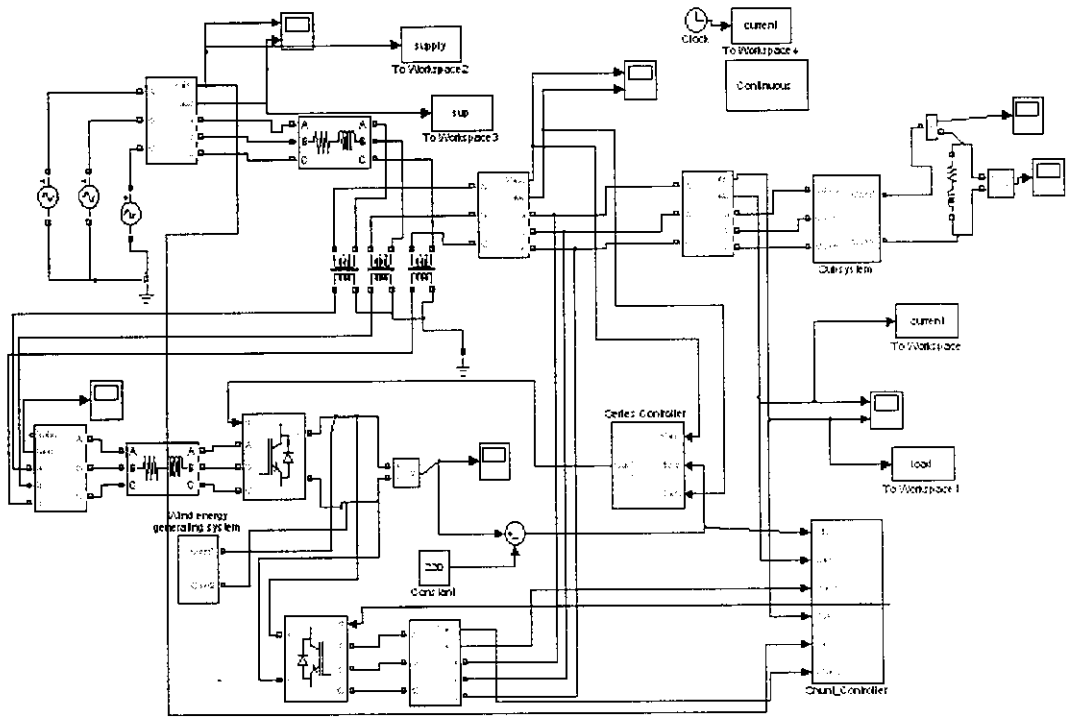



Figure 4.1 Overall System Matlab/Simulink Block

### 4.1.2 Modeling of Series Controller:

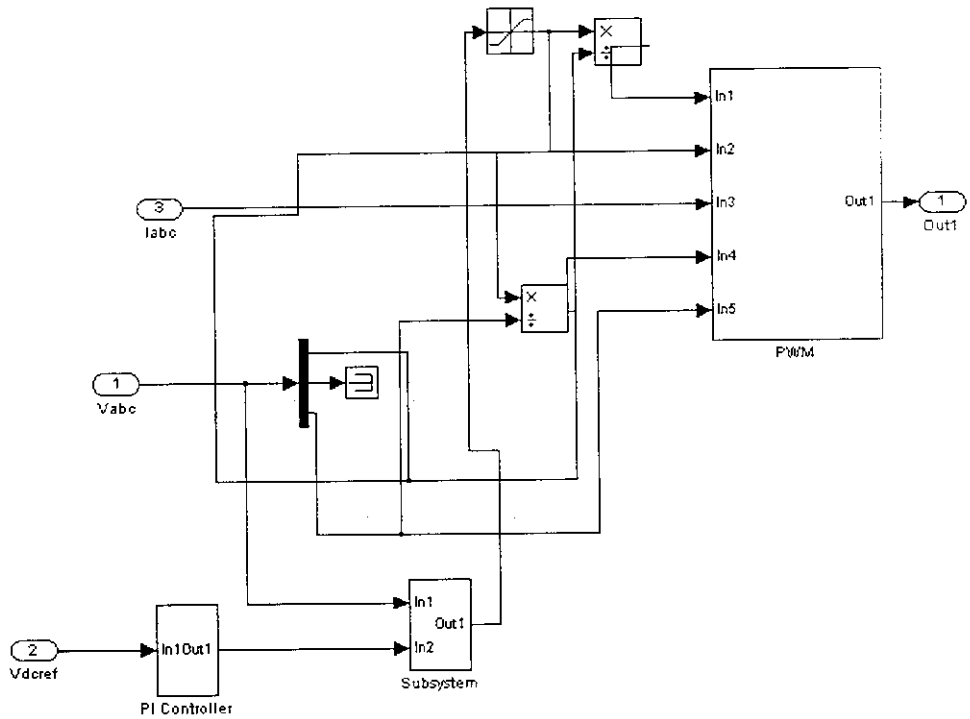



Figure 4.2 Series controller circuit configuration

In the series controller modeling, there are three subsystems. First one is a PI controller. To avoid DC voltage fluctuation, a PI controller is used. The input of the PI controller is the error between the actual DC link voltage and the reference value. The proportional and integral gain for DC voltage controller used in simulation are $K_P$=0.2 and $K_I$=9.32 respectively.

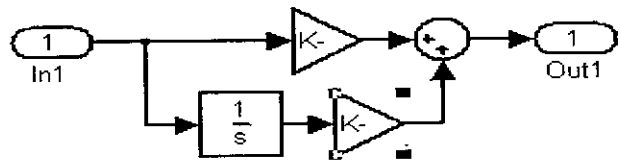



Figure 4.3 PI Controller Subsystem

The PI controller output is added to the feed back load voltage to produce the actual desired voltage. The output of this subsystem is given to a current limiter and finally to the PWM subsystem.

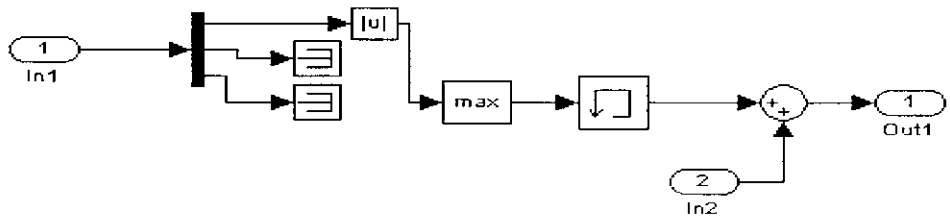



Figure 4.4 Reference current subsystem

The input two and five for the PWM subsystem is the feed back load voltage and three is feed back load current.

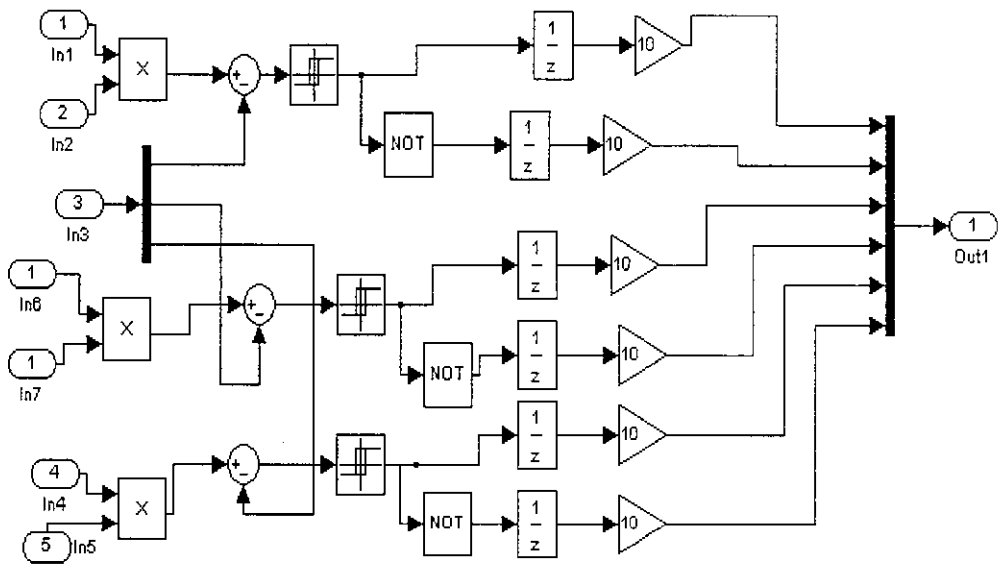



Figure 4.5 PWM subsystem

The reference current compared with the feed back signal, the error is given to the relay point where the output value switch between the specified limits and then to a gain of 10. The complement is also taken. Thus, the six pulses for the series inverter

block is generated. Thus, the series inverter compensates the voltage disturbance in the source side.

### 4.1.3 Modeling of Shunt Controller:

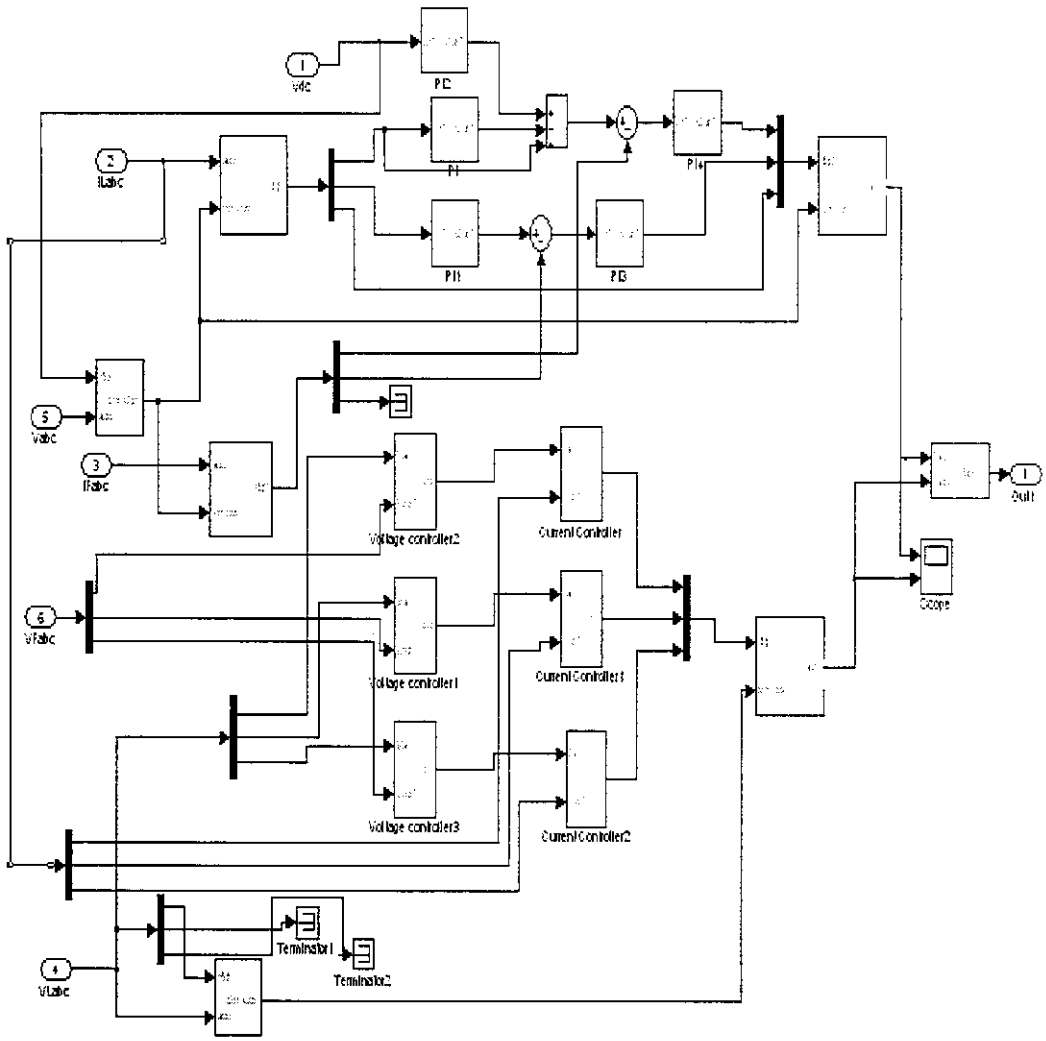



Figure 4.6 Shunt Controller Circuit Configuration

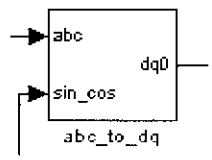



Figure 4.7 abc-dq Transformation Block

This block performs abc-dq0 transformation on a set of three phase signals. It computes the direct axis $V_d$, quadratic axis $V_q$ and zero sequence V0 quantities in a two-axis rotating reference frame according to the following transformation.

$V_d=2/3[V_a* \sin(\omega t)+V_b* \sin(\omega t-2\pi/3)+V_c* \sin(\omega t+2\pi/3]$

$V_q=2/3[V_a* \cos(\omega t)+V_b* \cos(\omega t-2\pi/3)+V_c* \cos(\omega t+2\pi/3]$

$V0=1/3[V_a+V_b+V_c]$

where ω is the speed of rotating frame in rad/sec. In addition, this transformation is known as Park transformation.

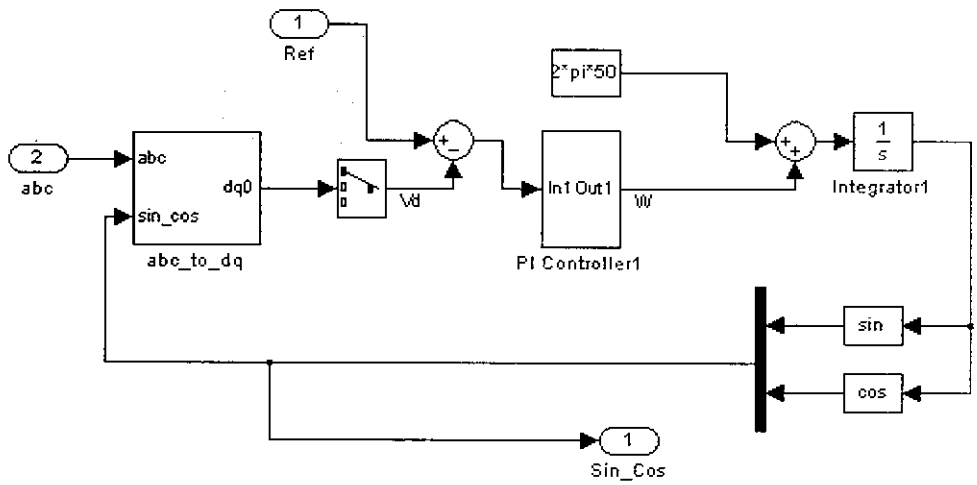



Figure 4.8 PLL block

After doing the transformation, the direct axis component is compared with the DC error signal. It then given to the PI controller and added with the reference signal. Then it given to the integrator to calculate the phase angle.

The load current is transformed in to dq0 quantities. By using a LPF and a comparator block, the harmonic content in the load current is calculated. The output signal then compared with the actual shunt active feed back current and the error signal is given to a PI controller for to avoid the fluctuations. The reverse

transformation is by using the following equations to get the reference abc signal for PWM pulse generation of shunt inverter.

$V_a=V_d* \sin(\omega t)+V_q* \cos(\omega t)+V0$

$V_b=V_d* \sin(\omega t-2\pi/3)+V_q* \cos(\omega t-2\pi/3)+V0$

$V_c=V_d*\sin(\omega t+2\pi/3)+V_q*\cos(\omega t+2\pi/3)+V0$

The load voltage and feed back shunt controller voltage get compared and then given through the current and voltage controllers to produce the actual voltage signal. The reference current signal and the actual signal compare and produce the pulses for the shunt inverter.

## 4.2 SIMULATION RESULTS:

The operation of proposed system is evaluated by computer simulations using Matlab/Simulink.Using these simulations, it is possible to evaluate the performance of the proposed system in compensating the harmonics due to non-linearity in loads. A variable step (ODE 23tb) solver is used for calculations during simulation.

The UPQC is made of two single-phase full bridge inverters, with the help of IGBT/diode module having rating of 1200V, 5A. The DC link capacitor is 2200μF, 220 V dc. The windmill output is taken from a rectifier unit. The gird voltage is applied is a balanced sinusoidal voltage of 230V ac 50 Hz. The source impedance is represented by a RL branch which has R=0.1 ohm and L=0.15mH.

The load is a thyristor-controlled rectifier, which has an R-L load at its dc side. Here R=100ohm and L=200 mH. Due to non-linearity in load, it causes the waveform distortion in the utility grid. They are compensated by the series and shunt inverters. The waveforms of both load side and supply side voltage and current waveforms are compared for both the conditions, i.e. with and without compensator. In addition, THD values of the both the current and voltage waveforms for five cycles are also compared. From the results, we can see that, both current and voltage THD values are with in the specified limits.

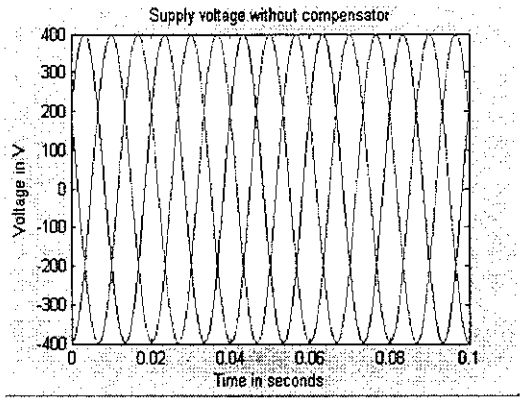



Figure 4.9 Supply voltage without Compensator

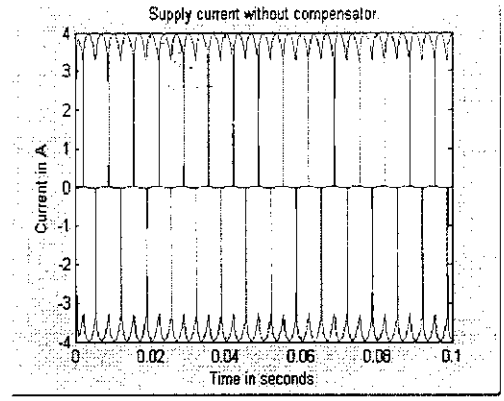



Figure 4.10 Supply current without Compensator

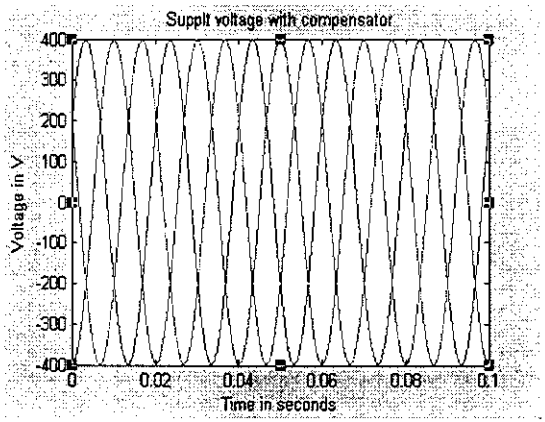



Figure 4.11 Supply voltage with Compensator

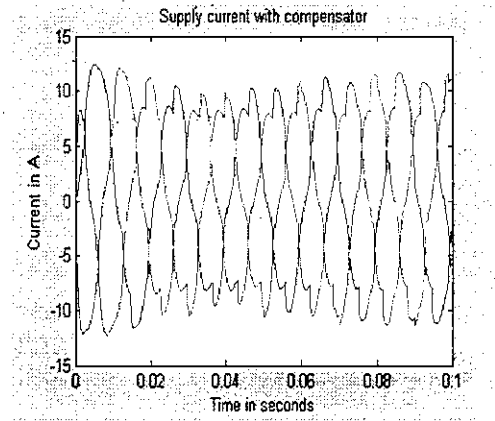



Figure 4.12 Supply current with Compensator

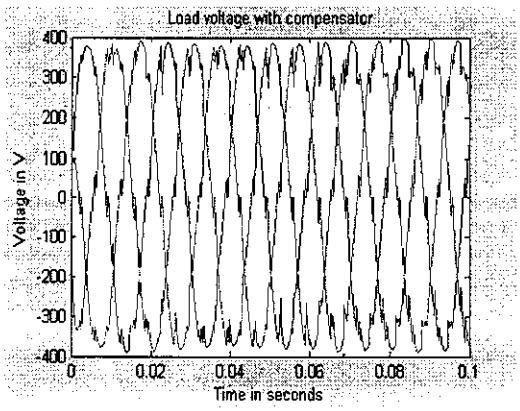



Figure 4.13 Load voltage with compensator

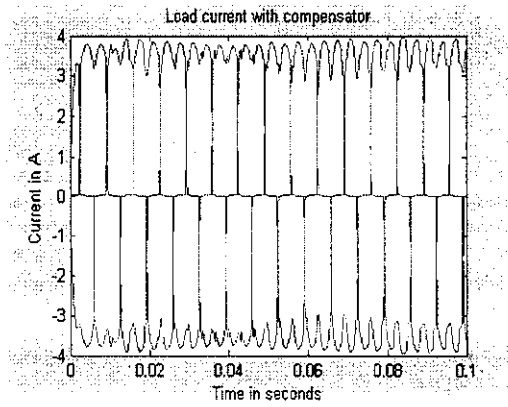



Figure 4.14 Load current with compensator

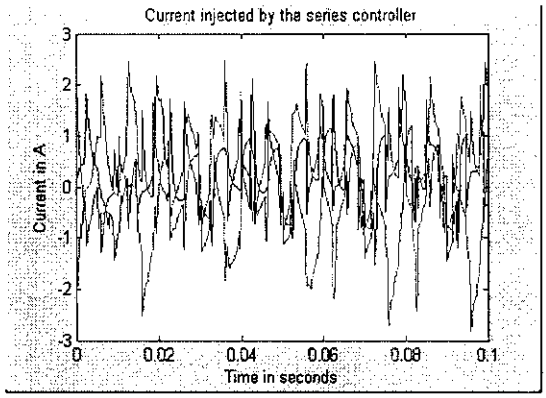



Figure 4.15 Series controller current

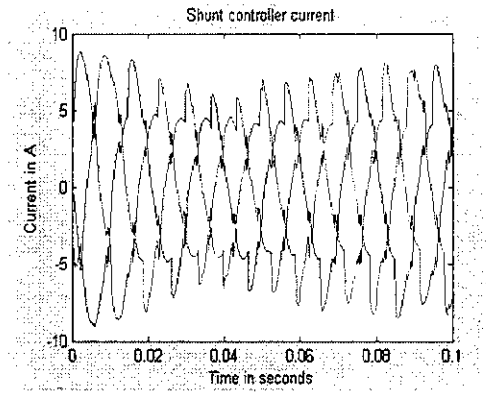



Figure 4.16 Shunt controller current

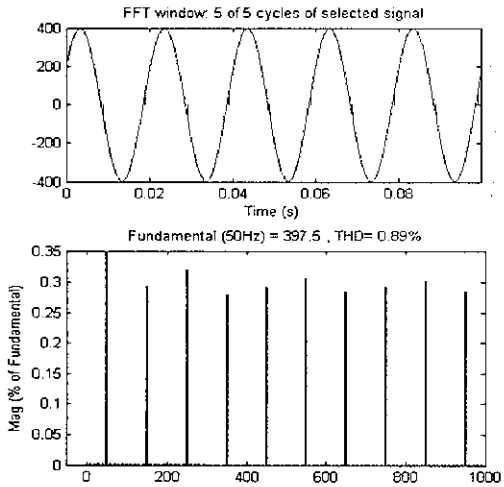



Figure 4.17 Supply voltage THD without Compensator

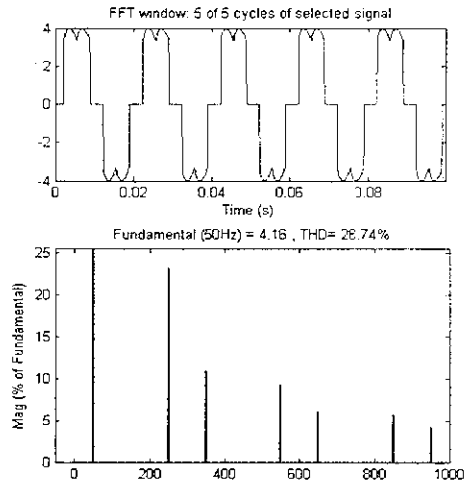



Figure 4.18 Supply current THD without Compensator

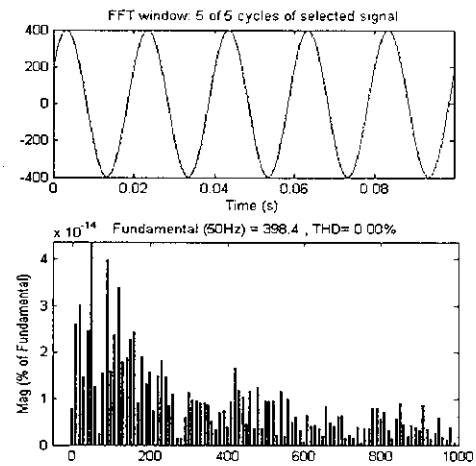



Figure 4.19 Supply voltage THD with Compensator

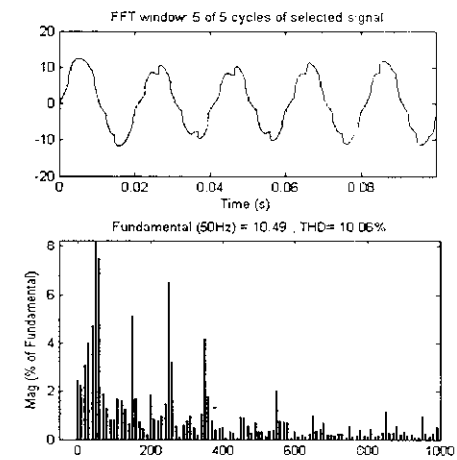



Figure 4.20 Supply current THD with Compensator

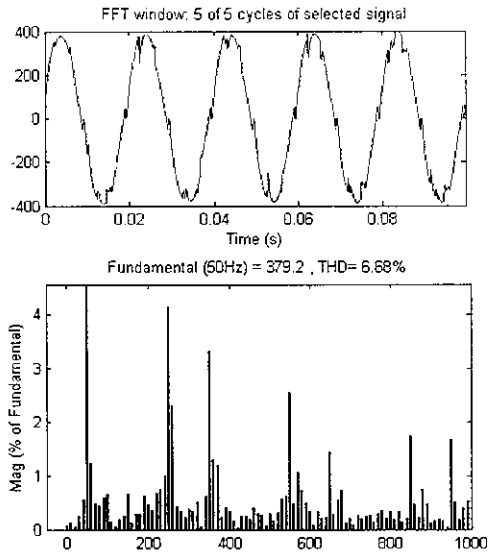



Figure 4.21 Load voltage THD with Compensator

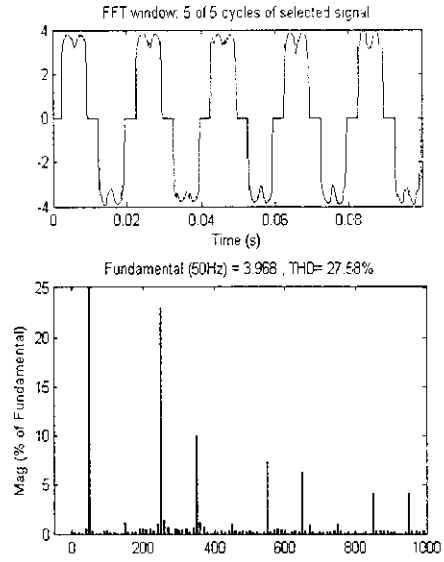



Figure 4.22 Load current THD with Compensator

Table 4.1

Comparison of THD

| Sl.No | Voltage/ Current | Supply/ Load side | With/Without Compensator | THD % |
|---|---|---|---|---|
| 1 | Voltage | Supply side | Without compensator | 0.89 |
| 2 | Current | Supply side | Without compensator | 29.74 |
| 3 | Voltage | Supply side | With compensator | 0.00 |
| 4 | Current | Supply side | With compensator | 10.09 |
| 5 | Voltage | Load side | With compensator | 6.68 |
| 6 | Current | Load side | With compensator | 27.58 |

# CHAPTER 5

# PROTOTYPE OF UPQC WITH WEGS

The purpose of the combined operation of UPQC with WEGS is to supply quality power to the load, whatever may be grid voltage. Here only the interconnected mode is explained. The PIC micro controller used to generate the switching pulses for inverters according to the grid voltage variations. MOSFET is used as switching element in inverters. The optocoupler used to provide isolation between micro controller and MOSFET.

## 5.1 EXPERIMENTAL SETUP OF HARDWARE:

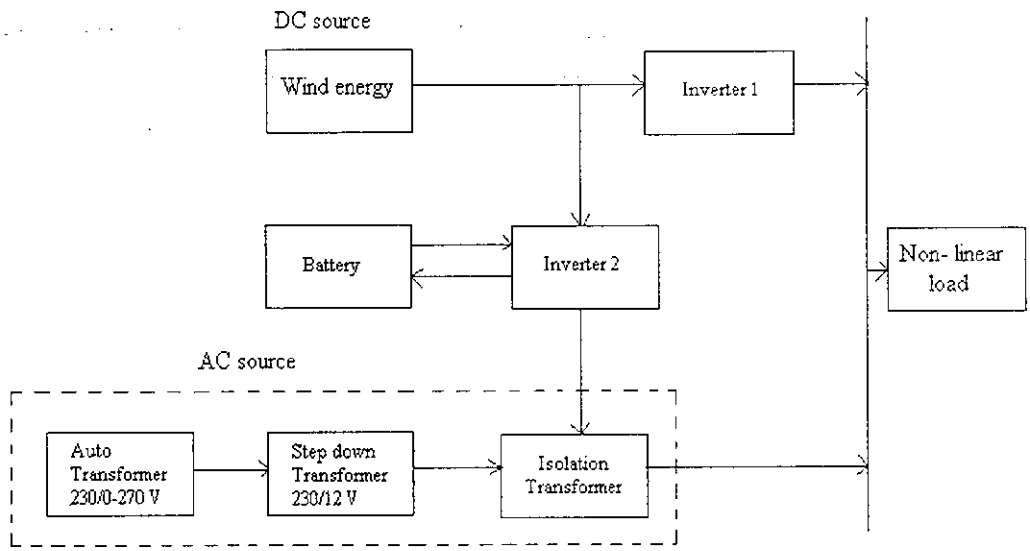



Figure 5.1 Block Diagram of Experimental Setup

## 5.2 OBJECTIBE OF THE HARDWARE:

The figure 5.1 shows the experimental setup of the hardware. Here the grid voltage is represented by AC source. It consists of an autotransformer, to show the grid voltage variations, a step down transformer and an isolation transformer. When the grid voltage is above the specified limit, then it will feed the load. The WEGS is

represented by a DC source. When the gird voltage is less than the specified limit, then the WEGS supplies the power to the grid to compensate the lower voltage. If the grid voltage is too low, and WEGS cant alone compensate it, then the power from the battery is also added to the grid for compensation. In addition, if the WEGS power is too low, at the time of lower wind speed, then the output energy of the WEGS is used to charge the battery unit.

## 5.3 BLOCK DIAGRAM DESCRIPTION:

The entire system can be divided into the following sub-systems for the easiness of understanding.

- 12V DC source
- 230 1ph AC supply
- Series inverter (inverter 1)
- Shunt inverter (inverter2)
- Isolation transformer
- Autotransformer (230/0-270 V)
- PIC micro controller
- Relays
- Optocoupler

The Figure 5.1 shows the experimental setup used in this project. The 1-ph supply is given through a potential transformer 230/0-270 V to a step down transformer 230/12 V. This 12 V ac voltage represents grid supply. It is directly connected to the load through an isolation transformer, 12V/12V .The 12V DC source, which represents windmill output is connected to the load through inverter 1. The series and shunt inverter consist of six MOSFET full bridge inverters. Here the PIC micro controller is generating pulses for the inverters according to the feed back signals from windmill and grid voltage. Relays are used to control the whole operation of the system. Optocoupler isolation is used between power circuit and signal level circuit. A buffer circuit is used for the driving circuit for MOSFET.

## 5.4 DESIGN OF POWER SUPPLY CIRCUIT:

This section introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in figure 5.2. The ac voltage, typically 230V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

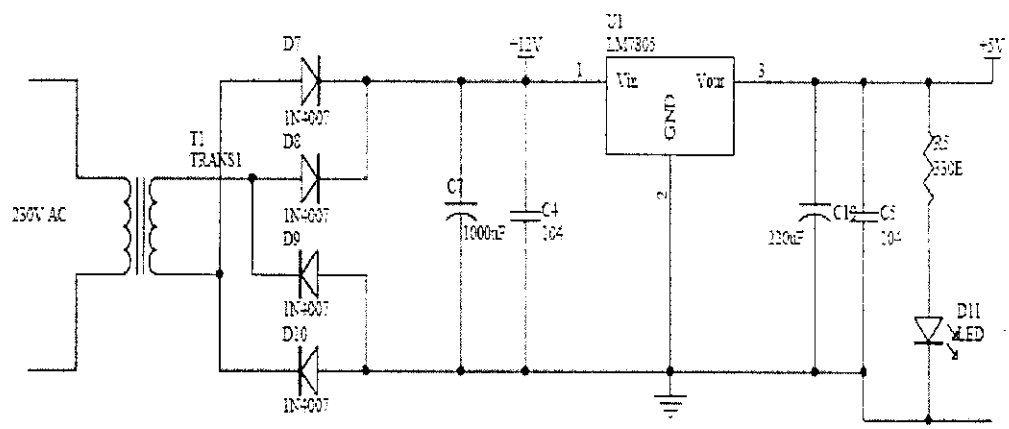



Fig. 5.2 +5 V regulated and +12V unregulated Power supply

The 78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid-state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents. The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating. Considerable effort was expanded to make the 78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply. For output voltage other than 5V, 12V and 15V the 117 series provides an output voltage range from 1.2V to 57V. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

**5.4.1. Step down transformer:**

Alternating current of 230V, 50 Hz supply is given to the primary side of the step down transformer of 230V/ 0-12V type to perform step down operation. The current rating of the transformer is 1A. Now this can be used for rectification purpose.

**5.4.2. Rectifier unit:**

Rectification is achieved using a full bridge rectifier circuit, which comprises of four 1N 4007 solid-state diodes. Two diodes will conduct during the positive cycle and the other two will conduct during the negative half cycle. The output obtained is not a pure DC and therefore filtration has to be done.

### 5.4.3. Filtering unit:

Filter circuits usually consist of a capacitor, which smoothens the pulsating DC. It is helpful in reduction of the ripples from pulsating (1000μF/ 25V) and it maintains stability at the load side (10μF/ 25V).

### 5.4.4. Voltage regulator:

Voltage regulators play an important role in any power supply unit. The primary purpose of a regulator is to aid the rectifier and filter circuit in providing a constant DC voltage to the device. Power supplies without regulators have an inherent problem of changing DC voltage values due to variations in the load or due to fluctuations in the AC line voltage. MC 7805 is used to provide +5V regulated DC supply respectively.

### 5.4.5. Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

## 5.5. MOSFET-FULL BRIDGE INVERTER:

Here three phase full bridge inverter is used for both shunt and series inverters. Each inverter needs six MOSFET. The circuit connection of the full -Bridge inverter is shown in figure 5.3.

### 5.5.1. Advantages of MOSFET:

MOSFETs provide much better system reliability.

- Driver circuitry is simple and cheaper.
- MOSFET's fast switching speeds permit much higher switching frequencies and there by the efficiency are increased.
- Overload and peak current handling capacity is high.

- MOSFETs have better temperature stability.
- MOSFET's leakage current is low.
- Drain-source conduction threshold voltage is absent which eliminates electrical noise.

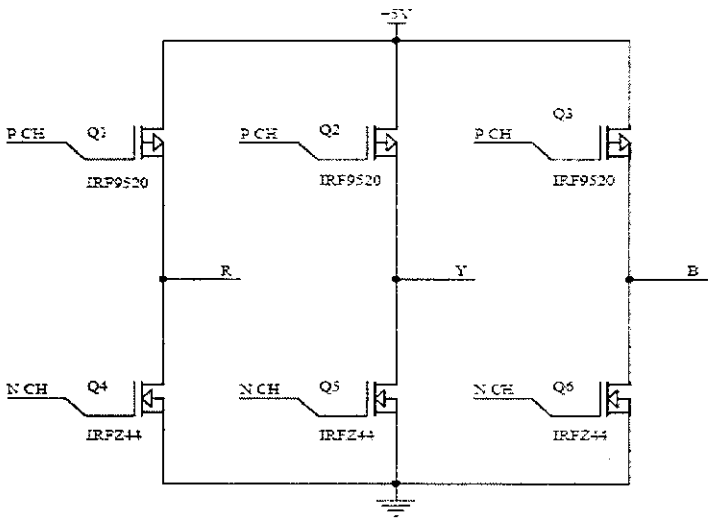



Figure 5.3 3ph full bridge inverter using MOSFET

MOSFETs are able to operate in hazardous radiation environments. Here three P channel IRF9520 MOSFET and three N channel IRFZ44 MOSFETs are used to construct the 3ph full bridge inverter.

**5.5.2. Generation of MOSFET drive signal:**

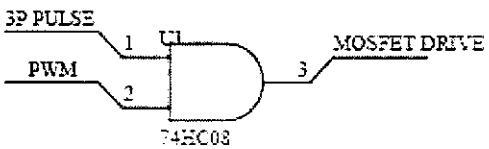



Figure 5.4 Generation of MOSFET drive signal

The figure 5.4 shows how the drive signal is produced for the MOSFET. The PIC controller produces the pulses for the inverter circuit according to the feed back signals. It then mixed with the PWM signals of 100 KHz. Then both are given to an AND gate and the output is used to give as input for the MOSFET driving circuit.

### 5.5.3. MOSFET drive signal:

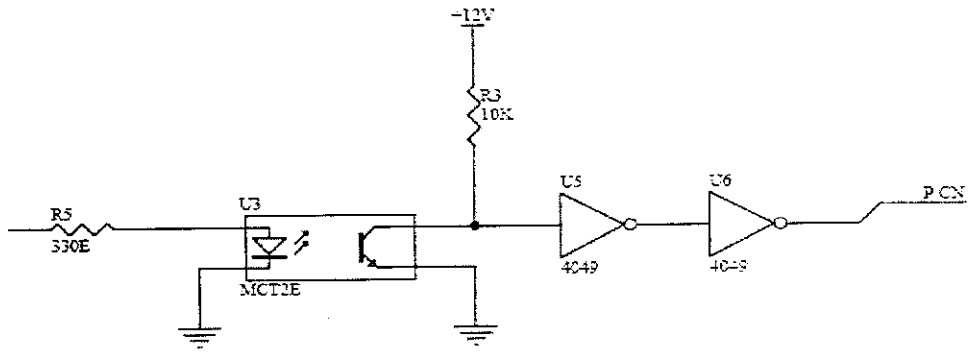



Figure 5.5 Connection diagram of driver circuit for P-channel MOSFET

The figure 5.5 shows the drive circuit for the P-channel MOSFET. Here the drive signal first given to an optocoupler for isolating the signals from the power circuit. Then it is given to two NAND gate circuit to produce the driver signal for the MOSFET of the PWM inverters.

## 5.6 PHOTOTRANSISTOR OPTOCOUPLER:

A phototransistor optocoupler is a combination of a light source and a photosensitive detector. In the optocoupler, or photon coupled pair, the coupling is achieved by light being generated on one side of a transparent insulating gap and being detected on the other side of the gap without an electrical connection between the two sides (except for minor amount of coupling capacitance). In the optocoupler, an infrared light emitting background generates the light, and the photo-detector is a silicon diode, which drives and amplifies, example transistor. The sensitivity of the silicon material peaks at the wavelength emitted by the LED, giving maximum signal coupling.

### 5.6.1. Phototransistor optocoupler MCT2E:

These high-speed optocouplers are designed for use in analog or digital interface applications that require high voltage isolation between the input and output. The MCT2XXX series opto isolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in –line package. Applications include line receivers that require high common mode transient immunity and analog or logic circuits that require input-to-output electrical isolation. The MCT2E each consist of light emitting diode and an integrated photon detector composed of a photodiode and an open-collector output transistors. Separate connections are provided for the photodiode bias and the transistor collect output. This feature reduces the transistor base to collector capacitance, result in speed up to one hundred times that of a conventional phototransistor optocoupler. The MCT2E is designed for wide-band analog applications. The optocoupler schematic diagram is shown the figure 5.6.

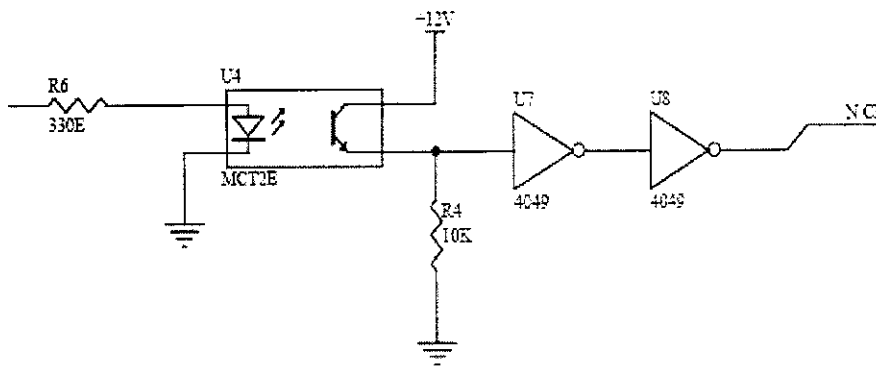



Figure 5.6 Connection diagram of driver circuit for N-channel MOSFET

### 5.7 PULSE GENERATING CIRCUIT:

PIC16F877A micro controller is used as the pulse generating circuit. PIC16F877A is a 40pin; CMOS flash micro controller with A/D controller. It has five I/O ports and has fifteen interrupts. In addition, it has eight A/D channels and the parallel port is implemented in it.

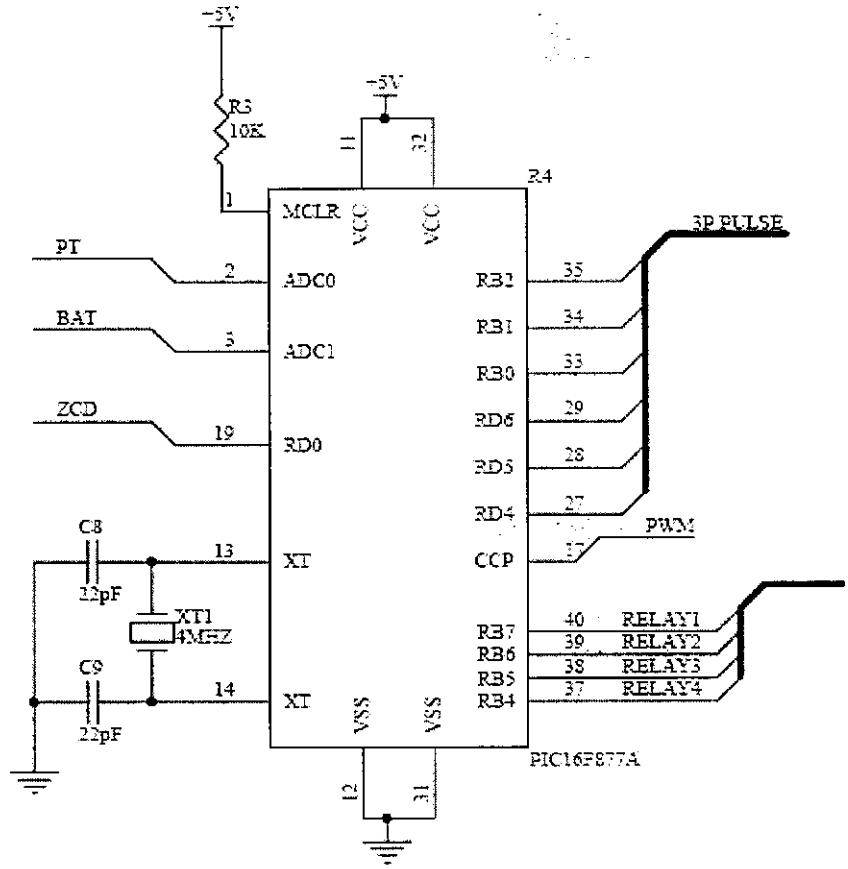



Figure 5.7 Pin configuration used in PIC controller

Pin number 1 is master clear. It is given by +5V supply. Port A is a bi-directional I/O port. Here we configure it as input channel. The potential transformer and battery feed back signals are given as inputs. Port D is also a bi-directional I/O port and configure it as input pin and the zero crossing detector output is given to it. Here we use a crystal oscillator is connected; whose frequency is 4MHz. Pin number 13 and 14 is used for this purpose. Pin numbers 12 and 31 are the ground reference for logic and I/O pins. Therefore, we ground those pins. Pin numbers 11 and 32 are the positive supply for logic and I/O pins. Therefore, we connect +5 V across it. Port B is also a bi-directional port and we configure it as output port. RB0-RB2 configured as output pins to output the PWM pluses. Port D is also a bi-directional port and we use RD4 and RD6 as output pins for PWM pulses. Pins RB4-RB7 used as output pins for the controlling pulses for the relay circuit. Pin number 17 is RC2 which is a bi-

directional pin used here as PWM output pin. The data sheet, pin diagram and features are given in the Appendix B.

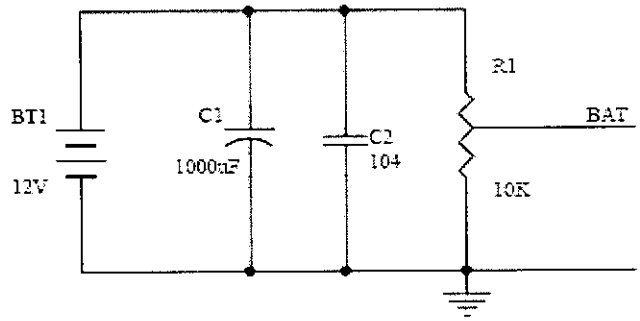



Figure 5.8 Battery feedback signal for PIC controller

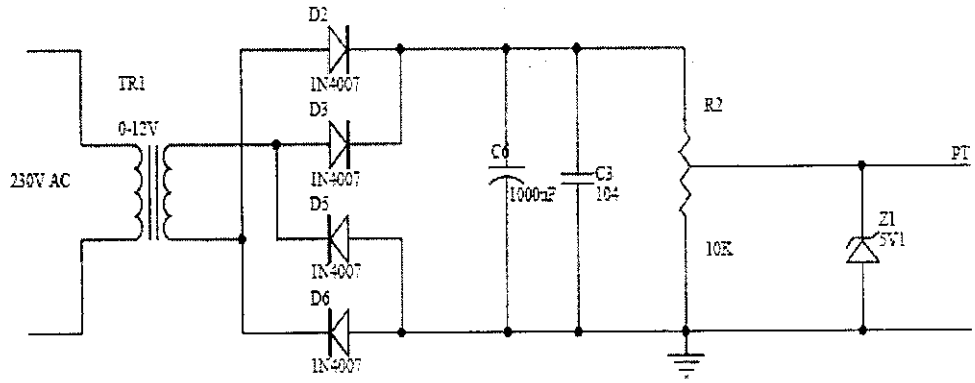



Figure 5.9 Potential transformer feed back signal for PIC controller

### 5.7.1 PWM MODE:

In pulse width modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORT C data latch, the TRISC 2 bit must be cleared to make the CCP1 pin an output. The Block Diagram of the PWM Mode and the PWM output is given in figures 5.11 and 5.12 respectively.

A PWM output has a time-base (period) and a time that the output has high (duty cycle). The frequency of the PWM is the inverse of the period (1/period). The PWM period is specified by writing to the PR2 register. The PWM period is calculated using the following formula:

PWM period = [(PR2) + 1] * 4 *TOSC

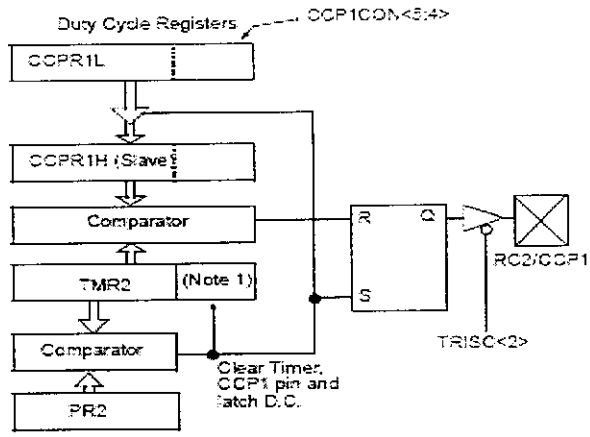



Figure 5.10 Functional Block Diagram of PWM operation

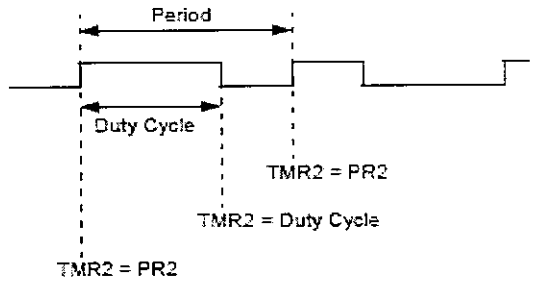



Figure 5.11 PWM output

### 5.7.2 PWM DUTY CYCLE:

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON 5, 4 bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSBs and the CCP1CON5, 4 contains the two LSBs. This 10-bit value is represented by CCPR1L: CCP1CON 5, 4. The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L:CCP1CON 5, 4)*Tosc* (TMR2 prescale value)

CCPR1L and CCP1CON 5,4 can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register. The following steps should be taken when configuring the CCP module for PWM operation:

1.Set the PWM period by writing to the PR2 register.

2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON 5, 4 bits

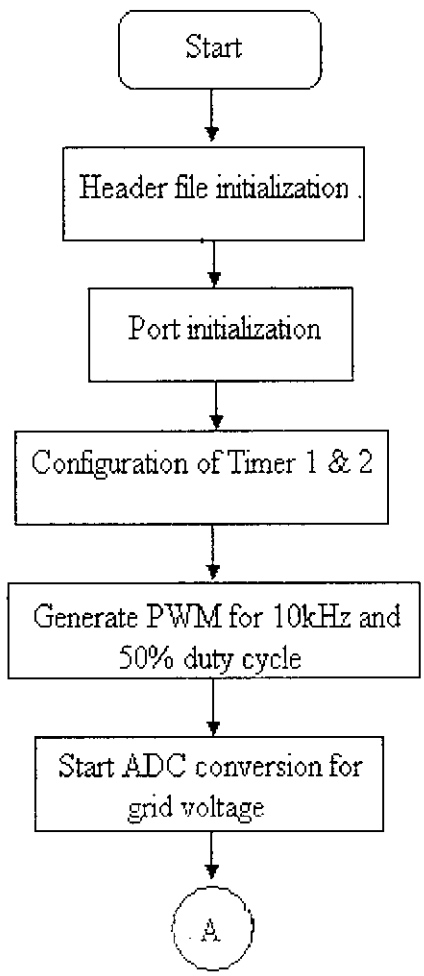
3.Make the CCP1 pin an output by clearing the TRISC 2 bit.

4.Set the TMR2 prescale value and enable Timer2 by writing to T2CON.

5.Configure the CCP1 module for PWM operation.

The program for the PIC micro controller for PWM pulse generation is given in the Appendix A.

**5.7.3 FLOWCHART:**



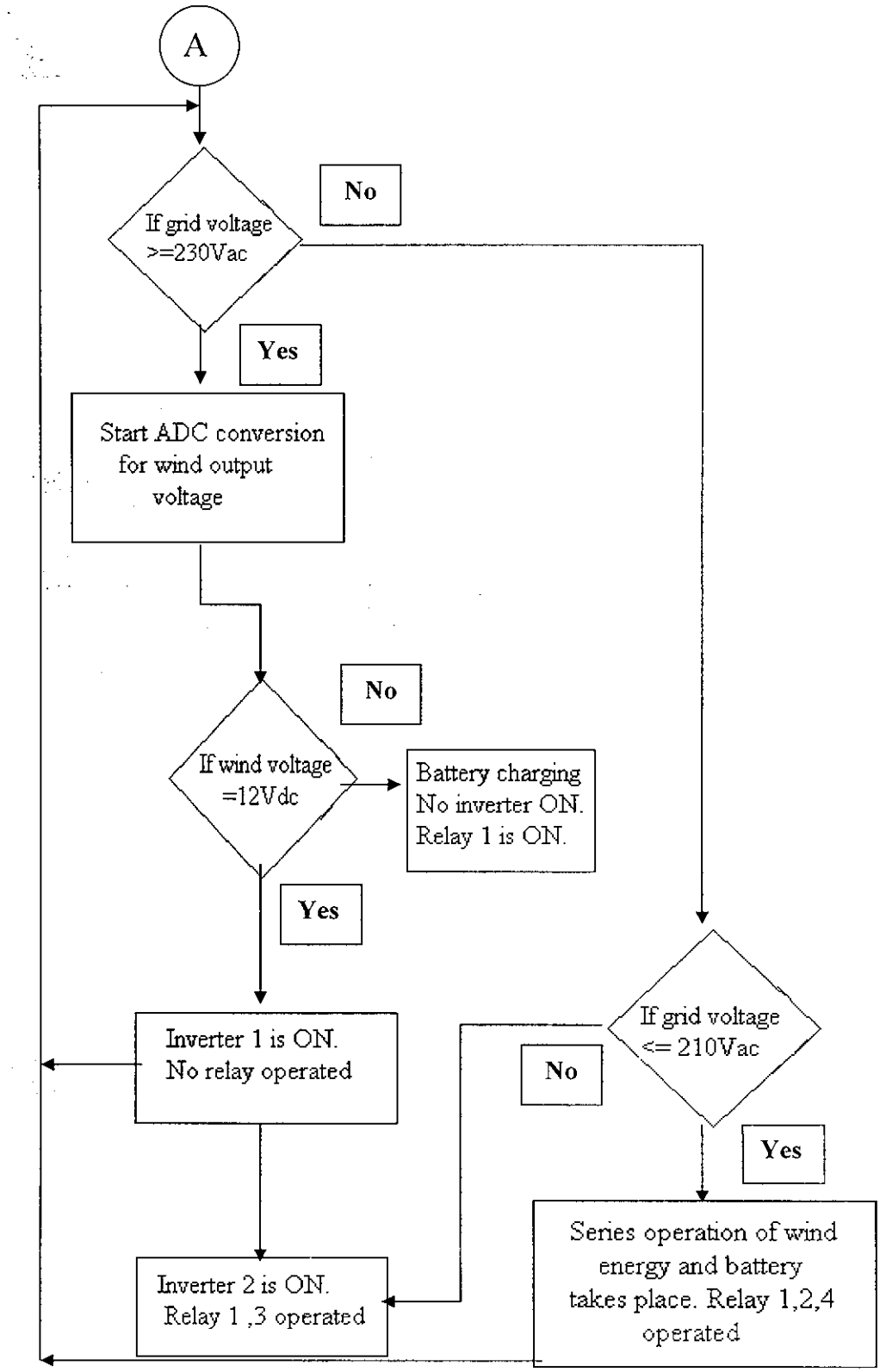



Figure 5.12 Flow chart of the PIC program

## 5.8 RELAY:

The relay circuit used in this hardware implementation is as shown in figure 5.13. There are four relays used, on which two are single pole and other two are double pole. Relays are remote control electrical switches that are controlled by another switch such as computer as in a power train control module. They allow a small current flow circuit to control a higher current circuit. Relay has two circuits, a control circuit and a load circuit. Control circuit has a small control coil while the load circuit has a switch. The coil controls the operation of the switch. When current passes through control coil, an electro magnetic field produce and switch is closed.

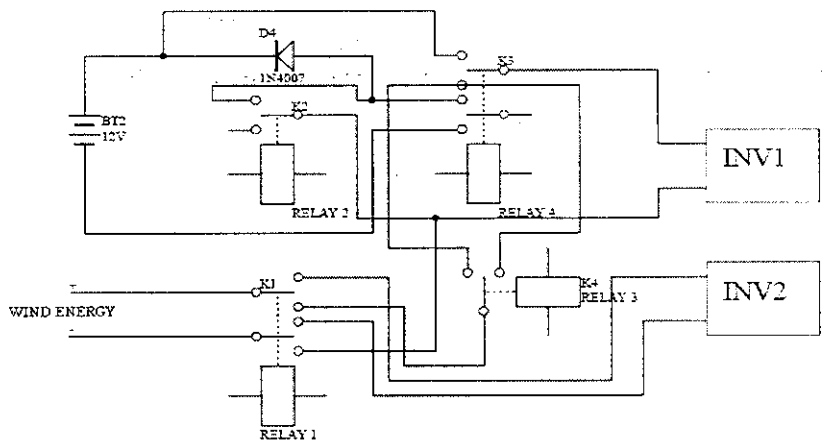



Figure 5.13 Circuit diagram for the relay operation

Table 5.1 Relay operations

| Normal | All relay OFF | Inverter 1 ON |
|---|---|---|
| Decision 1 | Relay 1 ON | Battery charging |
| Decision 2 | Relay 1 and 3 ON | Inverter 2 ON |
| Decision 3 | Realy 1,2,and 4 ON | Series operation of battery and wind energy source |

### 5.8.1 Driver circuit for Relay operation:

In order to amplify the pulses from the PIC controller to the power level, we are using driver circuit for relay. Here we are using ULN2003A Darlington pair for this purpose. It is seven Darlington per pack. The output current is 500mA per driver and output voltage is 50 V. They are 16-pin pack with copper lead frame to reduce the thermal resistance. The connection diagram of relay with the driver circuit is as shown in figure.

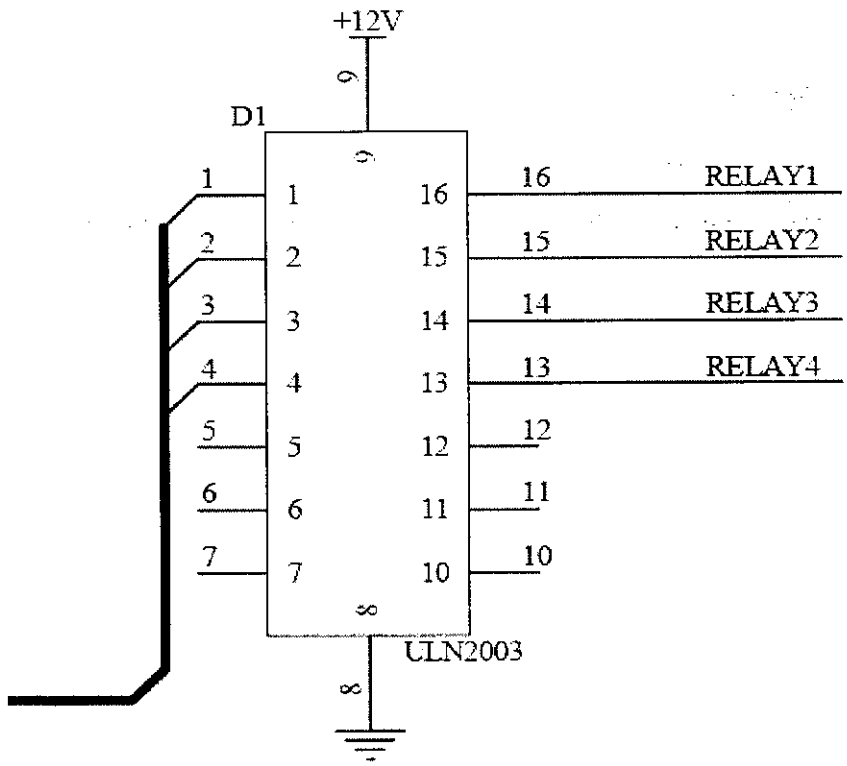



Figure 5.14 Driver circuit for relay operation

Here pins 1-4 are input pins, which are connected to the PIC output pins. Pin 13-16 are output pins, which are connected to the relay coil. Pin 8 is logic ground for the circuit. Pin 9 is positive power supply for the ULN2003, which is connected by a +12 V DC supply.

## 5.9 HARDWARE TESTING RESULTS:

The above hardware is fabricated and tested. The following table shows the test results.

Table 5.2 Hardware operations

| | |
|---|---|
| If grid voltage is greater than or equal to 230 V and Wind output=12V dc | Inverter 1 is ON, no relay operated |
| If grid voltage is less than 230 V and greater than 210 V and Wind output is don't care | Inverter 2 is ON and relay 1 and 3 ON |
| If grid voltage is less than 210 V and Wind output is don't care | Output is available between 12 V DC and battery terminal.No inverter is ON.Relay 1,2 and 4 are ON |
| If grid voltage is greater than or equal to 230 V and Wind output is less than 11V DC | LED glow indicated that battery is charging<br>No inverter is ON.<br>Relay 1 is ON |

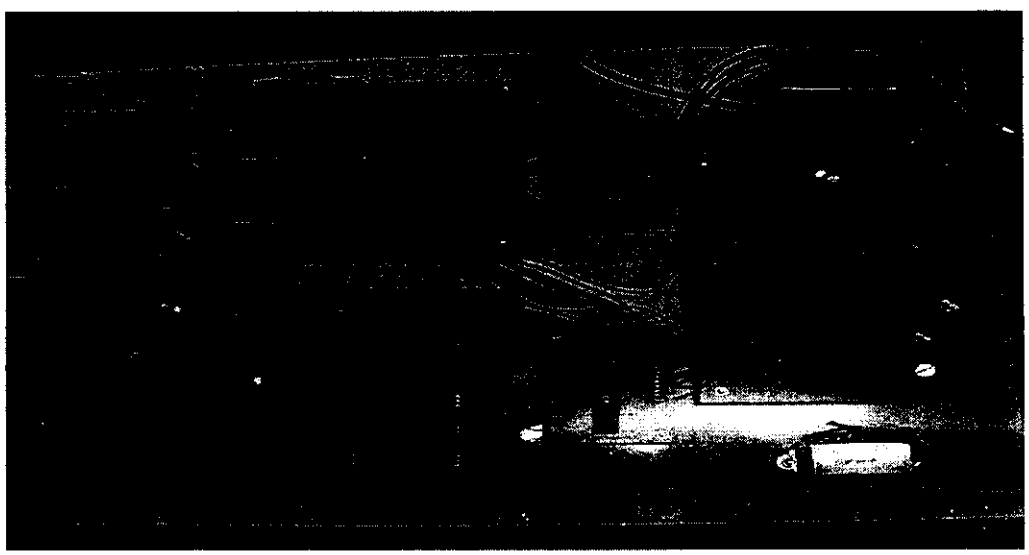


Figure 5.15 Prototype photograph

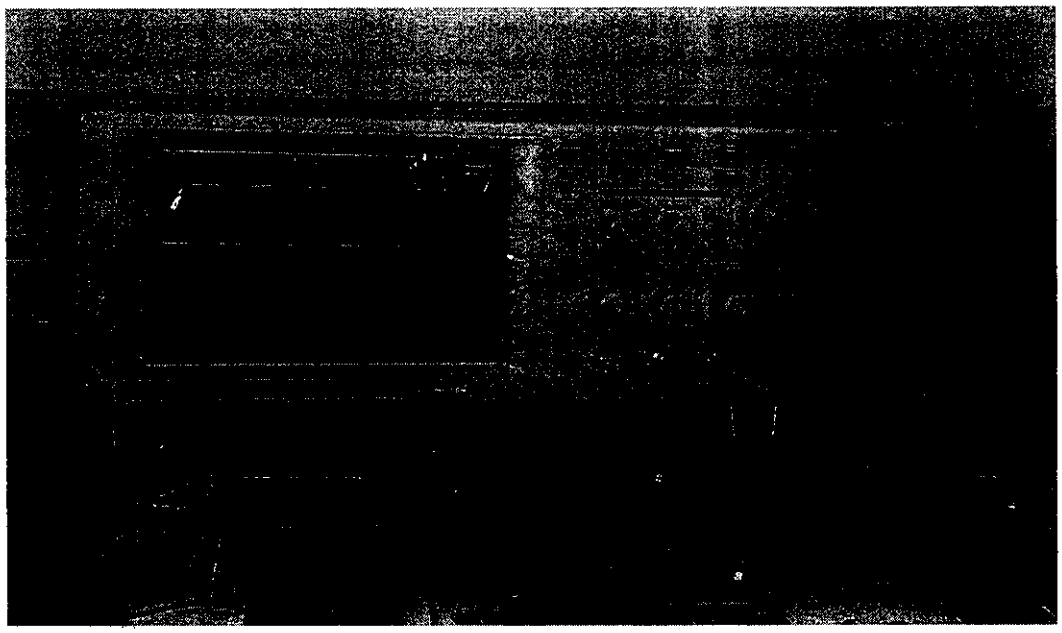


Figure 5.16 Generated pulses

Figure 5.17 PWM pulse with 10KHz and 50%duty cycle

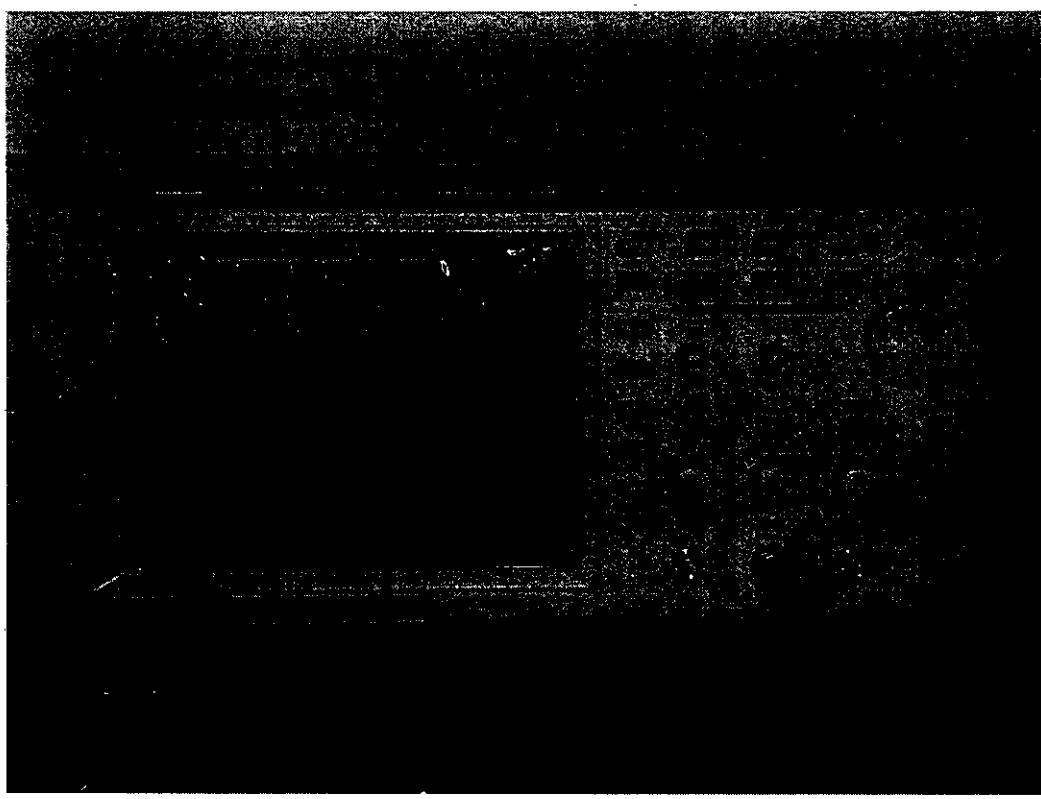


Figure 5.18 Inverter output

# CHAPTER 6

# CONCLUSION AND FUTURE SCOPE

This project describes analysis results of a combined operation of the Unified Power Quality Conditioner with Wind Energy Generation System. The proposed system consists of a series inverter, a shunt inverter and a windmill connected in the DC link. The proposed system can compensate voltage sag and swell, harmonics and reactive power in the interconnected mode. The performance of the proposed system is analyzed using simulation with MATLAB/Simulink. The proposed system can improve the power quality at the point of installation on power distribution system in any non-linear load conditions.

In this work, only interconnected mode is tested. The second mode, i.e. islanding mode can be tested in future work. We can connect a Wind Energy Generating Model in the common DC link, and by controlling the speed of induction generator, we can track maximum power from WEGS. The simulation model described in this report can be utilized as a reference for the development of power systems.

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# APPENDIX A: PIC16F877A

## FEATURES OF PIC16F877A

### High-Performance RISC CPU:

- Only 35 single word instructions to learn.
- All instructions are 1μs (@4MHz) except for program branches, which are 2 cycles.
- Operating speed: DC - 20MHz clock input.

### Peripheral Features:

- Two 8-bit timer/counter (TMR0, TMR2) with 8-bit programmable prescaler.
- One 16-bit timer/counter (TMR1)
- High source/sink current: 25ma
- 12.5 ns resolution for PWM mode.
- Two Capture/Compare PWM (CCP) Modules.
- Brown-out detection circuitry for brown-out Reset (BOR).
- Synchronous serial port (SSP) with SPI (Master mode) and I2C (Master/slave mode).
- Universal synchronous asynchronous receiver/transmitter (USART/SCI) with 9-bit address detection.

### Special Micro controller Features

- Power-On Reset Power-up Timer (PWRT) and Oscillator
- Selectable oscillator options.
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation.
- Self-reprogrammable under software control.
- Power saving Sleep mode.

### CMOS Technology

- Fully static design
- Low power, high speed CMOS FLASH technology
- Wide operating voltage range: 2.0V to 5.0V

- < 0.6 mA typical @ 3V, 4MHz.

**Timing diagram for the generation of pulse by using micro-controller, PIC 16F877A**

- For generating the pulse, timer 1 of PIC16F877A is used.
- The first two sequences are repeated for every 10m
- The last sequence is repeated for every 20ms.
- Whenever the timer 1 is overflow, an interrupt is generated.
- That time, a count variable is increased.
- This count value will be compared with the predefined variable.
- If the present count value is greater than the predefined one, then the pulse will be generated.
- The timer1 is set to overflow for every 0.5ms.

**PIN CONFIGURATION OF PIC16F877:**

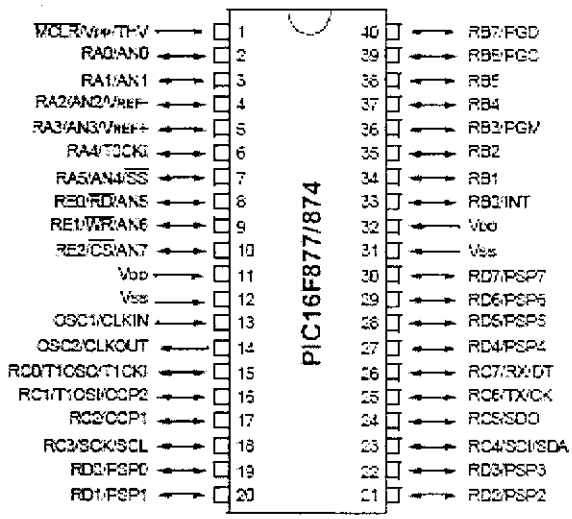



Fig 5.5 Pin diagram of PIC 16F877

**MEMORY ORGANIZATION:**

The PIC16F877 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F877 devices have 8K x 14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h.

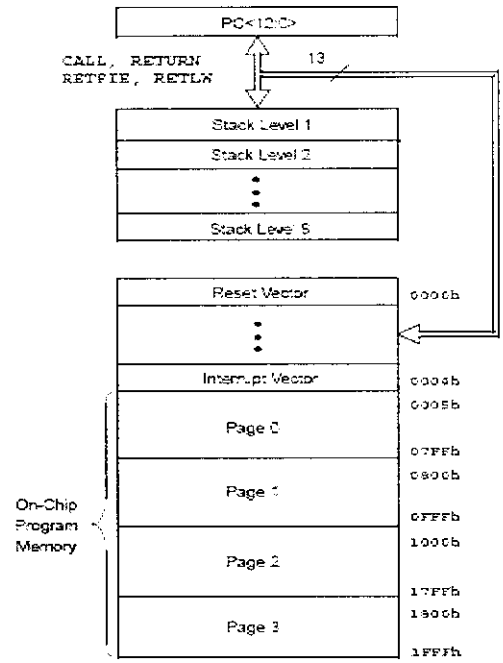



Fig 5.6 Memory Organization of PIC 16F877

**FLASH PROGRAM MEMORY:**

The Data EEPROM and FLASH Program Memory are readable and writable during normal operation over the entire VDD range. The data memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (SFR). There are six SFRs used to read and write the program and data EEPROM memory.

These registers are:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

The PIC 16F877 also has three timers namely:

- Timer 0 Module
- Timer 1 Module
- Timer 2 Module

**TIMER 0 MODE:**

Timer mode is selected by clearing bit T0CS (OPTION_REG 5). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler).Counter mode is selected by setting bit T0CS (OPTION_REG 5). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE of (OPTION_REG 4). Clearing bit T0SE selects the rising edge. The prescaler is mutually exclusively shared between the Timer0 module and the watchdog timer.

**TIMER 1 MODE:**

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L), which are readable and writable. The TMR1 Register pair (TMR1H: TMR1L) increments from 0000h to FFFFh and rolls over to 0000h.Timer1 can operate in one of two modes:

- As a timer
- As a counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON 1).In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON 0).

**TIMER 2 MODE:**

Timer 2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device reset. The Timer2 module has an 8-bit period register PR2.Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

**CAPTURE/COMPARE/PWM MODES:**

Each Capture/Compare/PWM (CCP) mode contains a 16-bit register, which can operate as, a :

- 16-bit Capture register
- 16-bit Compare register

• PWM master/slave Duty Cycle register

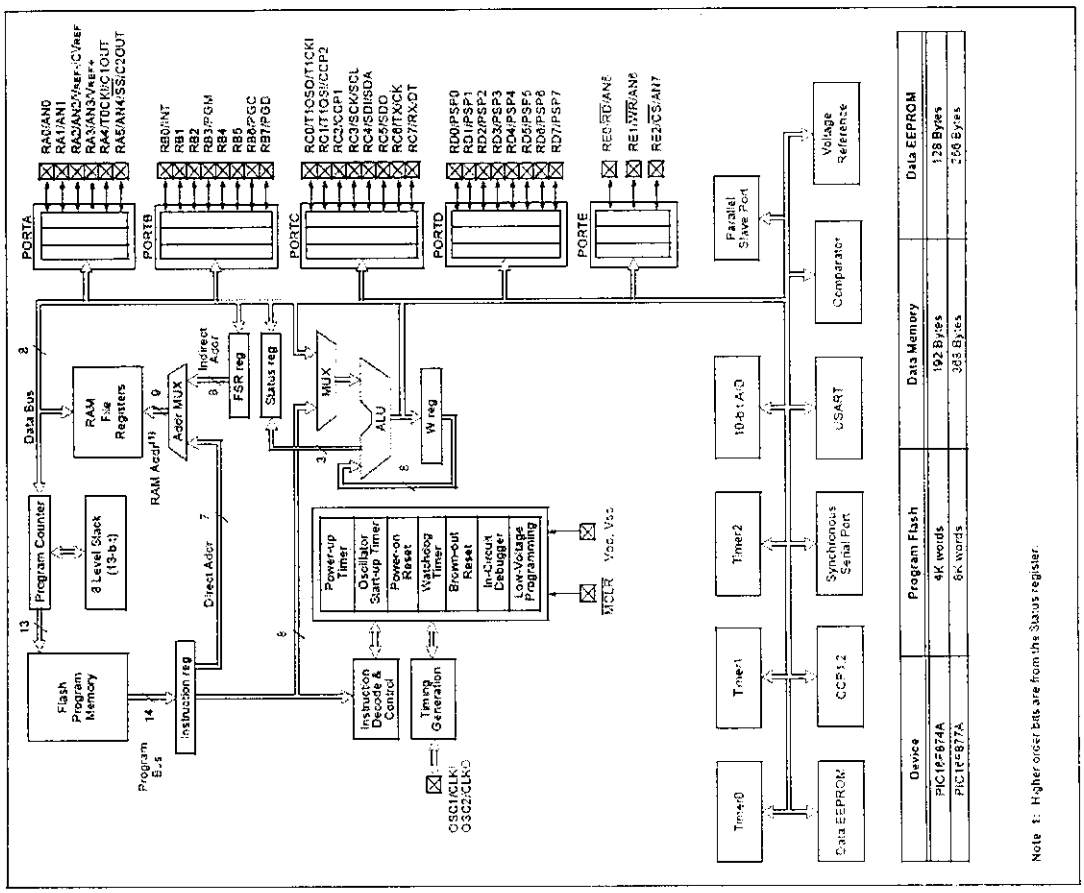
Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger.

**CCP 1 MODE:**

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

**CCP 2 MODE:**

Capture/Compare/PWM Register 2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer 2 and start an A/D conversion.




Block diagram of 16F877A

## APPENDIX B: PIC PROGRAMMING:

```
#include<pic.h>
unsigned int RES=0;
unsigned char count=0;
unsigned char ct_rly=0;

#define relay1 RB7
#define relay2 RB6
#define relay3 RB5
#define relay4 RB4

#define S1 RB1
#define S2 RD5
#define S3 RD6
#define S4 RB2
#define S5 RD4
#define S6 RB0

__CONFIG(WDTDIS & XT & PWRTEN & BOREN & LVPDIS);
void main()
{
        TRISA=0X1F;
        TRISB=0;
        TRISC=0;

      TRISD=0X0F;
```

```
 PORTB=0;
 PORTC=0;
 PORTD=0;

T1CON=0X01;
 TMR1H=0XF2;
 TMR1L=0XFB;
 ADCON1=0X82;
 T2CON=0X04;
 PR2=99;

CCP1CON=0X0C;
 CCPR1L=50;
 GIE=PEIE=TMR1IE=1;
 while(1)
 {
      ADCON0=0X89;
        delay();
        ADGO=1;
        delay();
        while(ADGO);
        RES=ADRESH*256+ADRESL;
        RES=RES/2;
        if(RES<210)
        {
             relay3=0;
```

```
        relay1=1;
        relay2=1;
        relay4=1;
}
else if(RES<230)
{
        relay2=0;
        relay4=0;
        relay1=1;
        relay3=1;
}
else
{
        relay3=0;
        relay2=0;
        relay4=0;
        ADCON0=0X91;
        delay();
        ADGO=1;
        delay();
        while(ADGO);
        RES=ADRESH*256+ADRESL;
        RES=RES/2;
        if(RES<350)             // 11.5 volt
        {
                ct_rly++;
                if(ct_rly>20)
```

```
                {
                        ct_rly=20;
                        relay1=1;
                }
        }
        else
        {
                ct_rly=0;
                relay1=0;
        }

    }

        delay1();

        delay();
    }
}

void interrupt isr()
{
    if(TMR1IF==1)
    {
        TMR1IF=0;
        TMR1H=0XF2;
        TMR1L=0XFB;
//      TMR1H=0XFF;
```

```
//              TMR1L=0XC8;

                count++;
                if(count==1)
                {
                        S2=1;
                        S6=0;
                }
                if(count==2)
                {
                        S1=1;
                        S3=0;
                }
                if(count==3)
                {
                        S2=0;
                        S4=1;
                }
                if(count==4)
                {
                        S3=1;
                        S5=0;
                }
                if(count==5)
                {
                        S6=1;
                        S4=0;
```

```
                }
                if(count==6)
                {
                        count=0;
                        S5=1;
                        S1=0;
                }
        }
}
delay()
{
        unsigned int i;
        for(i=0;i<=400;i++);
}
delay1()
{
        unsigned int i;
        for(i=0;i<50000;i++);
}
```

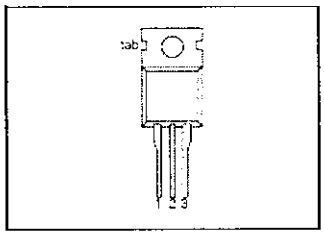
## APPENDIX C:

# N-channel enhancement mode TrenchMOS™ transistor

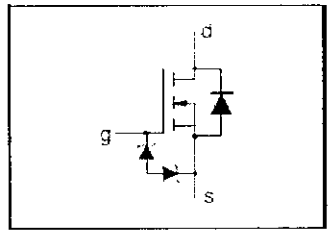
**PINNING - TO220AB**

| PIN | DESCRIPTION |
|---|---|
| 1 | gate |
| 2 | drain |
| 3 | source |
| tab | drain |

**PIN CONFIGURATION**




**SYMBOL**




## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 55 | V |
| $I_D$ | Drain current (DC) | 49 | A |
| $P_{tot}$ | Total power dissipation | 110 | W |
| $T_j$ | Junction temperature | 175 | °C |
| $R_{DS(ON)}$ | Drain-source on-state resistance $V_{GS}$ = 10 V | 22 | mΩ |

### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | - | - | 55 | V |
| $V_{DGR}$ | Drain-gate voltage | $R_{GS}$ = 20 kΩ | - | 55 | V |
| $\pm V_{GS}$ | Gate-source voltage | - | - | 20 | V |
| $I_D$ | Drain current (DC) | $T_{mb}$ = 25 °C | - | 49 | A |
| $I_D$ | Drain current (DC) | $T_{mb}$ = 100 °C | - | 35 | A |
| $I_{DM}$ | Drain current (pulse peak value) | $T_{mb}$ = 25 °C | - | 160 | A |
| $P_{tot}$ | Total power dissipation | $T_{mb}$ = 25 °C | - | 110 | W |
| $T_{stg}$, $T_j$ | Storage & operating temperature | - | - 55 | 175 | °C |

### ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_C$ | Electrostatic discharge capacitor voltage, all pins | Human body model (100 pF, 1.5 kΩ) | - | 2 | kV |

### THERMAL RESISTANCES

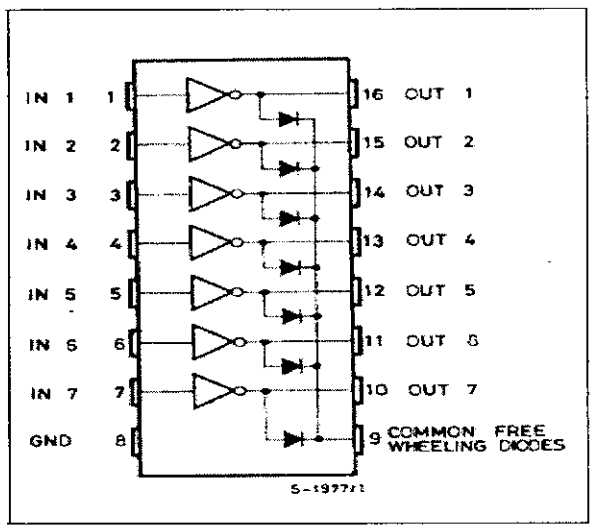
| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $R_{th\,j\text{-}mb}$ | Thermal resistance junction to mounting base | - | - | 1.4 | K/W |
| $R_{th\,j\text{-}a}$ | Thermal resistance junction to ambient | in free air | 60 | - | K/W |

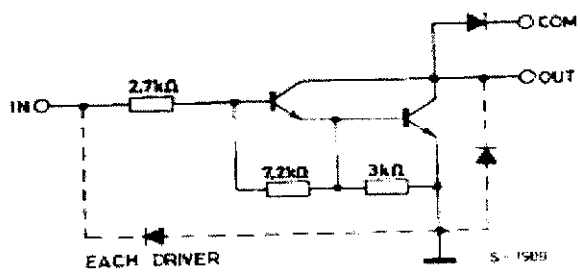
# ULN2003A

## SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRATED SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

PIN CONNECTION




Series ULN-2003A
(each driver)

# PHOTOTRANSISTOR OPTOCOUPLERS
# MCT2E

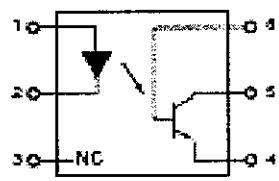
## DESCRIPTION

The MCT2XXX series optoisolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package.

## FEATURES

- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  -Add option V for white package (e.g., MCT2V-M)
  -Add option 300 for black package (e.g., MCT2.300)
- MCT2 and MCT2E are also available in white package by specifying -M suffix, eg. MCT2-M

**SCHEMATIC**




PIN 1. ANODE
2. CATHODE
3. NO CONNECTION
4. EMITTER
5. COLLECTOR
6. BASE

## APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

National Semiconductor

June 1989

# 54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

## General Description

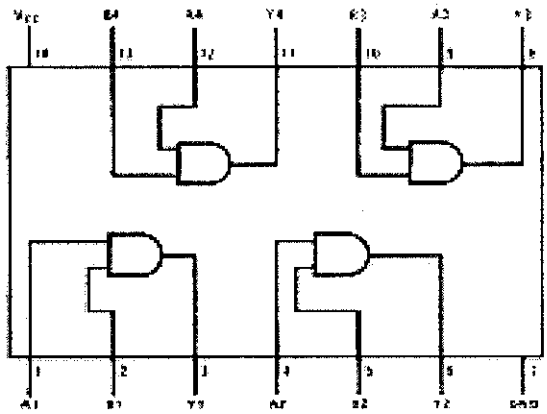
This device contains four independent gates each of which performs the logic AND function.

## Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

## Connection Diagram

Dual-In-Line Package



TL/F/6347–1

Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$Y = AB$

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = High Logic Level

L = Low Logic Level

# MC78XX/LM78XX/MC78XXA

## 3-Terminal 1A Positive Voltage Regulator

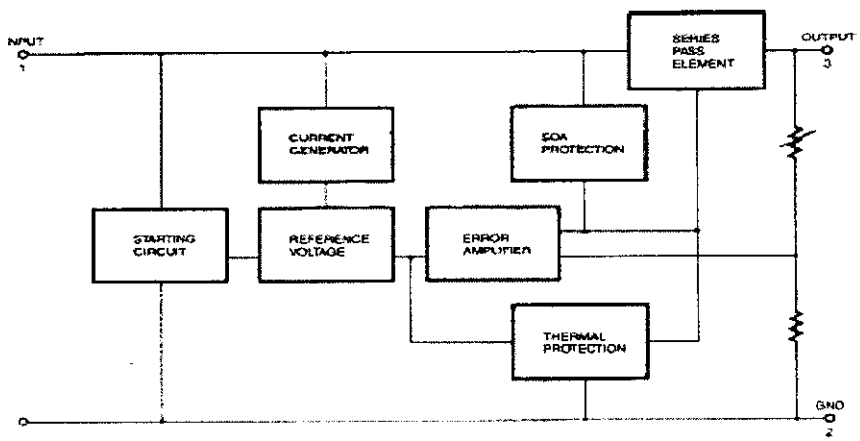
## Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

## Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

## Internal Block Digram



# CD4049UBC • CD4050BC
# Hex Inverting Buffer • Hex Non-Inverting Buffer

## General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage ($V_{DD}$). The input signal high level ($V_{IH}$) can exceed the $V_{DD}$ supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at $V_{DD}$ = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

## Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than $V_{DD}$

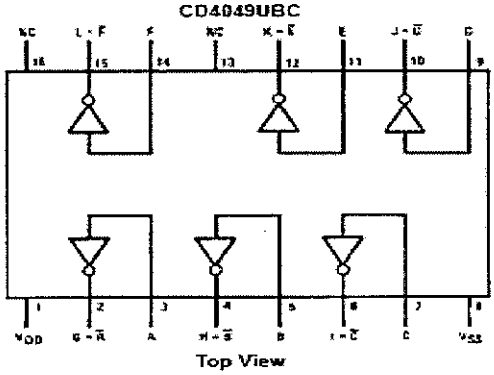
## Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS HIGH-to-LOW logic level converter

## Connection Diagrams

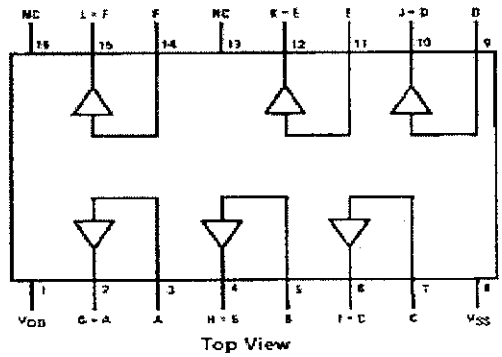
Pin Assignments for DIP

CD4049UBC



Top View

CD4050BC



Top View

# 6A, 100V, 0.600 Ohm, P-Channel Power MOSFET

# IRF9520

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17501.

## Features

- 6A, 100V
- $r_{DS(ON)} = 0.600\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

## Symbol