DESIGN AND IMPLEMENTATION OF AN IMPEDANCE SOURCE INVERTER WITH FPGA SYSTEM

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BONAFIDE CERTIFICATE

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ABSTRACT

This project presents an Impedance Source power Converter with FPGA system and its control method of implementing ac-ac, ac-dc, dc-ac, dc-dc power conversion. The Impedance Source Inverter is a network which couples the main circuit along with the power circuit thus reducing the power stages which cannot be obtained when using a voltage or current source inverter where a capacitor or inductor is used respectively. The impedance source inverter overcomes the barriers and limitations of a traditional voltage and current source inverter. The Z-source inverter system employs a unique *LC* network in the dc link and a small capacitor on the ac side of the diode front end. By controlling the shoot-through duty cycle, the Z-source can produce any desired output ac voltage, even greater than the line voltage.

This project has been implemented in three levels such as

- Matlab simulation of Impedance Source Inverter.
- VLSI simulation of generating PWM pulses.
- Embedded system based hardware implementation.

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CONTENTS

CHAPTER 3. DESIGN OF Z-SOURCE INVERTER

CHAPTER 4. SIMULATION OF Z SOURCE INVERTER

CHAPTER 5. HARDWARE SIMULATION IN FPGA SYSTEM WITH PWM TECHNIQUE

LIST OF FIGURES

LIST OF SYMBOLS

SYMBOL	UNIT	DESCRIPTION
B	-	Boost Factor
B_b	-	Buck-Boost Factor
C	-	Capacitance
d_s	-	Duty cycle of the shoot –through
D_s	-	Diode
E_s	V	Voltage Source of ZSI
I_c	A	Capacitor current of ZSI
I_i	A	Current at the output terminal
I	A	Inductance current of ZSI
I_s	A	Input Current at the terminals of impedance network
I_{fA}	A	Final value of current in Active- 1
I_{fS}	A	Final value of current in Shoot-Through
I_{iA}	A	Initial value of current in Active- 1
I_{iS}	A	Initial value of current in Shoot-Through
K		Ratio of peak ripples to their average
L	H	Inductance
M	-	Modulation Index
t_s	sec	Shoot-Through-1 state
t_A	sec	Active-1 state
T	sec	Total time period

T_s	sec	Period of the switching cycle of VSI
T_1	sec	Non-Shoot -Through period
v_a	V	Phase A inverter output voltage
V_{ac}	V	Output line voltage of Z-source inverter
v_b	V	Phase B inverter output voltage
v_c	V	Phase C inverter output voltage
V_c	V	Capacitor Voltage
V_{ciA}	V	Initial capacitor voltage in active
V_{cfS}	V	Final capacitor voltage in active
V_{cmin}	V	Minimum capacitor voltage
V_{dc}	V	DC voltage
V_i	V	Voltage at the output terminal connected to the VSI
V_L	V	Inductance voltage
V_s	V	Source voltage

CHAPTER 1

BASIC CONSIDERATION

1.1 Introduction:

The Z-Source Inverter (ZSI) system employs a unique LC network in the dc link and a small capacitor on the ac side of the diode front end. By controlling the Shoot-Through duty cycle, the Z-source can produce any desired output ac voltage, even greater than the line voltage. As a result, the new ZSI system provides ride-through capability during voltage sags, reduces line harmonics, improves power factor and reliability, and extends output voltage range.

1.2 Traditional Inverters:

1.2.1 Inverter:

Traditionally, power inverters can be broadly classified as either the Voltage Source Inverter (VSI) or Current Source Inverter (CSI) type. For a VSI the inverter is fed from a dc voltage source usually with a relatively large capacitor connected in parallel. It is well known that the maximum ac voltage output of a VSI is limited to 1.15 times half the dc source voltage (using modulation strategies with offsets added) before being over-modulated. The VSI can therefore only be used for buck (step-down) dc-ac power conversion or boost (step-up) ac-ac power rectification assuming that no additional dc-dc inverter is used to buck/boost the dc link voltage. On the other hand, a CSI is fed from a dc current source, which is usually implemented by connecting a dc source in series with a relatively large inductor and its ac voltage output is always greater than the dc source voltage that feeds the dc-side inductor. The CSI is therefore only suitable for boost dc-ac power conversion or buck ac-dc power rectification.

1.2.2 Voltage Source Inverter:

Fig. 1.1 shows the traditional VSI structure. A dc voltage source supported by a relatively large capacitor feeds the main inverter circuit, a three-phase bridge. The dc voltage-source can be a battery, fuel-cell stack, diode rectifier and/or capacitor. Six

switches are used in the main circuit; each is traditionally composed of a power transistor and an anti-parallel (or freewheeling) diode to provide bidirectional current flow and unidirectional voltages blocking capability.

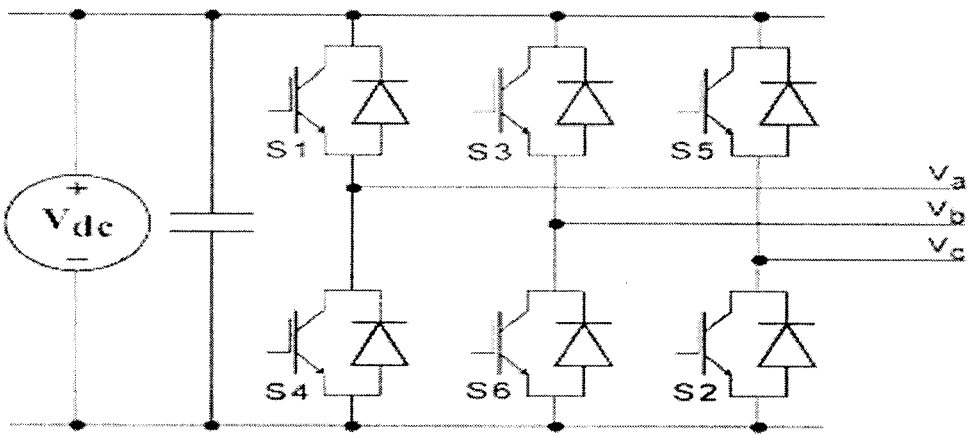


Fig. 1.1 Traditional Voltage Source Inverter

1.2.3 Current Source Inverter:

Fig. 1.2 shows the traditional three-phase CSI structure. A dc current source feeds the main inverter circuit, a three-phase bridge. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel cell stack, diode rectifier, or thyristor inverter. Six switches are used in the main circuit, each is traditionally composed of a semiconductor switching device with reverse blocking capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking.

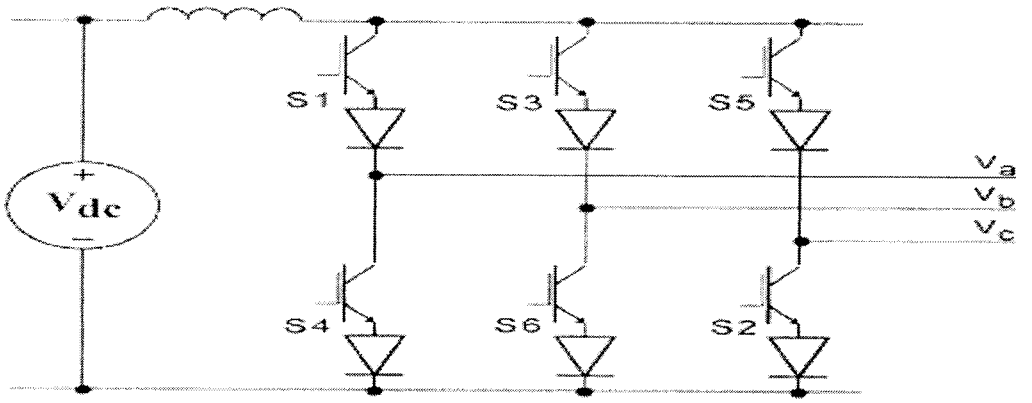


Fig. 1.2 Traditional Current Source Inverter

1.2.4 Drawbacks:

The VSI has the following conceptual and theoretical barriers and limitations.

1. The ac output voltage is limited below and cannot exceed the dc-rail voltage or the dc-rail voltage has to be greater than the ac input voltage. Therefore, the VSI is a buck (step-down) inverter for dc-to-ac power conversion and the VSI is a boost (step-up) rectifier (or boost converter) for ac-to-dc power conversion. For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost inverter is needed to obtain a desired ac output. The additional power inverter stage increases system cost and lowers efficiency.
2. The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a Shoot-Through would occur and destroy the devices. The shoot-Through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the converter's reliability. Dead time to block both upper and lower devices has to be provided in the VSI, which causes waveform distortion.
3. An output LC filter is needed for providing a sinusoidal voltage compared with the CSI, which causes additional power loss and control complexity.

The CSI has the following conceptual and theoretical barriers and limitations,

1. The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. Therefore the CSI is a boost inverter for dc-dc power conversion and the CSI is a buck rectifier for ac-ac power conversion. For applications where a over drive is desirable, an additional dc-dc buck (or boost) converter is needed. The additional power conversion stage increases system cost and lowers efficiency.
2. At least one of the upper devices and one of the lower devices have to be gated on and maintained on any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open circuit problem by EMI noise's misgating-off is a major concern of the inverter's reliability. Overlap time for safe current communication is needed in the CSI, which also causes waveform distortion.
3. The main switches of the CSI have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high-performance IGBT modules.

In addition both the VSI and the CSI have the following common problems,

1. They are either a boost or a buck converter and cannot be a buck-boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage.

2. Their main circuits cannot be interchangeable. In other words, neither the VSI main circuit can be used for the CSI nor vice versa.

3. They are vulnerable to EMI noise in terms of reliability.

1.3 Impedance Source Inverter:

To overcome the above problems of the traditional VSI and CSI, an impedance-source (or impedance-fed) power inverter and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion is proposed. Fig. 2.3 shows the general ZSI structure proposed. It employs a unique impedance network to couple the

inverter main circuit to the power source, load, or another inverter, for providing unique features that cannot be observed in the traditional VSI and CSI where a capacitor and inductor are used, respectively.

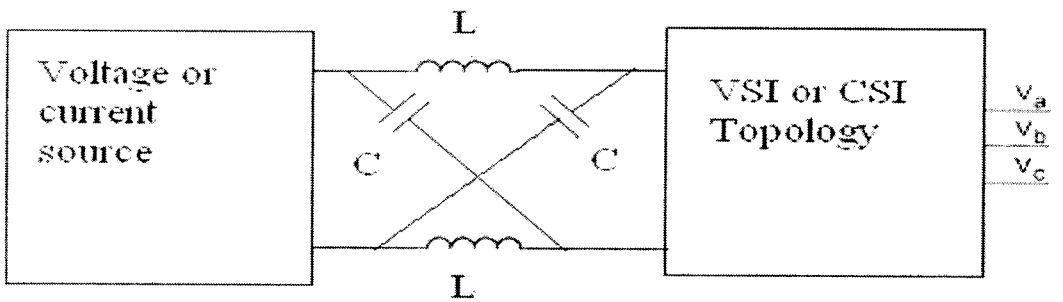


Fig. 1.3 Z-Source Inverter

1.3.1 Advantages:

The ZSI overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional VSI and CSI provides a novel power conversion concept.

1.3.2 Objective of the project

To design an Impedance Source Inverter with Field Program Gate Array (FPGA) to improve the efficiency and reduce the power stages in Permanent Magnet Wind Energy System.

Table 1.1 Comparison of ZSI with Traditional Inverters

Current Source Inverter(CSI)	VoltageSourceInverter(VSI)	Impedance SourceInverter(ZSI)
1. As inductor is used in the dc link, the source impedance is high. .A constant current source is realized.	As capacitor is used in the dc link, it acts as a low impedance voltage source.	As capacitor and inductor are used in the dc link, it acts as a constant high impedance voltage source.
2. A current source inverter is capable of withstanding short circuit across any two of its output terminals. Hence momentary short circuit on load and mis-firing of switches are acceptable.	A VSI leads to dangerous situation as the parallel capacitor could feed more power into the fault.	In ZSI mis-firing of the switches may be acceptable.
3. Used in buck or boost operation of the inverter.	Used in a buck mode of operation of inverter.	Used in both buck and boost operating modes of Inverter.
4. Affected by the EMI noise.	Affected by the EMI noise	Less affected by the EMI noise. Impedance Source act as a filter
5. Considerable amount of harmonic distortion	Considerable amount of harmonic distortion	Harmonics distortion is low
6.Low efficiency because of power loss	Low efficiency because of high power loss	Higher efficiency because of low power loss

CHAPTER 2

IMPEDANCE SOURCE NETWORK

2.1 Structure of Z Source

ZSI appears to be gaining popularity over the others mainly because it continues to employ a conventional VSI as the power inverter yet with a modified dc link. An impedance network connected between the variable dc voltage source and the conventional VSI are the main differences in the power circuit. As seen in the figure 2.1, a symmetrical impedance network consists of two identical inductors and two identical capacitors connected in a specific manner to achieve the desired properties. The impedance network changes the circuit configuration from that of a voltage source to an impedance source. It allows the VSI to be operated in a new state called the Shoot-Through state in which the two switching devices in the same leg are simultaneously switched-on to effect a short-circuit of the dc link. During this state, energy is transferred from the capacitors to inductors, thereby giving rise to the voltage boost capability of the ZSI. As the capacitors may be charged to higher voltages than the input source voltage, the diode D_s is necessary to prevent discharging of them through the input source.

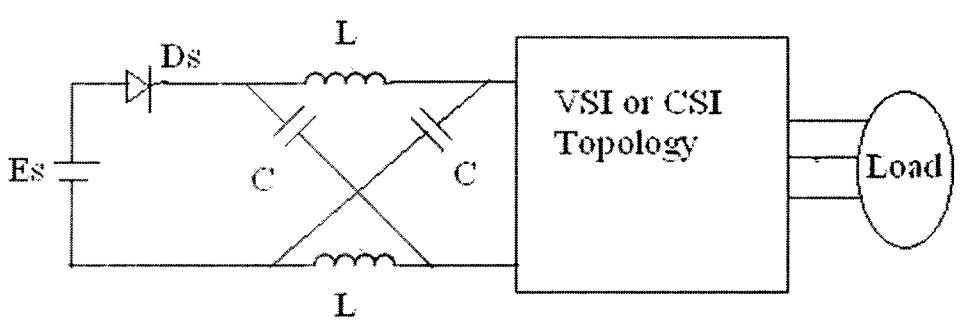


Fig 2.1 ZSI based on a conventional VSI

2.2 Operating states of the impedance network:

The operating states of the impedance network at the dc link is decided by the switching states of the semiconductor devices on its input and output terminals. As illustrated in Fig.2.2, the diode D_s on its input side has two switching states as 'On' and 'Off' and the VSI on its output side has three switching states as 1, 2& 3.

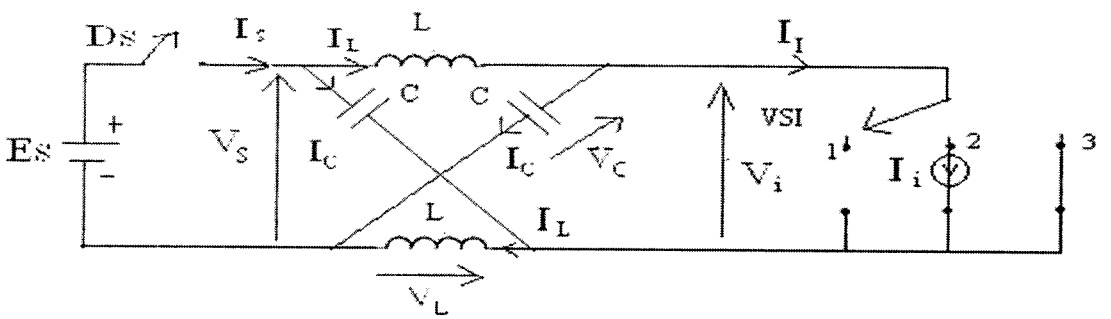


Fig.2.2 Switching equivalent of Z source Inverter

Thus, in general, the impedance network of the ZSI at a given time can operate in any one of the six possible states given in Table 2.1.

Table 2.1 Possible operating states of the Impedance Network

VSI Input state	Open		Active		Shoot-Through	
Diode Ds	On	Off	On	Off	On	Off
State of Impedance Network	Open-1	Open-2	Active-1	Active-2	Shoot-Through-1	Shoot-Through-2

A switching cycle of the ZSI may consist of any number of states ranging from two to six. However, as will be seen later in the following sections, the Open-1, Active-1, Shoot-Through-1 states are the desired states in practical applications. The three states, Open-2, Active-2, and Shoot-Through-2 are undesirable and are to be avoided by proper sizing of the inductors and capacitors of the impedance network. The impedance network in general can be written as,

$$V_l = L\left(\frac{dI_l}{dt}\right); \qquad I_c = C\left(\frac{dV_c}{dt}\right)$$

$$V_s = V_c + V_l, \qquad I_s = I_c + I_l \tag{2.1}$$

$$V_i = V_c - V_l, \qquad I_i = I_l - I_c \tag{2.2}$$

A. Open -1 state:

Fig.2.3 illustrates the equivalent circuit of the ZSI during Open-1 state.

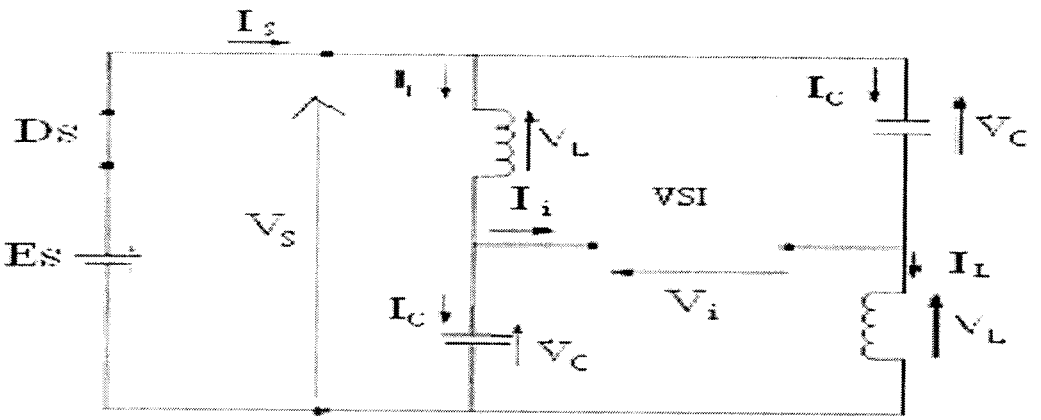


Fig. 2.3 Equivalent circuit of ZSI during Open-1 state

The equations that define the open-1 state are given by,

$$V_s = E_s; \quad I_i = 0; \tag{2.3}$$

The inductor voltage and output voltage in this state are given by,

$$V_l = E_s - V_c; \quad V_i = 2V_c - E_s; \tag{2.4}$$

B. Open-2 state:

In the Open-2 state, the diode remains in the Off states and the VSI in the Open state. Therefore, the state defining equations can be written as,

$I_s=0;\quad I_i=0;$

In order to avoid this state, the necessary condition for the minimum value of inductor current (I_{lomin}) can be seen as,

$I_{lomin}>0.$

C. Active-1 state:

As seen in the equivalent circuit given in the Fig.2.4, the only difference between Open-1 state is the presence of the constant current source Io across the input terminals of the VSI.

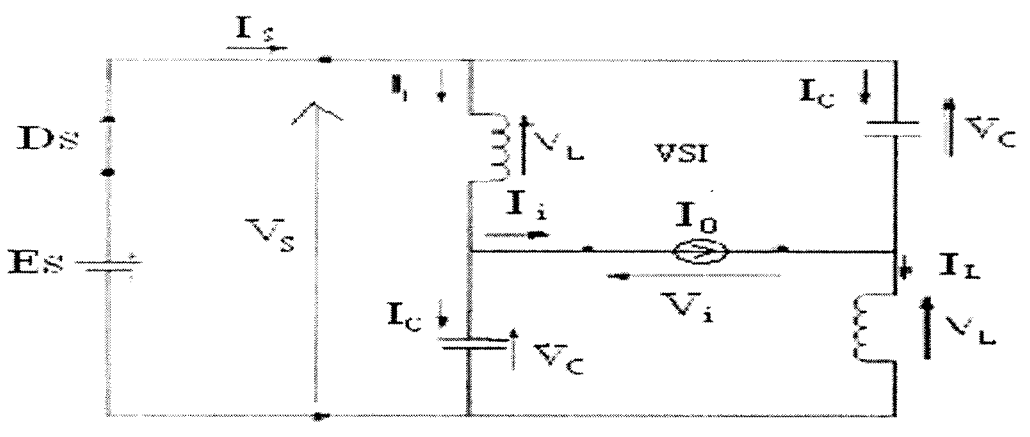


Fig.2.4 Equivalent circuit of ZSI during Active-1 state.

The state defining equations for Active-1 state are,

$V_s= E_s;\quad I_i=I_o$ (2.5)

It can be seen that the current through the diode, Is, will be zero and the diode will turn off when,

$$I_l = -I_c = \frac{I_o}{2} \tag{2.6}$$

This marks the end of Active-1 state and the beginning of Active-2 state.

D. Active-2 state:

The state defining equations for Active-2 state are

$$I_i = I_o; \quad I_s = 0 \tag{2.7}$$

Substituting (1.7) in (1.1) and (1.2), it can be seen that the currents remain constant at $I_l = -I_c = \frac{I_o}{2}$ and the capacitor discharges linearly with time at the rate of $\frac{I_o}{2C}$

In order to avoid Active-2 state in appearing during operation, the necessary condition for minimum inductor current in Active-1 period (I_{lAmin}) is

$$I_{lAmin} > \frac{I_o}{2} \tag{2.8}$$

E. Shoot-Through-1 state:

As seen from Fig. 1.8, the state defining equations for Shoot-Through-1 state are,

$$I_s = 0; \quad V_i = 0 \tag{2.9}$$

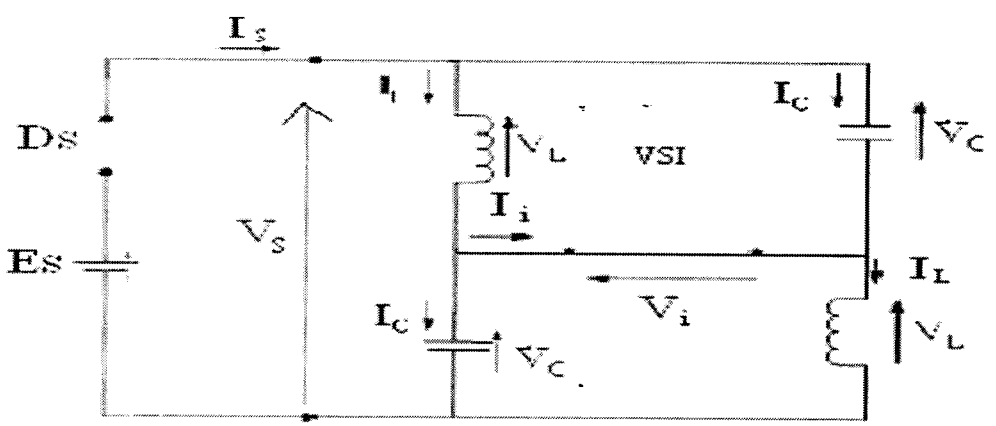


Fig. 2.5 Equivalent circuit of ZSI during Shoot-Through-1 state

The energy stored in the capacitors during Open and Active state is transferred to inductors during Shoot-Through-1 state, thereby allowing the boosting of the voltage applied to the VSI.

F. Shoot-Through-2 state:

The defining equations of Shoot-Through-2 state can be written as,

$$V_s=E_s; \qquad V_i=0 \tag{2.10}$$

In order to prevent appearing of Shoot-Through-2 state during operation the necessary condition for minimum capacitor voltage (V_{cmin}) is

$$V_{cmin} \geq \frac{E_s}{2} \tag{2.11}$$

From the preceding discussion it is clear that the Open-2, Active-2, Shoot-Through-2 states do not contribute to the power conversion process and should be avoided. Thus they are named as 'static states' .Practical inverters are operated only in two or three of the Open-1, Active-1, Shoot-Through-1 states. They are hereby named as 'dynamic states'. Since the three static states appear only when the capacitor voltage and inductor current fluctuate in a wide leading to the violation of conditions given in the Open-2, Active-2, Shoot-Through-2 states, it is necessary to limit the ripples of the related voltage and current by increasing the sizes of the inductors and capacitors appropriately.

2.3 Shoot-Through time period, Boost factor, Modulation Index:

2.3.1 Shoot-Through time period:

Shoot-Through time period is defined as the duration at which the two switches of the same-phase leg are gated on at the same time.

2.3.2 Boost factor:

$$V_i = \frac{T}{T_1 - T_0} V_s \qquad (2.12)$$

Where,

T0 is the Shoot-Through time period in seconds

T1 is the non Shoot-Through time period or Active state of ZSI

T is the Total time period in sec

V_s is the input source voltage

$V_i = B\ V_o$

Where B is the Boost factor resulting from the Shoot-Through zero state.

2.3.3 Modulation Index:

On the other side the output peak phase voltage from the inverter can be expressed as,

$$V_{ac} = \frac{M.V_i}{2} \qquad (2.13)$$

Where

M is the Modulation Index.

V_{ac} is the output line voltage of ZSI.

Using equations (1.12) , (1.13) can be further expressed as ,

$$V_{ac} = \frac{M.B.V_o}{2} \qquad (2.14)$$

$$V_{ac} = \frac{B_b.V_o}{2} \qquad (2.15)$$

Where, B_b is the buck boost factor.

CHAPTER 3

DESIGN OF Z-SOURCE INVERTER

3.1 Assumption:

1. Identical L and C.
2. Dynamic states are alone considered.

3.2 Impedance network for operating with two dynamic states:

Since Open -1 period is not essential for the conversion process and Open -2 and Active-1 state behave in a similar manner, the Open-1 period is considered as part of the Active-1 period. Thus, ZSI operates only in the Active-1 and Shoot-Through-1 state as depicted in Fig.2.1.since the final value of the variable in one state in the initial value of the same variable in the other state , the boundary conditions can be defined as,

$$V_{ciA} = V_{cfS} \; ;$$
$$V_{ciS} = V_{cfA}; \qquad (3.1)$$

$$I_{liA} = I_{lfS} \; ;$$
$$I_{liS} = I_{lfA} \; ; \qquad (3.2)$$

Furthermore, since one switching cycle of VSI has only the Active-1 and Shoot-Through-1 periods,

$$t_A + t_s = T_s; \qquad (3.3)$$

Where T_s is the period of switching cycle of VSI , which is assumed to be known.

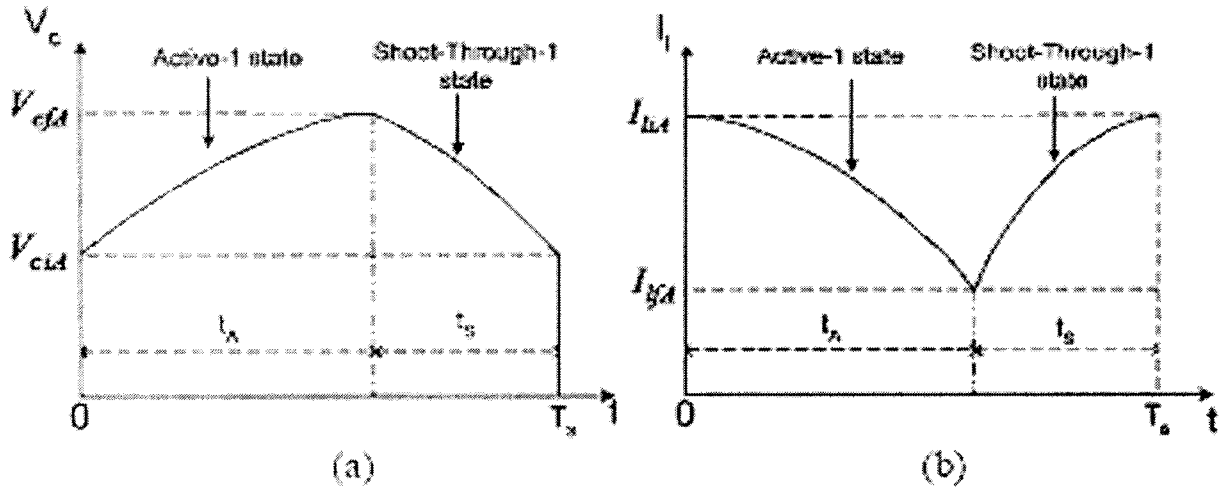


Fig.3.1 Steady state waveforms of (a) Capacitor Voltage
(b) Inductor Current for the operation with two dynamic states.

The duty cycle of the shoot-Through state,

$$d_s = \frac{t_s}{T_s};$$

It is not a simple task to accurately design the impedance network even for the simplest case of operation with two dynamic states as it involves many equations. Hence a less accurate, yet a much simpler method is proposed in the next section for the sizing of the impedance network..

3.3 Approximate design with Linearised waveform:

A ripple in the capacitor voltage in turn appears as a ripple in the dc link voltage applied to the VSI. A large ripple in the dc link voltage degrades the waveform of the ac voltage by giving rise to unexpected harmonics in addition to increasing the voltage rating of VSI. As a consequence, the ripple of the capacitor voltage in practical converters is limited by these concerns and leads to a much smaller ripple than the one allowed. Similarly, the ripple of the inductor current in turn appears as a ripple in the current through the diode and the source. In order to limit the current rating of the diode and the source, the ripple of the inductor current is constrained to a range which is much smaller ripples allowed by the condition .Due to the small ripples allowed, the changes in

the capacitor voltage and the inductor current can be assumed as linear, instead of sinusoidal, for simpler analysis and designing of the ZSI.

Fig.3.2 illustrates the waveform of the capacitor voltage and inductor current under this condition. The average values of V_c and I_l respectively and the peak values of their ripples are given as ΔV_c and ΔI_l respectively.

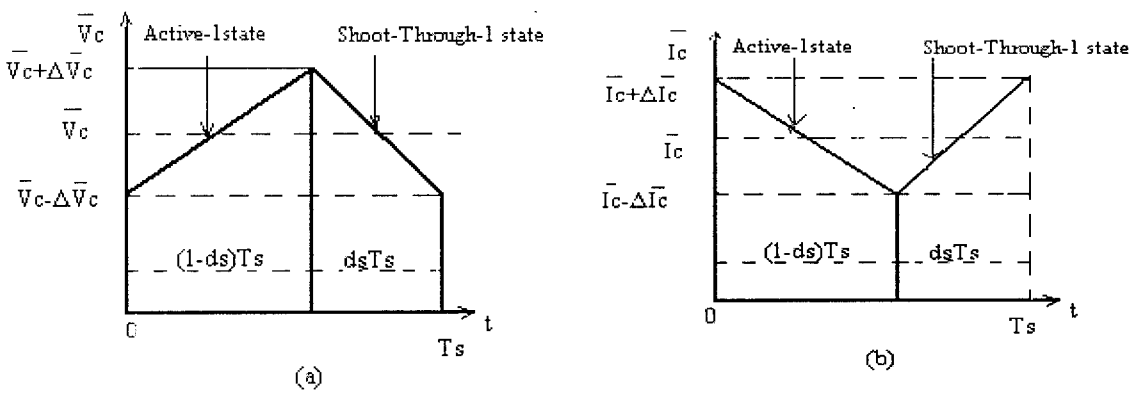


Fig.3.2 Linearised waveforms of (a) Capacitor Voltage (b) Inductor Current for small ripples.

With linear variations of waveform, from (3.2), the peak ripples ΔV_c and ΔI_l can be expressed as,

$$\Delta V_c = \frac{\bar{I}_c \Delta t}{C};$$
$$\Delta I_l = \frac{\bar{V}_l \Delta t}{C}; \qquad (3.4)$$

Considering the Shoot-Through-1 period,

$$C = \frac{I_c d_s T}{2\Delta V_c};$$
$$L = \frac{V_c d_s T}{2\Delta I_c}; \qquad (3.5)$$

Since the average inductor voltage and average capacitor current over a complete switching cycle in steady-state are zero,

$$\frac{\overline{V_c}}{E_s} = \frac{\overline{I_l}}{I_0} = \lambda; \tag{3.6}$$

By expressing the ratio of peak ripples to their average values as k, where k<<1 for linear waveforms,(3.5) and(3.6) can be combined as,

$$C = \frac{I_0 d_s T_s}{2kE_s};$$
$$L = \frac{E_s d_s T_s}{2kI_0}; \tag{3.7}$$

Thus, if the source voltage, load current , switching period and duty ratio of Shoot-Through state are known, C and L for any control strategy can be calculated from(3.7) to result in a desired level of ripples.

Furthermore, for simple –boost control, the average voltage applied to the VSI during active state, as given by,

$$\overline{V}_{iA} = 2\overline{V}_c - E_s = \frac{2V_m}{(1-d_s)}; \tag{3.8}$$

Substituting for $\overline{V}_c$ in (3.6) from (3.8), it can be simplified as,

$$\lambda = \frac{2V_m}{E_s};$$

$$d_s = \frac{(2V_m - E_s)}{(4V_m - E_s)}; \tag{3.9}$$

With the substitution of λ and ds from (3.10) in (3.7) and (3.8) respectively, it can be found that

$$\overline{V}_c = 2V_m;$$
$$I = \frac{2V_m I_0}{Es}; \tag{3.10}$$

$$C = \frac{I_0 T_s(2V_m - E_s)}{2kE_s(4V_m - E_s)}; \qquad (3.11)$$

$$L = \frac{E_s T_s(2V_m - E_s)}{2kI_0(4V_m - E_s)};$$

3.4 Calculation procedure:

The design process based on approximate method is shown below:

Let a 3-phase,50Hz,400V(line-line),25A,Y-connected resistive load be supplied by a ZSI operating at 10kHz under simple- boost control with a constant input dc source voltage of 200V.

For this case, the circuit parameters required for the design procedure can be calculated as,T_s=10^-4 ;E_s=200V;V_m=√2.400/√3=326.6V.From (3.9),it can be found that λ=3.266,ds=0.41 and M=0.59.Using (3.10),it can be determined that $\overline{V}_c$ = 653.2 and then from (3.8),the equivalent dc link voltage can be found as, $\overline{V}_{iA}$ =1106.4V.The input current of VSI due to the load can be determined by considering power balance as , Io=3VmIm/(2 $\overline{V}_{iA}$ (1-ds))=26.53Awhere I_m is the peak phase current of the load . The average inductor can then be found from (3.6) asI_l=86.66A.The capacitor and inductor values are given by (3.7) or (3.11) as C=2.72kμF and L=0.154/kmH where factor k is chosen to limit the ripples of capacitor voltage and inductor current .For the ripples to be 5% of their average values, k=0.05 and then C=54.4μF and L=3.09mH.

CHAPTER 4

SIMULATION OF Z SOURCE INVERTER

4.1 Introduction to MATLAB:

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. Typical uses include

1. Math and computation
2. Algorithm development
3. Data acquisition Modeling, simulation, and prototyping
4. Data analysis, exploration, and visualization
5. Scientific and engineering graphics
6. Application development, including graphical user interface building

SIMULINK is a software package for modeling, simulating, and analyzing dynamic systems. It supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. Systems can also be multirate, i.e., have different parts that are sampled or updated at different rates. As MATLAB and SIMULINK are integrated, we can simulate, analyze, and revise our models in either environment at any point. Thus using SIMULINK, MATLAB models have been created for Z Source Inverter and its triggering circuit and their simulation results have been obtained.

4.2 MATLAB model:

The following models have been created using SIMULINK:

Fig.4.1 shows MATLAB model of ZSI. This model contains three phase programmable voltage source ,rectifier bridge, ZSI circuit, with upper and lower triggering circuit and three phase V-I measurement.

Fig.4.2 shows MATLAB model of the upper triggering circuit. This circuit serves to produce triggering pulses for the switches T1, T3 andT5 in the ZSI.

Similarly Fig 4.3 shows MATLAB model of the lower triggering circuit which serve to produce the triggering pulses for the switches T2,T4 and T6 in the ZSI.

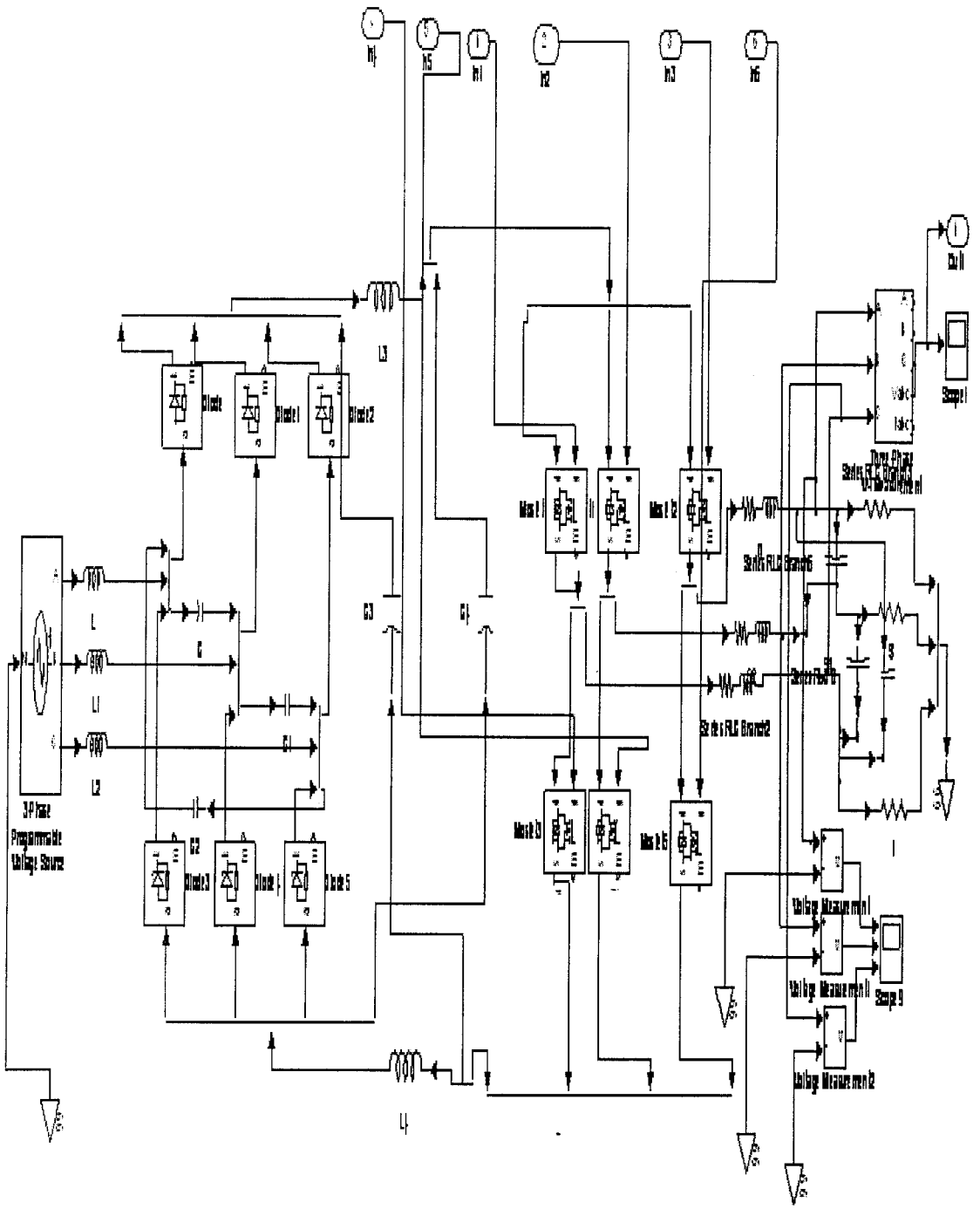


Fig. 4.1 Z-Source Inverter

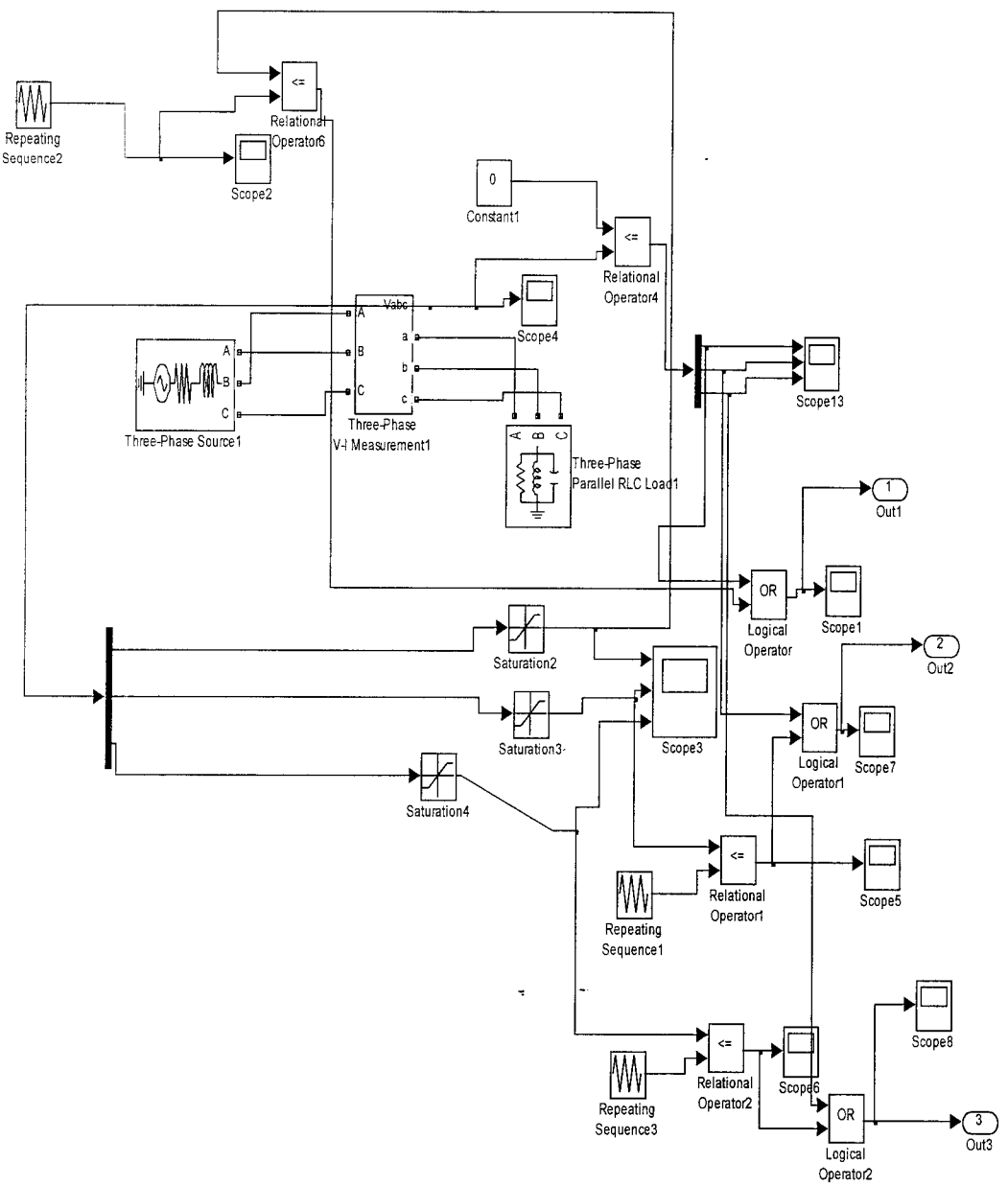


Fig. 4.2 Upper triggering circuit

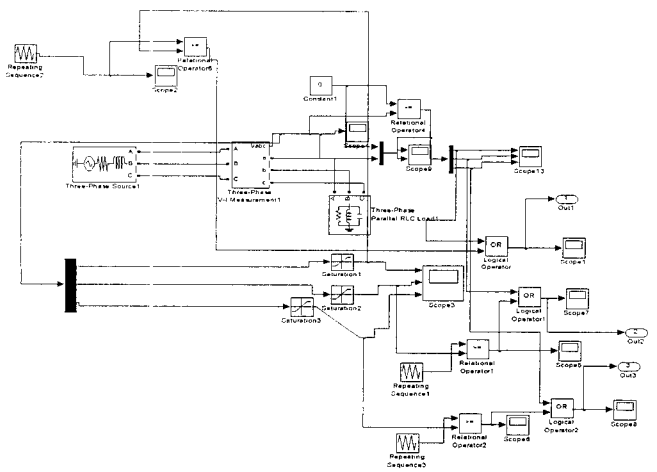


Fig. 4.3 Lower triggering circuit

4.3 Simulation results for various input voltage level:

Figure 4.4 illustrates the gate pulse given to each individual switch.

4.3.1 Triggering pulse:

Fig.4.4 shows the triggering pulses, which are given to the switches of the ZSI. These pulses have been obtained after the simulation of the MATLAB model shown in the Fig.4.1

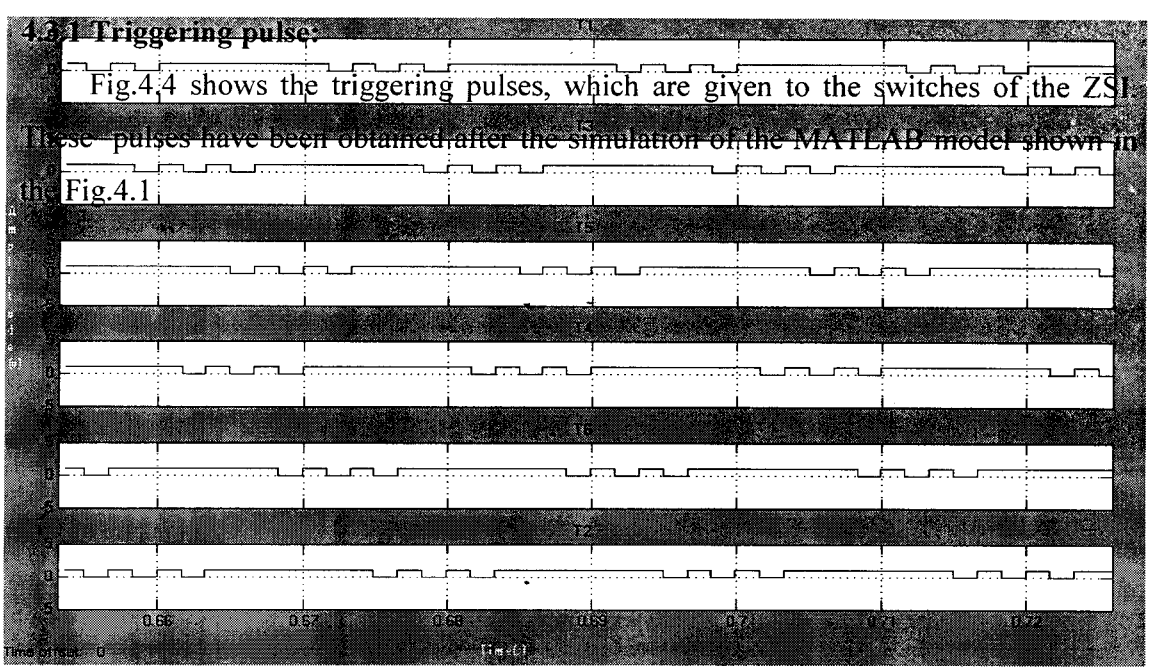


Fig.4.4 Triggering pulses given to Z Source Inverter

4.3.1 Input voltage:

The various input voltage which are given to the rectifier bridge are 50v,100v and 155v.

4.3.2 Output voltage:

For the given input voltages, the various output voltage from the inverter are 140v, 280v and 415v.

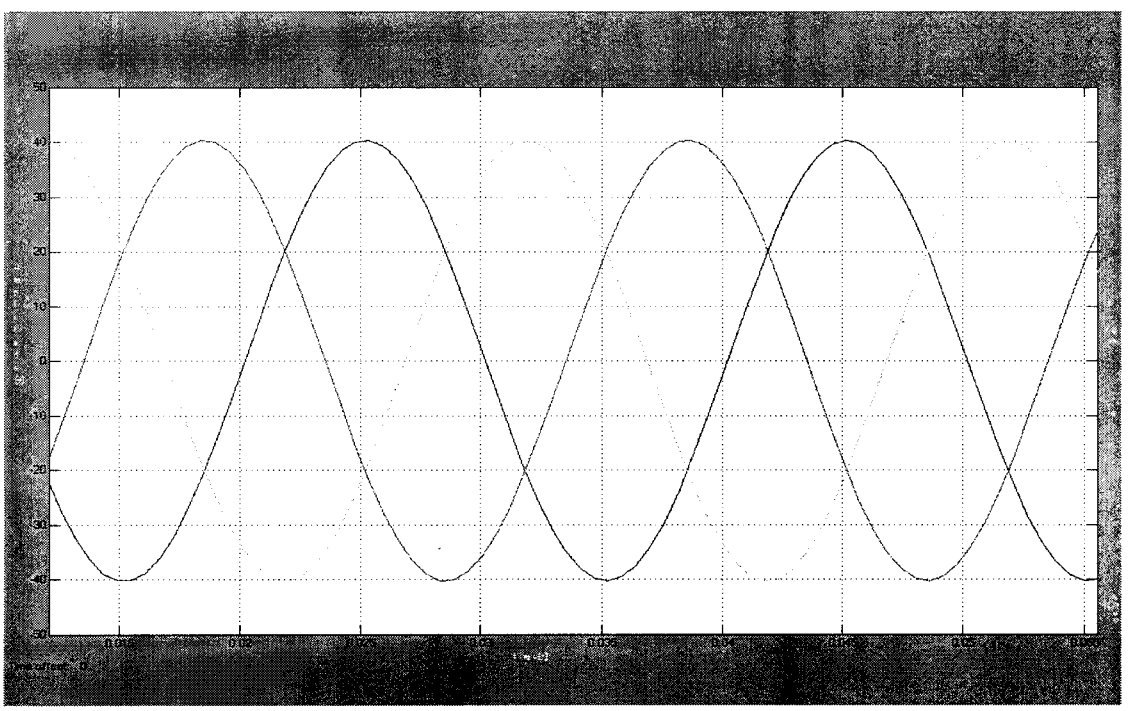


Fig.4.5 Input voltage-50v

Fig.4.5 shows the input voltage of 50v which is given to rectifier bridge. It shows the simulated input voltage which is given as an input to the rectifier bridge. The rectifier bridge converts the ac voltage into dc voltage , which is then applied to ZSI to get the boosted ac output voltage.

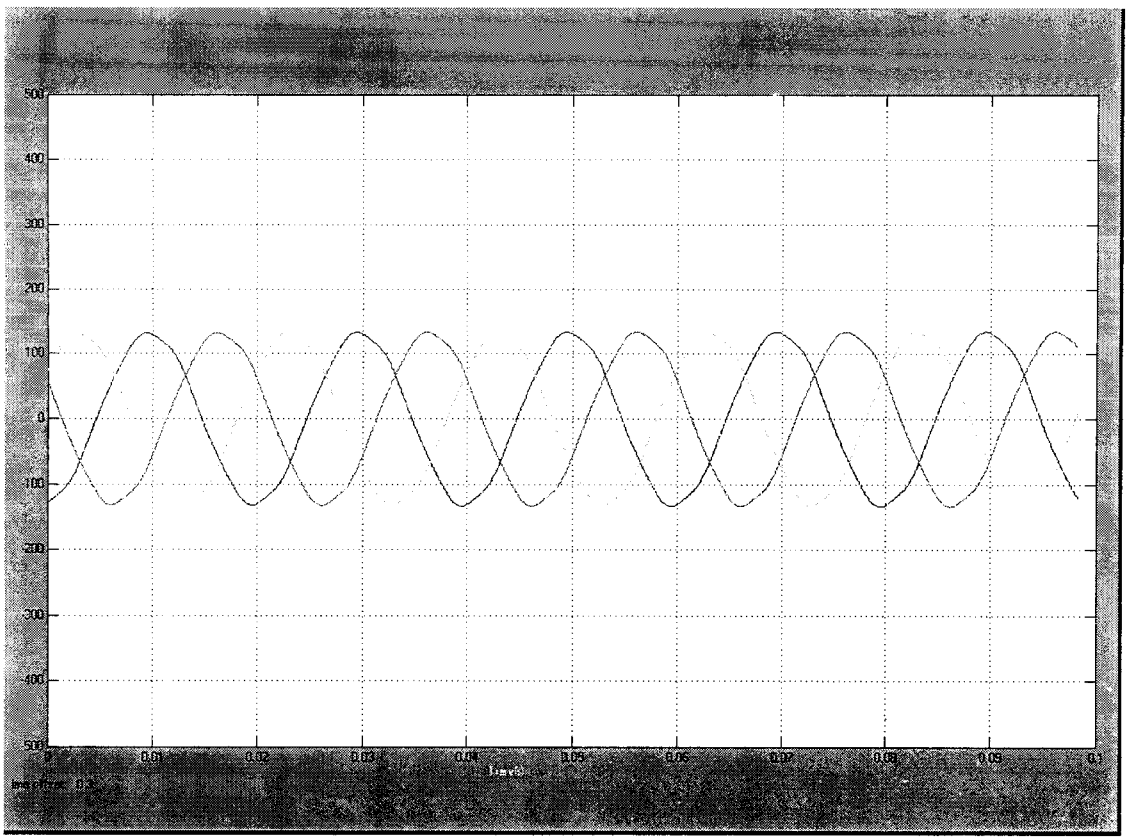


Fig.4.6 Output voltage-140v when input is 50v

Fig.4.6 shows the output voltage of 140v from the inverter circuit when the input is 50v.It represents the simulated output of the MATLAB model (Fig.4.1).The output voltage has been boosted to 2.8 times the input voltage can be inferred from this result.

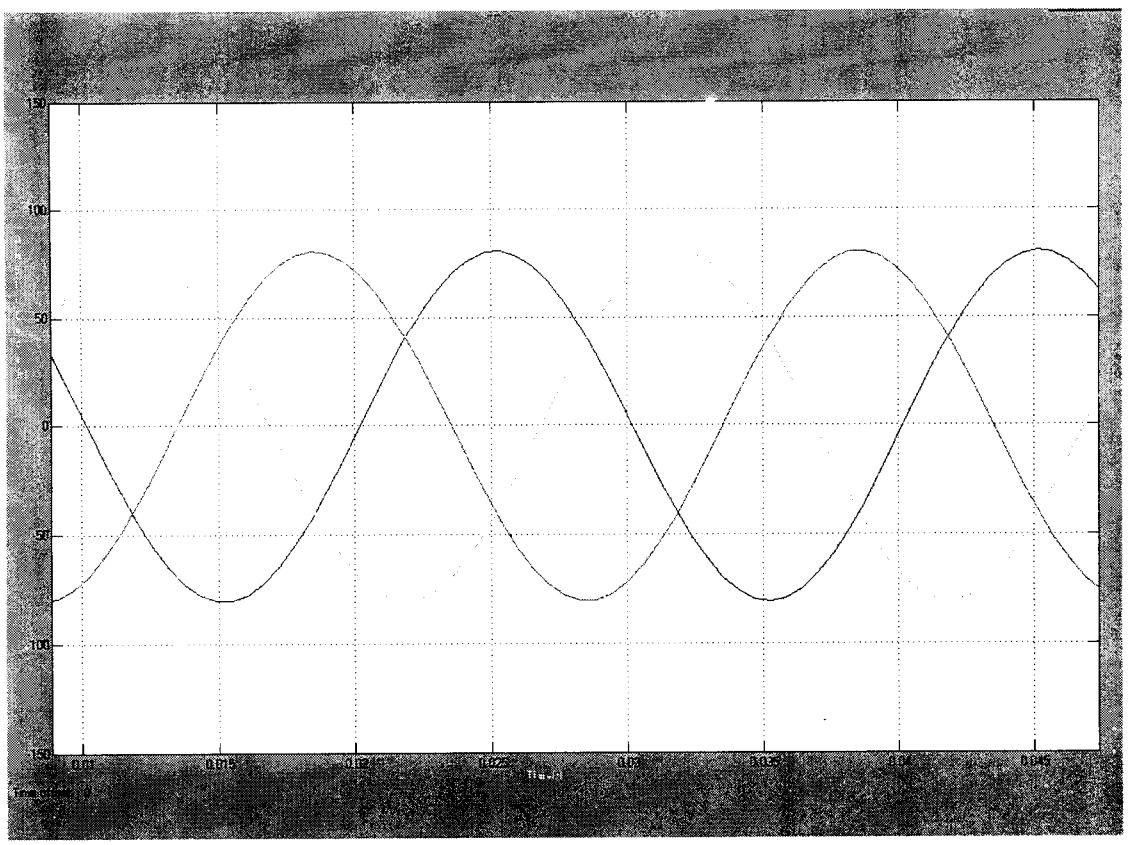


Fig.4.7 Input voltage-100v

Fig.4.7 shows the input voltage of 100v which is given to rectifier bridge. It shows the simulated input voltage which is given as an input to the rectifier bridge. The rectifier bridge converts the ac voltage into dc voltage , which is then applied to ZSI to get the boosted ac output voltage.

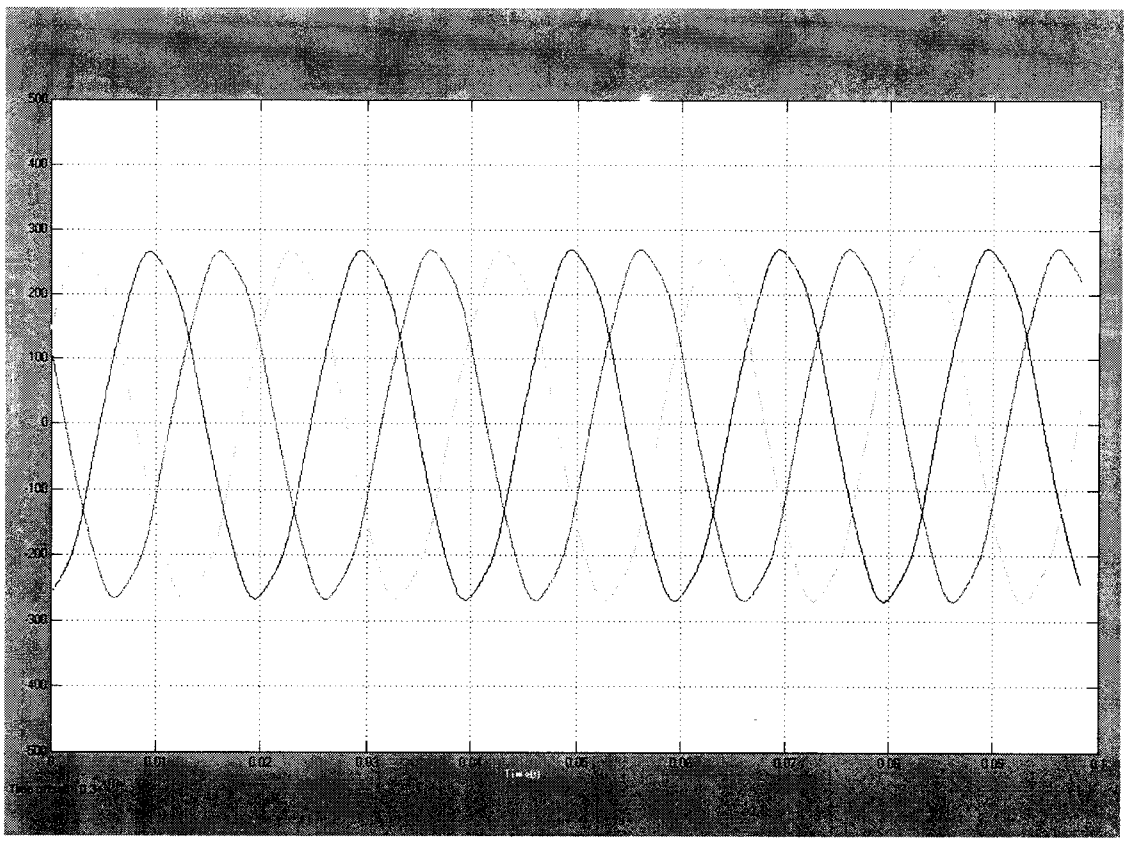


Fig.4.8 Output voltage-280v when input is 100v

Fig.4.8 shows the output voltage of 280v from the inverter circuit when the input is 100v. It represents the simulated output of the MATLAB model (Fig.4.1).The output voltage has been boosted to 2.8 times the input voltage can be inferred from this result.

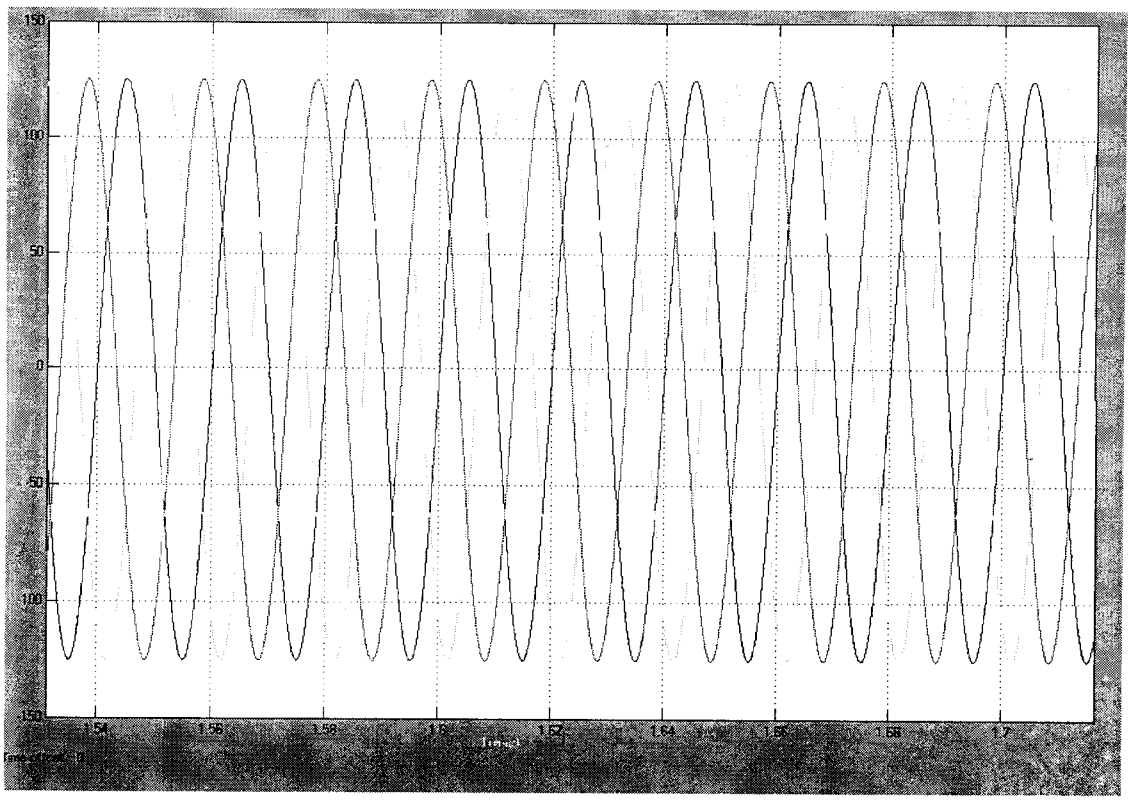


Fig.4.9 Input voltage-155v

Fig.4.9 shows the input voltage of 155v which is given to rectifier bridge. It shows the simulated input voltage which is given as an input to the rectifier bridge. The rectifier bridge converts the ac voltage into dc voltage , which is then applied to ZSI to get the boosted ac output voltage.

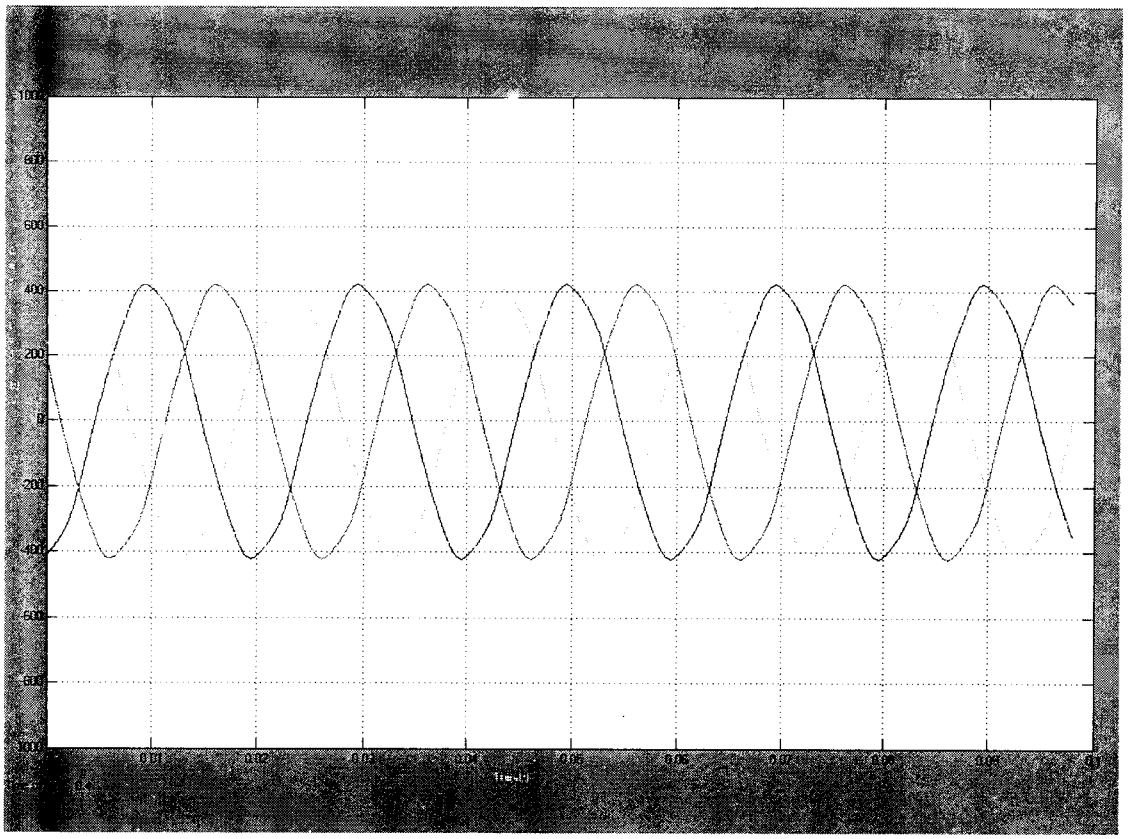


Fig.4.10 Output voltage-415v when input is 155v

Fig.4.10 shows the output voltage of 415v from the inverter circuit when the input is 155v. It represents the simulated output of the MATLAB model (Fig.4.1).The output voltage has been boosted to 2.8 times the input voltage can be inferred from this result.

CHAPTER 5
HARDWARE SIMULATION IN FPGA SYSTEM WITH PWM TECHNIQUE

5.1 Introduction

The Field Programmable Gate Array (FPGA) is a general-purpose device filled with digital logic building blocks. The most primitive FPGA building block is called either a Logic Cell (LC) by Xilinx or a Logic Element (LE). In either case, this building block consists of a look-up table for logical functions and a flip-flop for storage. In addition to the Logic Cell/Logic Element block, FPGAs also contain memory, clock management, input/output (I/O), and multiplication blocks. For the purposes of this study, LC/LE consumption is used in determining system cost. The designer of an FPGA embedded processor system has complete flexibility to select any combination of peripherals and controllers. The designer can invent new, unique peripherals that can be connected directly to the processor's bus. If a designer has a non-standard requirement for a peripheral set, this can be met easily with an FPGA embedded processor system.

5.2 Need for FPGA System with PWM technique

- PWM technique used enables the reduction of harmonics.
- Variable values of duty cycles can be simulated.
- Derived values of duty cycle can be fabricated in the microcontrollers.

5.3 Structure of Field Programmable Gate Array

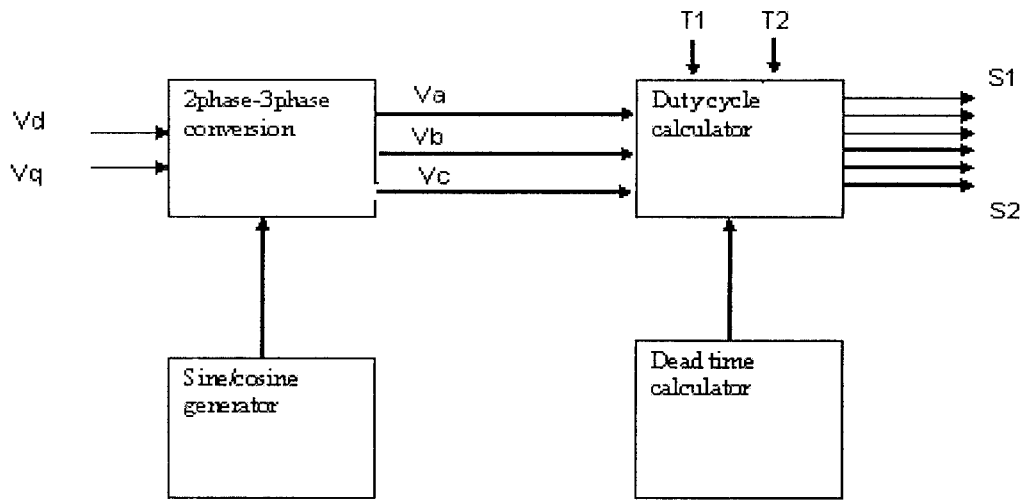


Figure 5.1 Structure of Field Programmable Gate Array

5.4Example of switching time of each switch

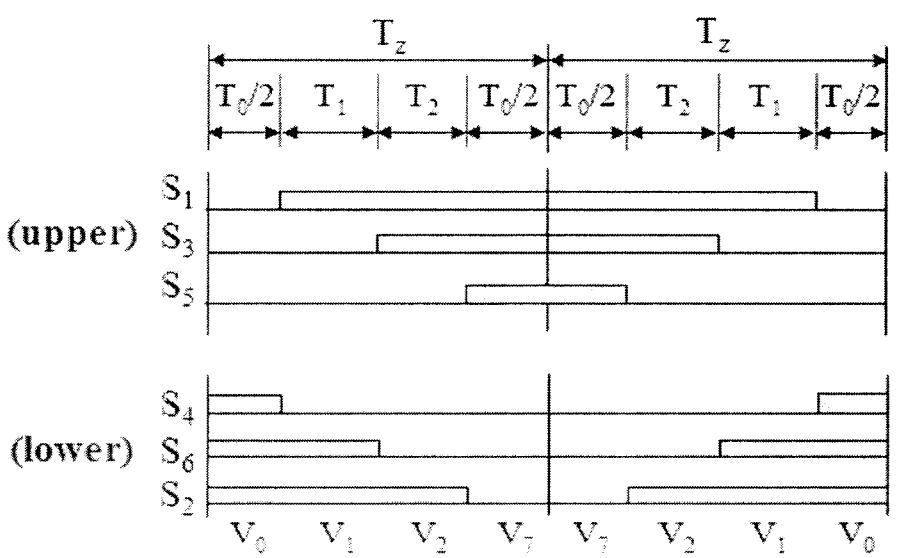


Figure 5.2 samples switching for each switch

5.5 Software Package

The SimCoupler Module is an add-on module to the PSIMsoftware. It provides interface between PSIM and Matlab/Simulink for co-simulation, so that part of a system can be implemented and simulated in PSIM, and the rest in Matlab/Simulink.

5.6 Experimental results of FPGA system with PWM technique

The experimental results of the hardware simulation of FPGA system with PWM technique has been discussed below.

5.4.1 Pulse pattern

In figure 5.3, the pulse pattern for each switch is been created from the FPGA system.

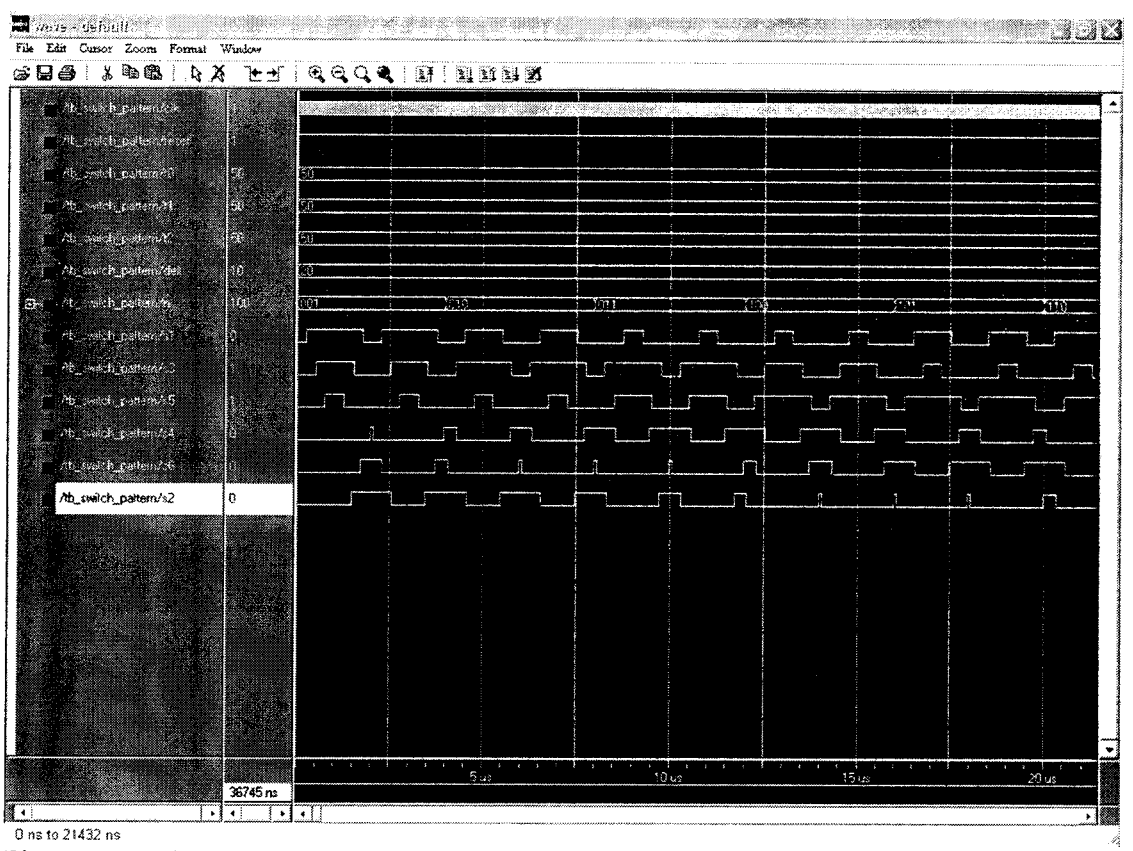


Figure 5.3 pulse pattern for each switch

5.4.2 Two phase to three phase Transformation

The three phase output voltage is shown in the figure 5.4, where the transformation of two phase to three phase is also shown.

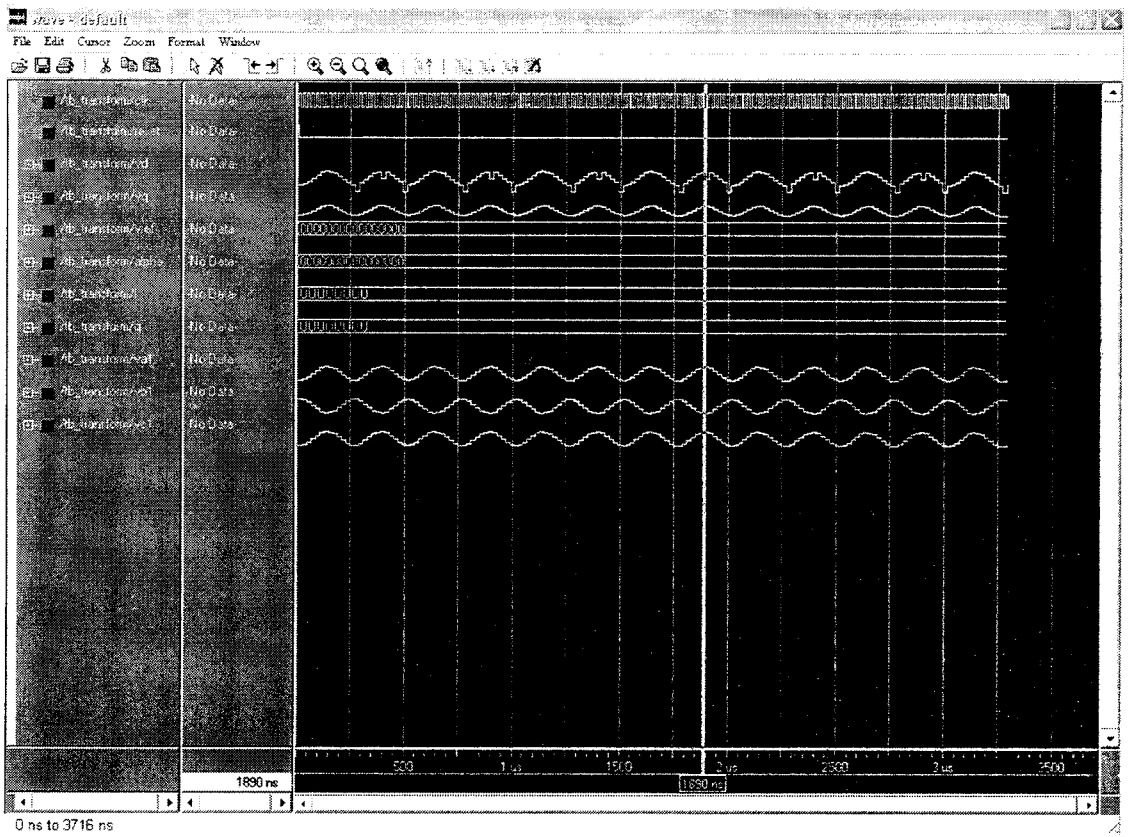


Figure 5.4 Three phase output voltage waveform

The three phase output voltage waveform for 2phase to 3phase transformation by various values of cosine and sine term has been derived and the corresponding output voltage waveform is shown in the above diagram.

CHAPTER 6

HARDWARE DESCRIPTION

6.1 Introduction to hardware setup

The hardware circuit implemented for the impedance source inverter is build up with two inductors and two capacitors of similar values respectively. The capacitors are connected in cross shape across the inductors, which help in the boosting of the voltage in the output. The pulse pattern is derived from the microcontroller, and hence the duty cycle is decided by the PIC microcontroller used in the system.

For switching of the device, high speed power MOSFET. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

The MOSFETs are triggered by the PIC Microcontroller based PWM technique. The duty cycle is studied and the time period is measured and the turn on (T0) and turn off (T1) pulse are given to the switch from the microcontroller.

6.2 Impedance Source

In traditional inverters either a capacitor or an inductor is involved in the dc link. In voltage source inverters a capacitor is used where as in the current source inverters an inductor is used. But in this Impedance source inverter both the capacitor and an inductor is involved so that the rectifier output can be boosted as well as bucked as per the requirement. Here the capacitor and the inductor is connected in a manner so as the bridge looks like X . This bridge boosts the rectifier output so that the output of the inverter bridge is maintained as per the requirement.

6.3 MOSFET driver circuit

The IR2112(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volt.

6.4 MOSFET

The MOSFET used in the hardware circuit is MOSFET IRF240. This device features with very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability. It also features with voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

6.5 Hardware circuit

The design of the hardware circuit with PIC Microcontroller is shown in the figure 6.1.

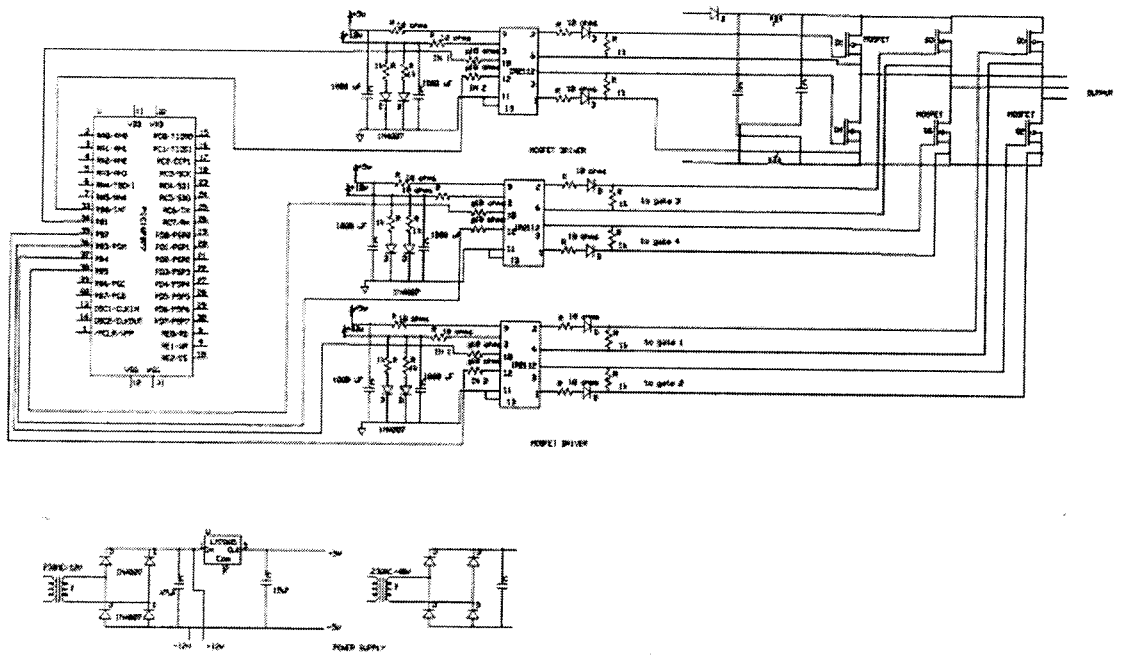


Figure 6.1 Hardware Circuit

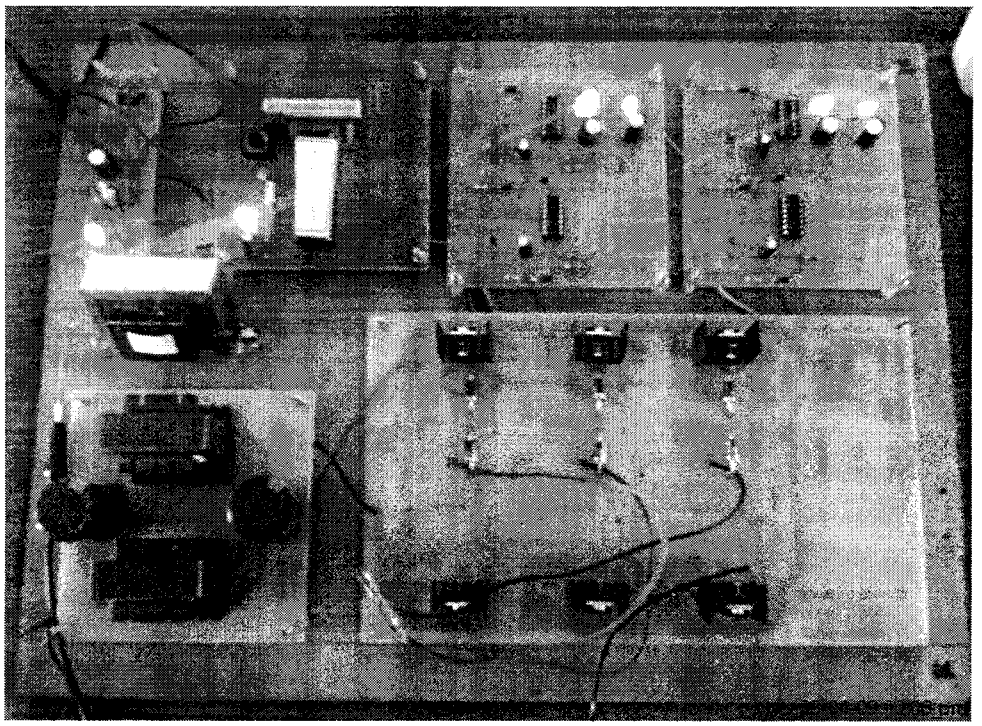


Fig 6.2 Hardware Assembly of Impedance Source Inverter

CHAPTER 7

PIC MICROCONTROLLER

7.1 Introduction

For generating gate pulse to the MOSFET in the converter, either a microprocessor or microcontroller scheme can be effectively used. Of the two schemes, the microcontroller based one is more compact as it requires less hardware and is also more reliable. In the present project, a low cost, high performance PIC 16F87XA has been used for generating the gate pulse to the MOSFET in the dc-dc converter. The details of the hardware required for the pulse generation are described in this chapter.

7.2 Pic Microcontroller

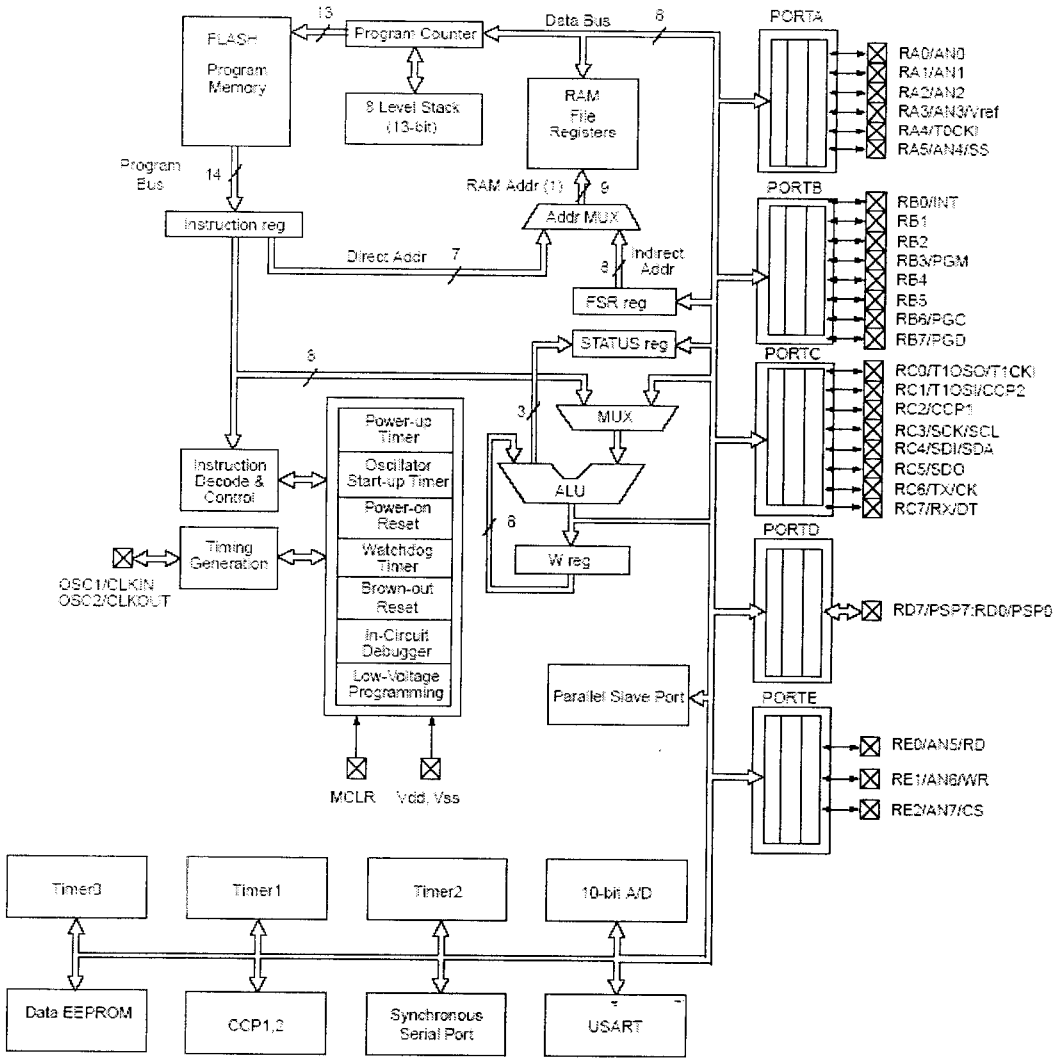
16f877A PIC Microcontroller is used for controlling the width of the pulses from pwm generator, by fixing either the frequency or voltage so that the MOSFETs are turned ON and OFF in the desired sequence.

7.2.1 The need for micro controller based PWM generation

- Micro controller has inbuilt functions such as timer, ADC, PWM, oscillator which reduce the hardware components used.
- PWM technique used enables the reduction of harmonics
- Wide variation in speed since frequency is used as control parameter.
- Digital circuits used employ a faster response.
- Automatic speed control is achieved since no manual parts all involved.
- The Micro controller IC Chip senses the input speed requirement and gives the output in favor of the input.
- No external commutation circuits are required.

7.2.2 Architecture of PIC 16F877A

Device	Program Flash	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes



Note 1: Higher order bits are from the STATUS register.

Figure 7.1 .Architecture of PIC 16F877A Microcontroller

7.2.3 16F877A PIC Microcontroller Pin Diagram

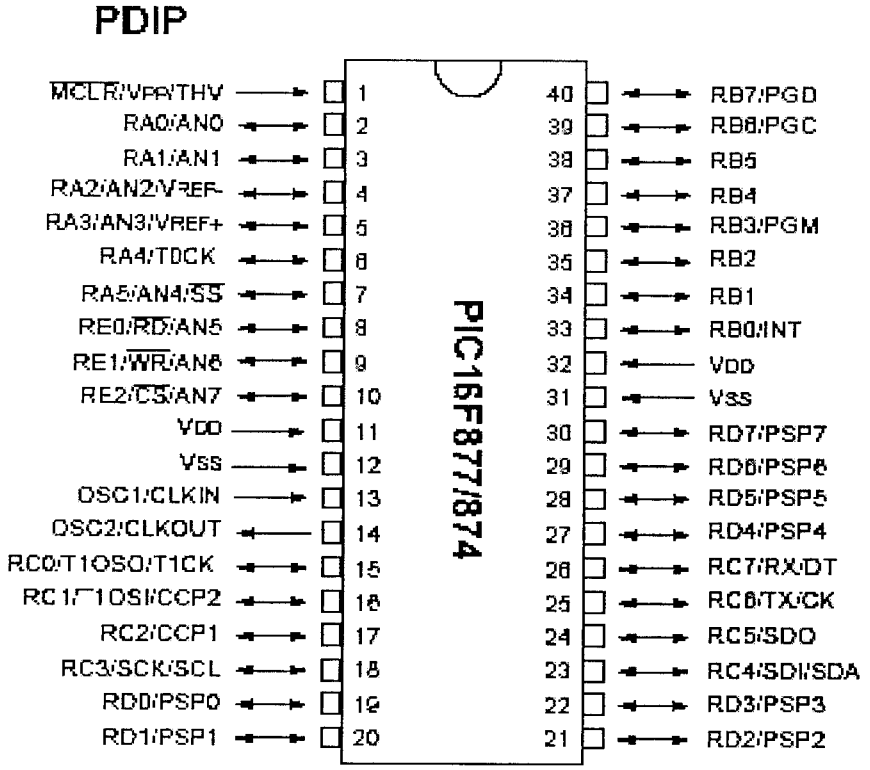


Figure 7.2. Pin diagram of PIC 16F877 Microcontroller

Figure 6.5 shows the pin out diagram of the PIC 16F877 Microcontroller. It is a 40 pin dual inline package (DIP) IC. It has five input / output ports named as Port A, Port B, Port C, Port D and Port E .

CHAPTER 8

CONCLUSION

The project entitled "Design and Implementation of Impedance Source Inverter with FPGA System" has been implemented in three levels such as

- Matlab simulation of Impedance Source Inverter
- VLSI simulation of generating PWM pulses
- Embedded system based hardware implementation.

The Matlab simulation is of 3phase, 440V 50Hz design. The hardware design input voltage is 12V and the derived output voltage is 25V.

8.1 FUTURE SCOPE

This project can be expanded with Field Programmable Gate Array (FPGA) implementation in the hardware in the future.

REFERENCES

1. Fang Zheng Peng, Alan Joseph, JinWang, IEEE,Miaosen Shen, Lihua Chen, Zhiguo Pan, Eduardo Ortiz-Rivera 'Z-Source Inverter for Motor Drives', *IEEE Transactions on Power Electronics* Vol. 20 ,No. 4 ,pp. 857-863, July 2005.

2. F. Z. Peng, M. Shen, and Z. Qian, 'Maximum boost control of the z-source inverter', in *Proc. 39th IEEE Industry Applications Conf.*, Vol. 1, Oct. 2004.

3. F. Z. Peng, 'Z-Source Inverter',*IEEE Trans. Industrial Applications,* Vol. 39, No. 2, pp. 504–510, Mar. /Apr. 2003.

4. Miaosen Shen, Jin Wang, Alan Joseph ,Fang Zheng Peng , Leon M.Tolbert , and Donald J. Adams , 'Constant Boost control of the Z-Source Inverter to Minimize Current Ripple and Voltage Stress', in *IEEE Transaction on Industrial Application* ,Vol. 42, No. 3, May/June 2006.

5. S.Rajakaruna, and Y.R.L.Jayawickrama, 'Designing Impedance Network of Z-Source Inverters', *power engineering conference*,Vol. 2,No. 5,pp. 962-967 , Mar/Apr2005.

6. Alan Joseph, Jin Wang Vol20, July, "Z-source inverter for motor drives", IEEE 2005

7. O. Ogasawara, H. Akagi, and A. Nabel, "A novel PWM scheme of voltage-source inverters based on space vector theory," in Proc. EPE European Conf. Power Electronics and Applications.

8. H. W. v. d. Brocker, H. C. Skudenly, and G. Stanke, "Analysis and realization of a pulse width modulator based on the voltage space vectors, "in Conf. Rec. IEEE-IAS Annu. Meeting, Denver, CO, pp. 244–251, 1986.

APPENDIX

16F877 PIC MICROCONTROLLER CODING

SOFTWARE CODE

```
#include<pic.h>
#define RS RD0
#define RW RD1
#define EN RD2

void enable();
void busycheck();
void lcd_init();
void delaylcd();
void delaylcd1();
void display(unsigned char);
void cursor_loc(unsigned char);
void display_string(unsigned char const*);

void delay1s( );
void delay20( );
void res( );
void res1( );

unsigned char const title[]=" Z - SOURCE INV ";
unsigned char const vol1[]="Volt 1%";
unsigned char const vol2[]="Volt 2%";
unsigned char const vol3[]="Volt 3%";
unsigned char const vol4[]="Volt 4%";
unsigned char const vol5[]="Volt 5%";
```

```
unsigned char const fre1[]="Freq 1%";
unsigned char const fre2[]="Freq 2%";
unsigned char const fre3[]="Freq 3%";
unsigned char const fre4[]="Freq 4%";
unsigned char const fre5[]="Freq 5%";

unsigned int pin=0,s=0,q=0,p=0,k=0,h=0,h1=0;

void main()

{
 ADCON1=0X06;
 TRISB=TRISC=TRISD=0;

 TRISA=0X07;
 PORTA =PORTB =PORTC =PORTD = 0;

 pin=s=q=0;
 delay1s();
 lcd_init();
 delay1s();
 cursor_loc(0x81);
 display_string(title);
 cursor_loc(0xCC);
 display_string("OFF");

while(1)

{

 if(RA0==1)
```

```
{
   h++;
   if(h>=2)
{
   h=0;
}

   switch(h)
{
   case 0:
            delay1s();
            cursor_loc(0xCC);
            display_string("              ");
            cursor_loc(0xCC);
            display_string("OFF");
             h1=0;
            RA3=0;
            break;

  case 1:
            delay1s();
            cursor_loc(0xCC);
            display_string("              ");
            cursor_loc(0xCC);
            display_string("ON");
            h1=1;
            RA3=1;
            break;
}
}
```

```
while(RA1==1)
    {
      k++;
       if(k>=6)
    {
      k=1;
    }

      switch(k)
   {
     case 1:
         res();
         RA4=1;
         cursor_loc(0xc0);
         display_string(vol1);
         break;
     case 2:
         res();
         RA5=1;
         cursor_loc(0xc0);
         display_string(vol2);
         break;
     case 3:
         res();
         RC0=1;
         cursor_loc(0xc0);
         display_string(vol3);
         break;
     case 4:
         res();
         RC1=1;
```

```
    {
        delay1s();
        RC3=RC4=RC5=RC6=RC7=0;
    }
void delay20()
    {
        unsigned int i=0;
        for(i=0;i<=4000;i++);
    }
        void delay1s()
    {
        unsigned int j=0;
        for(j=0;j<=65000;j++);
      }
```