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Design of Power Conditioner for Harmonic Minimization

A Project Report

Submitted by

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BONAFIDE CERTIFICATE

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ABSTRACT

The past several years have seen a rapid increase of power electronics-based loads connected to the distribution system. These types of loads draw non sinusoidal current from the mains, degrading the power quality by causing harmonic distortion. This project proposes a single-phase hybrid active power filter. The proposed topology interconnects a passive high-pass filter in parallel with a shunt active power filter. The specialty of the proposed project is that the control circuit is implemented by extended instantaneous reactive power theorem algorithm which is the best suited time domain control for single phase filters. This theorem simplifies the equations for the current reference estimation, thus leading to a more efficient process of filtering

To generate the compensation current that follows the current reference, the fixed-band hysteresis current control method is adopted. This work describes the design of circuit topology, control system, high-pass filter and compensation current reference estimation. The system is verified by simulation using MATLAB/Simulink simulation package. Simulation results show that the system effectively reduces the total harmonic distortion of the source current from 21.35% to 4.41 %. Furthermore, it is demonstrated that the system can also supply active power to the load. The prototype experimental setup with microcontroller has been developed which shows the improvement of quality of input current.

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LIST OF ABBREVIATIONS

AC - Alternating current

ADC - Analogue-to-digital converter

APF - Active power filter

ASD - Adjustable-speed motor drive

CPU - Central processing unit

DAC - Digital-to-analogue converter

DC - Direct current

DCO - Digitally-controlled oscillator

DSP - Digital signal processor

FFT - Fast Fourier Transform

HPF - High-pass filter

I/O - Input/output

IGBT - Insulated gate bipolar transistor

LPF - Low-pass filter

MOSFET - Power metal oxide-semiconductor field-effect transistor

p-q - Instantaneous reactive-power

PCC - Point of common coupling

PI - Proportional-integral controller

PLL - Phase-lock loop

PQ - Power quality

PWM - Pulse width modulation

rms - Root-mean-square

THD - Total harmonic distortion

VSI - Voltage source inverter

CHAPTER 1
INTRODUCTION

1.1 POWER QUALITY

The power quality (PQ) problems in power distribution systems are not new, but only recently the effects of these problems have gained public awareness. Advances in semiconductor device technology have fuelled a revolution in power electronics over the past decade, and there are indications that this trend will continue. However these power equipments which include adjustable-speed motor drives (ASDs), electronic power supplies, direct current (DC) motor drives, battery chargers, electronic ballasts are responsible for the rise in related PQ problems. These nonlinear loads are constructed by nonlinear devices, in which the current is not proportional to the applied voltage. In the case of a sinusoidal voltage when applied to a simple nonlinear resistor in which the voltage and current vary non-linearly, the voltage is perfectly sinusoidal, the resulting current is distorted.

Nonlinear loads appear to be prime sources of harmonic distortion in a power distribution system. Harmonic currents produced by nonlinear loads are injected back into power distribution systems through the point of common coupling (PCC). These harmonic currents can interact adversely with a wide range of power system equipment, most notably capacitors, transformers, and motors, causing additional losses, overheating and overloading.

There are set of conventional solutions to the harmonic distortion problems which have existed for a long time. The passive filtering is the simplest conventional solution to mitigate the harmonic distortion. Although simple, these conventional solutions that use passive elements do not always respond correctly to the dynamics of the power distribution systems. Some even tuned to bypass specific harmonic frequencies. However, the use of passive elements at high power level makes the filter heavy and bulky. Moreover, the passive filters are known to cause resonance, thus affecting the stability of the power distribution systems.

Remarkable progress in power electronics had spurred interest in active power filter (APF) for harmonic distortion mitigation. The basic principle of APF is to utilize power electronics technologies to produce currents components that cancel the harmonic currents from the nonlinear loads. Previously, majority of controllers developed for APF are based on analogue circuits. As a result, the APF is inherently subjected to signal drift. Digital controller using digital signal processor (DSP) or microprocessor is preferable, primarily due to its flexibility and immunity to noise signals. However it is known that using digital methods, the high order harmonics are not filtered effectively. This is due to the hardware limitation of sampling rate in real-time application. Moreover, the utilization of fast switching transistors (i.e. IGBT or MOSFET) in APF application causes switching frequency noise to appear in the compensated source current. This switching frequency noise requires additional filtering to prevent interference with other sensitive equipments.

The idea of Hybrid Power Filter has been proposed by several researchers. In this scheme, a low cost passive high-pass filter (HPF) is used in addition to the conventional APF is implemented. The harmonics filtering task is divided between the two filters. The APF cancels the lower order harmonics, while the HPF filters the higher order harmonics. The main objective of Hybrid Power Filter therefore is to improve the filtering performance of high-order harmonics while providing a cost-effective low order harmonics mitigation.

1.2 Objective of Project

The objectives of the research are

(1) to propose a hybrid Active Power Filter topology.

(2) to design a simple current reference estimation method for the proposed topology.

(3) to fabricate a hardware system as per the design.

To achieve the first objective, this research proposes a Hybrid Power Filter topology for a single-phase system, connected to a DC source which is preferable. The topology is well suited because it effectively filters harmonic currents of low and high frequencies to obtain sinusoidal source current.

For the second objective, this research proposes the application of the extension instantaneous reactive-power (p-q) theorem to estimate the compensation current reference. Although the estimation of current reference based on extension p-q theorem is not new, this approach has proved to be one of the most efficient time domain approaches to a single-phase Hybrid Power Filter system involving passive HPF and a shunt APF. Using the extension p-q theorem, the resulting equations for the current reference is simpler compared with the conventional p-q theorem.

A prototype will be developed using a PIC microcontroller and an H-Bridge mosfet inverter acting as the shunt filter. Injection of compensation current is done through a coupling transformer into the supply–load system and the waveforms obtained on a CRO.

1.3 Outline of the report

The report consists of an introductory chapter which briefs about power system harmonics, its sources and the conventional and advanced methods of mitigation. The other chapters are as follows.

Chapter 2 gives a detailed study about fundamentals of power harmonics, its impacts on power system. Harmonic mitigation methods with various topologies are discussed. The various control techniques and reference signal estimation is also explained.

Chapter 3 presents the single phase hybrid filter topology proposed. The proposed overall system and control technique is discussed.

Chapter 4 is dedicated to the control algorithm and the estimation of reference current using the p-q theorem.

Chapter 5 shows the complete details of the simulation model developed. The details of individual blocks and the design values of the power elements are given.

In Chapter 6, the results with and without filter shows the improvement in power quality conforming to the IEEE standards, by the filter designed in the matlab simulink.

Chapter 7 explains the hardware implementation using a PIC microcontroller. Details of individual components used and their images are included. The image results obtained before and after compensation are shown. nd then the report is concluded discussing the future scope of the project using advanced techniques and the applications are also discussed.

CHAPTER 2
POWER SYSTEM HARMONICS AND FILTERS

2.1 Introduction

This chapter reviews the development of active power filter (APF) technologies. The discussion also includes a brief overview of harmonic distortion problems and their impacts on electric power quality (PQ). The conventional harmonic mitigation approaches using passive filters are presented first, followed by the improved mitigation methods using APF techniques. . In addition, different types of reference signal estimation techniques are reviewed. Finally, an Overview on the APF control strategies is also provided.

2.2 Power Quality Problems

Power systems are designed to operate at frequencies of 50 or 60 Hz. However, certain types of loads produce currents and voltages with frequencies that are integer multiples of the 50 or 60 Hz fundamental frequency. These frequencies components are a form of electrical pollution known as harmonic distortion. Harmonic distortion has sparked research that has led to the present-day understanding of PQ problems. In this section, the concept of Harmonic distortion is introduced and its impacts on electric PQ are discussed.

2.2.1 Fundamental of Harmonic Distortion

Due to the proliferation of nonlinear loads from power electronics converters, one of the electric PQ issues that received much attention is the harmonic distortion. These nonlinear loads control the flow of power by drawing currents only during certain intervals of the 50/60 Hz period. Thus, the current drawn by the nonlinear load is nonsinusoidal and appear chopped or flattened.

Figure 2.1 illustrates that any periodic, distorted waveform can be expressed as a sum of pure sinusoids. The sum of sinusoids is referred to as a *Fourier series*, named after the great mathematician who discovered the concept. The Fourier analysis permits a periodic distorted waveform to be decomposed into an infinite series containing DC component, fundamental

component (50/60 Hz for power systems) and its integer multiples called the harmonic components. The harmonic number (h) usually specifies a harmonic component, which is the ratio of its frequency to the fundamental frequency.

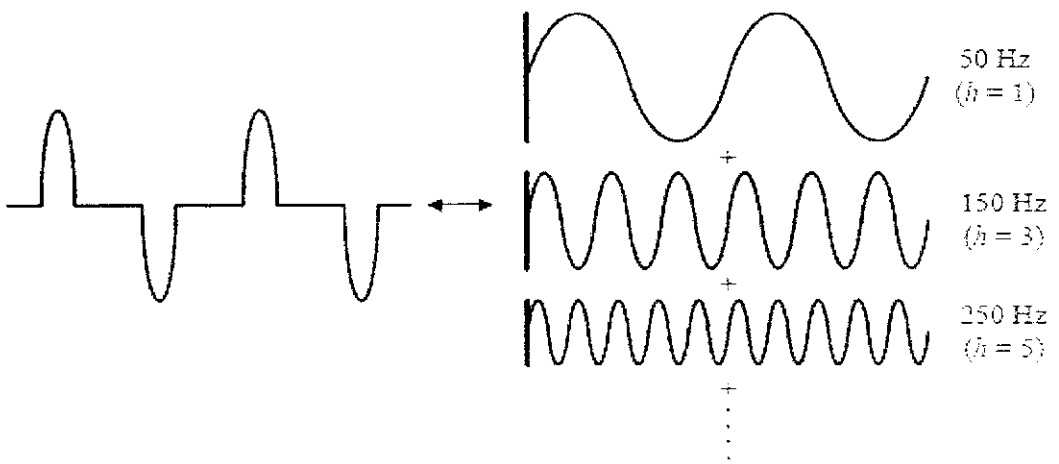


Figure 2.1 Fourier series representation of a distorted waveform

The total harmonic distortion (THD) is the most common measurement indices of harmonic distortion. THD applies to both current and voltage and is defined as the root-mean-square (rms) value of harmonics divided by the rms value of the fundamental, and then multiplied by 100% as shown in the following equation:

$$THD = \frac{\sqrt{\sum_{h=2}^{h_{max}} M_h^2}}{M_1} \times 100\%$$

Where M_h is the rms value of harmonic component h of the quantity M.

THD of current varies from a few percent to more than 100%. THD of voltage is usually less than 5%. Voltage THDs below 5% are widely considered to be acceptable, while values

above 10% are definitely unacceptable and will cause problems for sensitive equipment and loads.

2.2.2 Harmonic Distortion Impacts on Electric Power Quality

For nearly all analyses, it is sufficient to treat nonlinear loads simply as harmonic currents source. As Figure 2.2 shows, voltage distortion is the result of distorted currents passing through the linear, series impedance of power distribution system. Although the source bus is a pure sinusoid, there is a nonlinear load that draws a distorted current. The harmonic currents passing through the impedance of the system cause a voltage drop for each harmonic. This results in harmonic voltages appearing at the PCC. The amount of voltage distortion depends on the source impedance and the current. Harmonics have a number of undesirable effects on electric PQ. These falls into two basic categories: short-term and long-term. Short-term effects are usually the most noticeable and are related to excessive voltage distortion. On the other hand, long-term effects often go undetected and are usually related to increased resistive losses or voltage stresses. In addition, the harmonic currents produced by nonlinear loads can interact adversely with a wide range of power system equipment, most notably capacitors, transformers, and motors, causing additional losses, overheating, and overloading. These harmonic currents can also cause interferences with telecommunication lines and errors in metering devices.

Because of the adverse effects that harmonics have on electric PQ, certain Standards have been developed to define a reasonable framework for harmonic control. The objective of such Standard is to propose steady-state harmonic limits that are acceptable by both electric utilities and their customers.

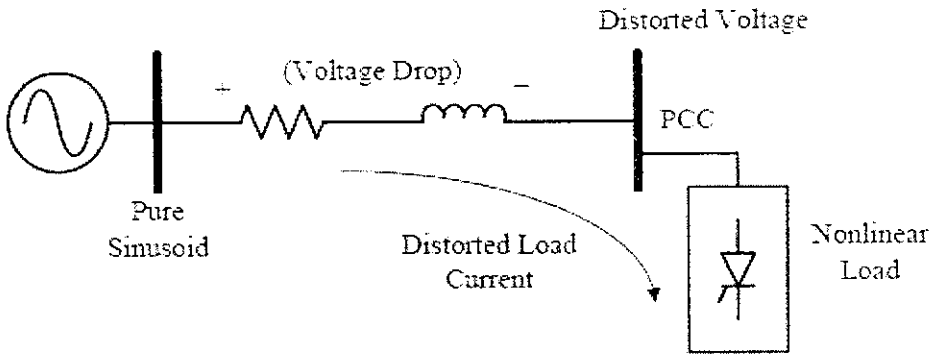


Figure 2.2 Harmonic currents flowing through the system impedance result in harmonic voltages at the PCC

2.3 Harmonic Mitigation Approaches

Harmonic distortion in power distribution systems can be suppressed through three basic approaches namely:

(1) Passive filter.

(2) Active power filter.

(3) Hybrid power filter.

This section discusses general properties of various approaches for harmonic distortion mitigation. The advantages, disadvantages, and limitations of these approaches are also compiled in this section.

2.3.1 Passive Filtering of Harmonic

Conventional solutions to the harmonic distortion problems have existed for a long time. The passive filtering is the simplest conventional solution to mitigate the harmonic distortion. Passive filters are inductance, capacitance, and resistance elements configured and tuned to control harmonics. Figure 2.3 shows common types of passive filters and their configurations.

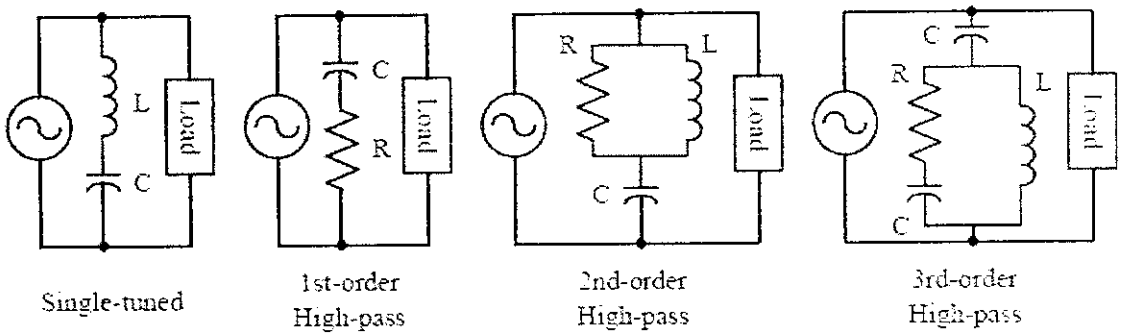


Figure 2.3 Common types of passive filters and their configurations

The single-tuned "notch" filter is the most common and economical type of passive filter. The notch filter is connected in shunt with the power distribution system and is series-tuned to present low impedance to a particular harmonic current. Thus, harmonic currents are diverted from their normal flow path through the filter.

Another popular type of passive filter is the high-pass filter (HPF). A HPF will allow a large percentage of all harmonics above its corner frequency to pass through. HPF typically takes on one of the three forms, as shown in Figure 2.3. The first-order, which is characterized by large power losses at fundamental frequency, is rarely used. The second-order HPF is the simplest to apply while providing good filtering action and reduced fundamental frequency losses. The filtering performance of the third-order HPF is superior to that of the second-order HPF. However, it is found that the third-order HPF is not commonly used for low voltage or medium-voltage applications since the economic, complexity, and reliability factors do not justify them.

Although simple and least expensive, the passive filter inherits several shortcomings. The filter components are very bulky because the harmonics that need to be suppressed are usually of the low order. Furthermore the compensation characteristics of these filters are influenced by the source impedance. As such, the filter design is heavily dependent on the power system in which it is connected to. The passive filter is also known to cause resonance, thus affecting the stability of the power distribution systems. Frequency variation of the power distribution system and tolerances in components values affect the filtering characteristics. The size of the components become impractical if the frequency variation is large. As the regulatory requirements become

more stringent, the passive filters might not be able to meet future revisions of a particular Standard. This may required a retrofit of new filters.

2.3.2 Active Filtering of Harmonic

Remarkable progress in power electronics had spurred interest in APF for harmonic distortion mitigation. The basic principle of APF is to utilize power electronics technologies to produce specific currents components that cancel the harmonic currents components caused by the nonlinear load. Figure 2.4 shows the components of a typical APF system and their connections. The information regarding the harmonic currents and other system variables are passed to the compensation current/voltage reference signal estimator. The compensation reference signal from the estimator drives the overall system controller. This in turn provides the control for the gating signal generator. The output of the gating signal generator controls the power circuit via a suitable interface. Finally, the power circuit in the generalized block diagram can be connected in parallel, series or parallel/series configurations depending on the interfacing inductor/transformer used.

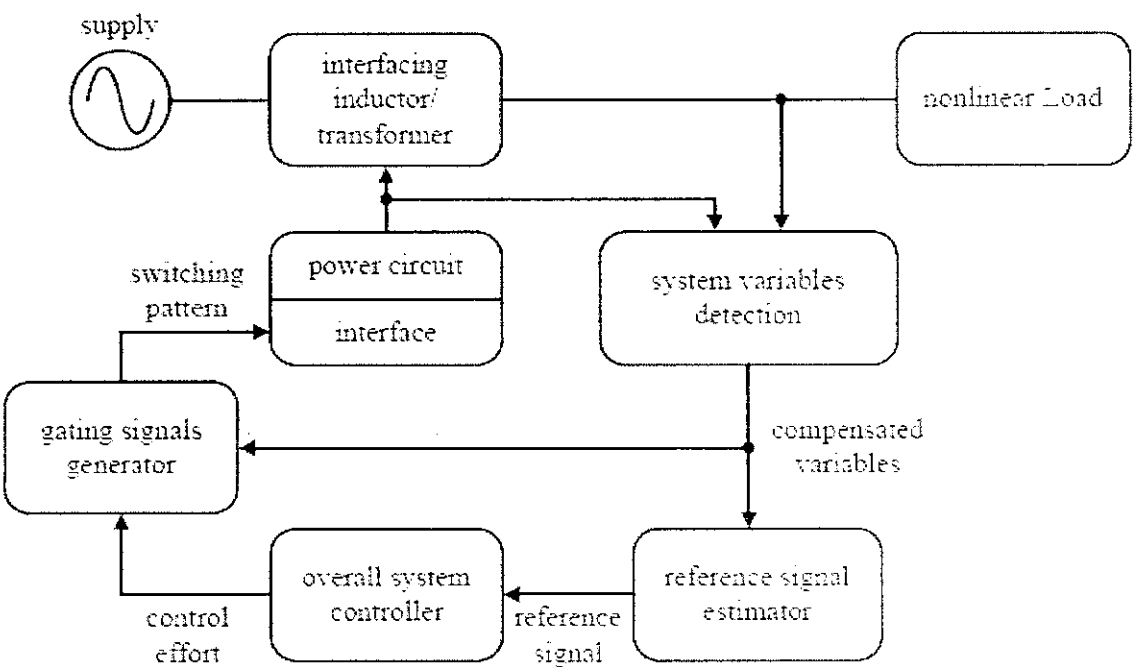


Figure 2.4 Generalized block diagram for APF

APFs have a number of advantages over the passive filters. First of all, they can suppress not only the supply current harmonics, but also the reactive currents. Moreover, unlike passive filters, they do not cause harmful resonances with the power distribution systems. Consequently, the APFs performances are independent of the power distribution system properties.

On the other hand, APFs have some drawbacks. Active filtering is a relatively new technology, practically less than four decades old. There is still a need for further research and development to make this technology well established. An unfavorable but inseparable feature of APF is the necessity of fast switching of high currents in the power circuit of the APF. This results in a high frequency noise that may cause an electromagnetic interference (EMI) in the power distribution systems.

2.3.2.1 Shunt Active Power Filter

This is most important configuration and widely used in active filtering applications. A shunt APF consists of a controllable voltage or current source. The voltage source inverter (VSI) based shunt APF is by far the most common type used today, due to its well known topology and straight forward installation procedure.

Figure 2.6 shows the principle configuration of a VSI based shunt APF. It consists of a DC-bus capacitor (C_f), power electronic switches and an interfacing inductors (L_f). Shunt APF acts as a current source, compensating the harmonic currents due to nonlinear loads. The operation of shunt APF is based on injection of compensation current which is equivalent to the distorted current, thus eliminating the original distorted current. This is achieved by "shaping" the compensation current waveform (i_f), using the VSI switches. The shape of compensation current is obtained by measuring the load current (i_L) and subtracting it from a sinusoidal reference. The aim of shunt APF is to obtain a sinusoidal source current (i_s) using the relationship: $i_s = i_L - i_f$.

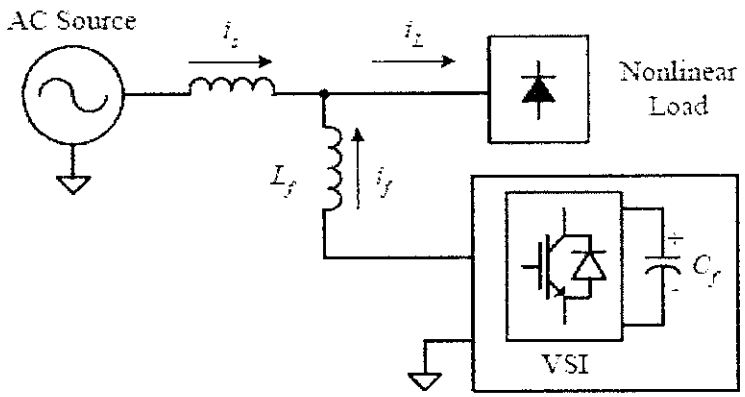


Figure 2.5 Principle configuration of a VSI based shunt APF

Figure 2.6 shows the ideal source current when the shunt APF performs harmonic filtering of a diode rectifier. The injected shunt APF current completely cancels the current harmonics from the nonlinear load, resulting in a harmonic free source current. From the nonlinear load current point of view, the shunt APF can be regarded as a varying shunt impedance. The impedance is zero, or at least small, for the harmonic frequencies and infinite in terms of the fundamental frequency. As a result, reduction in the voltage distortion occurs because the harmonic currents flowing through the source impedance are reduced. Shunt APFs have the advantage of carrying only the compensation current plus a small amount of active fundamental current supplied to compensate for system losses. It can also contribute to reactive power compensation. Moreover, it is also possible to connect several shunt APFs in parallel to cater for higher currents, which makes this type of circuit suitable for a wide range of power ratings.

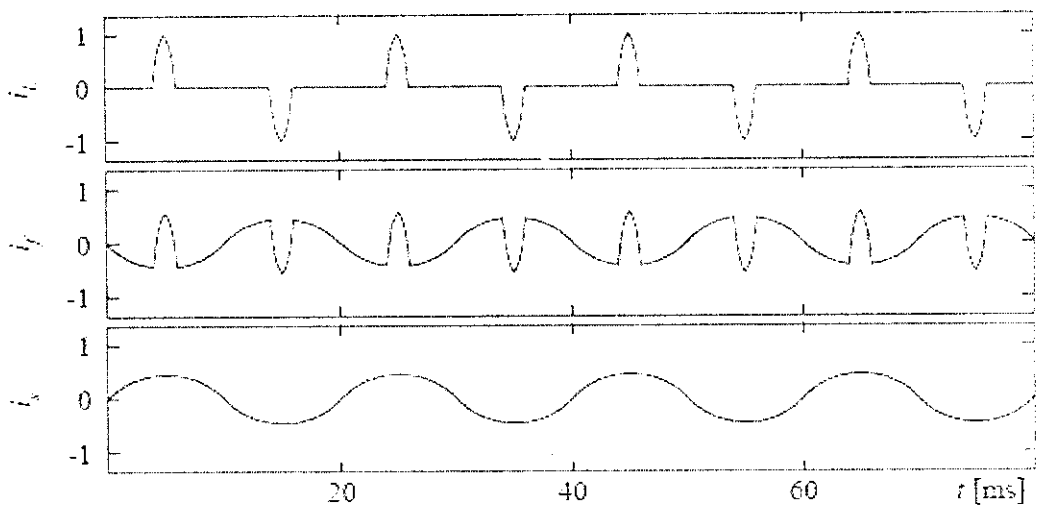


Figure 2.6 Shunt APF harmonic filtering operation principle

2.3.2.2 Series Active Power Filter

The series APF is shown in Figure 2.7. It is connected in series with the distribution line through a matching transformer. VSI is used as the controlled source, thus the principle configuration of series APF is similar to shunt APF, except that the interfacing inductor of shunt APF is replaced with the interfacing transformer.

The operation principle of series APF is based on isolation of the harmonics in between the nonlinear load and the source. This is obtained by the injection of harmonic voltages (v_f) across the interfacing transformer. The injected harmonic voltages are added/subtracted, to/from the source voltage to maintain a pure sinusoidal voltage waveform across the nonlinear load. The series APF can be thought of as a harmonic isolator as shown in Figure 2.8. It is controlled in such a way that it presents zero impedance for the fundamental component, but appears as a resistor with high impedance for harmonic frequencies components. That is, no current harmonics can flow from nonlinear load to source, and vice versa.

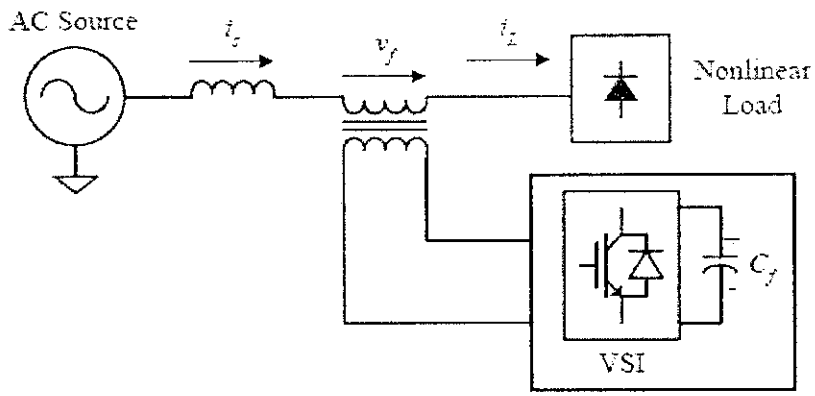


Figure 2.7 Principle configuration of a VSI based series APF

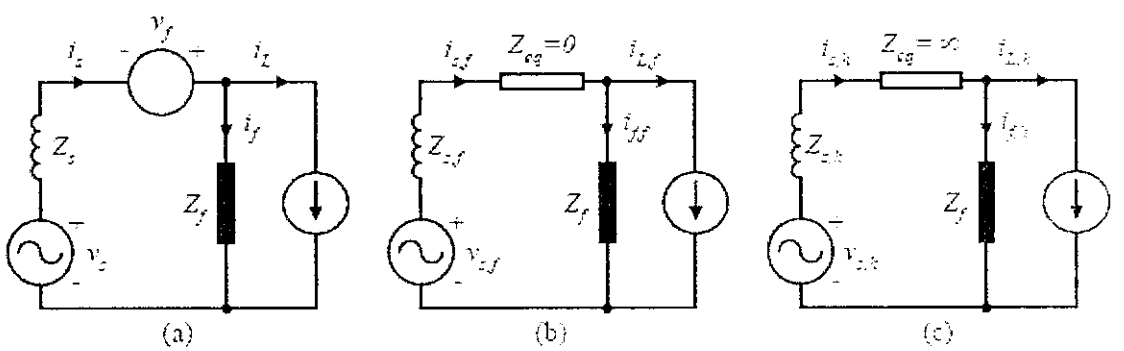


Figure 2.8 Operation principle of series APF: (a) single-phase equivalent of series APF, (b) fundamental equivalent circuit, and (c) harmonic equivalent circuit

Series APFs are less common than their rival, i.e. the shunt APF. This is because they have to handle high load currents. The resulting high capacity of load currents will increases their current rating considerably compared with shunt APF, especially in the secondary side of the interfacing transformer. This will increase the I^2R losses. However, the main advantage of series APFs over shunt one is that they are ideal for voltage harmonics elimination. It provides the load with a pure sinusoidal waveform, which is important for voltage sensitive devices (such as power system protection devices). With this feature, series APF is suitable for improving the quality of the distribution source voltage.

2.3.2.3 Hybrid Power Filter

Previously, majority of the controllers developed for APF are based on analogue circuits. As a result, the APF performance is inherently subjected to signal drift. Digital controllers using DSPs or microcontrollers are preferable, primarily due to its flexibility and immunity to noise. However it is known that using digital methods, the high-order harmonics are not filtered effectively. This is due to the hardware limitation of sampling rate in real-time application. Moreover, the utilization of fast switching transistors (i.e. IGBT or MOSFET) in APF application causes switching frequency noise to appear in the compensated source current. This switching frequency noise requires additional filtering to prevent interference with other sensitive equipment. Technical limitations of conventional APFs mentioned above can be overcome with Hybrid Power Filter configurations. They are typically the combination of basic APFs and passive filters. Hybrid Power Filters, inheriting the advantages of both passive filters and APFs provide improved performance and cost-effective solutions. The idea behind this scheme is to simultaneously reduce the switching noise and electromagnetic interference. There are various Hybrid Power Filters reported in literature, but the two most prominent ones are shown in Figure 2.9. Figure 2.9 (a) is the system configuration of the hybrid shunt APF. Both the shunt APF and passive filter are connected in parallel with the nonlinear load. The function of the Hybrid Power Filter can thus divided into two parts: the low-order harmonics are cancelled by the shunt APF, while the higher frequency harmonics are filtered by the passive HPF. This topology lends itself to retrofit applications with the existing shunt APF. Figure 2.9 (b) shows the system configuration of hybrid series APF, in which the series APF is coupled to the distribution line by an interfacing transformer. The shunt passive filter consists of one or more single-tuned LC filters and/or a HPF. The hybrid series APF is controlled to act as a harmonic isolator between the source and nonlinear load by injection of a controlled harmonic voltage source. It is controlled to offer zero impedance (short circuit) at the fundamental frequency and high impedance (ideally open circuit) at all undesired harmonic frequencies. This constrains all the nonlinear load current harmonics to flow into the passive filter, decoupling the source and nonlinear load at all frequencies, except at the fundamental.

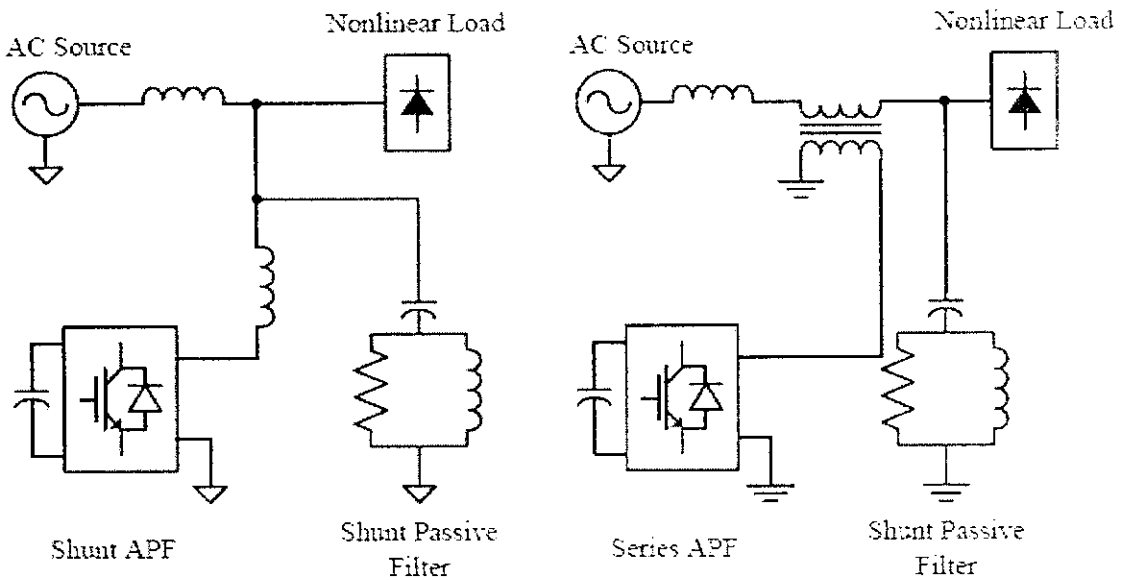


Figure 2.9 Hybrid Power Filters: (a) combination of shunt APF and shunt passive filter and (b) combination of series APF and shunt passive filter

2.4 Reference Signal Estimation Techniques

As shown in Figure 2.4, the reference signal to be processed by the controller is the key component that ensures the correct operation of APF. The reference signal estimation is initiated through the detection of essential voltage/current signals to gather accurate system variables information. The voltage variables to be sensed are AC source voltage, DC-bus voltage of the APF, and voltage across interfacing transformer. Typical current variables are load current, AC source current, compensation current and DC-link current of the APF. Based on these system variables feedbacks, reference signals estimation in terms of voltage/current levels are estimated in frequency-domain or time-domain. Numerous publications, for example report on the theories related to detection and measurement of the various system variables for reference signals estimation. Figure 2.10 illustrates the considered reference signal estimation techniques. These techniques cannot be considered to belong to the control loop since they perform an independent task by providing the controller with the required reference for further processing. This section

presents the considered reference signal estimation techniques, providing for each of them a short description of their basic features.

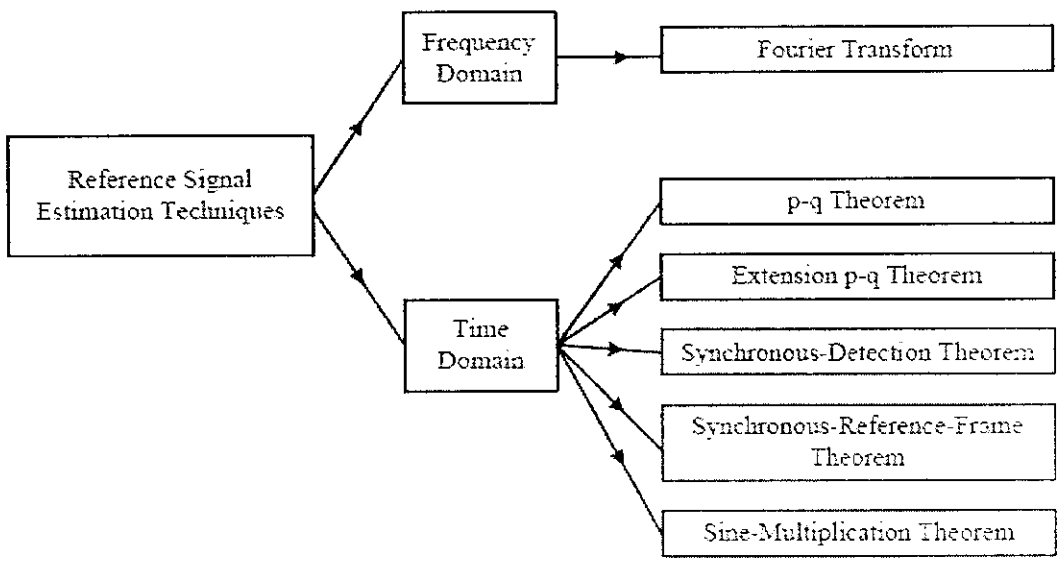


Figure 2.10 Subdivision of reference signal estimation techniques

2.5 Control Techniques for Active Power Filter

The aim of APF control is to generate appropriate gating signals for the switching transistors based on the estimated compensation reference signals. The performance of an APF is affected significantly by the selection of control techniques. Therefore, the choice and implementation of the control technique is very important for the achievement of a satisfactory APF performance. A variety of control techniques, such as linear control, digital deadbeat control, hysteresis control, etc., have been implemented for the APF applications. Several publications comprehensively report the theories related to APF control techniques. This section briefly describes the considered control techniques and their basic features.

2.5.1 Linear Control Technique

Linear control of an APF is accomplished by using a negative-feedback system as shown in Figure 2.11. In this control scheme, the compensation current (i_f) or voltage (v_f) signal is compared with its estimated reference signal ($i_{f,ref}$ or $v_{f,ref}$) through the compensated error amplifier to produce the control signal. The resulting control signal is then compared with a saw tooth signal through a pulse width modulation (PWM) controller to generate the appropriate gating signals for the switching transistors. The frequency of the repetitive saw tooth signal establishes the switching frequency. This frequency is kept constant in linear control technique. As shown in Figure 2.11, the gating signal is set high when the control signal has a higher numerical value than the saw tooth signal and via versa.

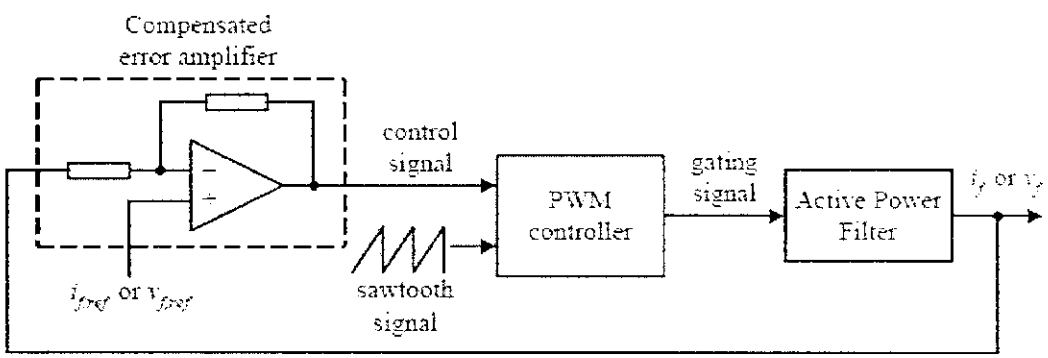


Figure 2.11 Block diagram of linear control technique

Generally, the Nyquist stability criterion and the Bode plots are used to determine the appropriate compensation in the feedback loop for the desired steady state and transient responses. With analogue PWM circuit, the response is fast and its implementation is simple. Nevertheless, due to inherent problem of analogue circuitry, the linear control technique has an unsatisfactory harmonic compensation performance. This is mainly due to the limitation of the achievable bandwidth of the compensated error amplifier.

2.5.2 Hysteresis Control Technique

The control of APF can also be realized by the hysteresis control technique. It imposes a bang-bang type instantaneous control that forces the APF compensation current (i_f) or voltage (v_f) signal to follow its estimated reference signal within a certain tolerance band. This control scheme is shown in a block diagram form in Figure 2.17. In this control scheme, a signal deviation (H) is designed and imposed on $i_{f,ref}$ or $v_{f,ref}$ to form the upper and lower limits of a hysteresis band. The i_f or v_f is then measured and compared with reference values ,the resulting error is subjected to a hysteresis controller to determine the gating signals when exceeds the upper or lower limits set by (estimated reference signal + $H/2$) or (estimated reference signal $H/2$). As long as the error is within the hysteresis band, no switching action is taken. Switching occurs whenever the error hits the hysteresis band. The APF is therefore switched in such a way that the peak-to-peak compensation current/voltage signal is limited to a specified band determined by H as illustrated by Figure 2.12.

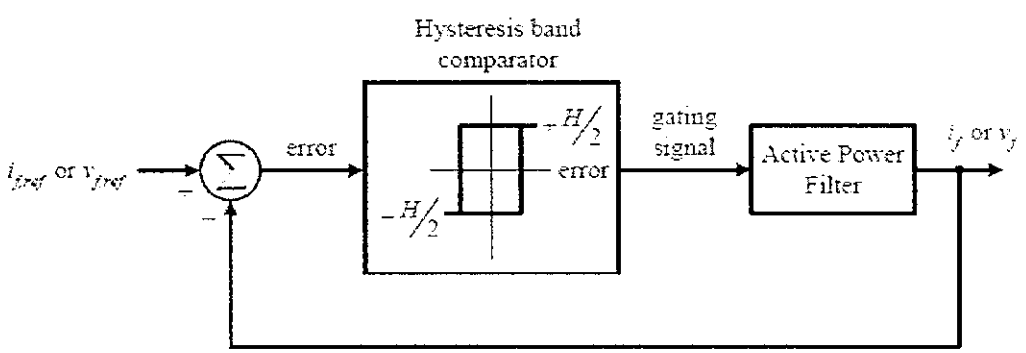


Figure 2.12 Block diagram of hysteresis control technique

In this particular work, a hysteresis current controller with a fixed H is implemented. To obtain a compensation current ($f\,i$) with switching ripples as small as possible, the value of H can be reduced. However, doing so results in higher switching frequency. Thus, increases losses on the switching transistors.

The advantages of using the hysteresis current controller are its excellent dynamic performance and controllability of the peak-to-peak current ripple within a specified hysteresis band. Furthermore, the implementation of this control scheme is simple; this is evident from the controller structure shown in Figure 2.12. However, this control scheme exhibits several unsatisfactory features. The main drawback is that it produces uneven switching frequency. Consequently, difficulties arise in designing the passive HPF. Furthermore, there is possibly generation of unwanted resonances on the power distribution system. Besides, the irregular switching also affects the APF efficiency and reliability.

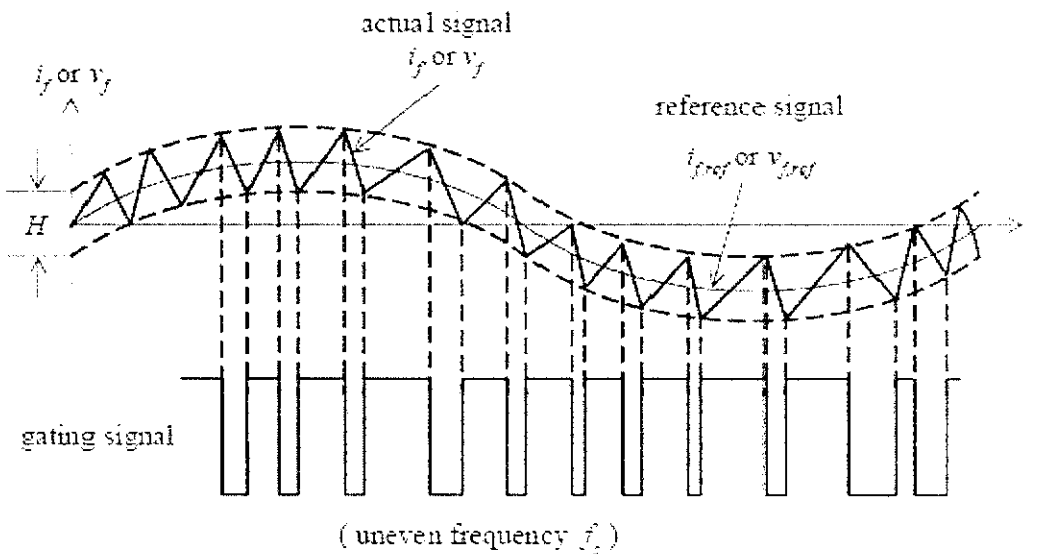


Figure 2.13 Gating signal generation by hysteresis controller

CHAPTER 3

A SINGLE PHASE HYBRID POWER FILTER

3.1 INTRODUCTION

An alternative to the passive filter is use of the Active filter, which displays better dynamics and controls the harmonic and fundamental currents.

Due the intensive use of power converter and other non linear load in industry and by consumers in general it can be observed an increasing deterioration of the power systems. Only one filter needed to eliminate all the unwanted harmonics

3.2 LINEAR AND NON LINEAR LOAD

Linear load is a load that is having constant impedance and the resulting current follows the supply voltage changes.

Examples of such loads are

- Resistance heating
- Incandescent lamp
- Unsaturated reactor

A non linear load is a load whose impedance various within each cycle and draws current disproportional to the supply voltage. At each and every point of the waveform, the load impedance varies resulting into higher or lower current then it should be. This makes load current to be non sinusoidal, resulting in to harmonics creation or distortion.

Examples of non linear load are

- Computer
- Printers
- Modem
- Variable frequency drives
- UPS
- Adjustable Speed Drives
- Diode Bridge

Figure 3.1, represent as the distortions in current similarly linear and non linear load.

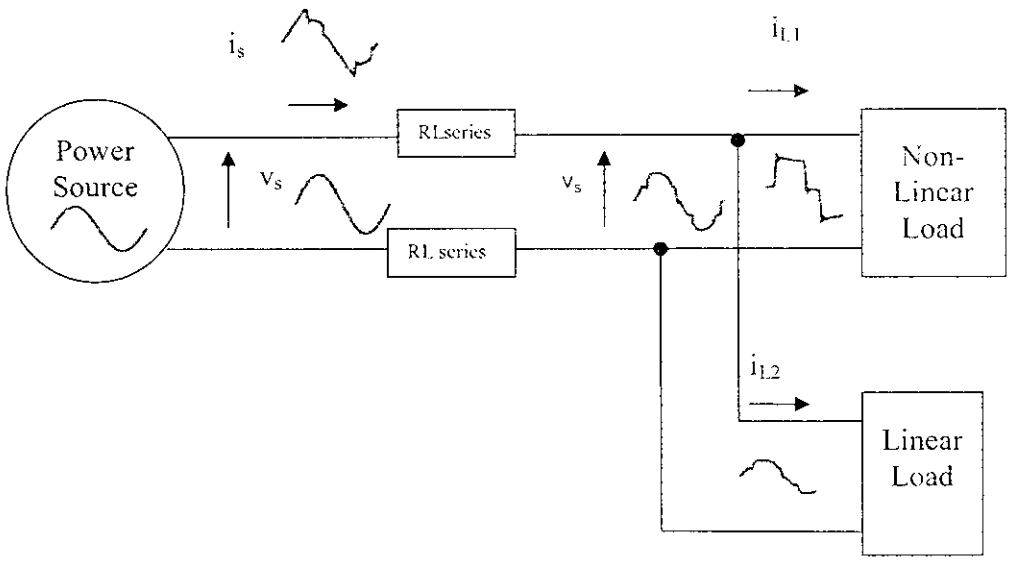


Figure 3.1 Problem due to Non linear load

3.3 Principle of the Proposed Hybrid Power Filter

The operation principle of the proposed Hybrid Power Filter is illustrated in Figure 3.2. It generates compensation current (i_f) equal to the reactive load current ($i_{L,q}$), harmonic load current ($i_{L,h}$) and reactive HPF current ($i_{hp,q}$). This compensation current is injected into the point of common coupling (PCC) through an interfacing inductor. The compensated source current (i_s) is desired to be sinusoidal and in phase with the source voltage (v_s) to yield a maximum power factor.

In the proposed scheme, the low-order harmonics are compensated using the shunt APF, while the high-order harmonics are filtered by a passive high-pass filter (HPF). Since the aim in using the HPF is to improve the filtering performance of high-order harmonics, the HPF's resonant frequency can be tuned to frequency where the filtering performance of the shunt APF is impaired, i.e. over 1 kHz. In this way, the size of the HPF can be kept small. It is envisaged that this configuration is effective to improve the filtering performance of high-order harmonics.

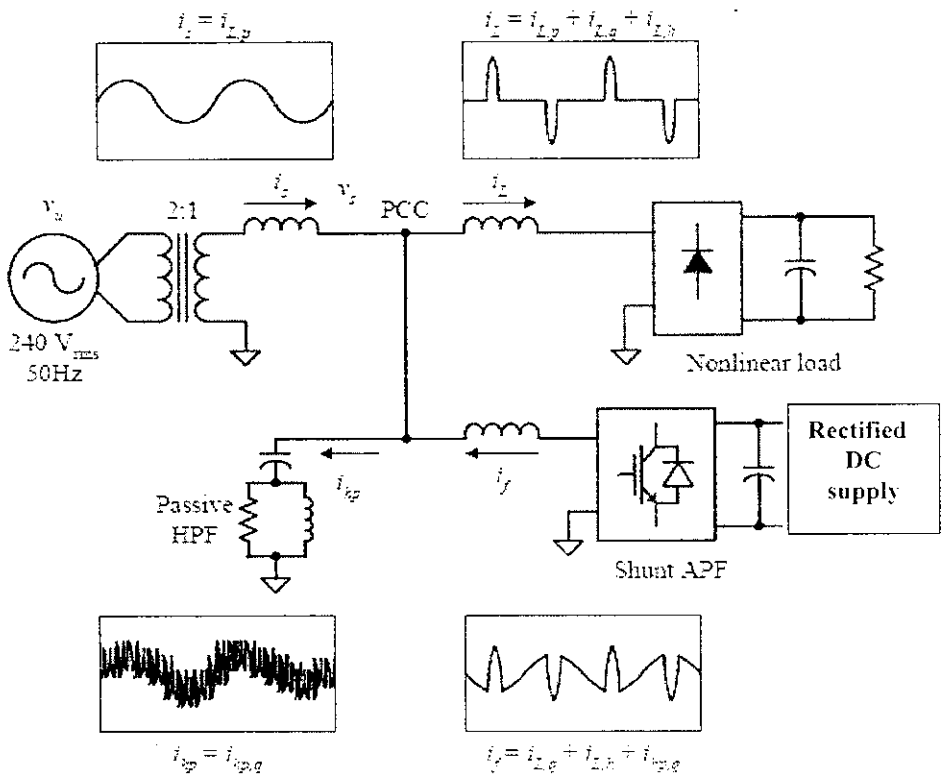


Figure 3.2 Operating principle of the proposed hybrid power filter

3.4 The Proposed System Configuration

In this section, the system configuration of the proposed single-phase Hybrid Power Filter topology is presented.

3.4.1 Proposed Overall System

Figure 3.3 shows the system configuration of the proposed single-phase Hybrid Power Filter topology, connected in parallel with the nonlinear load. It consists of a passive HPF, a single-phase shunt APF constructed using a full-bridge voltage source inverter (VSI) and a DC source that represents PV array. Subscript *s*, *L*, *f*, and *hp* refer to source, load, shunt APF and passive HPF. The shunt APF and the DC source are connected back-to-back with a DC-bus capacitor (C_f). The VSI used in this topology is operated in current controlled mode (CCM) to make the compensation current (i_f) control possible. This VSI uses DC-bus capacitor as the

supply and switches at high-frequency to generate a compensation current that follows the estimated current reference. Thus, the voltage across the DC-bus capacitor (V_{dc}) must kept to a value that is higher than the amplitude of the source voltage (> $\sqrt{2} \cdot V_s$).

The proposed Hybrid Power Filter is connected with the distribution line at the PCC through an interfacing inductor (L_f). This interfacing inductor provides isolation from the distribution line. A large interfacing inductor is preferable because it results in small switching ripple. However, the large interfacing inductor limits the dynamic response of the compensation current. Therefore, there is a compromise involved in sizing the interfacing inductor.

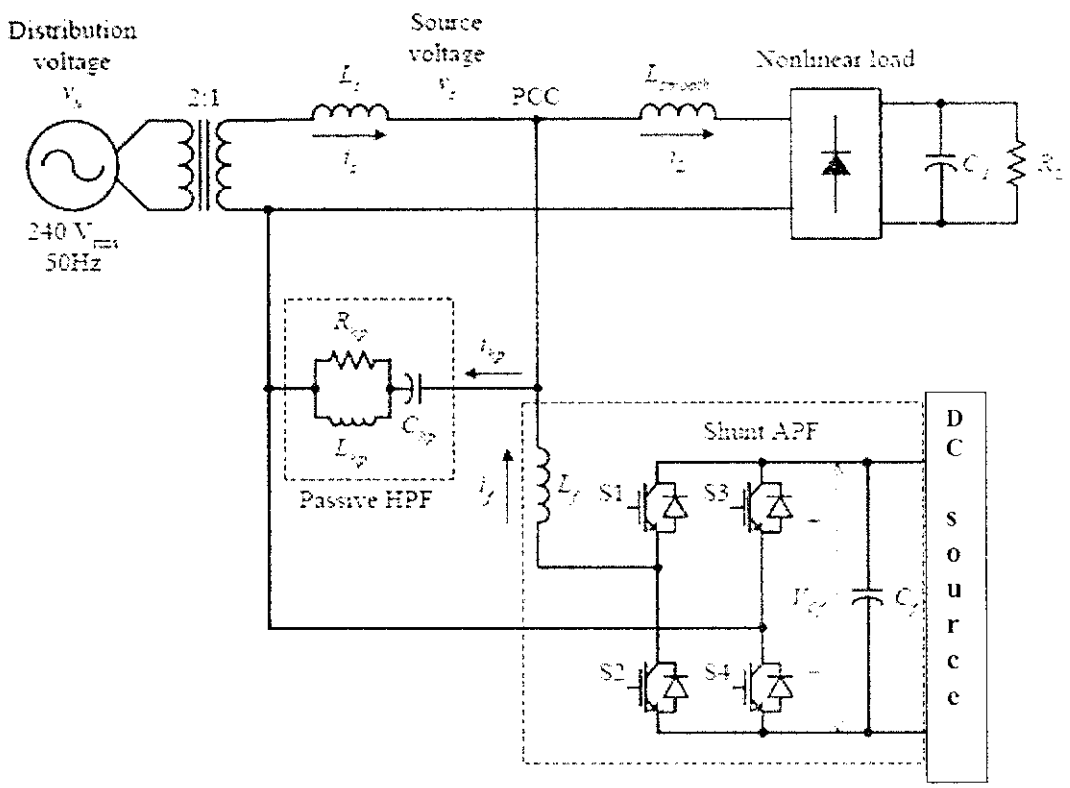


Figure 3.3 System configuration of the proposed Hybrid Power Filter

3.4.2 Proposed Extension Instantaneous Reactive-Power Theorem

The conventional p-q theorem is revised and extended to make it applicable for three-phase unsymmetrical and distorted voltage system. It differs from the conventional p-q theorem presented in. In extension p-q theorem, the source voltages are shifted by 90° for instantaneous reactive power calculation. Instead of the AC components in conventional p-q theorem, the DC components are extracted using low-pass filters (LPFs) and taking inverse transformation to obtain the compensation reference signals in terms of either currents or voltages. The main advantage of this technique is that it is simpler to find three-phase instantaneous reactive power than the conventional p-q theorem.

This technique is also suitable for single-phase APF systems. In order to illustrate the difference between the extension p-q theorem with its former, the basics of extension p-q theorem for single-phase system are presented.

The instantaneous active power of the load can be derived as

$$p = v_s(t) \cdot i_L(t) = \overline{p} + \tilde{p}$$

The instantaneous reactive power of the load can be derived as

$$q = v_s'(t) \cdot i_L(t) = \overline{q} + \tilde{q}$$

The DC components ($\overline{p}$ and $\overline{q}$) are extracted from the derived instantaneous active and reactive power using LPFs. The extracted DC components are then used for compensation reference signal estimation. It is clearly seen that the resulting equations for the instantaneous active and reactive power of the load based on extension p-q theorem are simpler compared with the conventional p-q theorem.

CHAPTER 4

THE CONTROL SYSTEM

The overall control system of the proposed single-phase Hybrid Power Filter is described in this section. The extended instantaneous reactive power theorem is used to compute the compensation current.

4.1 Overall Control System

Figure 3.4 shows the overall control system for the proposed Hybrid Power Filter. Subscript *s*, *L*, *f*, and *hp* refer to source, load, shunt APF and passive HPF. The task of the control system is to produce appropriate gating signals for the switching transistors (IGBTs or MOSFETs). The control system consists of an instantaneous active/reactive power calculator, three LPFs, a compensation current estimator, a proportional integral (PI) controller, a PLL and a hysteresis current controller.

Three current sensors and two voltage sensors are required for system variables detection. The load current (i_L), HPF current (i_{hp}) and compensation current (i_f) are detected using Hall-Effect current sensors, while the source voltage (V_s) and DC-bus voltage (V_{cf}) are detected using Hall-Effect voltage sensors. The digital based PLL is responsible to generate the reference sinewave ($\sin(\omega t)$ and $\sin(\omega t - 90^\circ)$) with unity amplitude and synchronous with the source voltage.

The instantaneous active/reactive power calculator receives the load current, source voltage and passive HPF current signals in real time. The instantaneous active load power (P_L), instantaneous reactive load power (q_L) and the instantaneous reactive HPF power (q_{hp}) are calculated based on the extension p-q theorem. Their DC components are filtered with three digital second-order Butterworth LPFs. These DC components are then fed to the compensation current reference estimator to obtain the reactive load current, harmonic load current and reactive HPF current. The summation of these three current signals will form the first component of the current reference signal.

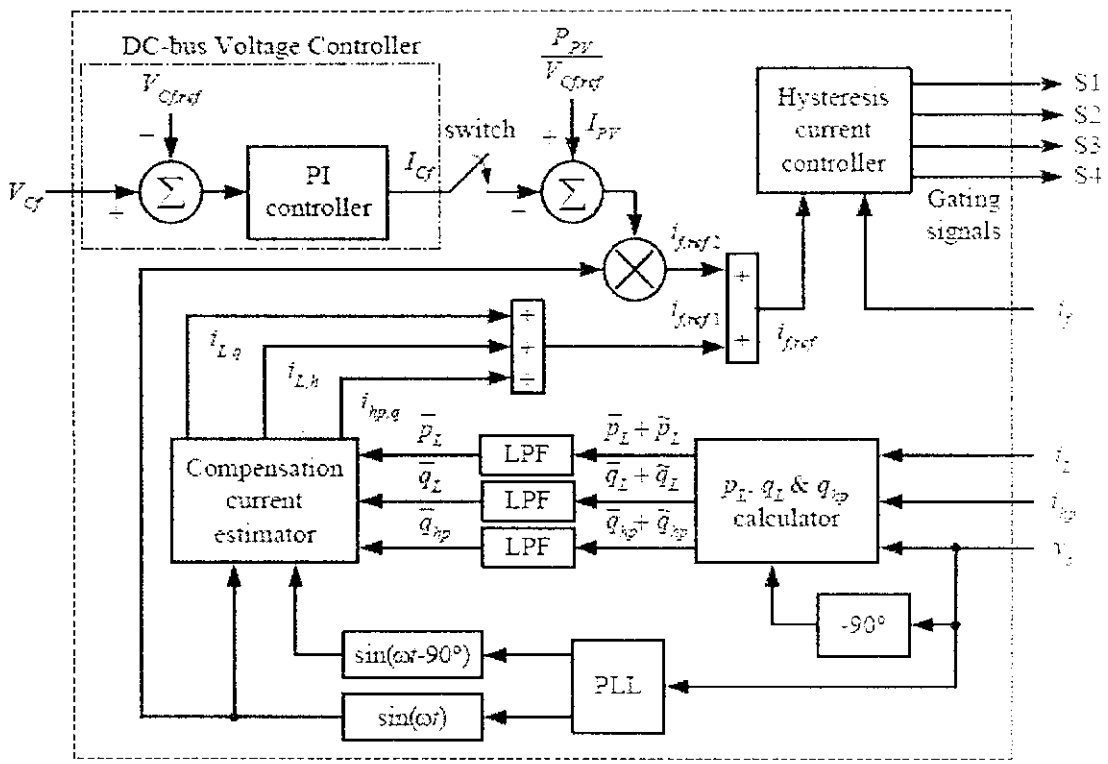


Figure 4.1 Overall control system of the proposed Hybrid Power Filter

The DC voltage across the DC-bus capacitor is detected and compared with its reference voltage (V_{Cf_ref}). The compared result is processed by a PI controller to obtain the desired amplitude of the DC-bus capacitor charging current (I_{Cf}). The resulting current is then multiplied with the reference sinewave ($\sin(\omega t)$) to form the second component of current reference signal (i_{f_ref2}).

In order to generate the compensation current that follows the current reference signal, the fixed-band hysteresis current control method is adopted. The estimated compensation current reference signal (i_{f_ref}) and the actual compensation current signal (i_f) are fed to a fixed-band hysteresis current controller to generate appropriate gating signals for the switching transistors.

4.2 DC-Bus Voltage Control

Under a loss free situation, the Hybrid Power Filter need not provide any active power to cancel the reactive and harmonic currents from the load, and the reactive current from the HPF. These currents show up as reactive power. Thus, it is indeed possible to make the DC-bus capacitor delivers the reactive power demanded by the proposed Hybrid Power Filter. As the reactive power comes from the DC-bus capacitor and this reactive energy transfers between the load and the DC-bus capacitor (charging and discharging of the DC-bus capacitor), the average DC-bus voltage can be maintained at a prescribed value.

However, due to switching loss, capacitor leakage current, etc., the distribution source must provide not only the active power required by the load but also the additional power required by the VSI to maintain the DC-bus voltage constant. Unless these losses are regulated, the DC-bus voltage will drop steadily.

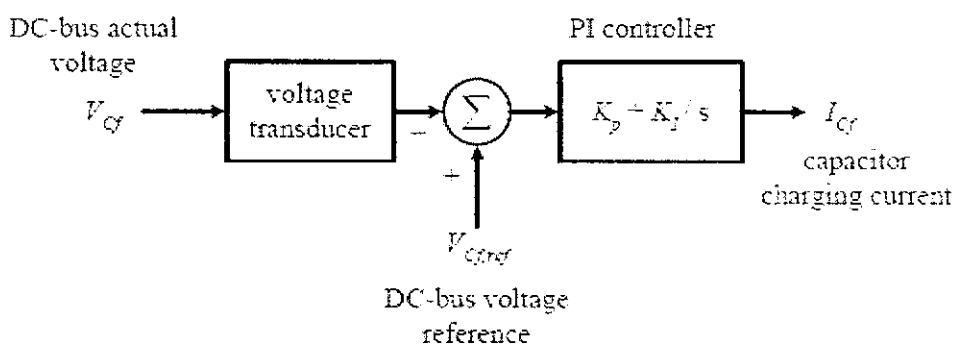


Figure 4.2 PI controller for DC-bus voltage control

4.3 Compensation Current Reference Estimation

Compensation current reference estimation for single-phase shunt APF based on extension p-q theorem. In this work, the application of the theorem is further extended to a single-phase Hybrid Power Filter. In the proposed topology, the extension p-q theorem is adopted for the estimation of active, reactive and harmonic components of load current, and the reactive component of HPF current.

The compensation current reference can be estimated as

$$i_{f,ref} = i_{L,q} + i_{L,h} + i_{hp,q} - I_{cf}.\sin(\omega t) + \frac{P}{V_{cf,\,ref}}.\sin(\omega t)$$

Here,

$i_{L,q}$ - Reactive load current

$i_{L,h}$ - Harmonic load current

$i_{hp,q}$ - HPF current

I_{cf} - DC bus capacitor charging current

$V_{cf,\,ref}$ - DC bus reference voltage

CHAPTER 5

SIMULATION OF THE PROPOSED HYBRID ACTIVE POWER FILTER

5.1 INTRODUCTION

The simulation of power electronic systems provides advantages in the design process by allowing various options to be tried out before the hardware is built. To validate the feasibility of the proposed approach, a virtual implementation of the SAPF is done using Simulink.

MATLAB is a software package for high performance numerical computation and visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. The name MATLAB stands for matrix laboratory. There are several optional toolboxes available from the developers of MATLAB. These toolboxes are collection of functions written for special application such as sim power system, control system, artificial intelligent, image processing etc.

5.2 SIMULINK MODEL OF PROPOSED SYSTEM

The complete simulation model of the proposed scheme, constructed using the MATLAB/Simulink environment is depicted. It consists of distribution source, nonlinear load, shunt APF, passive HPF, overall control system and DC bus capacitor. Both the models of the system with and without power filter are shown.

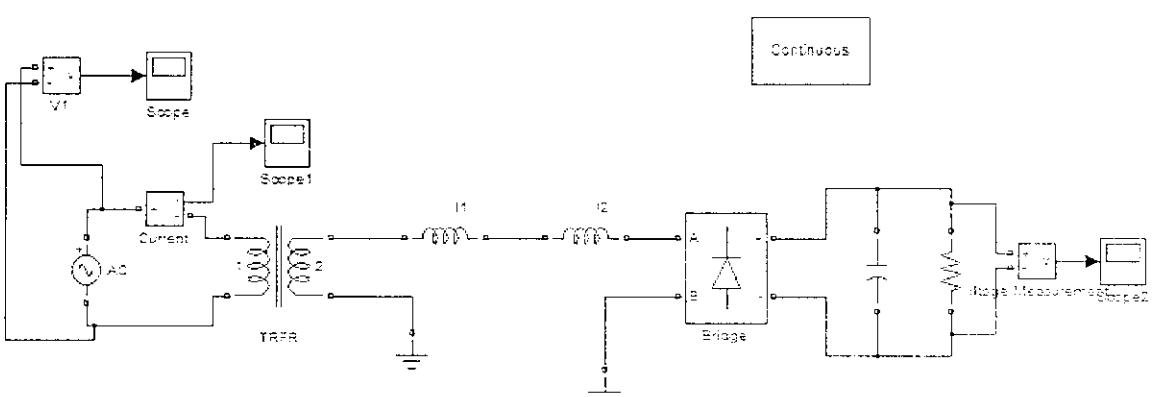


Figure 5.1 simulink model without hybrid filter

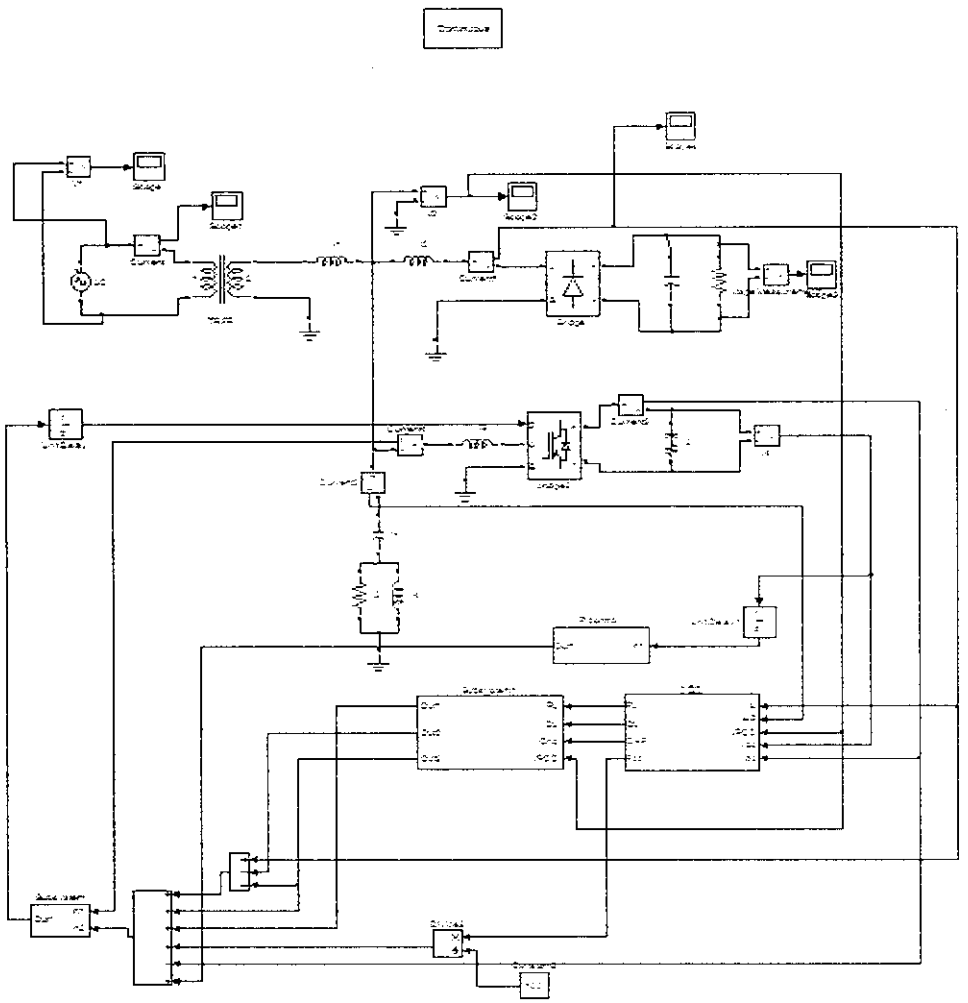


Figure 5.2 simulink model with hybrid filter

The power distribution source considered in the simulations is a 240 V_{rms}, 50 Hz sinusoidal single-phase AC voltage source. This corresponds to the domestic utility voltage in India. The distribution voltage is generated by the "AC Voltage Source" blockset from "SimPowerSystems\Electrical Source" library. The isolation transformer with turn ratio of 2:1 is constructed using the "Linear Transformer" blockset from "SimPowerSystems\Elements" library. Note that the secondary leakage inductor of the isolation transformer is considered as the source inductor (L_s). A source resistor (R_s) is connected in series to limit the inrush current. The L_s and R_s are constructed using "Series RLC Branch" blockset.

A diode bridge rectifier circuit which feeds a resistive load filtered by a capacitor which symbolizes normal rectification process in practical loads like arc furnace, smps. etc. A controlled rectifier circuit with thyristor can also be chosen as a source of non linear current which practically takes place in the case of variable speed drives.

The shunt APF block consists of a VSI bridge inverter fed by a DC bus capacitor. The bridge inverter circuit is simulated using IGBTs as the switching devices. IGBTs have a good dynamic response and fast switching compared to other options like mosfet. The DC bus capacitor is the source for VSI whose DC voltage should be controlled (a PI controller is used for that purpose).

5.3 OVERALL CONTROL SYSTEM

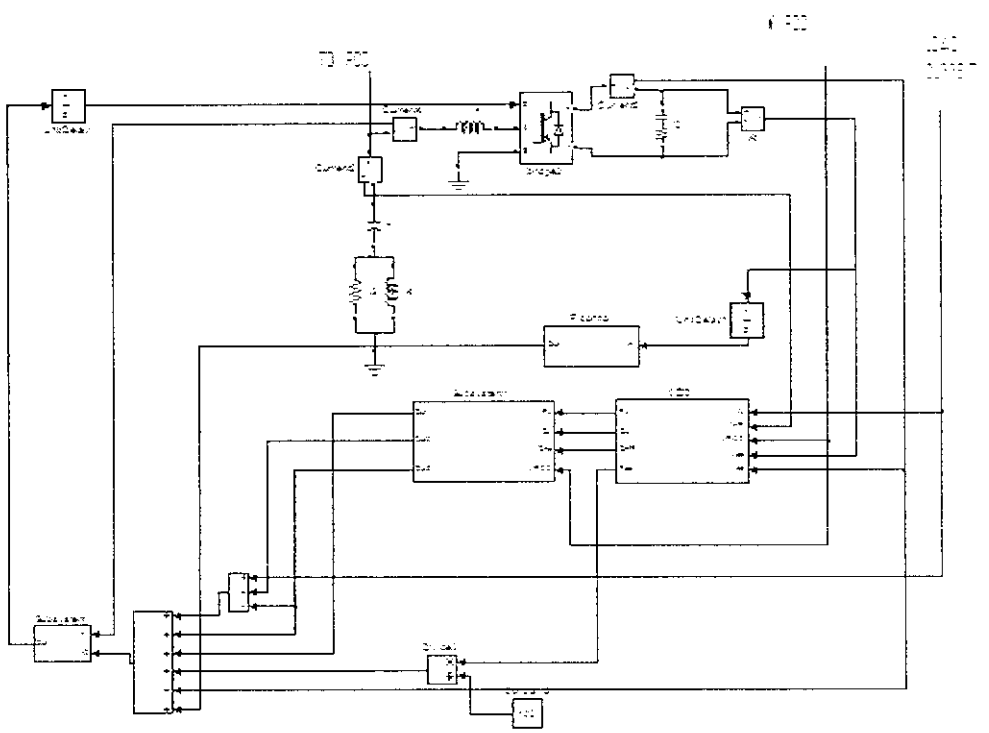


Figure 5.3 simulink model of overall control system

The overall control system performs the extended p-q theorem. The subsystem p@q gets input data of load current, high pass filter current, pcc voltage, dc bus capacitor voltage and its current. The outputs generated from this block are real and reactive powers of load, real power of dc bus capacitor and the reactive power of HP filter. From these outputs the subsystem 1 generates further the compensation reference current which is used to generate the compensation current from the VSI bridge.

CHAPTER 6

SIMULATION RESULTS

6.1 INTRODUCTION

The purpose of the simulation is to show the usefulness of the proposed APF control strategy. The main aim of this simulation is to bring the THD value in the source current waveform to a level below 5% as per the IEEE standards.

6.2 PROPOSED SYSTEM WITH OUT FILTER

The filter is not connected in between the source and load side means current harmonics will acquire in the source side. Its clearly represent the figure 5.1 and 5.2. The below mentioned figure represent as the wave form of a source current and THD plot value of source current in without filter. There for source current obtain the high distortion. So the Current THD is 21.35%. It is higher than the IEEE (IEEE 519) standard. So we reduced the THD value use the active power filter.

Figure 6.1 source current without filter

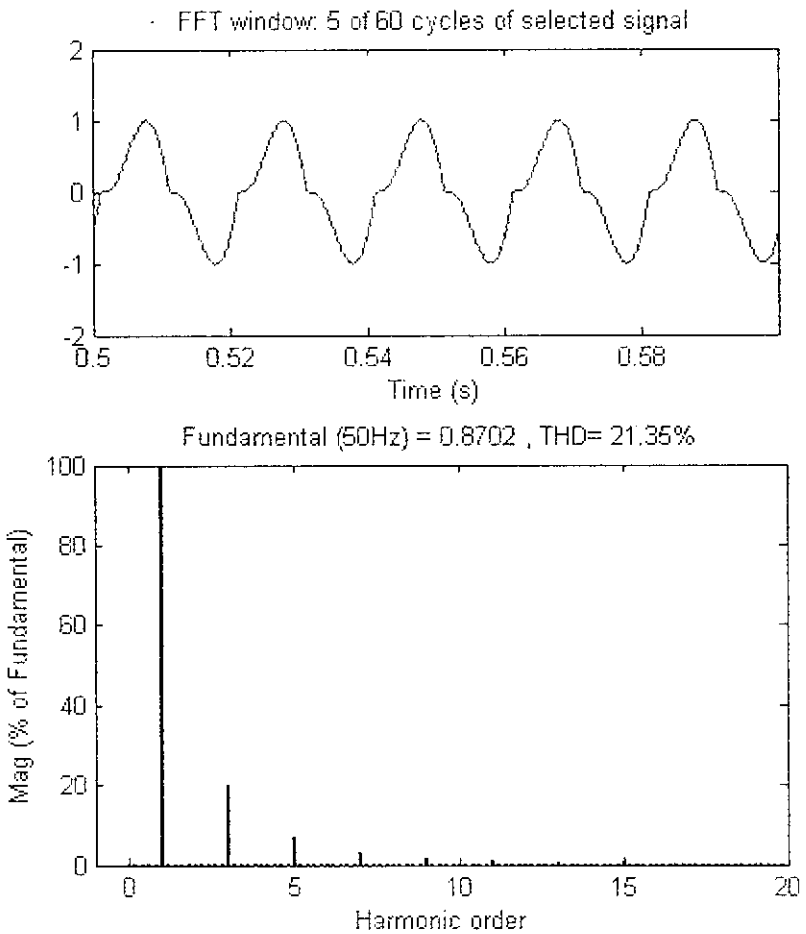


Figure 6.2 source current and THD values without filter

6.3 PROPOSED SYSTEM WITH FILTER

Use the proposed algorithm is used to minimize the current harmonics in source side, thereby reducing the THD value, and improve the power factor. Its clearly represent as the following figures.

Therefore source current with reduced distortions are obtained and the Current THD reduced to is 4.41%. The following figure represents the source current and their THD with the presence of hybrid filter.

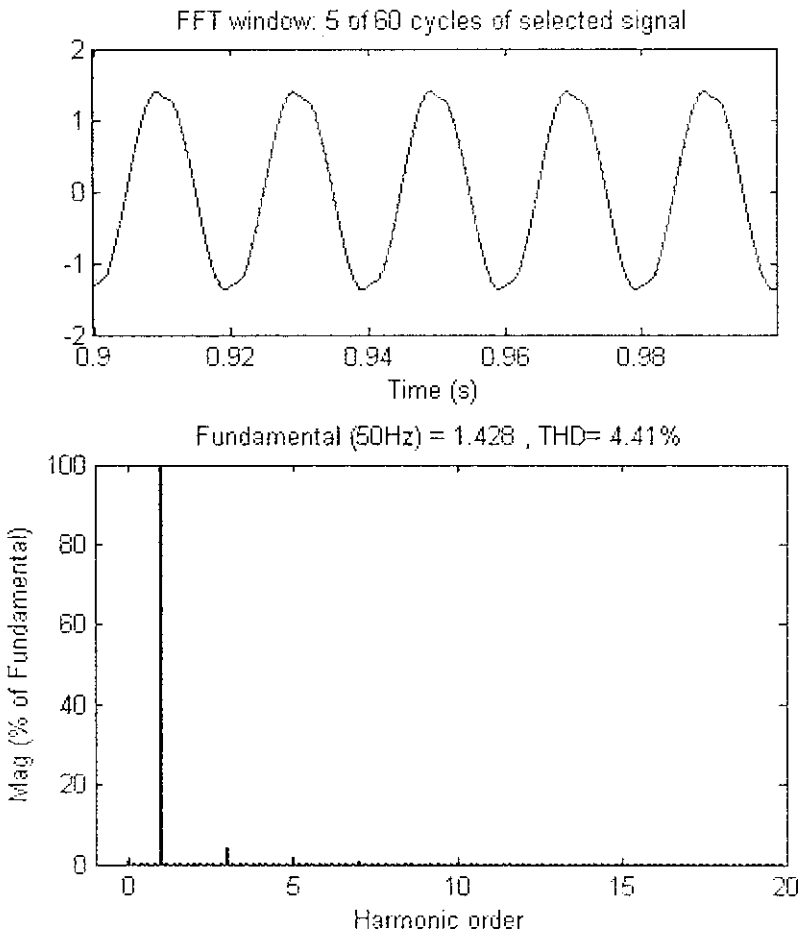


Figure 6.3 source current and THD values with filter

6.4 ANALYSIS AND DISCUSSION OF SIMULATION RESULTS

The simulation results are available for two cases considered From figure 5.1 to Figure 5.3, it is clearly represent the with filter and without filter conditions and the APF compensates harmonic currents into the line there for making the input supply is sinusoidal. The improvisation of power quality is given below as THD improvement.

Source current THD in % (Without filter)	Source current THD in % (With filter)
21.35	4.41

CHAPTER-7

HARDWARE IMPLEMENTATION AND RESULTS

7.1 INTRODUCTION

A prototype of the project is developed using a PIC microcontroller as the control circuit and a mosfet bridge as the VSI inverter. A H-bridge inverter with four IRF250 mosfets is constructed which is then coupled to the main system using a coupling transformer. The inverter circuit obtains the command from the microcontroller. A potentiometer is used to bring changes in the source current and to which the controller code activates the gating pulses to the inverters.

7.2 HARDWARE SETUP

The hardware consists of three main portions. The power supply and load section, the microcontroller and the VSI inverter bridge with DC capacitor.

Three separate power supply circuits are being used in this project. A 230V/50 Hz power supply is stepped down to 9V by a step down transformer. This stepped down supply is fed to the diode bridge rectifier through a 63V/2200mfd capacitor in parallel which acts as a smoothing filter. A 1 ohm /5V resistor is fixed in series with the rectifier across which the CRO is connected to view the waveform. A 230VAC supply is stepped down to a 5V and 15V by step down transformers to supply the isolation circuits. These supplies are regulated by the IC voltage regulators.

The VSI Bridge is supplied from a step supply across a 1000mfd capacitor which derives its energy from the stepped down supply. The microcontroller senses the input current through the port RA0 in pin2 which acts an ADC in this project. The driving commands to the VSI bridge inverter is fired through the ports RB4, RB5, RB6, RB7 through an opto-isolator circuit.

The VSI bridge inverter converts the input dc to the compensating waveform as commanded by the microcontroller. A reset circuit is also provided to the microcontroller through a 7414 IC at pin1. The output of VSI Bridge is injected into the source –load system through a coupling transformer with 1:1 ratio.

7.3 WORKING:

The RL load connected in the setup acts as the source of harmonics. The harmonics produced due to this load is shown below in the picture. The supply is 9V AC. The current is sensed through a potentiometer which is adjusted to bring the compensation. The microcontroller performs the algorithm to generate the PWM driving pulses for the H-bridge MOSFET. These signals are isolated and amplified through the opto-isolators provided for each MOSFET device. The opto-coupler devices are given with separate supply for functioning.

The inverter is supplied with DC supply of 12V through a bridge rectifier. The inverter produces compensating waveforms as commanded by the controller. This compensating current is fed to the line through a transformer.

As the load varies the distortion or the waveform shape varies accordingly. This project is designed for a particular load of bridge rectifier supplying an RL load. To view the results for various values of the resistance / inductance a reset circuit of the controller is used each time for the corresponding compensation waveform.

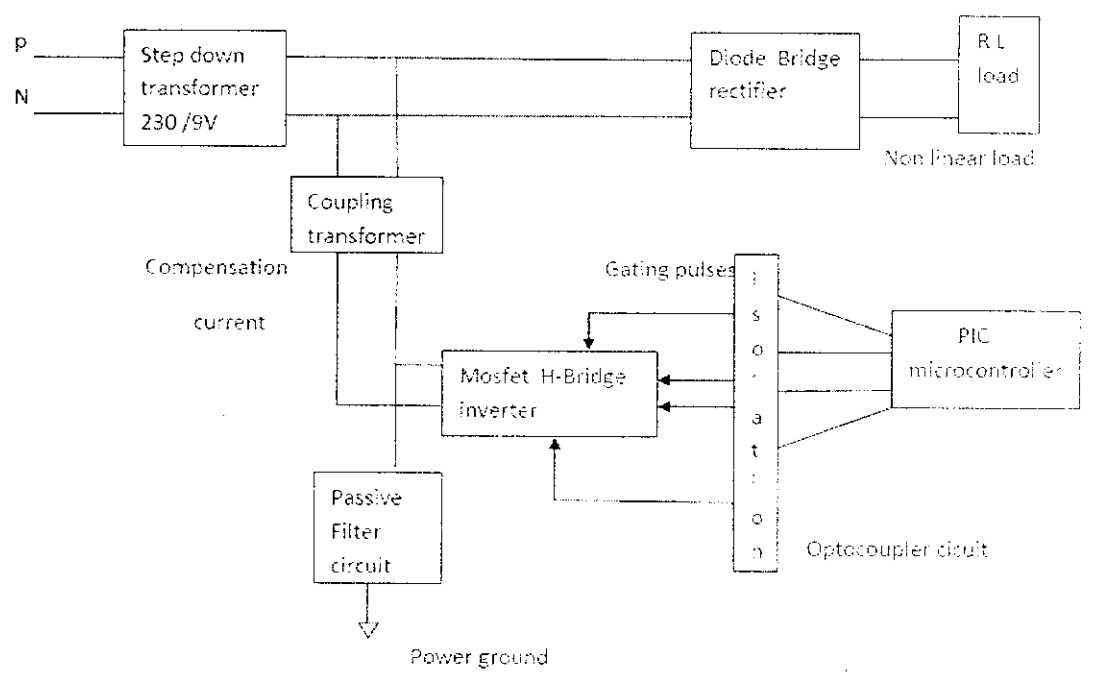


FIG 7.1 BLOCK DIAGRAM OF THE PROTOTYPE DEVELOPED

FIG 7.2 The hardware setup with a RL load (without filter condition)

7.4 WAVEFORM RESULTS:

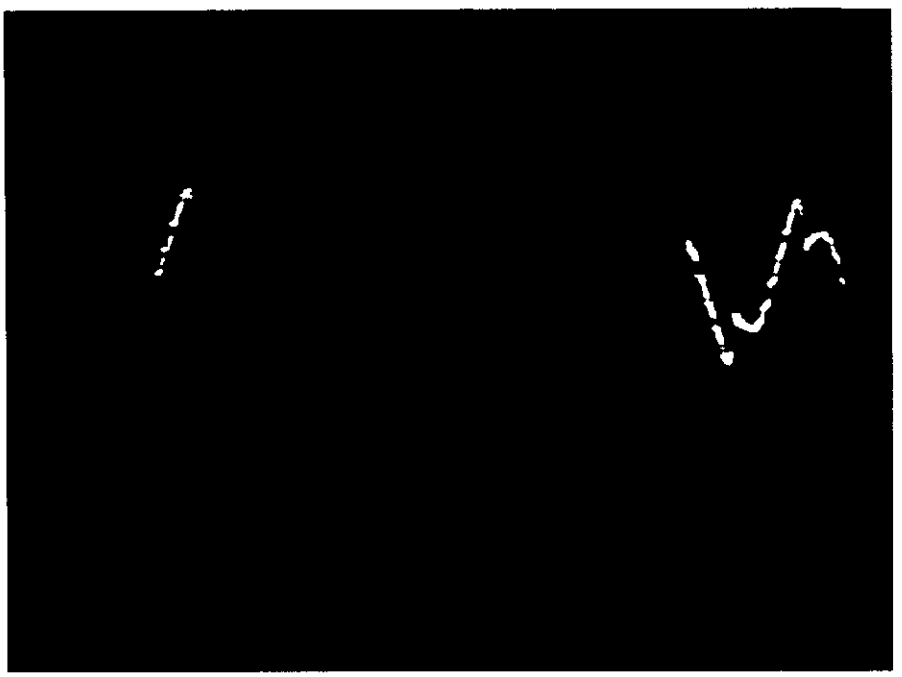


FIG 7.3a WAVEFORM OF SOURCE CURRENT WITH R-L LOAD

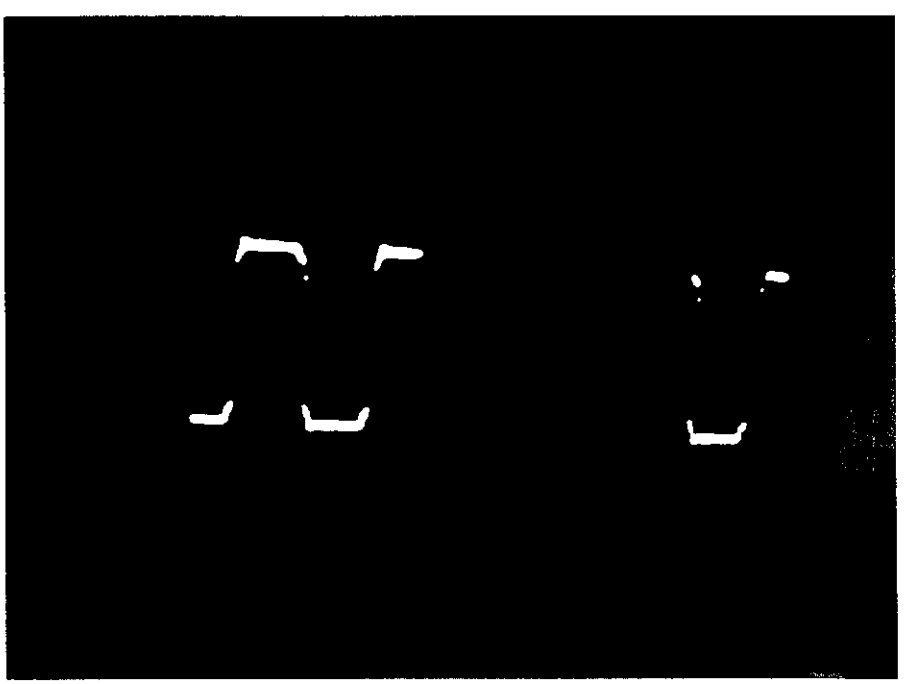


FIG 7.3b WAVEFORM WITH SAME SETUP AFTER FILTERING

7.5 DESCRIPTION OF THE COMPONENTS

7.5.1 POWER SUPPLY

The ac voltage, typically 220V rms, is connected to a transformer, which steps that ac voltage down to the level of the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation.

A regulator circuit removes the ripples and also remains the same dc value even if the input dc voltage varies, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of the popular voltage regulator IC units.

THREE-TERMINAL VOLTAGE REGULATORS

Fig shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

FIXED POSITIVE VOLTAGE REGULATORS:

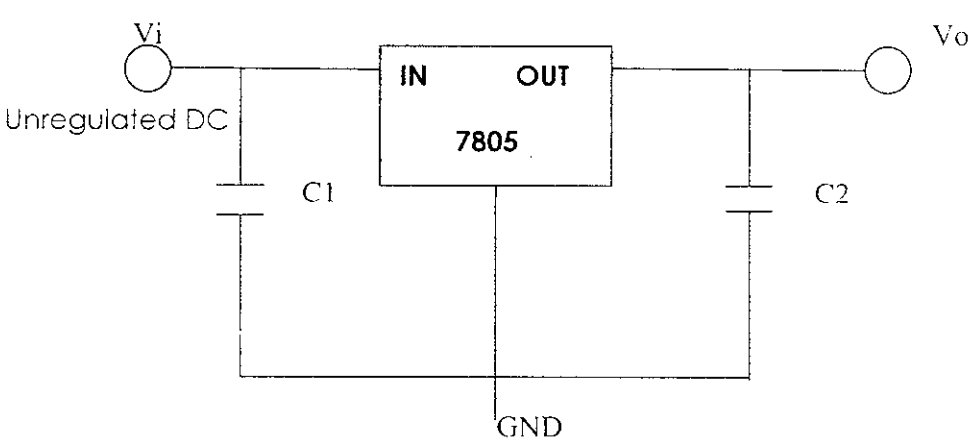


Fig 7.4 voltage regulator IC

The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated + 12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulated ICs is provided in table below.

IC Part	Output Voltage (V)	Minimum Vi (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

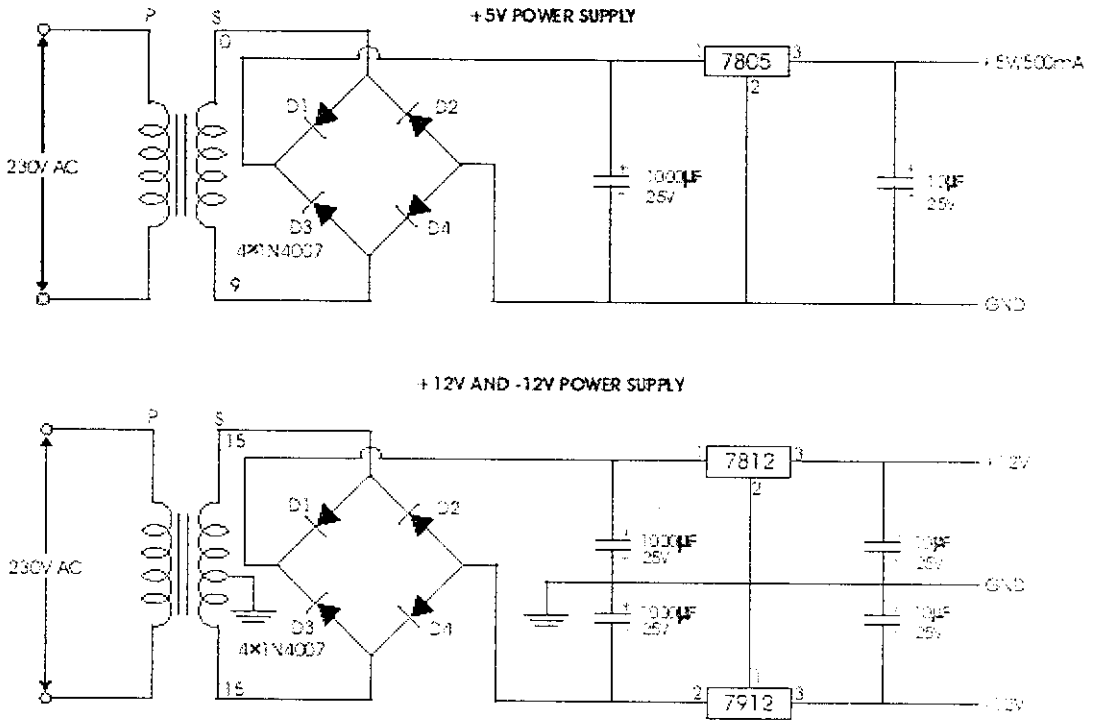


Fig7.5 Power supply circuit diagram

7.5.2 H-BRIDGE INVERTER

The bridge inverter circuit is constructed using mosfet devices. They are isolated from the control circuit using opto-couplers which protects the damage of any control devices.

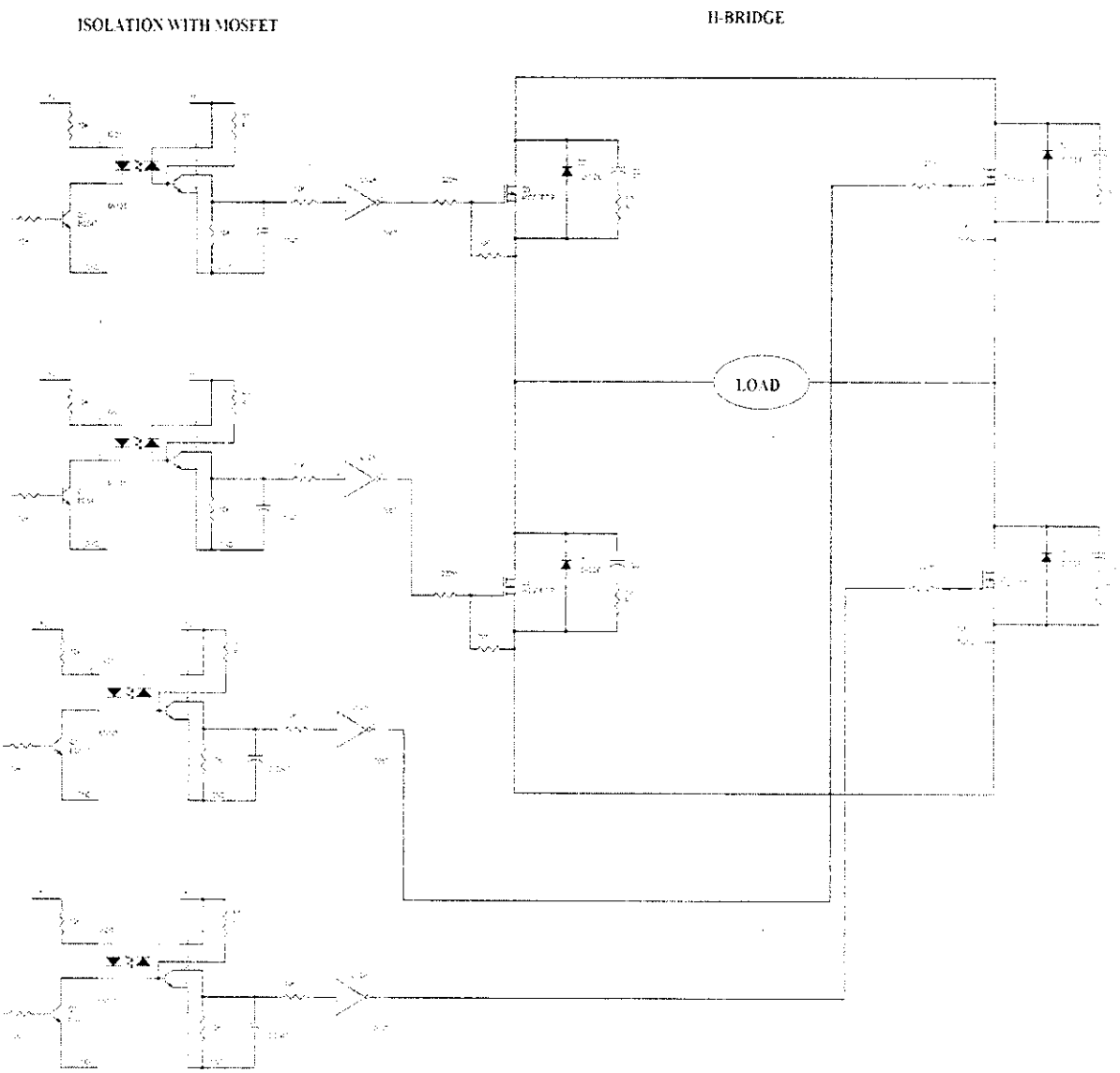


Fig 7.6 H-bridge inverter circuit

CIRCUIT WORKING DESCRIPTION:

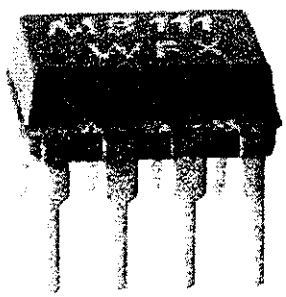
The isolation circuit is mainly used to isolate the high voltage and low voltage circuit, SCR and Triac circuit, mechanical relay and pulse transformer. Here the isolation circuit is constructed by the 6N135 opto coupler. The opto coupler consists of photo LED and photo transistor. The photo transistor conducting only when light rays falls on the base of the transistor. The signal to be isolated is given to base of BC547 switching transistor.

Whenever the signal is high, the transistor is switched ON, so the emitter and collector terminals are shorted. Now the photo LED is conducting and light rays falls on the photo transistor. Due to that the photo transistor is conducting and shorts the emitter and collector terminal. The 7667 inverter is connected in the collector terminal. So the ground signal that is zero signals is given to inverter input and high pulse is taken from the inverter output. Now the output pulse is equal to input pulse as applied to the base of the transistor BC547 (Q1).

OPTOCOUPLER :

In electronics, an opto-isolator (or optical isolator, optocoupler, photocoupler, or photoMOS) is a device that uses a short optical transmission path to transfer a signal between elements of a circuit, typically a transmitter and a receiver, while keeping them electrically isolated — since the signal goes from an electrical signal to an optical signal back to an electrical signal, electrical contact along the path is broken. A common implementation involves a LED and a phototransistor, separated so that light may travel across a barrier but electrical current may not. When an electrical signal is applied to the input of the opto-isolator, its LED lights, its light sensor then activates, and a corresponding electrical signal is generated at the output. Unlike a transformer, the opto-isolator allows for DC coupling and generally provides significant protection from serious overvoltage conditions in one circuit affecting the other.

With a photodiode as the detector, the output current is proportional to the amount of incident light supplied by the emitter. The diode can be used in a photovoltaic mode or a photoconductive mode. In photovoltaic mode, the diode acts like a current source in parallel with a forward-biased diode. The output current and voltage are dependent on the load impedance and light intensity.



In photoconductive mode, the diode is connected to a supply voltage, and the magnitude of the current conducted is directly proportional to the intensity of light. An opto-isolator can also be constructed using a small incandescent lamp in place of the LED; such a device, because the lamp has a much slower response time than an LED, will filter out noise or half-wave power in the input signal. In so doing, it will also filter out any audio- or higher-frequency signals in the input. It has the further disadvantage, of course, (an overwhelming disadvantage in most applications) that incandescent lamps have relatively short life spans. Thus, such an unconventional device is of extremely limited usefulness, suitable only for applications such as science projects.

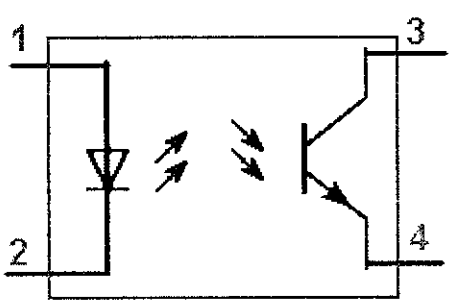


Fig 7.7 Optocoupler

The optical path may be air or a dielectric waveguide. The transmitting and receiving elements of an optical isolator may be contained within a single compact module, for mounting, for example, on a circuit board; in this case, the module is often called an optoisolator or opto-isolator. The photosensor may be a photocell, phototransistor, or an optically triggered SCR or Triac.

Occasionally, this device will in turn operate a power relay or contactor. They are used to isolate low-current control or signal circuitry from transients generated or transmitted by power supply and high-current control circuits. The latter are used within motor and machine control function blocks.

MOSFET:

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is by far the most common field-effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material (see article on semiconductor devices), and is accordingly called an NMOSFET or a PMOSFET (also commonly nMOSFET, pMOSFET).

The 'metal' in the name is now often a misnomer because the previously metal gate material is now a layer of polysilicon (polycrystalline silicon; why polysilicon is used will be explained below). Previously aluminium was used as the gate material until the 1980s when polysilicon became dominant, owing to its capability to form self-aligned gates.

To overcome power consumption increase due to gate current leakage, high-? dielectric is replacing silicon dioxide as the gate insulator, and metal gates are making a comeback by replacing polysilicon .

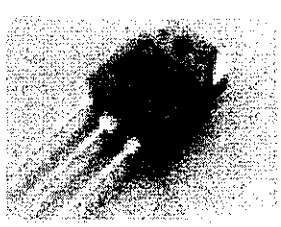


Fig 7.8 Mosfet IRF250

IGFET is a related, more general term meaning insulated-gate field-effect transistor, and is almost synonymous with MOSFET, though it can refer to FETs with a gate insulator that is not oxide. Some prefer to use "IGFET" when referring to devices with polysilicon gates, but most still call them MOSFETs.

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM, have begun to use a mixture of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces and thus are not suitable for MOSFETs. However there continues to be research on how to create insulators with acceptable electrical characteristics on other semiconductor material.

The gate is separated from the channel by a thin insulating layer of what was traditionally silicon dioxide, but more advanced technologies used silicon oxynitride. Some companies have started to introduce a high-? dielectric + metal gate combination in the 45 nanometer node.

When a voltage is applied between the gate and source terminals, the electric field generated penetrates through the oxide and creates a so-called "inversion layer" or channel at the semiconductor-insulator interface. The inversion channel is of the same type – P-type or N-type – as the source and drain, so it provides a conduit through which current can pass. Varying the voltage between the gate and body modulates the conductivity of this layer and makes it possible to control the current flow between drain and source.

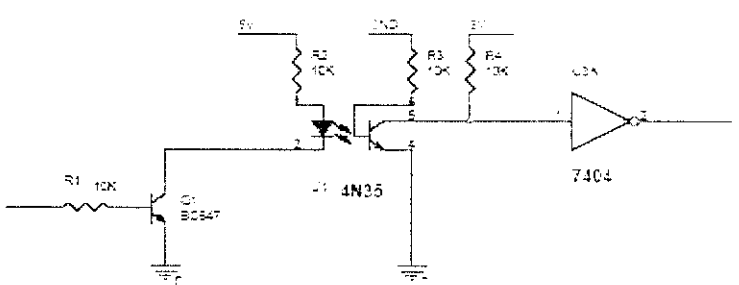


Fig 7.9 Opto Coupler with isolation

7.5.3 MICROCONTROLLER:

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complimentary

metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

PIC (16F877):

Various microcontrollers offer different kinds of memories. EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

SPECIAL FEATURES OF PIC MICROCONTROLLER:

CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input

  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,

  Up to 368 x 8 bytes of Data Memory (RAM)

  Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external

- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:

  < 2mA typical @ 5V, 4 MHz

  20mA typical @ 3V, 32 kHz

  < 1mA typical standby current

PERIPHERAL FEATURES:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules

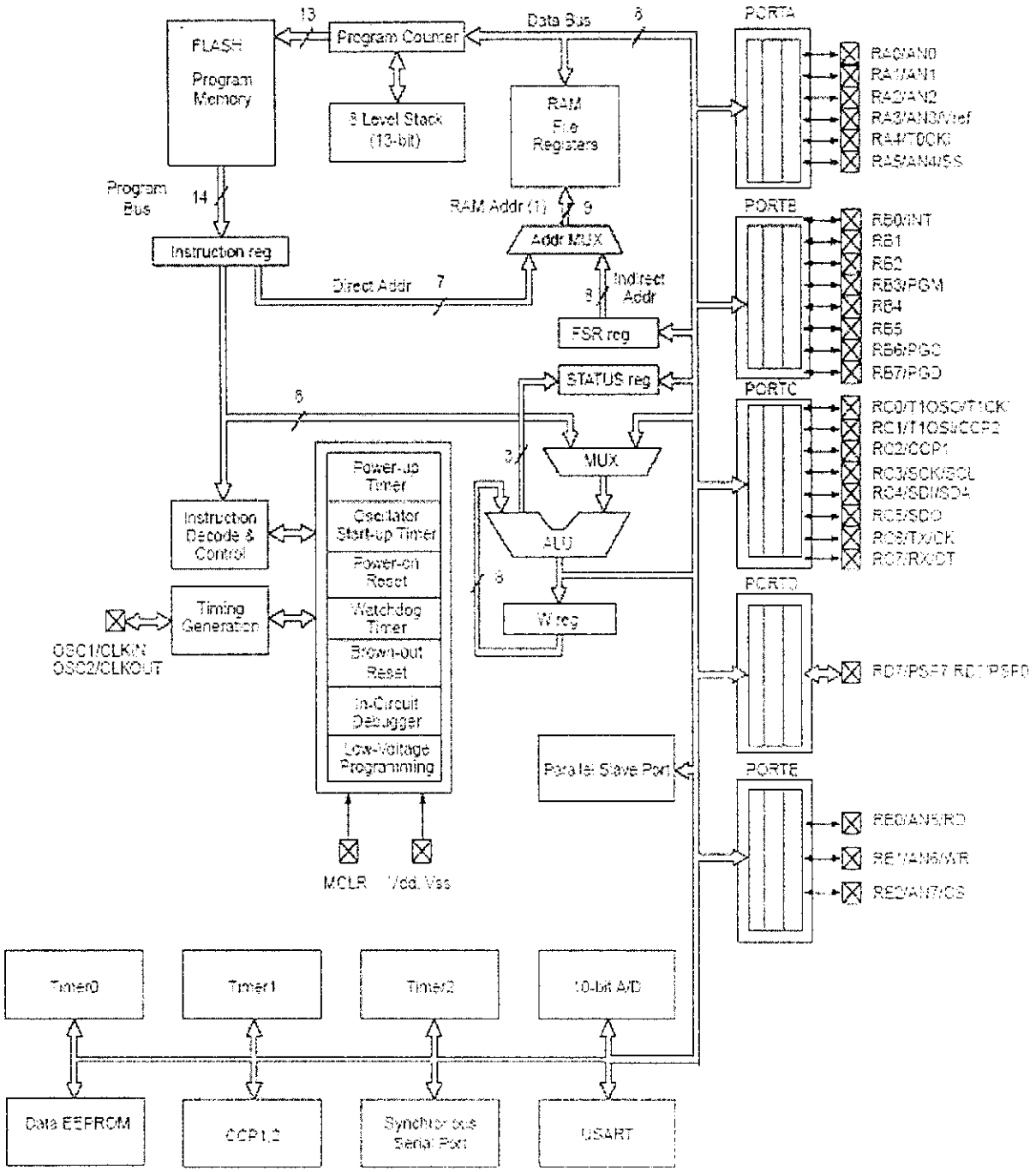
  Capture is 16-bit, max resolution is 12.5 ns,

  Compare is 16-bit, max resolution is 200 ns,

  PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9- bit address detection.

ARCHITECTURE OF PIC 16F877 :

The complete architecture of PIC 16F877 is shown in the fig 2.1. Table 2.1 gives details about the specifications of PIC 16F877. Fig 2.2 shows the complete pin diagram of the IC PIC 16F877.



Note 1: Higher order bits are from the STATUS register.

fig 7.10 ARCHITECTURE OF PIC 16F877A

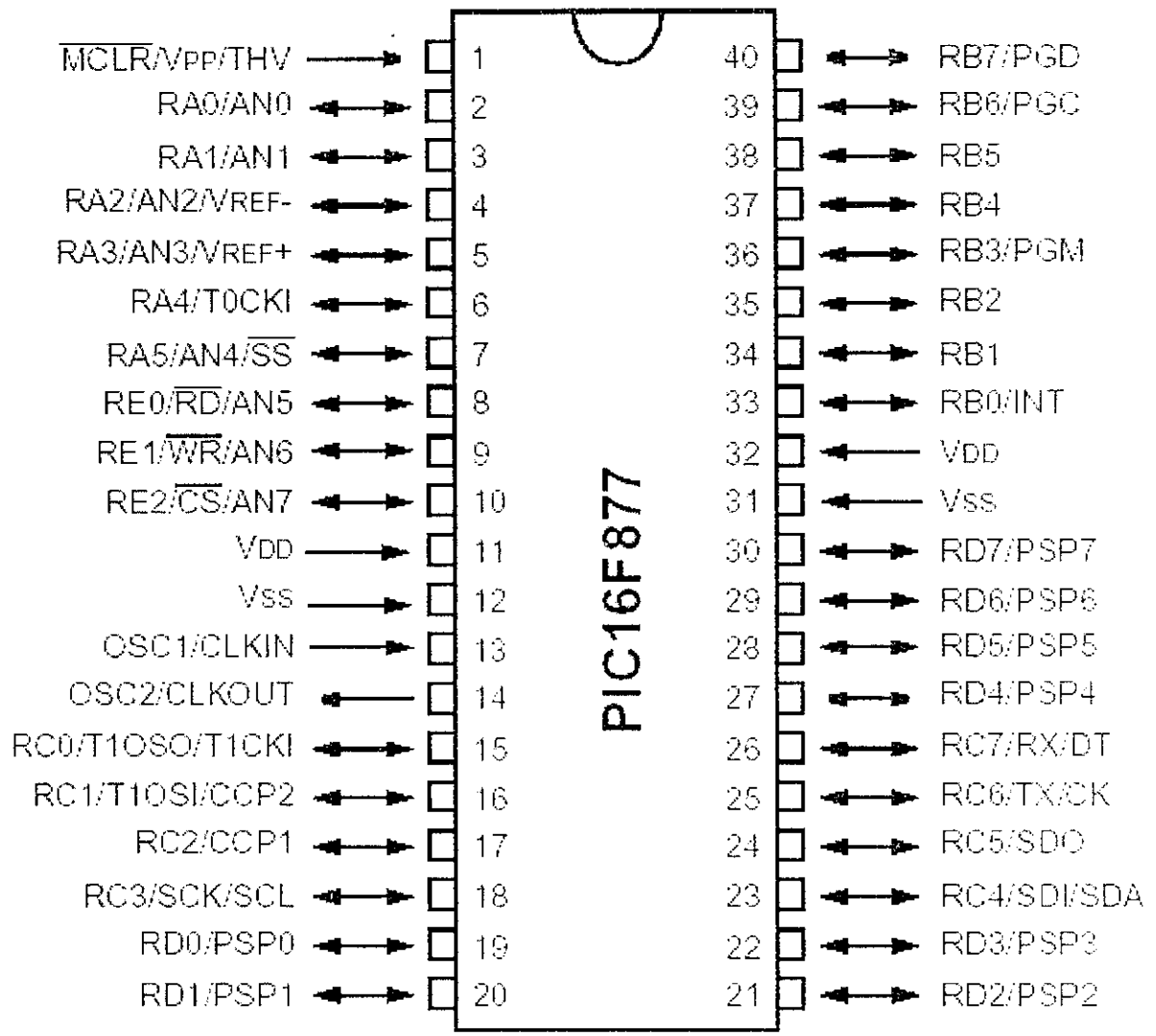


Fig 7.11 Pin diagram of PIC 16F877A

I/O PORTS:

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

MEMORY ORGANISATION:

There are three memory blocks in each of the PIC16F877 MUC's. The program memory and Data Memory have separate buses so that concurrent access can occur.

PROGRAM MEMORY ORGANISATION:

The PIC16f877 devices have a 13-bit program counter capable of addressing 8K *14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

DATA MEMORY ORGANISTION:

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the special functions Registers. Bits RP1 (STATUS<6) and RP0 (STATUS<5>) are the bank selected bits.

RP1:RP0	Banks
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (1238 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some frequently used special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

ANALOG TO DIGITAL CONVERTER (ADC)

There are two types of analog to digital converter is present in this IC. We use 10-bit ADC. The ADC module can have up to eight analog inputs for a device. The analog input charges a sample and hold capacitor. The output of sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation. The A/D conversion of the analog input signal results in a

Corresponding 10-bit digital number. The A/D module has high and low voltage reference input that is software selectable to some combination of VDD, VSS, and RA2 Or RA3.

The A/D module has four registers. These registers are

A/D result high register (ADRESH)

A/D RESULT LOW REGISTER (ADRESL)

A/D CONTROL REGISTER 0 (ADCON0)

A/D CONTROL REGISTER 1 (ADCON1)

CHAPTER 8

CONCLUSION

8.1 POWER QUALITY IMPROVEMENT

The current harmonics in the power utility systems cause various quality problems like low power factor, overheating of electrical equipments, reduction in efficiency, false tripping of CB without fault currents. By this project a methodology is developed to compensate the harmonics present in the current waveform and bring current in phase with the voltage thus rectifying the effect of harmonics on source side.

The simulink model performs the instantaneous reactive power theorem algorithm to extract the reference waveform. The size of the coupling inductor should be compromised between the dynamic response of the filter and the switching ripples. From the simulation we obtained nearly sinusoidal source current waveform with THD **21.35% improved to 4.41%** which conforms to the **IEEE (519-1992)** standards which specifies acceptable levels of harmonics in power systems.

A prototype is then developed using a PIC microcontroller and an H-Bridge mosfet inverter acting as the shunt filter. Injection of compensation current is done through a coupling transformer into the supply–load system and the waveforms obtained on a CRO.

8.2 FUTURE SCOPE :

The future scope of the project involves the implementation of the p-q theory algorithm using advanced and sophisticated digital controllers like Digital Signal Processors. Digital Signal Processors are well suited for this implementation with their high sampling and processing speeds and better immunity to external interferences. Still researches are made on DSP implementation to bring better results than existing and mainly to figure out a cost effective method. More advanced techniques using Artificial Neural Networks and Wavelet technologies are still under research. These methods prove to bring far better results in near future.

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APPENDIX

A.1 HARMONIC LIMITATION

IEEE 519-1992

Sets limits for harmonic voltage and currents at the Point of Common Coupling (PCC). It places responsibility on large commercial and industrial consumers.

Voltage Distortion Limits		
Bus Voltage at PCC	**Individual voltage distortion [%]***	**Total voltage distortion [%]**
below 69kV	3.0	5.0
69kV to 138kV	1.5	2.5
Above 138kV	1.0	1.5

* maximum for individual harmonic

Current Distortion Limits						
Maximum odd harmonic current distortion in percent of I_L for general distribution systems (120V – 69kV)						
I_{SC}/I_L	<11	11≤n<17	17≤n<23	23≤n<35	35≤n	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

I_{SC} - maximum short circuit current at the PCC

I_L - fundamental of the average (over 12 months) maximum monthly demand load current at PCC

TDD – total demand distortion. harmonic current distortion in % of maximum demand load current (15 or 30 minute demand)

IEC 61000-3-2 (IEC 1000-3-2)

It is addresses for small customer equipment. Emphasis on *public, low-voltage and household.*

IEC 1000-3-2 Limits for Class D Equipment		
Harmonic order	**Maximum permissible harmonic current per watt**	**Maximum permissible harmonic current**
N	mA/W	A
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13≤n≤39 (odd har. only)	3.85/n	Refer to class A

IEC 61000-3-4 (IEC 1000-3-4)

It's addresses for larger customers (single and three-phase harmonic limits). It gives a consideration of the short circuit ratio R_{SCC}.

IEC 1000-3-4 limits for three-phase equipment						
Minimal R_{SCC}	**Upper limits for harmonic distortion factors**		**Limits for individual harmonic in % of I_1**			
	THD	*PWHD*	I_5	I_7	I_{11}	I_{13}
66	17	22	12	10	9	6
120	18	29	15	12	12	8
175	25	33	20	14	12	8
250	35	39	30	20	13	9
350	48	46	40	25	15	10
450	58	51	50	35	20	15
>600	70	57	60	40	25	18

A.2 MEASURES OF HARMONIC DISTORTION

A distorted periodic current or voltage waveform expanded into a Fourier series expressed as follows.

$$i(t) = \sum_{h=1}^{\infty} I_h \cos\left(h\omega_0 t + \phi_h\right) \qquad \text{(A 1.1)}$$

$$v(t) = \sum_{h=1}^{\infty} V_h \cos\left(h\omega_0 t + \theta_h\right) \qquad \text{(A 1.2)}$$

Where

I_h is the h th harmonic peak current

V_h is the h th harmonic peak voltage

ϕ_h is the h th harmonic current phase

ω_0 is the fundamental angular frequency

A.2.1 Rms Voltage And Rms Current

The expressions for rms voltage and rms current are given by.

$$V_{rms} = \sqrt{\sum_{h=1}^{\infty} V_{hrms}^2} \qquad \text{(A.1.3)}$$

$$I_{rms} = \sqrt{\sum_{h=1}^{\infty} I_{hrms}^2} \qquad \text{(A 1.4)}$$

Where,

V_{hrms} is the rms harmonic voltage

I_{hrms} is the rms harmonic current

A.2.2 VOLTAGE AND CURRENT DISTORTION FACTORS

Voltage distortion factor or voltage total harmonic distortion is defined as

$$THD_v = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty} V_h^2} = \sqrt{(V_{rms}/V_{1rms})^2 - 1} \qquad (A\ 1.5)$$

Current distortion factor or current total harmonic distortion is defined as

$$THD_I = \frac{1}{I_1}\sqrt{\sum_{h=2}^{\infty} I_h^2} = \sqrt{(I_{rms}/I_{1rms})^2 - 1} \qquad (A\ 1.6)$$

Where V_1 and I_1 represent the fundamental peak voltage and peak current respectively.

A.3 MICROCONTROLLER CODE

```
#include<pic.h>

#include<lcd.h>


void Adc_Tmr_Init(void);

void adc0(void);


static bit input   @((unsigned) &PORTC*8+0);

static bit output1 @((unsigned) &PORTB*8+0);

static bit output2 @((unsigned) &PORTB*8+1);

static bit output3 @((unsigned) &PORTB*8+2);

static bit output4 @((unsigned) &PORTB*8+3);


unsigned int count,val,count1,a1;

//unsigned char val;
```

```
bit a,b;

void main()
{
TRISC=0x01;
TRISB=0x00;
output1=output2=output3=output4=0;

lcd_init();
//Adc_Tmr_Init();

command(0x80);
lcd_condis("  50Hz Sine.W.  ",16);
command(0xc0);
lcd_condis("with Sqre Pulse.",16);
delay(50000);

while(!input);
while(input);
a=0;
//TMR1ON=1;
while(1)
{
adc0();
```

```
//command(0xc0);
//hex_dec1(val);
if(val>40)
{
if(input && !a)
{
output3=output2=0;
 delay(50);
a=1;
output1=output4=1;
}
if(!input && a)
{
output1=output4=0;
 delay(50);
a=0;
output2=output3=1;
}


}
else output4=output1=output3=output2=0;
}
}
```

```
void Adc_Tmr_Init()
{
 ADCON1=0x02;          // 8-channel, Left justified, ADC control
 TRISA=0xff;           // to select the port A as input port

  GIE=1;
  PEIE=1;
  TMR1IE=1;
  TMR1L=0x05;
  TMR1H=0xff;
  T1CON=0x80;
  TMR1ON=0;
}

void interrupt FUNCTION(void)
{
}

void adc0()
{
//val=0;
//for (j=0; j<10; j++)
{
```

```
    ADCON0=0x01;        // Channel select (Cha: 0)
//    ADON=1;             // ADC module ON
    delay(1);
    ADCON0 =0x05;         // selecting a particular channel and making the go/done bit high
    while(ADCON0!=0X01);  // Chk whether conversion finished or not
   val = ADRESH;      // 8 bit value taken into one variable
}
//val= val*2;
//if(val>250) val=250;
//temp1=val;
}
```

A.4 DATA SHEETS

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS14
Hex Inverter with Schmitt Trigger Inputs

General Description

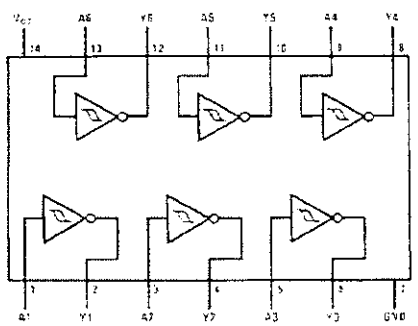
This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output

Ordering Code:

Order Number	Package Number	Package Description
DM74LS14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

 DS006353

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.5	0.8	1	V
HYS	Input Hysteresis (Note 2)	0.4	0.8		V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Note 2: V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		V_{CC} = Min, I_{OL} = 4 mA		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}		−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}		−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		6.6	16	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		12	21	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

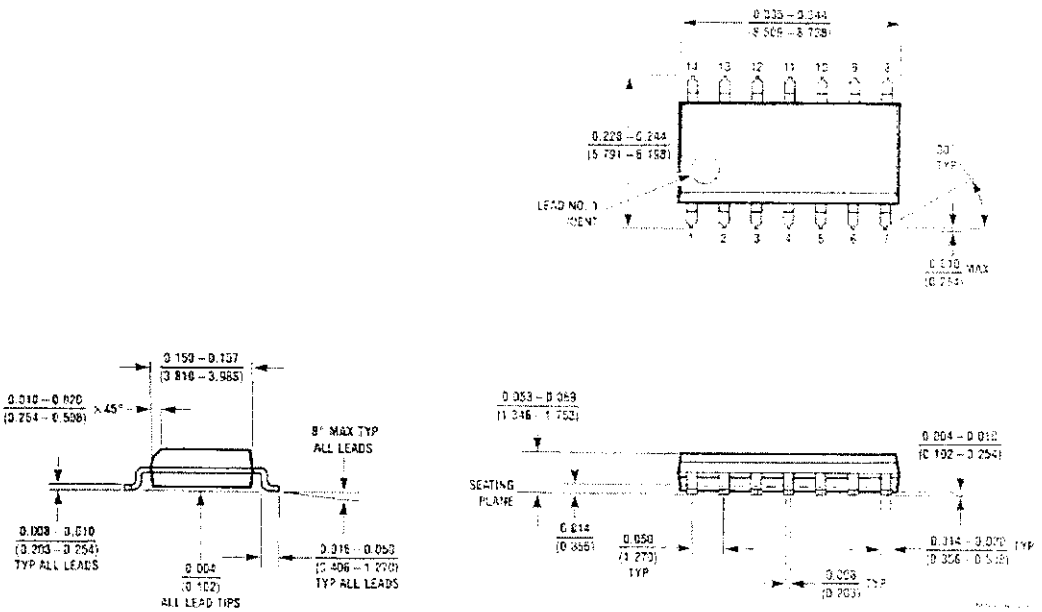
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

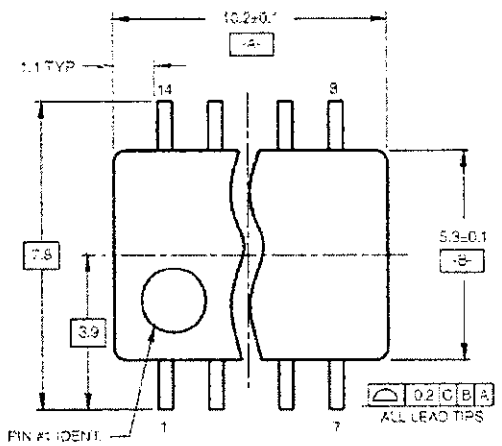
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	9	22	9	26	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	9	22	10	33	ns

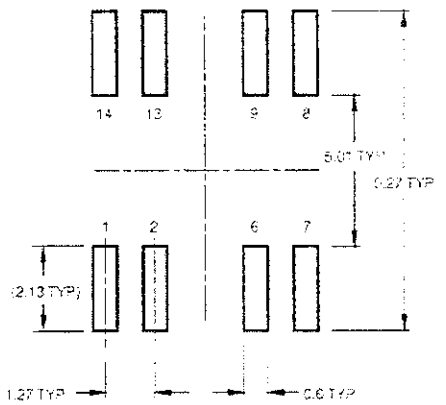
Physical Dimensions inches (millimeters) unless otherwise noted



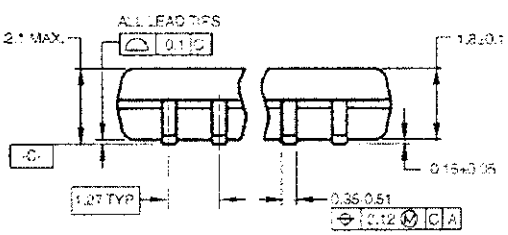
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

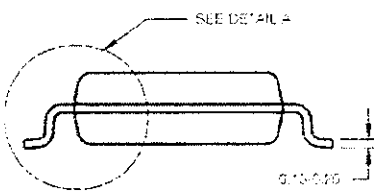




LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



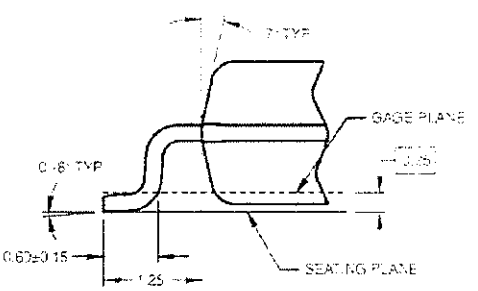
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

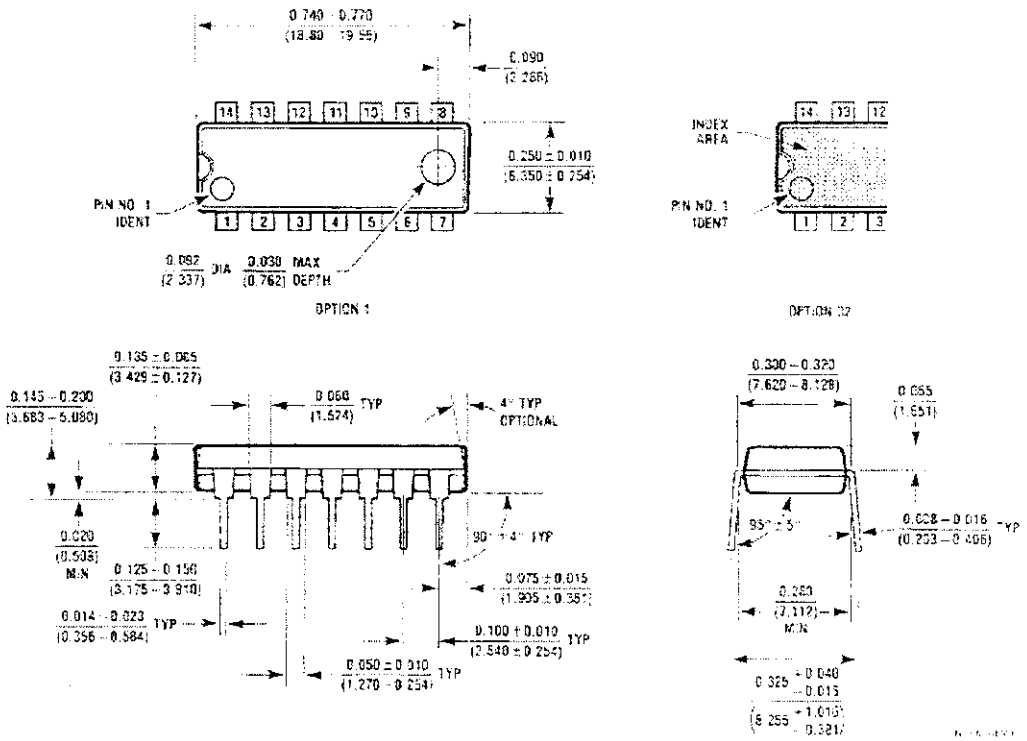
M14DRevB1



DETAIL A

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

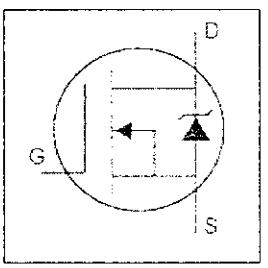
International
IOR Rectifier

PD - 9.4008

IRFP250N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 200V

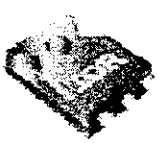
$R_{DS(on)}$ = 0.075Ω

I_D = 30A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	30	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	21	
I_{DM}	Pulsed Drain Current ①	120	
P_D @T_C = 25°C	Power Dissipation	214	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	315	mJ
I_{AR}	Avalanche Current①	30	A
E_{AR}	Repetitive Avalanche Energy①	21	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.6	V/ns
T_J	Operating Junction and	-55 to +175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.075	Ω	V_{GS} = 10V, I_D = 18A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	17	—	—	S	V_{DS} = 50V, I_D = 18A ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	123	nC	I_D = 18A
Q_{gs}	Gate-to-Source Charge	—	—	21		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	57		V_{GS} = 10V, See Fig. 6 and 13 ③
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 100V
t_r	Rise Time	—	43	—		I_D = 18A
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		R_G = 3.9Ω
t_f	Fall Time	—	33	—		R_D = 5.5Ω, See Fig. 10 ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2159	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	315	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	83	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	120		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 18A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	186	279	ns	T_J = 25°C, I_F = 18A
Q_{rr}	Reverse Recovery Charge	—	1.3	2.0	µC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglig ble (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 1.9mH R_G = 25Ω, I_{AS} = 18A. (See Figure 12)

③ I_{SD} ≤ 18A, di/dt ≤ 374A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%

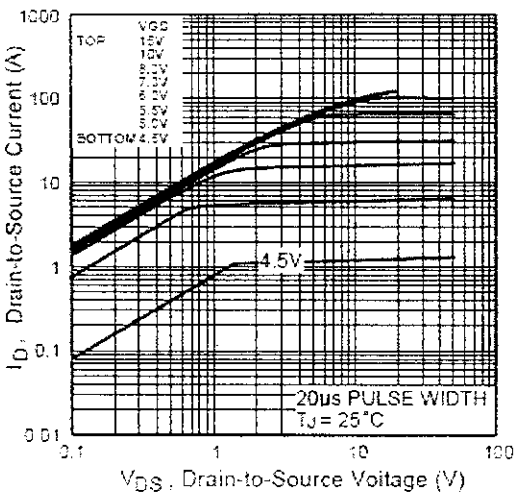


Fig 1. Typical Output Characteristics

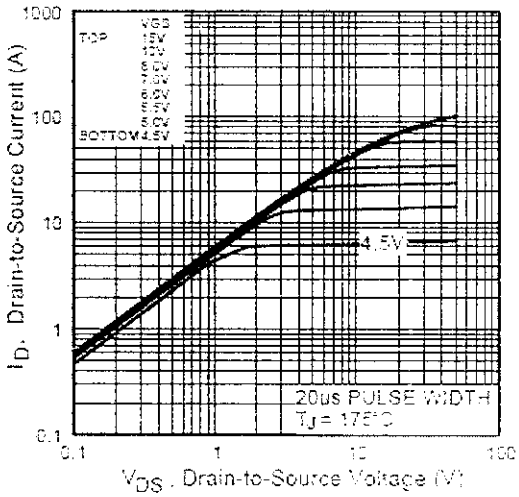


Fig 2. Typical Output Characteristics

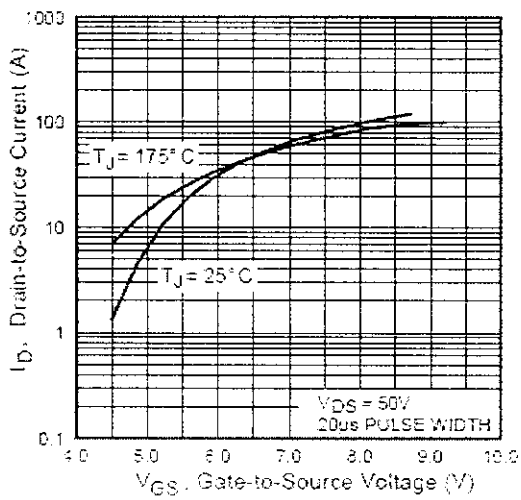


Fig 3. Typical Transfer Characteristics

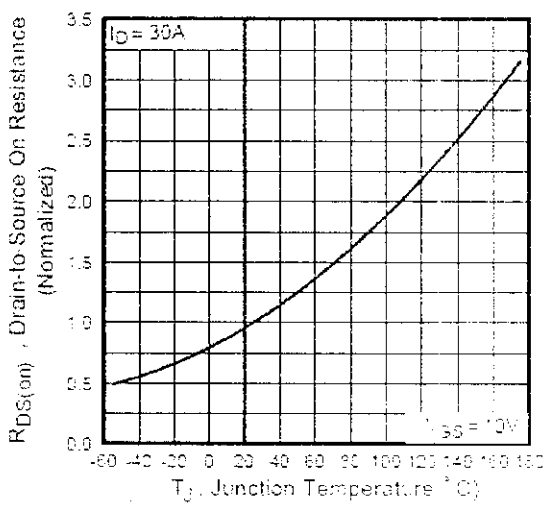
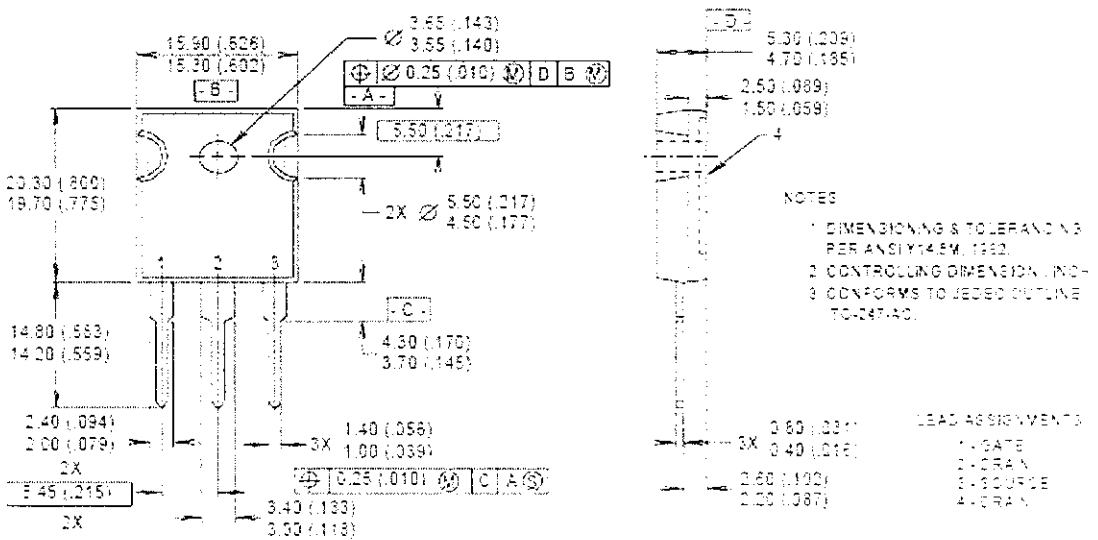


Fig 4. Normalized On-Resistance
Vs. Temperature

Package Outline

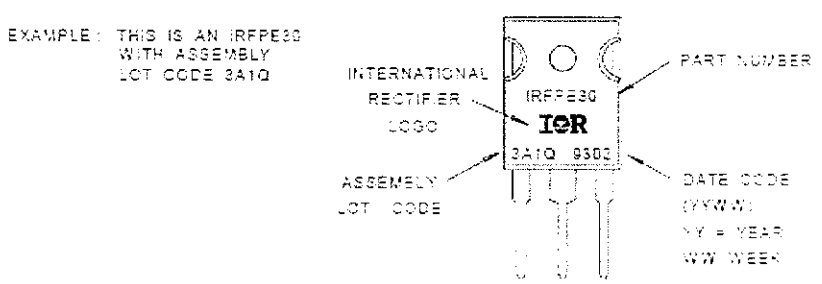
TO-247AC Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-247AC



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IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 0BL, UK Tel: +44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: +49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: +39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: +65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Hwa South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

FAIRCHILD
SEMICONDUCTOR®

March 2009

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

Block Diagram

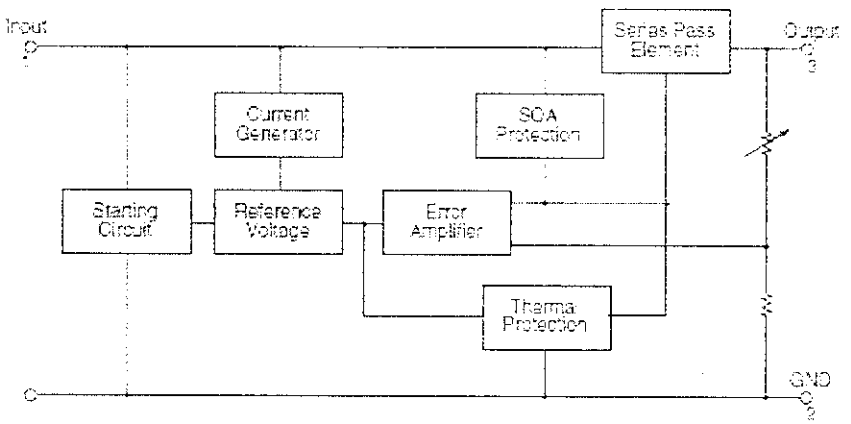

Figure 1.

Pin Assignment

Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM79xx	-40 to +125	°C
		LM79xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (LM7809) (Continued)

Refer to the test circuits. $-40°C < T_J < 125°C$, $I_O = 500mA$, $V_I = 18V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	$T_J = +25°C$		8.65	9.0	9.35	V
		$5mA \le I_O \le 1A$, $P_O \le 15W$, $V_I = 11.5V$ to 24V		8.6	9.0	9.4	
Regline	Line Regulation[7]	$T_J = +25°C$	$V_I = 11.5V$ to 25V	–	6.0	180	mV
			$V_I = 12V$ to 17V	–	2.0	90.0	
Regload	Load Regulation[7]	$T_J = +25°C$	$I_O = 5mA$ to 1.5A	–	12.0	180	mV
			$I_O = 250mA$ to 750mA	–	4.0	90.0	
I_Q	Quiescent Current	$T_J = +25°C$		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	$I_O = 5mA$ to 1A		–	–	0.5	mA
		$V_I = 11.5V$ to 26V		–	–	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift[8]	$I_O = 5mA$		–	-1.0	–	mV/°C
V_N	Output Noise Voltage	$f = 10Hz$ to 100kHz, $T_A = +25°C$		–	58.0	–	$\mu V/V_O$
RR	Ripple Rejection[8]	$f = 120Hz$, $V_O = 13V$ to 23V		56.0	71.0	–	dB
V_{DROP}	Dropout Voltage	$I_O = 1A$, $T_J = +25°C$		–	2.0	–	V
r_O	Output Resistance[8]	$f = 1kHz$		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	$V_I = 35V$, $T_A = +25°C$		–	350	–	mA
I_{PK}	Peak Current[8]	$T_J = +25°C$		–	2.2	–	A

Notes:

7. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
8. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7812) (Continued)

Refer to the test circuits. $-40°C < T_J < 125°C$, $I_O = 500mA$, $V_I = 19V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$ unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	$T_J = +25°C$		11.5	12.0	12.5	V
		$5mA \le I_O \le 1A$, $P_O \le 15W$, $V_I = 14.5V$ to $27V$		11.4	12.0	12.6	
Regline	Line Regulation[11]	$T_J = +25°C$	$V_I = 14.5V$ to $30V$	–	10.0	240	mV
			$V_I = 16V$ to $22V$	–	3.0	120	
Regload	Load Regulation[11]	$T_J = +25°C$	$I_O = 5mA$ to $1.5A$	–	11.0	240	mV
			$I_O = 250mA$ to $750mA$	–	5.0	120	
I_Q	Quiescent Current	$T_J = +25°C$		–	5.1	8.0	mA
ΔI_Q	Quiescent Current Change	$I_O = 5mA$ to $1A$		–	0.1	0.5	mA
		$V_I = 14.5V$ to $30V$		–	0.5	1.0	
$\Delta V_O/\Delta T$	Output Voltage Drift[12]	$I_O = 5mA$		–	-1.0	–	mV/°C
V_N	Output Noise Voltage	$f = 10Hz$ to $100kHz$, $T_A = +25°C$		–	76.0	–	$\mu V/V_O$
RR	Ripple Rejection[12]	$f = 120Hz$, $V_I = 15V$ to $25V$		55.0	71.0	–	dB
V_{DROP}	Dropout Voltage	$I_O = 1A$, $T_J = +25°C$		–	2.0	–	V
r_O	Output Resistance[12]	$f = 1kHz$		–	18.0	–	mΩ
I_{SC}	Short Circuit Current	$V_I = 35V$, $T_A = +25°C$		–	230	–	mA
I_{PK}	Peak Current[12]	$T_J = +25°C$		–	2.2	–	A

Notes:

11. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

12. These parameters, although guaranteed, are not 100% tested in production.