DESIGN AND IMPLEMENTATION OF A SOFT SWITCHING SINGLE PHASE THREE-LEVEL RECTIFIER

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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ABSTRACT

This project is concerned with the design and implementation of a single phase boost-type three-level rectifier. The converter is supposed to present high input power factor, low current harmonics, low total harmonic distortion, and simple control scheme. In order to minimize switching losses, a passive non dissipative snubber is associated with the aforementioned converter. Multi-level rectifiers are the modification of bridge rectifiers. They are normally connected in series to form stacks of levels. The multi-level circuits are used to generate multiple voltage levels. The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occur in series-connected devices. Each level voltage is equal in magnitude and thus can be used to supply the balanced loads.

The boost-type converter switch is a MOSFET switch and this switch has a capacitor connected across it in parallel. This capacitor charges and discharges continuously there by enabling zero voltage across it for zero voltage switching. The zero voltage switching technique is referred to as soft switching technique which is capable of minimizing the switching losses to a great extent. In this, the PIC or the triggering unit is programmed in such a way that it closes the switch at the zero voltage instant by sending the gate pulse and thus reduces the switching losses. The pulse width of the gate pulse can be changed by varying the potentiometer and this in turn brings about corresponding changes in the output voltage and the speed of the motor.

ACKNOWLEDGEMENT

The completion of this project can be attributed to the combined efforts made by us and the contribution made in one form or the other by the individuals we hereby acknowledge.

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LIST OF ABBREVIATIONS AND NOMENCLATURE

Abbreviations

ZVS	-	Zero Voltage Switching
ZCS	-	Zero Current Switching
CCM	-	Continuous Conduction Mode
EMI	-	Electro Magnetic Interference
PFC	-	Power Factor Control
PIC	-	Programmable Interface Controller/Peripheral Interrupt Controller

Nomenclature

Symbol	Expansion
V_i	input voltage
f	grid frequency
f_s	switching frequency
V_{o1}, V_{o2}, V_o	output voltages
P_o	output power
?	efficiency
? V_o	output voltage ripple
? $I_{lb(max)}$	Maximum input current ripple
L_b	Boost inductor
C_{o1},C_{o2}	Output capacitors
S_1,S_2	Switches
D_{b1},D_{b2}	Boost diodes
L_s	Snubber inductor
C_{b1},C_{b2}	Buffer capacitors
C_{s1},C_{s2}	Snubber capacitors
D_{a11}, D_{a12}, D_{a13}, D_{a21}, D_{a22}, D_{a23}	Snubber diodes

CHAPTER 1

1. INTRODUCTION

1.1 OBJECTIVE OF THE PROJECT

The main objective of our project is to enable the converter to present high input power factor, low current harmonics, low total harmonic distortion and simple control scheme. This project also aims at reducing the switching losses by using a passive non dissipative snubber which employs zero voltage switching technique. Moreover, the circuit can supply balanced loads without any voltage transients using the multi level concept.

Simulation is an effective tool by which we can experience the practical results through the software. There are a number of simulation softwares available and the most efficient tool is MATLAB. Hence, the simulink part of the matlab is employed in this project.

1.2 OUTLINE OF THE REPORT

Chapter 1 explains the main objectives of the project.

Chapter 2 gives a brief idea about the multi-level concept, its advantages and the overall block diagram of the project with its functional units.

Chapter 3 describes the various switching techniques that are existing, the advantages of soft switching over hard switching and its application.

Chapter 4 gives the complete architecture and features of the PIC 16F877A which is the triggering unit for the switch.

Chapter 5 describes the various classifications of the converters, the comparison between them, MOSFET switch and its structure.

Chapter 6 gives the operation of driver circuit and its components.

Chapter 7 projects the need for employing MATLAB simulation and provides a discussion on the simulated results.

Chapter 8 explains the hardware implementation and interpreted results.

Chapter 9 provides the conclusion, scope and applications of the project.

Appendix I has the source code used in PIC.

Appendix II contains the data sheets of various components used in the project.

CHAPTER 2

2. THREE LEVEL RECTIFIER

2.1 MULTI - LEVEL CONCEPT

Recent advances in power electronics have made the multi level concept practical. Infact the concept is so advantageous that several major drives manufacturers have obtained recent patents on multi level power converters and associated switching techniques. It is evident that the multi level concept will be a prominent choice for power electronic systems in future years, especially for medium voltage operation. Multi-level rectifiers are the modification of bridge rectifiers. They are normally connected in series to form stacks of levels.

The topological structure of multi-level rectifier must cope with the following points:

It should have less switching devices as far as possible.

- ❖ It should be capable of enduring very high input voltage in case of high power applications.
- ❖ Each switching device should have low switching frequencies owing to multi-level approach.

There are various multi-level concepts used for various applications. The multi-level circuits are used to generate multiple voltage levels.

2.2 ADVANTAGES OF MULTILEVEL RECTIFIERS

In general multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- ❖ The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occur in series-connected devices.
- ❖ Spectral performance of multilevel waveforms is superior to that of their two level counter parts.
- ❖ Multilevel waveforms naturally limit the problems of large voltage transients that occur due to the reflections on cables, which can damage the motor windings and cause other problems.

2.3 OVERALL BLOCK DIAGRAM:

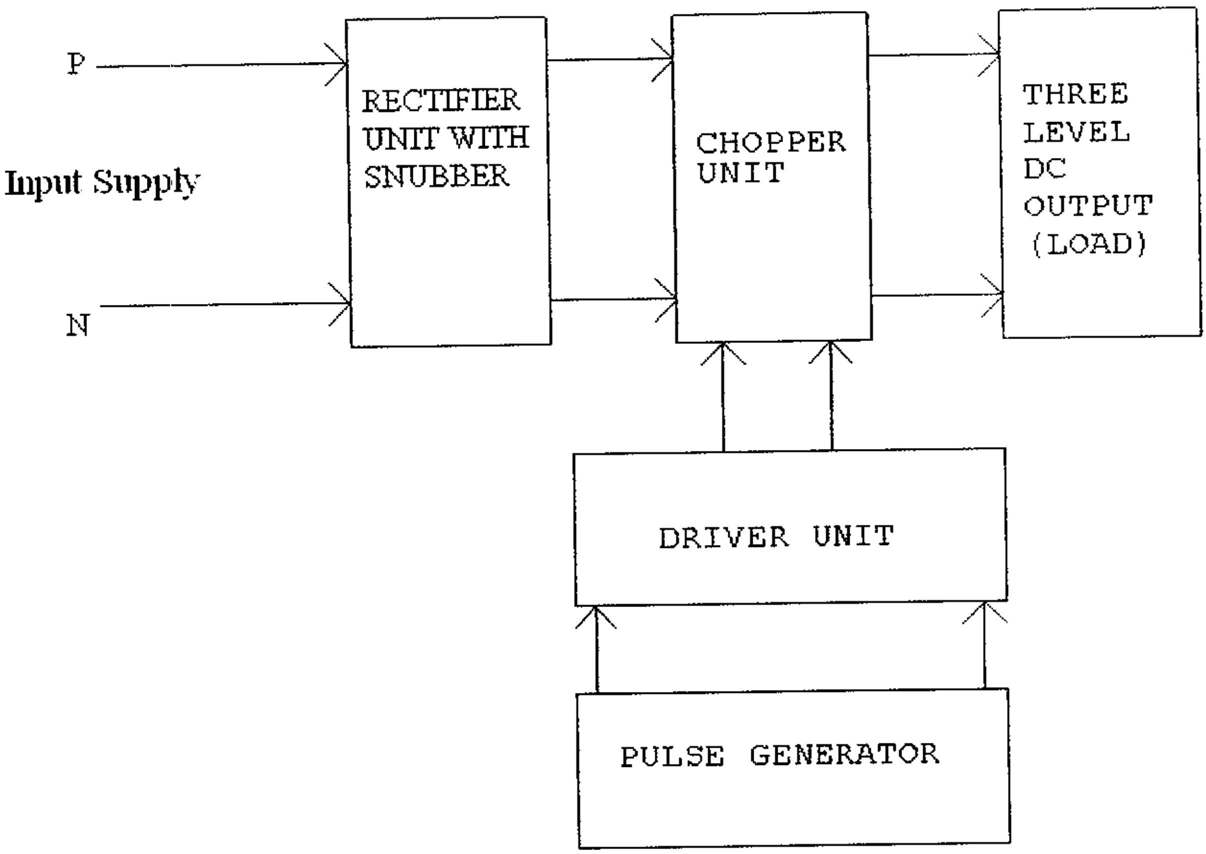


Fig. 2.1 Overall block diagram

This block diagram gives an overview of the various functional units of the project namely

- Rectifier and Snubber unit

  This unit has the snubber circuit followed by the rectifier. Rectifier unit has 3 diodes for each level and these diodes are used to convert the input ac supply into dc. Snubber circuit possesses capacitors and inductors to enable soft switching of diodes as well.

- Chopper unit

  Chopper unit has a MOSFET switch which converts the dc voltage to a voltage of desirable level by zero voltage switching technique. The chopper used is a boost-type chopper.

- Driver unit

  Driver unit is used to amplify the pulse from the microcontroller to the MOSFET s gate. It has transistors connected in totem pole fashion.

- Triggering unit

  Triggering unit has a PIC microcontroller used to generate gate pulses for closing the MOSFET switch.

CHAPTER 3

3. SOFT SWITCHING TECHNIQUE

3.1. INTRODUCTION

The boost converter topology has been extensively used in various ac/dc and dc/dc applications. In fact, the front end of today's ac/dc power supplies with power-factor correction (PFC) is almost exclusively implemented with boost topology. Also, the boost topology is used in numerous applications with battery-powered input to generate a high output voltage from a relatively low battery voltage. At higher power levels, the continuous-conduction-mode (CCM) boost converter is the preferred mode of operation for the implementation of a front end with PFC. As a result, in recent years, significant effort has been made to improve the performance of high-power boost converters. Generally, the reduction of reverse-recovery-related losses require that the boost rectifier is "softly" switched off, which can be achieved by controlling the turn-off rate of its current. There are two types of switching techniques

i) Hard switching technique and

ii) Soft switching technique.

3.2 SOFT SWITCHING TECHNIQUES

3.2.1 CLASSIFICATION

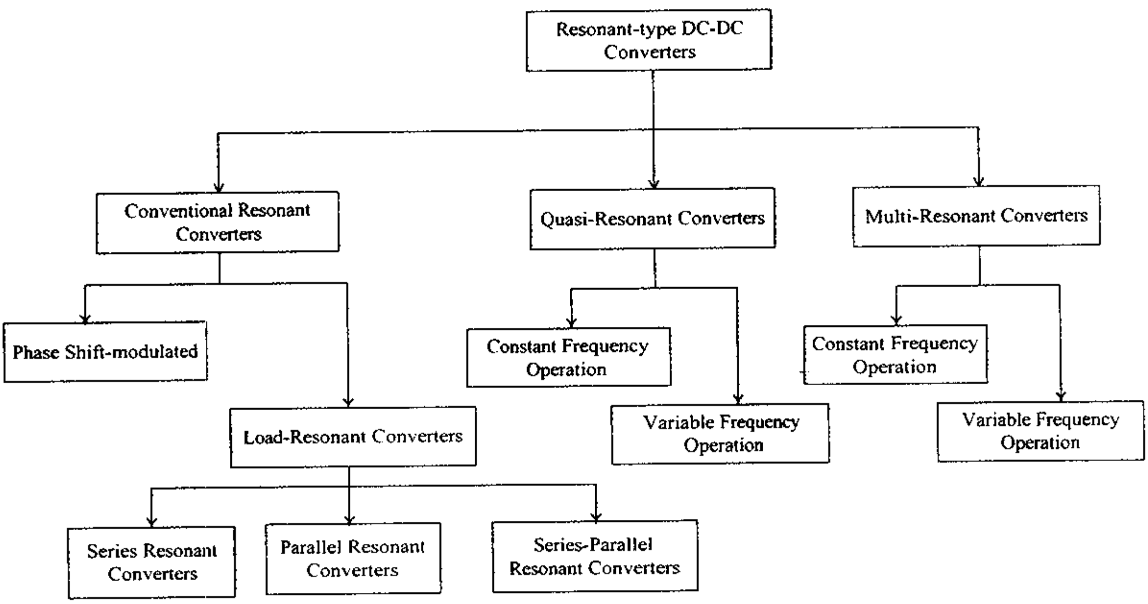
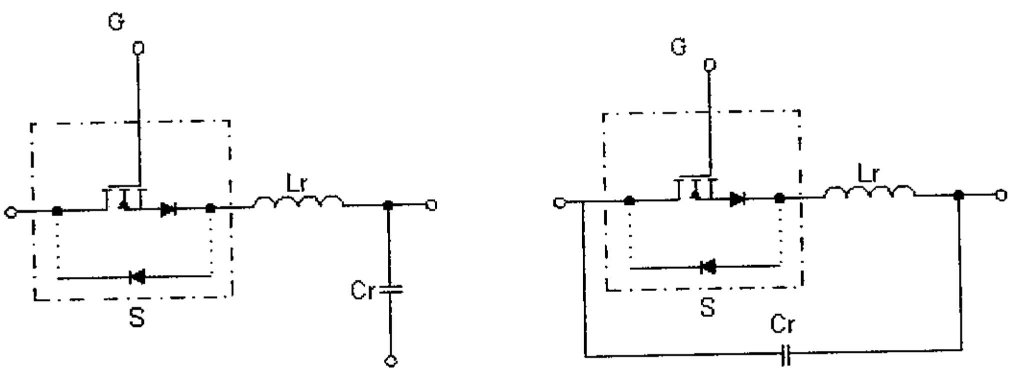


Fig 3.1 Classification of Converters.

3.2.2 RESONANT SWITCHES

ZERO CURRENT (ZC) RESONANT SWITCH

In a Zero Current resonant switch, an inductor L_r is connected in series with a power switch S in order to achieve zero-current-switching (ZCS). If the switch S is a unidirectional switch, the switch current is allowed to resonate in the positive half cycle only. The resonant switch is said to operate in *half-wave* mode. If a diode is connected in anti-parallel with the unidirectional switch, the switch current can flow in both directions. In this case, the resonant switch can operate in *full-wave* mode. At turn-on, the switch current will rise slowly from zero. It will then oscillate, because of the resonance between L_r and C_r. Finally, the switch can be commutated at the next zero current duration. The objective of this type of switch is to shape the switch current waveform during conduction time in order to create a zero-current condition for the switch to turn off.



(a) (b)

Fig.3.2 Zero-current (ZC) resonant switch.

ZERO VOLTAGE (ZV) RESONANT SWITCH

In a Zero Voltage resonant switch, a capacitor C_r is connected in parallel with the switch S for achieving zero-voltage-switching (ZVS). If the switch S is a unidirectional switch, the voltage across the capacitor C_r can oscillate freely in both positive and negative half-cycle. Thus, the resonant switch can operate in *full-wave* mode. If a diode is connected in anti-parallel with the unidirectional switch, the resonant capacitor voltage is clamped by the diode to zero during the negative half-cycle. The resonant switch will then operate in *half-wave* mode. The objective of a ZV switch is to use the resonant circuit to shape the switch voltage waveform during the off time in order to create a zero-voltage condition for the switch to turn on.

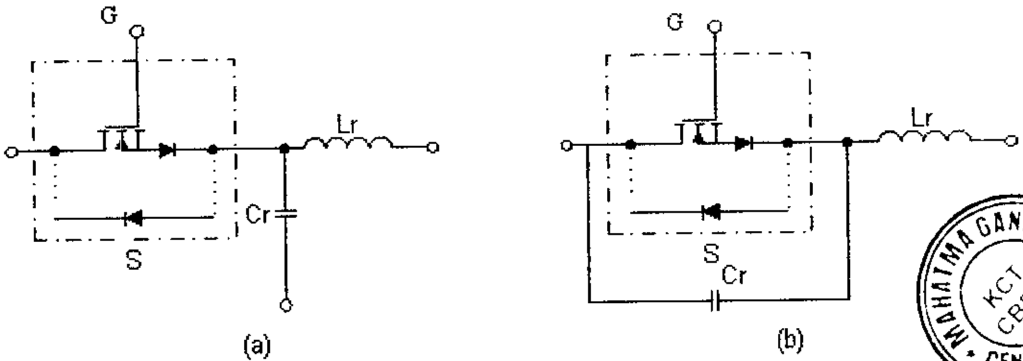


Fig.2.3 Zero-voltage (ZV) resonant switch.

3.2.3 COMPARISON BETWEEN ZCS AND ZVS

ZCS can eliminate the switching losses at turn-off and reduce the switching losses at turn-on. As a relatively large capacitor is connected across the output diode during resonance, the converter operation becomes insensitive to the diode's junction capacitance. The major limitations associated with ZCS when power mosfets are used are the capacitive turn-on losses. Thus, the switching loss is proportional to the switching frequency. During turn-on, considerable rate of change of voltage can be coupled to the gate drive circuit through the Miller capacitor, thus increasing switching loss and noise. Another limitation is that the switches are under high current stress, resulting in high conduction loss. It should be noted that ZCS is particularly effective in reducing switching loss for power devices (such as IGBT) with large tail current in the turn-off process. ZVS eliminates the capacitive turn-on loss. It is suitable for high-frequency operation. For single-ended configuration, the switches could suffer from excessive voltage stress, which is proportional to the load. For both ZCS and ZVS, output regulation of the resonant converters can be achieved by variable frequency control. ZCS operates with constant on-time control, while ZVS operates with constant off-time control. With a wide input and load range, both techniques have to operate with a wide switching frequency range, making it not easy to design resonant converters optimally.

3.3. ADVANTAGES AND APPLICATIONS OF SOFT SWITCHING:

ADVANTAGES

Advances in soft switching converters have set new benchmarks in performance and cost in power converter technology, and have shown promise in overcoming the limitations of conventional hard switching technology. Resonant dc link inverters have been realized at power ratings of 200 kVA in single modules. The use of zero voltage switching with MOSFET power devices demonstrates of some aggressive benchmarks when compared with conventional technology. These include:

- 100% power device utilization
- Low EMI which meet Mil-specs
- Enhanced robustness.
- High power densities
- High switching frequencies
- High efficiencies

APPLICATIONS:

- Traction motors
- Industrial SMPS systems
- Aircraft Power supplies
- Industrial Oven Controls
- High frequency applications.

CHAPTER 4

4. TRIGGERING UNIT

4.1. INTRODUCTION:

PIC 16F877A is used for producing switching pulses to multilevel rectifier, so as to use those vectors which do not generate any common mode voltage at the rectifier poles. This eliminates common mode voltage. Also it is used to eliminate capacitor voltage unbalancing. The microcontroller are driven via the driver circuit so as to boost the voltage triggering signal to 9V.To avoid any damage to micro controller due to direct passing of 230V supply to it we provide an isolator in the form of optocoupler in the same driver circuit.

4.2 PIC MICROCONTROLLER

4.2.1 TRIGGERING OPERATION

In this project, the PIC 16F877A is used to produce gate signal to trigger the switch. The programmable interface controller evaluation board receives 12 volts from a 230/12 volts step down transformer and this ac voltage is converted to dc voltage using a bridge rectifier. Constant 5 volts dc supply is maintained for the controller input using a voltage regulator. This constant dc voltage is fed to the controller through the input port B. The output gate pulse is obtained from port C which is fed to the driver unit for amplification. The amplified gate pulse from the driver unit triggers the MOSFET.

4.2.2 FEATURES

1. High-Performance RISC CPU:

- Only 35 single- word instructions to learn .Hence it is user friendly. Easy to use
- All single - cycle instructions except for program branches, which are two-cycle
- Operating speed: DC – 20 MHz clock input DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM Data Memory. It is huge one

2. Peripheral Features:

- Timer0: 8-bit timer/counter with 8 – bit prescaler. It is used for synchronization
- Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep

• Timer2:8-bit timer/counter with 8-bit period register, prescaler and postscaler

• Two Capture, Compare and some PWM modules, having following features

3. Analog features:

(1) Two analog comparators

(2) Programmable on-chip voltage reference (VREF) module

4.2.3 PIN DIAGRAM OF PIC 16F877A

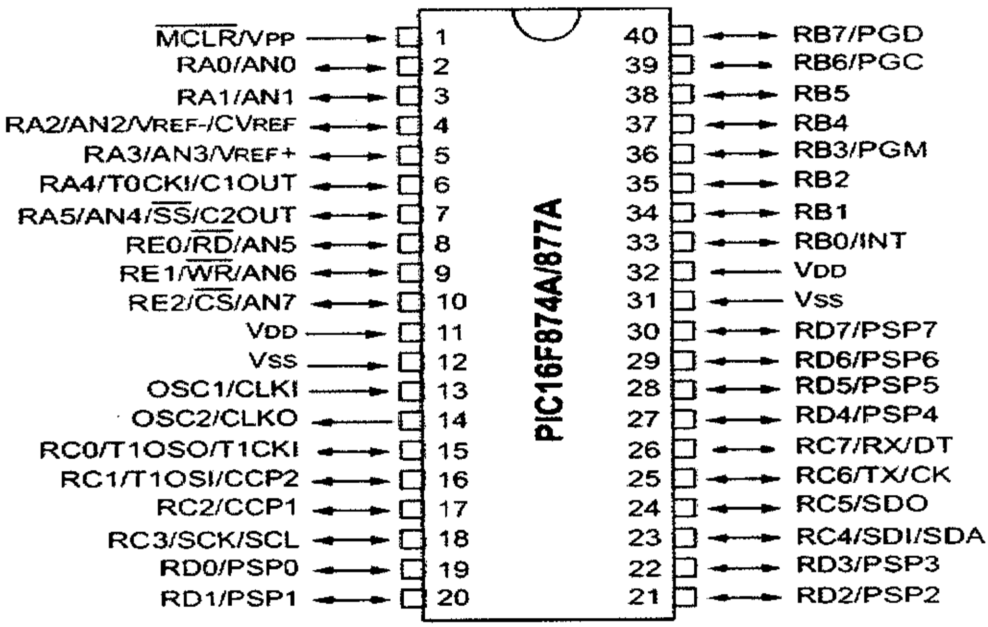


Fig 4.2: Pin diagram of 40 pin dual inline package of PIC 16F877A

PIN DESCRIPTION:

OSC1/CLKI:

Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).

OSC2/CLKO:

Oscillator crystal or clock output. Oscillator crystal output. Connects to the crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.

MCLR/VPP:

Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low Reset to the device. Programming voltage input.

- RA0/AN0.
- RA1/AN1.
- RA2/AN2/VREF-/CVREF.
- VREFCVREF.
- RA3/AN3/VREF+.
- VREF+.
- RA4/T0CKI/C1OUT.
- T0CKI.
- C1OUT.
- RA5/AN4/SS/C2OUT/SS/C2OUT.

I/O PORTS:

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORT A AND THE TRIS A REGISTER:

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High – Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; the value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open-drain output. All other PORTA pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and the analog VREF input for both the A/D converters and the comparators. The operation of each pin is selected by clearing/setting the appropriate control bits in the ADCON1 and/or CMCON registers. The TRISA register controls the direction of the port pins even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

PORT B AND THE TRIS B REGISTER:

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the In-Circuit Debugger and Low-Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD.

Four of the PORTB pins, RB7:RB4, have an interruption- change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interruption- change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB port change interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on- change feature. This interrupt-on-mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression.

PORT C AND THE TRIS C REGISTER:

PORTC is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High- Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). PORTC is multiplexed with several peripheral functions (Table 4-5). PORTC pins have Schmitt Trigger input buffers. When the I2C module is enabled, the PORTC<4:3> pins can be configured with normal I2C levels, or with SMBus levels, by using the CKE bit (SSPSTAT<6>). When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify write instructions (BSF, BCF, XORWF) with TRISC as the destination, should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

PORT D AND TRIS D REGISTERS:

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTD can be configured as an 8-bit wide microprocessor port (Parallel Slave Port) by setting control bit, PSP MODE (TRISE<4>). In this mode, the input buffers are TTL.

PORT E AND TRIS E REGISTER:

PORTE has three pins (RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7) which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers. The PORTE pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make certain that the TRISE<2:0> bits are set and that the pins are configured as digital inputs. Also, ensure that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL. Register 4-1 shows the TRISE register which also controls the Parallel Slave Port operation. PORTE pins are multiplexed with analog inputs.

When selected for analog input, these pins will read as '0's. TRISE controls. The direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

CHAPTER 5

5. BOOST CONVERTER AND MOSFET

5.1. INTRODUCTION

DC to DC converters

In electronics engineering, a DC to DC converter is a circuit which converts a source of direct current from one voltage to another. It is a class of power converter. The purpose of a DC-DC converter is to supply a regulated DC output voltage to a variable-load resistance from a fluctuating DC input voltage. In many cases the DC input voltage is obtained by rectifying a line voltage that is changing in magnitude. DC-DC converters are commonly used in applications requiring regulated DC power, such as computers, medical instrumentation, communication devices, television receivers, and battery chargers. DC-DC converters are also used to provide a regulated variable DC voltage for DC motor speed control applications.

5.2. USAGE

DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, which are supplied with power from batteries. Such electronic devices often contain several sub-circuits with each sub-circuit requiring a unique voltage level different than that supplied by the battery (sometimes higher or lower than the battery voltage, and possibly even negative voltage). Additionally, the battery voltage declines as its stored power is drained. DC to DC converters offer a method of generating multiple controlled voltages from a single variable battery voltage, thereby saving space instead of using multiple batteries to supply different parts of the device.

5.3. Conversion methods

5.3.1 Linear

A simple method of converting one voltage to another is a circuit known as a voltage divider. This technique uses resistors in series with the voltage supply to provide a lower voltage. However, this method suffers serious drawbacks:

* Provides no voltage regulation
* Requires knowledge of the resistance of the load
* Poor efficiency, which also leads to excess heat dissipation
* Impossible to generate voltages higher than the supply voltage
* Impossible to generate negative voltages, unless the system ground is defined by a node in the resistor network.

Any kind of voltage regulator solves the first two problems, however, linear regulators still have the last three problems.

5.3.2 Switched-mode conversion

Electronic switch-mode DC to DC converters are available to convert one DC voltage level to another. These circuits, very similar to a switched-mode power supply, generally perform the conversion by applying a DC voltage across an inductor or transformer for a period of time (usually in the 100 kHz to 5 MHz range) which causes current to flow through it and store energy magnetically, then switching this voltage off and causing the stored energy to be transferred to the voltage output in a controlled manner. By adjusting the ratio of on/off time, the output voltage can be regulated even as the current demand changes. This conversion method is more power efficient (often 80% to 95%) than linear voltage conversion which must dissipate unwanted power. This efficiency is beneficial to increasing the running time of battery operated devices. A drawback to switching converters is the electronic noise they generate at high frequencies, which must sometimes be filtered.

Isolated DC-DC converters convert a DC input power source to a DC output power while maintaining isolation between the input and the output, generally allowing differences in the input-output ground potentials in the range of hundreds or thousands of volts. They can be an exception to the definition of DC-DC converters in that their output voltage is often (but not always) the same as the input voltage. A current-output DC-DC converter accepts a DC power input, and produces as its output a constant current, while the output voltage depends on the impedance of the load.

5.4. CONVERTER CONFIGURATIONS

The various topologies of the DC to DC converter can generate voltages higher, lower, higher and lower or negative of the input voltage; their names are:

* Buck
* Boost
* Buck-boost
* Cuk

5.4.1. BUCK CONVERTER STEP-DOWN CONVERTER

In this circuit the transistor turning ON will put voltage Vin on one end of the inductor. This voltage will tend to cause the inductor current to rise. When the transistor is OFF, the current will continue flowing through the inductor but now flowing through the diode. We initially assume that the current through the inductor does not reach zero, thus the voltage at Vx will now be only the voltage across the conducting diode during the full OFF time. The average voltage at Vx will depend on the average ON time of the transistor provided the inductor current is continuous.

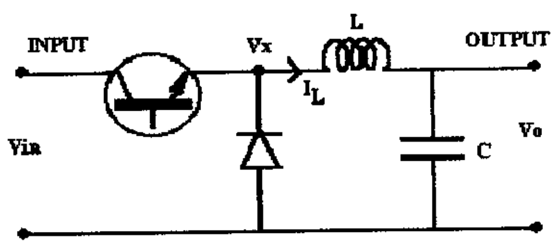


Fig. 5.1: Buck Converter

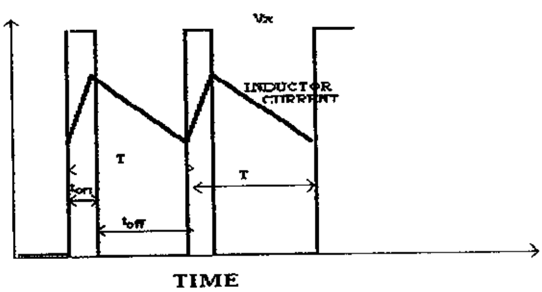


Fig. 5.2: Voltage and current changes

To analyse the voltages of this circuit let us consider the changes in the inductor current over one cycle. From the relation

$$V_x - V_o = L\frac{di}{dt}$$

the change of current satisfies

$$di = \int_{ON}(V_x - V_o)dt + \int_{OFF}(V_x - V_o)dt$$

For steady state operation the current at the start and end of a period T will not change. To get a simple relation between voltages we assume no voltage drop across transistor or diode while ON and a perfect switch change. Thus during the ON time $V_x = V_{in}$ and in the OFF $V_x = 0$. Thus

$$0 = di = \int_0^{t_{on}}(Vin - Vo)dt + \int_{t_{on}}^{t_{on}+t_{off}}(-Vo)dt$$

which simplifies to

$$(Vin - Vo)t_{on} - Vo\ t_{off} = 0$$

or

$$\frac{Vo}{Vin} = \frac{t_{on}}{T}$$

and defining "duty ratio" as

$$D = \frac{t_{on}}{T}$$

the voltage relationship becomes Vo=D Vin Since the circuit is lossless and the input and output powers must match on the average $V_o * I_o = V_{in} * I_{in}$. Thus the average input and output current must satisfy I_{in} =D I_o These relations are based on the assumption that the inductor current does not reach zero.

5.4.2. BOOST CONVERTER STEP-UP CONVERTER

The schematic in Fig. 6 shows the basic boost converter. This circuit is used when a higher output voltage than input is required.

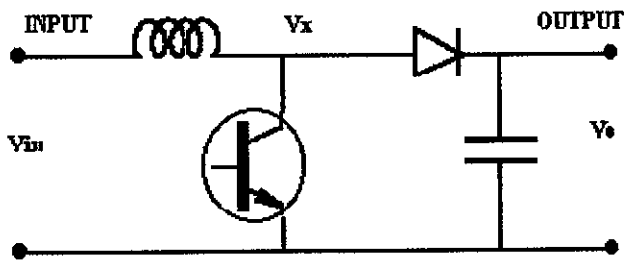


Fig.5.3: Boost Converter Circuit

While the transistor is ON $V_x = V_{in}$, and the OFF state the inductor current flows through the diode giving $V_x = V_o$. For this analysis it is assumed that the inductor current always remains flowing (continuous conduction). The voltage across the inductor is shown in Fig. 7 and the average must be zero for the average current to remain in steady state

$$Vin\, t_{on} + (Vin - Vo)t_{off} = 0$$

This can be rearranged as

$$\frac{Vo}{Vin} = \frac{T}{t_{off}} = \frac{1}{(1-D)}$$

and for a lossless circuit the power balance ensures

$$\frac{Io}{Iin} = (1-D)$$

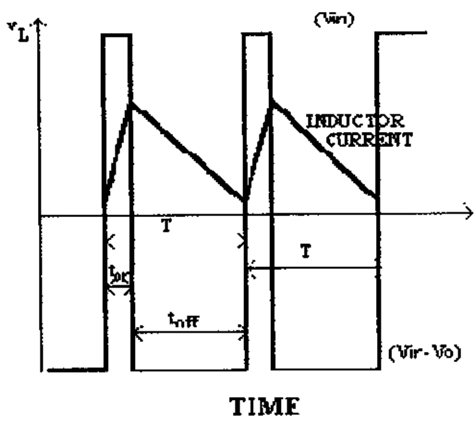


Fig. 5.4: Voltage and current waveforms (Boost Converter)

Since the duty ratio "D" is between 0 and 1 the output voltage must always be higher than the input voltage in magnitude. The negative sign indicates a reversal of sense of the output voltage.

5.4.3. BUCK-BOOST CONVERTER

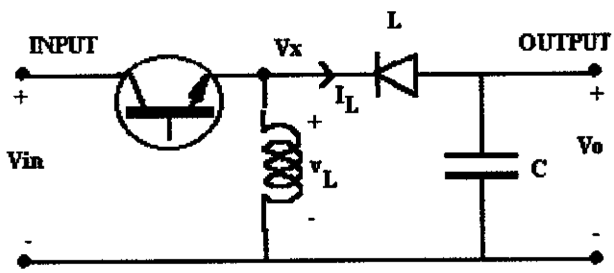


Fig. 5.5: schematic for buck-boost converter

With continuous conduction for the Buck-Boost converter $V_x = V_{in}$ when the transistor is ON and $V_x = V_o$ when the transistor is OFF. For zero net current change over a period the average voltage across the inductor is zero

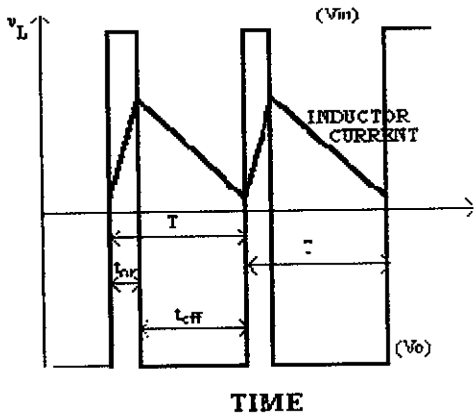


Fig. 5.6: Waveforms for buck-boost converter

$$Vin\,t_{ON} + Vo\,t_{OFF} = 0$$

which gives the voltage ratio

$$\frac{Vo}{Vin} = -\frac{D}{(1-D)}$$

and the corresponding current

$$\frac{Io}{Iin} = -\frac{(1-D)}{D}$$

Since the duty ratio "D" is between 0 and 1 the output voltage can vary between lower or higher than the input voltage in magnitude. The negative sign indicates a reversal of sense of the output voltage.

5.4.4. CUK CONVERTER

The buck, boost and buck-boost converters all transferred energy between input and output using the inductor, analysis is based of voltage balance across the inductor. The CUK converter uses capacitive energy transfer and analysis is based on current balance of the capacitor. The circuit in Fig. 11 is derived from DUALITY principle on the buck-boost converter.

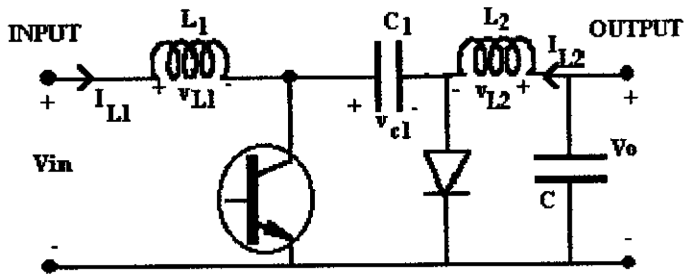


Fig. 5.7: CUK Converter

If we assume that the current through the inductors is essentially ripple free we can examine the charge balance for the capacitor C1. For the transistor ON the circuit becomes

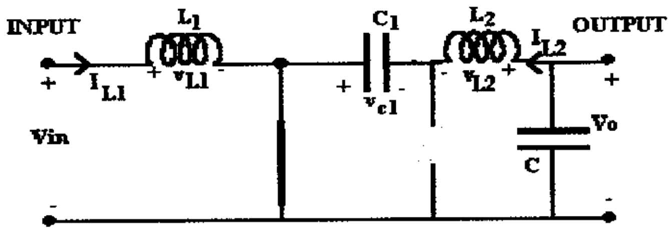


Fig. 5.8: CUK "ON-STATE"

and the current in C1 is I_{L1}. When the transistor is OFF, the diode conducts and the current in C1 becomes I_{L2}.

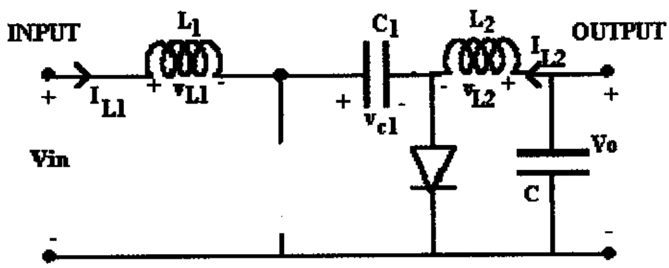


Fig. 5.9: CUK "OFF-STATE"

Since the steady state assumes no net capacitor voltage rise ,the net current is zero

$$I_{L1}t_{ON} + (-I_{L2})t_{OFF} = 0$$

which implies

$$\frac{I_{L2}}{I_{L1}} = \frac{(1-D)}{D}$$

The inductor currents match the input and output currents, thus using the power conservation rule

$$\frac{Vo}{Vin} = -\frac{D}{(1-D)}$$

Thus the voltage ratio is the same as the buck-boost converter. The advantage of the CUK converter is that the input and output inductors create a smooth current at both sides of the converter while the buck, boost and buck-boost have at least one side with pulsed current.

5.5. CONVERTER COMPARISON

The voltage ratios achievable by the DC-DC converters is summarised in Fig. 5.10. Note that only the buck converter shows a linear relationship between the control (duty ratio) and output voltage. The buck-boost can reduce or increase the voltage ratio with unit gain for a duty ratio of 50%.

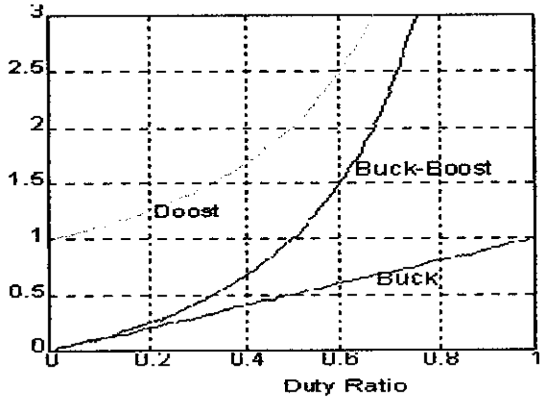


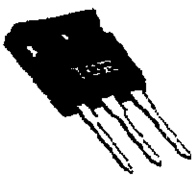
Fig. 5.10: Comparison of Voltage ratio

Here, in our project we use a boost converter in which the output voltage is greater than the input. Even for smaller duty ratios the output voltage is found to be high compared to other configurations as shown.

5.6. MOSFET

5.6.1. INTRODUCTION

The component that is used as the switch in the inverter unit is the MOSFET which is a voltage controlled device. They are the power semi conductor devices that have a fast switching property with a simple drive requirement.



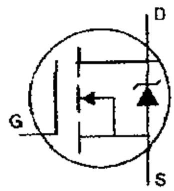


Fig 5.11 MOSFET symbol

5.6.2. MOSFET STRUCTURE

ENHANCEMENT MODE – MOSFET

Both the junction FET and the depletion mode MOSFET operate in a generally intuitive manner. In both device types, an electric field is used to deplete the channel of current carriers to one degree or another, so that a control voltage will directly affect and control the amount of current flowing through the channel. But what happens if we have a device with no working channel, but with room to put a channel in place.

Fig 5.12 Mosfet

The mechanical structure of this device is shown to the right. In an IC, we would place two n-type regions side by side within a p-type area and then place the gate between the n-type regions. However, the important region still consists of the two n-type regions and the p-type area between them. This is the portion we have depicted to the right. With no applied bias, we have what amounts to an npn transistor with no base connection. The two n-type regions are isolated from each other, and are electrically separate. Even with a voltage applied between the two n-type regions, there is no channel present and no current flow. While we still apply the usual positive voltage to the drain with respect to the source, this time we will also apply a positive voltage to the gate region. This has the effect of attracting free electrons towards the gate. The larger the positive gate voltage, the wider its electric field and the more free electrons it will attract. You might not think this would have any effect on the p-type region, where the majority current carriers are holes. However, there are some free electrons here as well. In addition, the source junction is forward biased, so the positive gate voltage can attract electrons across this junction towards the gate. The net result is that the electrons attracted towards the gate actually enhance a channel within the p-type region, as shown to the left. This is a channel formed of free electrons, and actually bridges the gap between source and drain. Now we have a channel, which can conduct current from source to drain through the device. Because these devices operate by having a channel enhanced in the semiconductor material where no channel was constructed, they are known as enhancement-mode MOSFETs.

Enhancement-mode MOSFETs have the same advantages and disadvantages as their depletion-mode cousins. However, when they are constructed as part of an IC rather than as individual devices, they are not readily subject to random static charges. Such ICs are constructed with input protection circuitry for any MOSFET input that must be made accessible to external circuitry.

CHAPTER 6

6. DRIVER UNIT

6.1 INTRODUCTION

It is used to provide 9 to 20 volts to switch the MOSFET Switches of the inverter. Driver amplifies the voltage from microcontroller which is 5volts. Also it has an optocoupler for isolating purpose. So damage to MOSFET is prevented.

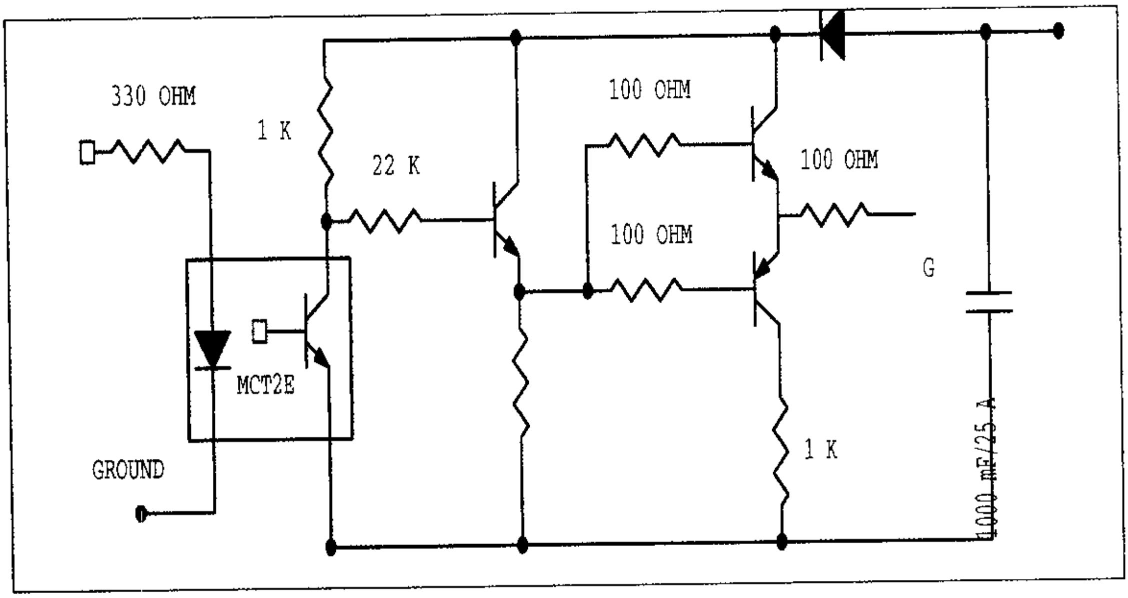


FIG 6.1: DRIVER CIRCUIT.

6.2. COMPONENTS

1. IRFP460
2. Diode N4007
3. Capacitors

   1000uF/50V

   1000uF/25V

   1000uF/250V

4. Optocoupler MCT2E

5. Transistors

2N2222

CK100

6. Resistors

1k, 100 ohm

6.3. OPTOCOUPLER

6.3.1 INTRODUCTION

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct ohmic electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor, which is operating from 5V DC but being used to control a triac that is switching 240V AC. In such situations the link between the two must be an isolated one, to protect the microprocessor from over voltage damage. Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature circuit components. Because they're electro-mechanical, relays are also not as reliable and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an **optocoupler**. These use a beam of light to transmit the signals or data across an electrical barrier, and achieve excellent isolation.

Optocouplers typically come in a small 6-pin or 8-pin IC package, but are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (light-emitting diode) and an optical receiver such as a phototransistor or light-triggered diac. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. The basic idea is shown in Fig.1, along with the usual circuit symbol for an optocoupler. Usually the electrical connections to the LED section are brought out to the pins on one side of the package and those for the phototransistor or diac to the other side, to physically separate them as much as possible. This usually allows optocouplers to withstand voltages of anywhere between 500V and 7500V between input and output. Optocouplers are essentially, digital or switching devices, so they're best for transferring either on-off control signals or digital data. Analog signals can be transferred by means of frequency or pulse-width modulation.

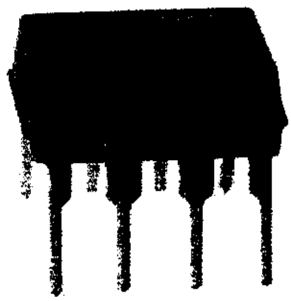


Fig 6.2: An opto-isolator integrated circuit

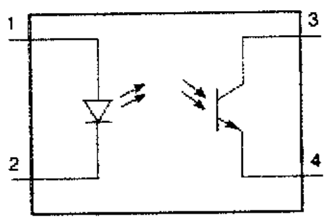


Fig 6.3: Schematic diagram

6.3.2 MCT2E OPTOCOUPLER

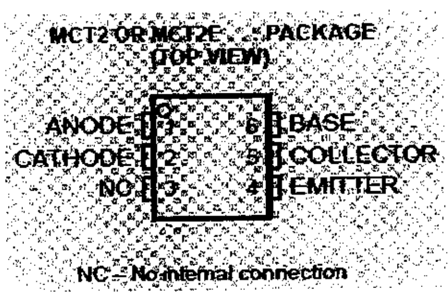


Fig 6.4:MCT2E package top view

SPECIFICATIONS

Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor

High Direct-Current Transfer Ratio

Base Lead Provided for Conventional Transistor Biasing

High-Voltage Electrical Isolation.

1.5-kV, or 3.55-kV Rating

Plastic Dual-In-Line Package

High-Speed Switching:

t_r = 5 µs, t_f = 5 µs Typical

Designed to be Interchangeable with General Instruments MCT2 and MCT2E

CHAPTER 7

7. MATLAB SIMULATION

7.1 INTRODUCTION

New designs of power electronics systems are the norms due to new applications and the lack of standardization in specifications is because of varying customer demands. Accurate simulation is necessary to minimize costly repetitions of designs and bread boarding and hence, reduce the overall cost and the concept-to-production time.

There are many benefits of simulation in the design process, some of which are listed here

- Simulation is well suited for educational purposes. It is an efficient way for designer to learn-how a circuit and its control work.
- It is normally much cheaper to do a thorough analysis than to build the actual circuit in which component stresses are measured. A simulation can discover possible problems and determine optimal parameters, increasing the possibility of getting the prototype "right the first time". Simulation can be used to optimize the performance objective by letting the simulation search over a large number of variables.
- Destructive tests that cannot be done in the laboratory, either because of safety or because of the costs involved, can easily be simulated. Responses to faults and abnormal conditions can also be thoroughly analyzed.
- It is possible to simplify the parts of the circuits in order to focus on a specific portion of the circuit. This may not be possible in a laboratory setup.
- Simulated waveforms at different places in the circuit are easily monitored without the hindrance of measurement noise(and other noise sources). As switching frequencies increases, the problem of laboratory measurements becomes increasingly difficult. Hence simulation is essential.

7.2 SIMULATION MODEL

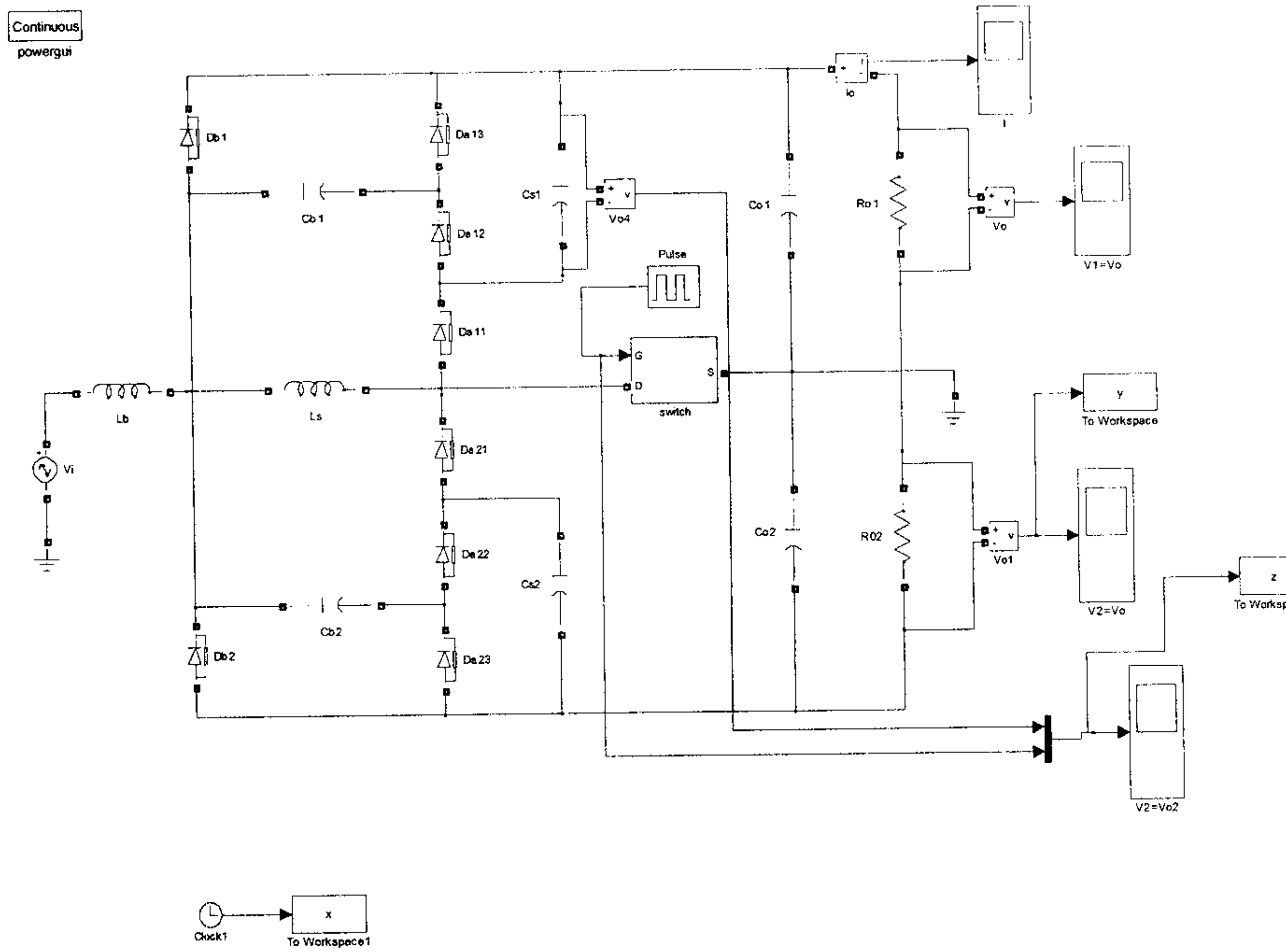
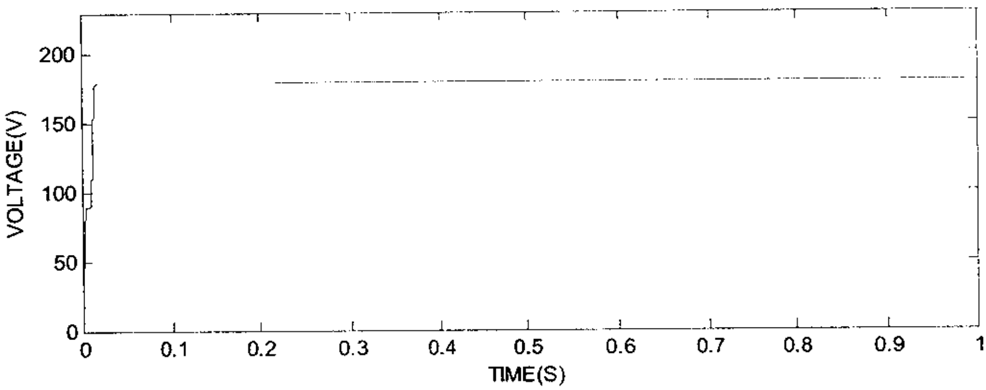


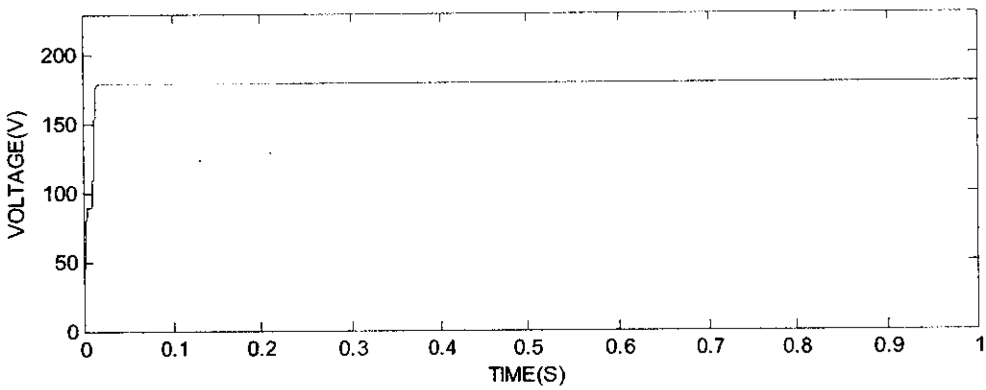
Fig 7.1 Simulink model

7.3 SIMULATION RESULTS

LEVEL 1 OUTPUT:



LEVEL 2 OUTPUT:



ZERO VOLTAGE SWITCHING:

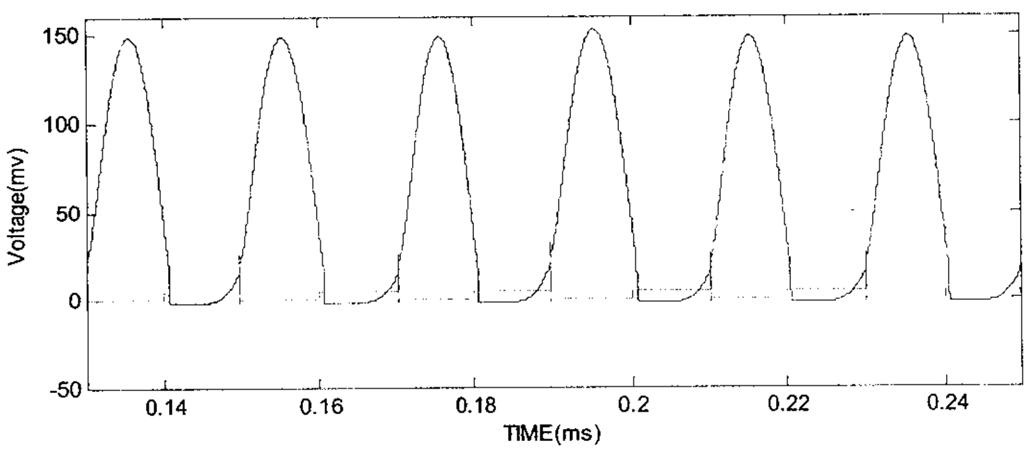


Fig 7.2 Simulation output waveforms

The above waveforms are the simulated results. Here, we can see that the dc output voltage of level 1 and level 2 are of the same magnitude. So two symmetrical or balanced loads can be connected and supplied at the same time. The waveform below the two output voltage level waveforms indicates the zero voltage switching. Here, the gate pulse is triggered when the capacitor voltage is nearing zero or at the zero instant. This is to make sure that the voltage across the particular power switch is zero. After the pulse is triggered, the capacitor starts charging and the procedure is repeated as shown in the waveform. For every charging and discharging cycle of the capacitor, a gate pulse is produced and thus the switch is turned on and off. The switching practically takes place in fraction of seconds.

CHAPTER 8

8. HARDWARE IMPLEMENTATION

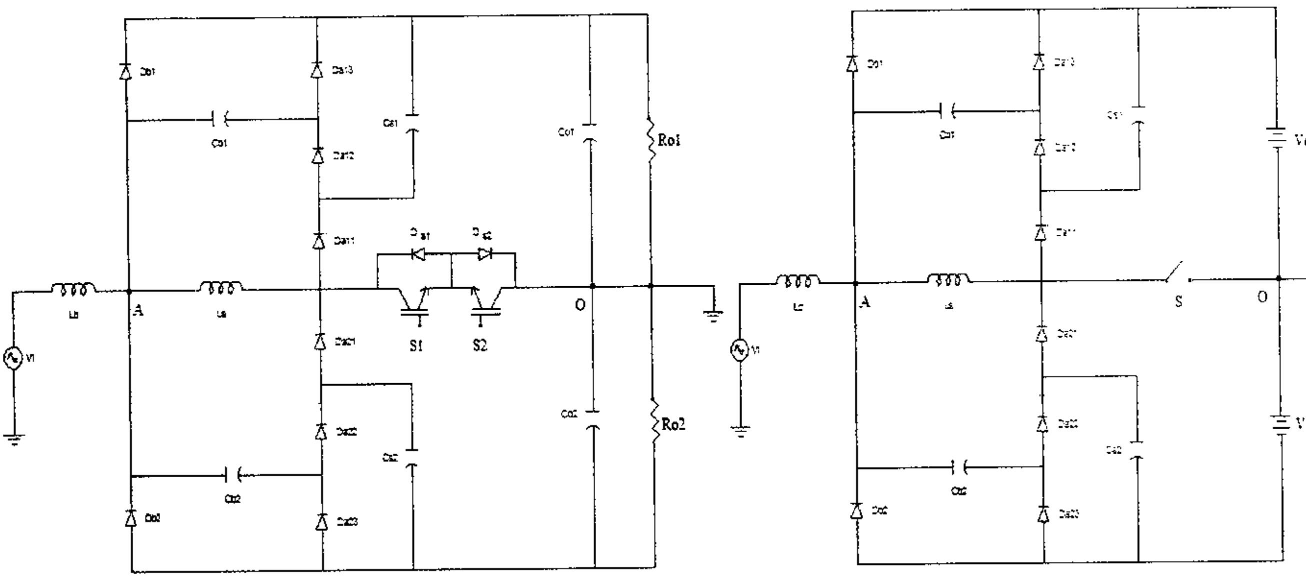
8.1. INTRODUCTION

The boost PFC circuit operating in continuous conduction mode is by far the popular choice for medium and high-power (from 400 W to a few kilowatts) applications. This is because the continuous nature of the boost converter's input current results in low conducted electromagnetic interference (EMI) compared to other active PFC topologies such as the buck–boost and buck converters. Another way to obtain the PFC is using static filters between the power source and the diode bridge, but this is a heavy and bulky solution because the filter frequency is low (50–60 Hz) and the filter needs big capacitors and inductors. For three-phase applications, several pulse width-modulated boost rectifiers are available in the literature. The six-switch full-bridge rectifier allows bidirectional power flow, although current stresses are quite high and very high switching frequencies are necessary to reduce the filters' size. This converter presents high cost and low efficiency if compared to similar topologies

For low-power applications, the concept of three level rectifiers can be extended to a single-phase structure, and these three-level structures present good characteristics. In three-level rectifiers, the reverse recovery of boost diodes is an undesirable effect . It occurs via a low-impedance loop, formed by the turned-on switches and the output stages, causing high current peaks in the switches at the same time when they are submitted to the output voltage. Thus, conduction losses are quite high during turning on. SiC Schottky diodes present zero-recovery current and negligible switching losses and have become a benchmark for virtually lossless operation. They can deliver highly efficient switching at frequencies up to several hundred kilohertz and have been deployed as the boost diodes in PFC units of switched-mode power supplies operating in continuous-current mode.

However, SiC diodes remain more expensive than their silicon equivalents due to higher material costs. To obtain soft switching, many alternatives were developed , but they are not well suited for this type of application because it demands a lot of components to obtain soft-switching characteristics. Another alternative is the introduction of inductors between diodes and switches, establishing some impedance path regarding the recovery of diodes. It limits the current increasing rate during the turning on and reduces the peak current that also flows through the switches, providing a zero-current switching (ZCS) at turning on . Another problem related to commutation lies in the *d?/dt* rates and high-frequency voltage ripple during turning off, which can be mitigated by the introduction of capacitors in parallel with the switches, providing a zero-voltage switching (ZVS) during the turning off. Within this context, this project implements a single-phase three level rectifier with soft switching. Theoretical background on the proposed snubber is presented, which is associated with the topology.

8.2. CIRCUIT DIAGRAM:



(a) (b)

Fig. 8.1. Single-phase three-level rectifier associated with a passive snubber cell.
(a) Proposed topology. (b) Simplified topology.

8.3. OPERATING PRINCIPLE AND MATHEMATICAL ANALYSIS

Fig. 8.1(b) shows the simplified circuit considered in the analysis of the operating stages. Additionally, the following conditions are assumed.

1) All semiconductors are ideal except for diodes $Db1$ and $Db2$.

2) Since bidirectional power flow is possible due to switches $S1$ and $S2$, and also intrinsic diodes $Ds1$ and $Ds2$, they can be replaced by a bidirectional switch S.

3) Considering that loads are perfectly balanced, output capacitances $Co1$ and $Co2$ are treated as constant voltage sources Vo. If loads are unbalanced, asymmetry between the positive and

negative half cycles of the input current results. Therefore, the operation will only be possible if an additional control circuit is implemented to compensate such imbalance.

4) The input current Ii is constant within one switching cycle.

5) The boost inductance is much greater than Ls.

A. First Stage [t0, t1]

Switch S is turned on at $t0$. During the turning-on process, diode Db1 is not immediately turned off because of the reverse recovery phenomenon. The increase rate of the drain–current is restricted by the snubber inductor to softly turn on the MOSFET. The current through Ls is

$$i\mathrm{Ls}(t) = Ii(t0) - Vo/Ls \cdot (t - t0)$$

where $ii(t)$ is the input current.

B. Second Stage [t1, t2]

The reverse-recovery phenomenon finishes at $t1$. As soon as$D$b1 is turned off, diode Da12 is naturally turned on because VCs1 and VCb1 are equal to zero. Snubber inductor Ls, snubber capacitor Cs1, and buffer capacitor Cb1 are charged by the output through the first resonant path Vo - Cs1 - Da12 - Cb1 - Ls - S. The increase rate of the voltage across Db1, which is equal to VCs1 + VCb1, is restricted to achieve ZVS turning off of diode Db1. Snubber inductor current, snubber capacitor voltage, and buffer capacitor voltage are

$$i\mathrm{Ls}(t) = - Vo/Z1 \cdot \sin[\omega 1 \cdot (t - t1)] - Irr \cdot \cos[\omega 1 \cdot (t - t1)]$$

$$v\mathrm{Cs1}(t)\,[Cb1/(Cs1 + Cb1)] \cdot v(t)$$

$$v\mathrm{Cb1}(t) = [Cs1/(Cs1 + Cb1)] \cdot v(t)$$

C. Third Stage [t2, t3]

After VCs1 is charged to output voltage Vo at t2, Da11 is turned on, and VCs1 remains constant. The current through Ls keeps charging Cb1 through the second resonant path Da11 - Da12 - Cb1. Ls and Cb1 are performing one-way resonance because of diodes Da11 and Da12. The current through Ls and the voltage across Cb1 are given by (12) and (13), respectively.

$$i_{Ls}(t) = [C_{s1}/C_{b1}] \cdot [V_o/Z_2] \cdot \sin[\omega_2 \cdot (t - t_2)] - I_{S2} \cdot \cos[\omega_2 \cdot (t - t_2)]$$

$$v_{Cb1}(t) = I_{S2} \cdot Z_2 \cdot \sin[\omega_2 \cdot (t - t_2)] + [C_{s1}/C_{b1}] \cdot V_o \cdot \cos[\omega_2 \cdot (t - t_2)]$$

where

$$I_{S2} = [V_o/Z_1] \cdot \sin[\omega_1 \cdot (t_2 - t_1)] + I_{rr} \cdot \cos[\omega_1 \cdot (t_2 - t_1)]$$

$$Z_2 = \sqrt{L_s/C_{b1}}$$

$$\omega_2 = 1/\sqrt{L_s \cdot C_{b1}}.$$

Since the energy in Ls is transferred to Cb1 in this stage, the following expression is valid:

$$E_{Cb1}(t_3) = 1/2 \cdot C_{b1} \cdot V^2_{Cb1}(t_3)$$

$$= E_{Ls}(t_2) + E_{Cb1}(t_2)$$

$$= 1/2 \cdot L_s \cdot I^2_{rr} + 1/2 \cdot C_{s1} \cdot V^2_o$$

Furthermore, the peak voltage across the buffer capacitor $V_{Cb1(pk)}$ is

$$V_{Cb1(pk)} = V_{Cb1}(t_3) = \sqrt{[L_s \cdot I^2_{rr} + C_{s1} \cdot V^2_o]/C_{b1}}.$$

It also determines the voltage stress across boost diode, which is equal to V_o plus $V_{Cb1(pk)}$.

D. Fourth Stage [t3, t4]

At t_3, I_{Ls} is constant while D_{a11} and D_{a12} are turned off. The voltage across C_{b1} is constant after instant t_3.

E. Fifth Stage [t4, t5]

After switch S is turned off at t_4, current $I_i(t_4)$ flows through D_{a11} to discharge C_{s1} to the output. Diodes D_{a12} and D_{a13} are not turned on because they are reverse-biased by V_{Cs1}. The drain–source voltage across S is equal to $V_o - V_{Cs1}$. Slow dv/dt of the drain–source voltage is obtained, whereas V_{Cs1} is discharged from V_o to zero. Assuming that $i_i(t)$ is constant during this stage, V_{Cs1} is given by

$$v_{Cs1}(t) = V_o - [I_i(t_4)/C_{s1}](t - t_4).$$

F. Sixth Stage [t5, t6]

Diodes D_{a12} and D_{a13} are turned on when C_{s1} is discharged to zero at t_5. Then, the following expression is valid.

$$v_{Cb1}(t) = V_{Cb1}(t_2) \cdot \cos[\omega_2 \cdot (t - t_5)].$$

G. Seventh Stage [t6, t7]

Current I_{Ls} becomes null, and diodes D_{a11} and D_{a12} are turned off. After $t6$, $i_i(t)$ discharges C_{b1} to output through D_{a13}. The ZVS turning on of diode D_{b1} is achieved by slow $d?/dt$ of V_{Cb1}. Assuming that $i_i(t)$ is constant in this stage, $?_{Cb1}(t)$ is given by

$$?_{Cb1}(t) = V_{Cb1}(t6) - [I_i(t6)/C_{b1}] \cdot (t - t6).$$

H. Eighth Stage [t7, t8]

Capacitor voltage V_{Cb1} is fully discharged at $t7$. D_{a13} is turned off, and D_{b1} is turned on simultaneously. The snubber energy-recovery process is accomplished when all energy in the buffer capacitor C_{b1} is transferred to the output. After that, input current $i_i(t)$ flows through D_{b1} instead of D_{a13} to prevent C_{s1} from being reversely charged as a new switching cycle begins.

8.4. PASSIVE SNUBBER ELEMENTS

Snubber inductor L_s, snubber capacitor C_{s1}, and buffer capacitor C_{b1} are the three main elements to be designed. The following rules should be noticed when designing the respective values. In stage 6, diodes D_{a11} and D_{a12} should be naturally turned off before the voltage across C_{b1} is discharged to zero, or the remaining current will turn on D_{a11}, D_{a12}, and D_{a13} for the entire switching period. In other words, the following inequality has to be obeyed. Larger C_{s1} results in higher MOSFET current stress and higher diode voltage stress. C_{b1} has to be at least 16 times C_{s1} to limit V_{Cb1} to 100 V with a 400-V output, for instance. Practically, C_{b1} should be about 30 times C_{s1} considering reverse-recovery energy. Snubber inductor L_s should be selected as large as possible to decrease reverse-recovery loss.

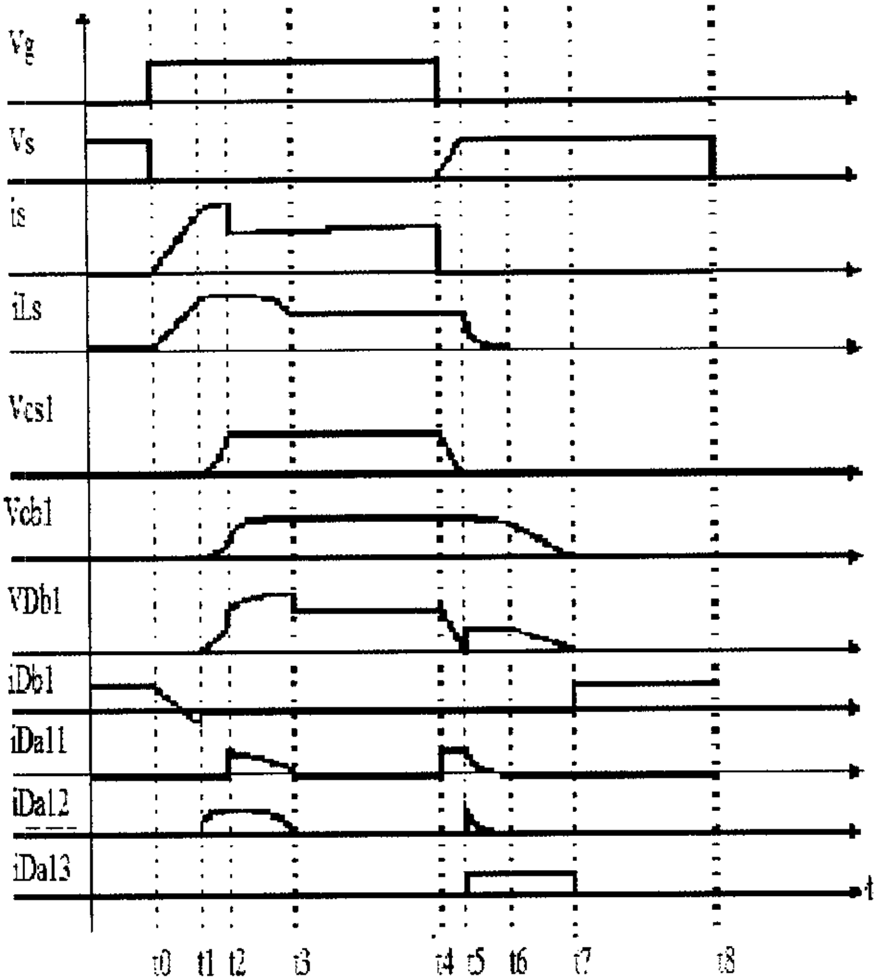


Fig 8.2 Main theoretical waveforms

V_g	-	Gate voltage
V_s	-	Source voltage
i_s	-	Current through the switch
i_{Ls}	-	Current through the inductor L_s
V_{cs1}	-	Voltage across capacitor C_{s1}
V_{cb1}	-	Voltage across the capacitor C_{b1}
V_{Db1}	-	Voltage across the diode D_{b1}
i_{Db1}	-	current through the diode D_{b1}
i_{Da11}, i_{Da12}, i_{Da13}	-	current through the diodes D_{a11}, D_{a12}, D_{a13} respectively.

8.5 HARDWARE ASSEMBLY

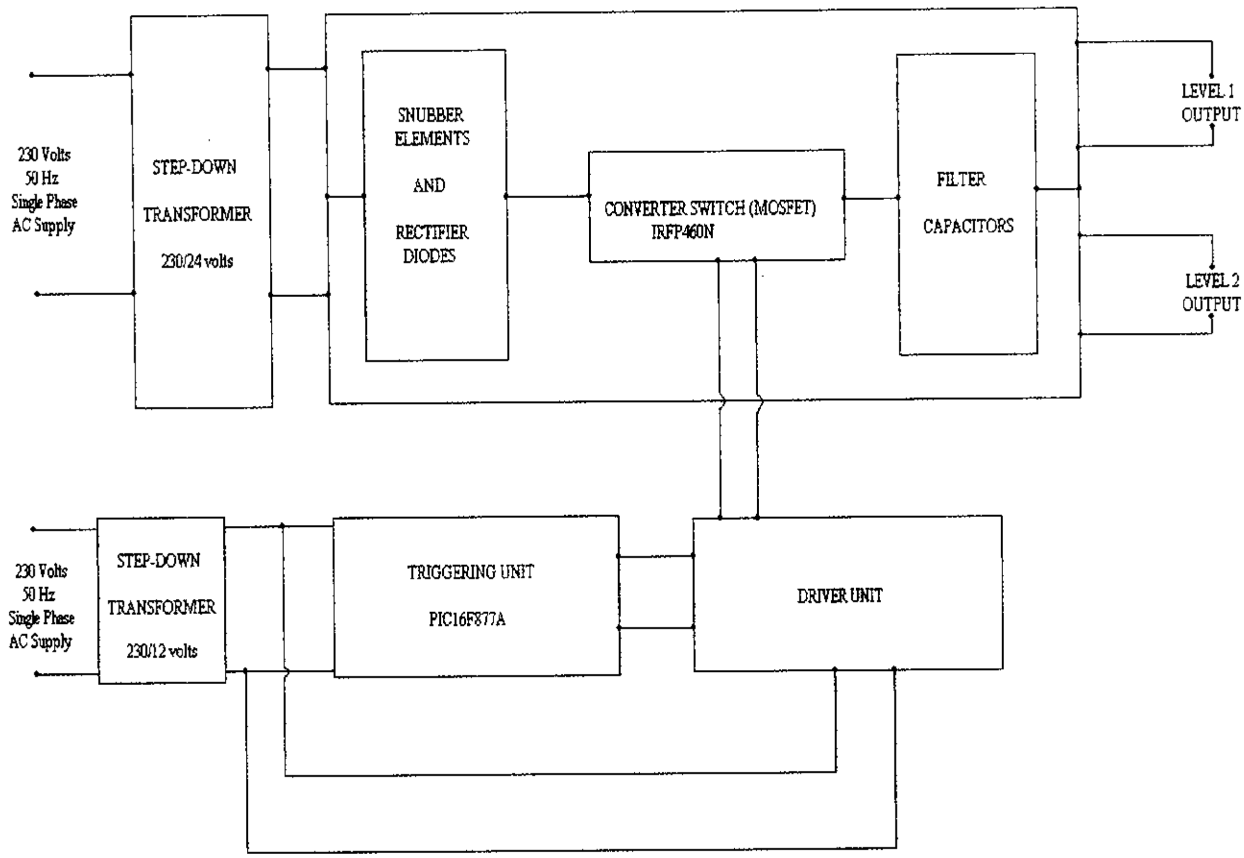


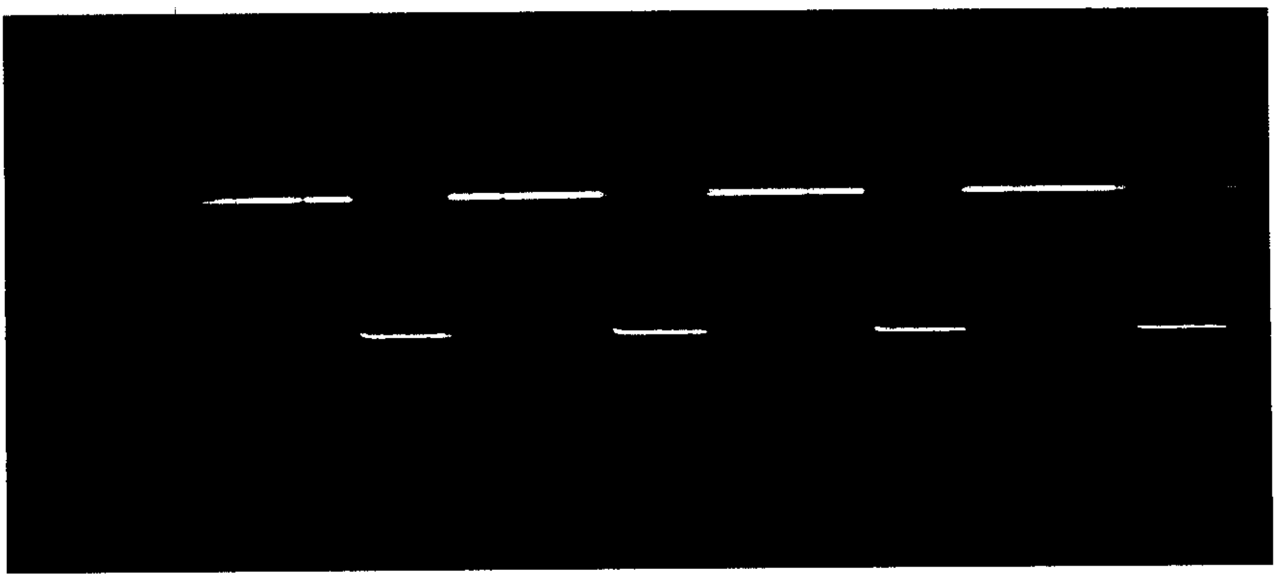
Fig 8.3 Hardware assembly

Fig shows the overall hardware assembly. The 230 volts,50 Hz, single phase ac voltage input is stepped down to 24 volts by a step down transformer. This ac voltage is fed into the snubber circuit and a rectifier assembly. Snubber circuit has snubber inductors and snubber capacitors to restrict di/dt and dv/dt of the diodes. It also consists of snubber diodes in order to reduce switching losses and EMI noise during turning on and off. The output from the rectifier assembly is an uncontrolled dc voltage which can be regulated and controlled by a converter. Here a MOSFET switch is used which performs the boost operation. This MOSFET receives gate pulses from the triggering unit which has a PIC microcontroller. MOSFET receives gate signals when the voltage across it is zero, thereby enabling zero voltage switching. The triggering unit receives the same input ac voltage which is stepped down to 12 volts by a transformer shown. The gate pulses produced by the microcontroller is only 5 volts which is not sufficient to trigger the switch. Hence, it is required to amplify the pulse which is done by the driver circuit. Finally, a filter capacitor is used to reduce the harmonics so that a pure dc voltage is supplied to the load.

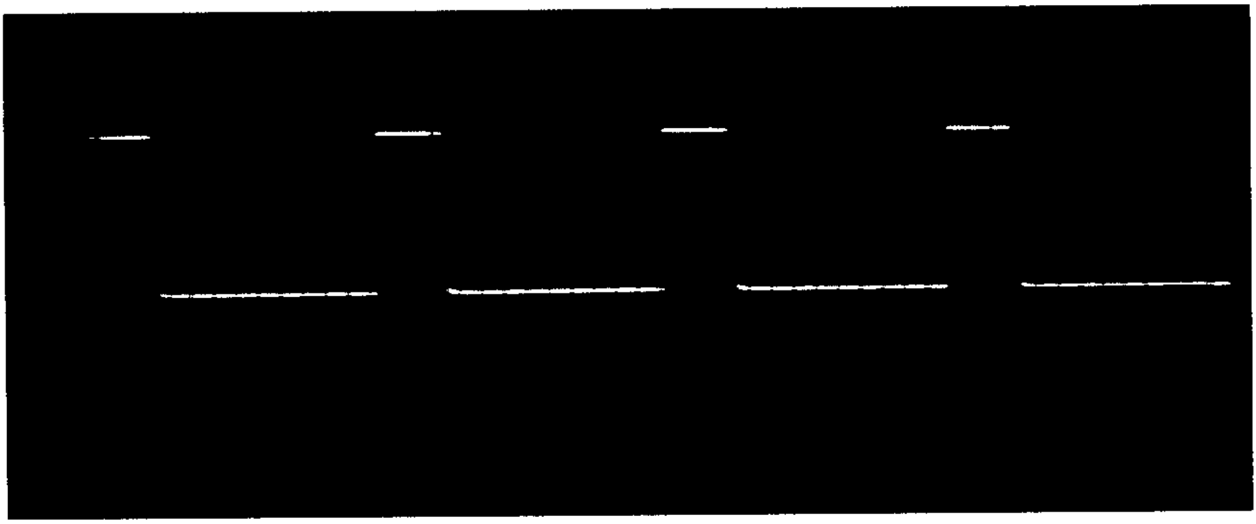
8.6 HARDWARE RESULTS

VARIATION OF OUTPUT VOLTAGE WITH PULSEWIDTH:

PULSE WIDTH(Gate Pulse)-Ton (ms)	OUTPUT VOLTAGE(Rectifier) (volts)
0.15	6.7
0.16	7.7
0.18	8.7
0.20	10.2
0.24	12



CRO output 1: Pulse width of gate pulse (Ton) = 0.24 ms, Corresponding output voltage = 12 V



CRO output 2: Pulse width of gate pulse (Ton) = 0.15 ms, Corresponding output voltage = 6.7 V

HARDWARE IMAGE:

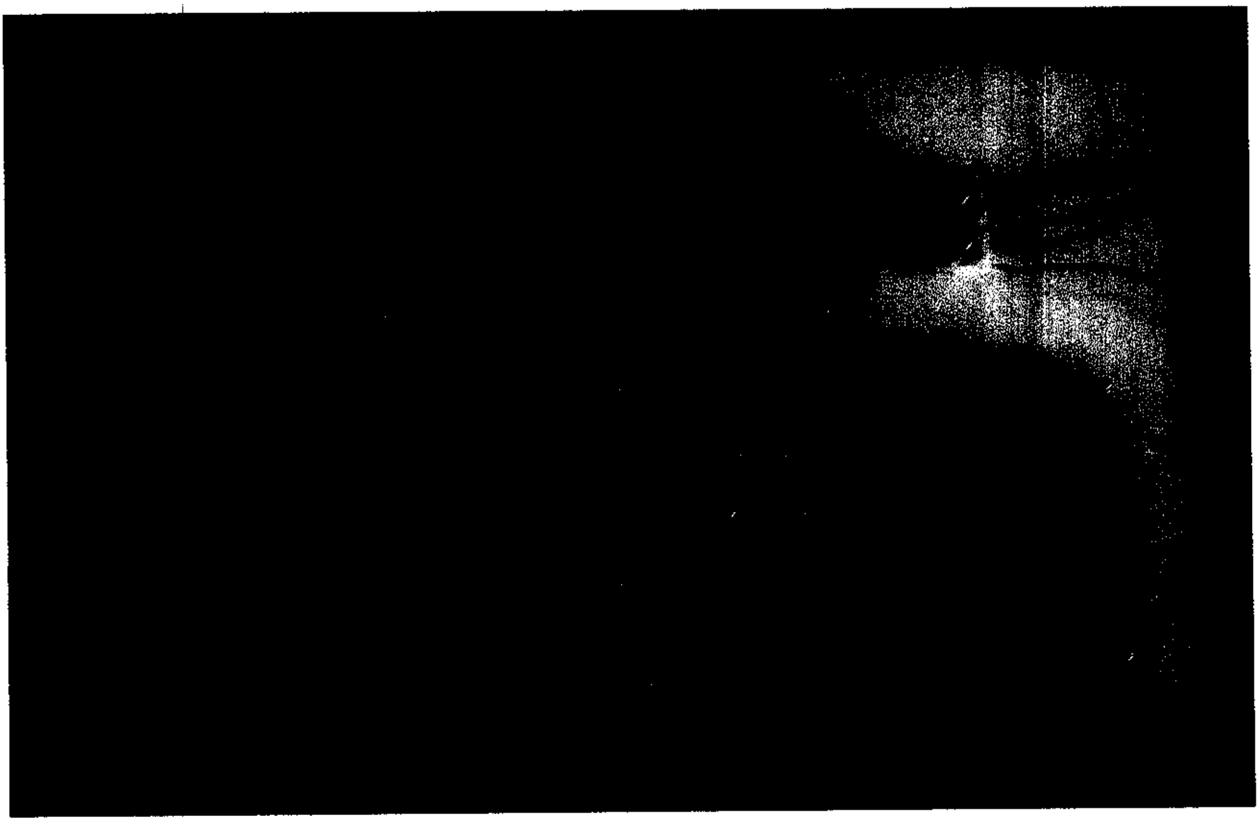


IMAGE 1: OVERALL HARDWARE

CHAPTER 9

9. CONCLUSION

9.1 OUTCOME OF THE PROJECT

A soft switching single phase three-level rectifier has been designed, fabricated and tested in the project. The design topology provides high efficiency as it operates with reduced conduction losses. The device voltage rating is only half of the output voltage, which is desirable for high-power applications, and minimizes both conduction and switching losses. By using an average current-mode control, the converter achieves a nearly unity power-factor operation and a low harmonic content of the input current. The proposed snubber presents only one resonant inductor instead of two magnetic elements. Then, reduced cost, weight, and number of devices and, consequently, increased robustness are the direct advantages. The former characteristics such as soft switching, high efficiency, unity power factor, and low harmonic distortion are also maintained. The use of a passive non dissipative snubber provides soft commutation of the main switches, without the aid of auxiliary switches, reducing control complexity. If di/dt and d?/dt rates are limited, the ZCS turning on and ZVS turning off can be achieved, as switching losses become negligible.

9.2 FUTURE SCOPE OF THE PROJECT:

The multi level concept will be a prominent choice for power electronic systems in future years, especially for medium voltage operation. The circuit can be further simplified by reducing the number of switches thus minimizing the components .This can be further extended to high power applications by using higher rating devices.

9.3 APPLICATIONS:

- Shipping electrical connections & equipments
- Battery chargers
- Traction applications

REFERENCES

REFERENCES

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[2] J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase AC supplies and using either single or split DC rail voltage outputs," in *Proc. APEC*, Mar. 1995, vol. 1, pp. 473–479.

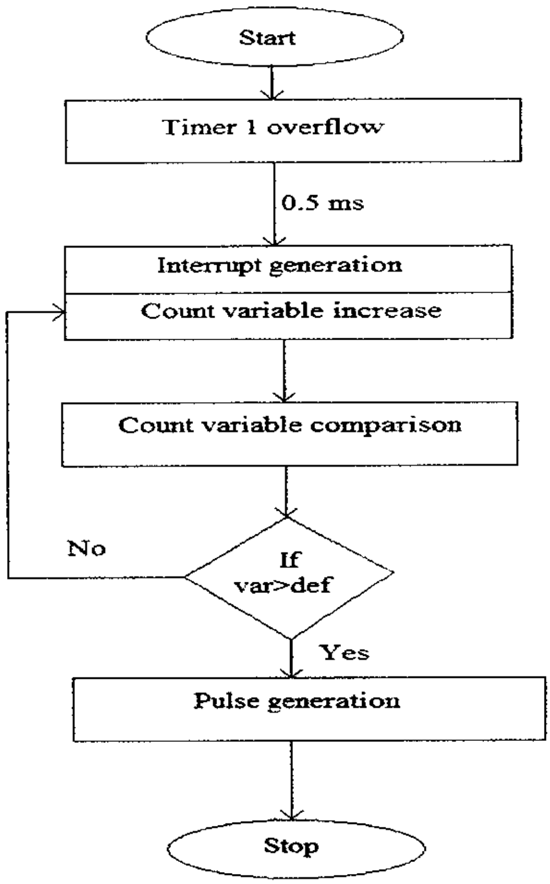
[3] R. Teichmann, M. Malinowske, and S. Bernet, "Evaluation of three-level rectifiers for low-voltage utility applications," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 471–481, Apr. 2005.

[4] A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 83–92, Jan. 1991.

[5] J. W. Kolar and F. C. Zach, "A novel three-phase three-switch threelevel PWM rectifier," in *Proc. 28th Power Convers. Conf.*, Jun. 1994, pp. 125–138.

APPENDIX I

LOGIC FLOWCHART FOR PULSE GENERATION



PIC PROGRAMMING SOURCE CODE:

```
#include<pic.h>
#include<stdio.h>
#include "delay.c"
__CONFIG(0x3f72);
unsigned char n=1;
void main()
{
        RBPU=0;
```

```
TRISB=0XFF;
TRISC=0x00;
PORTC=0;
PORTB=0xFF;
while(1)
{
        if(RB0==0)
                n=1;
        if(RB1==0)
                n=2;
        if(RB2==0)
                n=3;
        if(RB3==0)
                n=4;


 if(n==1)
        {
                PORTC=0x03;
               DelayMs(49);
         PORTC=0x00;
               DelayMs(1);
               PORTC=0x0c;
               DelayMs(49);
        PORTC=0x00;
               DelayMs(1);


        }
        else if(n==2)
        {
 PORTC=0x03;
```

```
    DelayMs(9);
    PORTC=0x00;
    DelayMs(1);

    PORTC=0x0c;
    DelayMs(9);
        PORTC=0x00;
    DelayMs(1);

      }
      else if(n==3)
      {
              PORTC=0x03;
    DelayMs(7);
    DelayUs(334);
    PORTC=0x00;
    DelayMs(1);

    PORTC=0x0c;
    DelayMs(7);
    DelayUs(334);
                   PORTC=0x00;
    DelayMs(1);

  }
                   else if(n==4)
      {
                   PORTC=0x00;
      }
  }
}
```

APPENDIX II

FAIRCHILD
SEMICONDUCTOR®

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							μA
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							μA μA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Typical Characteristics

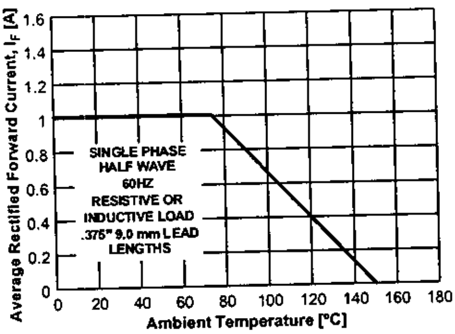


Figure 1. Forward Current Derating Curve

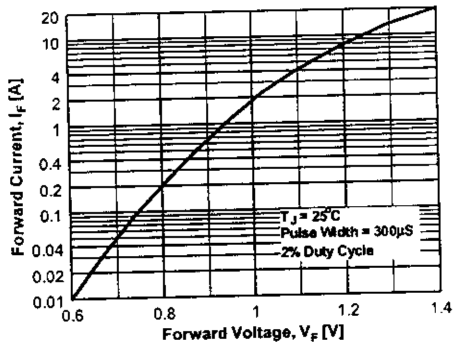


Figure 2. Forward Voltage Characteristics

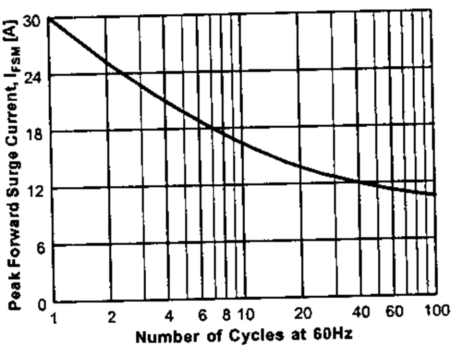


Figure 3. Non-Repetitive Surge Current

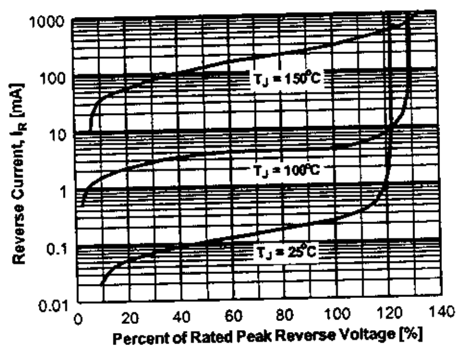


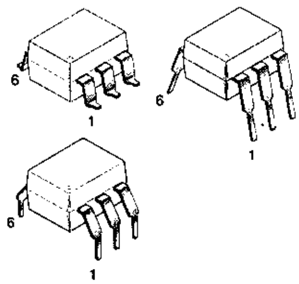
Figure 4. Reverse Current vs Reverse Voltage

FAIRCHILD
SEMICONDUCTOR®

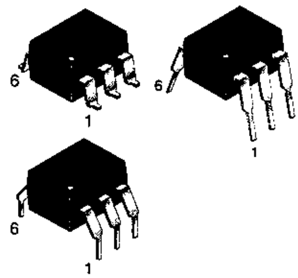
PHOTOTRANSISTOR OPTOCOUPLERS

MCT2 **MCT2E** **MCT210** **MCT271**
MCT2200 **MCT2201** **MCT2202**

WHITE PACKAGE (-M SUFFIX)



BLACK PACKAGE (NO -M SUFFIX)



DESCRIPTION

The MCT2XXX series optoisolators consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package.

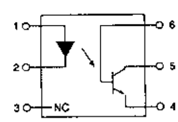
FEATURES

- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  - -Add option V for white package (e.g., MCT2V-M)
  - -Add option 300 for black package (e.g., MCT2.300)
- MCT2 and MCT2E are also available in white package by specifying -M suffix, eg. MCT2-M

APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

SCHEMATIC



PIN 1. ANODE
2. CATHODE
3. NO CONNECTION
4. EMITTER
5. COLLECTOR
6. BASE

FAIRCHILD SEMICONDUCTOR®

PHOTOTRANSISTOR OPTOCOUPLERS

MCT2 **MCT2200** **MCT2E** **MCT2201** **MCT210** **MCT2202** **MCT271**

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER							
Input Forward Voltage	(I_F = 20 mA)	V_F	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202		1.25	1.50	V
	(T_A = 0-70°C, I_F = 40 mA)		MCT210		1.33		
Reverse Leakage Current	(V_R = 3.0 V)	I_R	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202		0.001	10	μA
	(T_A = 0-70°C, V_R = 6.0 V)		MCT210				
DETECTOR							
Collector-Emitter Breakdown Voltage	(I_C = 1.0 mA, I_F = 0)	BV_{CEO}	ALL	30	100		V
	(T_A = 0-70°C)		MCT210				
Collector-Base Breakdown Voltage	(I_C = 10 μA, I_F = 0)	BV_{CBO}	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202	70	120		V
	(T_A = 0-70°C)		MCT210	30			
Emitter-Collector Breakdown Voltage	(I_E = 100 μA, I_F = 0)	BV_{ECO}	MCT2/-M MCT2E/-M MCT271 MCT2200 MCT2201 MCT2202	7	10		V
	(T_A = 0-70°C)		MCT210	6	10		
Collector-Emitter Dark Current	(V_{CE} = 10 V, I_F = 0)	I_{CEO}	ALL		1	50	nA
	(V_{CE} = 5 V, T_A = 0-70°C)					30	μA
Collector-Base Dark Current	(V_{CB} = 10 V, I_F = 0)	I_{CBO}	ALL			20	nA
Capacitance	(V_{CE} = 0 V, f = 1 MHz)	C_{CE}	ALL		8		pF

** Typical values at T_A = 25°C

FAIRCHILD
SEMICONDUCTOR®

PHOTOTRANSISTOR OPTOCOUPLERS

MCT2 MCT2200 MCT2E MCT2201 MCT210 MCT2202 MCT271

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristic	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Output Collector Current	(T_A = 0-70°C) (I_F = 10 mA, V_{CE} = 5 V)	CTR	MCT210	150			%
	(I_F = 10 mA, V_{CE} = 5 V)		MCT2200	20			
			MCT2201	100			
			MCT2202	63		125	
	(I_F = 10 mA, V_{CE} = 10 V)		MCT2	20			
			MCT2-M	20			
			MCT2E	20			
			MCT2E-M	20			
			MCT271	45		90	
	(I_F = 3.2 mA to 32 mA, V_{CE} = 0.4 V) (T_A = 0-70°C)		MCT210	50			
Collector-Emitter Saturation Voltage	(I_C = 2 mA, I_F = 16 mA)	$V_{CE\ (SAT)}$	MCT2			0.4	V
			MCT2-M				
			MCT2E				
			MCT2E-M				
			MCT271				
	(I_C = 16 mA, I_F = 32 mA, T_A = 0-70°C)		MCT210				
	(I_C = 2.5 mA, I_F = 10 mA)		MCT2200				
			MCT2201				
			MCT2202				
AC Characteristic Saturated Turn-on Time from 5 V to 0.8 V	(I_F = 15 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = Open) (Fig. 20)	t_{on}	MCT2		1.1		µs
			MCT2E		1.1		
	(I_F = 20 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = 100 kΩ) (Fig. 20)		MCT2		1.3		
			MCT2E		1.3		
Saturated Turn-off Time from SAT to 2.0 V	(I_F = 15 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = Open) (Fig. 20)	t_{off}	MCT2		50		
			MCT2E		50		
	(I_F = 20 mA, V_{CC} = 5 V, R_L = 2 kΩ) (R_B = 100 kΩ) (Fig. 20)		MCT2		20		
			MCT2E		20		
Turn-on Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_{on}	MCT2-M MCT2E-M		2		
Turn-off Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_{off}	MCT2-M MCT2E-M		2		
Rise Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_r	MCT2-M MCT2E-M		2		
Fall Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)	t_f	MCT2-M MCT2E-M		1.5		

** Typical values at T_A = 25°C

TRANSFER CHARACTERISTICS (Cont.)

AC Characteristic	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Saturated turn-on time	(I_F = 16 mA, R_L = 1.9kΩ, V_{CC} = 5 V) (Fig. 20)	t_{on}	MCT271		1.0		μs
Saturated turn-off time (Approximates a typical TTL interface)		t_{off}			48		
Saturated turn-on time	(I_F = 16 mA, R_L = 4.7kΩ, V_{CC} = 5 V) (Fig. 20)	t_{on}			1.0		
Saturated turn-off time (Approximates a typical low power TTL interface)		t_{off}			98		
Saturated rise time	(I_F = 16 mA, R_L = 560Ω, V_{CC} = 5 V) (Fig. 20, 21)	t_r	MCT210		1.0		
Saturated fall time		t_f			11		
Saturated propagation delay - high to low	(I_F = 16 mA, R_L = 2.7kΩ) (Fig. 20, 21)	$T_{PD\ (HL)}$			1.0		
Saturated propagation delay - low to high		$T_{PD\ (LH)}$			50		
Non-saturated turn on time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100Ω (Fig. 20)	T_{ON}	MCT2200 MCT2201 MCT2202		2	10	
Non-saturated turn off time		T_{OFF}			2	10	
Non-saturated rise time	(I_C = 2 mA, V_{CC} = 5 V, R_L = 100Ω) (Fig. 20)	t_r	MCT210		2		
Non-saturated fall time		t_f			2		
Non-saturated turn-on time	(I_C = 2 mA, V_{CC} = 5 V, R_L = 100Ω) (Fig. 20)	t_{on}	MCT271		2	7	
Non-saturated turn-off time		t_{off}			2	7	

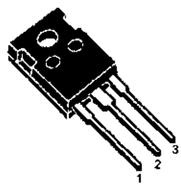
** Typical values at T_A = 25°C

IRFP460

N - CHANNEL 500V - 0.22 Ω - 20 A - TO-247 PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFP460	500 V	< 0.27 Ω	20 A

- TYPICAL $R_{DS(on)}$ = 0.22 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-247

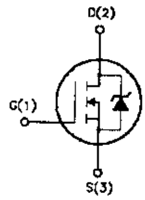
DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- DC/DC COVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT.

INTERNAL SCHEMATIC DIAGRAM



SC06140

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	20	A
I_D	Drain Current (continuous) at T_c = 100 °C	13	A
I_{DM}(•)	Drain Current (pulsed)	80	A
P_{tot}	Total Dissipation at T_c = 25 °C	250	W
	Derating Factor	2	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 20$ A, di/dt ≤ 160 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 250 V I_D = 10 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 1)		32 15		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V I_D = 20 A V_{GS} = 10 V		100 21 37	130	nC nC nC

SWITCHING OFF

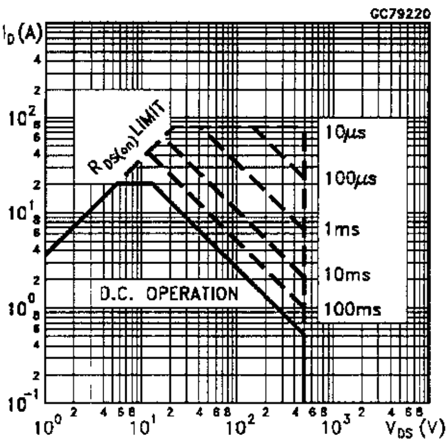
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400 V I_D = 20 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		20 25 47		ns ns ns

SOURCE DRAIN DIODE

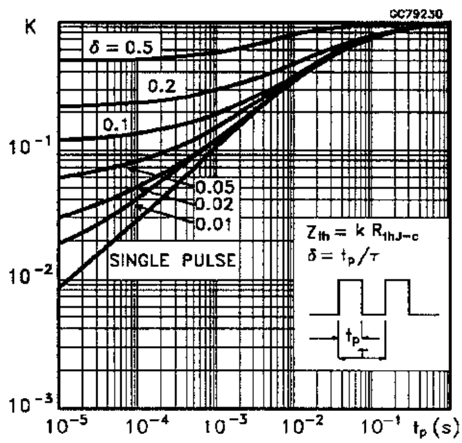
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 20 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 3)		700 9 25		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

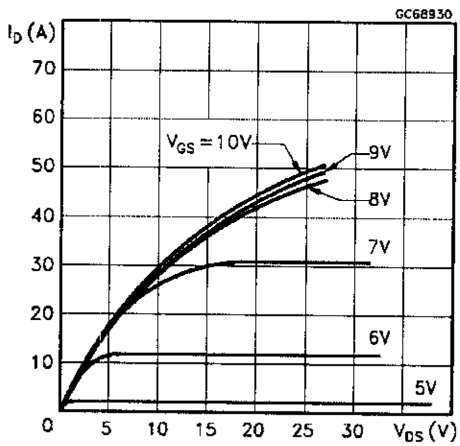
Safe Operating Area



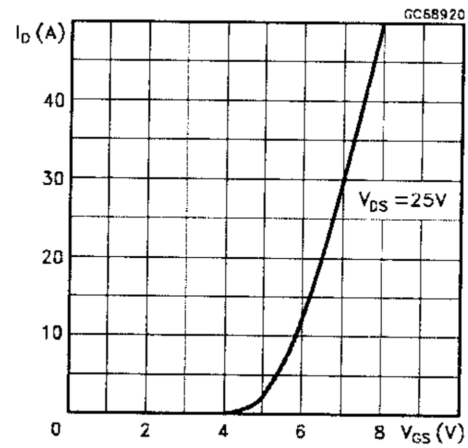
Thermal Impedance



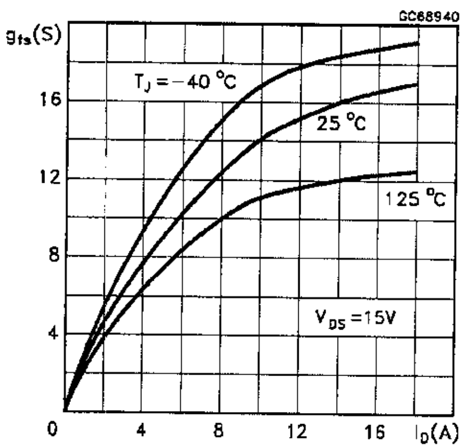
Output Characteristics



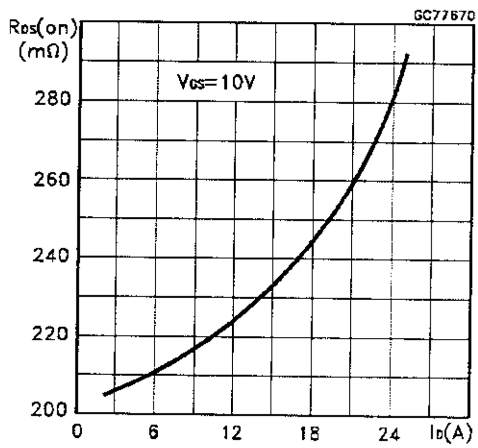
Transfer Characteristics



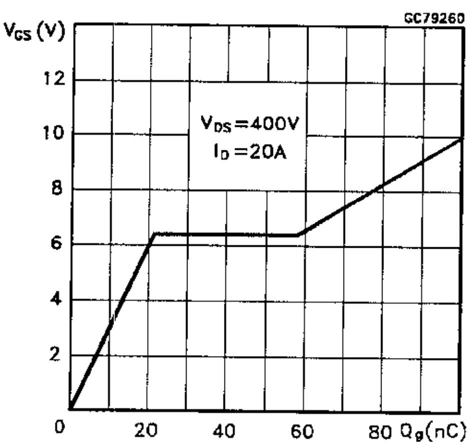
Transconductance



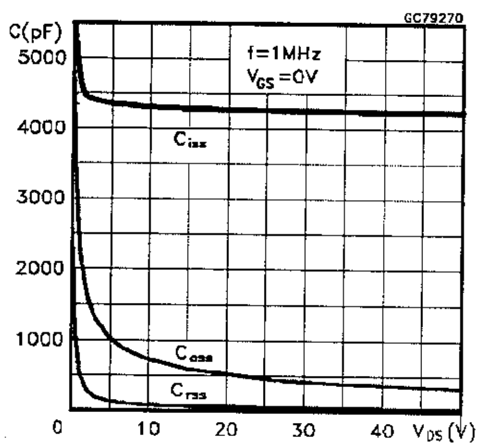
Static Drain-source On Resistance



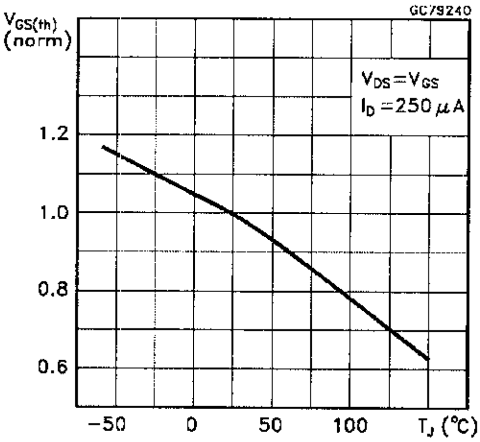
Gate Charge vs Gate-source Voltage



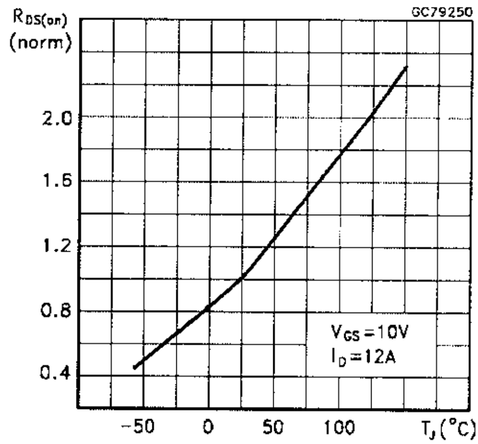
Capacitance Variations



Normalized Gate Threshold Voltage vs



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics