Position Control of Feeder Section in an Offset Printing Machine

PROJECT REPORT

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CHARACTER IS LIFE

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○ DTP ○ Computers ○ Softwares ○ Mini Offset ○ Services

[illegible]

TO WHOEVER IT MAY CONCERN

This is to certify that the following final [illegible] students from Department of Electrical and Electronics Engineering of Kumaraguru College of Technology, Coimbatore - 6.., as below have completed the project entitled **POSITION CONTROL OF FEEDER SECTION IN AN OFFSET PRINTING MACHINE** in our concern. The [illegible] is done with total satisfaction [illegible] regular and punctuality [illegible] the firm.

Name of the Students

1. Mr. V.Dhathathriyan
2. Mr. S.Sathish kumar
3. Mr. U.N.Srijith
4. Ms. V.P.Sudha

We are proud to have enthusiastic students [illegible] and their interest is shown in the [illegible] promotion of the above [illegible].

We wish them a grand success in [illegible].

For PERFECT SOFT SYSTEMS

S.Sundaresan
Chief Executive

Date : 20th March [illegible]

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SYNOPSIS

In the existing **SHEETFED MINI OFFSET PRINTING MACHINE** the movement of the paper tray is controlled using gearwheels and ratchets manually.This process is rather complicated and has the disadvantage of mechanical failure due to the mishandling by the operators. This requires frequent replacement of gearwheels and ratchets. To overcome this drawback, both commercially and technically,it is proposed to use a microprocessor controlled stepper motor in a closed loop mode. An eight bit microprocessor(8085A) is interfaced with a Programmable Peripheral Interface (8255 A) along with other additional hardware to control the motion of the stepper motor in both the directions i.e.,clockwise (upward movement) and anticlockwise (downward movement).A paper sensor is used as a feedback element.

In this project, interfacing circuit between microprocessor and programmable peripheral interface, drive circuit for the stepper motor are designed and fabricated. A program in assembly language is developed for the control of stepper motor using Microprocessor.

The whole system is tested and the test results are presented in this report.

CONTENTS

1.1 THE PRINTING MACHINE

MAST'R - THE MINI OFFSET PRINTING MACHINE is developed by PERFECT SOFT SYSTEMS. There are at present two models: MAST'R-1510 and MAST'R-1520.These two models differ on the basis of the maximum size of paper that can be printed.

1.1.1 DRIVE AND OPERATION OF THE MACHINE

The following controls are provided on the machine.

1. "MOTOR ON" and "MOTOR OFF" push switches for starting and stopping the D.C. motor.

2. "Speed Control"- Controlling the operating speed of the machine

3. Two "INCH" push switches are provided on the machine. These switches also act as Emergency stop switch.

4. "VACUUM ON" AND "VACUUM OFF" push switches to start and stop the vacuum pump in the machine. Extra "VACUUM STOP" switch is provided at the operating side of the feeder.

5. Electromagnetic counter system to count the number of sheets.

1.1.1a Control Panel :- The control panel incorporates following features.

- Field failure relay to remove motor power, in case field winding of the motor fails.
- Overcurrent limiting circuit breaker for the entire system.

- Non contacting long life magnetic / inductive proximity
- Switches for operating the sheet counter.

1.1.1b Variable Speed Control :-

The speed of the machine can be adjust using the "Speed Control Knob" to the required graduation. The speed can be varied from 0 to 6000 impressions per hour.

1.1.2 FEEDER SECTION

1.1.2a Centering the Sheet :-

The centering of the sheet is done by folding the sheet down the middle to locate the centre of the lead edge, and then place this crease directly under the detector finger. This should be done when the stop fingers are in towards paper, so that they are just touching the trailing edge of the sheet to avoid any bouncing back of the sheet during operation.

1.1.2b Lowering and Raising the Feeder Pile :-

Hold the crank with one hand and depress the elevator release lever with the other hand. Turn the handle counter clockwise to lower the elevator. The spring loading crank must be released to bypass the safety stop.

To raise the feeder, the elevator release lever is released and the handle is turned in the clockwise direction.

1.1.2c Paper Guides and Back Stop :-

In order to prevent the pile from moving away from the front stoppers, the back stop is set firmly against the back edge of the pile. The paper guides are used to hold the top of the pile exactly square with the pullover rolls so that the sheets being fed will enter on the conveyer table evenly

1.1.2d Paper Separator :-

If two sheets are picked up by the suction bar, it is the function of the paper separator to remove the second sheet. It is mounted directly below the suction bar.

1.1.3 SUCTION BAR and BLOWER TUBES :-

The purpose of the blower tubes is to introduce air between the top sheets of the pile and thus assist the sucket bar in lifting one sheet at a time. Each tube has three samll openings . The suction bar feeds the paper from the pile to the conveyer table.

1.1.4 CONVEYER TABLE :-

The conveyer table transports the paper from the feeder section to the printing section.

1.1.5 PRINTING SECTION

The printing section consists of INKING UNIT, DAMPENING UNIT and PRINTING UNIT

1.1.5a INKING UNIT:-

The inking unit of the machines consists of one fountain roller, one ductor roller, two distribiting rollers, one intermediate roller, one idler roller, one large vibrator roller and two form rollers.

1.1.5b DAMPENING UNIT:-

The dampening unit of consists of one fountain roller, one ductor roller, one distributor roller and one form roller

1.1.5c PRINTING UNIT :-

The printing unit has a master drum, image drum and printing drum. The MASTER ie; the material to be printed is fixed on the master drum. The dampening unit sprays water on the MASTER. The MASTER is weted with water on all the places except on places where there is an impression. These areas are dampened with ink. Now the image drum gets the image of the MASTER on it. The paper fixed on the printing drum takes the image from the image drum. This process of printing is konwn as **OFFSET PRINTING**

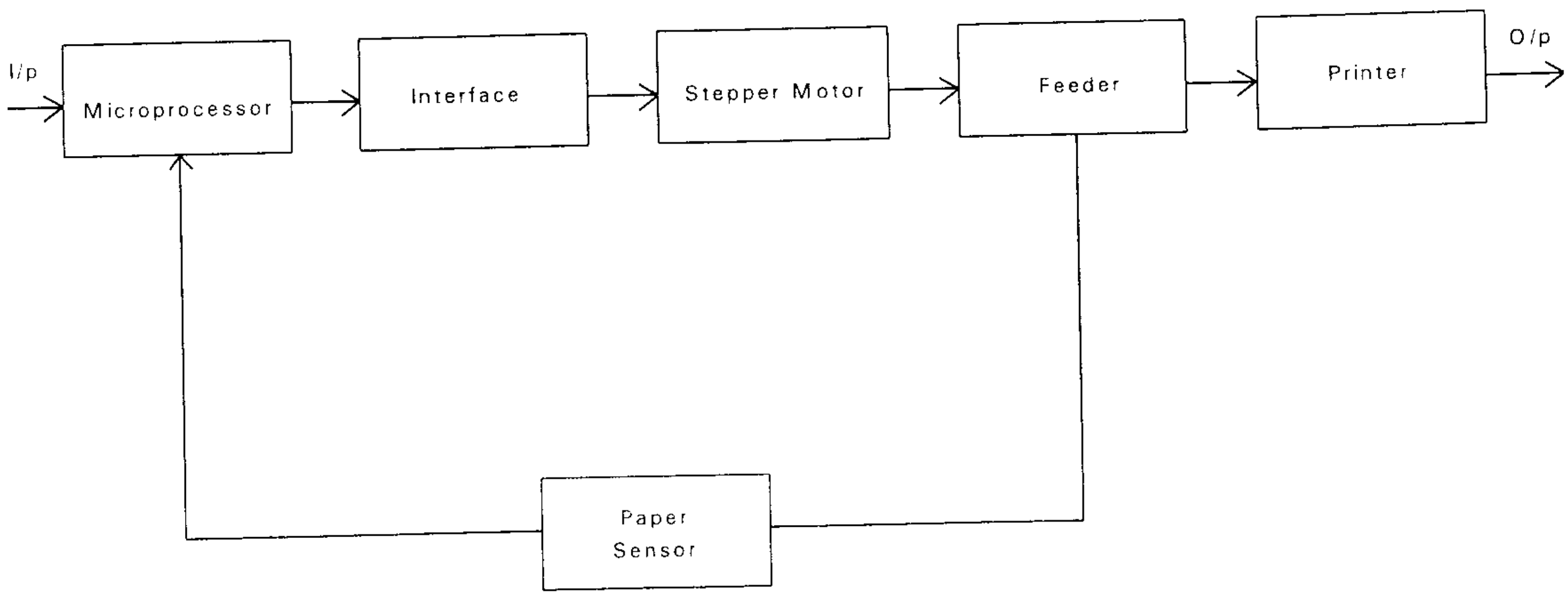


Fig. 1.2 - BASIC BLOCK DIAGRAM

1.2 BASIC BLOCK DIAGRAM DESCRIPTION

MICROPROCESSOR :

This is the brain of the entire system which includes the memory, peripheral interfacing chips, drivers and decoders. It co-ordinates the activities of the system.

INTERFACE :

This acts as a communication channel of the system through which the microprocessor controls the motion of the stepper motor in either direction.

STEPPER MOTOR :

The stepper motor plays a vital role in the movement of the tray. Since it is a continous duty operation, the selection of the motor is based on the load inertia and load torque.

FEEDER :

The paper is conveyed from the paper tray to the feeder by means of sucker bar and paper rollers.The sucker bar is connected to the suction stroke of a compressor.

PRINTER :

The feeder feeds paper to the printer which consist of ink rollers and image spread on a polymorse sheet.The printer impresses the image to the feeded paper.

SENSOR :

This is the feedback element of the system which senses for paper and gives feedback signal to the microprocessor, to maintain the constant paper level in the feeder.

2.1 INTRODUCTION

Since the advent of Microprocessor in the year 1971, the usage of microprocessor has multiplied to an extent that a revolutionary development in the Electronic Industry is presently observable. Microprocessor based system design and implementation results in many benefits as discussed below.

The Microprocessor is a " Programmable Logic Device" designed with registers, flip-flops and timing elements . With reference to the field of computers the term 'Microprocessor ' refers to the central processing unit of a small computer system. The Microprocessor is an electronic integrated circuit manufactured by using either a Large Scale (LSI) or Very Large Scale (VLSI) Technique. Although a microprocessor chip cannot function by itself, the addition of a few memories and I/O devices make a typical computer system.The Microprocessor has a set of instructions designed internally, to manipulate data and communicate with peripherals.

2.2 MERITS OF MICROPROCESSOR BASED SYSTEM DESIGN :

*** Cost of savings in hard ware :**

A single chip on LSI basis replaces several discrete logic gates resulting in the reduction of cost as well as the size of the system.

*** Reliability :**

As the number of discrete logic gates decreases the probability of malfunctioning decreases. This enhances the system performance.

*** Flexibility :**

To modify a system one has to merely reprogram the memory elements without redesigning.

*** Expandability :**

Additional interfaces can be added to the system bus and software can be suitably modified to cater to the system growth.

*** Speed :**

The speed at which the Microprocessor performs an operation makes it extremely useful in time controlled processes, where the time is the main criterion.

*** Compactness :**

As the single chip on LSI or VLSI replaces several discrete logic gates, the usage of that single chip greatly reduces the overall size of the system.

2.3 THE INTEL 8085A - MICROPROCESSOR ARCHITECTURE

The INTEL 8085A is an general purpose Microprocessor capable of addressing 64k 0f memory. The INTEL 8085A is a complete 8 bit parallel central processing unit (CPU) implemented in N-channel depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed.

The special features of the INTEL 8085A microprocessor are :

* Single +5 volts power supply with 10% voltage margins.
* Operate with a 3 MHz single phase clock.
* It is more than 50% faster than 8080A.
* 20% lower power consumption than 8080A.
* 100% software compatible with 8080A.
* On-chip clock generator (with external crystal,LC or RC network.
* Four vectored interrupt inputs (One is non maskable) plus an 8080A
- compatible Interrupt.
* serial in / serial out port.
* Decimal , binary and double precision arithmetic.
* Direct Addressing capability to 64k bytes of memory.

2.2.1 FUNCTIONAL DESCRIPTION :

The Figure 2.2.2 shows the logic pinout (functional) diagram of 8085A Microprocessor. All the signals can be classified into six groups:

(a) Address bus,

(b) Data bus ,

(c) Control and status signals,

(d) Power supply and frequency signals,

(e) Interrupts and peripheral initiated signals,

(f) Serial I/O ports.

(a) ADDRESS BUS :

The 8085A has eight signal lines, A15 - A8 which are unidirectional and used as the higher order Address Bus .

(b) MULTIPLEXED ADDRESS / DATA BUS :

The signal lines AD7 - AD0 are bidirectional, they serve a dual purpose. They are used as the lower order address bus as well as the data bus In executing an instruction, during the earlier part of the cycle, these lines are used as lower order address bus. During the later part of the cycle, these lines are used as the data bus.(This is known as Multiplexing the bus.) However the lower order address bus can be seperated from these signals by using a latch.

(c) CONTROL AND STATUS SIGNALS :

This group of signal includes two control signals (READ and WRITE), three status signals (INPUT OUTPUT / MEMORY,S1 and S0) to identify the nature of the operation , and one special signal (ALE) to indicate the beginning of the operation. The signals are as follows :

* ADDRESS LATCH ENABLE :

This is a positive going signal generated every time the 8085A begins an operation (machine cycle):It indicates that the bits on AD7 to AD0 are address bits . This signal is used primarily to latch the lower order address from the multiplexed bus and generate a seperate set of eight address lines.A7 to A0.

* READ :

This is a read control signal (active low). This signal indicates that the selected I/O are memory device to be read and data are available on the data bus.

* WRITE :

This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I O location.

* INPUT OUTPUT / MEMORY :

This is a status signal used to differentiate between I/O and memory operation. When it is high, it indicates an I/O operation;when it is low it indicates a memory operation.This signal is combined with READ and WRITE to generate I/O and control signals.

* S1 AND S0 :

These status signals, similar to INPUT OUTPUT/ MEMORY,can identify various operations, but they are rarely used in small systems.

(d) POWER SUPPLY AND CLOCK FREQUENCY :

The power supply and frequency are as follows.

* Vcc : +5 volt power supply.

* Vss : Ground Reference.

* X1,X2 : A crystal (or RC , LC network) is connected at these two pins.The frequency is divided by two ; therefore, to operate a system at 3MHz, the crystal should have frequency of 6MHz.

* CLK (OUT) - Clock output :

This signal can be used the system clock in other devices.

(e) INTERRUPTS AND EXTERNALLY INITIATED OPERATIONS :

The 8085A has five interrupt signals that can be used to interrupt a program execution.One of the signals, INTR(interrupt request), is identical to the 8080A Microprocessor interrupt signal (INT); others are enhancements to the 8080A. The microprocessor acknowledges an interrupt by the INTA (Interrupt Acknowledge) signal.

In addition to the interrupts, three pins - RESET, HOLD, and READY - accept the externally initiated signals as inputs. To respond to the HOLD request, it has one signal called HLDA (Hold Acknowledge).

* RESET IN :

When the signal on this pin goes low, the program counter is set to zero, the buses are tri-stated, and the MPU is reset.

* RESET OUT:

This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

(f) SERIAL I/O PORTS:

The 8085A has two signals to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data).

2.2.2 INTERNAL ARCHITECTURE OF INTEL 8085A :-

The internal architecture of 8085A includes the programmable register array,the ALU (arithmetic and logic unit), timing and control unit, instruction registers and decoder,interrupt control and serial I/O control as shown in fig. 2.2.1

ARITHMETIC AND LOGIC UNIT (ALU) .

The arithmetic and logic unit performs the computing functions: it includes the accumulator, the temporary register, the arithmetic and logic circuits and five flags.The temporary register is used to hold datas during arithmetic and logic operation. The result is stored in the accumulator, and the flags are set or reset according to the result of the operation.

The flags are afffected by the arithmetic anmd logic operation in the ALU. In most of these operations, the result is stored in the accumulator. Therefore, the flags generally reflect data conditions in the accumulator - with some exceptions.

* TIMING AND CONTROL UNIT :

This unit synchronizes all the microprocessor operations with the clock, and generates the control signals necessary for communication between the processor and peripherals.

* INSTRUCTION REGISTER AND DECODER :

The instruction register and the decoder are the part of the ALU. When an instruction is fetched from the memory it is loaded in the instruction register . The decoder decodes the instruction and establishes the sequence of events to follow. The instruction register is not programmable and cannot be accesed through any instruction.

* REGISTER ARRAY :

Apart from the programmable registers, two additional registers, called temporary registers W and Z, are included in the register array. These registers are used to hold 8 - bit data during the execution of some instruction. However since they are used internally, they are not avialable to the programmer.

2.3 THE 8255A PROGRAMABLE PHERIPHERAL INTERFACE

The 8255A - Programmable peripheral interface, is a widely used, programmable,parallel I/O device.It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versat le and economical. The logic pin out diagram is shown in fig. 2.3.1.

The special features of the INTEL 8255A - THE PROGRAMMABLE PERIPHERAL INTERFACE are :

* 24 Programmable I/O Pins
* Completely TTL compatible
* Fully compatible with intel Microprocessor families
* Direct bit set/reset capability easing control application interface
* Improved DC driving capability
* 40 Pin DIP package

2.3.1 FUNCTIONAL DESCRIPTION :

The 8255A has 24 I/O pins that can be grouped primarily into two 8 bit parallel ports: A & B, with the remaining 8 bits as port C . The 8 bits of port C used as individual bits or be grouped in two 4 bit ports : C Upper & C Lower. This device is like three 8212s with many more additional features. The function of these ports are defined by writing control word in the control register.

2.3.1A OPERATING MODES :

All the functions of the 8255A can be classified into two major modes namely Bit set / reset mode and the I/O mode.The Bit set / reset mode is used to set or reset the bits in port C. Under I/O mode. there are three major modes of operation namely Mode 0, Mode 1 and Mode 2.

MODE 0 (BASIC INPUT OR OUTPUT) :

This functional configuration provides simple input and output operations for each of three ports.Data is simply read from or written to a specified port.

Basic functional definitions :

* Two 8 bit ports and two 4 bit ports.
* Any port can be input or output.
* Outputs are latched.
* Inputs are not latched.
* 16 different input / output configurations are possible.

MODE 1 (STROBED INPUT OR OUTPUT) :

This functional configuration provides a means for transferring I/O data to or from a specified port in conjuction with strobes or " Handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these " handshaking" signals.

Basic functional definition :

* Two Groups (Group A and Group B)

* Each group contains one 8 bit data port and one 4 bit control or data port.

* The 8 bit data port can be either input or output. Both inputs and outputs are latched.

* The 4 bit port is used for control and status of the 8 bit data port.

MODE 2 (STROBED BIDIRECTIONAL BUS INPUT OR OUTPUT) :

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8 bit bus for both transmitting and recieving data.The "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to mode 1. Interrupt generation and enable or disable functions are also avialable.

Basic functional definitions :

* Used in group A only.

* One 8 bit, bidirectional bus port (port A) and a 5 bit control port (port C).

* Both inputs and outputs are latched.

* The 5 bit port (port C) is used for control and status for the 8 bit, bidirectional bus port(port A).

2.3.1B CONTROL LOGIC :

The control section has six lines. Their functions and connections are as follows:

(1) READ :

This control signal enables the read operation. When the signal is low, the MPU reads data from a selected I/O port of the 8255A.

(2) WRITE :

This control signal enables the write operation. When the goes low, the MPU writes into a selected I/O port or the control register .

(3) RESET :

This is an active high signal; it clears the control register and sets all ports in the input mode.

(4) CHIP SELECT, A0 AND A1 :

These are device select signals. Chip select is connected to a decoded address and A0 and A1 are generally conected to MPU address lines A0 and A1, respectively.

The chip select signal is the master chip select, and A0 and A1 specify one of the input and output ports or the control register as given below:

CS	A1	A0	SELECTED
CS	A1	A0	SELECTED
CS	A1	A0	SELECTED

0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	CONTROL REGISTER
1	X	X	8255A is NOT SELECTED

The port addresses are determined by the CS, A0 and A1 lines. The chip select line goes low when A7 = 1 and A6 through A2 are at logic 0.When these signals are combined with A0 and A1, the port addresses range from 80H to 83H , as shown in the figure.

CONTROL WORD :

Figure shows a register called the CONTROL REGISTER. The contents of the register, called the control word, specify an I/O function for each port. This register can be accessed to write a control word when A0 and A1 are at logic 1. the register is not accessible for a read operation.

To Communicate with peripherals through the 8255, three steps are necessary

(1) Determine the address of port A,B,and C and of control Register according to the chip select logic and address lines A0 and A1.

(2) Write the control word in the control register.

(3) Write instructions to communicate with peripherals through ports A, B, and C.

2.4 THE INTEL 2732 - UV ERASABLE PROM

The INTEL 2732 is a 32,768 (4K * 8) bit ultraviolet erasable and electrically programmable read only memory (EPROM). The 2732 operates from a single +5 volt power supply, has a stand by mode. and features an output enable control.The total programming time for all bits is 210 seconds. All these features make designing with the 2732 in microcomputer system faster, easier and more economical. The logic pin out diagram is shown in fig. 2.4.1.

The special features of the INTEL 2732 - ERASABLE PROGRAMMABLE READ ONLY MEMORY are :

* Fast access time
  - 450 nano seconds Max. 2732
  - 550 nano seconds Max. 2732 - 6
* Single +5 volt +/- 5% power supply.
* Low power dissipation :
  - 150 mA Max. Active current
  - 30 mA Max. standby current
* Pin compatible to INTEL 2716 EPROM
* Completely static
* Simple programming requirements
  - single location programming
  - programs with one 50 mS pulse
* Three state output for direct bus interface

An important 2732 feature is the seperate output control, output enable from the chip enable control.The OUTPUT ENABLE control eliminates bus contention in multiple bus microprocessor systems.

The 2732 has a standby mode which reduces the power dissipation without increasing accesss time. The maximum active current is 150 mA, while the maximum standby current is only 30 mA, an 80% savings.The standby mode is achieved by applying a TTL high to the CHIP ENABLE input.

2.5 THE INTEL 8212 - 8 BIT INPUT / OUTPUT PORT

The INTEL 8212 input/output port consists of an 8 bit latch with 3 state output buffers along with control and device selection logic. Also included is a service request flip flop for the generation and control of interrupts to the micro processor. The logic pin out diagram is shown in fig. 2.5.1.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers . Thus, all of the principal peripheral and input output functions of a microcomputer system can be implemented with this device.

The special features of the INTEL 8212 - INPUT OUTPUT LATCH are

* Fully parallel 8 bit data register and buffer.
* Service request flip-flop for interrupt generation.
* Low input load current - 0.25 mA Max.
* Three state outputs
* Output sink 15 mA
* 3.65 volt Output high voltage for Direct interface to 8085A CPU

* Asynchronous register clear

* Replaces buffers, latches and multiplexers in microcomputer systems.

2.5.1 FUNCTIONAL DESCRIPTION :

DATA LATCH :

The 8 flip - flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high.Latching will occur when the clock (C) returns low.

OUTPUT BUFFER :

The outputs of the data latch (Q) are connected to 3 state, non-inverting output buffers. These buffers have a common control line (EN):this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer,forcing the output into a high impedance state.(Tristate)

CONTROL LOGIC :

The 8212 has control inputs DS 1 , DS 2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop .

2.6 TEXAS 74LS138 - DECODERS / DEMULTIPLEXERS

The 74LS138 Decoder accepts three binary weighted inputs (A0, A1, A2) and when enable, provides eight mutually exclusive, active LOW outputs The device features three enable inputs: two active low and one active high.

Every output will be high unless the two active low inputs are low and the active high signal is high.

The device can be used as an eight output demultiplexer by using one of the active low enable inputs as the data input and the remaining enable inputs as strobes. Enable inputs not used must be permanently tied to their active high or avtive low state.

The special features of the TEXAS 74LS238 - DECODERS DEMULTIPLEXERS are :

* Demultiplexing capability.
* Multiple input enable for easy expansion.
* Ideal for memory chip select decoding.
* Direct replacement for INTEL 3205.
* Requires +5 volt for its operation.

2.7 TEXAS 74LS245 - OCTAL TRANSCIEVER

The 74LS245 is an octal transciever featuring non-inverting tristate bus copatible output in both send and recieve irections. The outputs are all capable of sinking 24 mA and sourcing upto 15mA producing very good capacitive drive characteristics. The device features a chip enable (CE) input for easy cascading and a send / recieve (S/R) input for direction control. The logic pin out diagram is shown in fig. 2.7.1.

All data inputs have hysteresis built in to minimize AC noise effects.

The special features of the TEXAS 74LS245 - OCTAL TRANSCIEVER are :

* Octal bidirectional bus interface.
* Tristate buffer outputs.
* PNP inputs for reduced loading.
* Hysteresis on all data inputs.
* Requires +5 volt for its operation.

2.8 TEXAS 74LS244 - OCTAL LINE DRIVER

The octal buffer 74LS244 is a tristate buffer. It is also known as LINE DRIVER or LINE RECIEVER.This device is commonly used as a driver for the address bus in a bus oriented system.It consists of two groups of four buffers with noninverted tristate output.The buffers are controlled by two active low enable lines. Until these lines are enabled, the output of the driver remains in the high impedance state. Each buffer is capable of sinking 24mA and sourcing 15 mA of current. The logic pin out diagram is shown in fig. 2.7.2.

The special features of the **TEXAS 74LS244 - OCTAL LINE DRIVER** are :

* Octal unidirectional bus interface.
* Tristate buffer outputs.
* Hysteresis on all data inputs.
* Requires +5 volt for its operation.

3.1 INTRODUCTION

Conventional Direct Current Electric motors provide a mechanical output in the form of a continous, smooth rotation. Speed and direction are easly controlled. If precise control of rotational position is required with a dc motor then it is almost essential to provide some form of feedback from the shaft which can be used to sense its position and adjust the supply to it accordingly. This arrangement is known as a servo system and systems are commonplace in position control systems.

Stepper motors offer a completely different approach to the problem of controlling position as they are designed to produce a machanical output which will respond to a command signal by rotating in discrete increments or "steps" rather than the smooth, spinning motion of their dc counterparts. The direction and number of these steps canbe controlled by applying appropriate pulses to the stator windings of the motor.

The stepper motor is essentialy a device that converts input ionformation in digital form to a mechanical output, thereby providing a natural interface with the digital computer.Though the stepper motor is driven by a properly sequenced set of digital, the motor itself has the characteristics of a synchronous motor.

3.1.1 What is a stepper motor ?

A Stepper Motor is a special electric motor which is given with DC (Direct Current) to stator windings, generates rotating power by drawing a rotor with electromagnetic force produced therein and goes on rotating in stepwise at designated angle (step angle) by changing over stator windings which current. This is also called as a PULSE MOTOR or a STEPPING MOTOR.

3.1.2 Classification of stepper motor :

(1) According to type of motion :

(a) Linear stepper motor.

(b) Rotary stepper motor.

(2) According to type of rotor construction :

(a) Variable reluctance type.

(i) Distributed winding type.

(ii) Multiple stack type.

(b) Permanent magnet type.

(i) 2 - Pole type.

(ii) Multi - pole type.

(c) Hybrid type.

(3) According to the number of phases to be excited :

(a) Single phase excitation.

(b) Two - phase excitation.

(c) Half - step excitation.

3.1.3 The Characteristics of Stepper Motor :

Stepper motors are driven by a device to excite stator windings in the specified sequence. Connect the motor with this kind of driving unit and provide input pulse signals. The rotor will rotate through a fixed angle and stay at rest until the next pulse is provided. If input are given in a sequence, the rotor will rotate with a stepped motion. The constructional diagram is shown in fig. 3.1.1.

The degree of precision to which the motor shaft may be positioned depends upon the number of steps per revolution of the rotor. Many stepper motors offer a resolution of 200 steps, that is, the shaft may be positioned in 1.8 degree steps. It is, in fact, possible to achieve 0.9 degree resolution with such a motor by a technique known as "Half step excitation".

Because the input signal is usually given in pulses, the aggregate rotation angle of the output shaft is proportional with the total number of input pulses and the rotation speed is proportional with the frequency of input pulses

(1) Rotation angle is proportional with the number of input pulses.

(2) Rotation speed is proportional with the frequency of input pulses.

(3) Without receiving an input signal the rotor keeps the same position at rest.

(4) The motor is capable of immediate stop.

The characteristics of the stepper motor vary widely depending on the driving system.

3.1.4 Closed loop drive :

The performance of a stepper motor is limited in the open loop drive systems because of disadvantages such as unstable performance due to vibration, possible step out depending on the relation between response frequency and load inertia. A closed loop drive is designed to overcome these drawbacks.

3.1.5 Checking points in selection of stepper motor :

The following factors are to be considered to select a stepper motor :

(1) Actual Load torque.

(2) Load Inertia (in terms of motor shaft)

(3) The maximum frequency to be applied.

3.1.6 Advantages :

(1) Smaller size

(2) Lower cost

(3) Light weight

(4) High torque capability

(5) High rotor inertia

3.1.7 Applications :

(1) For carriage transport and paper feeding of printers.

(2) To drive the head of hard and floppy disks.

(3) For card feeding of card machines.

(4) For paper feeding of facsimiles.

(5) To drive the tape of reading machines.

(6) For positioning of photo typesetters.

(7) To set pages in copiers.

(8) For X Y axle drive of plotters.

(9) For carriage transport and paper feeding of a printer of a calculator.

(10) For X Y axle drive of machine tools.

(11) Semiconductor manufacturing equipment

3.1.8 GLOSSARY

Since special terms are used about the stepper motor they are defined below with reference to characteristic curves.

(1) HOLDING TORQUE :

The maximum static torque that occurs when the rated current is provided to each phase to give an angular displacement to the motor shaft at the rest position.If the amount of external torque is smaller than the holding torque, the shaft returns to the original position when the external torque is removed

(2) STARTING CHARACTERISTICS :

The relation between the input pulse and the maximum torque that can be applied to the shaft when each step corresponds to each input pulse.

(3) MAXIMUM STARTING PULSE RATE :

The maximum frequency that can be applied to the shaft of an unexcited motor when each step corresponds to each input pulse.

(4) SLEWING CHARACTERISTICS :

After starting a motor in the self starting characteristic range, the pulse frequency is gradually increased. The relation between the frictional load torque and the maximum pulse frequency with which the motor can synchronize is called slewing characteristic.

(5) MAXIMUM SLEWING PULSE RATE :

The maximum frequency with which the motor can synchronize with the pulse train after an unloaded stepper motor starts with a frequency below the maximum starting pulse rate and enters the slewing characteristic range.

3.2 STEPPER MOTOR INTERFACING

Interfacing is necessary to control the stepping motion ofthe stepper motor through the microprocessor. The current requirements of the stepper motor, in any case, will be considerable and a TTL / Power interface board is required to interface the motor to the microprocessor user port.

The circuit diagram of the TRANSISTOR - TRANSISTOR LOGIC (TTL) / Power interface for stepper motor is shownin the figure 3.2.1.

The TTL level control pulses are applied to the bases of TR1, TR3, TR5, TR7 which form DARLINGTON pairs with the power driver transistor TR2, TR4, TR6, TR8. The collectors of these are connected to directly to the motor phases so that current in them may be turned ON and OFF.

Diodes D1, D2, D3 and D4 afford protection against damage to the darlington pairs by the back emf across the winding at current switch OFF.

A low value resistor is normally included in the power supply to the phases in order to decrease the electical inertia of the highly inductive windings. this permits a more rapid increase of current at swith ON and hence gives faster startup characteristics.

In this application the stepper motor has four coils, but only two of these have current flowing through them at a particular time. The stepper motor will move from one fixed position to another by applying pulses to the driver port in the correct sequence.

Table 3.2.1

CLOCKWISE ROTATION

STEP NO:	OUTPUT TO DRIVERS			
	0	1	2	3
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1
4	0	1	1	0
1	1	1	0	0

Table 3.2.2

ANTICLOCKWISE ROTATION

STEP NO:	OUTPUT TO DRIVERS			
	0	1	2	3
1	1	1	0	0
2	1	0	0	1
3	0	0	1	1
4	0	1	1	0
1	1	1	0	0

The generation of these pulse sequences and their application to the stepper motor can be achieved by a SOFTWARE SYSTEM.

4.1 LOAD CALCULATIONS

4.1.1 CALCULATION OF LOAD INERTIA WHEN THE MOTOR IS LIFTING AN

OBJECT :

$$J = 3.1415 \times (p/32) \times L \times \{(D1)^4 - (D2)^4 \} + (m/4)(D1)^2$$

Where .,

J - Load inertia in kg-sqcm

p - specific gravity of the pulley in kg/cubic cm

For steel p = 0.00786 kg/cubic cm

For aluminium p = 0.00269 kg/cubic cm

L - Width of the sprocket (pulley) in cm

D1- Outer dia of the sprocket (pulley) in cm

D2- Outer dia of the motor shaft in cm

m - Mass to be lifted in kg

Here we are using mild steel sprockets to withstand wear and tear and the size of the (outer diameter) of the sprocket is limited to 35 mm i.e., 3.5 cms.The width of the sprocket will be around 5 mm i.e., 0.5 cm.The motor shaft's outer dia is 16 mm as given in the drawing.The total mass to be lifted is approximately around 60 kgs which includes the tray weight along with paper fully mounted.With these data the load inertia is found to be :

J = 3.14 x (.00786/32) x 0.5 x {150.0625 - 6.5536} + 60/4 * 12.25

J = 1.701446 + 183.75

J = 185.451446 kg-sqcm

4.1.2 CALCULATION OF LOAD TORQUE AND TORQUE REQUIREMENT OF THE

STEPPER MOTOR :

T = W x D1 /200 N-m

Where .,

T - Load torque in Newton - metre

W - Weight of the load in Newton

D1 - Outer dia of the sprocket in cm

Conversion factor : 1 kgf = 9.8 N

Therefore 60 kgf = 588 N

Outer diameter of the sprocket = 0.035 m

therefore the load torque ic calculated as,

T = 588 x 3.5 /200

T = 2058/200

T = 10.29 N-m

Hence the requirement of the stepper motor is found to be load torque with 10.5 N-m (app) and load inertia with 185.5 Kg-sqcm(app). We are supposed to buy the motor from System controls, Bangalore., who are the dealers of step-syn stepping motors manufactured by SANYO DENKI CO., LTD., TOKYO,JAPAN.

The model number of the motor which suits our requirement is 103H89223-5241 (5211) which is a two phase type and uses bipolar drive method with ratings are as follows,

Basic step angle = 2.8 deg

Rated phase current = 6 Amps

Holding torque = 12 N-m

Rotor inertia = 14.6 Kg sqcm

Motor weight = 7.5 Kg

4.2 HARDWARE DESIGN

The hardware design is divided into the following subsystems:

(1) 8085A - based MPU and its bus architecture

(2) EPROM Memory

(3) Frequency and power requirements

(4) Externally triggered signals (Interrupts,Reset)

(5) Input and output (stepper motor control)

(6) Feedback element

(7) Drive ciruit.

4.2.1 8085A - BASED MPU AND ITS BUS ARCHITECTURE :

The buses of the 8085A (both address bus and data bus) have less driving capacity to meet our requirement hence the buses need more driving capacity than that of 8085A Microprocessor. Similarly peripherals specially designed to be compatible with 8085A are not used here and hence the lower order address bus must be demultiplexed and I/O and memory related control signals must be generated.

ADDRESS BUS :

The 74LS244, an octal bus driver used with the high order address bus to increase its driving capacity. the low-order address bus is demultiplexed by using the ALE signal and the 8212 as a latch.

DATA BUS :

The 74LS245,an 8 - bit bidirectional bus driver is used to increase the driving capacity of the data bus.This has 8 bidirectional data lines : the direction of the data flow is determined by the direction control line (DIR).

CONTROL BUS :

The 8085A generates three signals IO/MEMORY ,READ and WRITE .The IO/MEMORY signal differentiates between I/O and memory functions. By combining IO/MEMORY with READ and WRITE signals,appropriate control signals can be generated.

4.2.2 EPROM MEMORY :

The 2732 ,32K UV ERASABLE PROM is used to store the assembly Language program for controlling the stepper motors rotation. The 74LS138 is used to generate the chip select signal by using the address lines. A15 - A11 .

4.2.3 FREQUENCY AND POWER REQUIREMENTS :

The 8085A can operate with a maximum clock frequency of 3 MHz. The 8085A has two clock inputs : X1 and X2 . These inputs is driven with a crystal.

The 8085A and other components used in this system require a power supply of +5volts. The MPU and the memory components of the system require less than 400 mA.

4.2.4 EXTERNAL TRIGGERED SIGNALS :

The 8085A has four external input signals: RESET, INTERRUPT , READY and HALT. Of these signals, the RESET and INTERRUPT is used, the other two pins are grounded.

RESET :

The RESET IN is an active low signal used to reset the system. When this pin goes low,the program counter is set to zero, the interupt enable and HLDA flipflops are reset.

INTERRUPT:

The 8085A has five interrupt signals: TRAP,RST 7.5, RST 6.5,RST 5.5 and INTR .Since TRAP and INTR are not used, these are grounded. The RST 7.5 pin is connected to the lower limit switch. The RST 6.5 pin is connected to the upper limit switch. The RST 5.5 is connected to the capacitive proximity switch (PAPER SENSOR).

4.2.5 INPUT AND OUTPUT :

The inputs to this control system are the signals from the capacitive proximity switch,the upper and lower limit switches. The output of this system is in the form of angular motion of the stepper motor.

4.2.6 FEEDBACK ELEMENT :

The hardware design of this project forms a closed loop system in which the capacitive proximity switch(paper sensor) acts as a feedback element. The output of the proximity switch is trimmed by a trimmer circuit to give an output of 5 volt (approximately).This 5 volt signal is given to the RST 5.5 (PIN No: 9) of 8085A.This initiates the Microprocessor to give discrete pulses to the stepper motor through the 8255A, the programmable peripheral interface.

4.2.7 DRIVE CIRCUIT :

Since the Microprocessor cannot supply the current required by the stepper motor, a seperate drive circuit is designed and implemented to drive the stepper motor.The drive circuit consist of power transistors connected in darlington mode for each phase, to provide sufficient currrent gain. A feedback diode is connected to afford protection against damage to darlington pairs by the back emf across the winding at current switch OFF. The complete hardware circuitry is shown in fig. 4.2.1.

4.3 SOFTWARE DEVELOPEMENT

The software has three interrupt routine .In the main routine the processor is made to execute a dummy loop when the processor has no work .When an interrupt signal is received the processor, recogonises the interrupt and executes the interrupt routine .The three interrupts used in this project are RST 7.5.RST 6.5 and RST 5.5. Here RST 7.5 is given the highest priority hence it is used to stop the system on the reception of signal from the lower limit switch.The next priority is given to RST 6.5, so it is used to reverse the motion of the feeder tray on the reception of signal from the upper limit switch.The RST 5.5 is used for initiating the upward motion of the feeder tray when the capacitive proximity switch sends a signal.

Apart from these another routine is written to hang the system for some other work in the printing machine. The software flow chart is shown in fig 4.3.1 and the program is written in assembly language.

4.3 PROGRAM TO CONTROL STEPPER MOTOR

Address	Mnemonic	Operand	Opcode	Comment
	ORG	0000H	00, 00	Address org
	JMP	6000	C3, 00, 60	Jump to start
	ORG	003CH	3C, 00	Interrupt 7.5
6001	JMP	6300	C3, 00, 63	Jump to Stop
	ORG	0034H	34, 00	Interrupt 6.5
6004	JMP	6100	C3, 00, 61	Jump to Reverse
6007	RET	6000	C9, 00, 60	Return to start
	ORG	02CH	2C, 00	Interrupt 5.5
600A	JMP	6200	C3, 00, 62	Jump to Clockwise
600D	RET	6000	C9, 00, 60	Return to start
6000	JMP	6000	C3	Jump to start
6100	DI		F3	Disable Interrupt
	MVI	A, 80H	3E, 80	Get control word
	OUT	A	D3	Out control word
	MVI	A, 00H	3E, 00	Load Acc low
	OUT	A	D3	Out Acc
6107	MVI	A, OAH	3E, 0A	Load Acc width
	DCR	A	3D	Decrement
	JNZ	6107 H	C2, 07, 61	Jump on no zero
610D	MVI	A, FF H	3E, FF	Load Acc high
	OUT	A	B3	Out Acc.
	MVI	A, OAH	3E, 0A	Load Acc width
	DCR	A	3D	Decrement
	JNZ	610D	C2, 0D, 61	Jump no zero
	RET	6007	C9, 07, 60	Return to main
	EI		FB	Enable Interrupts
6200	DI		F3	Disable Interrupt
	MVI	A, 80H	3E, 80	Get control word
	OUT	A	D3	Out control word

	MVI	A, FFH	3E, FF	Load Acc High
	OUT	A	D3	Out Acc.
6207	MVI	A, OAH	3E, OA	Load Acc width
	DCR	A	3D	Decrement
	JNZ	6207	C2, 07, 62	Jump on no zero
	MVI	A, 00H	3E, OO	Load Acc Low
	OUT	A	D3	Out Acc
6211	MVI	A, OAH	3E, OA	Load Acc width
	DCR	A	3D	Decrement
	JNZ	6211	C2, 11, 62	Jump on no zero
	RET	600D	C9, 0D, 60	Return to main
	EI		FB	Enable Interrupt
6300	HLT		76	Halt

CONCLUSION

In this project, a system using a microprocessor controlled stepper motor has been designed to control the movement of the feeder tray in a **SHEETFED OFFSET PRINTING MACHINE**.Once the paper has been fully loaded in the tray, it is necessary to push the **START** push button to start the system operation.Then the movement of the tray in both direction is controlled by closed loop control in which the paper sensor i.e.,the capacitive proximity switch acts as a feedback element.After the tray has been emptied i.e., the printing process is over the system comes to rest and enters into a wait state.The entire system can be switched OFF by pushing the **STOP** push button. The interfacing circuits and drive circuits, designed and fabricated are working as per the design.

The developed system has the following advantages over the existing system

- The complicated system of gearwheels and ratchets have been eliminated
- The system can be hanged ,without having to shut down the machine
- The usage of stepper motor has enabled the precise movement of the feeder tray.

5.1 FURTHER DEVELOPMENTS

In the printing process the quality of the output depends on the perfect centering of the paper. In the machine the paper is being centered manually by trial and error method. At present in machines made in Germany and other developed countries they are using a special type of sensor called the REGISTERATION SENSOR used for sensing the regesteration mark on the MASTER. If the paper is not centered properly, then the sensor will give a signal to hang the system. These modifications can be incorporated in the system developed, as further development.

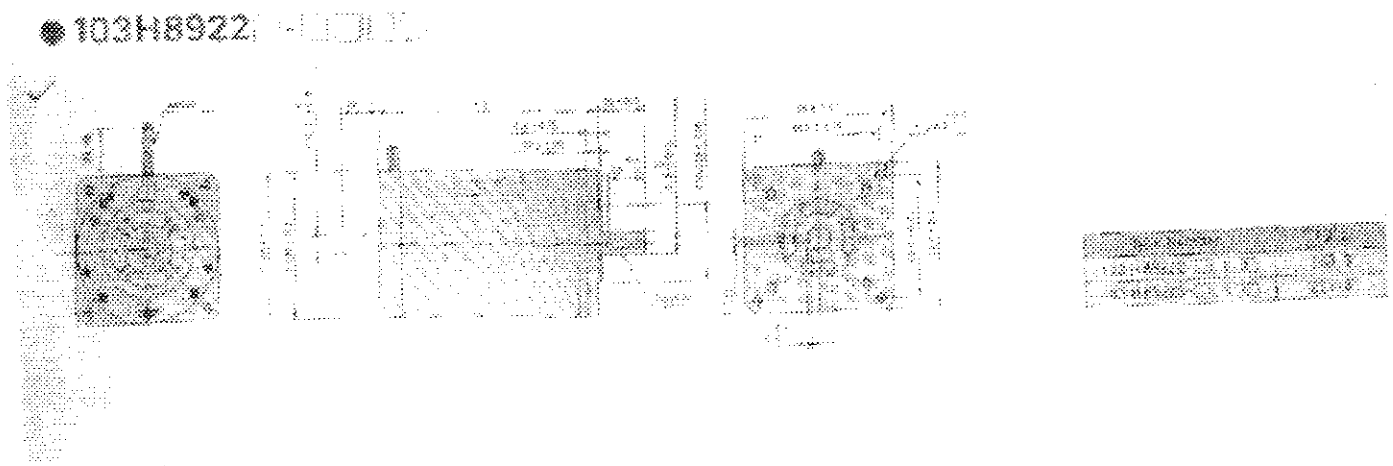


Fig. 3.1.1 - Constructional Details of Stepper Motor

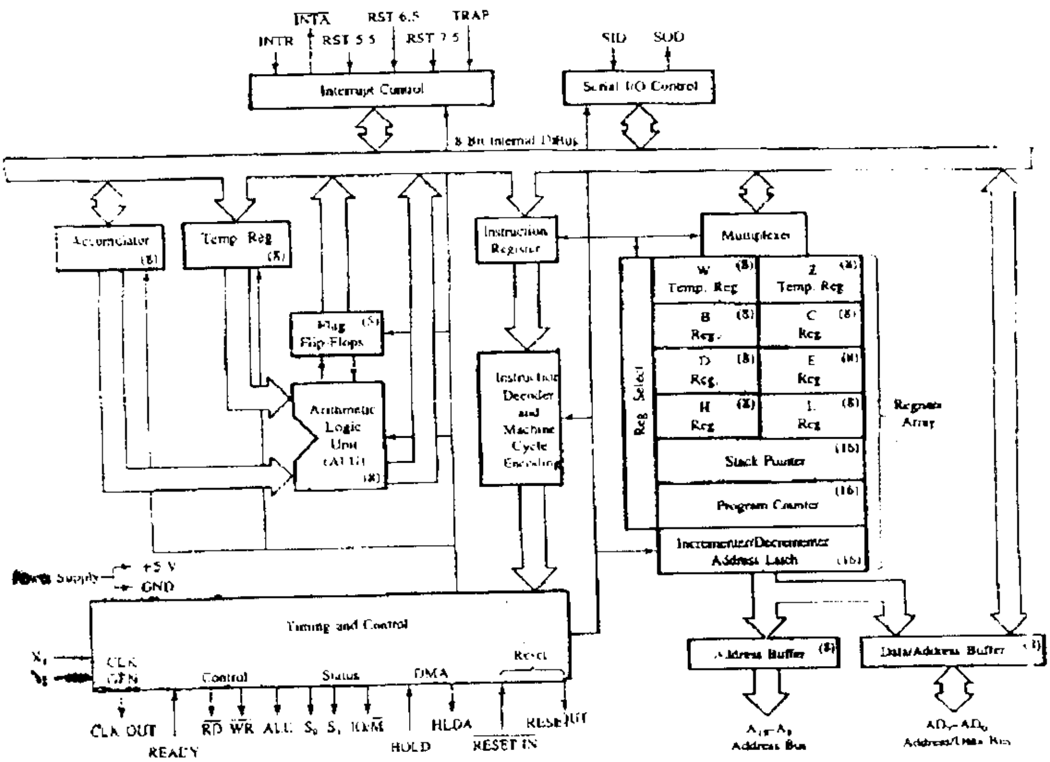


Fig. 2.2.1 - Internal Architecture of 8085A

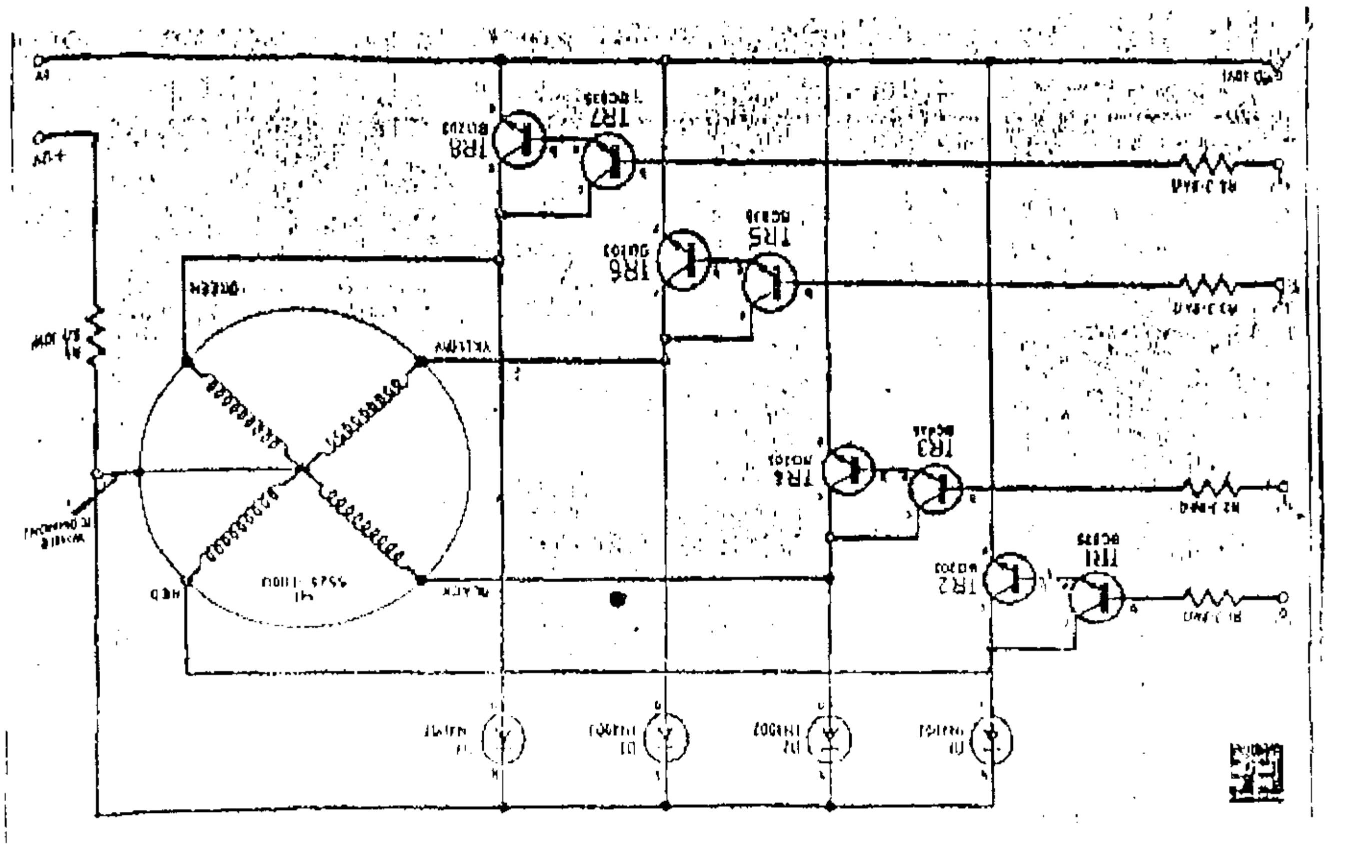
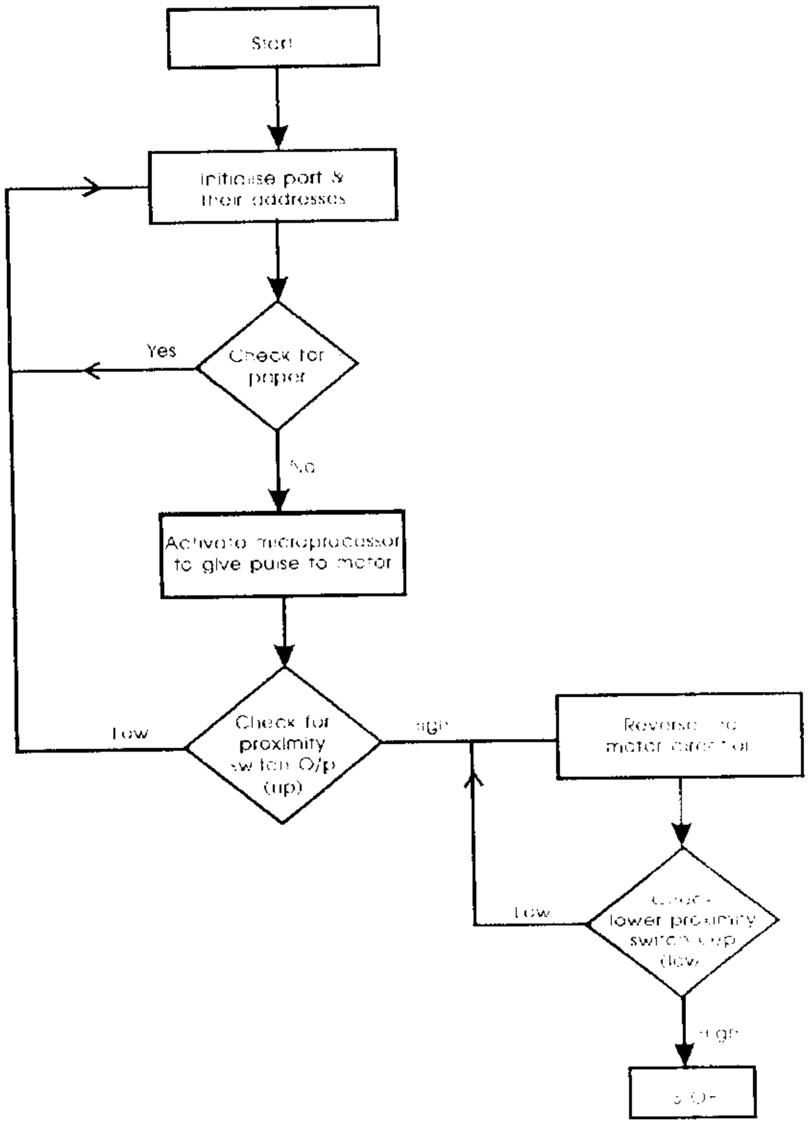


Fig. 3.2.1 - Interfacing Circuitry for Stepper Motor

4.3.2 FLOW CHART



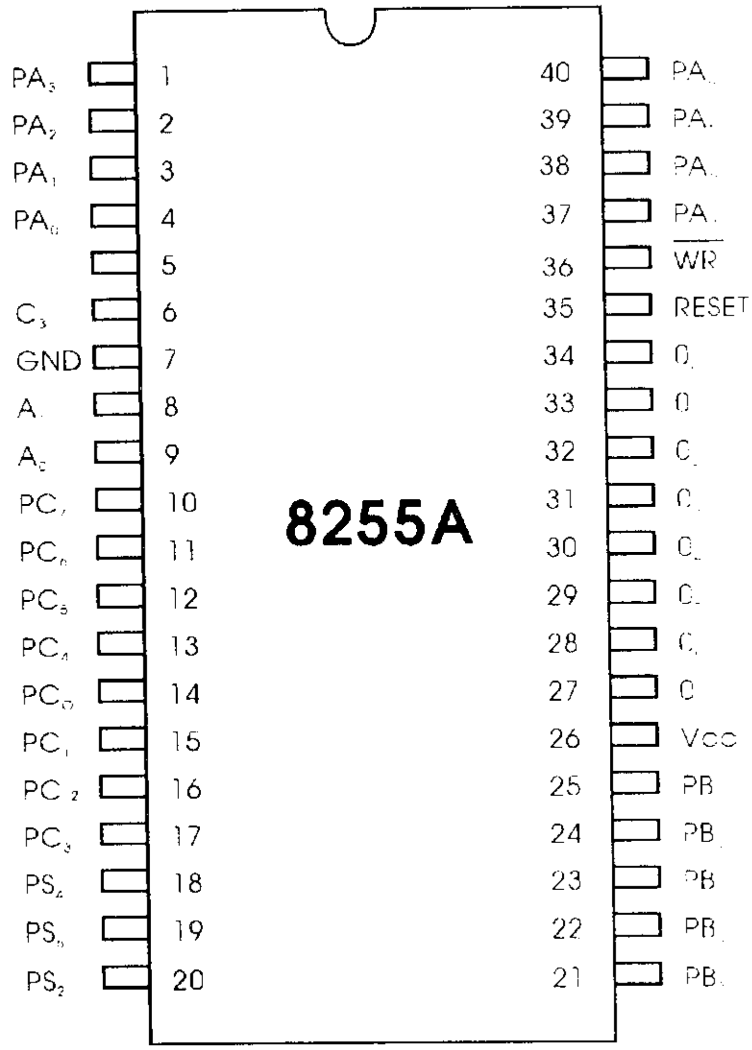


Fig. 2.3.1 PIN OUT DIAGRAM OF 8255A
(Programmable peripheral Interface)

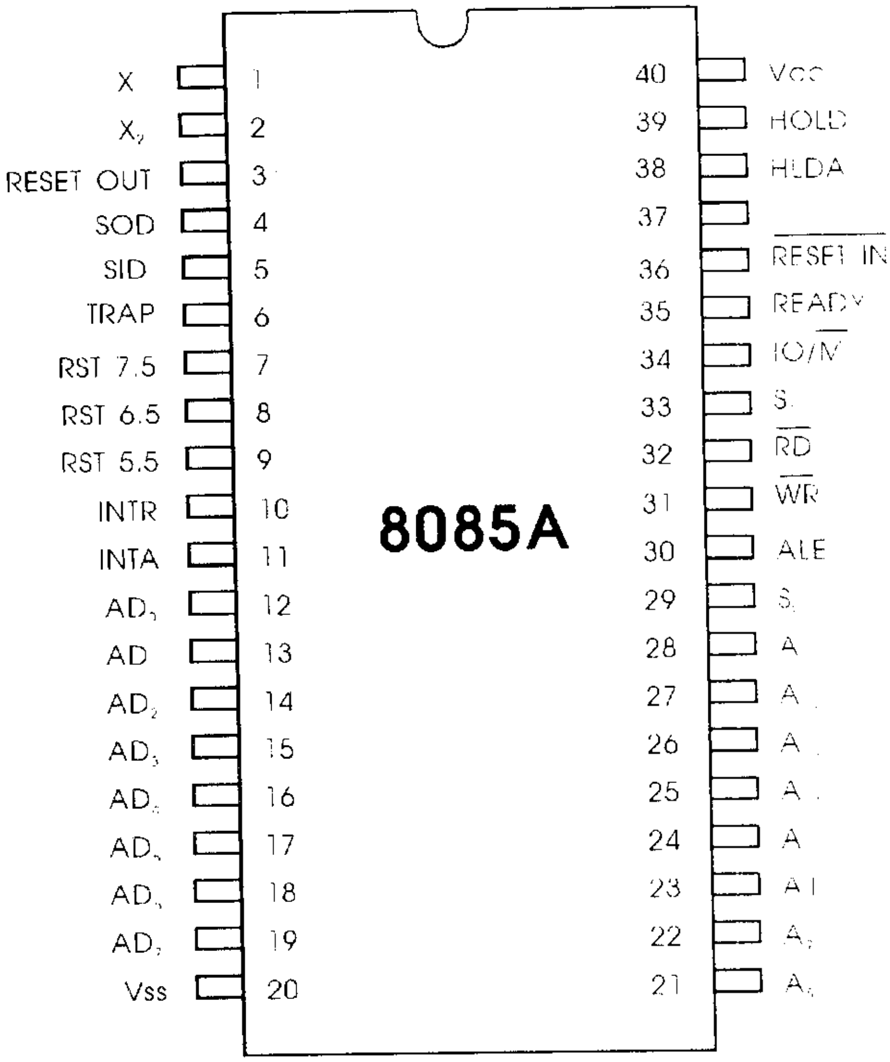


Fig. 2.2.2 PIN OUT DIAGRAM OF 8085A

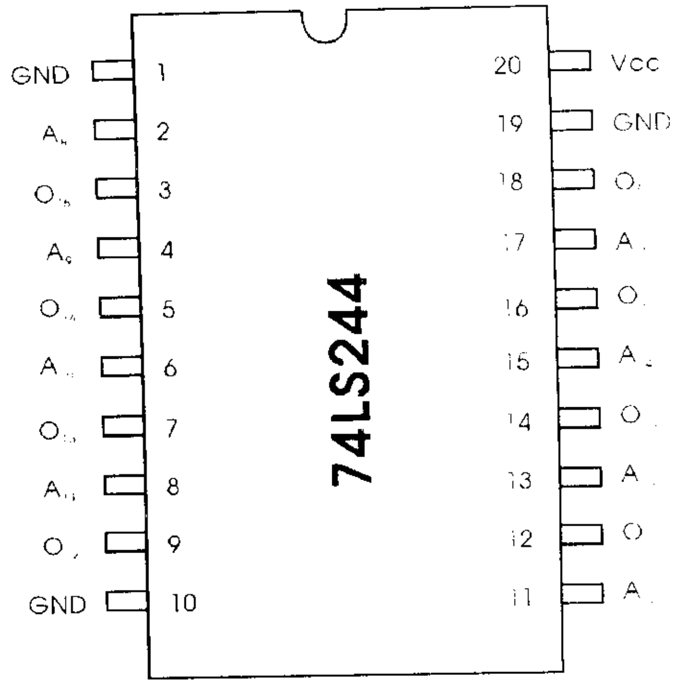


Fig. 2.7.1 PIN OUT DIAGRAM OF BUS DRIVER

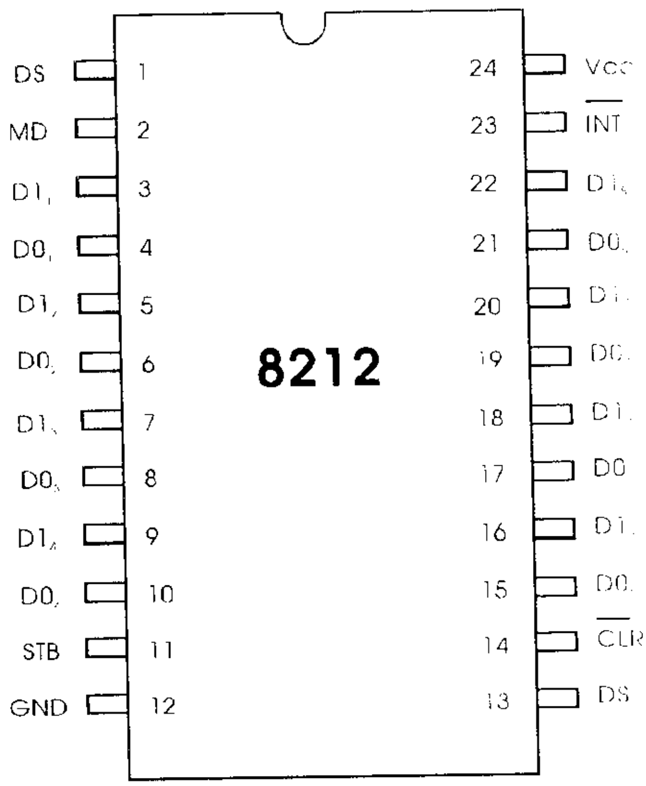


Fig. 2.5.1 PIN OUT DIAGRAM OF 8212 - LATCH

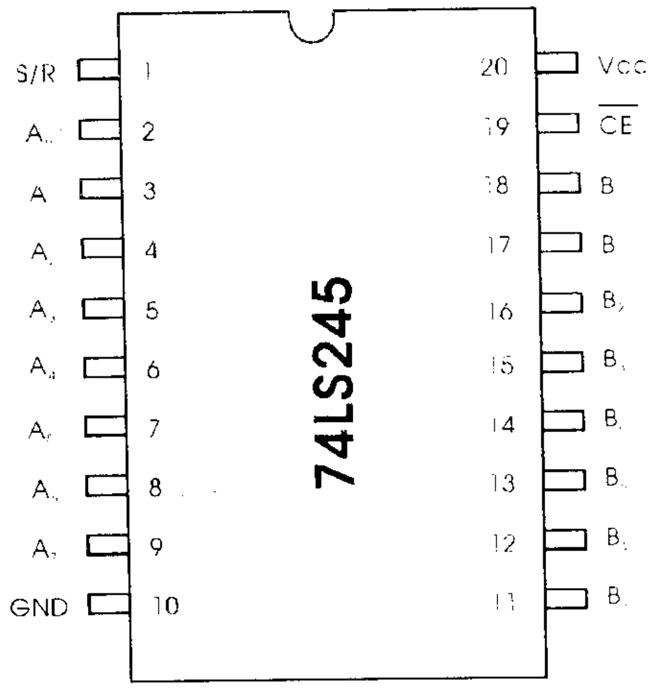


Fig. 2.7.2 PIN OUT DIAGRAM OF BUFFER DRIVER

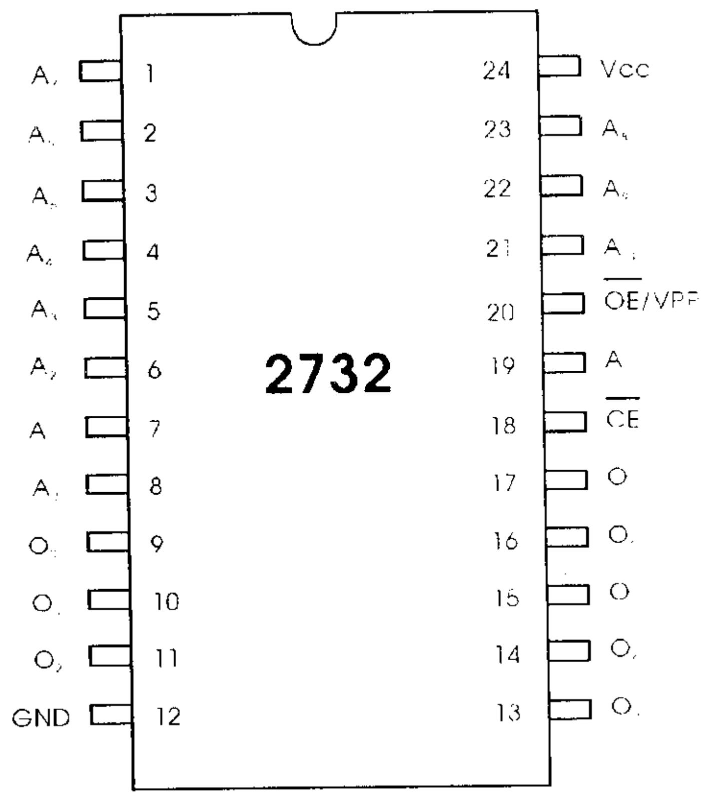


Fig. 2.4.1 PIN OUT DIAGRAM OF 2732 - EPROM

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