P-3047

AUTOMATIC SWITCHING OF CONTROL BETWEEN SIGNAL TRANSMISSION LINES

A PROJECT REPORT

Submitted by

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In partial fulfillement for the award of the degree

of

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IN

Electronics And Communication Engineering

KUMARAGURU COLLEGE OF TECHNOLOGY

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BONAFIDE CERTIFICATE

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EXTERNAL EXAMINER

April 13, 2010

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This is to certify that the Project Work entitled "**AUTOMATIC SWITCHING OF CONTROL BETWEEN SIGNAL TRANSMISSION LINES**" is a bona fide work of

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Kumaraguru College of Technology, Coimbatore . They have done this project with us during the period **20th December 2009 to 5th April 2010** in partial fulfillment of the requirements for the award of Bachelor of Engineering in Electronics and Communication Engineering.

Their performance and Conduct during the project work are good.

For Aircel Limited

S.Nagalakshmi
Manager - HR

"WE DEDICATE THIS PROJECT TO OUR PARENTS AND FRIENDS"

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

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ABSTRACT

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In the present mobile technology , the switching from one transmisssion line to the other line is done manually.We in our project , are going to implement the automatic switching of transmission line using microcontroller , ethernet .First, we have to interface the Microcontroller and Ethernet controller using microcontroller programming. We have to implement the circiuts at both end of the transmission lines.(For example: at Coimbatore and Salem). It must be connected in the LAN network via Ethernet cable. Thus, whenever there is a failure in one transmission path, this device will automatically transfer the transmission through the other path and this information will be passed to the other end via LAN network. Thus, in this way our project is implemented.

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LIST OF ABBREVIATIONS

ABBREVIATIONS		PAGE NO
AVR	Advanced RISC	1
MSC	Main Switching Centre	2
BTS	Base Transceiver Station	4
PSTN	Public Switched Telephone Network	4
IC	Integrated Circuits	4
CPU	Central Processing Unit	4
USART	Universal synchronous/asynchronous Receiver/Transmitter	4
SPI	Serial Pheripheral Interface	4
ADC	Analog To Digital Converter	4
MAC	Multiple Access Unit	6
PHY	Physical Layer	6
LED	Light Emitting Diode	7
ESR	Equivalent Series Resistance	8
DPDT	Double Pole Double Throw	9
SPDT	Single pole Double Throw	10
PCB	Printed Circuit Board	12
USART	Universal synchronous/asynchronous receiver/Transmitter	15
ALU	Arithmetic Logic Unit	18

INTRODUCTION

CHAPTER 1

INTRODUCTION

1.1 GENERAL VIEWS

Today technology has made our life simple and easy in communication field.

1.2 BASIC PRINCIPLE

The project describes how to switch the control between the signal transmission lines by using AVR microcontroller. If any fault occurs in the transmission line the AVR microcontroller switches the control from the faulty transmission line to the other line, both at the receiver and transmitter. By this the drop in calls is reduced.

1.3 BASIC BLOCK DIAGRAM

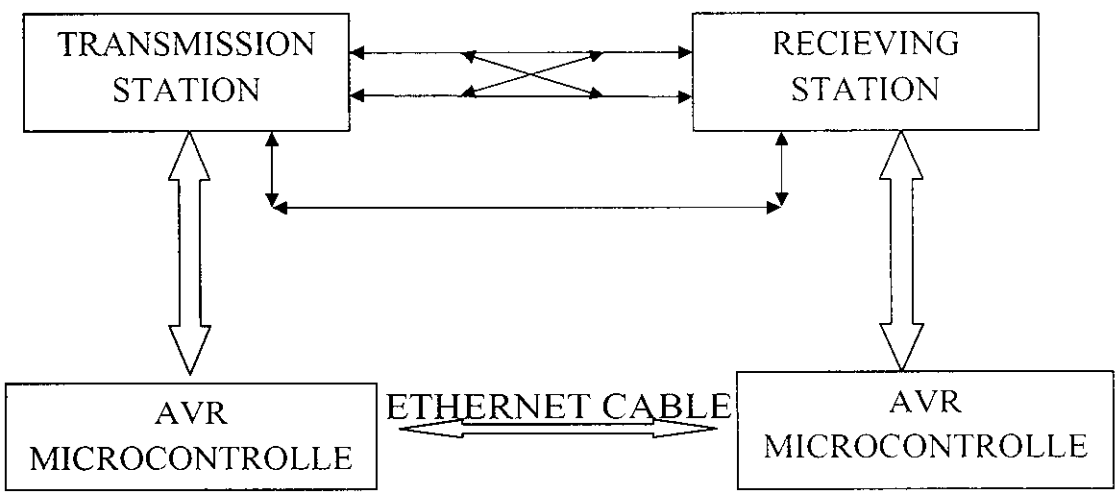

Fig 1.1 Basic block Diagram

1.3.1 WORKING

This is the basic block diagram of our system which shows the main block of our system.The main aim of our project is to switch the control automatically to another transmission line when there is a fault.

There will be transmission lines between the main switching centres with a cross over point.If there is a fault in one line, signals will flow through other line via the cross over point.If there is fault in both transmission lines, the AVR microcontroller will automatically switch the control to the spare line.

The AVR microcontrollers will be placed on both transmitter and receiver sides and they will be connected via ethernet cable.The microcontrollers will continously check the signal flow by pinging the circuit.If it detects a fault,it will change the control and the information will be sent to the other AVR microcontroller on the other side.

1.4 ADVANTAGES OF OUR SYSTEM

- Reduction of manpower
- Reduction of failure of calls.
- Easy maintenance.
- Low revenue loss.

1.5 APPLICATIONS

- It is mainly used in the Mobile Switching Centre (MSC) of the telecom service providers.

SCHEMATIC OVERVIEW

CHAPTER 2

SCHEMATIC OVERVIEW

The Block Diagram of our system is shown below.

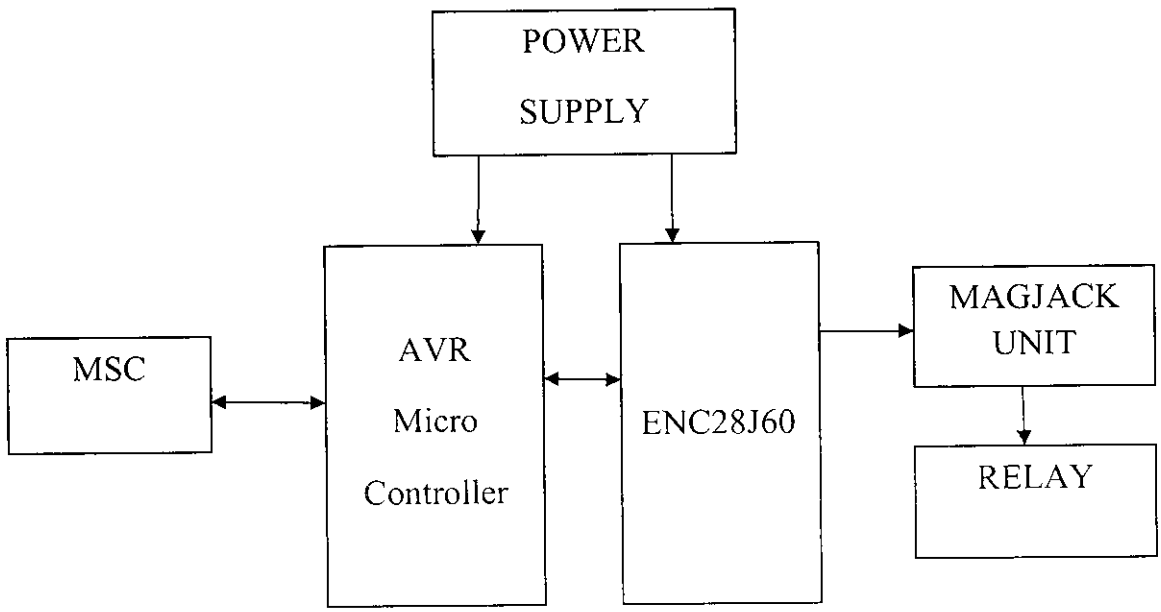

Fig 2.1 Block Diagram

2.1 BLOCK DIAGRAM DESCRIPTION

The block diagram consists of MSC , AVR Microcontroller , Power Supply , ENC28J60 , Magjack unit , Relay .

2.1.1 MSC

Mobile switching center (MSC)

A wireless network is divided geographically into a number of cells, each defined by a radio frequency (RF) radiation pattern from a respective base transceiver station (BTS) antenna. In circuit-switched wireless communication systems, the mobile switching center (MSC) connects the landline public switched telephone network (PSTN) system to the wireless communication system. A mobile switching center includes a first database for storing location information and the call details of a mobile terminal. The base stations route the communications to the MSC via a serving BSC. The MSC routes the communications to another subscribing wireless unit via a BSC/base station path to the terminating station.

2.1.2 AVR MICROCONTROLLER

The microcontroller used in our module is AT mega 88.The main function of this microcontroller is to get the inputs from MSC(Mobile switching centre) through the serial communication to check whether the communication through the transmission lines is working efficiently. If any fault occurs, it switches the control to another transmission line. Watchdog Timer-It resets the IC whenever a fault occurs. Five different modes of operation of IC's are possible. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning.The

Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode,the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

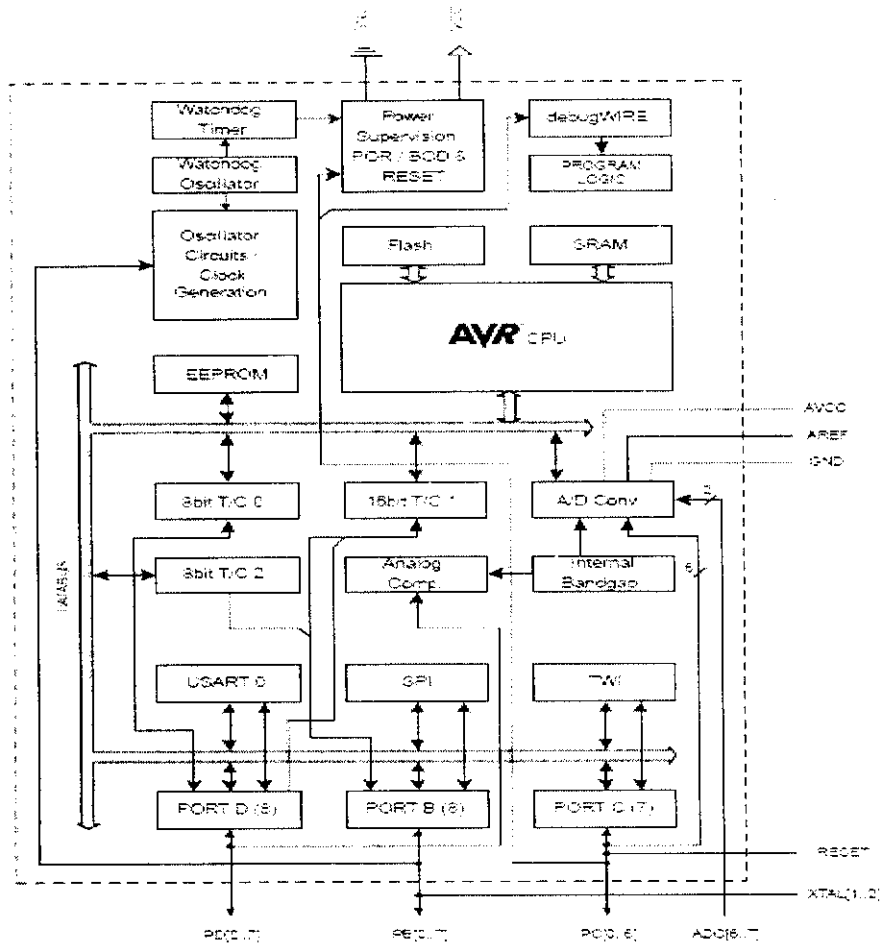

Fig 2.2 ATMEGA88 Block Diagram

2.1.3 ENC28J60

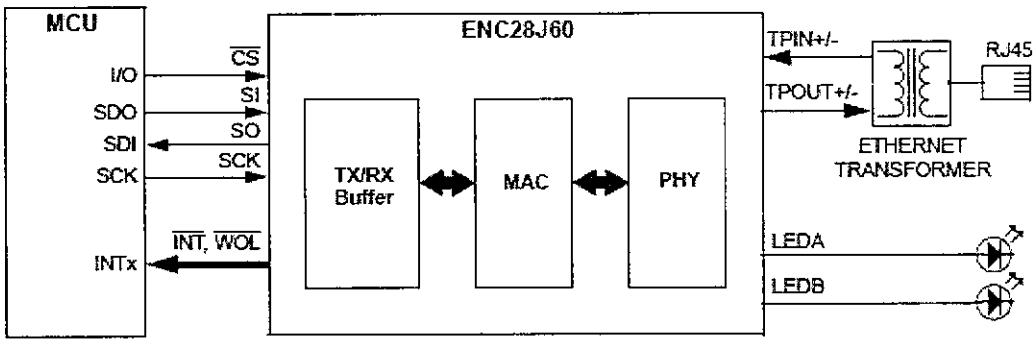

Fig 2.3 ENC28J60 BASED INTERFACE

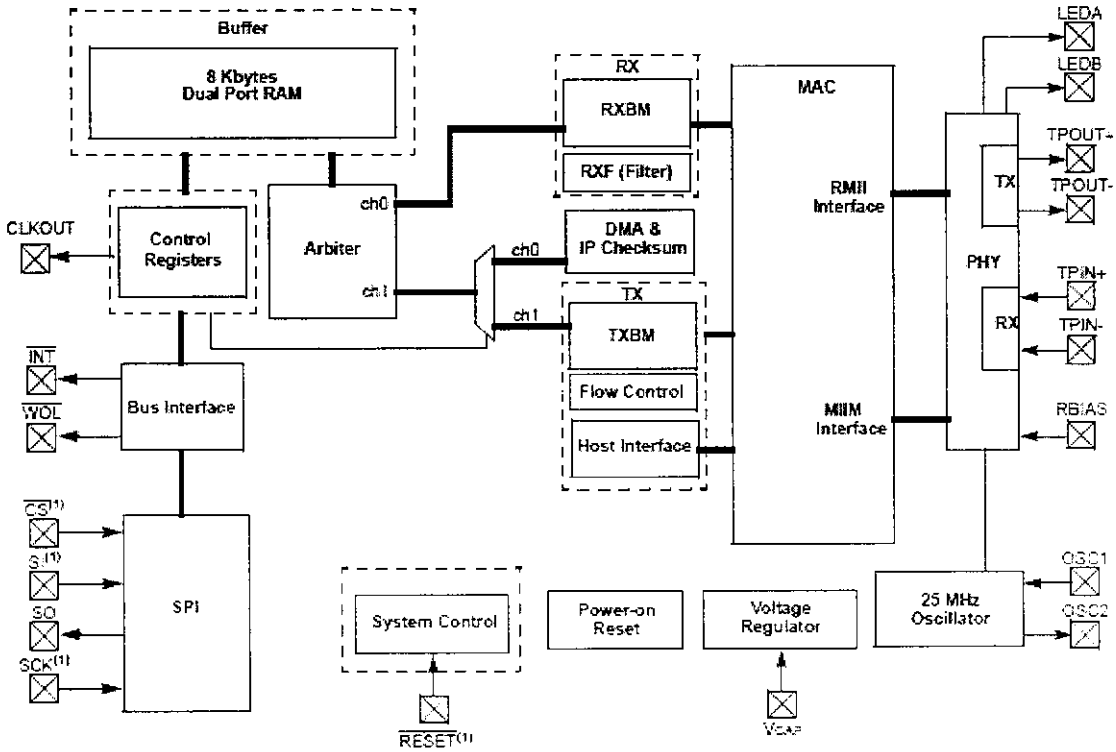

Fig 2.4 ENC28J60 BLOCK DIAGRAM

The ENC28J60 is a stand-alone Ethernet controller with an industry standard Serial Peripheral Interface(SPI™).It is designed to serve as an Ethernet network interface for any controller equipped with SPI.The ENC28J60 meets all of the IEEE 802.3 specifications.

SPI INTERFACE-communication channel between the Host Controller and the ENC28J60. RAM Buffer-To transmit and receive the data packets. ARBITER-To control the access to the RAM buffer when requests are made from DMA, transmit and receive blocks. Control registers which are used to control and monitor the ENC28J60.The bus interface that interprets data and commands received via the SPI interface. The MAC(Medium Access Control)module that implements IEEE 802.3 compliant MAC logic.The PHY(Physical Layer) module that encodes and decodes the analog data that is present on the twisted pair interface.

2.1.4 MAGJACK UNIT

Magjack unit consists of Ethernet port and LEDs.Ethernet is a physical and data link layer technology for local area networks.An Ethernet port is an opening that Ethernet cables plug into.These ports are alternatively called as sockets or jacks.Ethernet ports accept cables wit RJ45 connectors.In this unit there are yellow and green LED's to indicate the status of data packet transfers.The green LED on the Magjack should go on and stay on. The link LED on your relay should also go on. The green LED indicates that this link negotiation works and was successful.Yellow indicates the current state of the relay (on or off).

2.1.5 POWER SUPPLY

The voltage required for AVR microcontroller and ENC28J60 is 3.3V.A power supply circuit that consists

of a voltage regulator is used to produce 3.3V voltage.Here LM2937-33 is used as the voltage regulator.Thus the output of it is used to drive the microcontroller.

Features

- Fully specified for operation over -40°C to +125°C
- Output current in excess of 500 mA (400mA for SOT-223 package)
- Output trimmed for 5% tolerance under all operating conditions
- Wide output capacitor ESR range, 0.01Ω up to 5Ω
- Internal short circuit and thermal overload protection
- Reverse battery protection
- 60V input transient protection

Description

The LM2937-3.3 are positive voltage regulators capable of supplying up to 500 mA of load current.The regulator is ideal for converting a common 5V logic supply, or higher input supply voltage, to the lower 2.5V and 3.3V supplies to power VLSI ASIC's and microcontrollers. Special circuitry has been incorporated to minimize the quiescent current to typically only 10 mA with a full 500 mA load current when the input to output voltage differential is greater than 5V.The LM2937 requires an output bypass capacitor for stability. As with most regulators utilizing a PNP pass transistor, the ESR of this capacitor remains a critical design parameter, but the LM2937-3.3 include special compensation circuitry that relaxes ESR requirements. The LM2937 is stable for all ESR ratings less than 5Ω. This allows the use of low ESR chip capacitors.The regulators are also suited for automotive applications,

with built circuit and thermal shutdown protection are also built in protection from reverse battery connections, two-battery jumps and up to +60V/-50V load dump transients. Familiar regulator features such as short

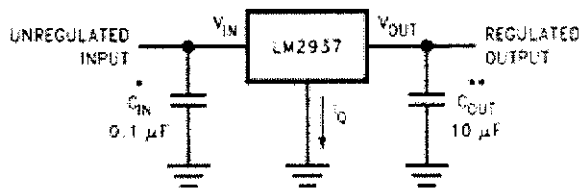

Fig 2.5 Power Supply Block Diagram

2.1.6 RELAY CIRCUIT

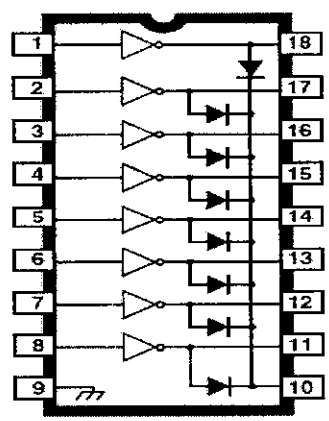

FIG 2.6 ULN2804 IC

Featuring continuous load current ratings to 500 mA for each of the drivers,

the ULN2804 highvoltage,high-current Darlington arrays are ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads. Typical power loads totaling over 260 W (350 mA x 8, 95 V) can be controlled at an appropriate duty cycle depending on ambient temperature and number of drivers turned on simultaneously. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

DPDT stands for Double Pole Double Throw. The double pole is for a dual switched output and the double throw is for the on or off conditions. DPDT consists of two separate switches that operate at the same time, each one with normally open and normally closed contact through a common connector. Each of the two contacts on the switch can be routed in different ways, depending on the position of the switch. An example of which is a mini-toggle switch or a switch using a push or pull control.

A DPDT Relay has a single coil with two arms that move simultaneously. Inside of the DPDT relay, there are two separate SPDT (Single Pole Double Throw) switch mechanisms. These are being used for signal switching applications more often than not, but can also be found in high power switching applications.

2.2 CIRCUIT DIAGRAM

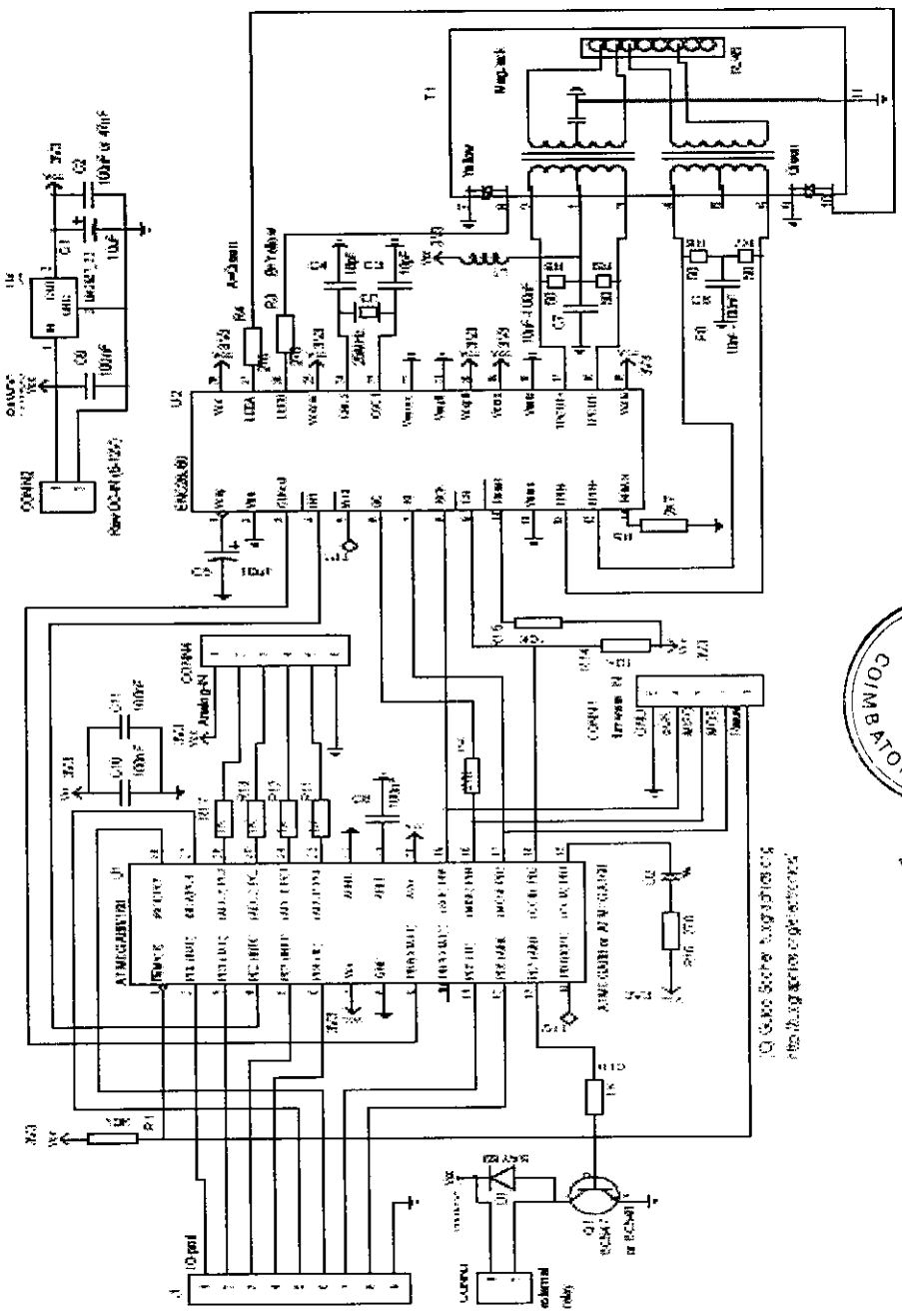

FIG 2.7 CIRCUIT DIAGRAM

CHAPTER 3

PCB DESIGN

3.1 INTRODUCTION

The PCB layout is designed using the Protel software. We have used only bottom layer for drawing the track which minimizes the cost for the fabrication. We used track width of 1mm for the power supply track and 0.5mm width for the other tracks.

3.2 PRINTED CIRCUIT BOARD

Making of PCB is as much an art as a technique partially, so they are to fabricated in very small numbers. There are several ways of drawing PCB patterns and making the final board,but the method most likely to interest people in need of just a few PCbs which are simple and economical. The making of PCB drawing.Fabricating the PCB itself from drawing.

The traditional method of making a PCB drawing with complete placement of parts, taking a photographic negative of the drawing. Developing the image of the negative formed on the photosensitized copper plate and dissolving the excess copper by etching in the standard practice being followed in large scale operations.

This procedure has its own advantages, as the lateral inversion problem is overcome. Also tracing of the circuit and fault finding is made easy, as the exactly matches with the original circuit so that one does not have to constantly look for positions to drill holes and place components.

3.3 PCB DRAWING

Making of PCB drawing involves some preliminary considerations such as Placement of components on a piece of paper Location of holes The optimum area of each components. The shape and location of islands for two or more components at a place. Full place utilization and prevention of over crowding of components at a particular place.

There is no other way to arrive at the components, 1mm diameter hole and for fixing PCB holding screws to the chairs 3mm diameter hole are recommended.

This sketch may be redrawn neatly in a fresh piece of paper, if desired this sketch is the mirror image of the PCB pattern desired, it show the component placement on the other side of the PCB laminate.

The mirror image of this sketch, the pattern can now be drawn with the help of thick tracing paper. The sketch is redrawn on a tracing paper would appears as the PCB pattern when viewed from the other side. To save time and effort, the sketch on the tracing paper itself right in beginning.

Alternatively, the PCB can be drawn from the sketch with the help of a carbon paper. A fresh carbon paper may be placed face upon a flat surface and covered with a plain sheet of paper. On this sheet the sketch may be placed. Now, by carefully tracing the sketch with a ball pen or hard pencil, the mirror image of the sketch may be obtained on the lower sheet of the paper.

3.4 PCB FABRICATION

The copper clad PCB laminate may now be prepared by rubbing away the oxide, grenade and dirt etc, with fine emery paper or sand paper. On this the final PCB drawing may be traced this time by using the carbon paper in the normal way clip should be used to prevent the carbon and the paper from slipping while the PCB pattern is being traced on the laminate. Only the connecting line in PCB island and holes should be traced tracing the position of the components are not required. The component position may be marked on the PCB reverse side, if desired. The marked holes in PCB may be drilled using 1mm or 3mm drill bits and the traced PCB pattern coating with black, quick enamel points, using a thin brush and a small metal scale. In case there is shooting of line due to spilling of points, there may be removed by scraping with a blade or knife after the point had dried.

HARDWARE TOOLS

CHAPTER 4

HARDWARE TOOLS

4.1 MICROCONTROLLER

4.1.1 INTRODUCTION

The ATMega88 is a low power,high performance low power AVR 8bit microcontroller with 512 bytes of electrical erasable read only memory (EEPROM) and flash programmable.The device is manufactured using Atmel's high density non-volatile memory technology and is compatible with the other industrial standards.The on-chip flash allows the program memory to be reprogrammed in-system or by a conventional non-volatile memory programmer.It has a dual programmable serial USARTS.

4.1.2 FEATURES

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 24 MIPS Throughput at 24 MHz
  - On-chip 2-cycle Multiplier
- Non-volatile Program and Data Memories
  - 512 Bytes EEPROM
  - 512/1K/1K Byte Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode

– One 16-bit Timer/Counter with Separate Prescaler, Compare Mode and Capture mode.

– Real Time Counter with Separate Oscillator

– Six PWM Channels

– 8-channel 10-bit ADC in TQFP and MLF package

– Programmable Serial USART

– Master/Slave SPI Serial Interface

– Byte-oriented 2-wire Serial Interface

– Programmable Watchdog Timer with Separate On-chip Oscillator

– On-chip Analog Comparator

– Interrupt and Wake-up on Pin Change

- Special Microcontroller Features

– Power-on Reset and Programmable Brown-out Detection

– Internal Calibrated Oscillator

– External and Internal Interrupt Sources

– Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby.

- I/O and Packages

– 23 Programmable I/O Lines

– 28-pin PDIP, 32-lead TQFP and 32-pad MLF

- Operating Voltage:

– 1.8 - 5.5V for ATmega48V/88V/168V

– 2.7 - 5.5V for ATmega48/88/168

- Temperature Range:

– -40°C to 85°C

- Speed Grade:

– ATmega88: 0 - 6 MHz @ 1.8 - 5.5V, 0 - 12 MHz @ 2.7 - 5.5V

– ATmega88: 0 - 12 MHz @ 2.7 - 5.5V, 0 - 24 MHz @ 4.5 - 5.5V

➢ Low Power Consumption

– Active Mode:1 MHz, 1.8V: 240µA

– Power-down Mode:0.1µA at 1.8V

4.1.3 PIN DIAGRAM

ATMEGA88

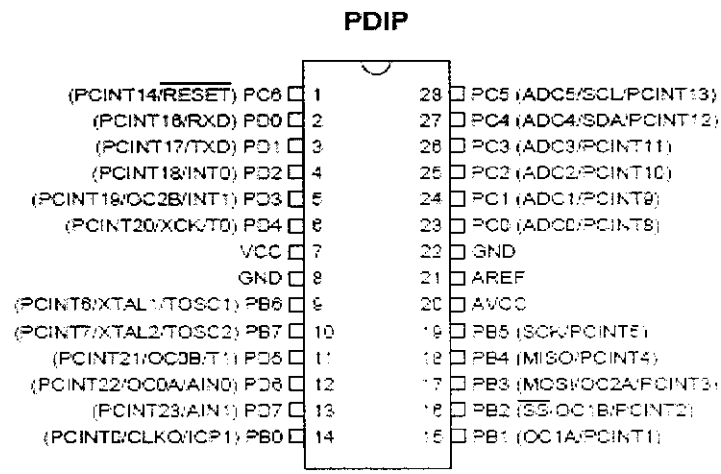

Fig 4.1 Pin Out Of ATMega88

4.1.4 ARCHITECTURE

In order to maximize performance and parallelism,the AVR uses a Harvard architecture with separate memories and buses for program and data.Instructions in the program memory are executed with a single level

pipelining.While one instruction is being executed,the next instruction is pre-fetched from the program memory.This concept enables instructions to be executed in every clock cycle.The program memory is In-System Reprogrammable Flash memory.

4.1.5 ARITHMETIC LOGIC UNIT

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers.Within a single clock cycle,arithmetic operations between general purpose registers or between a register and an immediate are executed.The ALU operations are divided into 3 main categories-arithmetic,logical and bit functions.

Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format.

CHAPTER 5

SOFTWARE DESCRIPTION

5.1 SOFTWARES USED

5.1.1 PROTEL ADVANCED PCB

Protel advanced PCB is a software tool for designing PCB Layout.Using protel software we can design multi layered PCB.Protel has a user friendly interface so that PCB design is made simple.Advanced PCB system resolution is 0.001 mil (0.0000254 mm).Tracks can be placed on any layer with any width from 0.001 to 999.999 mils wide.

We have used 1mm track width for power supply circuit and 0.5mm for other circuits.There are 16 layers for track routing.Anything placed on these layers will appear as copper on final PCB.Connectivity of the track depends on the used material.We have used only bottom layer in order to minimise the cost of fabrication.

5.1.2 CODEVISION AVR

Codevision AVR is a C cross-compiler, integrated development environment and automatic program generator designed for the Atmel AVR family of microcontrollers. The C cross-compiler implements nearly all the elements of the ANSI C language, as allowed by the AVR architecture, with some features added to take advantage of specificity of the AVR architecture and the embedded system needs. The compiled COFF object files can be C source level debugged, with variable watching, using ATMEL AVR studio debugger.

5.2 ALGORITHM

STEP 1:Start.

STEP 2:Set the IP address for Microcontroller.

STEP 3:Enter the password and verify to login.

STEP 4:Configure the LED's in Magjack unit.

STEP 5:New packets will be received and checked for errors.

STEP 6:Initialise the variable 't' used to select the lines.

STEP 7:If t=0, line 1 is selected.

STEP 8:If t=1, line 2 is selected.

STEP 9:If t=xx, invalid.

STEP 10:Datas are transmitted through the selected lines to output.

STEP 11:Stop .

5.3 FLOW CHART

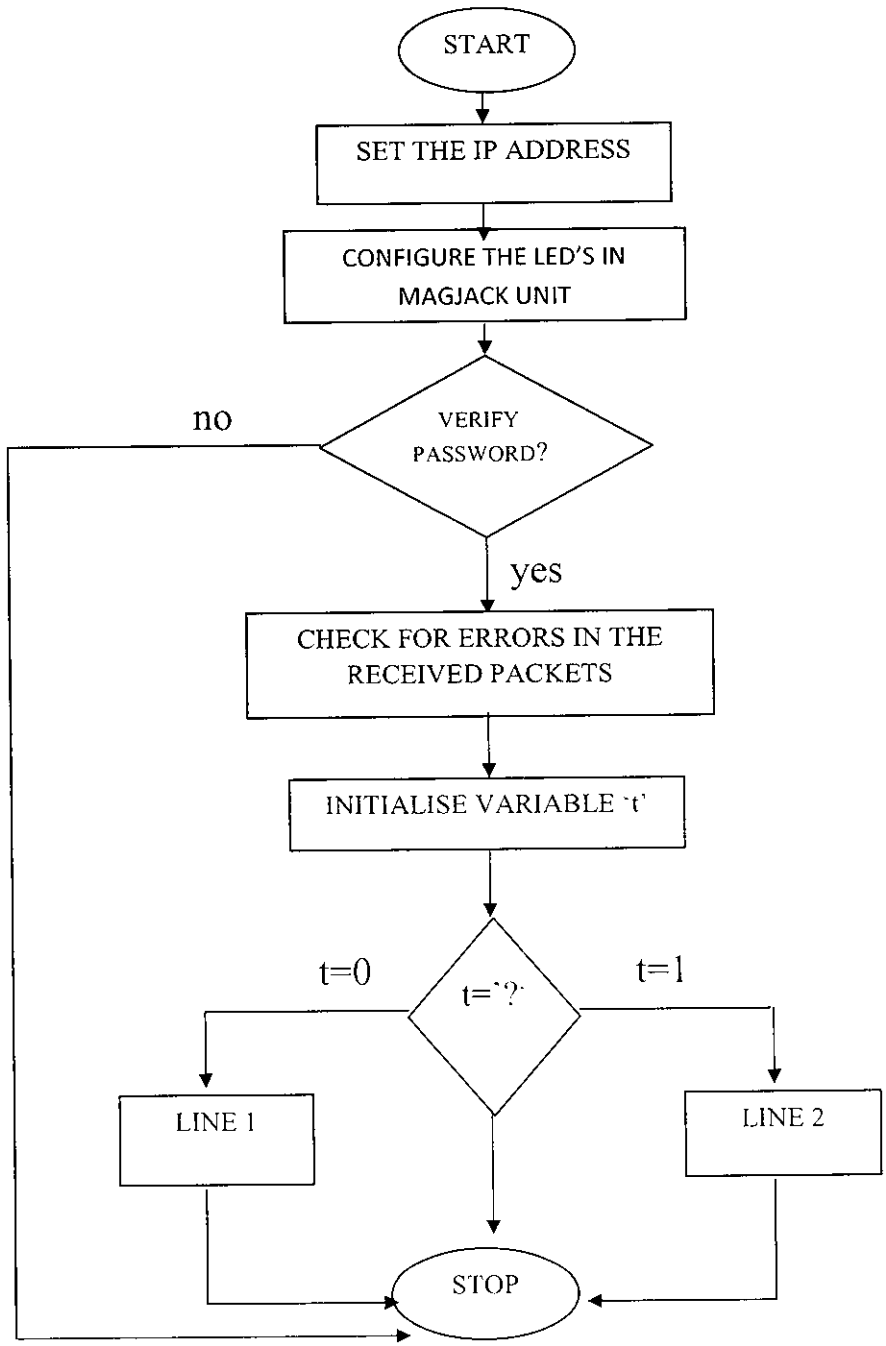

FIG 5.1 FLOW CHART

RESULTS

CHAPTER 6

RESULT

The AVR microcontroller continuously checks for errors in the transmission lines by pinging.

The output screen will be as below,

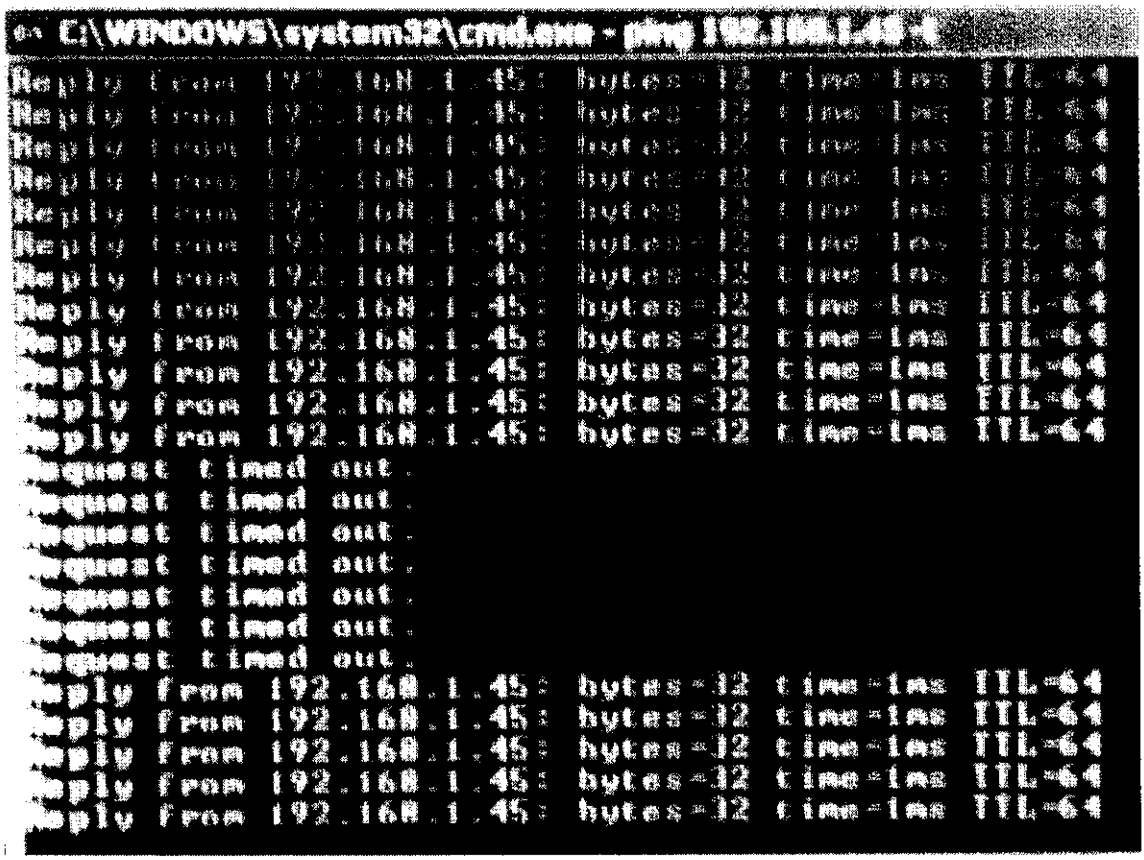

FIG 6.1 RESULTS

CONCLUSION

CONCLUSION

This project facilitates the industry to monitor the signal flow in the transmission lines using AVR microcontroller. When there is error in one of the transmission lines,the AVR microcontroller switches the control to the stand-by line and indicates this message to the receiver station via Ethernet connection.

Thus, this makes the error rectification problem in the signal transmission lines without any call loss.

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REFERENCES

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APPENDICES

APPENDIX 1

ENC28J60
Data Sheet

Stand-Alone Ethernet Controller with SPI™ Interface

ENC28J60

Stand-Alone Ethernet Controller with SPI™ Interface

Ethernet Controller Features

- IEEE 802.3 compatible Ethernet controller
- Integrated MAC and 10BASE-T PHY
- Receiver and collision squelch circuit
- Supports one 10BASE-T port with automatic polarity detection and correction
- Supports Full and Half-Duplex modes
- Programmable automatic retransmit on collision
- Programmable padding and CRC generation
- Programmable automatic rejection of erroneous packets
- SPI™ Interface with speeds up to 10 Mb/s

Buffer

- 8-Kbyte transmit/receive packet dual port SRAM
- Configurable transmit/receive buffer size
- Hardware-managed circular receive FIFO
- Byte-wide random and sequential access with auto-increment
- Internal DMA for fast data movement
- Hardware assisted IP checksum calculation

Medium Access Controller (MAC) Features

- Supports Unicast, Multicast and Broadcast packets
- Programmable receive packet filtering and wake-up host on logical AND or OR of the following:
  - Unicast destination address
  - Multicast address
  - Broadcast address
  - Magic Packet™
  - Group destination addresses as defined by 64-bit hash table
  - Programmable pattern matching of up to 64 bytes at user-defined offset
- Loopback mode

Physical Layer (PHY) Features

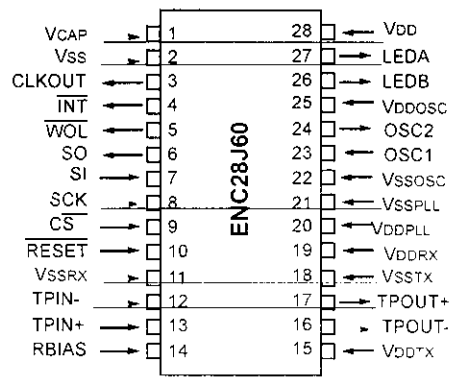
- Wave shaping output filter
- Loopback mode

Operational

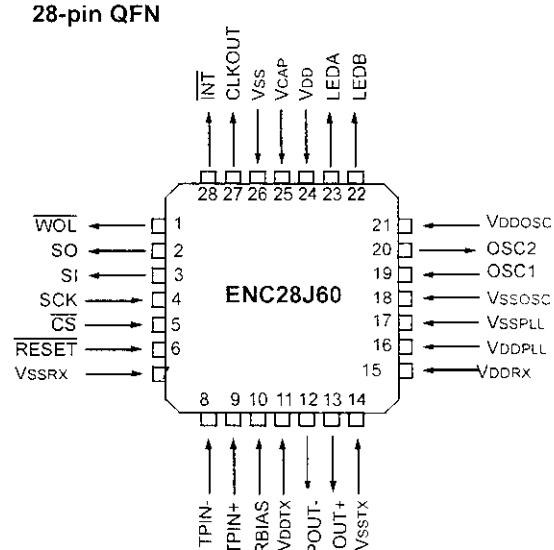
- Two programmable LED outputs for LINK, TX, RX, collision and full/half-duplex status
- Seven interrupt sources with two interrupt pins
- 25 MHz clock
- Clock out pin with programmable prescaler
- Operating voltage range of 3.14V to 3.45V
- TTL level inputs
- Temperature range: -40°C to +85°C Industrial, 0°C to +70°C Commercial (SSOP only)
- 28-pin SPDIP, SSOP, SOIC, QFN packages

Package Types

28-Pin SPDIP, SSOP, SOIC



28-pin QFN



1.0 OVERVIEW

The ENC28J60 is a stand-alone Ethernet controller with an industry standard Serial Peripheral Interface (SPI™). It is designed to serve as an Ethernet network interface for any controller equipped with SPI.

The ENC28J60 meets all of the IEEE 802.3 specifications. It incorporates a number of packet filtering schemes to limit incoming packets. It also provides an internal DMA module for fast data throughput and hardware assisted IP checksum calculations. Communication with the host controller is implemented via two interrupt pins and the SPI, with data rates of up to
10 Mb/s. Two dedicated pins are used for LED link and network activity indication.

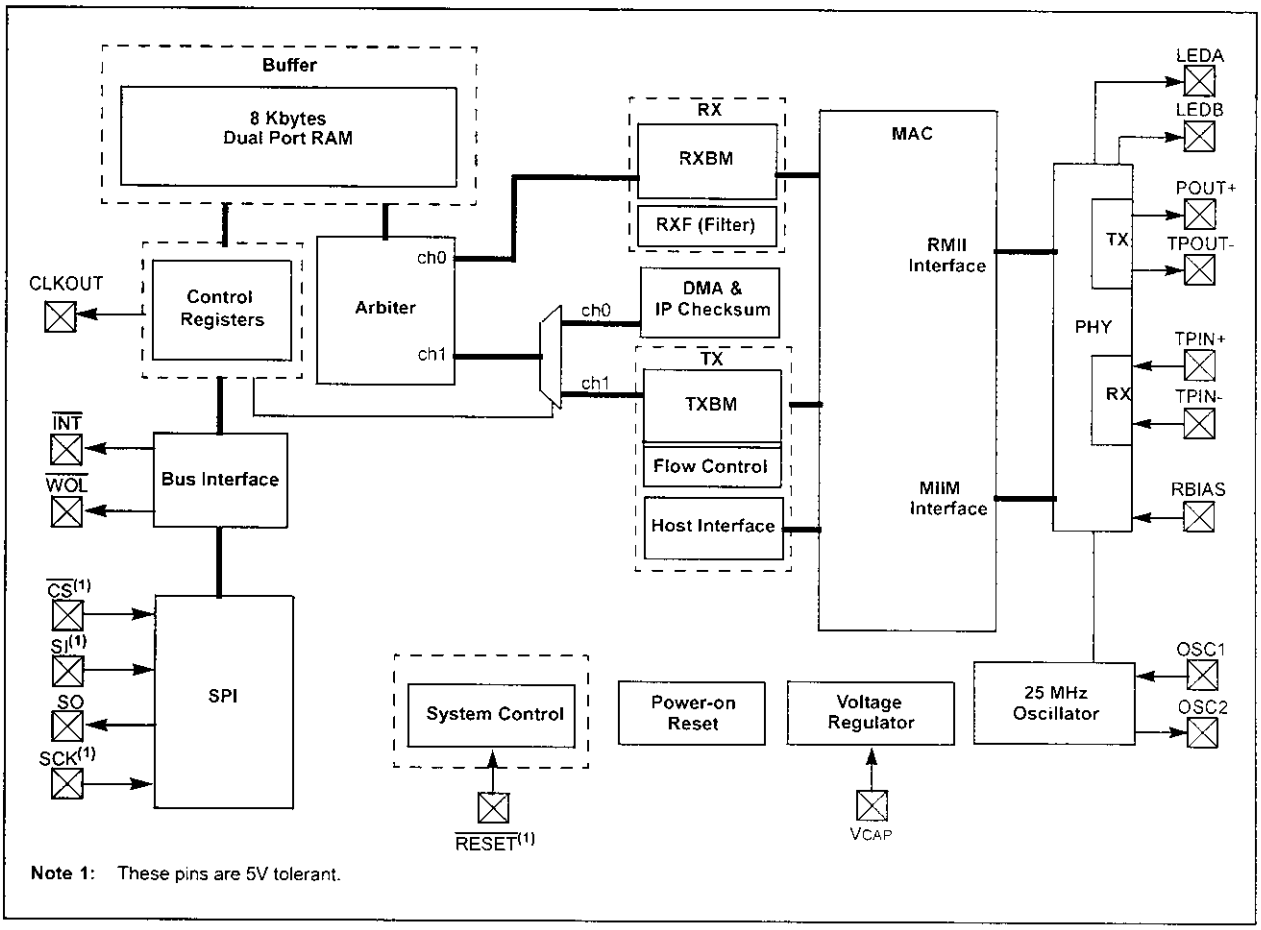
A simple block diagram of the ENC28J60 is shown in Figure 1-1. A typical application circuit using the device is shown in Figure 1-2. With the ENC28J60, two pulse transformers and a few passive components are all that is required to connect a microcontroller to a 10 Mbps

The ENC28J60 consists of seven major functional blocks:

1. An SPI interface that serves as a communication channel between the host controller and the ENC28J60.
2. Control Registers which are used to control and monitor the ENC28J60.
3. A dual port RAM buffer for received and transmitted data packets.
4. An arbiter to control the access to the RAM buffer when requests are made from DMA, transmit and receive blocks.
5. The bus interface that interprets data and commands received via the SPI interface.
6. The MAC (Medium Access Control) module that implements IEEE 802.3 compliant MAC logic.
7. The PHY (Physical Layer) module that encodes and decodes the analog data that is present on the twisted pair interface.

The device also contains other support blocks, such as the oscillator, on-chip voltage regulator, level translators to provide 5V tolerant I/Os and system control logic.

FIGURE 1-1: ENC28J60 BLOCK DIAGRAM



Note 1: These pins are 5V tolerant.

FIGURE 1-2: TYPICAL ENC28J60-BASED INTERFACE

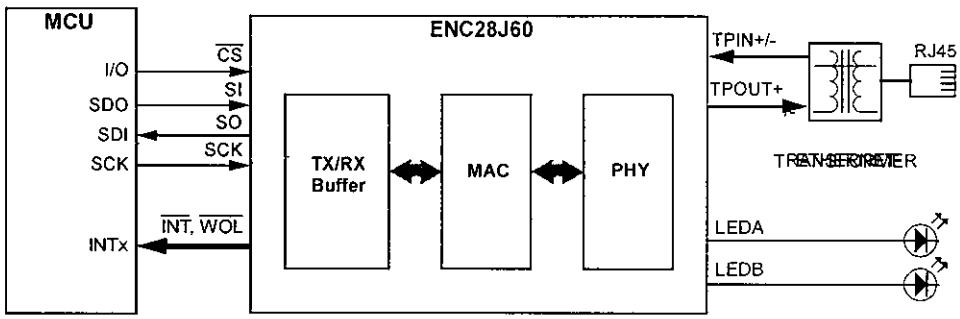


TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	SPDIP, SOIC, SSOP	QFN			
VCAP	1	25	P	—	2.5V output from internal regulator. A 10 µF capacitor to VSSTX must be placed on this pin.
VSS	2	26	P	—	Ground reference.
CLKOUT	3	27	O	—	Programmable clock output pin.(1)
$\overline{INT}$	4	28	O	—	INT interrupt output pin.(2)
$\overline{WOL}$	5	1	O	—	Wake-up on LAN interrupt out pin.(2)
SO	6	2	O	—	Data out pin for SPI™ interface.(2)
SI	7	3	I	ST	Data in pin for SPI interface.(3)
SCK	8	4	I	ST	Clock in pin for SPI interface.(3)
$\overline{CS}$	9	5	I	ST	Chip select input pin for SPI interface.(3,4)
$\overline{RESET}$	10	6	I	ST	Active-low device Reset input.(3, 4)
VSSRX	11	7	P	—	Ground reference for PHY RX.
TPIN-	12	8	I	ANA	Differential signal input.
TPIN+	13	9	I	ANA	Differential signal input.
RBIAS	14	10	I	ANA	Bias current pin for PHY. Must be tied to VSSRX through a 2 kΩ, 1% resistor.
VDDTX	15	11	P	—	Positive supply for PHY TX.
TPOUT-	16	12	O	—	Differential signal output.
TPOUT+	17	13	O	—	Differential signal output.
VSSTX	18	14	P	—	Ground reference for PHY TX.
VDDRX	19	15	P	—	Positive 3.3V supply for PHY RX.
VDDPLL	20	16	P	—	Positive 3.3V supply for PHY PLL.
VSSPLL	21	17	P	—	Ground reference for PHY PLL.
VSSOSC	22	18	P	—	Ground reference for oscillator.
OSC1	23	19	I	DIG	Oscillator input.
OSC2	24	20	O	—	Oscillator output.
VDDOSC	25	21	P	—	Positive 3.3V supply for oscillator.
LEDB	26	22	O	—	LEDB driver pin.(5)
LEDA	27	23	O	—	LEDA driver pin.(5)
VDD	28	24	P	—	Positive 3.3V supply.

Legend: I = Input, O = Output, P = Power, DIG = Digital input, ANA = Analog signal input, ST = Schmitt Trigger

Note 1: Pins have a maximum current capacity of 8 mA.

2: Pins have a maximum current capacity of 4 mA.

3: Pins are 5V tolerant.

4: Pins have an internal weak pull-up to VDD.

5: Pins have a maximum current capacity of 12 mA.

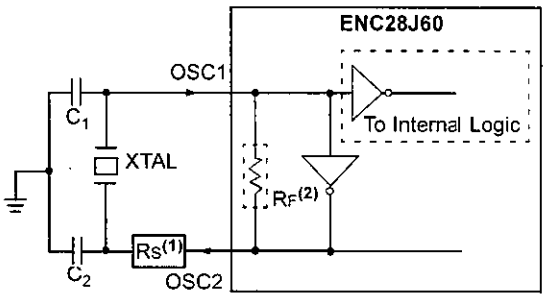
2.0 EXTERNAL CONNECTIONS

2.1 Oscillator

The ENC28J60 is designed to operate at 25 MHz with a crystal connected to the OSC1 and OSC2 pins. The ENC28J60 design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer specifications. A typical oscillator circuit is shown in Figure 2-1.

source connected to the OSC1 pin as shown in Figure 2-2.

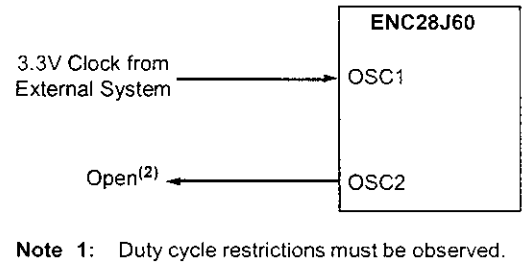
FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION



Note 1: A series resistor, Rs, may be required for AT strip cut crystals.

2: The feedback resistor, RF, is typically in the range of 2 to 10 MΩ.

FIGURE 2-2: EXTERNAL CLOCK SOURCE(1)



Note 1: Duty cycle restrictions must be observed.

2: A resistor to ground may be used to reduce system noise. This may increase system current.

2.2 Oscillator Start-up Timer

The ENC28J60 contains an Oscillator Start-up Timer (OST) to ensure that the oscillator and integrated PHY have stabilized before use. The OST does not expire until 7500 OSC1 clock cycles (300 µs) pass after Power-on Reset or wake-up from Power-Down mode occurs. During the delay, all Ethernet registers and buffer memory may still be read and written to through the SPI bus. However, software should not attempt to transmit any packets (set ECON1.TXRTS), enable reception of packets (set ECON1.RXEN) or access any MAC, MII or PHY registers during this period.

When the OST expires, the CLKRDY bit in the ESTAT register will be set. The application software should poll this bit as necessary to determine when normal device

Note: After a Power-on Reset, or the ENC28J60 is removed from Power-Down mode, the CLKRDY bit must be polled before transmitting packets, enabling packet reception or accessing any MAC, MII or PHY registers.

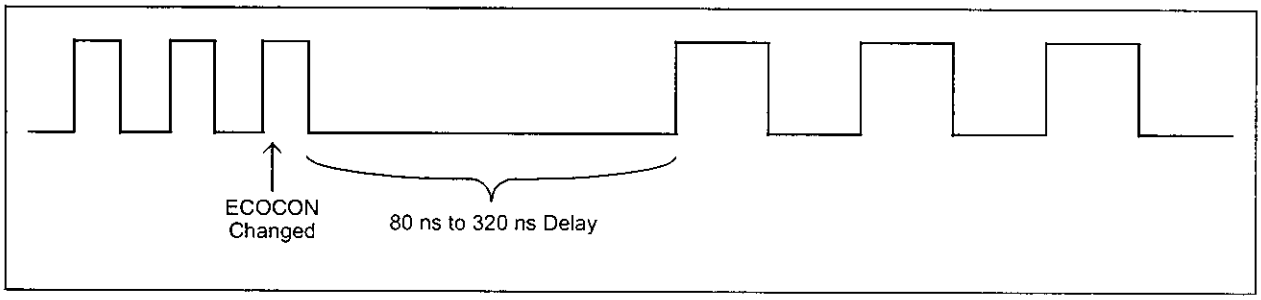
2.3 CLKOUT Pin

The clock out pin is provided to the system designer for use as the host controller clock or as a clock source for other devices in the system. The CLKOUT has an internal prescaler which can divide the output by 1, 2,
3, 4 or 8. The CLKOUT function is enabled and the prescaler is selected via the ECOCON register (Register 2-1).

To create a clean clock signal, the CLKOUT pin is held low for a period when power is first applied. After the Power-on Reset ends, the OST will begin counting. When the OST expires, the CLKOUT pin will begin outputting its default frequency of 6.25 MHz (main clock reset by software or the RESET pin, the CLKOUT function will not be altered (ECOCON will not change value). Additionally, Power-Down mode may be entered and the CLKOUT function will continue to operate. When Power-Down mode is cancelled, the OST will be reset but the CLKOUT function will continue. When the CLKOUT function is disabled (ECOCON = 0), the CLKOUT pin is driven low.

The CLKOUT function is designed to ensure that minimum timings are preserved when the CLKOUT pin function is enabled, disabled or the prescaler value is changed. No high or low pulses will be outputted which exceed the frequency specified by the ECOCON configuration. However, when switching frequencies, a delay between two and eight OSC1 clock periods will occur where no clock pulses will be produced (see Figure 2-3). During this period, CLKOUT will be held low.

FIGURE 2-3: CLKOUT TRANSITION



REGISTER 2-1: ECOCON: CLOCK OUTPUT CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	COCON2	COCON1	COCON0
bit 7							bit 0

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **COCON2:COCON0**: Clock Output Configuration bits

111 = Reserved for factory test. Do not use. Glitch prevention not assured.
110 = Reserved for factory test. Do not use. Glitch prevention not assured.
101 = CLKOUT outputs main clock divided by 8 (3.125 MHz)
100 = CLKOUT outputs main clock divided by 4 (6.25 MHz)
011 = CLKOUT outputs main clock divided by 3 (8.333333 MHz)
010 = CLKOUT outputs main clock divided by 2 (12.5 MHz)
001 = CLKOUT outputs main clock divided by 1 (25 MHz)
000 = CLKOUT is disabled. The pin is driven low.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.4 Magnetics, Termination and Other External Components

To complete the Ethernet interface, the ENC28J60 requires several standard components to be installed externally. These components should be connected as shown in Figure 2-4.

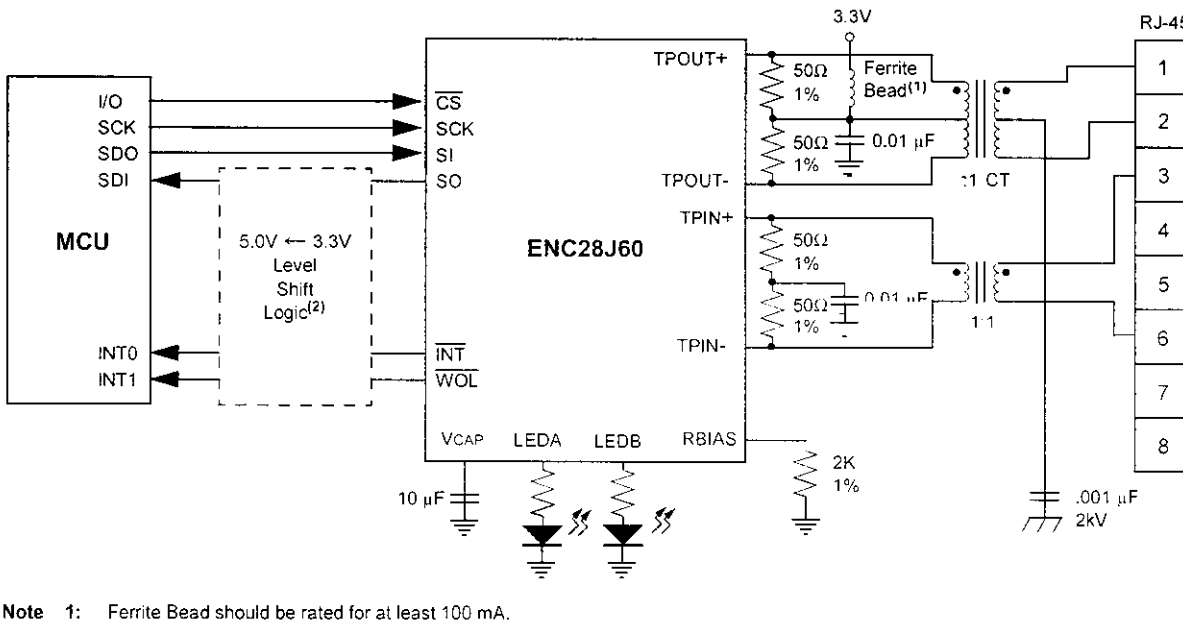
On the differential receive pins (TPIN+/TPIN-), a
required. On the differential transmit pins (TPOUT+/TPOUT-), a 1:1 pulse transformer with a center tap is required. The transformers should be rated for isolation of 2 kV or more to protect against static voltages. See **Section 16.0 "Electrical Charac- teristics"** for specific transformer requirements. Both portions additionally require two 50Ω, 1% resistors and a 0.01 µF capacitor for proper termination.

The internal analog circuitry in the ENC28J60 requires that an external 2 kΩ, 1% resistor be attached

Some of the digital circuitry in the ENC28J60 operates at a nominal 2.5V to reduce power consumption. A
2.5V regulator is incorporated internally to generate the necessary voltage. The only external component required is a 10 µF capacitor for stability purposes. This capacitor should be attached from VCAP to ground. The internal regulator was not designed to drive external loads.

All power supply pins must be externally connected to the same 3.3V power source. Similarly, all ground references should be externally connected to the same ground node. Each VDD and VSS pin pair should have a 0.1 µF ceramic bypass capacitor placed as close to the pins as possible. Relatively high currents are necessary to operate the twisted pair interface, so all wires should be kept as short as possible and reasonable wire widths should be used on power

FIGURE 2-4: EXTERNAL CONNECTIONS



Note 1: Ferrite Bead should be rated for at least 100 mA.

2: Required only if the microcontroller is operating at 5V.

2.5 I/O Levels

The ENC28J60 is a 3.3V part; however, it was designed to be easily integrated into 5V systems. SPI $\overline{CS}$, SCK and SI inputs, as well as the $\overline{RESET}$ pin, are all 5V tolerant. On the other hand, if the host controller is operated at 5V, it quite likely will not be within specifications when its SPI and interrupt inputs are driven by the 3.3V CMOS outputs on the ENC28J60. A unidirectional level translator would be necessary.

An economical 74HCT08 (quad AND gate), 74ACT125 (quad 3-state buffer) or many other 5V CMOS chips with TTL level input buffers may be used to provide the necessary level shifting. The use of 3-state buffers permits easy integration into systems which share the SPI bus with other devices. Figure 2-5 and Figure 2-6 show example translation schemes.

FIGURE 2-5: LEVEL SHIFTING USING AND GATES

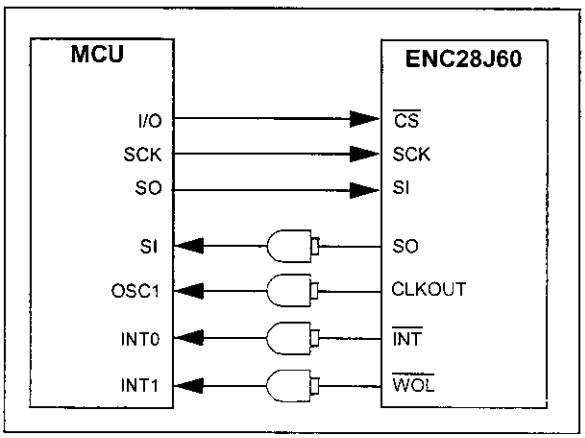
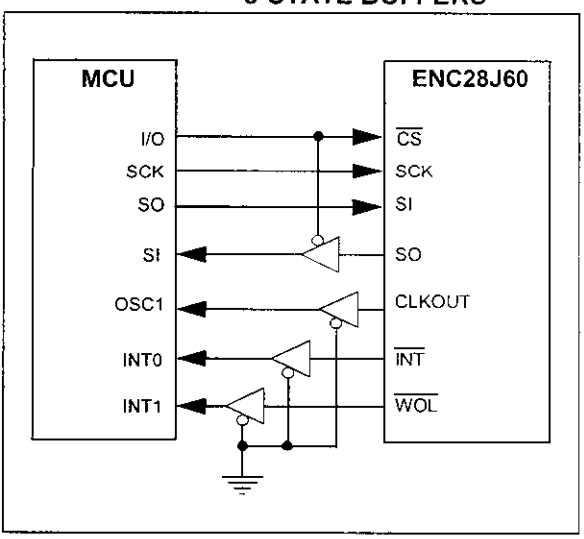


FIGURE 2-6: LEVEL SHIFTING USING 3-STATE BUFFERS

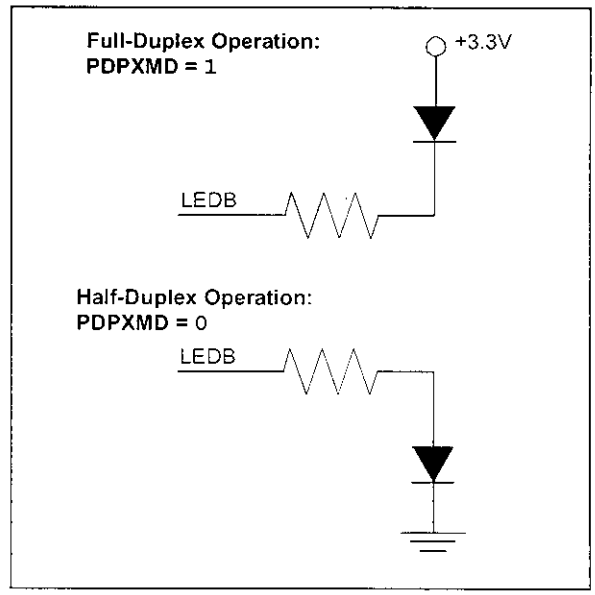


2.6 LED Configuration

The LEDA and LEDB pins support automatic polarity detection on Reset. The LEDs can be connected such that the pin must source current to turn the LED on, or alternately connected such that the pin must sink current to turn the LED on. Upon system Reset, the ENC28J60 will detect how the LED is connected and begin driving the LED to the default state configured by the PHLCON register. If the LED polarity is changed while the ENC28J60 is operating, the new polarity will not be detected until the next system Reset occurs.

LEDB is unique in that the connection of the LED is automatically read on Reset and determines how to initialize the PHCON1.PDPXMD bit. If the pin sources current to illuminate the LED, the bit is cleared on Reset and the PHY defaults to half-duplex operation. If the pin sinks current to illuminate the LED, the bit is set on Reset and the PHY defaults to full-duplex operation. Figure 2-7 shows the two available options. If no LED is attached to the LEDB pin, the PDPXMD bit will reset to an indeterminate value.

FIGURE 2-7: LEDB POLARITY AND RESET CONFIGURATION OPTIONS



REGISTER 2-2: PHLCON: PHY MODULE LED CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
r	r	r	r	LACFG3	LACFG2	LACFG1	LACFG0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-x
LBCFG3	LBCFG2	LBCFG1	LBCFG0	LFRQ1	LFRQ0	STRCH	r
bit 7							bit 0

bit 15-12 **Reserved:** Write as '0'

bit 11-8 **LACFG3:LACFG0:** LEDA Configuration bits
0000 = Reserved
0001 = Display transmit activity (stretchable)
0010 = Display receive activity (stretchable)
0011 = Display collision activity (stretchable)
0100 = Display link status
0101 = Display duplex status
0110 = Reserved
0111 = Display transmit and receive activity (stretchable)
1000 = On
1001 = Off
1010 = Blink fast
1011 = Blink slow
1100 = Display link status and receive activity (always stretched)
1101 = Display link status and transmit/receive activity (always stretched)
1110 = Display duplex status and collision activity (always stretched)
1111 = Reserved

bit 7-4 **LBCFG3:LBCFG0:** LEDB Configuration bits
0000 = Reserved
0001 = Display transmit activity (stretchable)
0010 = Display receive activity (stretchable)
0011 = Display collision activity (stretchable)
0100 = Display link status
0101 = Display duplex status
0110 = Reserved
0111 = Display transmit and receive activity (stretchable)
1000 = On
1001 = Off
1010 = Blink fast
1011 = Blink slow
1100 = Display link status and receive activity (always stretched)
1101 = Display link status and transmit/receive activity (always stretched)
1110 = Display duplex status and collision activity (always stretched)
1111 = Reserved

bit 3-2 **LFRQ1:LFRQ0:** LED Pulse Stretch Time Configuration bits
11 = Reserved
10 = Stretch LED events to approximately 139 ms
01 = Stretch LED events to approximately 73 ms
00 = Stretch LED events to approximately 40 ms

bit 1 **STRCH:** LED Pulse Stretching Enable bit
1 = Stretchable LED events will cause lengthened LED pulses based on the LFRQ configuration

bit 0 0 = Stretchable LED events will only be displayed while they are occurring

Legend:			
R = Readable bit	W = Writable bit	r = Reserved bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.0 MEMORY ORGANIZATION

All memory in the ENC28J60 is implemented as static RAM. There are three types of memory in the ENC28J60:

- Control Registers
- Ethernet Buffer
- PHY Registers

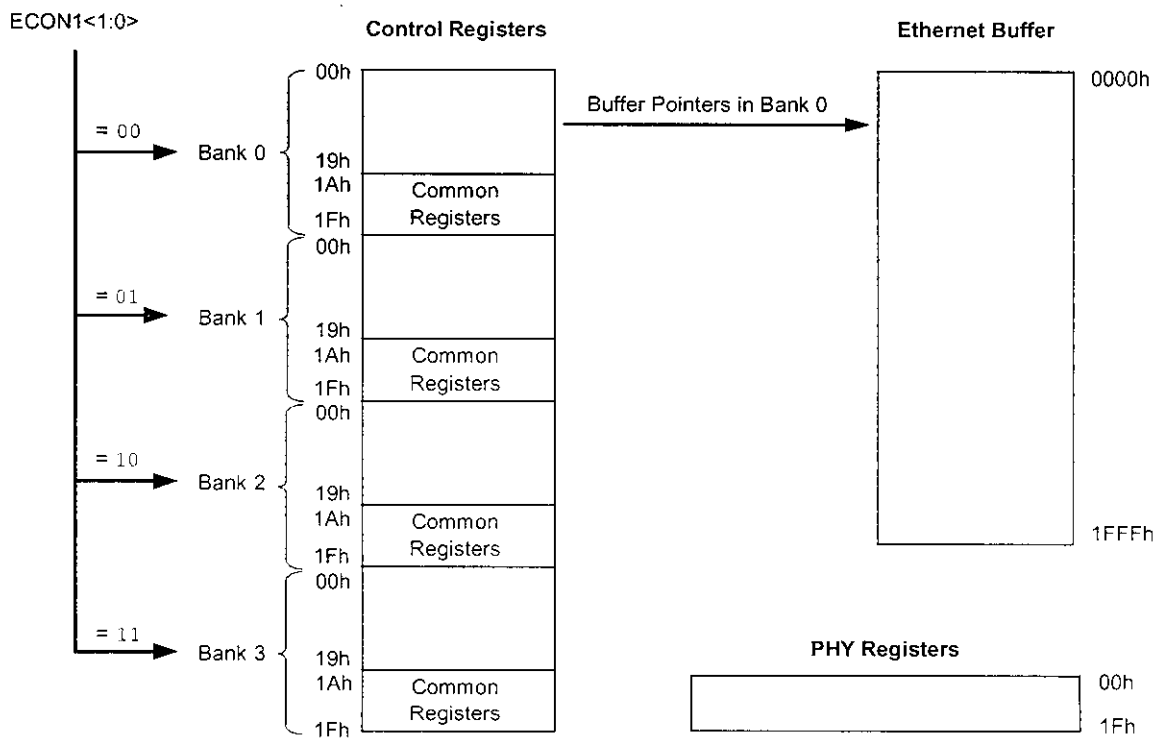
The control registers' memory contains Control Registers (CRs). These are used for configuration, control and status retrieval of the ENC28J60. The Control Registers are directly read and written to by the SPI interface.

The Ethernet buffer contains transmit and receive memory used by the Ethernet controller in a single memory space. The sizes of the memory areas are programmable by the host controller using the SPI interface. The Ethernet buffer memory can only be accessed via the read buffer memory and write buffer memory SPI commands (see **Section 4.2.2 "Read Buffer Memory Command"** and **Section 4.2.4 "Write Buffer Memory Command"**).

The PHY registers are used for configuration, control and status retrieval of the PHY module. The registers are not directly accessible through the SPI interface; they can only be accessed through the Media Independent Interface (MII) implemented in the MAC.

Figure 3-1 shows the data memory organization for the ENC28J60.

FIGURE 3-1: ENC28J60 MEMORY ORGANIZATION



Note: Memory areas are not shown to scale. The size of the control memory space has been scaled to show detail.

3.1 Control Registers

The Control Registers provide the main interface between the host controller and the on-chip Ethernet controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

The Control Register memory is partitioned into four banks, selectable by the bank select bits BSEL1:BSEL0 in the ECON1 register. Each bank is 32 bytes long and addressed by a 5-bit address value.

The last five locations (1Bh to 1Fh) of all banks point to a common set of registers: EIE, EIR, ESTAT, ECON2 and ECON1. These are key registers used in controlling and monitoring the operation of the device. Their common mapping allows easy access without switching the bank. The ECON1 and ECON2 registers are discussed later in

Some of the available addresses are unimplemented. Any attempts to write to these locations are ignored while reads return '0's. The register at address 1Ah in each bank is reserved; read and write operations should not be performed on this register. All other reserved registers may be read, but their contents must not be changed. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

Control registers for the ENC28J60 are generically grouped as ETH, MAC and MII registers. Register names starting with "E" belong to the ETH group. Similarly, registers names starting with "MA" belong to the MAC group and registers prefixed with "MI" belong

TABLE 3-1: ENC28J60 CONTROL REGISTER MAP

Bank 0		Bank 1		Bank 2		Bank 3	
Address	Name	Address	Name	Address	Name	Address	Name
00h	ERDPTL	00h	EHT0	00h	MACON1	00h	MAADR1
01h	ERDPTH	01h	EHT1	01h	MACON2	01h	MAADR0
02h	EWRPTL	02h	EHT2	02h	MACON3	02h	MAADR3
03h	EWRPTH	03h	EHT3	03h	MACON4	03h	MAADR2
04h	ETXSTL	04h	EHT4	04h	MABBIPG	04h	MAADR5
05h	ETXSTH	05h	EHT5	05h	—	05h	MAADR4
06h	ETXNDL	06h	EHT6	06h	MAIPGL	06h	EBSTSD
07h	ETXNDH	07h	EHT7	07h	MAIPGH	07h	EBSTCON
08h	ERXSTL	08h	EPMM0	08h	MACLCON1	08h	EBSTCSL
09h	ERXSTH	09h	EPMM1	09h	MACLCON2	09h	EBSTCSH
0Ah	ERXNDL	0Ah	EPMM2	0Ah	MAMXFLL	0Ah	MISTAT
0Bh	ERXNDH	0Bh	EPMM3	0Bh	MAMXFLH	0Bh	—
0Ch	ERXRDPTL	0Ch	EPMM4	0Ch	Reserved	0Ch	—
0Dh	ERXRDPTH	0Dh	EPMM5	0Dh	MAPHSUP	0Dh	—
0Eh	ERXWRPTL	0Eh	EPMM6	0Eh	Reserved	0Eh	—
0Fh	ERXWRPTH	0Fh	EPMM7	0Fh	—	0Fh	—
10h	EDMASTL	10h	EPMCSL	10h	Reserved	10h	—
11h	EDMASTH	11h	EPMCSH	11h	MICON	11h	—
12h	EDMANDL	12h	—	12h	MICMD	12h	EREVID
13h	EDMANDH	13h	—	13h	—	13h	—
14h	EDMADSTL	14h	EPMOL	14h	MIREGADR	14h	—
15h	EDMADSTH	15h	EPMOH	15h	Reserved	15h	ECOCON
16h	EDMACSL	16h	EWOLIE	16h	MIWRL	16h	Reserved
17h	EDMACSH	17h	EWOLIR	17h	MIWRH	17h	EFLOCON
18h	—	18h	ERXFCON	18h	MIRDL	18h	EPAUSL
19h	—	19h	EPKTCNT	19h	MIRDH	19h	EPAUSH
1Ah	Reserved	1Ah	Reserved	1Ah	Reserved	1Ah	Reserved
1Bh	EIE	1Bh	EIE	1Bh	EIE	1Bh	EIE
1Ch	EIR	1Ch	EIR	1Ch	EIR	1Ch	EIR
1Dh	ESTAT	1Dh	ESTAT	1Dh	ESTAT	1Dh	ESTAT

TABLE 3-2: ENC28J60 CONTROL REGISTER SUMMARY

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset	Details on Page
EIE	INTIE	PKTIE	DMAIE	LINKIE	TXIE	WOLIE	TXERIE	RXERIE	0000 0000	67
EIR	—	PKTIF	DMAIF	LINKIF	TXIF	WOLIF	TXERIF	RXERIF	-000 0000	68
ESTAT	INT	r	r	LATECOL	—	RXBUSY	TXABRT	CLKRDY(1)	0000 -000	66
ECON2	AUTOINC	PKTDEC	PWRSV	—	VRPS	—	—	—	100- 0---	16
ECON1	TXRST	RXRST	DMAST	CSUMEN	TXRTS	RXEN	BSEL1	BSEL0	0000 0000	15
ERDPTL	Read Pointer Low Byte ERDPT<7:0>								1111 1010	17
ERDPTH	—	—	—	Read Pointer High Byte (ERDPT<12:8>)					---0 0101	17
EWRPTL	Write Pointer Low Byte (EWRPT<7:0>)								0000 0000	17
EWRPTH	—	—	—	Write Pointer High Byte (EWRPT<12:8>)					---0 0000	17
ETXSTL	TX Start Low Byte (ETXST<7:0>)								0000 0000	17
ETXSTH	—	—	—	TX Start High Byte (ETXST<12:8>)					---0 0000	17
ETXNDL	TX End Low Byte (ETXND<7:0>)								0000 0000	17
ETXNDH	—	—	—	TX End High Byte (ETXND<12:8>)					---0 0000	17
ERXSTL	RX Start Low Byte (ERXST<7:0>)								1111 1010	17
ERXSTH	—	—	—	RX Start High Byte (ERXST<12:8>)					---0 0101	17
ERXNDL	RX End Low Byte (ERXND<7:0>)								1111 1111	17
ERXNDH	—	—	—	RX End High Byte (ERXND<12:8>)					---1 1111	17
ERXRDPTL	RX RD Pointer Low Byte (ERXRDPT<7:0>)								1111 1010	17
ERXRDPTH	—	—	—	RX RD Pointer High Byte (ERXRDPT<12:8>)					---0 0101	17
ERXWRPTL	RX WR Pointer Low Byte (ERXWRPT<7:0>)								0000 0000	17
ERXWRPTH	—	—	—	RX WR Pointer High Byte (ERXWRPT<12:8>)					---0 0000	17
EDMASTL	DMA Start Low Byte (EDMAST<7:0>)								0000 0000	75
EDMASTH	—	—	—	DMA Start High Byte (EDMAST<12:8>)					---0 0000	75
EDMANDL	DMA End Low Byte (EDMAND<7:0>)								0000 0000	75
EDMANDH	—	—	—	DMA End High Byte (EDMAND<12:8>)					---0 0000	75
EDMADSTL	DMA Destination Low Byte (EDMADST<7:0>)								0000 0000	75
EDMADSTH	—	—	—	DMA Destination High Byte (EDMADST<12:8>)					---0 0000	75
EDMACSL	DMA Checksum Low Byte (EDMACS<7:0>)								0000 0000	76
EDMACSH	DMA Checksum High Byte (EDMACS<15:8>)								0000 0000	76
EHT0	Hash Table Byte 0 (EHT<7:0>)								0000 0000	52
EHT1	Hash Table Byte 1 (EHT<15:8>)								0000 0000	52
EHT2	Hash Table Byte 2 (EHT<23:16>)								0000 0000	52
EHT3	Hash Table Byte 3 (EHT<31:24>)								0000 0000	52
EHT4	Hash Table Byte 4 (EHT<39:32>)								0000 0000	52
EHT5	Hash Table Byte 5 (EHT<47:40>)								0000 0000	52
EHT6	Hash Table Byte 6 (EHT<55:48>)								0000 0000	52
EHT7	Hash Table Byte 7 (EHT<63:56>)								0000 0000	52
EPMM0	Pattern Match Mask Byte 0 (EPMM<7:0>)								0000 0000	51
EPMM1	Pattern Match Mask Byte 1 (EPMM<15:8>)								0000 0000	51
EPMM2	Pattern Match Mask Byte 2 (EPMM<23:16>)								0000 0000	51
EPMM3	Pattern Match Mask Byte 3 (EPMM<31:24>)								0000 0000	51
EPMM4	Pattern Match Mask Byte 4 (EPMM<39:32>)								0000 0000	51
EPMM5	Pattern Match Mask Byte 5 (EPMM<47:40>)								0000 0000	51
EPMM6	Pattern Match Mask Byte 6 (EPMM<55:48>)								0000 0000	51
EPMM7	Pattern Match Mask Byte 7 (EPMM<63:56>)								0000 0000	51
EPMCSL	Pattern Match Checksum Low Byte (EPMCS<7:0>)								0000 0000	51
EPMCSH	Pattern Match Checksum High Byte (EPMCS<15:0>)								0000 0000	51

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved, do not modify. CLKRDY resets to '0' on Power-on Reset but is unaffected on all other Resets.

Note 1: EREVID is a read-only register.

2: ECOCON resets to '---- -100' on Power-on Reset and '---- -uuu' on all other Resets.

3:

APPENDIX 2

atures

gh Performance, Low Power AVR® 8-Bit Microcontroller
lvanced RISC Architecture
- 131 Powerful Instructions – Most Single Clock Cycle Execution
- 32 x 8 General Purpose Working Registers
- Fully Static Operation
- Up to 24 MIPS Throughput at 24 MHz
- On-chip 2-cycle Multiplier

on-volatile Program and Data Memories
- 4/8/16K Bytes of In-System Self-Programmable Flash (ATmega48/88/168)
  Endurance: 10,000 Write/Erase Cycles
- Optional Boot Code Section with Independent Lock Bits
  In-System Programming by On-chip Boot Program
  True Read-While-Write Operation
- 256/512/512 Bytes EEPROM (ATmega48/88/168)
  Endurance: 100,000 Write/Erase Cycles
- 512/1K/1K Byte Internal SRAM (ATmega48/88/168)
- Programming Lock for Software Security

ripheral Features
- Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
- One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
- Real Time Counter with Separate Oscillator
- Six PWM Channels
- 8-channel 10-bit ADC in TQFP and MLF package
- 6-channel 10-bit ADC in PDIP Package
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Byte-oriented 2-wire Serial Interface
- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change

ecial Microcontroller Features
- Power-on Reset and Programmable Brown-out Detection
- Internal Calibrated Oscillator
- External and Internal Interrupt Sources
- Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby

O and Packages
- 23 Programmable I/O Lines
- 28-pin PDIP, 32-lead TQFP and 32-pad MLF

perating Voltage:
- 1.8 - 5.5V for ATmega48V/88V/168V
- 2.7 - 5.5V for ATmega48/88/168

mperature Range:
- -40°C to 85°C

peed Grade:
- ATmega48V/88V/168V: 0 - 6 MHz @ 1.8 - 5.5V, 0 - 12 MHz @ 2.7 - 5.5V
- ATmega48/88/168: 0 - 12 MHz @ 2.7 - 5.5V, 0 - 24 MHz @ 4.5 - 5.5V

ow Power Consumption
- Active Mode:
  1 MHz, 1.8V: 240µA
  32 kHz, 1.8V: 15µA (including Oscillator)
- Power-down Mode:
  0.1µA at 1.8V

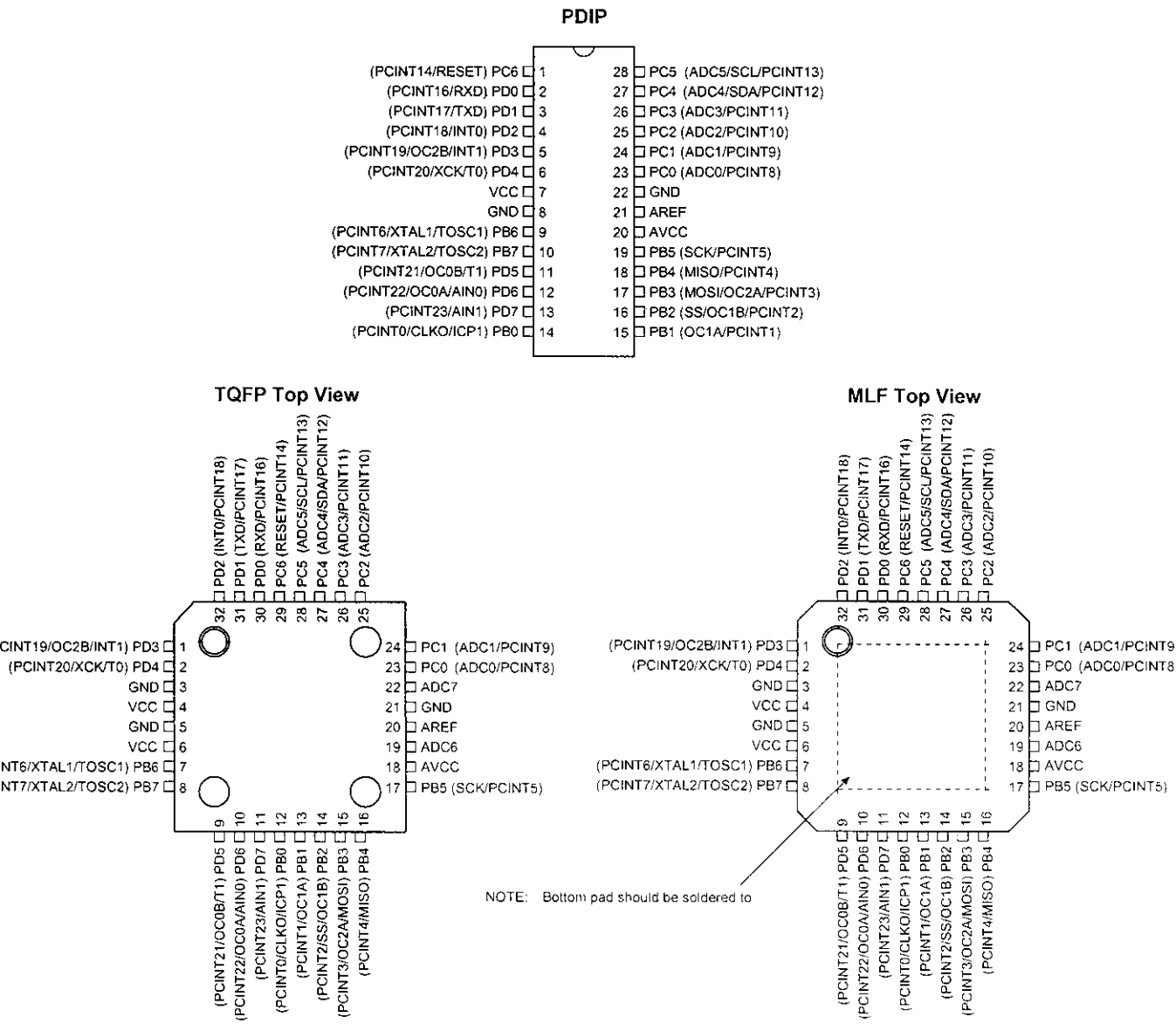
8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

ATmega48/V
ATmega88/V
ATmega168/V

Preliminary Summary

Configurations

e 1. Pinout ATmega48/88/168



laimer

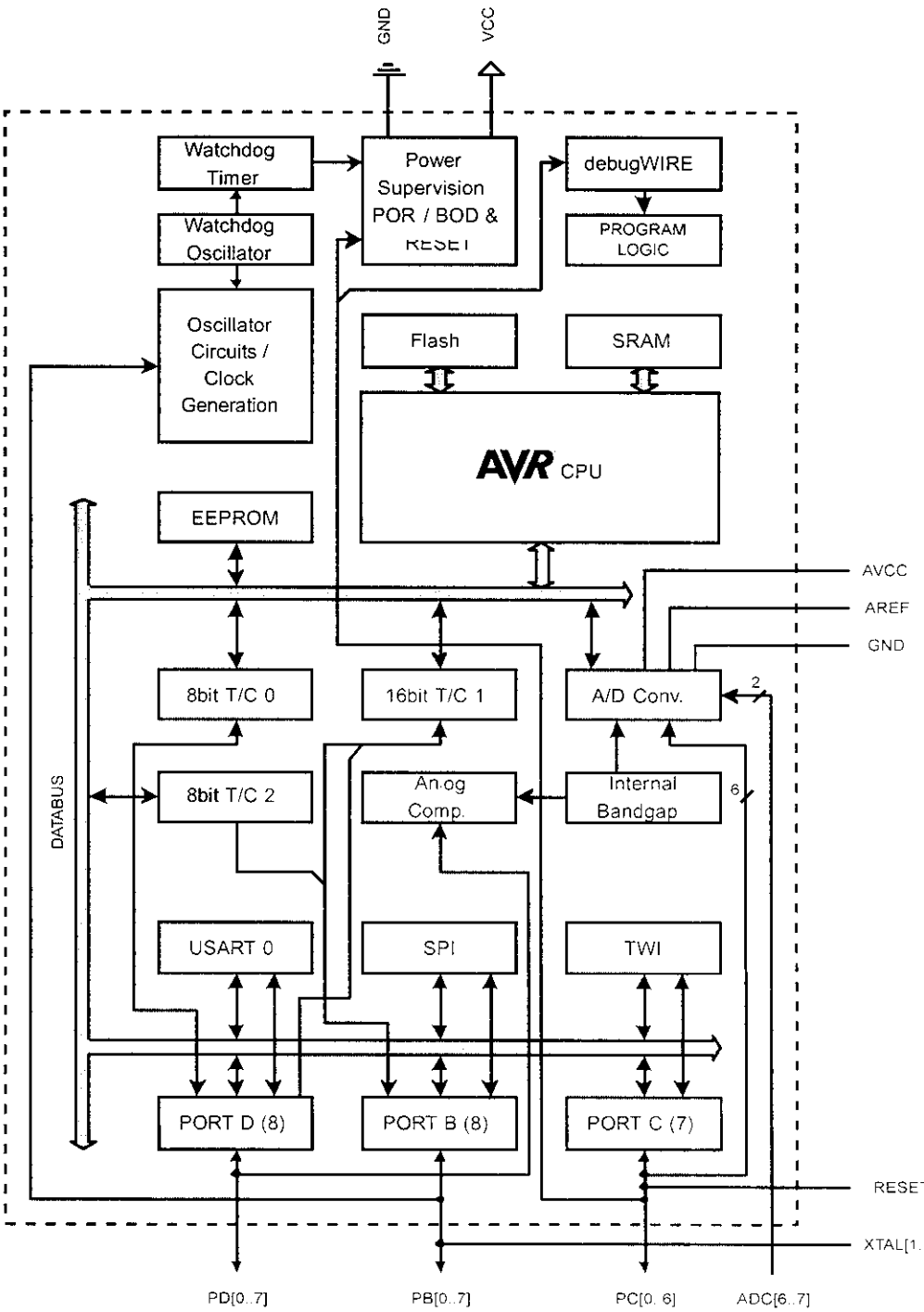
Typical values contained in this datasheet are based on simulations and characteriza-
tion of other AVR microcontrollers manufactured on the same process technology.

erview

The ATmega48/88/168 is a low-power CMOS 8-bit microcontroller based on the A enhanced RISC architecture. By executing powerful instructions in a single clock cy the ATmega48/88/168 achieves throughputs approaching 1 MIPS per MHz allowing system designer to optimize power consumption versus processing speed.

k Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registe All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allow two independent registers to be accessed in one single instruction executed in one cl cycle. The resulting architecture is more code efficient while achieving throughputs up ten times faster than conventional CISC microcontrollers.

The ATmega48/88/168 provides the following features: 4K/8K/16K bytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512 bytes EEPROM 512/1K/1K bytes SRAM, 23 general purpose I/O lines, 32 general purpose working r isters, three flexible Timer/Counters with compare modes, internal and exter interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface, SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and MLF packages), a p grammable Watchdog Timer with internal Oscillator, and five software selectable po saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counte USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioni The Power-down mode saves the register contents but freezes the Oscillator, disab all other chip functions until the next interrupt or hardware reset. In Power-save mo the asynchronous timer continues to run, allowing the user to maintain a timer ba while the rest of the device is sleeping. The ADC Noise Reduction mode stops the C and all I/O modules except asynchronous timer and ADC, to minimize switching no during ADC conversions. In Standby mode, the crystal/resonator Oscillator is runn while the rest of the device is sleeping. This allows very fast start-up combined with power consumption.

The device is manufactured using Atmel's high density non-volatile memory technolo The On-chip ISP Flash allows the program memory to be reprogrammed In-Syst through an SPI serial interface, by a conventional non-volatile memory programmer, by an On-chip Boot program running on the AVR core. The Boot program can use a interface to download the application program in the Application Flash memory. S ware in the Boot Flash section will continue to run while the Application Flash sectio updated, providing true Read-While-Write operation. By combining an 8-bit RISC C with In-System Self-Programmable Flash on a monolithic chip, the Atm ATmega48/88/168 is a powerful microcontroller that provides a highly flexible and c effective solution to many embedded control applications.

The ATmega48/88/168 AVR is supported with a full suite of program and system de opment tools including: C Compilers, Macro Assemblers, Progr Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

nparison Between ega48, ATmega88, ATmega168

The ATmega48, ATmega88 and ATmega168 differ only in memory sizes, boot loa support, and interrupt vector sizes. Table 1 summarizes the different memory and in rupt vector sizes for the three devices.

Table 1. Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48	4K Bytes	256 Bytes	512 Bytes	1 instruction word/vector
ATmega88	8K Bytes	512 Bytes	1K Bytes	1 instruction word/vector
ATmega168	16K Bytes	512 Bytes	1K Bytes	2 instruction words/vecto

ATmega88 and ATmega168 support a real Read-While-Write Self-Programming me anism. There is a separate Boot Loader Section, and the SPM instruction only execute from there. In ATmega48, there is no Read-While-Write support and sepa- rate Boot Loader Section. The SPM instruction can execute from the en

Descriptions

	Digital supply voltage.
	Ground.
B (PB7..0) XTAL1/ 2/TOSC1/TOSC2	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for e bit). The Port B output buffers have symmetrical drive characteristics with both high s and source capability. As inputs, Port B pins that are externally pulled low will sou current if the pull-up resistors are activated. The Port B pins are tri-stated when a re condition becomes active, even if the clock is not running. Depending on the clock selection fuse settings, PB6 can be used as input to the inv ing Oscillator amplifier and input to the internal clock operating circuit. Depending on the clock selection fuse settings, PB7 can be used as output from inverting Oscillator amplifier. If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used a TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set. The various special features of Port B are elaborated in "Alternate Functions of Port E on page 69 and "System Clock and Clock Options" on page 24.
C (PC5..0)	Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for e bit). The PC5..0 output buffers have symmetrical drive characteristics with both h sink and source capability. As inputs, Port C pins that are externally pulled low source current if the pull-up resistors are activated. The Port C pins are tri-stated whe reset condition becomes active, even if the clock is not running.
$\overline{\text{RESET}}$	If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the elec cal characteristics of PC6 differ from those of the other pins of Port C. If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level this pin for longer than the minimum pulse length will generate a Reset, even if the cloc not running. The minimum pulse length is given in Table 20 on page 41. Sho pulses are not guaranteed to generate a Reset. The various special features of Port C are elaborated in "Alternate Functions of Port C on page 73.
D (PD7..0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for e bit). The Port D output buffers have symmetrical drive characteristics with both h sink and source capability. As inputs, Port D pins that are externally pulled low source current if the pull-up resistors are activated. The Port D pins are tri-sta when a reset condition becomes active, even if the clock is not running. The various special features of Port D are elaborated in "Alternate Functions of P D"
C	AVCC is the supply voltage pin for the A/D Converter, PC3..0, and ADC7..6. It should externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should connected to V_{CC} through a low-pass filter. Note that PC6..4 use digital sup voltage, V_{CC}.
F	AREF is the analog reference pin for the A/D Converter.

gister Summary

ddress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	–	–	–	–	–	–	–	–	
(0xFE)	Reserved	–	–	–	–	–	–	–	–	
(0xFD)	Reserved	–	–	–	–	–	–	–	–	
(0xFC)	Reserved	–	–	–	–	–	–	–	–	
(0xFB)	Reserved	–	–	–	–	–	–	–	–	
(0xFA)	Reserved	–	–	–	–	–	–	–	–	
(0xF9)	Reserved	–	–	–	–	–	–	–	–	
(0xF8)	Reserved	–	–	–	–	–	–	–	–	
(0xF7)	Reserved	–	–	–	–	–	–	–	–	
(0xF6)	Reserved	–	–	–	–	–	–	–	–	
(0xF5)	Reserved	–	–	–	–	–	–	–	–	
(0xF4)	Reserved	–	–	–	–	–	–	–	–	
(0xF3)	Reserved	–	–	–	–	–	–	–	–	
(0xF2)	Reserved	–	–	–	–	–	–	–	–	
(0xF1)	Reserved	–	–	–	–	–	–	–	–	
(0xF0)	Reserved	–	–	–	–	–	–	–	–	
(0xEF)	Reserved	–	–	–	–	–	–	–	–	
(0xEE)	Reserved	–	–	–	–	–	–	–	–	
(0xED)	Reserved	–	–	–	–	–	–	–	–	
(0xEC)	Reserved	–	–	–	–	–	–	–	–	
(0xEB)	Reserved	–	–	–	–	–	–	–	–	
(0xEA)	Reserved	–	–	–	–	–	–	–	–	
(0xE9)	Reserved	–	–	–	–	–	–	–	–	
(0xE8)	Reserved	–	–	–	–	–	–	–	–	
(0xE7)	Reserved	–	–	–	–	–	–	–	–	
(0xE6)	Reserved	–	–	–	–	–	–	–	–	
(0xE5)	Reserved	–	–	–	–	–	–	–	–	
(0xE4)	Reserved	–	–	–	–	–	–	–	–	
(0xE3)	Reserved	–	–	–	–	–	–	–	–	
(0xE2)	Reserved	–	–	–	–	–	–	–	–	
(0xE1)	Reserved	–	–	–	–	–	–	–	–	
(0xE0)	Reserved	–	–	–	–	–	–	–	–	
(0xDF)	Reserved	–	–	–	–	–	–	–	–	
(0xDE)	Reserved	–	–	–	–	–	–	–	–	
(0xDD)	Reserved	–	–	–	–	–	–	–	–	
(0xDC)	Reserved	–	–	–	–	–	–	–	–	
(0xDB)	Reserved	–	–	–	–	–	–	–	–	
(0xDA)	Reserved	–	–	–	–	–	–	–	–	
(0xD9)	Reserved	–	–	–	–	–	–	–	–	
(0xD8)	Reserved	–	–	–	–	–	–	–	–	
(0xD7)	Reserved	–	–	–	–	–	–	–	–	
(0xD6)	Reserved	–	–	–	–	–	–	–	–	
(0xD5)	Reserved	–	–	–	–	–	–	–	–	
(0xD4)	Reserved	–	–	–	–	–	–	–	–	
(0xD3)	Reserved	–	–	–	–	–	–	–	–	
(0xD2)	Reserved	–	–	–	–	–	–	–	–	
(0xD1)	Reserved	–	–	–	–	–	–	–	–	
(0xD0)	Reserved	–	–	–	–	–	–	–	–	
(0xCF)	Reserved	–	–	–	–	–	–	–	–	
(0xCE)	Reserved	–	–	–	–	–	–	–	–	
(0xCD)	Reserved	–	–	–	–	–	–	–	–	
(0xCC)	Reserved	–	–	–	–	–	–	–	–	
(0xCB)	Reserved	–	–	–	–	–	–	–	–	
(0xCA)	Reserved	–	–	–	–	–	–	–	–	
(0xC9)	Reserved	–	–	–	–	–	–	–	–	
(0xC8)	Reserved	–	–	–	–	–	–	–	–	
(0xC7)	Reserved	–	–	–	–	–	–	–	–	
(0xC6)	UDR0	USART I/O Data Register								180
(0xC5)	UBRR0H						USART Baud Rate Register High			184
(0xC4)	UBRR0L	USART Baud Rate Register Low								184
(0xC3)	Reserved	–	–	–	–	–	–	–	–	
(0xC2)	UCSR0C	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01 /UDORD0	UCSZ00 / UCPHA0	UCPOL0	183/196
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	182
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	180

ddress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0xBF)	Reserved	–	–	–	–	–	–	–	–	
0xBE)	Reserved	–	–	–	–	–	–	–	–	
0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	–	209
0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	206
0xBB)	TWDR	2-wire Serial Interface Data Register								208
0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	208
0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	207
0xB8)	TWBR	2-wire Serial Interface Bit Rate Register								206
0xB7)	Reserved	–		–	–	–	–	–	–	
0xB6)	ASSR	–	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	148
0xB5)	Reserved	–	–	–	–	–	–	–	–	
0xB4)	OCR2B	Timer/Counter2 Output Compare Register B								147
0xB3)	OCR2A	Timer/Counter2 Output Compare Register A								147
0xB2)	TCNT2	Timer/Counter2 (8-bit)								147
0xB1)	TCCR2B	FOC2A	FOC2B	–	–	WGM22	CS22	CS21	CS20	146
0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	–	–	WGM21	WGM20	143
0xAF)	Reserved	–	–	–	–	–	–	–	–	
0xAE)	Reserved	–	–	–	–	–	–	–	–	
0xAD)	Reserved	–	–	–	–	–	–	–	–	
0xAC)	Reserved	–	–	–	–	–	–	–	–	
0xAB)	Reserved	–	–	–	–	–	–	–	–	
0xAA)	Reserved	–	–	–	–	–	–	–	–	
0xA9)	Reserved	–	–	–	–	–	–	–	–	
0xA8)	Reserved	–	–	–	–	–	–	–	–	
0xA7)	Reserved	–	–	–	–	–	–	–	–	
0xA6)	Reserved	–	–	–	–	–	–	–	–	
0xA5)	Reserved	–	–	–	–	–	–	–	–	
0xA4)	Reserved	–	–	–	–	–	–	–	–	
0xA3)	Reserved	–	–	–	–	–	–	–	–	
0xA2)	Reserved	–	–	–	–	–	–	–	–	
0xA1)	Reserved	–	–	–	–	–	–	–	–	
0xA0)	Reserved	–	–	–	–	–	–	–	–	
0x9F)	Reserved	–	–	–	–	–	–	–	–	
0x9E)	Reserved	–	–	–	–	–	–	–	–	
0x9D)	Reserved	–	–	–	–	–	–	–	–	
0x9C)	Reserved	–	–	–	–	–	–	–	–	
0x9B)	Reserved	–	–	–	–	–	–	–	–	
0x9A)	Reserved	–	–	–	–	–	–	–	–	
0x99)	Reserved	–	–	–	–	–	–	–	–	
0x98)	Reserved	–	–	–	–	–	–	–	–	
0x97)	Reserved	–	–	–	–	–	–	–	–	
0x96)	Reserved	–	–	–	–	–	–	–	–	
0x95)	Reserved	–	–	–	–	–	–	–	–	
0x94)	Reserved	–	–	–	–	–	–	–	–	
0x93)	Reserved	–	–	–	–	–	–	–	–	
0x92)	Reserved	–	–	–	–	–	–	–	–	
0x91)	Reserved	–	–	–	–	–	–	–	–	
0x90)	Reserved	–	–	–	–	–	–	–	–	
0x8F)	Reserved	–	–	–	–	–	–	–	–	
0x8E)	Reserved	–	–	–	–	–	–	–	–	
0x8D)	Reserved	–	–	–	–	–	–	–	–	
0x8C)	Reserved	–	–	–	–	–	–	–	–	
0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								129
0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								129
0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								129
0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								129
0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								129
0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								129
0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								129
0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								129
0x83)	Reserved	–	–	–	–	–	–	–	–	
0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	128
0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	127
0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	125
0x7F)	DIDR1	–	–	–	–	–	–	AIN1D	AIN0D	230
0x7E)	DIDR0	–	–	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	245

ddress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x7D)	Reserved	–	–	–	–	–	–	–	–	
0x7C)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	241
0x7B)	ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	244
0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	242
0x79)	ADCH	ADC Data Register High byte								244
0x78)	ADCL	ADC Data Register Low byte								244
0x77)	Reserved	–	–	–	–	–	–	–	–	
0x76)	Reserved	–	–	–	–	–	–	–	–	
0x75)	Reserved	–	–	–	–	–	–	–	–	
0x74)	Reserved	–	–	–	–	–	–	–	–	
0x73)	Reserved	–	–	–	–	–	–	–	–	
0x72)	Reserved	–	–	–	–	–	–	–	–	
0x71)	Reserved	–	–	–	–	–	–	–	–	
0x70)	TIMSK2	–	–	–	–	–	OCIE2B	OCIE2A	TOIE2	150
0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	130
0x6E)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	100
0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	83
0x6C)	PCMSK1	–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	83
0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	84
0x6A)	Reserved	–	–	–	–	–	–	–	–	
0x69)	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00	80
0x68)	PCICR	–	–	–	–	–	PCIE2	PCIE1	PCIE0	
0x67)	Reserved	–	–	–	–	–	–	–	–	
0x66)	OSCCAL	Oscillator Calibration Register								30
0x65)	Reserved	–	–	–	–	–	–	–	–	
0x64)	PRR	PRTWI	PRTIM2	PRTIM0	–	PRTIM1	PRSPI	PRUSART0	PRADC	37
0x63)	Reserved	–	–	–	–	–	–	–	–	
0x62)	Reserved	–	–	–	–	–	–	–	–	
0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	33
0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	49
F (0x5F)	SREG	I	T	H	S	V	N	Z	C	9
E (0x5E)	SPH	–	–	–	–	–	(SP10) [5]	SP9	SP8	11
D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
C (0x5C)	Reserved	–	–	–	–	–	–	–	–	
B (0x5B)	Reserved	–	–	–	–	–	–	–	–	
A (0x5A)	Reserved	–	–	–	–	–	–	–	–	
9 (0x59)	Reserved	–	–	–	–	–	–	–	–	
8 (0x58)	Reserved	–	–	–	–	–	–	–	–	
7 (0x57)	SPMCSR	SPMIE	(RWWSB) [5]	–	(RWWSRE) [5]	BLBSET	PGWRT	PGERS	SELFPRGEN	260
6 (0x56)	Reserved	–	–	–	–	–	–	–	–	
5 (0x55)	MCUCR	–	–	–	PUD	–	–	IVSEL	IVCE	
4 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	
3 (0x53)	SMCR	–	–	–	–	SM2	SM1	SM0	SE	35
2 (0x52)	Reserved	–	–	–	–	–	–	–	–	
1 (0x51)	MONDR	Monitor Data Register								
0 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	228
F (0x4F)	Reserved	–	–	–	–	–	–	–	–	
E (0x4E)	SPDR	SPI Data Register								160
D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	160
C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	158
B (0x4B)	GPIOR2	General Purpose I/O Register 2								23
A (0x4A)	GPIOR1	General Purpose I/O Register 1								23
9 (0x49)	Reserved	–	–	–	–	–	–	–	–	
8 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B								
7 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								
6 (0x46)	TCNT0	Timer/Counter0 (8-bit)								
5 (0x45)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	
4 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	
3 (0x43)	GTCCR	TSM	–	–	–	–	–	PSRASY	PSRSYNC	103/152
2 (0x42)	EEARH	(EEPROM Address Register High Byte) [5]								18
1 (0x41)	EEARL	EEPROM Address Register Low Byte								18
0 (0x40)	EEDR	EEPROM Data Register								18
F (0x3F)	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	18
E (0x3E)	GPIOR0	General Purpose I/O Register 0								23
D (0x3D)	EIMSK	–	–	–	–	–	–	INT1	INT0	81
C (0x3C)	EIFR	–	–	–	–	–	–	INTF1	INTF0	82

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
B (0x3B)	PCIFR	–	–	–	–	–	PCIF2	PCIF1	PCIF0	
A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
9 (0x39)	Reserved	–	–	–	–	–	–	–	–	
8 (0x38)	Reserved	–	–	–	–	–	–	–	–	
7 (0x37)	TIFR2	–	–	–	–	–	OCF2B	OCF2A	TOV2	151
6 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	130
5 (0x35)	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0	
4 (0x34)	Reserved	–	–	–	–	–	–	–	–	
3 (0x33)	Reserved	–	–	–	–	–	–	–	–	
2 (0x32)	Reserved	–	–	–	–	–	–	–	–	
1 (0x31)	Reserved	–	–	–	–	–	–	–	–	
0 (0x30)	Reserved	–	–	–	–	–	–	–	–	
F (0x2F)	Reserved	–	–	–	–	–	–	–	–	
E (0x2E)	Reserved	–	–	–	–	–	–	–	–	
D (0x2D)	Reserved	–	–	–	–	–	–	–	–	
C (0x2C)	Reserved	–	–	–	–	–	–	–	–	
B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	79
A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	79
9 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	79
8 (0x28)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	79
7 (0x27)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	79
6 (0x26)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	79
5 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	79
4 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	79
3 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	79
2 (0x22)	Reserved	–	–	–	–	–	–	–	–	
1 (0x21)	Reserved	–	–	–	–	–	–	–	–	
0 (0x20)	Reserved	–	–	–	–	–	–	–	–	

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1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addres should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In t registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega48/88/168 complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode fo IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/ instructions can be used.
5. Only valid for ATmega88/168

truction Set Summary

emonics	Operands	Description	Operation	Flags	#Cloc
METIC AND LOGIC INSTRUCTIONS					
	Rd, Rr	Add two Registers	Rd Rd + Rr	Z,C,N,V,H	1
	Rd, Rr	Add with Carry two Registers	Rd Rd + Rr + C	Z,C,N,V,H	1
	Rdl,K	Add Immediate to Word	Rdh:Rdl Rdh:Rdl + K	Z,C,N,V,S	2
	Rd, Rr	Subtract two Registers	Rd Rd - Rr	Z,C,N,V,H	1
	Rd, K	Subtract Constant from Register	Rd Rd - K	Z,C,N,V,H	1
	Rd, Rr	Subtract with Carry two Registers	Rd Rd - Rr - C	Z,C,N,V,H	1
	Rd, K	Subtract with Carry Constant from Reg.	Rd Rd - K - C	Z,C,N,V,H	1
	Rdl,K	Subtract Immediate from Word	Rdh:Rdl Rdh:Rdl - K	Z,C,N,V,S	2
	Rd, Rr	Logical AND Registers	Rd Rd Rr	Z,N,V	1
	Rd, K	Logical AND Register and Constant	Rd Rd K	Z,N,V	1
	Rd, Rr	Logical OR Registers	Rd Rd v Rr	Z,N,V	1
	Rd, K	Logical OR Register and Constant	Rd Rd v K	Z,N,V	1
	Rd, Rr	Exclusive OR Registers	Rd Rd Rr	Z,N,V	1
	Rd	One's Complement	Rd 0xFF Rd	Z,C,N,V	1
	Rd	Two's Complement	Rd 0x00 Rd	Z,C,N,V,H	1
	Rd,K	Set Bit(s) in Register	Rd Rd v K	Z,N,V	1
	Rd,K	Clear Bit(s) in Register	Rd Rd (0xFF - K)	Z,N,V	1
	Rd	Increment	Rd Rd + 1	Z,N,V	1
	Rd	Decrement	Rd Rd 1	Z,N,V	1
	Rd	Test for Zero or Minus	Rd Rd Rd	Z,N,V	1
	Rd	Clear Register	Rd Rd Rd	Z,N,V	1
	Rd	Set Register	Rd 0xFF	None	1
	Rd, Rr	Multiply Unsigned	R1:R0 Rd x Rr	Z,C	2
S	Rd, Rr	Multiply Signed	R1:R0 Rd x Rr	Z,C	2
SU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 Rd x Rr	Z,C	2
	Rd, Rr	Fractional Multiply Unsigned	R1:R0 (Rd x Rr) << 1	Z,C	2
LS	Rd, Rr	Fractional Multiply Signed	R1:R0 (Rd x Rr) << 1	Z,C	2
LSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 (Rd x Rr) << 1	Z,C	2
NCH INSTRUCTIONS					
P	k	Relative Jump	PC PC + k + 1	None	2
		Indirect Jump to (Z)	PC Z	None	2
)	k	Direct Jump	PC k	None	3
L	k	Relative Subroutine Call	PC PC + k + 1	None	3
		Indirect Call to (Z)	PC Z	None	3
(1)	k	Direct Subroutine Call	PC k	None	4
		Subroutine Return	PC STACK	None	4
		Interrupt Return	PC STACK	I	4
E	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC PC + 2 or 3	None	1/2/3
	Rd,Rr	Compare	Rd Rr	Z, N,V,C,H	1
	Rd,Rr	Compare with Carry	Rd Rr C	Z, N,V,C,H	1
	Rd,K	Compare Register with Immediate	Rd K	Z, N,V,C,H	1
C	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC PC + 2 or 3	None	1/2/3
S	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC PC + 2 or 3	None	1/2/3
	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC PC + 2 or 3	None	1/2/3
	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC PC + 2 or 3	None	1/2/3
S	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC PC+k + 1	None	1/2
C	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC PC+k + 1	None	1/2
Q	k	Branch if Equal	if (Z = 1) then PC PC + k + 1	None	1/2
E	k	Branch if Not Equal	if (Z = 0) then PC PC + k + 1	None	1/2
S	k	Branch if Carry Set	if (C = 1) then PC PC + k + 1	None	1/2
C	k	Branch if Carry Cleared	if (C = 0) then PC PC + k + 1	None	1/2
H	k	Branch if Same or Higher	if (C = 0) then PC PC + k + 1	None	1/2
O	k	Branch if Lower	if (C = 1) then PC PC + k + 1	None	1/2
	k	Branch if Minus	if (N = 1) then PC PC + k + 1	None	1/2
	k	Branch if Plus	if (N = 0) then PC PC + k + 1	None	1/2
E	k	Branch if Greater or Equal, Signed	if (N V= 0) then PC PC + k + 1	None	1/2
	k	Branch if Less Than Zero, Signed	if (N V= 1) then PC PC + k + 1	None	1/2
S	k	Branch if Half Carry Flag Set	if (H = 1) then PC PC + k + 1	None	1/2
C	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC PC + k + 1	None	1/2
S	k	Branch if T Flag Set	if (T = 1) then PC PC + k + 1	None	1/2
C	k	Branch if T Flag Cleared	if (T = 0) then PC PC + k + 1	None	1/2
S	k	Branch if Overflow Flag is Set	if (V = 1) then PC PC + k + 1	None	1/2
C	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC PC + k + 1	None	1/2

emonics	Operands	Description	Operation	Flags	#Clock
	k	Branch if Interrupt Enabled	if (I = 1) then PC PC + k + 1	None	1/2
	k	Branch if Interrupt Disabled	if (I = 0) then PC PC + k + 1	None	1/2
ND BIT-TEST INSTRUCTIONS					
	P,b	Set Bit in I/O Register	I/O(P,b) 1	None	2
	P,b	Clear Bit in I/O Register	I/O(P,b) 0	None	2
	Rd	Logical Shift Left	Rd(n+1) Rd(n), Rd(0) 0	Z,C,N,V	1
	Rd	Logical Shift Right	Rd(n) Rd(n+1), Rd(7) 0	Z,C,N,V	1
	Rd	Rotate Left Through Carry	Rd(0) C,Rd(n+1) Rd(n),C Rd(7)	Z,C,N,V	1
	Rd	Rotate Right Through Carry	Rd(7) C,Rd(n) Rd(n+1),C Rd(0)	Z,C,N,V	1
	Rd	Arithmetic Shift Right	Rd(n) Rd(n+1), n=0..6	Z,C,N,V	1
	Rd	Swap Nibbles	Rd(3..0) Rd(7..4),Rd(7..4) Rd(3..0)	None	1
	s	Flag Set	SREG(s) 1	SREG(s)	1
	s	Flag Clear	SREG(s) 0	SREG(s)	1
	Rr, b	Bit Store from Register to T	T Rr(b)	T	1
	Rd, b	Bit load from T to Register	Rd(b) T	None	1
		Set Carry	C 1	C	1
		Clear Carry	C 0	C	1
		Set Negative Flag	N 1	N	1
		Clear Negative Flag	N 0	N	1
		Set Zero Flag	Z 1	Z	1
		Clear Zero Flag	Z 0	Z	1
		Global Interrupt Enable	I 1	I	1
		Global Interrupt Disable	I 0	I	1
		Set Signed Test Flag	S 1	S	1
		Clear Signed Test Flag	S 0	S	1
		Set Twos Complement Overflow.	V 1	V	1
		Clear Twos Complement Overflow	V 0	V	1
		Set T in SREG	T 1	T	1
		Clear T in SREG	T 0	T	1
		Set Half Carry Flag in SREG	H 1	H	1
		Clear Half Carry Flag in SREG	H 0	H	1
TRANSFER INSTRUCTIONS					
	Rd, Rr	Move Between Registers	Rd Rr	None	1
V	Rd, Rr	Copy Register Word	Rd+1:Rd Rr+1:Rr	None	1
	Rd, K	Load Immediate	Rd K	None	1
	Rd, X	Load Indirect	Rd (X)	None	2
	Rd, X+	Load Indirect and Post-Inc.	Rd (X), X X + 1	None	2
	Rd, - X	Load Indirect and Pre-Dec.	X X - 1, Rd (X)	None	2
	Rd, Y	Load Indirect	Rd (Y)	None	2
	Rd, Y+	Load Indirect and Post-Inc.	Rd (Y), Y Y + 1	None	2
	Rd, - Y	Load Indirect and Pre-Dec.	Y Y - 1, Rd (Y)	None	2
	Rd,Y+q	Load Indirect with Displacement	Rd (Y + q)	None	2
	Rd, Z	Load Indirect	Rd (Z)	None	2
	Rd, Z+	Load Indirect and Post-Inc.	Rd (Z), Z Z+1	None	2
	Rd, -Z	Load Indirect and Pre-Dec.	Z Z - 1, Rd (Z)	None	2
	Rd, Z+q	Load Indirect with Displacement	Rd (Z + q)	None	2
	Rd, k	Load Direct from SRAM	Rd (k)	None	2
	X, Rr	Store Indirect	(X) Rr	None	2
	X+, Rr	Store Indirect and Post-Inc.	(X) Rr, X X + 1	None	2
	- X, Rr	Store Indirect and Pre-Dec.	X X - 1, (X) Rr	None	2
	Y, Rr	Store Indirect	(Y) Rr	None	2
	Y+, Rr	Store Indirect and Post-Inc.	(Y) Rr, Y Y + 1	None	2
	- Y, Rr	Store Indirect and Pre-Dec.	Y Y - 1, (Y) Rr	None	2
	Y+q,Rr	Store Indirect with Displacement	(Y + q) Rr	None	2
	Z, Rr	Store Indirect	(Z) Rr	None	2
	Z+, Rr	Store Indirect and Post-Inc.	(Z) Rr, Z Z + 1	None	2
	-Z, Rr	Store Indirect and Pre-Dec.	Z Z - 1, (Z) Rr	None	2
	Z+q,Rr	Store Indirect with Displacement	(Z + q) Rr	None	2
	k, Rr	Store Direct to SRAM	(k) Rr	None	2
		Load Program Memory	R0 (Z)	None	3
	Rd, Z	Load Program Memory	Rd (Z)	None	3
	Rd, Z+	Load Program Memory and Post-Inc	Rd (Z), Z Z+1	None	3
		Store Program Memory	(Z) R1:R0	None	-
	Rd, P	In Port	Rd P	None	1
	P, Rr	Out Port	P Rr	None	1
	Rr	Push Register on Stack	STACK Rr	None	2