P-3054

CONTROL OF DEVICES USING SPEECH RECOGNITION SYSTEM

A PROJECT REPORT

Submitted by

E.ARUNRAJ	71206106010
A.ASHOK KUMAR	71206106013
S.DEEPAN KUMAR	71206106016
S.RAMANI	71206106304

in partial fulfillment for the award of the degree

of

BACHELOR OF ENGINEERING

in

ELECTRONICS AND COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE

ANNA UNIVERSITY: CHENNAI 600 025

APRIL 2010

ANNA UNIVERSITY : CHENNAI 600 025

BONAFIDE CERTIFICATE

Certified that this project report **"CONTROL OF DEVICE USING SPEECH RECOGNITION SYSTEM"** is the bonafide work of **"E.ARUNRAJ, A.ASHOK KUMAR, S.DEEPAN KUMAR , S.RAMANI"** who carried out the project work under my supervision.

SIGNATURE

Dr. RAJESWARI MARIAPPAN Ph.d.,

HEAD OF THE DEPARTMENT

Electronics and
Communication Engineering
Kumaraguru College of Technology
Coimbatore - 641006.

SIGNATURE

Ms.R.HEMALATHA M.E.,

SUPERVISOR

SENIOR LECTURER

Electronics and
Communication Engineering
Kumaraguru College of Technology
Coimbatore - 641006.

The candidates with university register numbers **71206106010, 71206106013, 71206106016, 71206106304** were examined by us in the project viva-voce examination held on ..16-04-10...

16.04.2010
Internal Examiner

External Examiner

ACKNOWLEDGEMENT

We acknowledge our thanks to **Dr.J.SHANMUGAM Ph.d.,DIRECTOR,** Kumaraguru College of Technology, Coimbatore, for providing an opportunity to take up this project.

We acknowledge our thanks to **Dr.S.RAMACHANDRAN Ph.d., PRINCIPAL**, Kumaraguru College of Technology, Coimbatore, for providing an opportunity to take up this project.

We take this opportunity to thank, **Dr.RAJESWARI MARIAPPAN Ph.d., HEAD OF THE DEPARTMENT**, Electronics and Communication Engineering, Kumaraguru College of Technology, Coimbatore, for her extended support in completion of the project.

We wish to express our sincere thanks and deep sense of gratitude to our Project coordinator, **Ms.A.VASUKI M.E., ASST PROFESSOR,** Department of Electronics and Communication Engineering, Kumaraguru College of Technology, Coimbatore, for her wise counsel with timely and inspiring directions during this project work.

We take this opportunity to express our profound thanks to our guide **Ms.R.HEMALATHA M.E., SENIOR LECTURER** and **Mr.S.VENKATESH M.E., LECTURER** Department of Electronics and Communication Engineering, Kumaraguru College of Technology, Coimbatore, for their valuable guidance and support for the successful completion of the project work.

Finally, we express our thanks to our parents and friends for their encouragement in completion of this project work successfully.

TABLE OF CONTENT

ABSTRACT

The aim of the project is to control the devices like fan, tube light etc., for the physically challenged people through voice. Here a speech recognition kit is interfaced with the microcontroller which in turn operates the device. The relay is controlled by the microcontroller connected with the speech recognition circuit. In the speech recognition kit, HM2007 IC is used which is a speech recognition IC that will produce an 8-bit data output based on the word that has been inputted through microphone. The devices can be controlled by the command given as voice. Some of the interfacing applications which can be made are controlling home appliances, robotics movements, speech assisted technologies and many more.

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

CHAPTER 1

INTRODUCTION

1.1 BRIEF OVERVIEW:

In the near future, speech recognition will become the method of choice for controlling appliances, toys, tools, computers and robotics. There is a huge commercial market waiting for this technology to mature.

This project details the construction and building of a standalone trainable speech recognition circuit that may be interfaced to control anything, such as appliances, TVs, etc.

To command and control an appliance (fan, light, TV, etc.) by speaking to it, will make it easier, also increasing the efficiency and effectiveness of working with that device.

At its most basic level speech recognition allows the user to perform parallel tasks, while continuing to work with the computer or appliance.

The system has two sections – Speech recognition system and Microcontroller. Speech recognition system consists of IC HM2007 a speech recognition kit is interfaced with the microcontroller which in turn operates the device. The relay is controlled by the microcontroller connected with the speech recognition circuit. In the speech recognition kit, HM2007 IC is used which is a speech recognition IC that will produce an 8-bit data output based on the word that has been inputted through microphone. The devices can be controlled by the command given as voice. Some of the interfacing applications which can be made

are controlling home appliances, robotics movements, speech assisted technologies and many more.

BLOCK DIAGRAM:

The overall block diagram of the speech recognition system and the interfaces are shown in the figure 1.1.

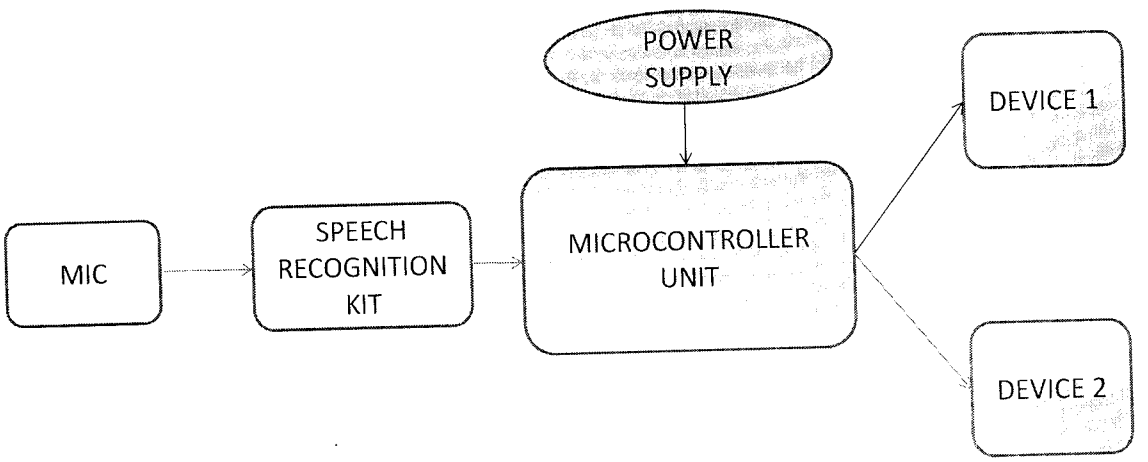


FIG 1.1 OVERALL BLOCK DIAGRAM

CHAPTER 2

POWER SUPPLY

2.1 INTRODUCTION:

This chapter introduces the operation of power supply units built using the filters, rectifiers and then voltage regulators. The ac voltage, typically 220V rms, is connected to a transformer, which steps down ac voltage to the level of the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit removes the ripples and also maintains the same dc value even if the input dc voltage varies, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of the popular voltage regulator IC units.

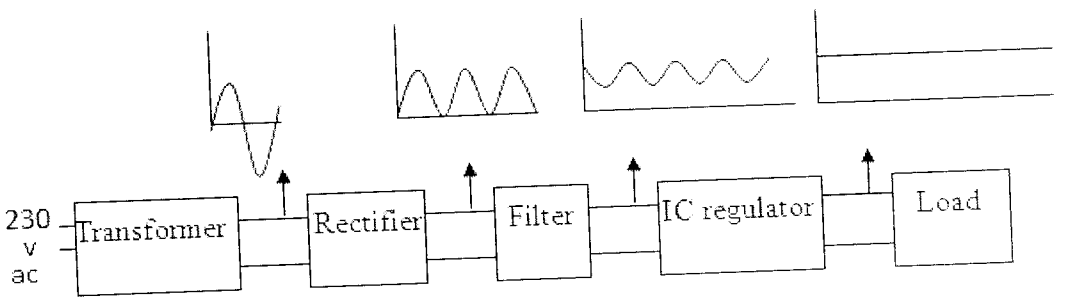


FIG 2.1 POWER SUPPLY- BLOCK DIAGRAM

2.2 CIRCUIT DIAGRAM:

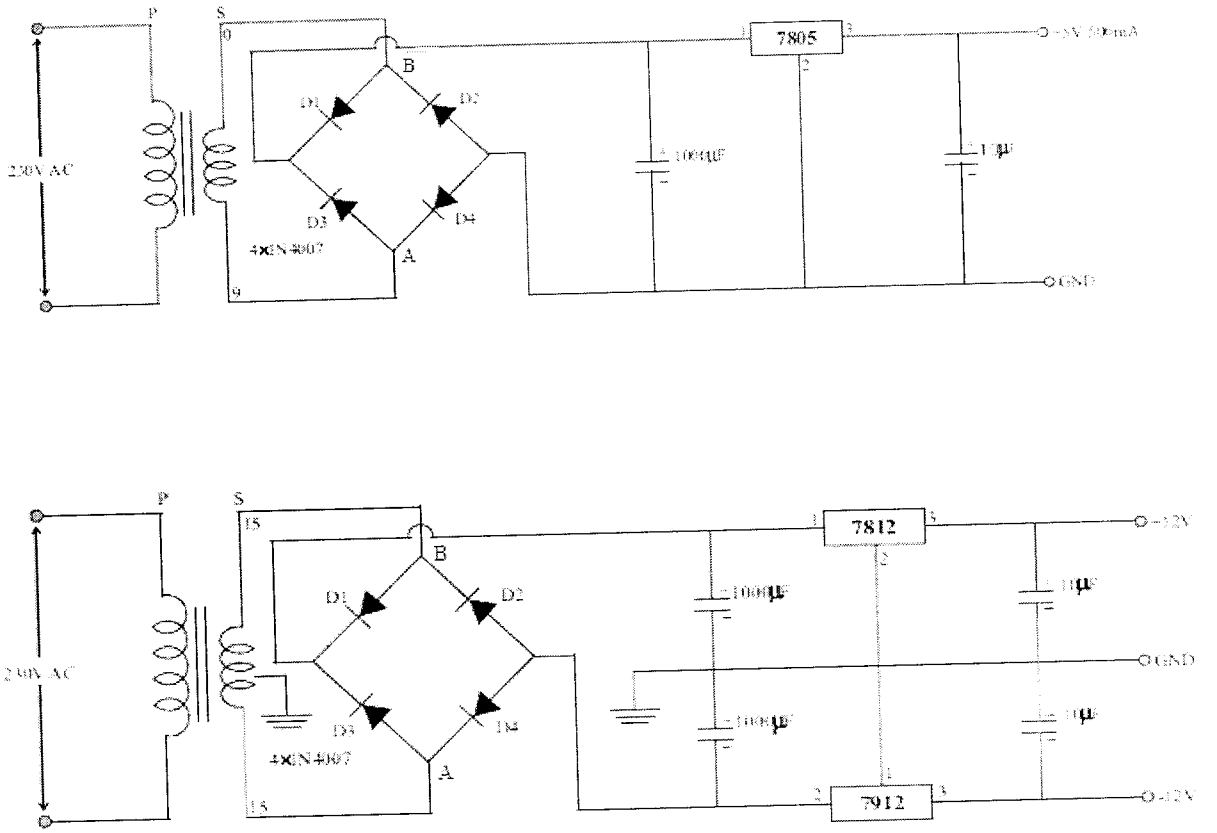


FIG 2.2 POWER SUPPLY- CIRCUIT DIAGRAM

2.3 WORKING PRINCIPLE:

TRANSFORMER:

The potential transformer will step down the power supply voltage (0-230V) to (0-6V) level. Then the secondary of the potential transformer will be connected to the precision rectifier, which is constructed with the help of op–amp. The advantages of using precision rectifier are it will give peak voltage output as dc, rest of the circuits will give only RMS output.

BRIDGE RECTIFIER:

When four diodes are connected as shown in figure 2.2, the circuit is called as bridge rectifier. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners.

Let us assume that the transformer is working properly and there is a positive potential at point A and a negative potential at point B. the positive potential at point A will forward bias D3 and reverse bias D4.

The negative potential at point B will forward bias D2 and reverse D1. At this time D3 and D2 are forward biased and will allow current flow to pass through them; D4 and D1 are reverse biased and will block current flow. During the positive half cycle the path for current flow is from point B through D1, up through R_L, through D4, through the secondary of the transformer back to point B. For the negative half cycle D2 and D3 is used for the current flow.

One-half cycle later the polarity across the secondary of the transformer reverse, forward biasing D2 and D4 and reverse biasing D1 and D3. Current flow will now be from point A through D4, up through R_L, through D2, through the secondary of T1, and back to point A. The current flow through R_L is always in the same direction. In flowing through R_L this current develops a voltage corresponding to the waveform. Since current flows through the load (R_L) during both half cycles of the applied voltage, this bridge rectifier is a full-wave rectifier.

One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit. This may be shown by as-

signing values to some of the components shown in views A and B. Assume that the same transformer is used in both circuits. The peak voltage developed between points X and Y is 1000 volts in both circuits. In the conventional full-wave circuit shown—in view A, the peak voltage from the center tap to either X or Y is 500 volts. Since only one diode can conduct at any instant, the maximum voltage that can be rectified at any instant is 500 volts.

The maximum voltage that appears across the load resistor is nearly-but never exceeds-500 volts, as result of the small voltage drop across the diode. In the bridge rectifier shown in view B, the maximum voltage that can be rectified is the full secondary voltage, which is 1000 volts. Therefore, the peak output voltage across the load resistor is nearly 1000 volts. With both circuits using the same transformer, the bridge rectifier circuit produces a higher output voltage than the conventional full-wave rectifier circuit.

IC VOLTAGE REGULATORS:

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage,

filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

THREE-TERMINAL VOLTAGE REGULATORS:

Fig 2.2 shows the connection of a three terminal voltage regulator IC to the load. The fixed voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated output dc voltage, Vo, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

TABLE 2.1 POSITIVE VOLTAGE REGULATOR IC:

IC	Output voltage	Minimum input voltage
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

The series 78 regulators provide fixed positive regulated voltages from 5 to 24 volts. Similarly, the series 79 regulators provide fixed negative regulated voltages from 5 to 24 volts.

SPEECH RECOGNITION SYSTEM

CHAPTER 3

SPEECH RECOGNITION SYSTEM

3.1 CIRCUIT DIAGRAM:

The circuit diagram of the speech recognition system is shown in the figure 3.1.

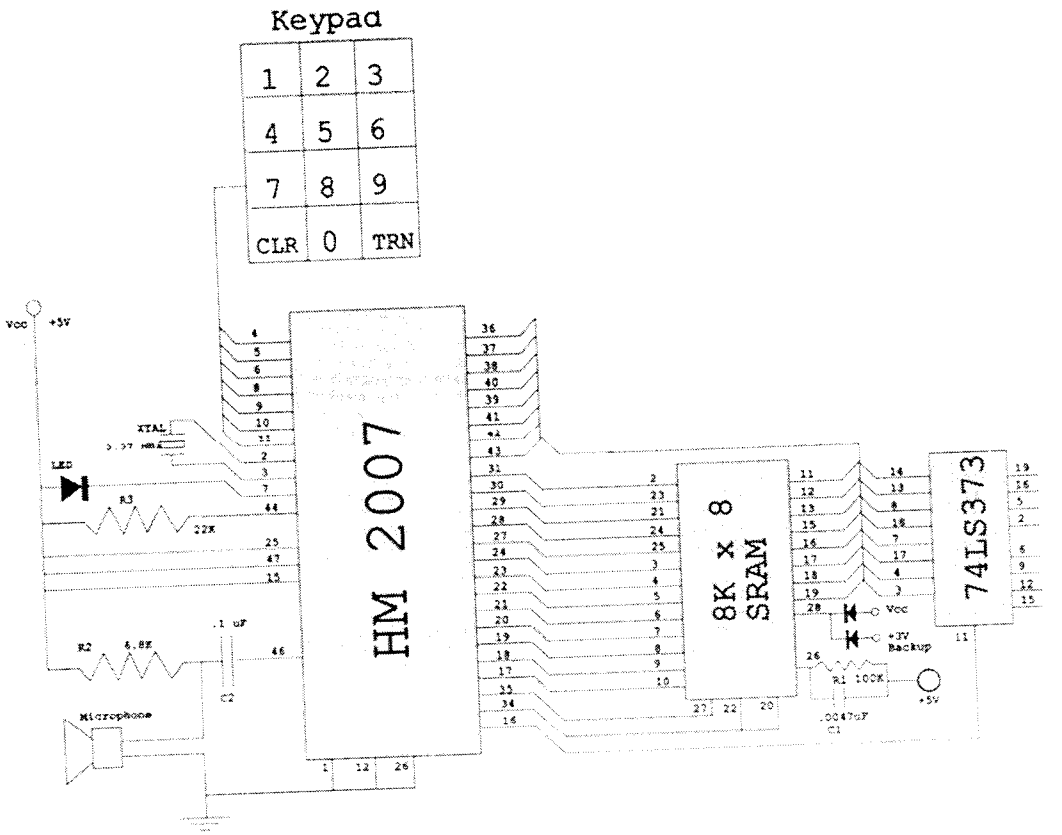


FIG 3.1 SPEECH RECOGNITION SYSTEM

3.2 FEATURES:

- Self-contained stand alone speech recognition circuit.
- User programmable.
- Up to 20 word vocabulary of duration two second each.
- Multi-lingual.
- Non-volatile memory back up with 3V battery onboard. Will keep the speech recognition data in memory even after power off.
- Easily interfaced to control external circuits & appliances.

SPECIFICATION:

Input Voltage 9 to 15 V DC Use a commonly available 12V, 500mA DC Adapter

Output Data 8 bits at 5V Logic Level

3.3 DESCRIPTION:

The speech recognition system is a completely assembled and easy to use programmable speech recognition circuit. This board allows to experiment with many facets of speech recognition technology. It has 8 bit data out which can be interfaced with any microcontroller for further development. Some of the interfacing applications which can be made are controlling home appliances, robotics movements, speech assisted technologies, speech to text translation, and many more.

USING THE SYSTEM:

The keypad and digital display are used to communicate with and program the HM2007 chip. The keypad is made up of 12 normally open momentary contact switches. When the circuit is turned on "00" is on the digital display, the red LED (READY) is lit and the circuit waits for a command.

TRAINING WORDS FOR RECOGNITION:

"1" is pressed on the keyboard and then "TRAIN" key is pressed to place the circuit in the training mode for word one. The target word should be recorded through the microphone. The circuit signals acceptance of the voice input by blinking the LED off then on. The word (or utterance) is now identified as the "01" word. Press "1" and then press "TRAIN" key if the LED does not signal the acceptance of the word. This may be continued by training words .The circuit will accept and recognize up to 20 words.

TESTING RECOGNITION:

The number of the trained words should be displayed on the LCD display once the word is repeated on the microphone. For instance, if the word "light" was trained as word number 20, saying the word "light" into the microphone will cause the number 20 to be displayed.

CLEARING MEMORY:

All the words in memory can be erased by pressing "99" and then "CLR". The numbers will quickly scroll by on the digital display as the memory is erased.

CHANGING AND ERASING THE WORDS:

Trained words can easily be changed by overwriting the original word. For instance, suppose voice six has the word "fan" and it has to be changed to the word "light", simply retraining the 6^{th} voice by saying the word "light" into the microphone will change the word. If the word has to be erased without replacing with another word, then it can be done by pressing the word number (in this case six) and then the CLR key.

SIMULATED INDEPENDENT RECOGNITION:

The speech recognition system is speaker dependant i.e., the voice that trained the system has the highest recognition accuracy. But independent speech recognition can be simulated. For making the recognition system simulate speaker independence more than one word space can be used for each target word. Now we use four word spaces per target word. Therefore we obtain four different enunciations of each target word. (speaker independent). The word spaces 01, 02, 03 and 04 are allocated to the first target word.We continue do this for the remaining word space. For instance, the second target word will use the word spaces 05, 06, 07 and 08. All the words are programmed in this manner. If you are experimenting with speaker independence use different people when training a target word. This will enable the system to recognize different voices, inflections

and enunciations of the target word. The more system resources that are allocated for independent recognition the more robust the circuit will become. If you are experimenting with designing the most robust and accurate system possible, train target words using one voice with different inflections and enunciation's of the target word.

HOMONYMS:

Homonyms are words that sound alike. For instance the words cat, bat, sat and fat sound alike. Because of their like sounding nature, they can confuse the speech recognition circuit. When choosing target words for the system, homonyms should not be used.

THE VOICE WITH STRESS & EXCITEMENT:

Stress and excitement alters ones voice. This affects the accuracy of the circuit's recognition. For instance assume you are sitting at your workbench and you program the target words like fire, left, right, forward, etc., into the circuit. Then you use the circuit to control a flight simulator game, Doom or Duke Nukem. Well, when you're playing the game you'll likely be yelling "FIRE! ...Fire! ...FIRE!!...LEFT ...go RIGHT!" In the heat of the action you're voice will sound much different than when you were sitting down relaxed and programming the circuit. To achieve a higher accuracy word recognition one needs to mimic the excitement in ones voice when programming the circuit.These factors should be kept in mind to achieve the high accuracy possible from the circuit. This becomes increasingly important when the speech recognition circuit is taken out of the lab and put to work in the outside world.

ERROR CODES:

When interfacing the external circuit through its data bus, the decoding circuit must recognize the word numbers from error codes. So the circuit must be designed to recognize error codes 55, 66 and 77 and not confuse them with word spaces 5, 6 and 7.

LEARNING TO LISTEN:

The ability to listen to one person speak among several at a party is beyond the capabilities of today's speech recognition systems. Speech recognition systems cannot separate and filter out what should be considered extraneous noise. Speech recognition does not understand speech. Understanding the meaning of words is a higher intellectual function. Because a circuit can respond to a vocal command doesn't mean it understands the command spoken. In the future, voice recognition systems may have the ability to distinguish nuances of speech and meanings of words, to "Do what I mean, not what I say!"

SPEAKER DEPENDENT / SPEAKER INDEPENDENT:

Speech recognition is divided into two broad processing categories; speaker dependent and speaker independent.

Speaker dependent systems are trained by the individual who will be using the system. These systems are capable of achieving a high command count and better than 95% accuracy for word recognition. The drawback to this approach is that the system only responds accurately only to the individual who trained the system. This is the most common approach employed in software for personal computers.

Speaker independent is a system trained to respond to a word regardless of who speaks. Therefore the system must respond to a large variety of speech patterns, inflections and enunciation's of the target word. The command word count is usually lower than the speaker dependent however high accuracy can still be maintain within processing limits. Industrial applications more often require speaker independent voice recognition systems.

RECOGNITION STYLE:

In addition to the speaker dependent/independent classification, speech recognition also contends with the style of speech it can recognize. They are three styles of speech: isolated, connected and continuous. Isolated Words are spoken separately or isolated. This is the most common speech recognition system available today. The user must pause between each word or command spoken. Connected: This is a half way point between isolated word and continuous speech recognition. It permits users to speak multiple words. The HM2007 can be set up to identify words or phrases 1.92 seconds in length. This reduces the word recognition dictionary number to 20. Continuous: This is the natural conversational speech we use to in everyday life. It is extremely difficult for a recognizer to shift through the sound as the words tend to merge together. For instance, "Hi, how are you doing?" to a computer sounds like "Hi, .howyadoin" Continuous speech recognition systems are on the market and are under continual development.

CHAPTER 4

SPEECH RECOGNITION IC HM2007

4.1 INTRODUCTION:

The HM2007 is a CMOS voice recognition LSI (Large Scale Integration) circuit. The chip contains an analog front end, voice analysis, regulation, and system control functions. The chip may be used in a stand alone or CPU connected.

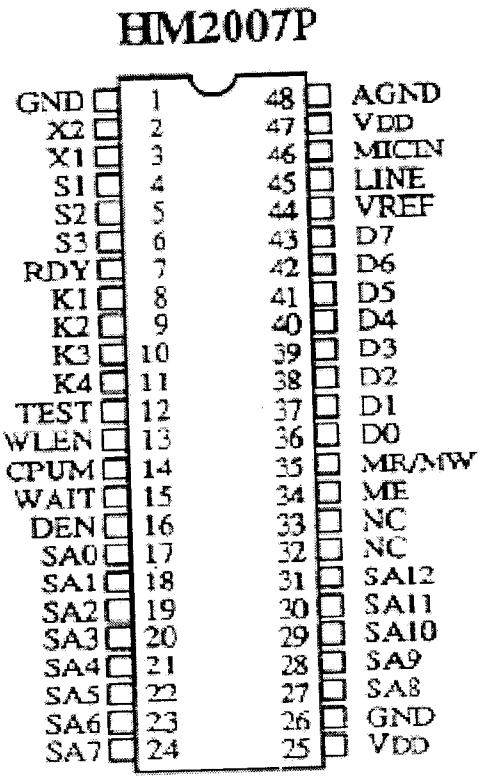


FIG 4.1 HM2007 PIN CONFIGURATION

4.2 PIN DESCRIPTION:

SYMBOL	PIN NUMBER	I/O	FUNCTION
Vref	44	I	The voltage reference input of internal ADC. Supply the reference voltage of the internal A/D converter.
LINE	45	O	For testing only
MICIN	46	I	Microphone connect pin. A microphone should be connected via a coupling capacitor and resistor.
Vdd	47		Positive power supply
AGND	48		Analog ground
GND	1		Negative power supply
X2,X1	2,3	I	Crystal connect pin. A 3.58 MHz crystal is connected to these pin.
S1,S2	4,5	I/O	Keypad scanning pin for manual mode and the read/write
S3	6		Control pins in the CPU mode
RDY	7	O	Voice input ready indicator. Active low output When HM2007 is already for the voice input i training or recognition mode, a low signal is sent. I

			the chip is busy, a high signal is sent.
K1,K2,K3,K4	8-11	I/O	The keypad pin in the manual mode and the bidirectional data bus (k-bus) in the CPU mode. In the manual mode, the four pins combined with S1 to S3 form the keypad scanning the circuit. Maximum 12 keys can be scanned. In the CPU mode, the data bus direction is determined by the S2 and S3.A high level signal that appears in the pin S2 will place the content of internal registers onto the data bus. (K-bus). The data may be come from the status register o the output buffer which is selected by the pin S1.I S1 is high, output buffer is selected .otherwise, th status register is selected. A high level signal tha appears in the pin S3 will place the content of K-bu into the input register. Note that user can not pla high level signal on S2 and S3 simultaneously.
TEST	12	I	"H": test mode ."L":Normal mode.
WLEN	13	I	Word length pin. Selecting the voice length to be recognized. Wh set to high, 1.92 sec is selected .Internally pull l for 0.9 sec is selected. Note that when 1.92 se

			selected. Only 20 words maximum can be recog-nized if 8K-byte memory is used.
CPUM	14	I	CPU mode select pin. Internally pull low for manual mode. When set to high, CPU mode is selected.
WAIT	15	I	Waiting control input. Active low input. When this pin is set to "L" and manual mode is selected,HM2007 is ready to get voice input, if this pin is set to "L",HM2007 will skip the voice input process and enter the command process.
DEN	16	O	Data enable signal. When the recognition or training process is com-plete, the chip will place its response on the data bus D0 to D7 and which can be latched onto externa devices by this pin
SA0-SA7	17-24	O	External memory address bus.
SA8-SA12	27-31		The bus is used as an external memory addres when ME pin is active.
Vdd	25		Positive power supply.
GND	26		Negative power supply

NC	32,33		No connection
ME	34	O	Memory enable pin. Active low output. This pin will send the memory enable signal to the external SRAM. This pin can be connected directly to the CE pin of 6264 SRAM
MR/MW	35	O	Memory read/write select pin. Read/write control signal of the external SRAM. This pin can be connected directly to the R/W pin of 6264 SRAM.
D0-D6	36-42	I/O	External memory data bus(D-bus)
D7	43		The bus is used as an external memory I/O bus when ME pin is active and used as output response bus when DEN pin is active

4.3 FEATURES:

- Single chip voice recognition CMOS LSI.
- Speaker dependent.
- External RAM support.
- Maximum 40 word recognition (.96 second).
- Maximum word length 1.92 seconds (20 word).
- Microphone support.
- Manual and CPU modes available.
- Response time less than 300 milliseconds.
- 5V power supply.

5.2 LOGIC BLOCK DIAGRAM

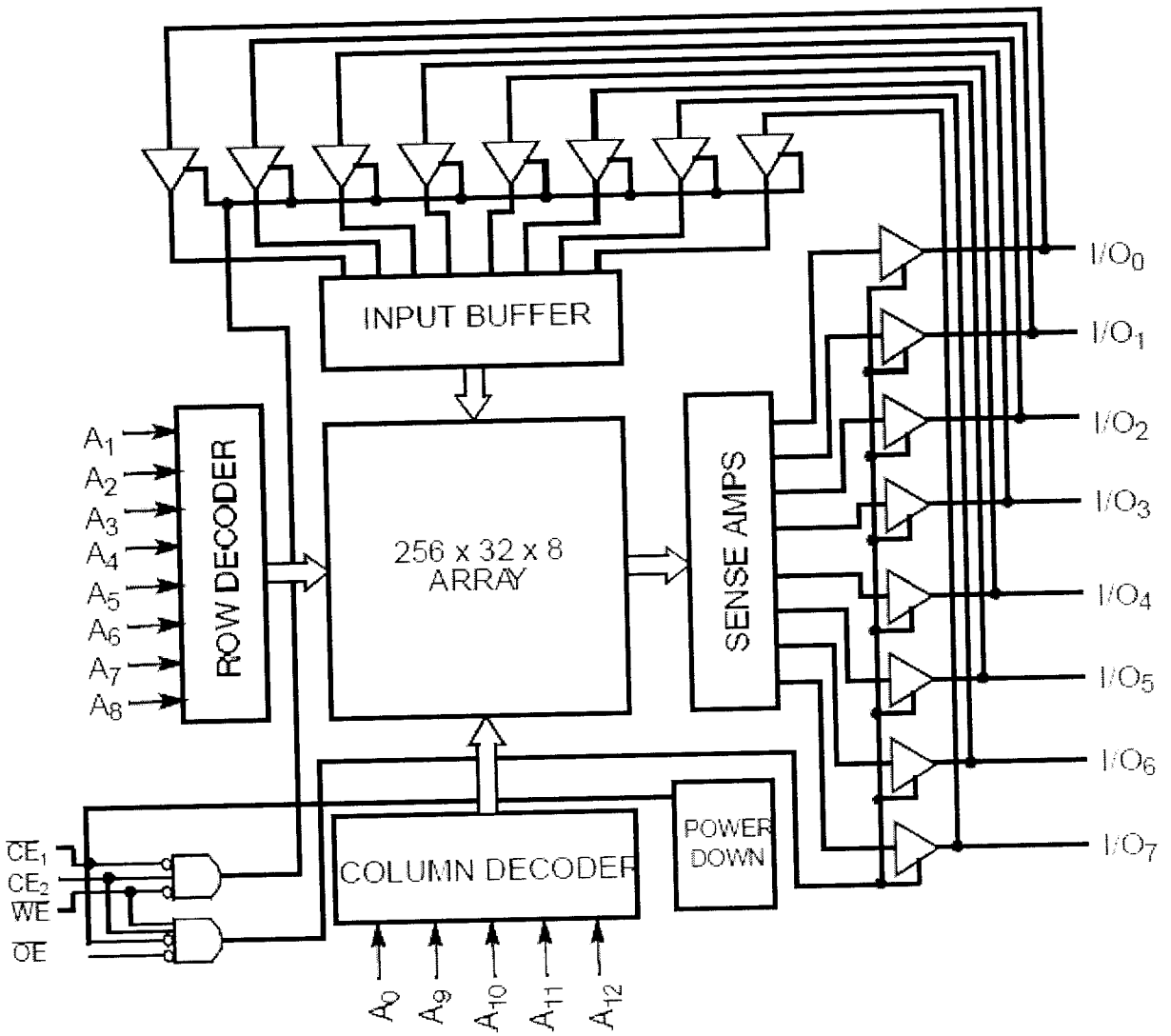


FIG 5.2 LOGIC BLOCK DIAGRAM

5.3 DESCRIPTION:

The IC6264 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE1), an active HIGH chip enable (CE2), and active LOW output enable (OE) and three-state drivers. Both devices have an automatic power- down feature (CE1), reducing the power consumption by over 70% when deselected. The 6264 is packaged in a 450-mil (300-mil body) SOIC. An active LOW write enable signal (WE) controls the writing/ reading operation of the memory. When CE1 and WE inputs are both LOW and CE2 is HIGH, data on the eight data input/output pins (I/O0 through I/O7) is written into the memory location addressed by the address present on the address pins (A0 through A12). Reading the device is accomplished by selecting the device and enabling the outputs, CE1 and OE active LOW, CE2 active HIGH, while WE remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins. The input/output pins remain in a high-impedance state unless the chip is selected; outputs are enabled, and write enable (WE) is HIGH. A die coat is used to insure alpha immunity.

CHAPTER 6

MICROCONTROLLER

1 ARCHITECTURE OF 8051:

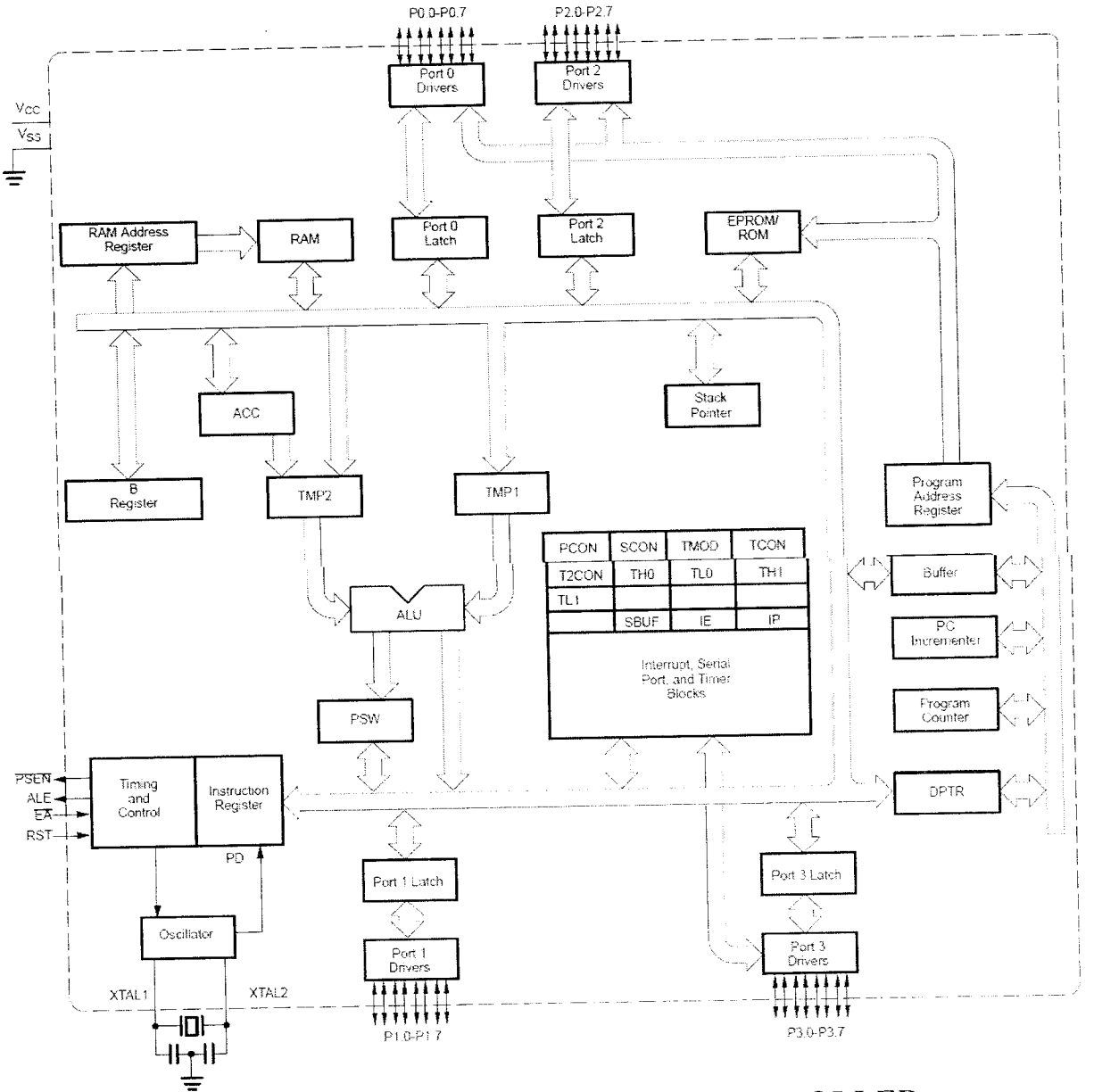


FIG 6.1 ARCHITECTURE OF MICROCONTROLLER

6.2 DESCRIPTION:

This provides a detailed description of the 80C51 microcontroller included in this description are:

- The port drivers and how they function both as ports and, for Ports 0 and 2, in bus operations
- The Timers/Counters
- The Serial Interface
- The Interrupt System
- Reset
- The Reduced Power Modes in CMOS devices
- The EPROM version of the 80C51

SPECIAL FUNCTION REGISTERS:

A Map of the on-chip memory area called the Special Function Register (SFR) space. Note that in the SFRs not all of the addresses are occupied.Unoccupied addresses are not implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have no effect.User software should not write 1s to these unimplemented locations,since they may be used in other 80C51 Family derivative products to invoke new features. The functions of the SFRs are described in the text that follows.

ACCUMULATOR:

ACC is the Accumulator register. The mnemonics for Accumulator Specific instructions, however, refer to the Accumulator simply as A.

B REGISTER:

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

PROGRAM STATUS WORD:

The PSW register contains program status information.

STACK POINTER:

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at locations 08H.

DATA POINTER:

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit register.

PORTS 0 TO 3:

P0, P1, P2, and P3 are the SFR latches of Ports 0, 1, 2, and 3, respectively. Writing a one to a bit of a port SFR (P0, P1, P2, or P3) causes the corresponding port output pin to switch high. Writing a zero causes the port output pin to switch low. When used as an input, the external state of a port pin will be held in the port SFR (i.e., if the external state of a pin is low, the corresponding port SFR bit will contain a 0; if it is high, the bit will contain a 1).

SERIAL DATA BUFFER:

The Serial Buffer is actually two separate registers, a transmit buffer and a receive buffer. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

TIMER REGISTERS BASIC TO 80C51:

Register pairs (TH0, TL0), and (TH1, TL1) are the 16-bit Counting registers for Timer/Counters 0 and 1, respectively.

CONTROL REGISTER FOR THE 80C51:

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port.

PORT STRUCTURES AND OPERATION:

All four ports in the 80C51 are bidirectional. Each consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer. The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the Port 2 pins continue to emit P2 SFR content.

All the Port 3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed below:

PORT PIN ALTERNATE FUNCTION:

P3.0 RxD (serial input port)

P3.1 TxD (serial output port)

P3.2 INT0 (external interrupt)

P3.3 INT1 (external interrupt)

P3.4 T0 (Timer/Counter 0 external input)

P3.5 T1 (Timer/Counter 1 external input)

P3.6 WR (external Data Memory write strobe)

P3.7 RD (external Data Memory read strobe)

The alternate functions can only be activated if the corresponding bitlatch in the port SFR contains a 1. Otherwise the port pin remains at 0.

I/O CONFIGURATIONS:

A functional diagram of typical bit latch and I/O buffer in each of the four ports. The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which will clock in a value from the internal bus in response to a "write to latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read pin" signal from the CPU. Some instructions that read a port activate the "read latch" signal, and others activate the "read pin" signal. The output drivers of Port 0 and 2 are switchable to an internal ADDR and ADDR/DATA bus by an internal CONTROL signal for use in external memory accesses. During external memory accesses, the P2 SFR remains unchanged, but

ACCESSING EXTERNAL MEMORY:

Accesses to external memory are of two types: accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal PSEN (program store enable) as the read strobe. Accesses to external Data Memory use RD or WR (alternate functions of P3.7 and P3.6) to strobe the memory. Fetches from external Program Memory always use a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @ DPTR) or an 8-bit address (MOVX @Ri).

Whenever a 16-bit address is used, the high bytes of the address comes out on Port 2, where it is held for the duration of the read or write cycle. Note that the Port 2 drivers use the strong pullups during the entire time that they are emitting address bits that are 1s. This is during the execution of a MOVX @DPTR instruction. During this time the Port 2 latch (the Special Function Register) does not have to contain 1s and the contents of the Port 2 SFR are not modified. If the external memory cycle is not immediately followed by another external memory cycle, the undisturbed contents of the Port 2 SFR will reappear in the next cycle. If an 8-bit address is being used (MOVX @Ri), the contents of the Port 2 SFR remain at the Port 2 pins throughout the external memory cycle.

In any case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDR/DATA signals drive both FETs in the Port 0 output buffers. Thus, in this application the Port 0 pins are not open-drain outputs, and do not require external pullups. ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written

the P0 SFR gets 1s written to it. If a P3 bit latch contains a 1, then the output level is controlled by the signal labeled "alternate output function." The actual P3.X pin level is always available to the pin's alternate input function, if any. Ports 1, 2, and 3 have internal pullups, and Port 0 has open drain outputs. Each I/O line can be independently used as an input or an output. (Port 0 and 2 may not be used as general purpose I/O when being used as the ADDR/DATA BUS for external memory during normal operation.) To be used as an input, the port bit latch must contain a 1, which turns off the output driver FET. Then, for Ports 1, 2, and 3, the pin is pulled high by a weak internal pullup, and can be pulled low by an external source. Port 0 differs in that its internal pullups are not active during normal port operation. The pullup FET in the P0 output driver is used only when the port is emitting 1s during external memory accesses. Otherwise the pullup FET is off. Consequently P0 lines that are being used as output port lines are open drain. Writing a 1to the bit latch leaves both output FETs off, so the pin floats. In that condition it can be used as a high-impedance input. Because Ports 1, 2, and 3 have fixed internal pullups, they are sometimes called "quasi- bidirectional" ports. When configured as inputs they pull high and will source current when externally pulled low. Port 0, on the other hand, is considered "true" bidirectional, because when configured as an input it floats. All the port latches in the 80C51 have 1s written to them by the reset function. If a 0 is subsequently written to a port latch, it can be reconfigured as an input by writing a 1 to it.

WRITING TO A PORT:

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6P2 of the final cycle of the

instruction. However, port latches are in fact sampled by their output buffers only during Phase 1 of a clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1). Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle. If the change requires a 0-to-1 transition in Port 1, 2, or 3, an additional pullup is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pullup can source about 100 times the current that the normal pullup can. It should be noted that the internal pull-ups are field-effect transistors, not linear resistors.

PORT LOADING AND INTERFACING:

The output buffers of Ports 1, 2, and 3 can each drive 4 LS TTL inputs. These ports on NMOS versions can be driven in a normal manner by a TTL or NMOS circuit. Both NMOS and CMOS pins can be driven by open-collector and open-drain outputs, but note that 0-to-1 transitions will not be fast. In the NMOS device, if the pin is driven by an open-collector output, a 0-to-1 transition will have to be driven by the relatively weak depletion mode FET. In the CMOS device, an input 0 turns off pullup pFET3, leaving only the very weak pullup pFET2 to drive the transition. Port 0 output buffers can each drive 8 LS TTL inputs. They do, however, require external pullups to drive NMOS inputs, except when being used as the ADDRESS/DATA bus for external memory.

READ-MODIFY-WRITE FEATURE:

Some instructions that read a port read the latch and others read the pin. The instructions that read the latch rather than the pin are the ones that read a value,

possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port, or a port bit, these instructions read the latch rather than the pin:

ANL (logical AND, e.g., ANL P1, A)

ORL (logical OR, e.g., ORL P2,A)

XRL (logical EX-OR, e.g., XRL P3,A)

JBC (jump if bit = 1 and clear bit, e.g., JBC P1.1,LABEL)

CPL (complement bit, e.g., CPL P3.0)

INC (increment, e.g., INC P2)

DEC (decrement, e.g., DEC P2)

DJNZ (decrement and jump if not zero)

MOV PX.Y,C (move carry bit to bit Y of Port X)

CLR PX.Y (clear bit Y of Port X)

SET PX.Y (set bit Y of Port X)

It is not obvious that the last three instructions in this list are read modify-write instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, and then write the new byte back to the latch.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

software should not write 1s to these positions, since they may be used in other 8051 family products.

HOW INTERRUPTS ARE HANDLED:

The interrupt flags are sampled at S5P2 of every machine cycle.The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered.

The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

Mode 0 operation is the same for the Timer 0 as for Timer 1. Substitute TR0, TF0, and INT0 for the corresponding Timer 1 signals. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

MODE 1:

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

MODE 2:

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 9. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged. Mode 2 operation is the same for Timer/Counter 0.

MODE 3:

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters.TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0.TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the "Timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. With Timer 0 in Mode 3, an 80C51 can look like it has three Timer/Counters.

appears on Port 0 just before WR is activated, and remains there until after WR is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated.

During any access to external memory, the CPU writes 0FFH to the Port 0 latch (the Special Function Register), thus obliterating whatever information the Port 0 SFR may have been holding.

External Program Memory is accessed under two conditions:
Whenever signal EA is active; or whenever the program counter (PC) contains a number that is larger than 0FFFH (in the 80C51). This require that the ROMless versions have EA wired low to enable the lower 4k program bytes to be fetched from external memory.

When the CPU is executing out of external Program Memory, all 8 bits of Port 2 are dedicated to an output function and may not be used for general purpose I/O. During external program fetches they output the high byte of the PC. During this time the Port 2 drivers use the strong pullups to emit PC bits that are 1s.

TIMER/COUNTERS:

The 80C51 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters.

In the "Timer" function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.In the "Counter" function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1.

When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full cycle. In addition to the "Timer"or "Counter" selection, Timer 0 and Timer 1 have four operating modes from which to select.

TIMER 0 AND TIMER 1:

The "Timer" or "Counter" function is selected by control bits C/T in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different.

MODE 0:

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or INT1 = 1. (Setting GATE = 1 allows the Timer to be controlled by external input INT1, to facilitate pulse width measurements). TR1 is a control bit in the Special Function Register TCON. GATE is in TMOD.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

INTERRUPTS:

The 80C51 provides 5 interrupt sources. The External Interrupts INT0 and INT1 can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, ratherthan the on-chip hardware.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except see Timer 0 in Mode 3). When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored. The Serial Port Interrupt is generated by the logical OR of RI and TI.Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI or TI that generated the interrupt and the bit will have to be cleared in software. All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

PRIORITY LEVEL STRUCTURE:

Each interrupt source can be individually programmed to one of two priority levels by setting or clearing a bit in Special Function Register IP. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.If two request of different priority levels are received simultaneously; the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as follows:

Source Priority within Level

1. IE0 (highest)
2. TF0
3. IE1
4. TF1
5. RI+TI (lowest)

Note that the "priority within level" structure is only used to resolve simultaneous requests of the same priority level.The IP register contains a number of unimplemented bits. IP.7, IP.6, and IP.5 are reserved in the 80C51. User

CHAPTER 7

LCD DISPLAY

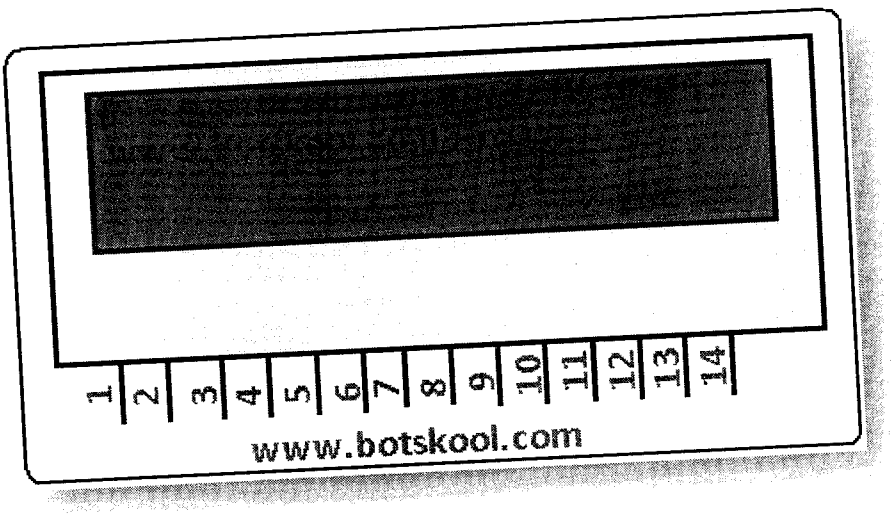


FIG 7.1 LCD DISPLAY

An **HD44780 Character LCD** is an industry standard liquid crystal display (LCD) device designed for interfacing with embedded electronics. These screens come in common configurations of 8x1 characters, 16x2, and 20x4 among others. The largest such configuration is 40x4 characters, but these are rare and are actually two separate 20x4 screens seamlessly joined together.

These screens are often found in copiers, fax machines, laser printers, industrial test equipment, networking equipment such as routers and storage devices, etc. These are not the kind of screens one would find in a cell phone, portable television, etc. They are limited to text only, with 8 customizable characters. Character LCDs can come with or without backlights. Backlights can be LED, fluores-

cent, or electroluminescent. Character LCDs use a standard 14-pin interface. If the screen has a backlight, it will have 16 pins. The pin outs are as follows:

1. Ground
2. VCC (+5V)
3. Contrast adjustment
4. Register Select (R/S)
5. Read/Write (R/W)
6. Clock (Enable)
7. Bit 0
8. Bit 1
9. Bit 2
10. Bit 3
11. Bit 4
12. Bit 5
13. Bit 6
14. Bit 7

Character LCDs can operate in 4-bit or 8-bit mode. In 4 bit mode, pins 7 through 10 are unused and the entire byte is sent to the screen using pins 11 through 14 by sending a nibble at a time.

The most commonly used LCDs found in the market today are 1 Line, 2 Line or 4 Line LCDs which have only one controller and support at most 80 characters, whereas LCDs supporting more than 80 characters make use of 2 HD44780 controllers. Apart from displaying some simple static characters animated text scripts can be created.

Most LCDs with 1 controller has 14 Pins and 16 Pins (two extra pins are for back-light LED connections). Pin description is shown in figure 7.2.

Pin No.	Name	Description
1	VSS	GND
2	VCC	+5V
3	VEE	Contrast adjust
4	RS	0 = Command register 1 = Data register
5	R/W	0 = Write to LCD module 1 = Read from LCD module
6	EN	Enable
7	D0	Data bus line 0 (LSB)
8	D1	Data bus line 1
9	D2	Data bus line 2
10	D3	Data bus line 3
11	D4	Data bus line 4
12	D5	Data bus line 5
13	D6	Data bus line 6
14	D7	Data bus line 7 (MSB)

www.botskool.com

FIG 7.2: PIN DESCRIPTION OF LCD DISPLAY

READ/WRITE (RW):

1.) RW= 0, the information is being written on LCD.

2.) RW=1, for reading from LCD. (Only one command that is "Get LCD status" is read commands all others are write command)

Read/Write is a control line. When RW is low (0), the information on the data bus is being written to the LCD. When RW is high (1), the program is effectively querying (or reading from) the LCD. Only one instruction ("Get LCD status") is a read command. All others are write commands, so RW will be low for majority of the time.

REGISTERS:

There are two very important registers in the LCD. The RS pin is used for their selection.

1.) RS= 0; The Instruction command code register, allows the user to send command such as clear display, cursor at home, etc.

2.) RS=1; the data register, allow user to send data to be displayed at LCD.

ENABLE (EN) PIN:

It is used to tell the LCD that we are sending it data. To enable LCD, a high to low pulse (of minimum length 450ns) should be given before sending any command/data to LCD.

STEPS TO PROGRAM:

1) Initialize the LCD.

2) Select the command or instruction register.

3) Set RW low (to write).

4) Send a high to low pulse on Enable pin.

5) Check if the LCD is busy.

6) Move to instruction or command function.

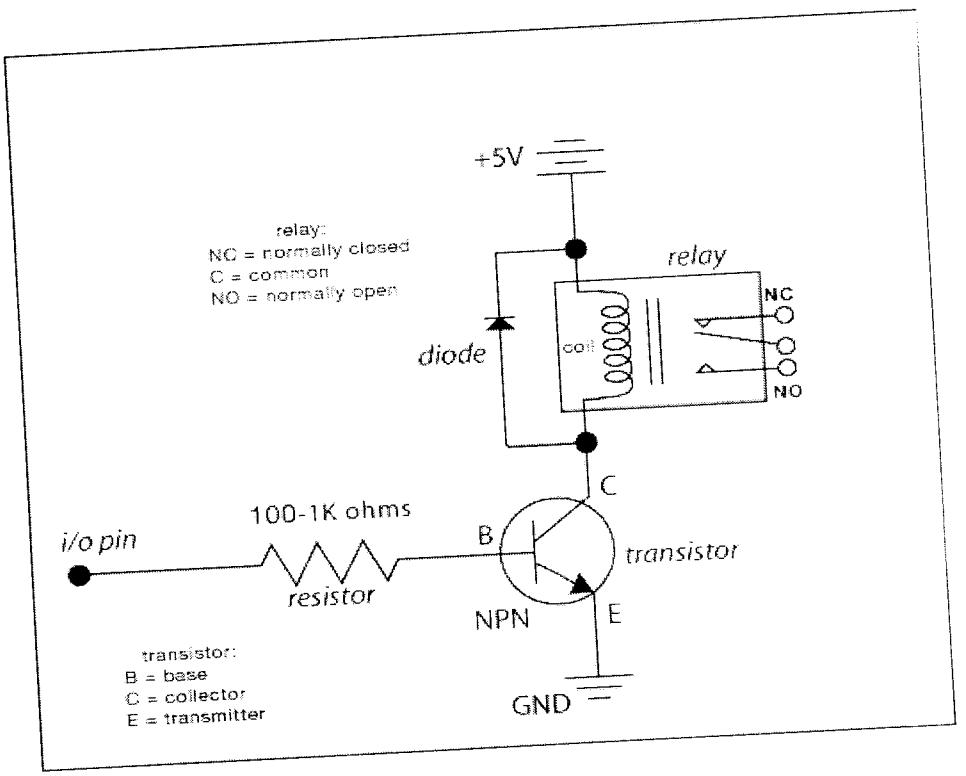
7) Repeat steps 4-7.

CHAPTER 8
RELAY

8.1 INTRODUCTION:

When a coil of wire is wound on a non-magnetic material such as plastic, paper etc, it is called an air-core solenoid or simply a solenoid. If a soft iron core is inserted into the coil, it becomes an electromagnet. This electromagnet is a basic component for relay and many other electromechanical devices such as electric bell circuit breaker etc.

8.2 RELAY CIRCUIT



8.3 OPERATION OF RELAY CIRCUIT

A relay is an **electrically operated switch**. Current flowing through the coil of the relay creates a magnetic field which attracts a lever and changes the switch contacts. The coil current can be on or off so relays have two switch positions and they are **double throw (changeover)** switches.

Relays allow one circuit to switch a second circuit which can be completely separate from the first. For example a low voltage battery circuit can use a relay to switch a 230V AC mains circuit. There is no electrical connection inside the relay between the two circuits; the link is magnetic and mechanical.

When a current flows through the coil, the resulting magnetic field attracts an armature that is mechanically linked to a moving contact. The movement either makes or breaks a connection with a fixed contact. When the current to the coil is switched off, the armature is returned by a force approximately of as strong as the magnetic force to its relaxed position .Usually this is a spring, but gravity is also used commonly in the industrial motor starters. Most relays are manufactured to operate quickly .In a low voltage application, this is to reduce noise. In a high voltage or high current application, this is to reduce to arcing.

CHAPTER 9

FLIP FLOP

9.1 PIN CONFIGURATION:

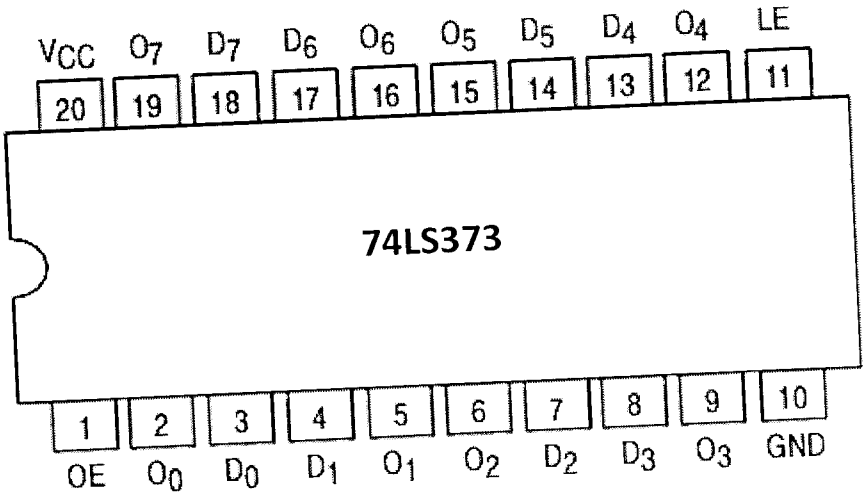


FIG 9.1 PIN CONFIGURATION

9.2 DESCRIPTION:

The 74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output

Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

FEATURES:

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

HARDWARE INTERFACING AND IMPLEMENTATION

CHAPTER 10
HARDWARE IMPLEMENTATION AND INTERFACING

Initially the voice is given as input to the speech recognition system through the microphone. The speech recognition system is interfaced with the microcontroller which in turn operates the device. In the speech recognition system, the voice is stored using the SRAM. Speech recognition IC HM2007 is the heart of the speech recognition system, which is used to recognize the voice. When the voice is recognized during the process, the corresponding location where that voice is present, is displayed in the LCD display. The output from the speech recognition system is an 8-bit data which indicates the location of the voice in the speech system. This output is given to the microcontroller. The microcontroller has been programmed in such a way that a particular output port will be enabled based on the output from the speech recognition system. Now the corresponding relay will be enabled by the microcontroller output. The relay is used to switch on and off the appliance.

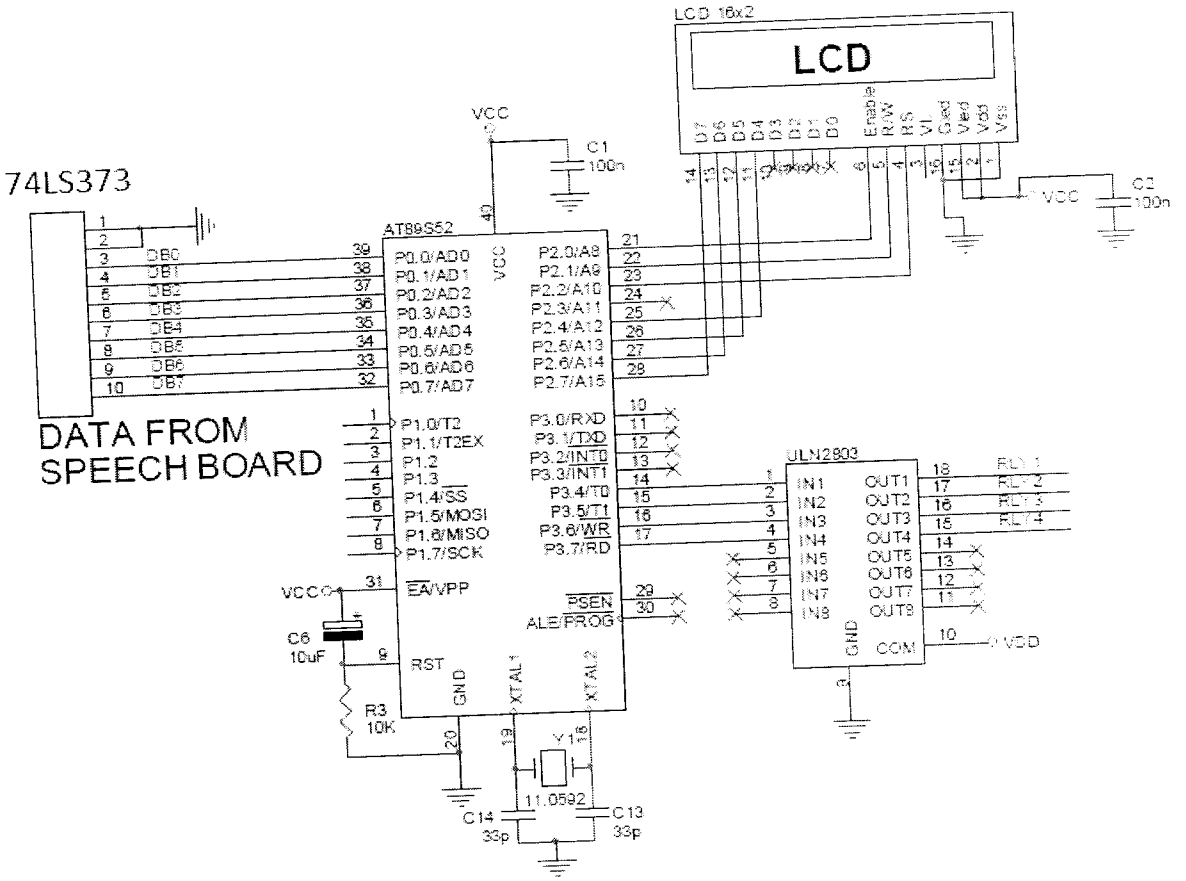


FIG 10.1 HARDWARE INTERFACING

CHAPTER 11

PROCESS FLOW

11.1 PSEUDO CODE:

STEP 1: Initialize, get the data from the speech recognition kit.

STEP 2: Check for the validation of the voice data.

STEP 3: Display the error code when voice is not valid.

STEP 4: When data is valid, display the corresponding stored number.

STEP 5: When voice1 is recognized, turn on the relay1.

STEP 6: When voice2 is recognized, turn off the relay1.

STEP 7: Repeat the same process for consecutive number of times for all the devices.

11.2 FLOWCHART:

FIG 11.1 TRAINING WORDS FOR RECOGNITION:

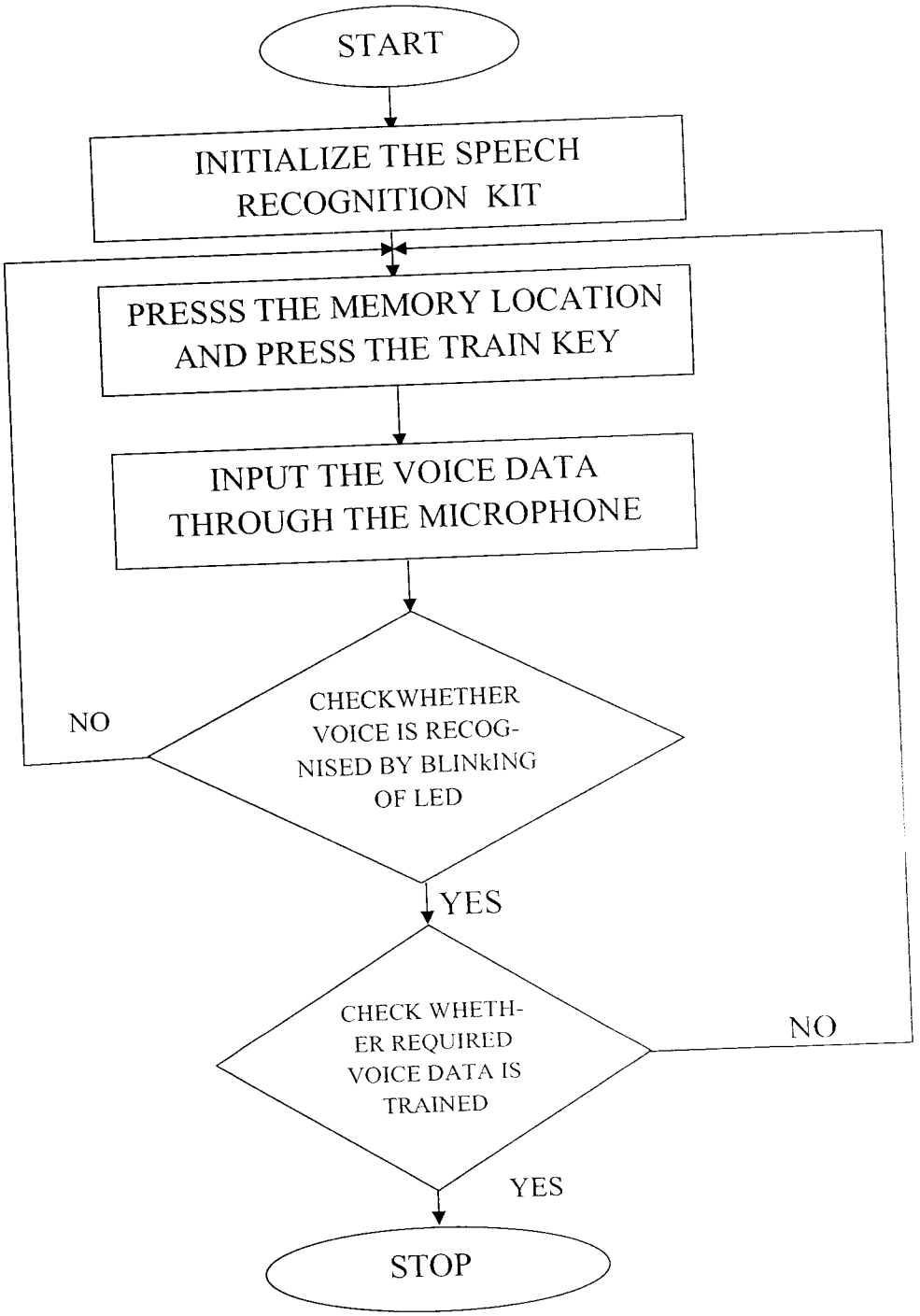
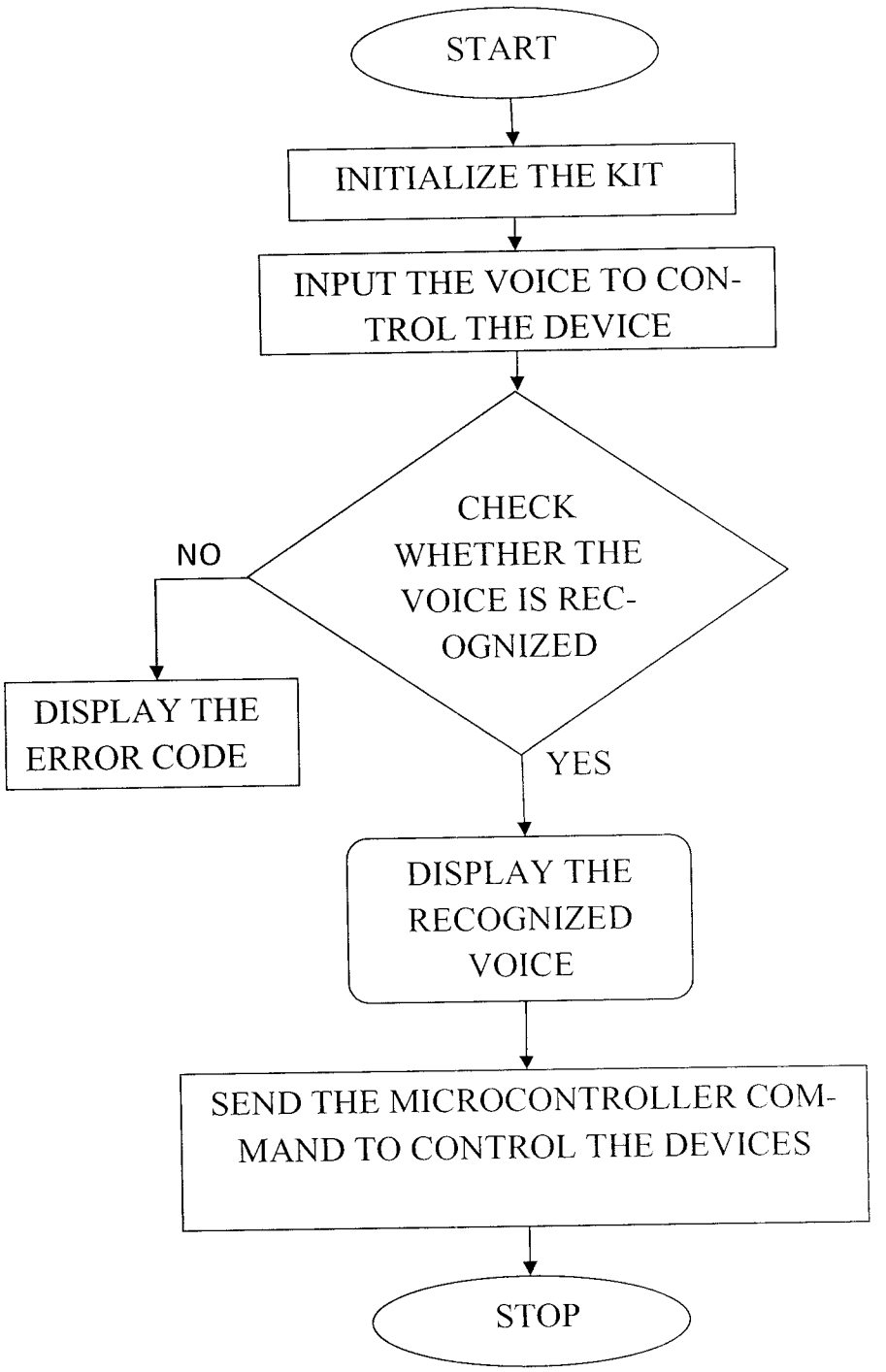


FIG 11.2 TESTING RECOGNITION



ADVANTAGES AND FUTURE CONSIDERATION

CHAPTER 12
APPLICATIONS AND FUTURE CONSIDERATION

12.1 APPLICATIONS:

There are several areas for application of voice recognition technology.

- Speech controlled appliances and toys
- Speech assisted computer games
- Speech assisted virtual reality
- Telephone assistance systems
- Voice recognition security

12.2 FUTURE CONSIDERATION:

SPEECH RECOGNITION SECURITY SYSTEM:

'Face recognition' along with the speech recognition system will provide an effective security system. Suppose the task is to control 'robot' or just 'small toy car' but in security system. The user's images will be already saved in the database and if the face is matched with the original, then user's login code will be sent to 'speech interaction system' from 'face recognition', and through that code specific commands which was allowed to that user will only work. Also his profile will be pronounced by 'speech interaction system' after login the user for better understanding.

CONCLUSION

CHAPTER 13

CONCLUSION

The implementation of device control for the physically challenged people through voice is done efficiently. The project has been designed for the multiple devices. A low cost, reliable and efficient device for controlling any electrical appliances is achieved using this project.

REFERENCES

[1] Kenneth J.Ayala "The 8051 Microcontroller:Architecture,Programming and Applications "

[2 James W.stewart,Kai X.Miao"8051 Microcontroller,The Hardware,Software,Interfacing&Applications"

[3]Data sheet of HM2007 www.datasheetcatalog.com/datasheets/HM2007

[4]Data sheet of IC 6264 www.alldatasheet.com

/