ICROCONTROLLER BASED AUTOMATIC CLEANING SYSTEM OF PREDEFINED SPACE

A PROJECT REPORT

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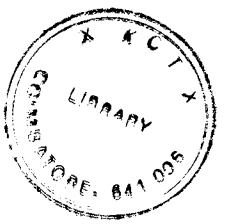

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ABSTRACT

In the present scenario, due to busy schedule people neither have the time nor energy to do their house hold work .Cleaning is one such job that demands a lot of human effort.

To bring a solution, this project would serve as a substitute in cleaning the floor and which would be cheap and convenient for a common man to purchase in the market. It is decided to design and build a microcontroller based automatic system capable of cleaning the floor of a predefined area without any human interaction other than just starting the system.

The robot works by incorporating three mechanisms. First, the robot should move in a defined path with the position of the obstacles being known. This is done using robot and feedback mechanisms. Next it should clean the surface simultaneously, while in motion and this is called as sweep mechanism. When it detects an unknown obstacle it gives a buzzer sound.

LIST OF FIGURES

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ABBREVIATIONS

IPS	INDUCTIVE PROXIMITY SENSORS
IR	INFRA RED
RAM	RANDOM ACCESS MEMORY
CMOS	COMPLIMENTARY METAL OSIDE SEMICONDUCTOR
TTL	TRISTATE TRANSISTOR LOGIC
UART	UNIVERSAL ASYNCHRONOUS RECIEVER TRANSMITTER
INT	INTERRUPT

Chapter 1

INTRODUCTION

1.1 Robotics

Robotics can be defined as the science or study of the technology primarily associated with the design, fabrication, theory, and application of robots.

A Robot is a mechatronic device which also includes resourcefulness or autonomy. A device with autonomy does its thing "on its own" without a human directly guiding it moment-by-moment.

A mechatronic Device is a degenerate robot with these components:

1. Sensors, which detect the state of the environment
2. Actuators, which modify the state of the environment
3. A Control System, which controls the actuators based on the environment as depicted by the sensors

Two main categories of robots:

1. **Machine pet:** A machine, capable of moving in some way, that it can sense its surroundings and can act on what it senses autonomously. Most of these robots have no real useful purpose, other than to entertain and challenge. These are also commonly used for experimenting with sensors, artificial intelligence, actuators and more.

2. **Autonomous machine:** A machine with sensors and actuators that can do some sort of work "on its own". This includes things like robotic lawn mowers, pick and place robot and also self-operating construction machines such as CNC cutters. Most industrial and commercial robots fall in this category.

Three laws of robotics – by Issac Asimov

1. A robot may not injure a human being or, through inaction, allow a human being to come to harm.
2. A robot must obey any orders given to it by human beings, except where such orders would conflict with the First Law.
3. A robot must protect its own existence as long as such protection does not conflict with the First or Second Law

Since this project is an automatic device capable of sensing the environment and moving on its own without human interaction along with a useful purpose it comes under the autonomous machine category of robotics. The system designed obeys the three laws of robotics.

1.2 Project Goal

The goal of our project is as follows

1. To clean a room that has its dimensions predefined.

2. To clean the room in a specified path, the one chosen in our project is a helix. The path starts from the door of the room and terminates at the centre covering the entire area to the maximum.

3. Since a room would have many things that would remain stationary, for eg tables, chairs. These items are considered as known obstacles. Their dimensions would be programmed so that the robot would turn without a collision and the whole area will be cleaned.

4. When there is an unknown obstacle, the device has to detect it, stop the rotation of its wheels and the cleaning mechanism and finally give an indication to the user to remove the unknown obstacle.

5. To differentiate the buzzer sounds to the user, so that he is clear whether there is an unknown obstacle or if the cleaning of the entire room is completed.

1.2.1Defined path

The room dimensions and the path for which our robot is programmed is shown in Fig.1.1

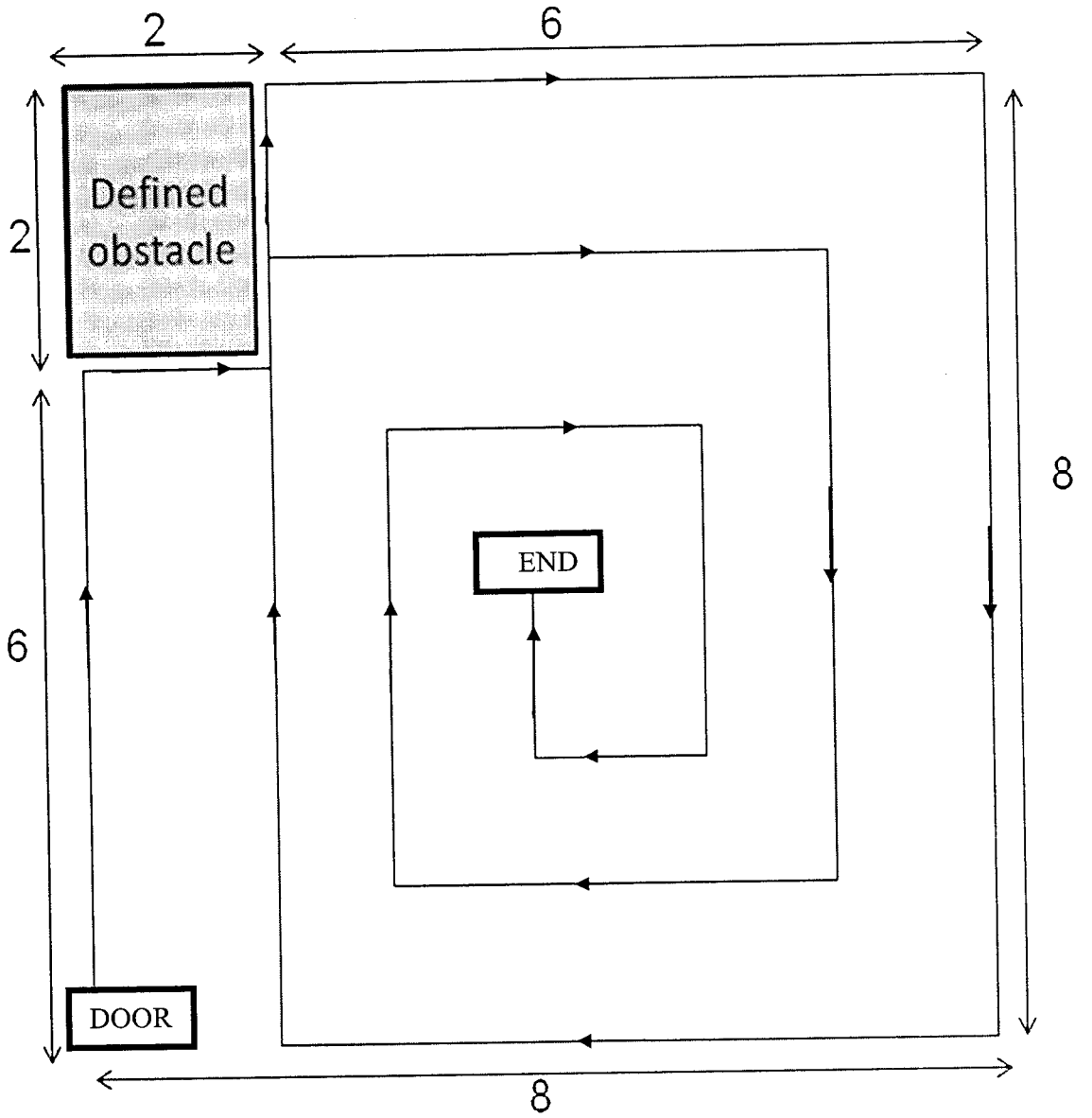


Fig.1.1 ROBOT PATH

DIMENSIONS: IN FEET

1.2.2 Surface cleaning tool

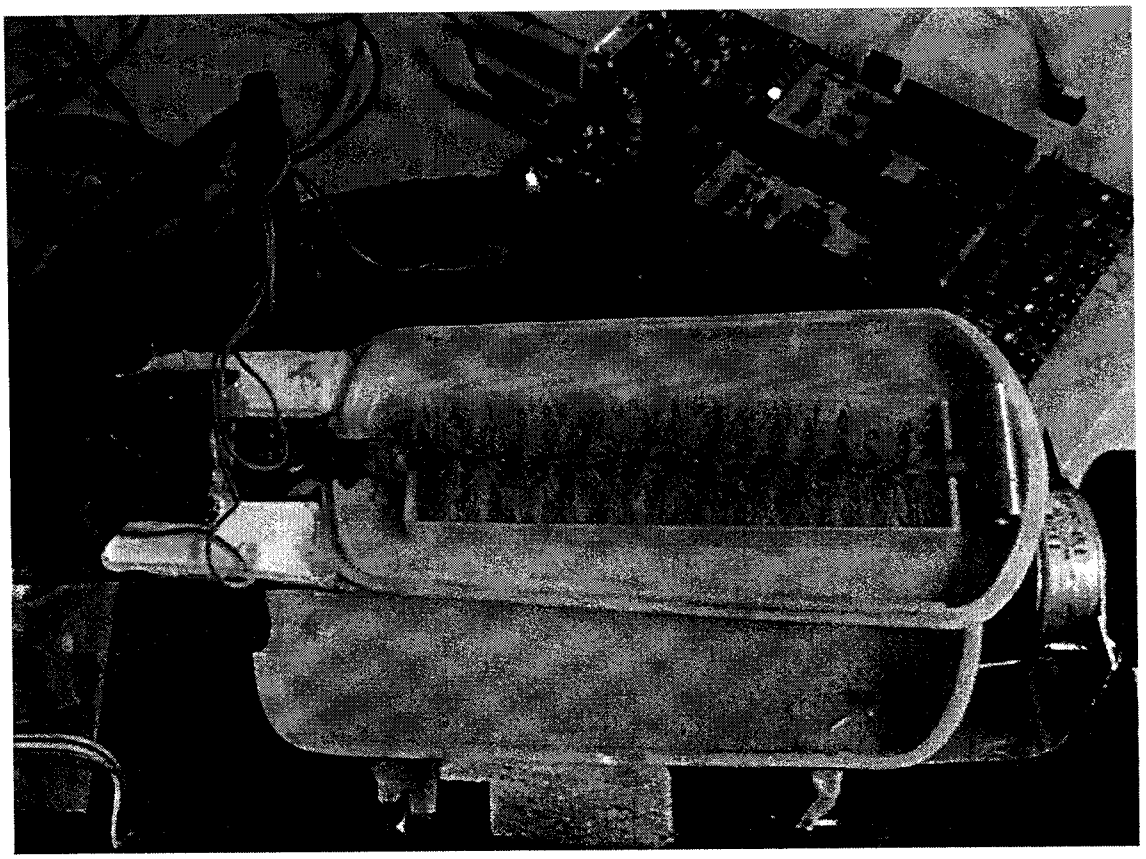


Fig.1.2 BRUSH WITH COLLECTOR

The surface cleaning tool used is a brush with collector which is shown in fig.1.2. The brush is rotated using a motor which sweeps of the dust and the collector holds the dust intact. It is more convenient to dispose the dust. This sweeping mechanism is very economical compared to vacuum cleaners which require large amount of power and they are expensive.

Chapter 2

BLOCK DIAGRAM DESCRIPTION

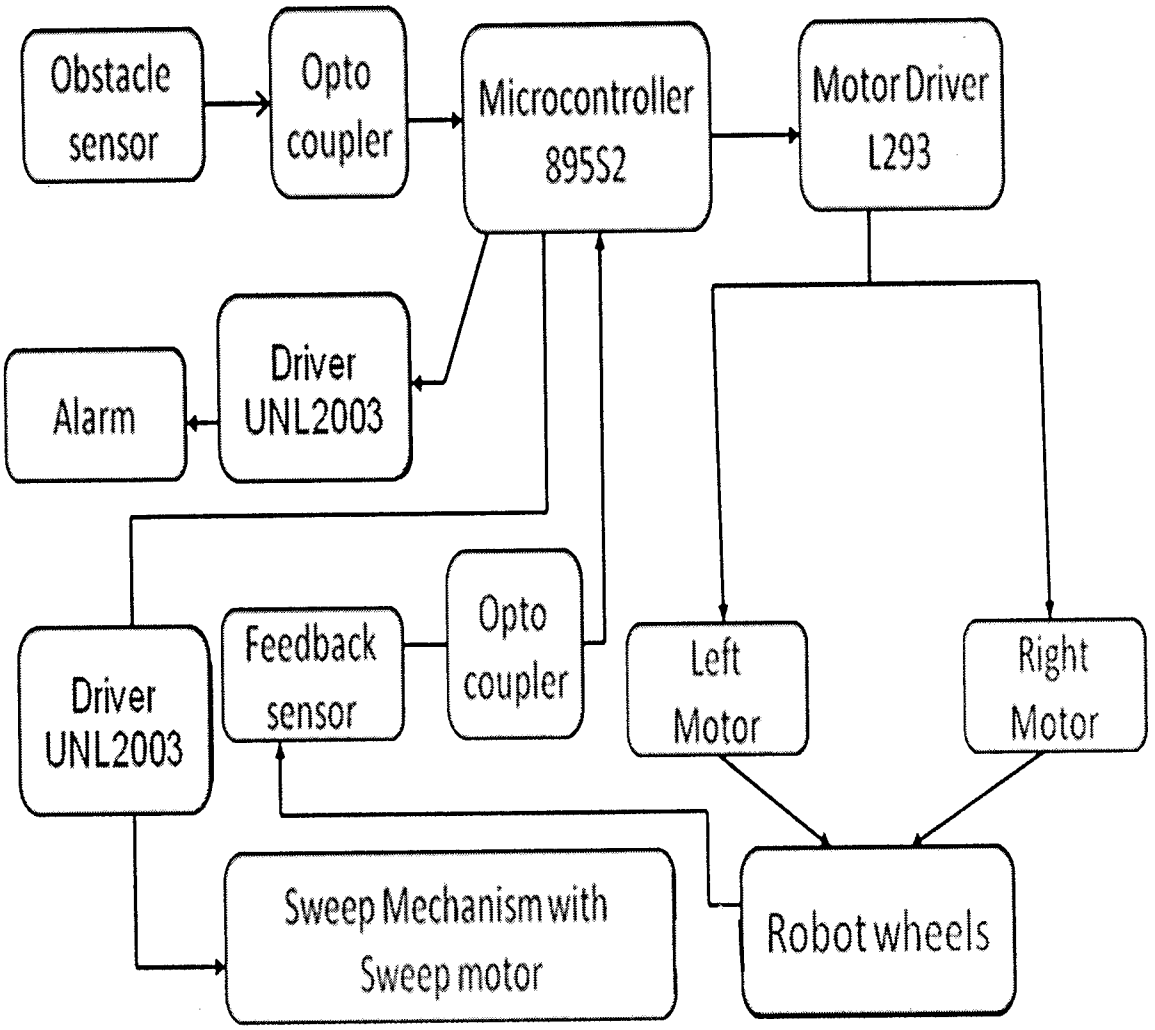


Fig.2.1 BLOCK DIAGRAM OF CLEANING SYSTEM

The various blocks in the block diagram are microcontroller, obstacle sensor, feedback sensor, opto coupler, motor divers, motors, alarm driver, alarm, sweeping tool (rotating brush with a collector).

The microcontroller plays the major role. Dimension of room is programmed in the microcontroller. When the robot is switched on microcontroller gives the control signal to the motor drivers. Motor driver 1 controls the left motor and motor driver 2 runs the right motor. Robot starts to move as per program in microcontroller. Mean time it activates the sweeper mechanism with sweep motor which cleans the floor. Feed back sensor senses the distance traveled by the robot. This signal is given to the microcontroller and it compares the signal with the set dimension to control the robot.

Microcontroller is pre programmed to move the robot suitable for the known obstacles. Obstacle sensor senses the unknown obstacle and this signal is given to the microcontroller. When this signal is received microcontroller stops the robot and activates the alarm driver. Alarm driver turns on the alarm to indicate to the user.

2.1Feedback Mechanism

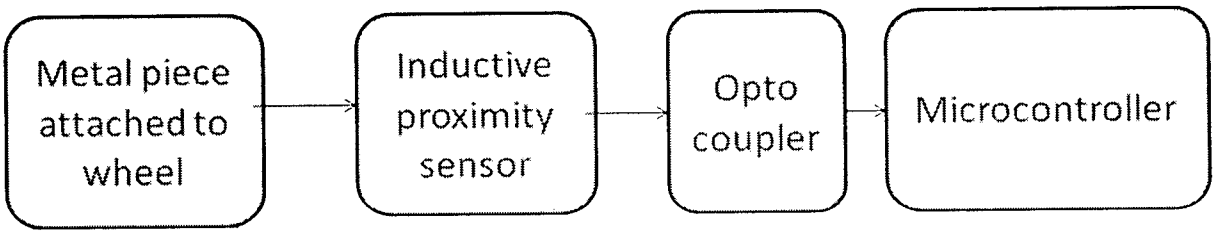


Fig.2.2 FEEDBACK MECHANISM

This mechanism shown in fig.2.2 is used to track the distance traveled by the robot. It is based on the principle that the distance travelled by the robot is equal to the product of circumference of the wheel and the number of wheel rotations. A small metal piece is attached to the rim of the wheel which will be detected by an

induction proximity sensor. A logic 0 signal will be given to the controller via an opto coupler whenever the metal piece is detected i.e. to indicate a complete wheel rotation.

2.2 Unknown Obstacle Detection Mechanism

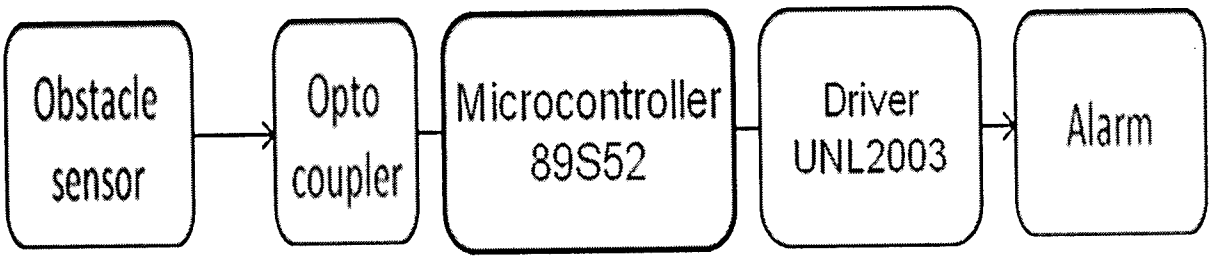


Fig.2.3 DETECTION MECHANISM

The mechanism shown in fig.2.3 is used to detect an unknown obstacle and to produce an alarm so that the user can remove the unknown obstacle for the robot to continue its defined path. The obstacle sensor is an IR proximity sensor. It gives a logic 0 signal to the controller via an opto coupler whenever an obstacle is detected in a nearby range of 15mm in front. At the same time the alarm is activated through an alarm driver to indicate the user that the obstacle has to be removed. This cycle keeps on repeating till the obstacle is removed

2.3 Sweep Mechanism

The mechanism in fig.2.4 is a simple one which is used to rotate the DC motor connected to the sweeping brush. Whenever the robot is turned on the sweep motor is activated by the controller via a motor driver. The motor is made to stop whenever an unknown obstacle is detected.

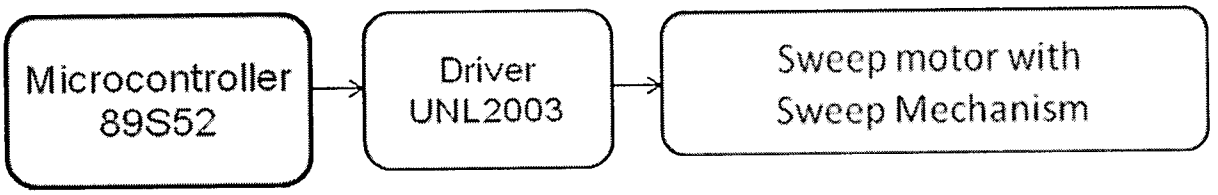


Fig.2.4 SWEEP MECHANISM

2.4 Robo Mechanism

This mechanism is used for controlling the robot movement in order to follow the defined path. Comparing the number of rotations obtained from the feedback mechanism and the set values the microcontroller provides the required control signal to the motor through motor driver chip. The motor driver is a 20 pin IC which is capable of controlling two motors at a time in both clockwise and anticlockwise direction. By controlling the motor directions the robot is made to move in forward, right and left directions

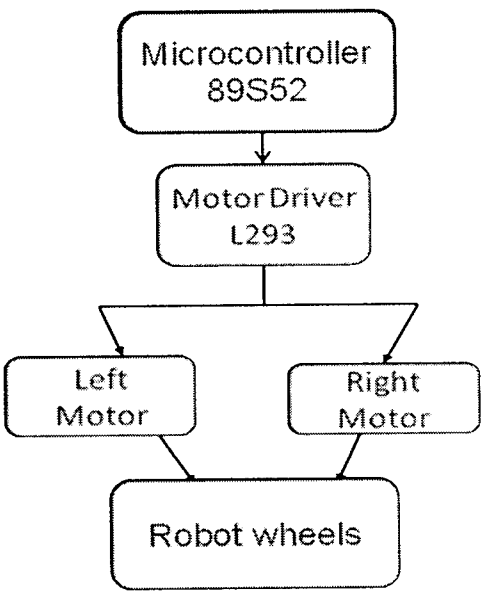


Fig.2.5 ROBO MECHANISM

Chapter 3

HARDWARE DESCRPTION

3.1 Microcontroller

3.1.1 Features

- Compatible with MCS-51 Products
- 8K bytes of In-System Programmable(ISP) Flash Memory
- Endurance: 10000 Write/Erase Cycles
- 4.0V to 5.0V Operating Range
- Fully Static Operation: 0 Hz to 33 Mhz
- Three level Program Memory Lock
- 256 * 8 – bit internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low power Idle and Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming(Byte and Page Mode)
- Green Packaging Option

3.1.2 Architecture

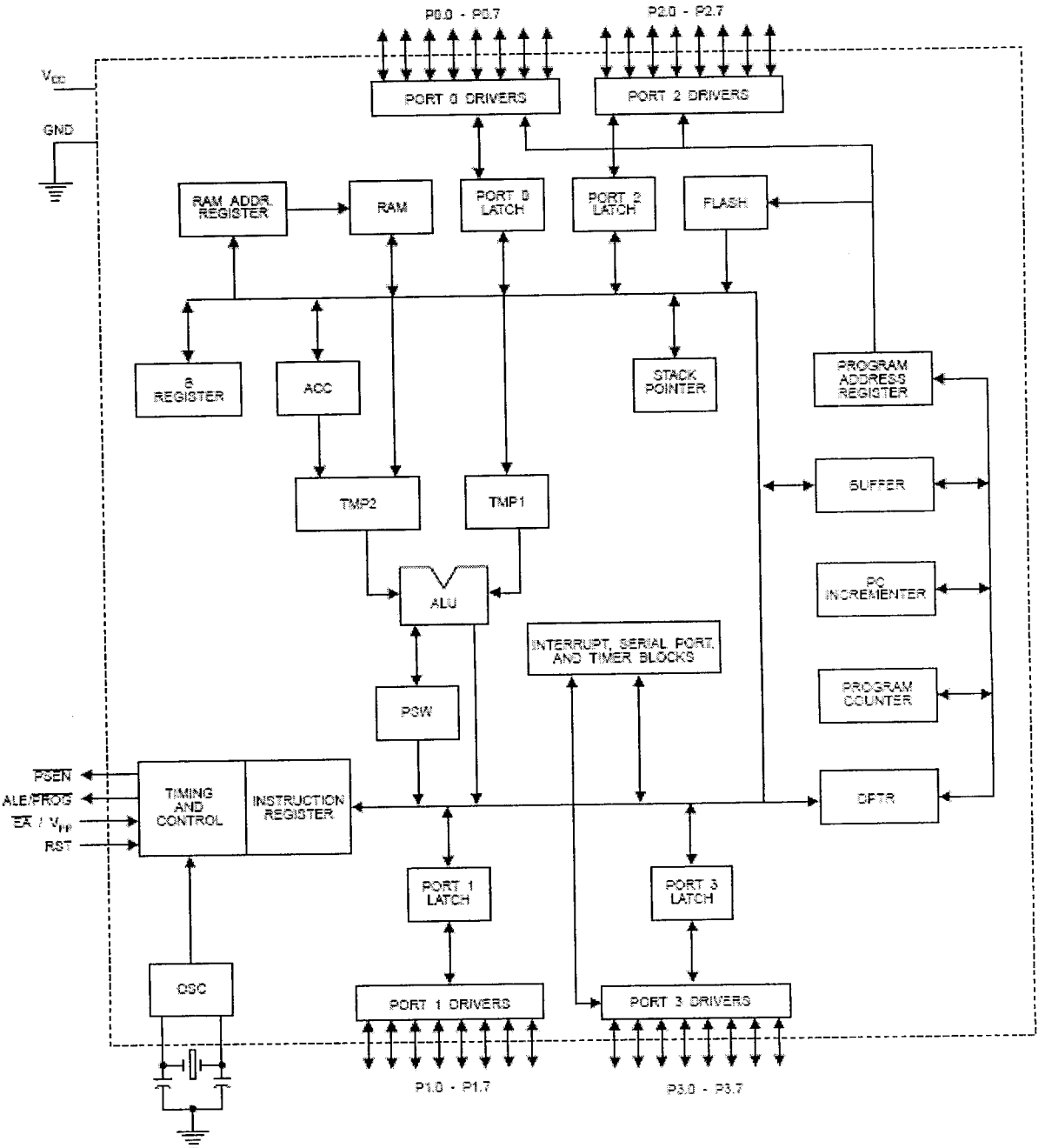


Fig.3.1 ARCHITECTURE OF 89S52

The AT89S52 is a low-power, high performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80c51 instruction set and pin out.

The on-chip flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S52 provides the following standard features: 8K bytes of Flash,256 bytes of RAM,32 I/O lines, Watch dog timer, two data pointers , three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

3.1.3 Pin Description

The pin diagram is shown in fig.3.2

1. VCC

Supply voltage

2. GND

Ground

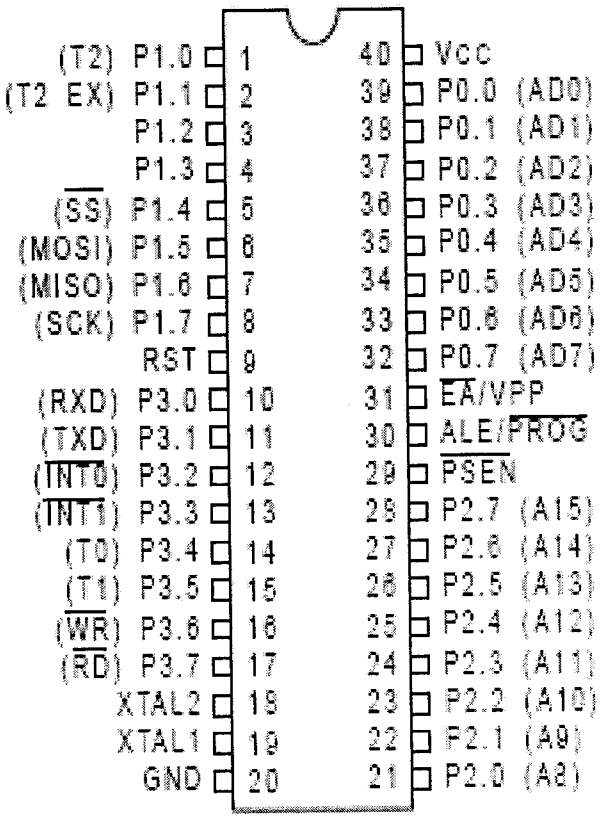


Fig.3.2 PIN DIAGRAM

3. Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL input. When 1's are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

4. Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IR) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/ T2EX) respectively. Port 1 also receives the low-order address bytes during Flash programming and verification.

5. Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (Iil) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR).In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit

addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

6. Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (Iil) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification. Port 3 also serves the functions of various special features of the AT89S52 as shown in the table 3.1

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

TABLE.3.1 PORT 3 ALTERNATE FUNCTIONS

7. RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR(address 8EH) can be used to disable this feature. In the default state of bit DISTRO, the RESET HIGH out feature is enabled.

8. ALE/ PROG

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

9. PSEN

Program Store Enable (PSEN) is the read strobe to external program memory. When the AT89S52 is executing code from external program memory,

PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

10. EA/VPP

External Access Enable, EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.This pin also receives the 12-volt programming enable voltage (Vpp) during Flash programming.

11. XTAL 1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

12. XTAL 2

Output from the inverting oscillator amplifier.

3.1.4 Memory Organization

MCS-51 devices have a separate address space for Program and Data memory. Up to 64K bytes each of external Program and Data memory can be addressed.

Program Memory

If the EA pin is connected to GND, all program fetches are directed to external memory. On the AT89S52, if EA is connected to Vcc, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SRF space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space. Instructions which use indirect addressing access the upper 128 bytes of RAM.

Special Function Registers

A map of the on-chip memory area is called the Special Function Register (SFR) is shown in fig.3.3.

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 0XXX0000 87H

Fig 3.3 SFR MAP

3.1.5 Timers

Timer Registers Register pairs (TH0, TL0), (TH1, TL1), and (TH2, TL2) are the 16-bit counting registers for Timer/Counters 0, 1, and 2, respectively

Timer 0

Timer 0 functions as either a timer or event counter in four modes of operation. Timer 0 is controlled by the four lower bits of the TMOD register (see

Table 3.2) and bits 0, 1, 4 and 5 of the TCON register (see Table 3.3). TMOD register selects the method of Timer gating (GATE0), timer or counter operation (T/C0#) and mode of operation (M10 and M00). The TCON register provides timer 0 control functions: overflow flag (TF0), run control bit (TR0), interrupt flag (IE0) and interrupt type control bit (IT0). For normal timer operation (GATE0= 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE0 and TR0 allows external pin INT0# to control timer operation. Timer0 overflow (count rolls over from all 1s to all 0s) sets TF0 flag, generating an interrupt request.

Mode 0 (13-bitTimer)

Mode 0 configures timer 0 as a 13-bit timer which is set up as an 8-bit timer (TH0 register) with a modulo 32 prescaler implemented with the lower five bits of the TL0 register .The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

Mode 1 (16-bitTimer)

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits. Mode 1 configures timer 0 as a 16-bit timer with the TH0 and TL0 registers connected in Cascade. The selected input increments the TL0 register

Mode 2 (8-bit Timer with Auto-Reload)

Mode 2 configures timer 0 as an 8-bit timer (TL0 register) that automatically reloads from the TH0. TL0 overflow sets TF0 flag in the TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged. The next reload value may be changed at any time by writing it to the TH0 register.

Timer Control Register

Tcon

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit Number	Bit Mnemonic	Description
7	TF1	**Timer 1 Overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer/counter overflow, when the timer 1 register overflows.
6	TR1	**Timer 1 Run Control Bit** Clear to turn off timer/counter 1. Set to turn on timer/counter 1.
5	TF0	**Timer 0 Overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer/counter overflow, when the timer 0 register overflows.
4	TR0	**Timer 0 Run Control Bit** Clear to turn off timer/counter 0. Set to turn on timer/counter 0.
3	IE1	**Interrupt 1 Edge Flag** Cleared by hardware when interrupt is processed if edge-triggered (see IT1). Set by hardware when external interrupt is detected on INT1# pin.
2	IT1	**Interrupt 1 Type Control Bit** Clear to select low level active (level triggered) for external interrupt 1 (INT1#). Set to select falling edge active (edge triggered) for external interrupt 1.
1	IE0	**Interrupt 0 Edge Flag** Cleared by hardware when interrupt is processed if edge-triggered (see IT0). Set by hardware when external interrupt is detected on INT0# pin.
0	IT0	**Interrupt 0 Type Control Bit** Clear to select low level active (level triggered) for external interrupt 0 (INT0#). Set to select falling edge active (edge triggered) for external interrupt 0.

Reset Value = 0000 0000b

TABLE 3.2 TCON REGISTER

Timer Mode Register

Tmod

7	6	5	4	3	2	1	0
GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00

Bit Number	Bit Mnemonic	Description
7	GATE1	**Timer 1 Gating Control Bit** Clear to enable timer 1 whenever the TR1 bit is set. Set to enable timer 1 only while the INT1# pin is high and TR1 bit is set.
6	C/T1#	**Timer 1 Counter/Timer Select Bit** Clear for timer operation: timer 1 counts the divided-down system clock. Set for Counter operation: timer 1 counts negative transitions on external pin T1.
5	M11	**Timer 1 Mode Select Bits** M11 M01 Operating mode 0 0 Mode 0: 8-bit timer/counter (TH1) with 5-bit prescaler (TL1). 0 1 Mode 1: 16-bit timer/counter. 1 0 Mode 2: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 1 1 Mode 3: timer 1 halted. Retains count.
4	M01	
3	GATE0	**Timer 0 Gating Control Bit** Clear to enable timer 0 whenever the TR0 bit is set. Set to enable timer/counter 0 only while the INT0# pin is high and the TR0 bit is set.
2	C/T0#	**Timer 0 Counter/Timer Select Bit** Clear for timer operation: timer 0 counts the divided-down system clock. Set for counter operation: timer 0 counts negative transitions on external pin T0.
1	M10	**Timer 0 Mode Select Bit** M10 M00 Operating mode 0 0 Mode 0: 8-bit timer/counter (TH0) with 5-bit prescaler (TL0). 0 1 Mode 1: 16-bit timer/counter. 1 0 Mode 2: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 1 1 Mode 3: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer using timer 1's TR0 and TF0 bits.
0	M00	

Reset Value = 0000 0000b

TABLE 3.2 TMOD REGISTER

3.1.6 Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts (INTO and INT1), three timer interrupts (Timers 0, 1 and 2) and the serial port interrupt.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global bit EA which disables all interrupts at once.

Note that the bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.
The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows. Refer datasheet for interrupt register details.

3.2 L293D Motor Driver

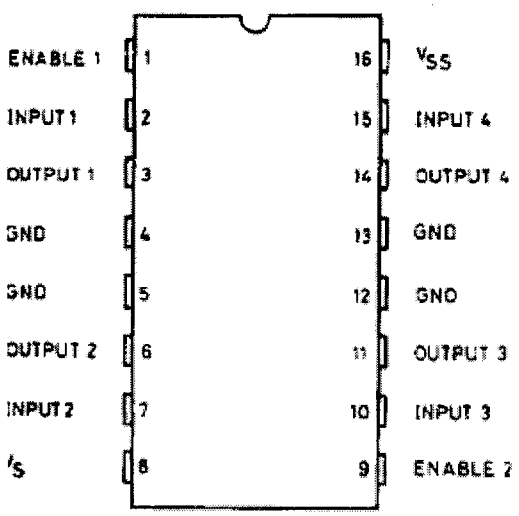


Fig.3.4 PIN DIAGRAM OF L293D

3.2.1 Features

- 600ma output current capability per channel
- 1.2a peak output current (non repetitive) per channel
- Enable facility
- Over temperature protection
- Logical "0" input voltage up to 1.5 v (high noise immunity)
- Internal clamp diode

3.2.2 Internal circuitry and description

The Device is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoids , DC and stepping motors) and switching power transistors. Internal circuitry is shown in fig.3.5.

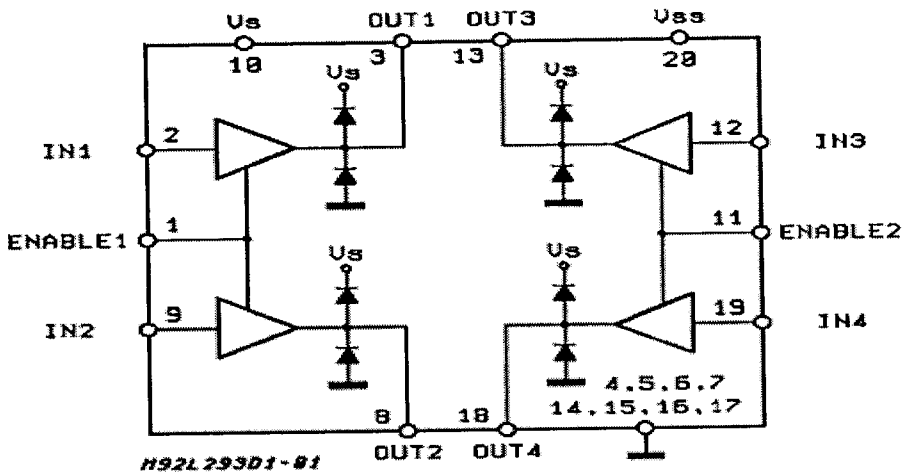


Fig.3.5 INTERNAL CIRCUITRY OF L293D

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included. This device is suitable for use in switching applications at frequencies up to 5 kHz. The L293D is assembled in a 16 lead plastic package (refer fig.3.4) which has 4 center pins connected together and used for heat sinking.

3.3 Dc Geared Motors

A gear motor is a type of electrical motor. Like all electrical motors, it uses the magnetism induced by an electrical current to rotate a rotor that is connected to a shaft. The energy transferred from the rotor to the shaft is then used to power a connected device. In a gear motor, the energy output is used to turn a series of gears in an integrated gear train. There are a number of different types of gear motors, but the most common are AC (alternating current) and DC (direct current).

3.3.1 Working

In a gear motor, the magnetic current (which can be produced by either permanent magnets or electromagnets) turns gears that are either in a gear reduction unit or in an integrated gear box. A second shaft is connected to these gears. The result is that the gears greatly increase the amount of torque the motor is capable of producing while simultaneously slowing down the motor's output speed. The motor will not need to draw as much current to function and will move more slowly, but will provide greater torque..

1271 series geared dc instrument motor

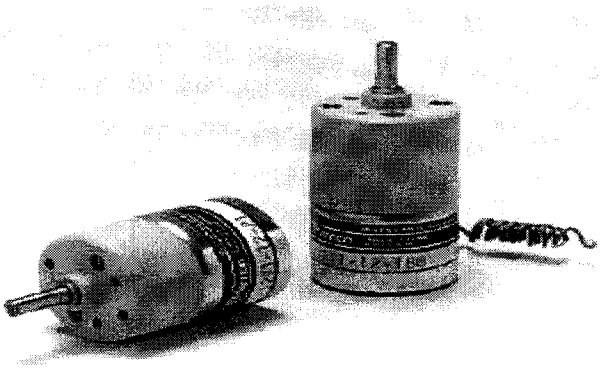


Fig.3.6 DC MOTOR

The 1271 geared instrument dc motor shown in fig.3.6 is ideally suited to a wide range of applications requiring a combination of low speed operation and small unit size. The integral iron core dc motor provides smooth operation and a bidirectional

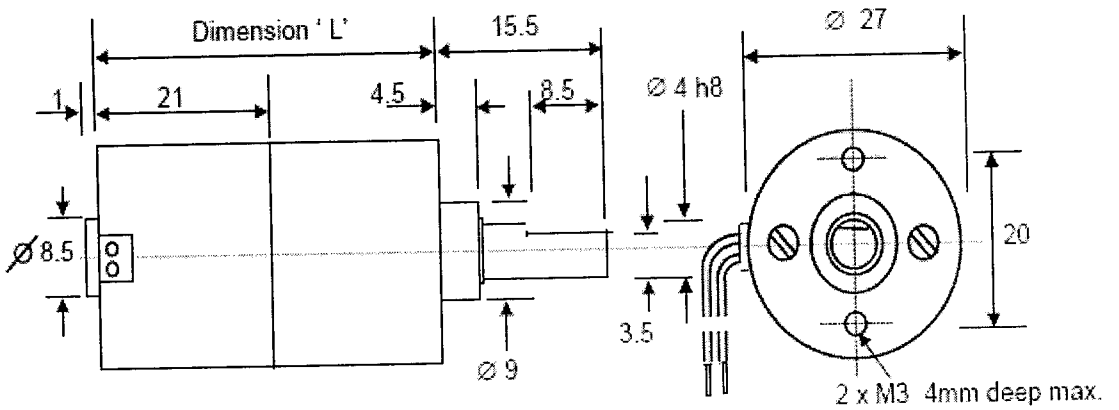
Variable speed capability while the gear head utilizes a multistage metal spur gear train rated for a working torque up to 0.2 Nm. The unit, which is suitable for mounting in any attitude, provides reliable operation over a wide ambient temperature range and is equipped with an integral VDR (voltage dependant resistor) electrical suppression system to minimize electrical interference. The 1271 unit offers a range of gear ratio options for operating speeds from 5- 200 rpm and is ideally suited to applications where small size and low unit price are important design criteria.

3.3.2 Applications

Gear motors are commonly used in conveyor-belt drives, home appliances, in handicap and platform lifts, medical and laboratory equipment, machine tools, packaging machinery and printing presses

3.3.3 Dimensions

Dimensions: mm



Length 'L' (mm)	Gear ratio	Nominal Voltage (V dc)	No-Load speed (rpm)	Rated Speed (rpm)	Rated Torque (N cm)	Rated Current (m A)	Mass (grams)
41	43:1	12	60	40	3.8	50	57

TABLE 3.4 MOTOR RATINGS

3.4 ULN2003-Driver IC

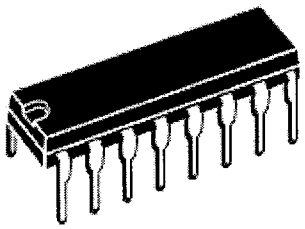


Fig.3.7 ULN2003 DIP PACKAGE

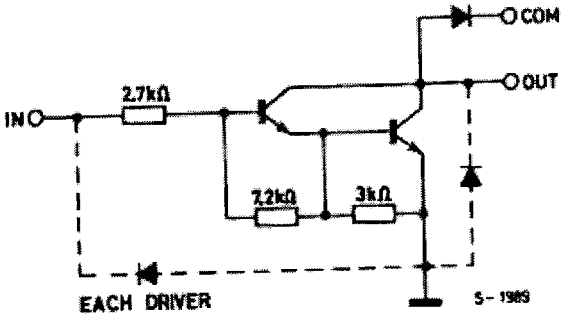


Fig.3.8 CHANNEL DIAGRAM

3.4.1 Features

- Seven Darlington per package
- Output current 500ma per driver
- Output voltage 50v
- Integrated suppression diodes for Inductive loads
- Outputs can be paralleled for higher current
- TTL/CMOS/PMOS/DTL compatible inputs
- Inputs pinned opposite outputs to simplify layout

3.4.2 Description

The ULN2003 is a 16 pin plastic DIP package(fig 3.7). It has high voltage, high current Darlington arrays each containing seven open collector Darlington pairs with common emitters.

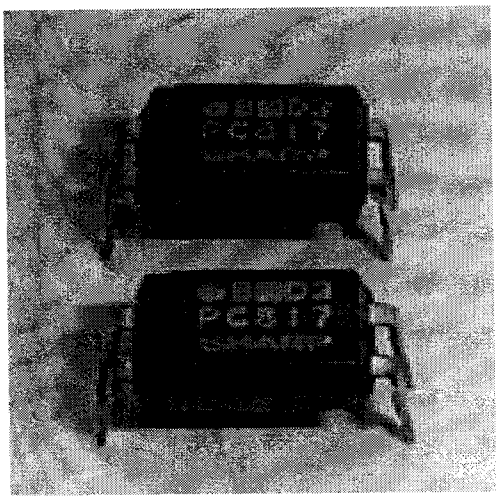
Each channel (fig 3.8) rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

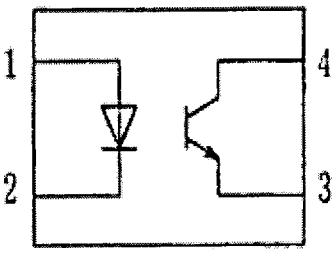
These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, buzzer, LED displays filament lamps, thermal print heads and high power buffers. They are supplied in 16 pin plastic DIP packages with a copper lead frame to reduce thermal resistance

3.5 Optocouplers –PC 817

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct ohmic electrical connection. Often this is because the source and destination are at very different voltage levels, like a microprocessor which is operating at 5V DC but being used to control a triac which is switching 240V AC or receive an input from sensors operating at 12V. In such situations the link between the two must be an isolated one, to protect the microprocessor from overvoltage damage. Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature circuit components. Because they are electro-mechanical, relays are also not as reliable and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an opto coupler.

These use a beam of light to transmit the signals or data across an electrical barrier, and achieve excellent isolation.





Pin Nos. and internal connection diagram

FIG.3.9. PIN DIAGRAM AND INTERNAL CIRCUIT

Opto couplers typically come in a small 6-pin or 4-pin IC package (in fig.3.9) but are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (light-emitting diode) and an optical receiver such as a phototransistor or light-triggered diac. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. Usually the electrical connections to the LED section are brought out to the pins on one side of the package and those for the phototransistor or diac to the other side, to physically separate them as much as possible. This usually allows opto couplers to withstand voltages of anywhere between 500V and 7500V between input and output. Opto couplers are essentially digital or switching devices, so they are best for transferring either on-off control signals or digital data. Analog signals can be transferred by means of frequency or pulse-width modulation.

3.6 Inductive Proximity Sensors

Proximity sensors are sensors able to detect the presence of nearby objects without any physical contact. A proximity sensor often emits an electromagnetic or electrostatic field, or a beam of electromagnetic radiation (infrared, for instance), and looks for changes in the field or return signal. The object being sensed is often referred to as the proximity sensor's target. Different proximity sensor targets demand different sensors. For example, a capacitive or photoelectric sensor might be suitable for a plastic target; an inductive proximity sensor requires a metal target.

The maximum distance that this sensor can detect is defined "nominal range". Some sensors have adjustments of the nominal range or means to report a graduated detection distance. Proximity sensors can have a high reliability and long functional life because of the absence of mechanical parts and lack of physical contact between sensor and the sensed object.

Conditioning the output of a proximity sensor is frequently difficult. Proximity sensor designers must confront linearity, hysteresis, excitation voltage instability, and voltage offset.

3.6.1 Types of Sensors

- Capacitive
- magnetic
- inductive
- photocell (reflective)
- laser rangefinders

- sonar (typically active or passive)
- radar
- doppler effect
- passive thermal infrared
- passive optical (such as CCDs)
- reflection of ionising radiation

3.6.2 Internal circuitry and working

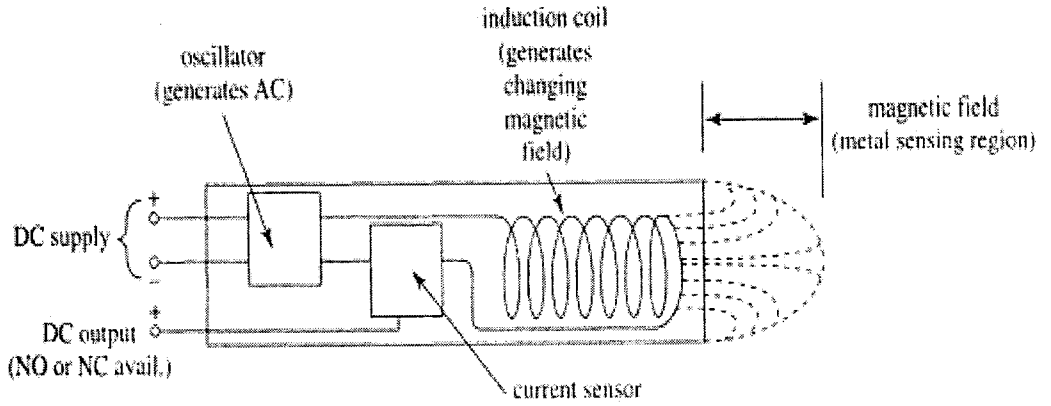


Fig.3.10 INTERNAL CIRCUIT OF IPS

Inductive proximity sensors(fig 3.11) operate under the electrical principle of inductance. Inductance is the phenomenon where a fluctuating current, which by definition has a magnetic component, induces an electromotive force (EMF) in a target object. To amplify a device's inductance effect, a sensor manufacturer twists wire into a tight coil and runs a current through it.

An inductive proximity sensor has four components; The coil, oscillator, detection circuit and output circuit as shown in fig.3.10. The oscillator generates a fluctuating magnetic field the shape of a doughnut around the winding of the coil

that locates in the device's sensing face. When a metal object moves into the inductive proximity sensor's field of detection, Eddy circuits build up in the metallic object, magnetically push back, and finally reduce the Inductive sensor's own oscillation field. The sensor's detection circuit monitors the oscillator's strength and triggers an output from the output circuitry when the oscillator becomes reduced to a sufficient level.

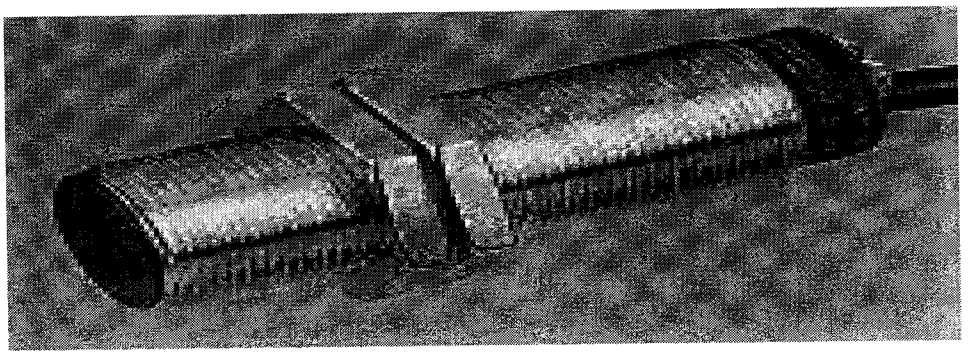


Fig.3.11 EXTERNAL VIEW OF IPS

3.7 IR Sensor

The Infrared sensor (fig 3.12) allows us to detect an object's distance from the robot. Attaching these sensors on the wing tips will help the robot navigate through the halls of any building. It consists of an IR emitter to produce the IR rays and an IR detector to detect the received IR rays.

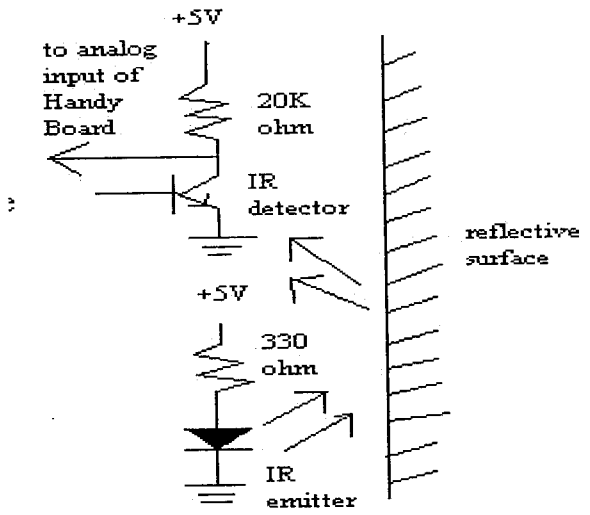


Fig.3.12 IR SENSOR

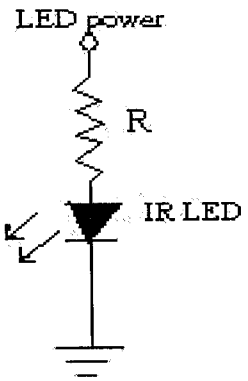
3.7.1 IR Emitter

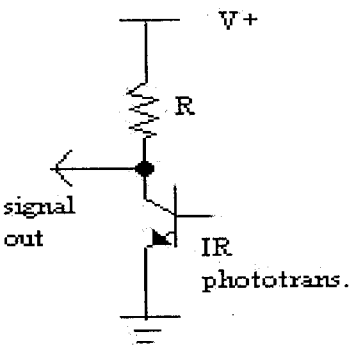
An infrared emitter (fig 3.13) is an LED made from gallium arsenide, which emits near-infrared energy at about 880nm.

3.7.2 IR Phototransistor

The infrared phototransistor acts as a transistor with the base voltage determined by the amount of light hitting the transistor. Hence it acts as a variable current source. Greater amount of IR light cause greater currents to flow through the collector-emitter leads. As shown in the fig 3.14, the phototransistor is wired in a similar configuration to the voltage divider. The variable current traveling through the resistor causes a voltage drop in the pull-up resistor.

This voltage is measured as the output of the device.





An IR emitter

An IR phototransistor

Fig.3.13 IR EMITTER

Fig.3.14PHOTOTRANSISTOR

3.8 Buzzer

A buzzer or beeper is an audio signaling device (fig 3.15), which may be mechanical, electromechanical, or electronic. Typical uses of buzzers and beepers include alarms, timers and confirmation of user input such as a mouse click or keystroke. It most commonly consists of a number of switches or sensors connected to a control unit that determines if and which button was pushed or a preset time has lapsed, and usually illuminates a light on the appropriate button or control panel, and sounds a warning in the form of a continuous or intermittent buzzing or beeping sound. The word "buzzer" comes from the rasping noise that buzzers made when they were electromechanical devices, operated from stepped-down AC line voltage at 50 or 60 cycles. Other sounds commonly used to indicate that a button has been pressed are a ring or a beep.

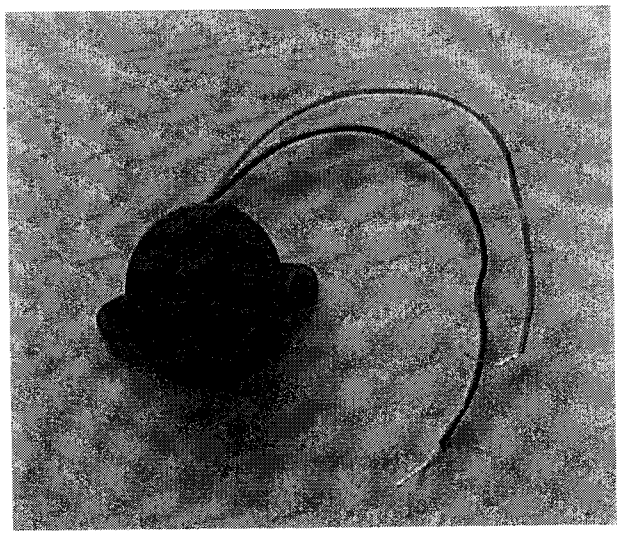


Fig.3.15 EXTERNAL VIEW OF BUZZER

3.8.1 Types of Buzzers

- Mechanical
- Electromechanical
- Electronic

3.8.2 Electronic Piezo electric disc beeper

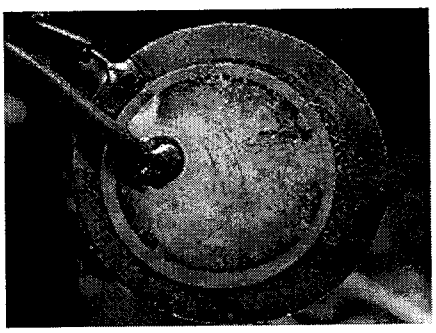


FIG.3.16 PIEZO ELECTRIC BUZZER

A piezoelectric element as shown in fig 3.16 may be driven by an oscillating electronic circuit or other audio signal source. Sounds commonly used to indicate that a button has been pressed are a click, a ring or a beep which were high-pitched tones. Usually these were hooked up to "driver" circuits which varied the pitch of the sound or pulsed the sound on and off. The symbol for a electronic buzzer is shown in fig 3.17.

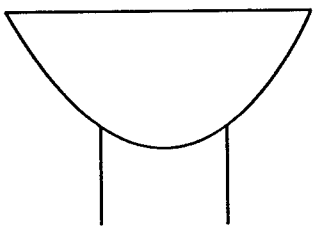


Fig.3.17 ELECTRONIC SYMBOL FOR BUZZER

3.9 Battery

An electrical battery is a combination of one or more electrochemical cells, used to convert stored chemical energy into electrical energy. Batteries may be used once and discarded, or recharged for years as in standby power applications

3.9.1 Lead Acid Battery and Description

Lead-acid batteries are the oldest type of rechargeable battery. Despite having a very low energy-to-weight ratio and a low energy-to-volume ratio, their ability to supply high surge currents means that the cells maintain a relatively large power-to-weight ratio. These features, along with their low cost, make them attractive for use in motor vehicles to provide the high current required by automobile starter motors

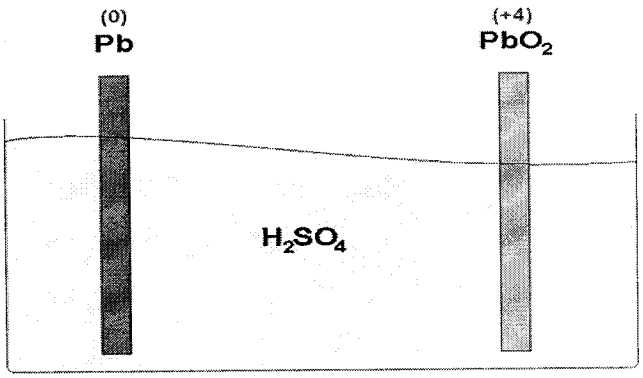


Fig.3.18 LEAD ACID ACCUMULATOR

The type of battery in general use in motor vehicles is lead-acid accumulator shown in fig 3.18. Cells can be connected in series to form a battery. The battery contains three 2 V cells to make a battery that delivers 6 V. In a lead-acid accumulator, each cell has one lead electrode, one lead (IV) oxide (PbO2) electrode and sulphuric acid as the electrolyte. When the battery supplies a current, lead and lead (IV) oxide are both converted into lead (II) ions. When the reactants have been used up, the battery can no longer supply a current; it is "flat". It can, however be recharged.

3.9.2 Charging a lead acid battery

It can then be recharged by connecting it to a battery charger, a transformer connected to the mains. This reverses the sign of each electrode and reverses the chemical reactions that have occurred at the electrodes. Lead and lead (IV) oxide are reformed, and the battery is again able to supply an e.m.f. The charge voltage is calculated according to the number of cells and desired voltage limit. In this project two lead acid batteries of 6v are connected in series to provide the necessary 12V required for operation.

Chapter 4

CIRCUIT DESCRIPTION

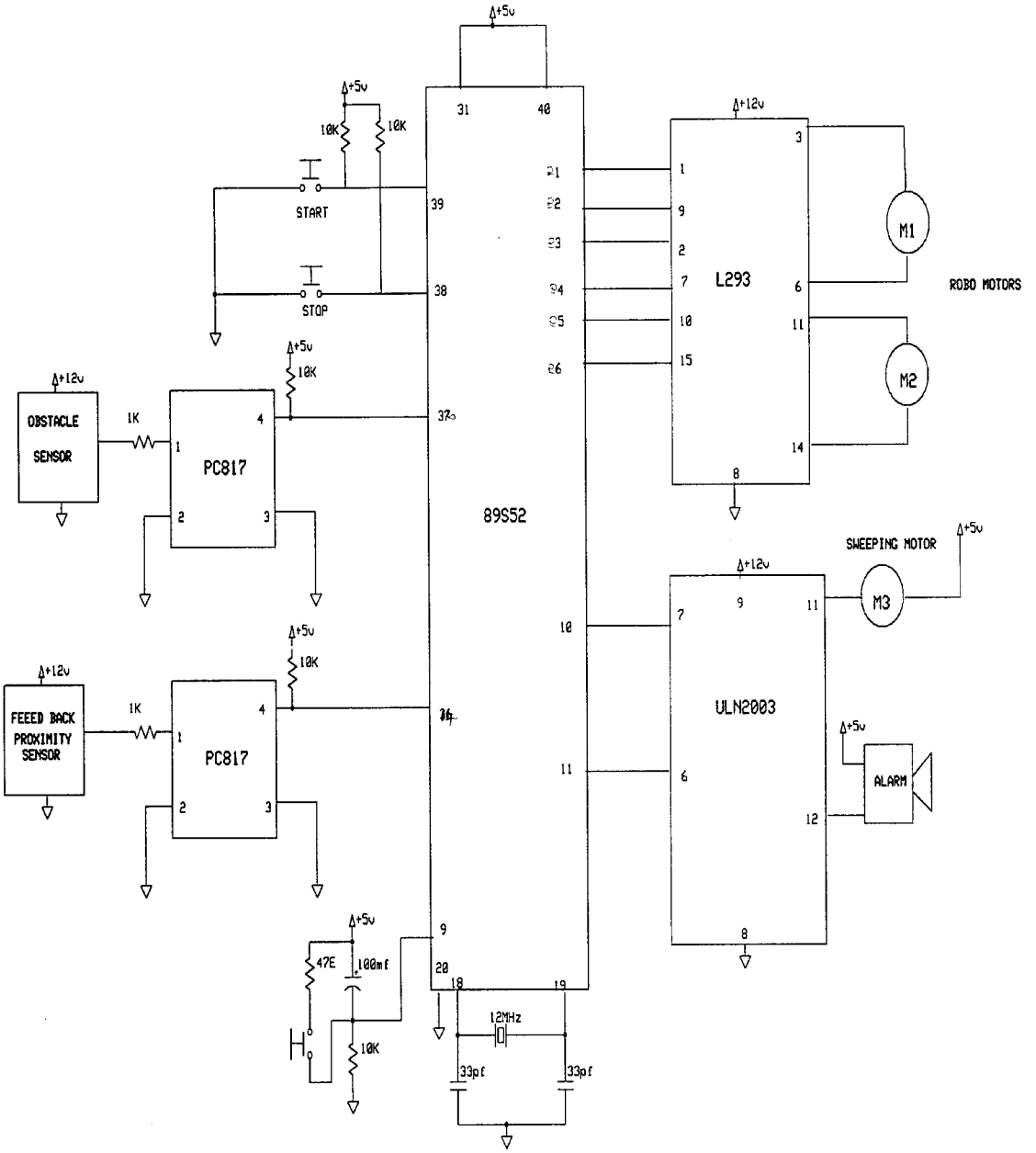


Fig 4.1 CIRCUIT DIAGRAM OF THE SYSTEM

4.1 Interfacing of Motors

4.1.1 Wheel Motors

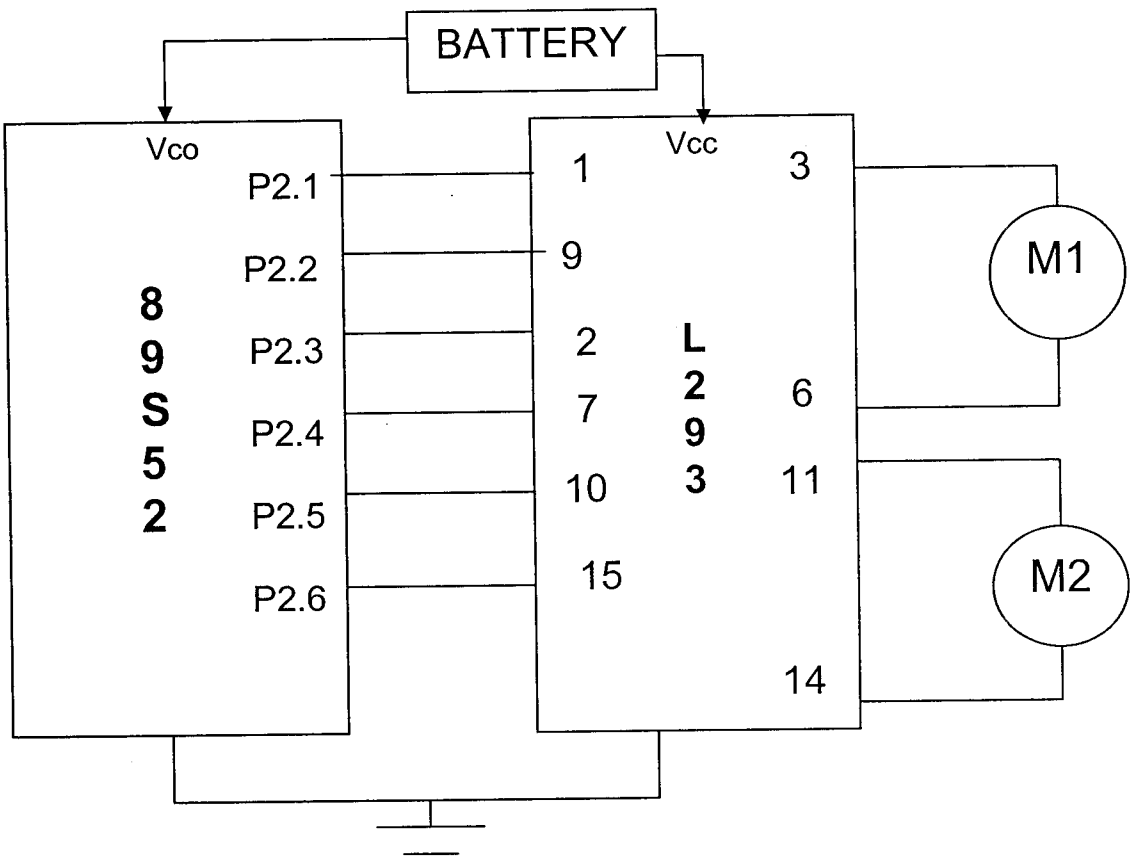


Fig 4.2 WHEEL MOTOR INTERFACING CIRCUIT

From fig4.2 it can be seen that P2.1 and P2.2 of the microcontroller is connected to the input of the motor driver L293 in order to control the motor 1. P2.3 of the microcontroller is connected to the enable1 of the driver. P2.4 and P2.5 of the microcontroller is connected to the input of the motor driver L293 in order to control the motor 2. P2.6 of the microcontroller is connected to the enable2 pin of the driver. The battery and ground terminals are connected to the microcontroller and driver as per the circuit diagram in fig 4.1.

The table 4.1 shows the input to driver through which the motors are controlled:

MICROCONTROLLER PINS						MOTORS		ROBO DIRECTION
P2.1	P2.2	P2.3	P2.4	P2.5	P2.6	RIGHT	LEFT	
1	0	1	0	1	1	CLOCKWISE	CLOCKWISE	FORWARD
1	0	0	0	1	0	CLOCKWISE	STOP	RIGHT
0	0	1	0	0	1	STOP	CLOCKWISE	LEFT
0	0	0	0	0	0	STOP	STOP	STOP

TABLE 4.1 CONTROL OUTPUTS FOR ROBO MOVEMENT

1. For the robot should move in forward direction, the right motor should move in clockwise direction and the left motor should also move in clockwise direction.
2. For the robot should move in right direction, the right motor should move in clockwise direction and the left motor should be stopped.
3. For the robot should move in left direction, the right motor should be stopped and the left motor should move in clockwise direction.
4. For the robot to stop, both the right and left motor should be stopped.

4.1.2 Sweep Motor

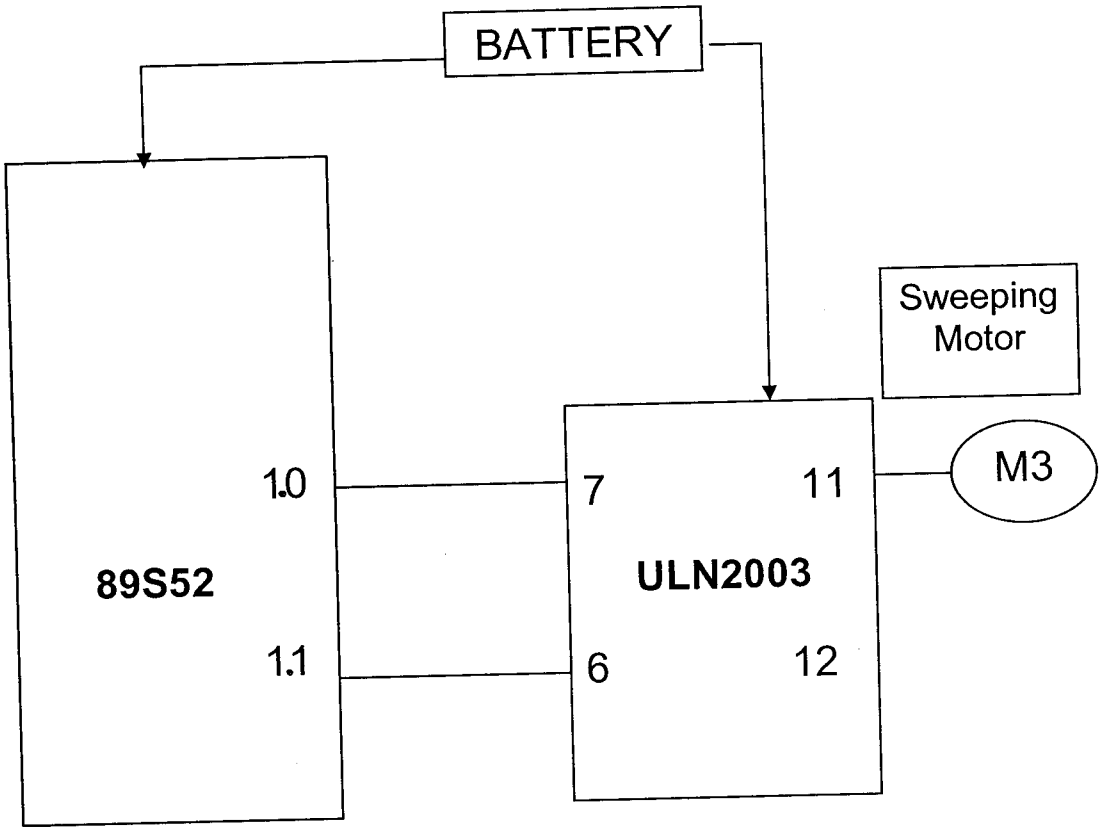


Fig 4.3 SWEEP MOTOR INTERFACING CIRCUIT

From fig4.3 it can be seen that the pin 10 of the microcontroller is connected to pin 7 of the ULN2003 driver and the pin 11 of the microcontroller is connected to pin 6 of the ULN2003 driver. The pin 11 of the driver is used to control the sweep motor. The driver acts as an isolation device and produces the required current to drive the motor

4.2 Interfacing of Sensors

4.2.1 Inductive Proximity Sensor

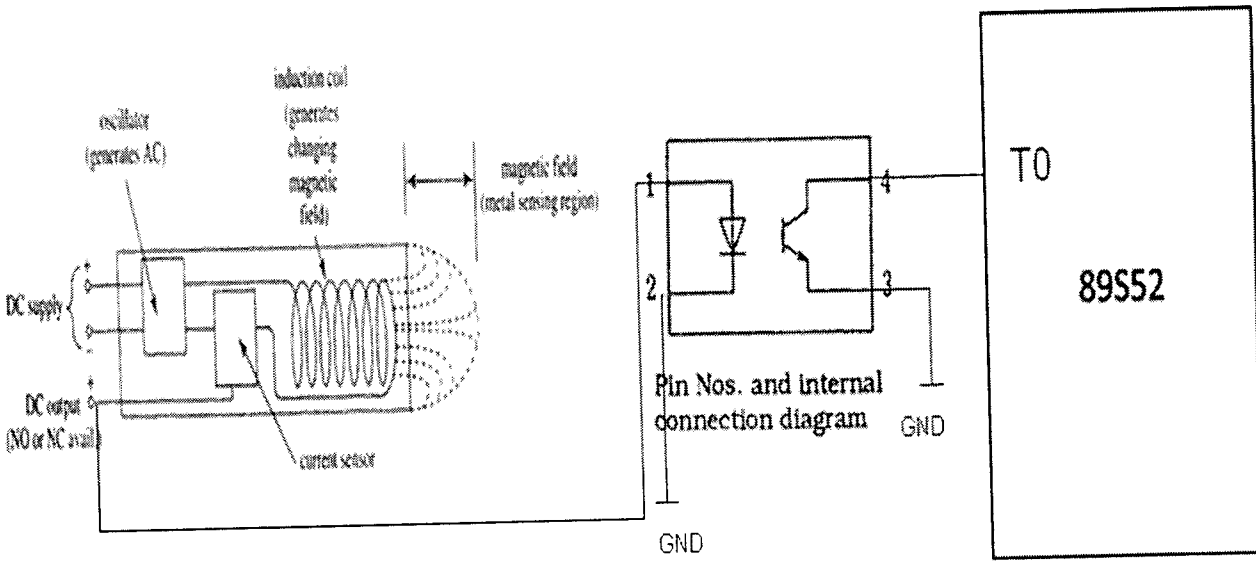


Fig 4.4 IPS INTERFACING CIRCUIT

The inductive proximity sensor is given the required dc supply from the battery. From fig 4.4 it can be seen that the output from the sensor is connected to the input pin of PC817 opto coupler's pin 1. The output from the opto coupler pin 4 is given to the port 3 timer0 pin 3.4.

The opto coupler is used for isolation purpose and for producing digital switching signals that can be directly fed to controller. Whenever the metal piece is detected the trigger pulse is sent to the timer which keeps on incrementing and when the timer reaches ff h value an interrupt will be generated in the next cycle through its overflow bit.

4.2.2 IR Sensor

The IR sensor is given the required dc supply from the battery. From fig4.5 it can be seen that the output from the sensor is connected to the input pin of PC817 opto coupler's pin 1. The output from the opto coupler pin 4 is given to the port 0 pin 3. Whenever an unknown obstacle is detected the reflected IR rays will not reach the sensor and an output voltage will be produced which is passed on to the controller through the opto coupler. The opto coupler is used for isolation purpose and for producing digital switching signals that can be directly fed to controller

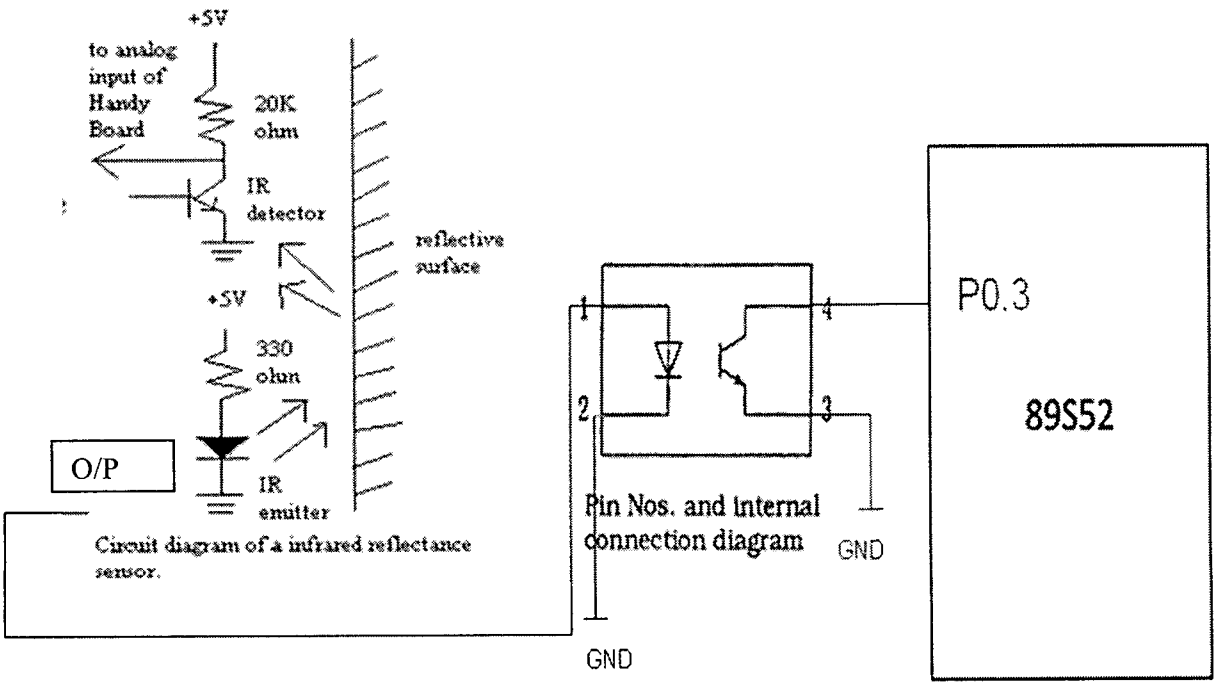


Fig 4.5 IR SENSOR INTERFACING CIRCUIT

4.3 INTERFACING OF BUZZER

The pin 10 of the microcontroller is connected to pin 7 of the ULN2003 driver and the pin 11 of the microcontroller is connected to pin 6 of the ULN2003 driver. The pin 10 of the driver is used to control the sweep motor. The driver acts as an isolation device and produces the required current to drive the buzzer.

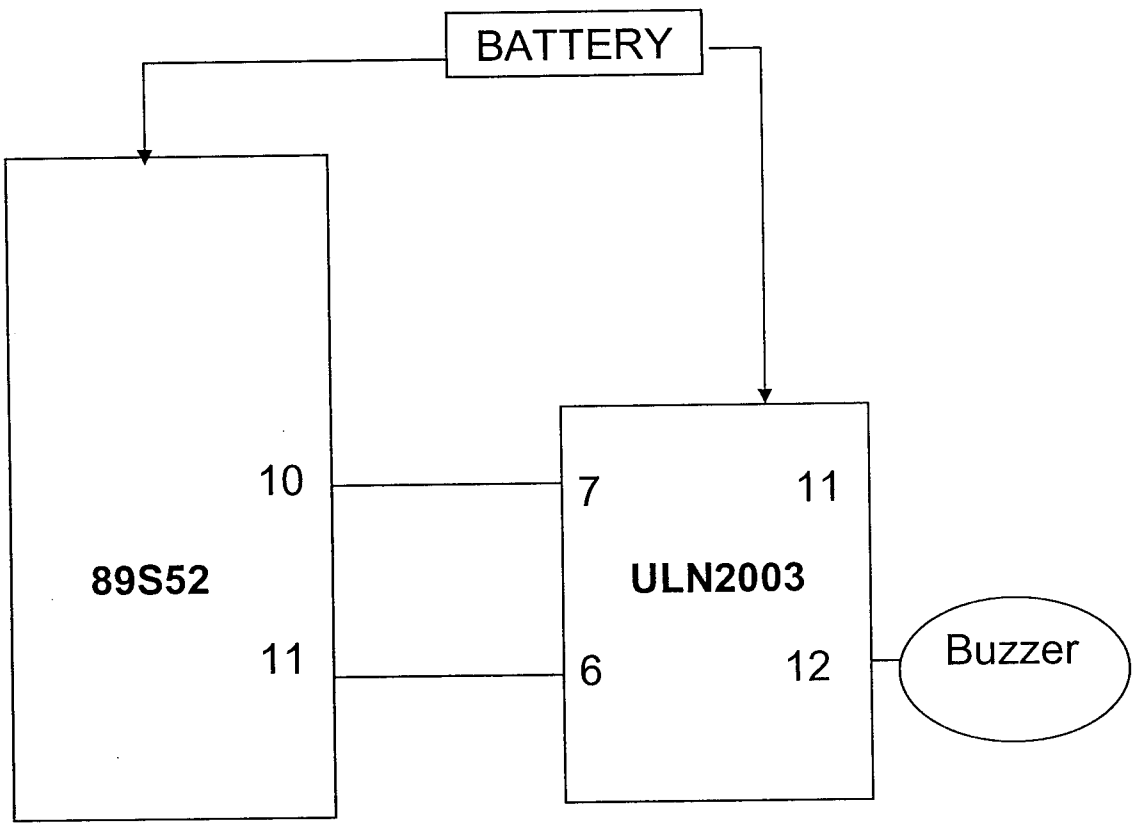
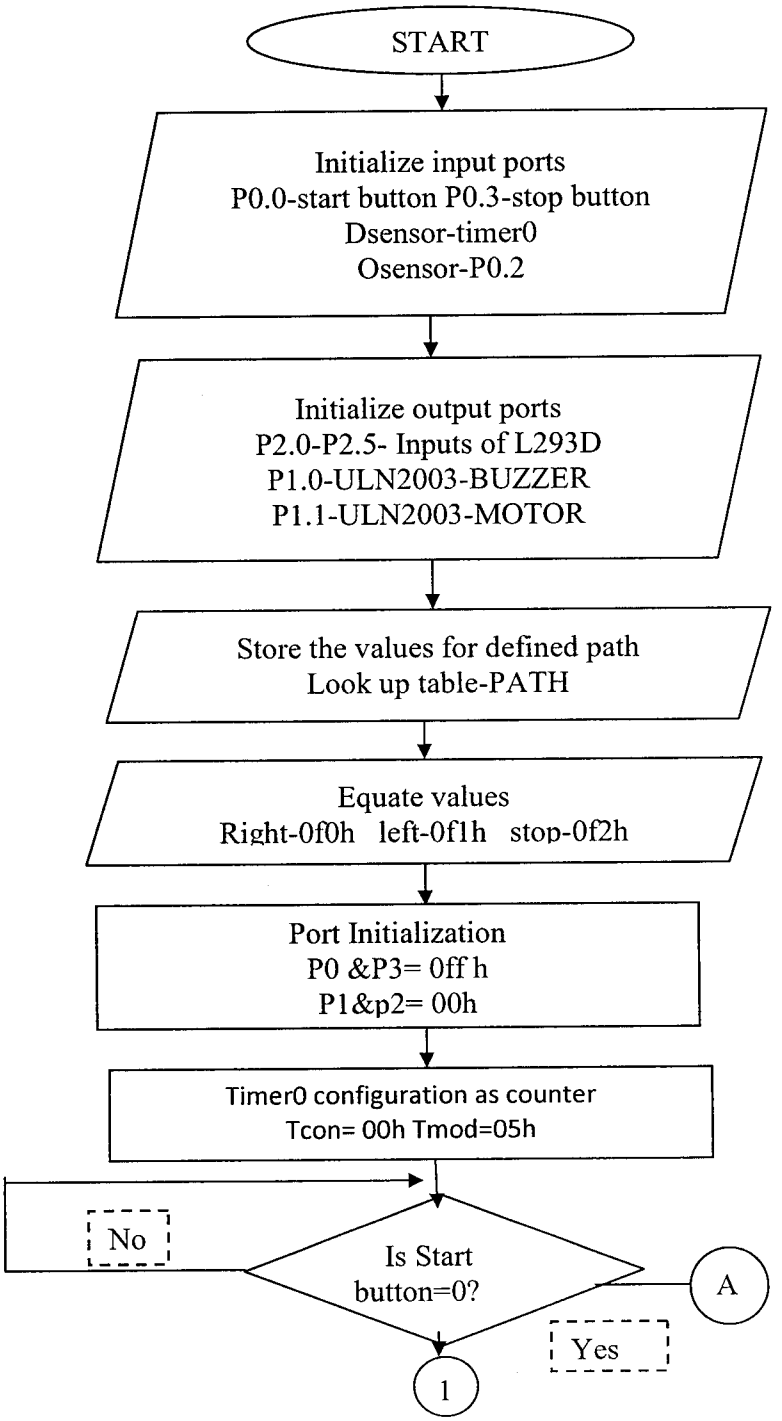
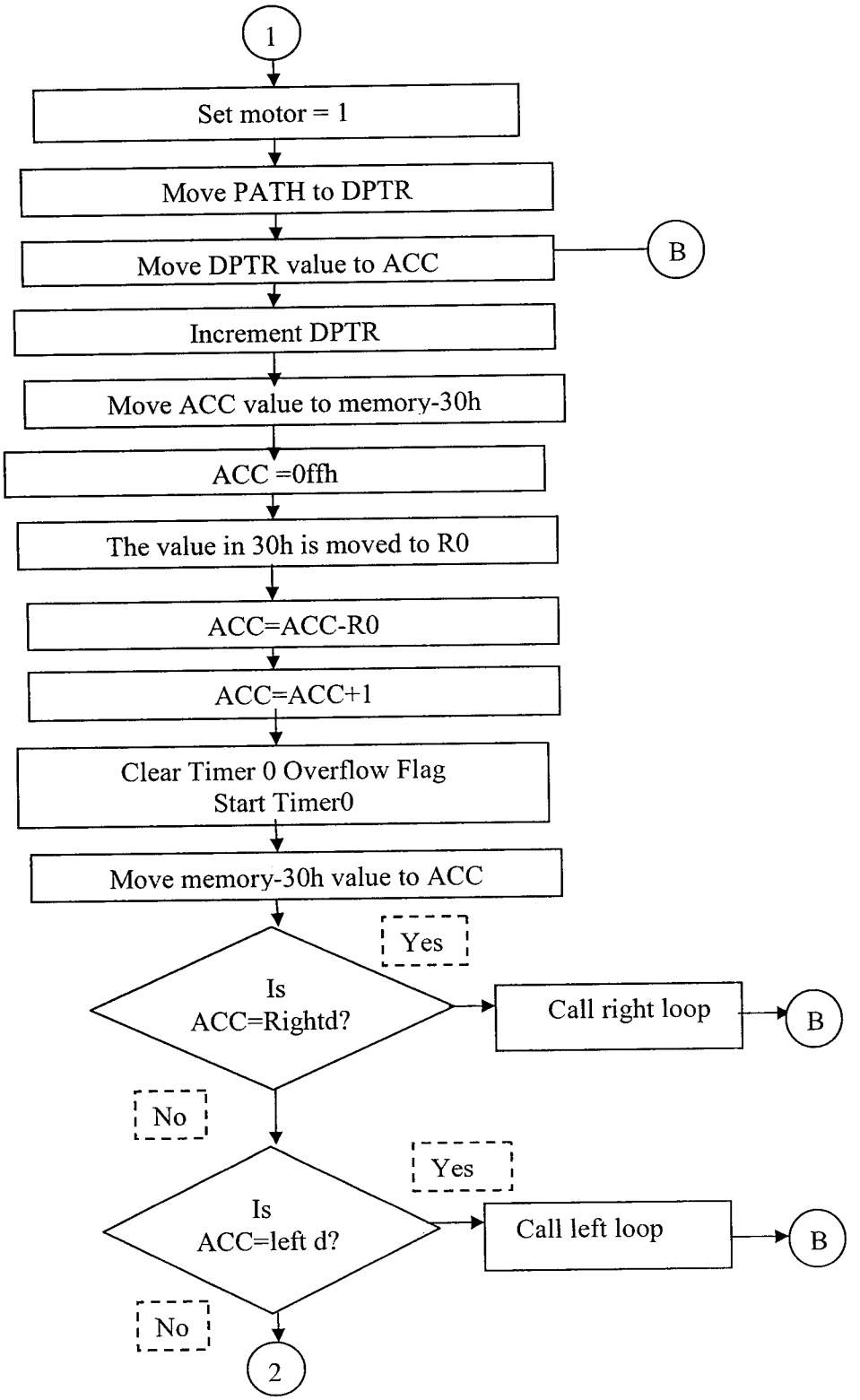


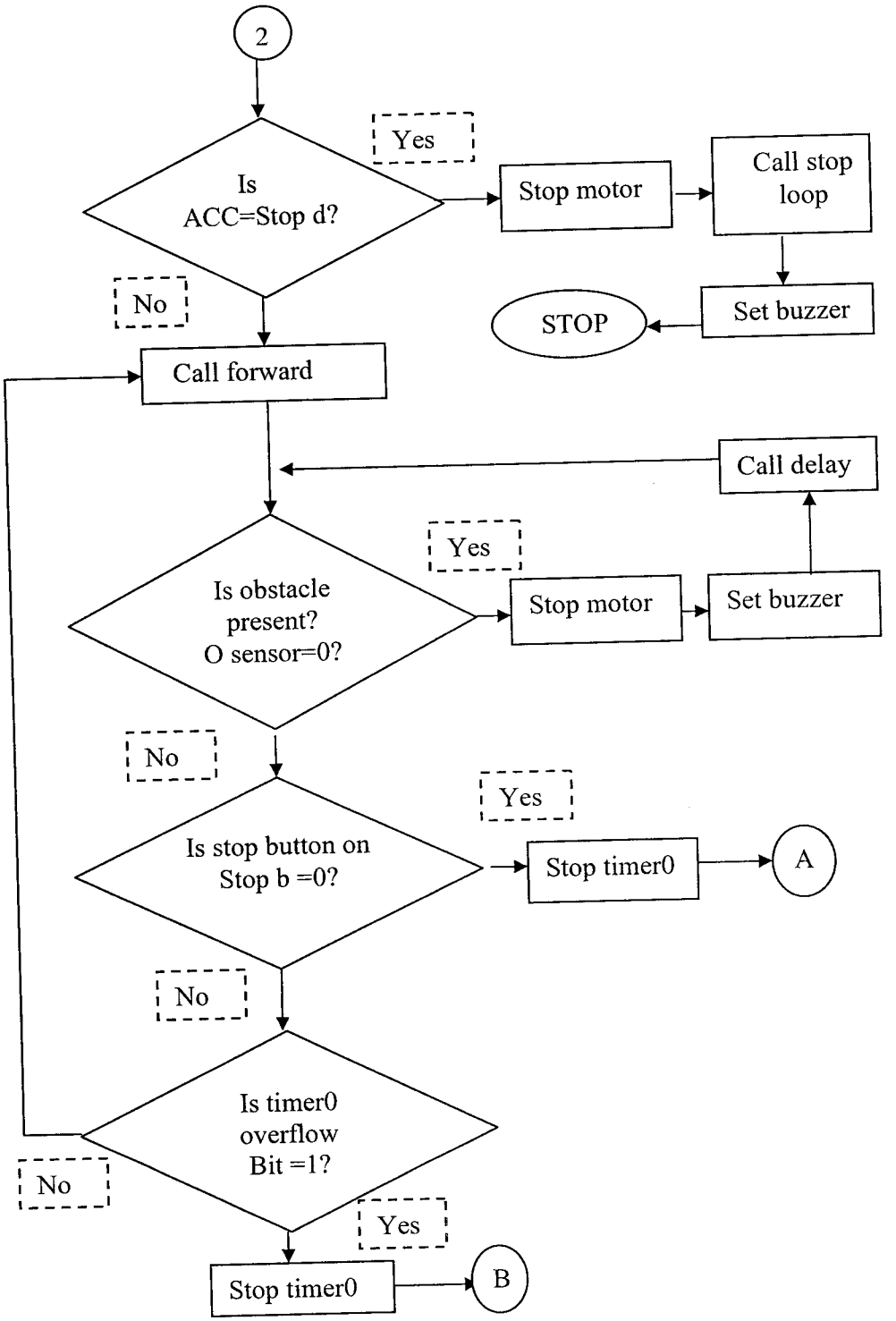
Fig 4.6 BUZZER INTERFACING CIRCUIT

Chapter 5

PROGRAM FLOW




1
Set motor = 1
Move PATH to DPTR
Move DPTR value to ACC
B
Increment DPTR
Move ACC value to memory-30h
ACC =0ffh
The value in 30h is moved to R0
ACC=ACC-R0
ACC=ACC+1
Clear Timer 0 Overflow Flag
Start Timer0
Move memory-30h value to ACC
Yes
Is
ACC=Rightd?
Call right loop
B
No
Yes
Is
ACC=left d?
Call left loop
B
No
2


2
Is
ACC=Stop d?
Yes
Stop motor
Call stop
loop
Set buzzer
STOP
No
Call forward
Call delay
Is obstacle
present?
O sensor=0?
Yes
Stop motor
Set buzzer
No
Is stop button on
Stop b =0?
Yes
Stop timer0
A
No
Is timer0
overflow
Bit =1?
No
Yes
Stop timer0
B

Chapter 6

CONCLUSION

This project provides solution for cleaning large spaces with fixed obstacles in an efficient and reliable manner. It finds its application in places like parking lots, shopping malls, libraries, auditoriums etc. depending on the varying room dimensions.

The robot works with a battery that is rechargeable and has a long life time. The power requirements were satisfied without much complexity. Since the sweeping mechanism used is a simple brush with the collector, dust can be disposed easily and replacement can be done without any hardware complexity. Different sizes of brush can be placed to remove various kinds of dust particles. This makes it more flexible.

Emptying the catch bin after a few minutes of testing is proof that although the sweeper might not be picking up everything in sight it clearly pulls in enough grime to be considered a success.

Considerations will be given to extend the project by detecting the dimensions of unknown obstacles by use of new algorithm and continuation of the path .Using RFID cleaning can be extended to several rooms.

APPENDIX

DATASHEET1

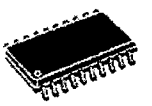
L293

SGS-THOMSON MICROELECTRONICS

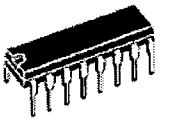
L293D
L293DD

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (non repetitive) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES



SO(12+4+4)



Powerdip (12+2+2)

ORDERING NUMBERS:

L293DD

L293D

DESCRIPTION

The Device is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

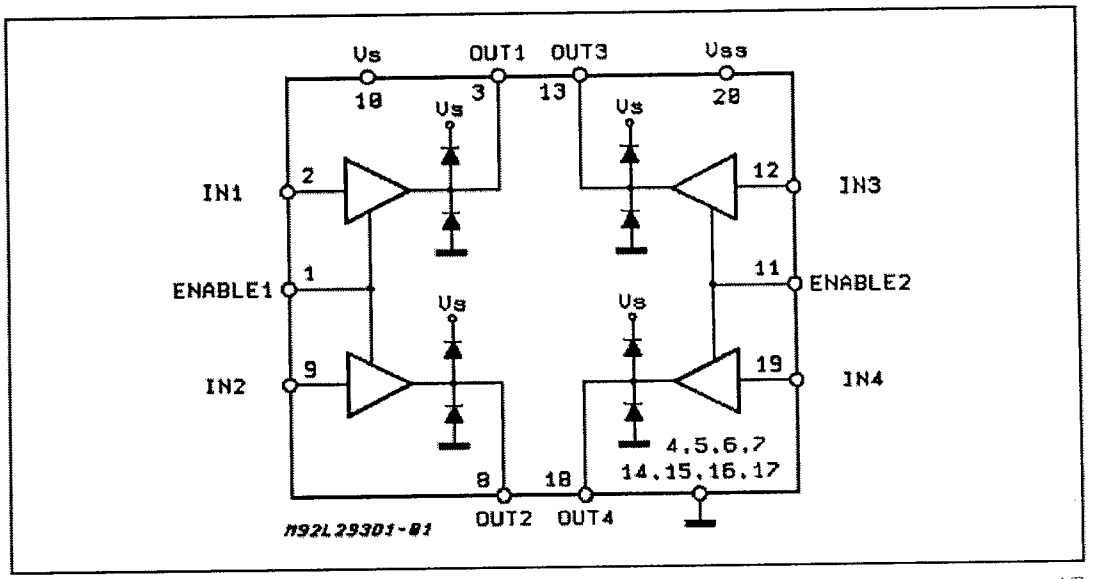
To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

The L293D is assembled in a 16 lead plastic packaage which has 4 center pins connected together and used for heatsinking

The L293DD is assembled in a 20 lead surface mount which has 8 center pins connected together and used for heatsinking.

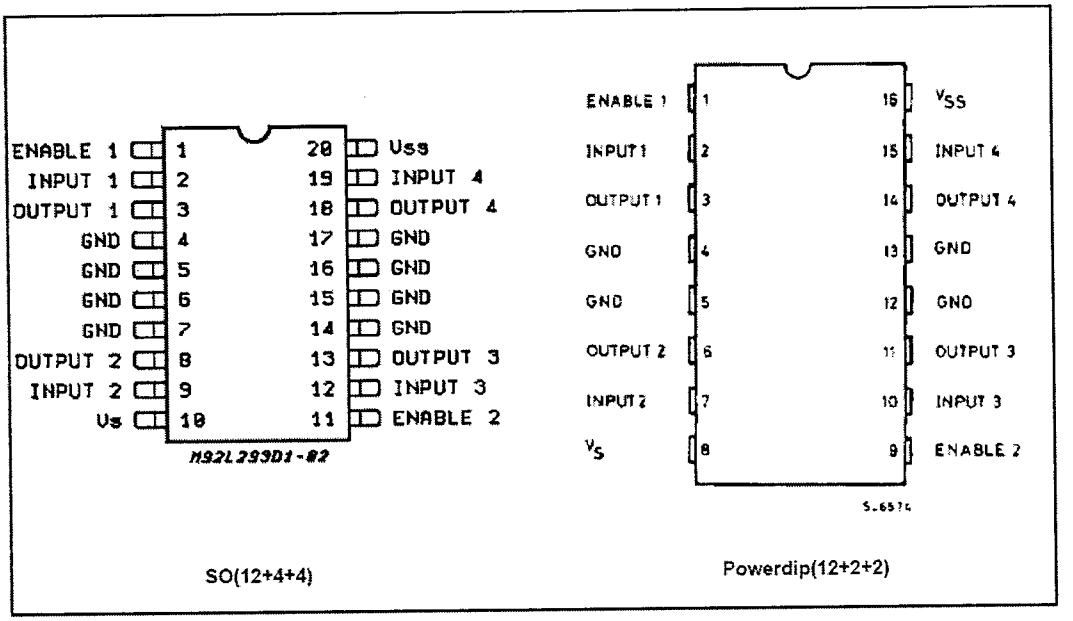
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	36	V
V_{SS}	Logic Supply Voltage	36	V
V_i	Input Voltage	7	V
V_{en}	Enable Voltage	7	V
I_o	Peak Output Current (100 µs non repetitive)	1.2	A
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C	4	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

PIN CONNECTIONS (Top view)



SO(12+4+4)

Powerdip(12+2+2)

THERMAL DATA

Symbol	Decription		DIP	SO	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	max.	–	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance junction-ambient	max.	80	50 (*)	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max.	14	–	

(*) With 6sq. cm on board heatsink.

ELECTRICAL CHARACTERISTICS (for each channel, V_S = 24 V, V_{SS} = 5 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 10)		V_{SS}		36	V
V_{SS}	Logic Supply Voltage (pin 20)		4.5		36	V
I_S	Total Quiescent Supply Current (pin 10)	V_i = L ; I_O = 0 ; V_{en} = H		2	6	mA
		V_i = H ; I_O = 0 ; V_{en} = H		16	24	mA
		V_{en} = L			4	mA
I_{SS}	Total Quiescent Logic Supply Current (pin 20)	V_i = L ; I_O = 0 ; V_{en} = H		44	60	mA
		V_i = H ; I_O = 0 ; V_{en} = H		16	22	mA
		V_{en} = L		16	24	mA
V_{IL}	Input Low Voltage (pin 2, 9, 12, 19)		– 0.3		1.5	V
V_{IH}	Input High Voltage (pin 2, 9, 12, 19)	$V_{SS} \leq 7$ V	2.3		V_{SS}	V
		$V_{SS} > 7$ V	2.3		7	V
I_{IL}	Low Voltage Input Current (pin 2, 9, 12, 19)	V_{IL} = 1.5 V			– 10	µA
I_{IH}	High Voltage Input Current (pin 2, 9, 12, 19)	$2.3\ V \leq V_{IH} \leq V_{SS} - 0.6$ V		30	100	µA
$V_{en\,L}$	Enable Low Voltage (pin 1, 11)		– 0.3		1.5	V
$V_{en\,H}$	Enable High Voltage (pin 1, 11)	$V_{SS} \leq 7$ V	2.3		V_{SS}	V
		$V_{SS} > 7$ V	2.3		7	V
$I_{en\,L}$	Low Voltage Enable Current (pin 1, 11)	$V_{en\,L}$ = 1.5 V		– 30	– 100	µA
$I_{en\,H}$	High Voltage Enable Current (pin 1, 11)	$2.3\ V \leq V_{en\,H} \leq V_{SS} - 0.6$ V			± 10	µA
$V_{CE(sat)H}$	Source Output Saturation Voltage (pins 3, 8, 13, 18)	I_O = – 0.6 A		1.4	1.8	V
$V_{CE(sat)L}$	Sink Output Saturation Voltage (pins 3, 8, 13, 18)	I_O = + 0.6 A		1.2	1.8	V
V_F	Clamp Diode Forward Voltage	I_O = 600nA		1.3		V
t_r	Rise Time (*)	0.1 to 0.9 V_O		250		ns
t_f	Fall Time (*)	0.9 to 0.1 V_O		250		ns
t_{on}	Turn-on Delay (*)	0.5 V_i to 0.5 V_O		750		ns
t_{off}	Turn-off Delay (*)	0.5 V_i to 0.5 V_O		200		ns

(*) See fig. 1.

DATASHEET 2

AT8952

Features

- Compatible with MCS-51™ Products
- 8 Kbytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- Eight Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

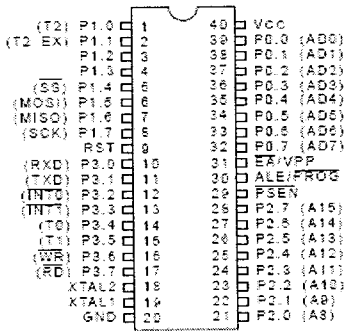
Description

The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8 Kbytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C52 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

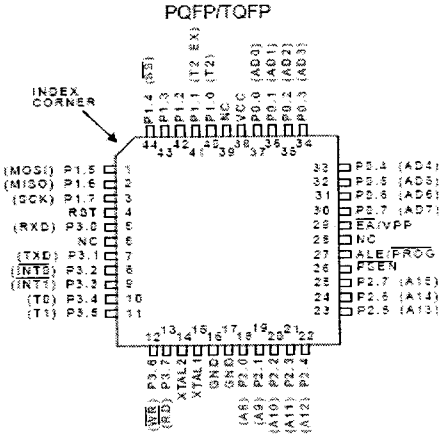
(continued)

Pin Configurations

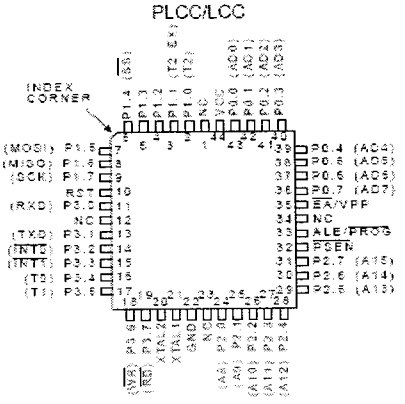
PDIP/Cerdip



PQFP/TQFP



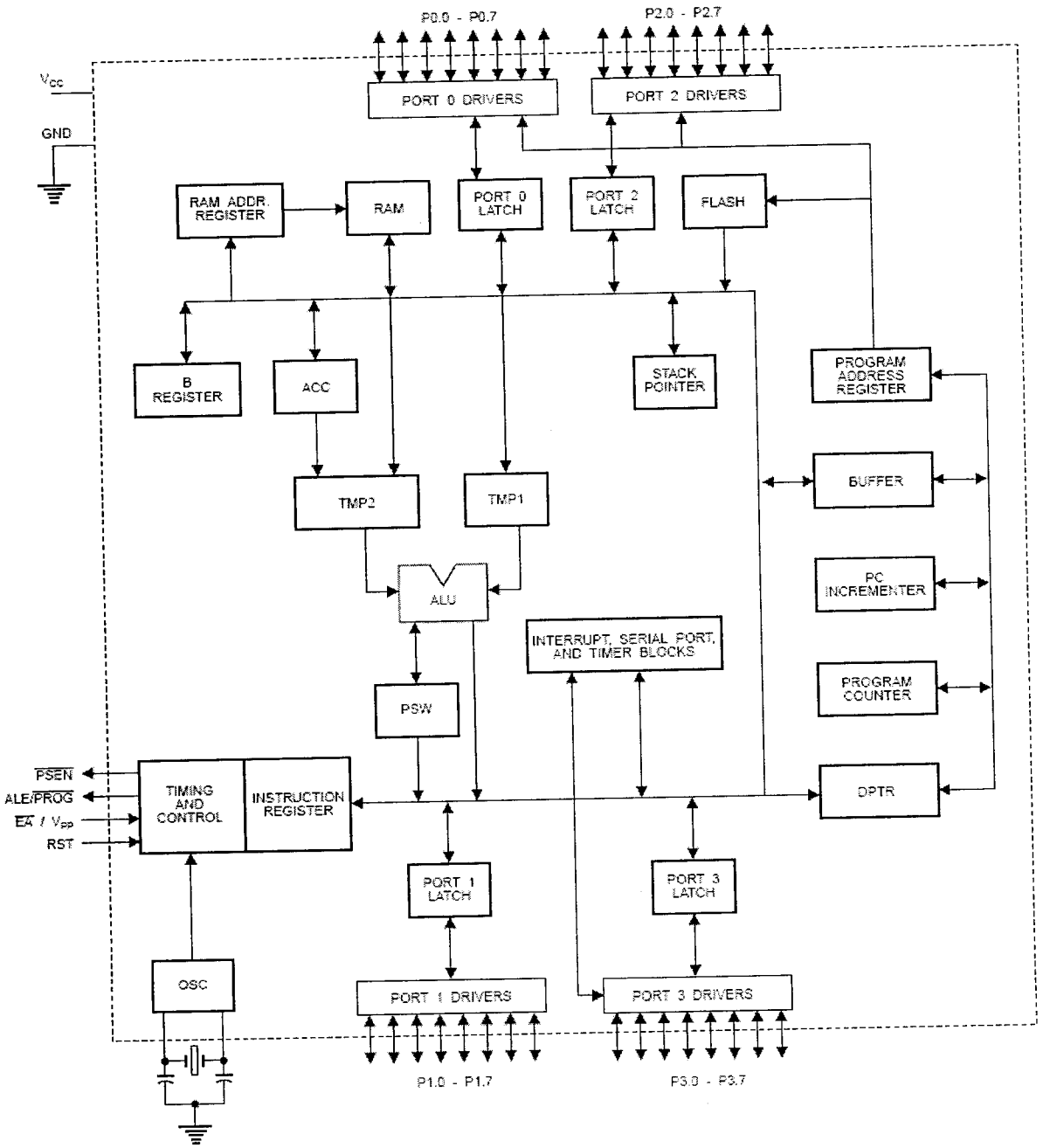
PLCC/LCC



8-Bit Microcontroller with 8 Kbytes Flash

AT89C52

Block Diagram



Description (Continued)

The AT89C52 provides the following standard features: 8 Kbytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

(continued)

Pin Description (Continued)

n normal operation, ALE is emitted at a constant rate of /6 the oscillator frequency and may be used for external iming or clocking purposes. Note, however, that one ALE ulse is skipped during each access to external data nemory.

f desired, ALE operation can be disabled by setting bit 0 if SFR location 8EH. With the bit set, ALE is active only luring a MOVX or MOVC instruction. Otherwise, the pin is veakly pulled high. Setting the ALE-disable bit has no ef- ect if the microcrontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external pro- gram memory.

When the AT89C52 is executing code from external pro- gram memory, PSEN is activated twice each machine cy- cle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 1. AT89C52 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000			PCON 0XXX0000	87H

Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

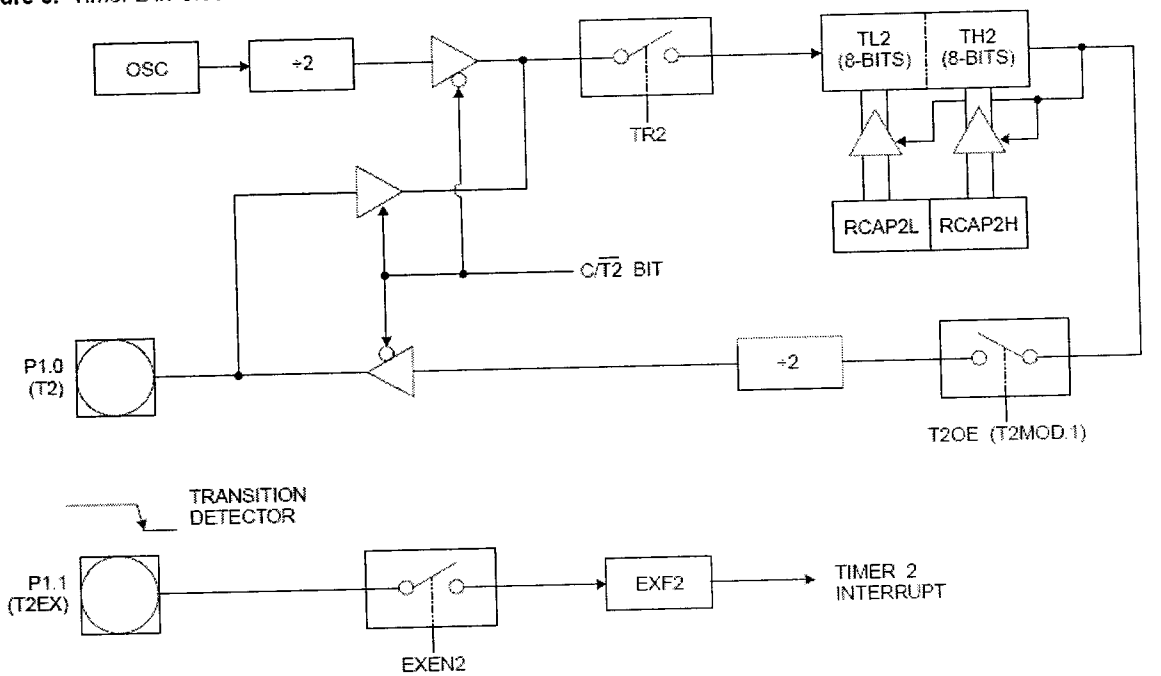
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 5. Timer 2 in Clock-Out Mode



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 4) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
$C/\overline{T2}$	Timer or counter select for Timer 2. $C/\overline{T2}$ = 0 for timer function. $C/\overline{T2}$ = 1 for external event counter (falling edge triggered).
$CP/\overline{RL2}$	Capture/Reload select. $CP/\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. $CP/\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Data Memory

The AT89C52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

MOV 0A0H, #data

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

MOV @R0, #data

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

The UART in the AT89C52 operates the same way as the UART in the AT89C51.

Interrupts

The AT89C52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TFI, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

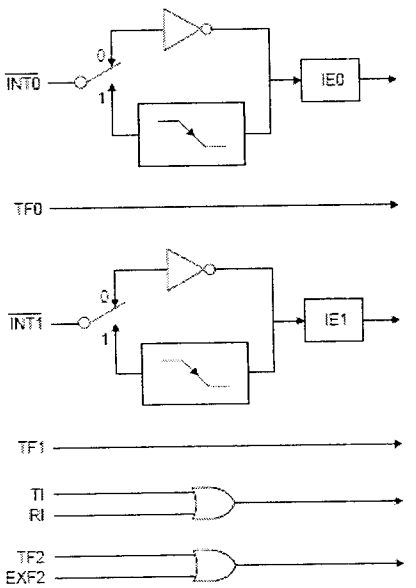
(MSB)							(LSB)
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

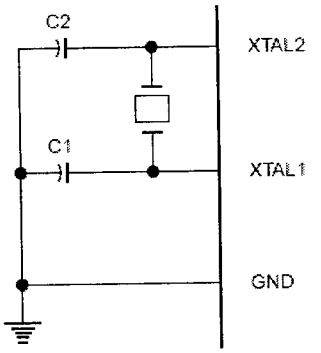
Figure 6. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 7. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 7. Oscillator Connections



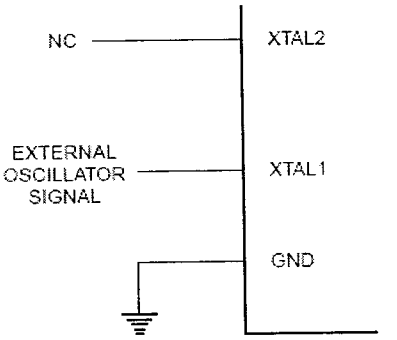
Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Figure 8. External Clock Drive Configuration



Power Down Mode

In the power down mode, the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before Vcc is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Status of External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89C52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled.
3	P	P	U	Same as mode 2, but verify is also disabled.
4	P	P	P	Same as mode 3, but external execution is also disabled.

Programming the Flash

The AT89C52 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C52 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C52 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12 V	V_{PP} = 5 V
Top-Side Mark	AT89C52 xxxx yyww	AT89C52 xxxx-5 yyww
Signature	(030H)=1EH (031H)=52H (032H)=FFH	(030H)=1EH (031H)=52H (032H)=05H

The AT89C52 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C52, the address, data and control signals should be set up according to the Flash programming mode table and Figures 9 and 10. To program the AT89C52, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12 V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C52 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true $\overline{data}$ is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock

(continued)

Programming the Flash (Continued)

bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all 1s. The chip erase operation must be executed before the code memory can be reprogrammed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 52H indicates 89C52
(032H) = FFH indicates 12 V programming
(032H) = 05H indicates 5 V programming

Programming Interface

Every code byte in the Flash array can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V(1)	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L	(2)	H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L		H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Notes: 1. The signature byte at location 032H designates whether V_{PP} = 12 V or V_{PP} = 5 V should be used to enableprogramming.

2. Chip Erase requires a 10 ms $\overline{PROG}$ pulse.

Figure 9. Programming the Flash Memory

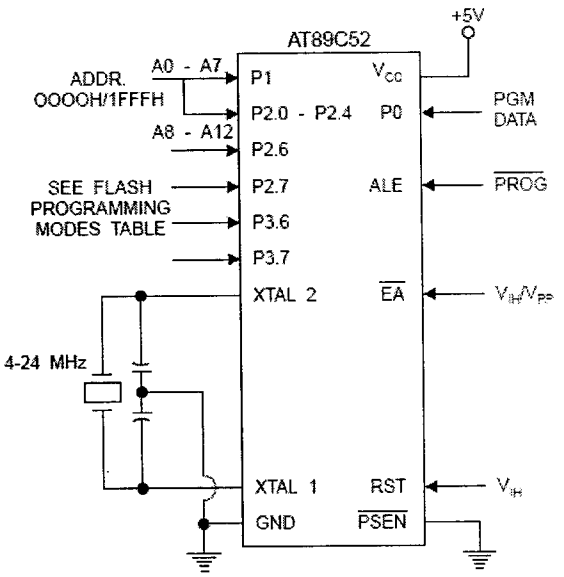
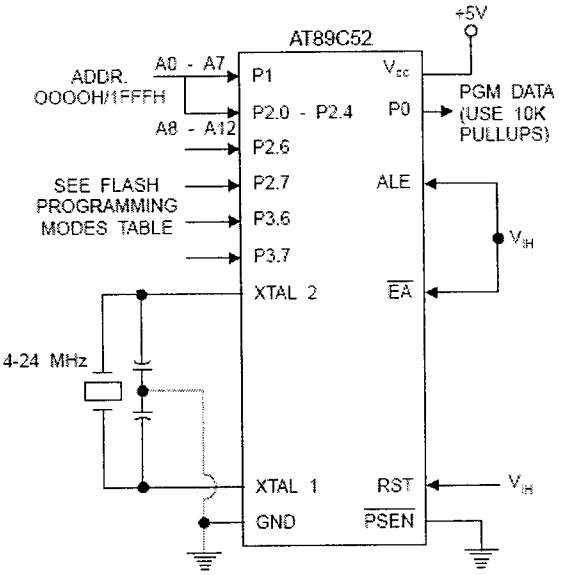


Figure 10. Verifying the Flash Memory



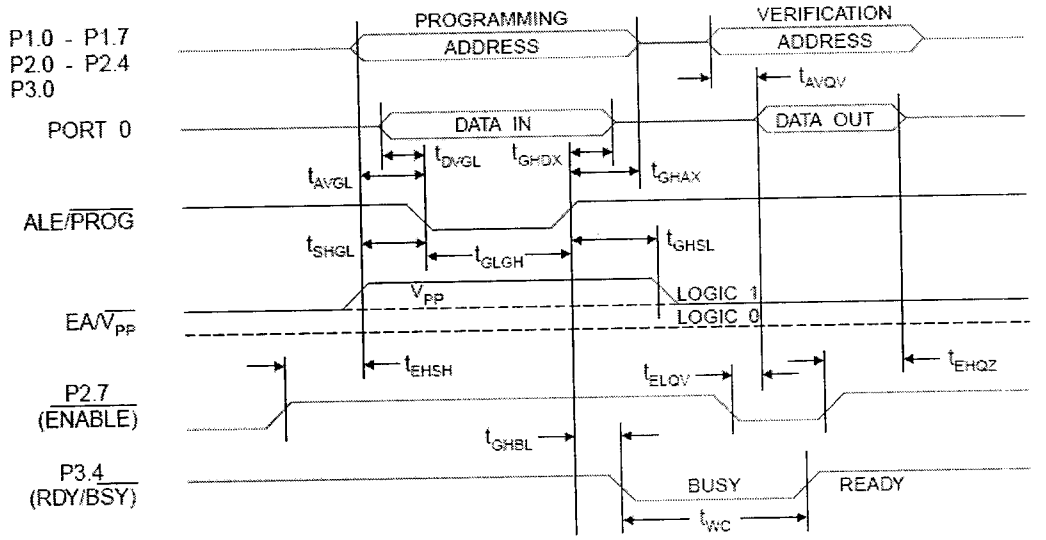
Flash Programming and Verification Characteristics

T_A = 21°C to 27°C, V_{CC} = 5.0 ± 10%

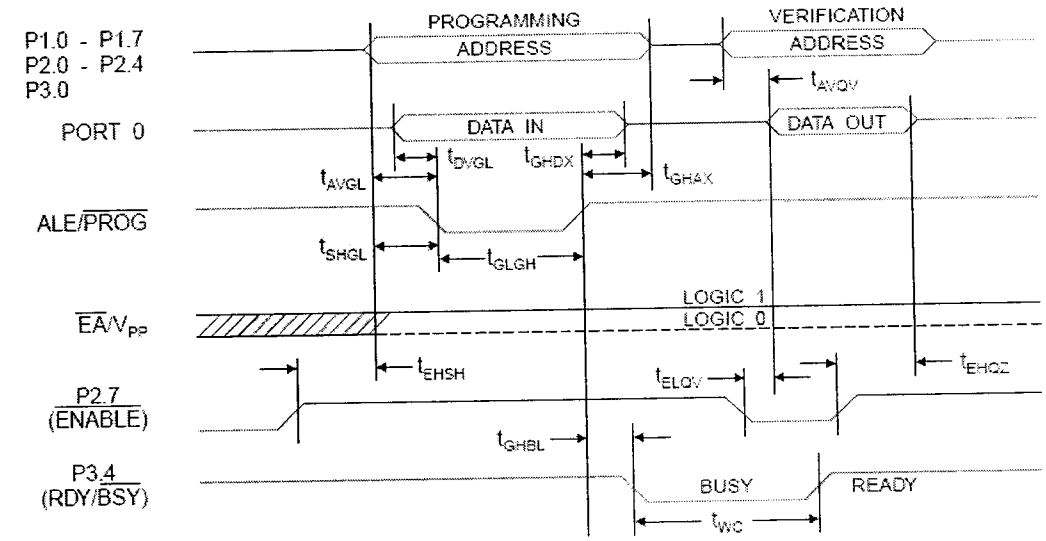
Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}[1]	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQV}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode



Flash Programming and Verification Waveforms - Low Voltage Mode



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0 V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, PSEN)	I_{OH} = -60 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5 V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45 V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2 V		-650	µA
I_{LI}	Input Leakage Current (Port 0, EA)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode[2]	V_{CC} = 6 V		100	µA
		V_{CC} = 3 V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin:10 mA
Maximum I_{OL} per 8-bit port:
Port 0:26 mA
Ports 1,2, 3:15 mA
Maximum total IOL for all output pins:71 mA
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2 V.

A.C. Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}-40$		ns
t_{AVLL}	Address Valid to ALE Low	28		$t_{CLCL}-13$		ns
t_{LLAX}	Address Hold After ALE Low	48		$t_{CLCL}-20$		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}-65$	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		$t_{CLCL}-13$		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}-20$		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}-45$	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		$t_{CLCL}-10$	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		$t_{CLCL}-8$		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}-55$	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}-100$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}-100$		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}-90$	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}-28$	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}-150$	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}-165$	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}-75$		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		$t_{CLCL}-20$		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}-120$		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		$t_{CLCL}-20$		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	$t_{CLCL}-20$	$t_{CLCL}+25$	ns

T

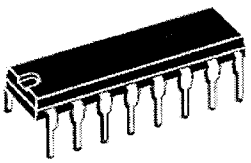
DATASHEET3

ULN2003

ULN2001A-ULN2002A
ULN2003A-ULN2004A

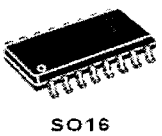
SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRATED SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



DIP16

ORDERING NUMBERS: ULN2001A/2A/3A/4A



SO16

ORDERING NUMBERS: ULN2001D/2D/3D/4D

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

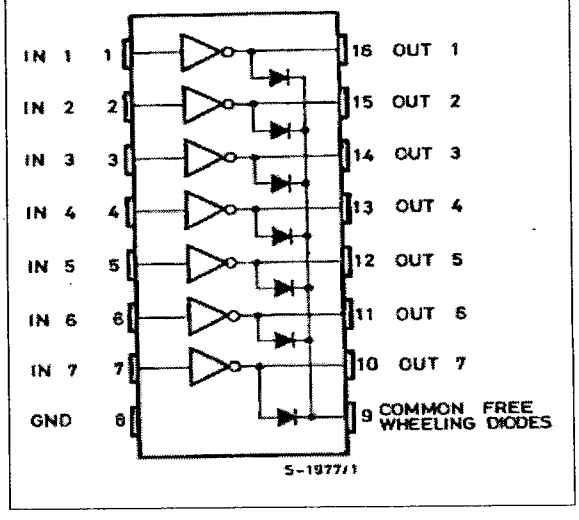
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25V PMOS
ULN2003A	5V TTL, CMOS
ULN2004A	6–15V CMOS, PMOS

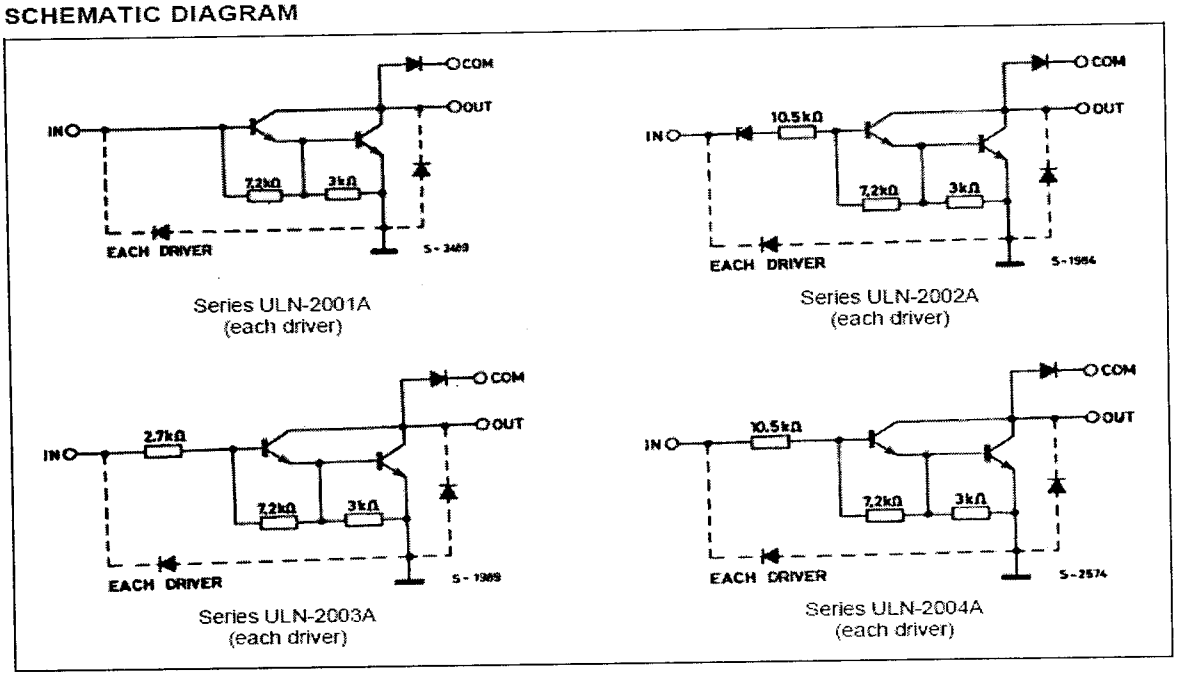
These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.

PIN CONNECTION



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

THERMAL DATA

Symbol	Parameter		DIP16	SO16	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70	120	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V T_{amb} = 70°C, V_{CE} = 50V T_{amb} = 70°C for ULN2002A V_{CE} = 50V, V_i = 6V for ULN2004A V_{CE} = 50V, V_i = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA, I_B = 250µA I_C = 200 mA, I_B = 350µA I_C = 350mA, I_B = 500µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2 2 2
$I_{i(on)}$	Input Current	for ULN2002A, V_i = 17V for ULN2003A, V_i = 3.85V for ULN2004A, V_i = 5V V_i = 12V		0.82 0.93 0.35 1	1.25 1.35 0.5 1.45	mA mA mA mA	3 3 3 3
$I_{i(off)}$	Input Current	T_{amb} = 70°C, I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	V_{CE} = 2V for ULN2002A I_C = 300mA for ULN2003A I_C = 200mA I_C = 250mA I_C = 300mA for ULN2004A I_C = 125mA I_C = 200mA I_C = 275mA I_C = 350mA			 13 2.4 2.7 3 5 6 7 8	V	5
h_{FE}	DC Forward Current Gain	for ULN2001A V_{CE} = 2V, I_C = 350mA	1000				2
C_i	Input Capacitance			15	25	pF	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	
I_R	Clamp Diode Leakage Current	V_R = 50V T_{amb} = 70°C, V_R = 50V			50 100	µA µA	6 6
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7