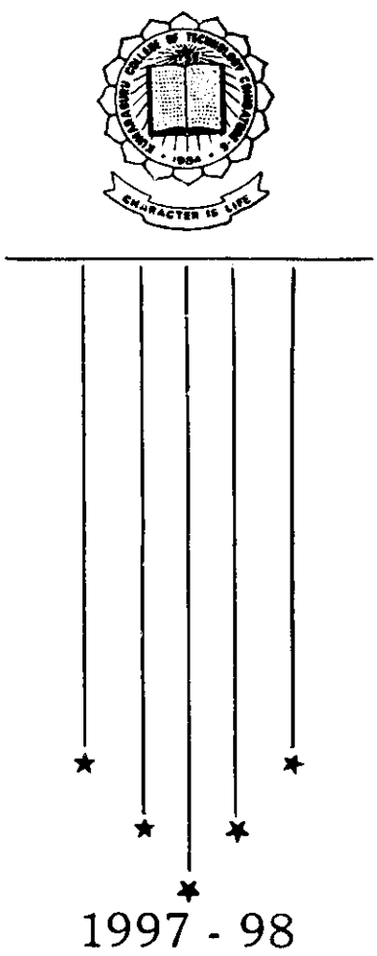
P-328

# Maximum Demand Monitor and Controller

*PROJECT REPORT*



1997 - 98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IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

BACHELOR OF ENGINEERING IN ELECTRICAL AND ELECTRONICS ENGINEERING

BRANCH OF BHARATHIAR UNIVERSITY
COIMBATORE


Department of Electrical and Electronic Engineering

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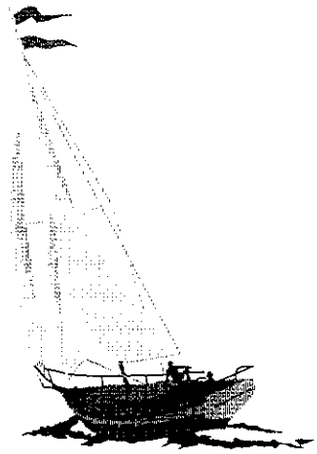

# CERTIFICATE

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## CERTIFICATE

*This is to certify that the report entitled*

**"MAXIMUM DEMAND MONITOR AND CONTROLLER"**

*has been submitted by*

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*during the academic year 1997-98*

4/5/98

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Head of the Department.

*Certified that the candidate with University Register Number ..... was examined in the project work & Viva-voce examination held on.....*

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*Internal Examiner*

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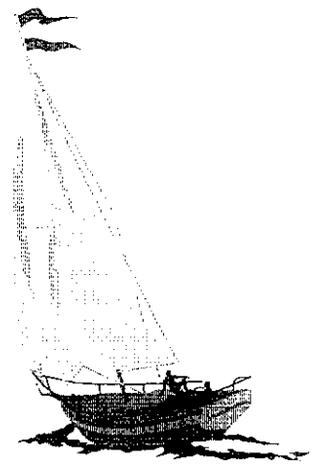
*External Examiner.*

Dedicated

To Our

Beloved Parents



# ACKNOWLEDGEMENT

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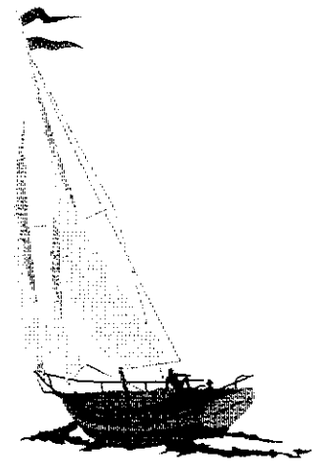
We are thankful to **Mr.M.VIVEKANANDHAN, M.Sc., (Electronics)** and **Mr.C.SREEDHAR, M.Sc.,(Electronics)** for helping us a lot to completion of the project.

We are very much thankful to our friends for having helped us in many ways during the course of the project. Also we thank lot technicians to their co-operation during the course of this work.



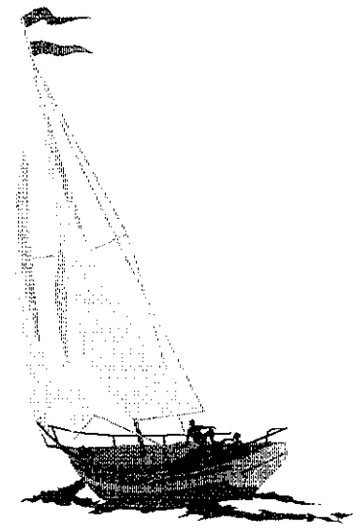
# SYNOPSIS

# SYNOPSIS

Power is the building block of Industries, the cradle for the millinium. Distribution of power properly among the masses is the need of the hour. Any Industry should not consume power above a limit during a stipulated time period as specified by the Electricity Board. So in order to continuously monitor the power and control the peak load maximum Demand Monitor and controller system is used.

This project aims at developing a microprocessor based maximum Demand Monitor and controller which is necessary to be used in all types of Industries. A control circuit for measuring and controlling the maximum demand is designed and assembled in PCB. An efficient assembly language program is developed to support the hardware. In this project the load consumption of the industry is continuously monitored and during a specific period of time, the system connects excess load to the generator automatically by energising the relays in order to maintain the maximum demand on the EB line as per the demand sanctioned.

Design and developement of hardware part and software implementation to support the hardware to energise the relay system are presented in the report. This microprocessor based maximum demand monitor and controller was tested for its performance in the Electrical Machines lab in the EEE department.



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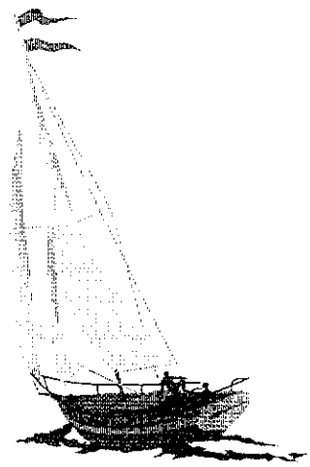
## CHAPTER 2



## CHAPTER 3



# INTRODUCTION

# CHAPTER 1

# INTRODUCTION

Maximum demand monitor and controller is basically a monitoring system used for polling the lodes in operation. This system consists of a basic sensor unit , electronic circuits like opto-coupler, AND gate, regulator etc, micro processor and a display unit.

The physical arrangement to switch the excess load to the generater & vice versa is the relay . The relay used here is transister operated relay .

The performance of the system depends upon the sensing circuits and microprocessor programming. The display unit displays the loads in operation .

The idea of this project can be extended for industrial application and also for small power demands. Working model has been developed for small power application up to 7.5 Kw and its detailed design and implementation are given in this report.

Both applications serve the same purpose exept that the sensing circuit differs. The algorithm for both are the same. We will be discussing about the idea of these two application in the forth coming chapter.

## 1.1. INDUSTRIAL IMPLEMENTATION

In industrial point of view power conciderations are large. So three phase current is taken from the primary side and three phase voltage from the secondary side of the industrial transformer and fed as input to the multiplexure whose output is converted to the digital signal by the ADC and fed in to the microprocessor . The general idea is represented in fig 1.1.

Real time clock cicuit is used to indicate the peak hours to the microprocessor . The output signals of the microprocessor is given to the relay in to the action ie, it connects the excess load to the EB or generator. This idea explained in funtional flowchart shown in fig 1.2. Any details regarding voltage, current, power consumed etc are displayed using a seven segment six digit display.

## 1.2. WORKING MODEL

Here in this model the loads must be known. according to the maximum demand the excess load is connected to the relay. The general idea of this model is shown in fig 1.3.

`The sensing circuit is connected across each load,which senses whether the load across it is in operation or not. All the sensed signals are given to the AND gate except for the excess load signal which is

directly given to the mocroprocessor. When all the loads are in operation the AND gate output signal is 1 which is given to the microprocessor. The microprocessor first checks whether the time at present is within the peak hours. If it is within the peak hours then it checks whether the signal from the AND gate is1 or 0. If it is 1, then the excess load is connected to the geberator else it is connected to the EB line.

The sensing circuit sends the signals to the AND gate, only when the load is in operation, otherwise the AND signal output is taken as 0, because there would not be any signal from the sensing circuit. The sequence of operation of Maximum Demand Monitor and Controller is explained in functional flowchart in fig 1.4.

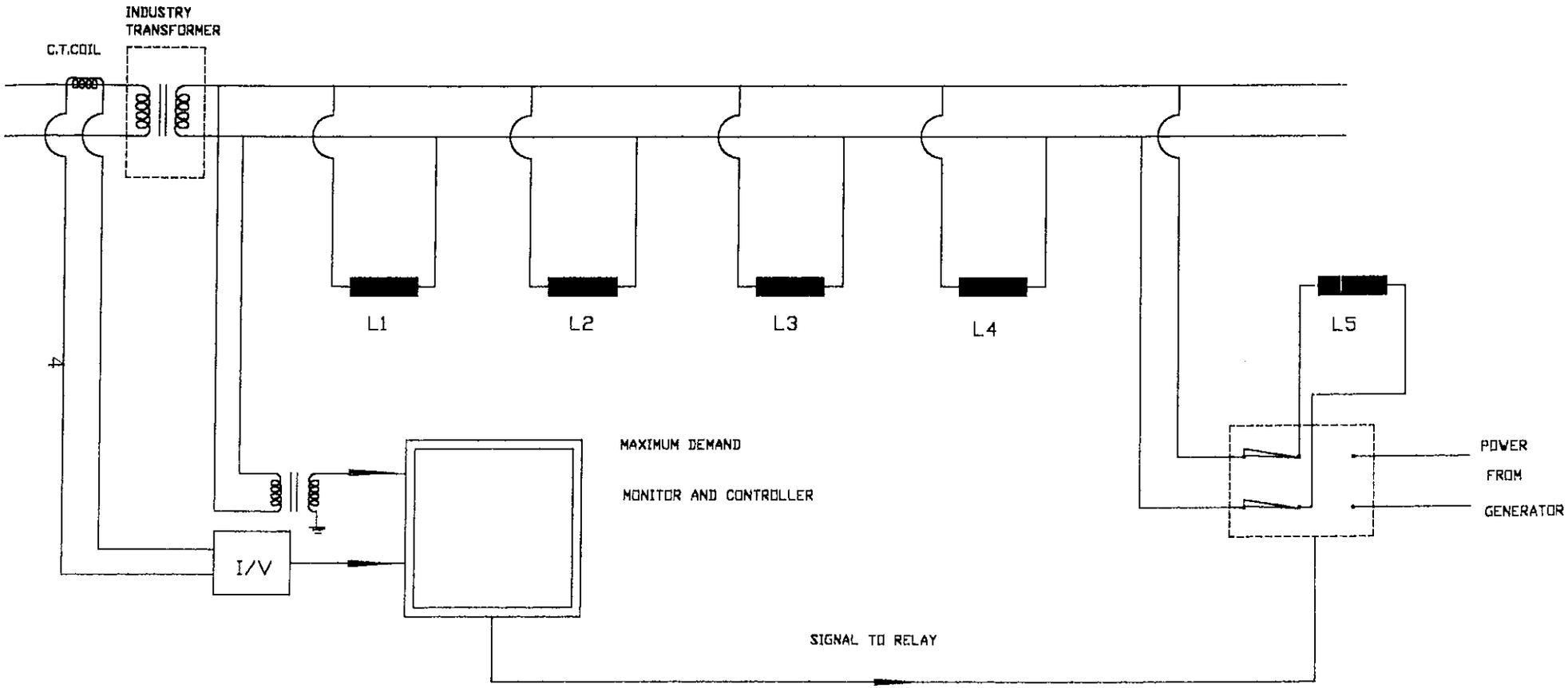



Fig 1.1 INDUSTRIAL APPLICATION OF MAXIMUM DEMAND MONITOR AND CONTROLLER

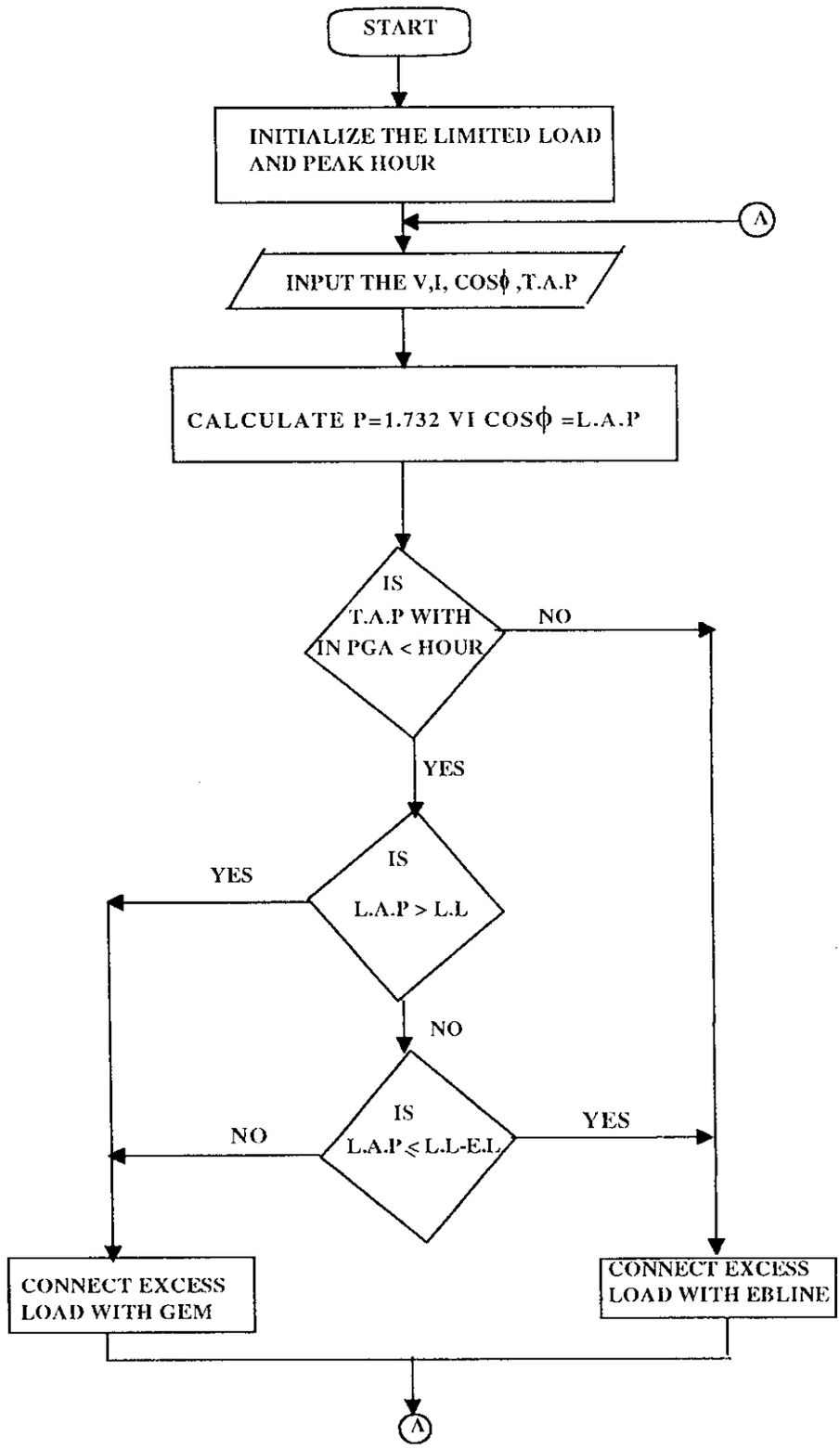



Fig. 1.2 FUNCTIONAL FLOWCHART

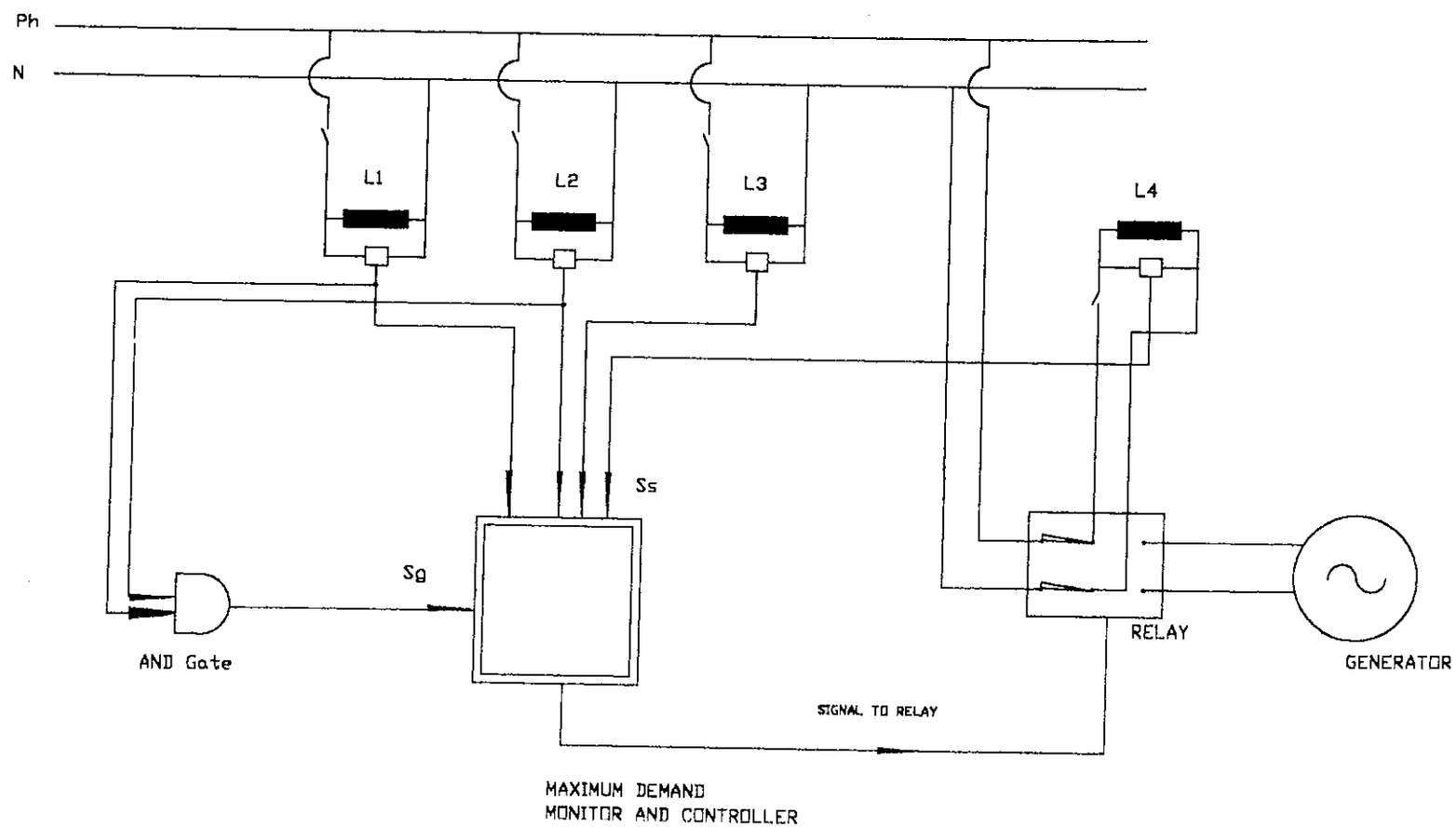



Fig 1.3 INDUSTRIAL APPLICATION OF MAXIMUM DEMAND MONITOR AND CONTROLLER

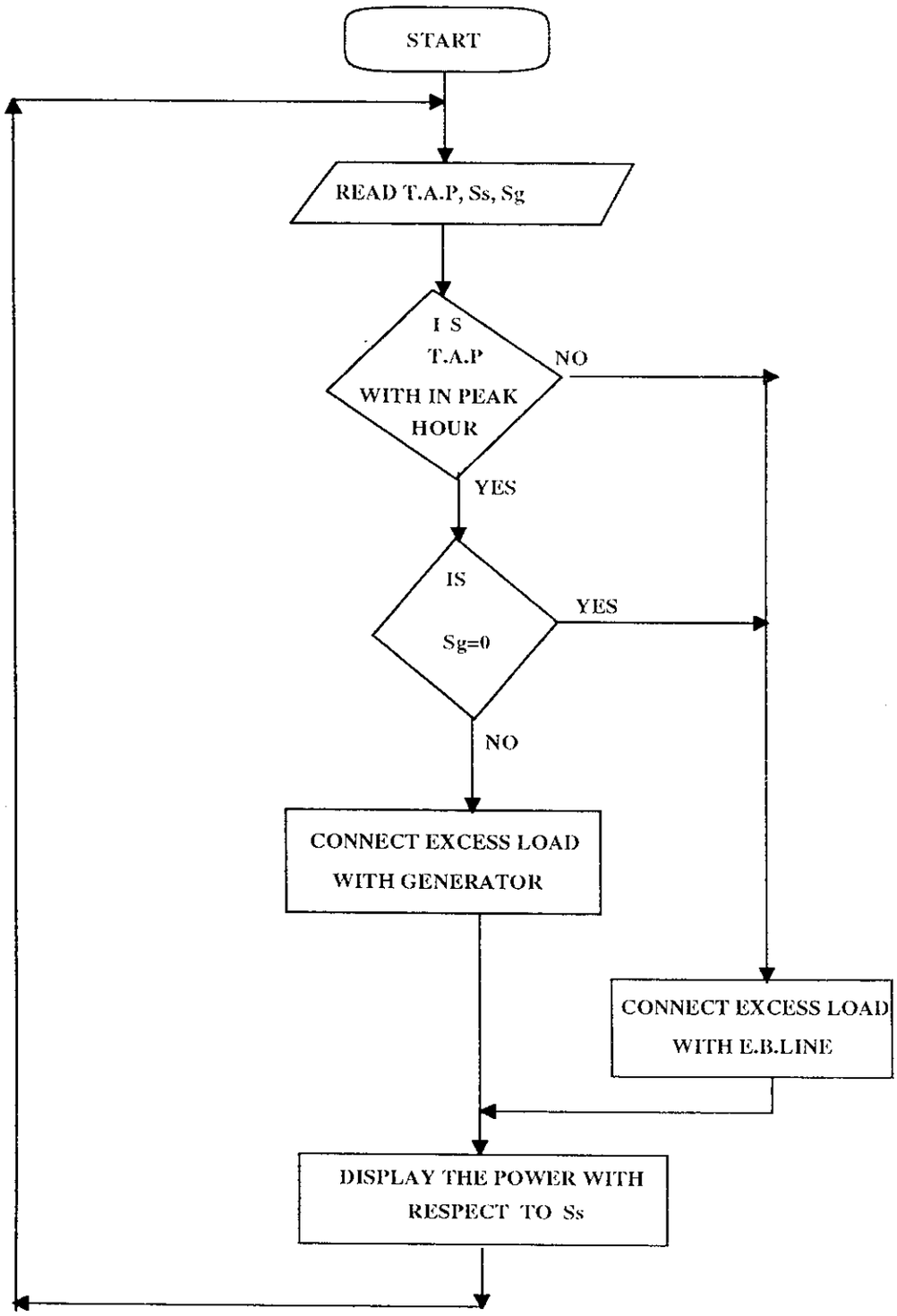



Fig. 1.4 FUNCTIONAL FLOWCHART OF MAXIMUM DEMAND MONITOR AND CONTROLLER

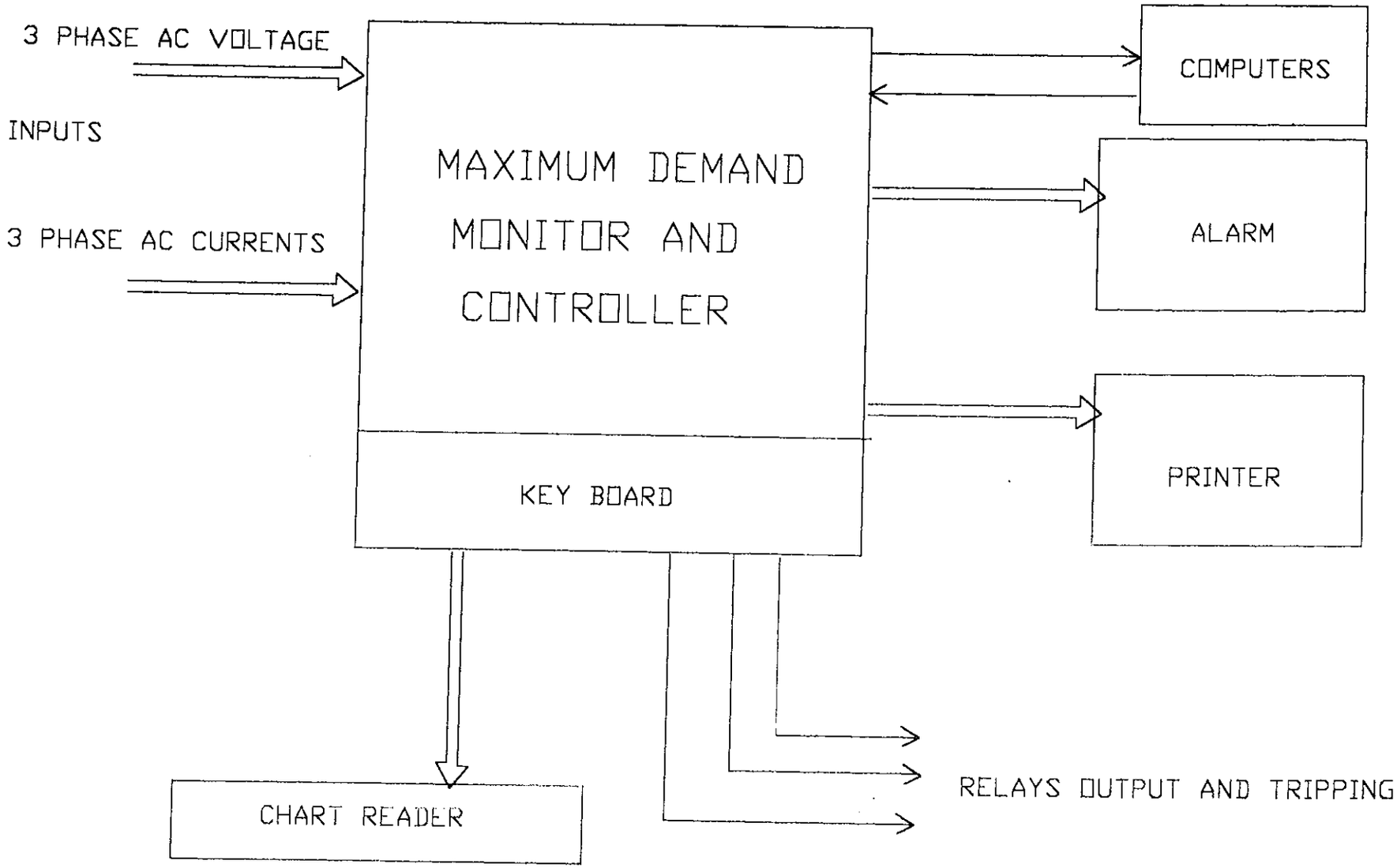



FIG. 1.5 ACCESSABILITIES OF MAXIMUM DEMAND MONITOR AND CONTROLLER

# HARDWARE DESIGN

# CHAPTER 2

# 2.HARDWARE DESIGN

## 2.1.INDUSTRIAL IMPLIMENTATION

The block diagram for the sensing circuit is given in fig 2. In actual case, the first stage consists of current to voltage converters employed for the channels corresponding to current inputs and potential transformer corresponding to voltage input. In this project the voltage and signals are given to the rectifier to restrict the negative voltage level and then fed to the multiplexure. From the multiplexure the signals are given to the microprocessor via the ADC. The microprocessor comunicates with the ADC with the help of status signals and obtains the digital input and performs various functions. At the same time the output of the multiplexure is fed to the conditioning circuit also, takes input directly from a particular channel prior to the multiplexure. The output of the conditioning circuit is also fed to the microprocessor which executes the appropriate measurement routine and displays voltage, current, power and phase. The digital display is done on a 7 segment 6 digit unit

### 2.1.0 CURRENT TO VOLTAGE CONVERTOR

The current to voltage converter provides a voltage proportional to current. The current to voltage conveter is shown in fig(2) Assuming ideal conditions,

$V_0 / V_s = -R_f / R_s$ (2.1)

where $V_s = R_s I_s$ (2.2)

$V_s$ =source voltage

$R_S$=Source Resistance.

In fig 2.2 it is shown in the form of current source.

Therefore $V_O / R_S I_S = - R_f / R_S$ (2.3)

or

$V_O = - R_f I_S$ (2.4)

Since the (-) input terminal is at virtual ground, no current flows through $R_S$ and current is flows through the feedback resistor $R_f$. Thus the output voltage is $V_O = - I_s R_f$. It may be noted that the lowest current that this circuit can measure will depend upon the bias current IB of the OP.AMP.

The circuit is used in sensing current from photodectors and in digital to analog converter applications.

It is common to parallel $R_f$ with a capacitance to reduce high - frequency noise and the possibility of oscillators. The current to voltage converter makes an excellent current measuring instrument since it is ammeter with zero voltage across the meter.

Current to voltage converter is also known as transistance amplifier.

### 2.1.1 RECTIFIER

The fig. 2.3 show the full wave rectifier using op.amp. Equal value resistors are used in the circuit. A positive going input signal reverse biases diode D2 and forward biases diode d1. Thus, effectively the two amplifiers are connected in cascade each having unity gain. Thus output is in phase with the input as well as its magnitude being equal to Vi when the forward biased while D1 is reverse biased. Thus, there are two feedback paths to the inverting input terminal of op.amp A1.

Assuming ideal circuit,

$$I_1 = I_2 = I_3 \qquad (2.5)$$

(or)

$$V_i / R = - V_0 / 3R_2 = V_2 / R \qquad (2.6)$$

But $V_2 = V_3 = V_0 \times 2R / 3R = 2/3\ V_0$ (2.7)

hence substituting we get, $V_0 = - V_i$

But $V_i$ is negative for negative going input hence $V_0$ is again in phase with $V_i$ with same magnitude.

### 2.1.2 MULTIPLEXERS

The multiplexer is a logic circuit that is used to select and route any one of no. of input signals to a single output. Apart from input and output lines, there are some control inputs. By applying the appropriate control inputs one can select any of the inputs to be output on the single

output lines. Since the control inputs make the logic circuit to select one of the many inputs and output, the multiplexer helps to reduce considerably the repetition of similar circuitry in digital systems and thus the overall cost is reduced.

CD4051B is a single 8 channel multiplexers. These are digitally controlled analog switches having low impedance and very low leakage current CD4051B is a single 8 channel multiplexer having 3 binary control input A,B and C and an inhibit input. The three binary signals select 1 of 8 channels to be given and connect one of the 8 inputs as output.

**FEATURES**

1. Wide range of digital and analog signal levels.

   Digital = -3 to 30V

   Analog = upto 20 Vpp

2. Low ON resistance : 125 or (typ) over 15 Vp-p signal output range

   for Vdd-Vee = 15V.

3. High OFF resistance : Channel leakage of I 100 PA (type)

   Vdd - Vee = 18V

4. Logic level conversion for digital addressing signals of 3 to 20v

   (Vdd-Vss = 3 TO 20 V) to switch signals to 20 Vp-p

   (Vdd-Vee = 20V).

5. Matched switch characteristics : (typ) for Vdd-Vee = 150V.

6. Very low qurescent power dissipation under all digital control input and supply conditions, 0.2 low (typ) Vdd-Vss = Vdd-Vee = 10V
7. Binary address decoding on chip.
8. 5,10 and 15V parametric ratings.
9. 100% tested for quiescent current at 20V.
10. Maximum input current of at 100nA at 18 V.
11. Break before make switching eliminates channel overlap.

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| D.C supply voltage range (Vdd) | -0.5 to + 20v |
| Input voltage range, all inputs | -0.5 to Vdd+0.5V |
| DC input current, anyone I/P | ±10mA |
| Operating temp range | -55 to 125°C |
| Storage temp range | -65 to 150°C |

### 2.1.3 ANALOG TO DIGITAL CONVERTER

An A/D converter is used to convert analog signals into digital ones. The digital output are fed to the microprocessor for processing. the most popular method of analog to digital conversion is by successive approximation method. It has an excellent compromise between speed and accuracy. An unknown voltage Vin is compared with a function of reference voltage Vr. For n-bits digital output comparisions is made n times with different function of Vr and value of particular bit is se to 1, if

Vin is greaer that the fraction of V1. The bit is set to 0, if Vin is less than the set fraction Vr. This fraction is given by,

$$\left[\sum_{i=1}^{n} b_i 2^{-i}\right] V_r \qquad (2.8)$$

Where bi is either 0 or 1.

In the first step the unknown voltage is compared with 1/2 Vr. If V > 1/2 Vr the MSB is set to 0. In the next step, Vin is compared with (1/2b1 + 1/4). bi is the value of MSB which has already been determined. Suppose b1=1, the fraction of reference voltage for second comparision becomes (1/2 + 1/4)Vr. If Vin > (1/2 +1/4) Vr the second bit is set to 0. If the MSB is zero th second comparision with (1/2 * 0 ÷ 1/4) Vr. If V is > 1/4 Vr, 2nd bit is set to 1.

If Vin < 1/4 Vr, the 2nd bit set to 0. To obtain the 3rd bit of digital output Vin is compared with (1/2 b1 + 1/4 b2 + 1/8)Vr and so on.

## 2.2 WORKING MODEL

Sensing circuit as shown in fig 2.5 and 2.6 are connected accross each load. The sensing circuit consists basically of a resistor where there would be a large voltage drop, a regulator , normally a zener diode to clip upto 10V, a capacitive filter to remove the ripples and an opto coupler. The signals from the sensing circuit is given to the gate whose out is given to the microprocesser. The microprocessor activates the relay according to the gate signals and the time in clock.

## 2.2.0 RECTIFIER

The rectifier used is a half wave diode rectifier. During positive half cycle of the input ac voltage, the diode D is forward biased (ON) and conducts. While conducting the diode acts as a short circuit so that circuit current flows and hence posive half cycle of the input ac voltage is dropped across the resistance. During the negative input half-cycle, the diode is reverse biased (OFF) and so does not conduct ie., there is no current flow . Hence there is no voltage drop.

equation of input supply voltage

$$V = V_m \sin\theta \qquad (2.9)$$

where $V_m$ = Max value of supply voltage

$$= \sqrt{2}\, V \qquad (2.10)$$

$V$ = RMS value of supply voltage.

## 2.2.1 ZENER DIODE AS A VOLTAGE REGULATOR

Voltage regulation is a measure of a circuit's ability to maintain a constant output voltage even when either input voltage or load current varies. A Zener diode when working in the breakdown region, can serve as a voltage regulator. The Zener diode is reverse connected across Vin. When the potential difference across the diode is greater than V2, it conducts and draws relatively large current through the series resistanceR. The voltage Vout is obtained parallely across the diode.

The total current I passing R equals the sum of diode current and load current

ie $I = I_z = I_L$ (2.11)

Hence, $V_{in} = IR + V_{out} = IR + V_z$ (2.12)

### 2.2.2 CAPACITIVE FILTER

This filter contains a combination of resistor and a capcitor. This filte circuit depends for its operation on the property of a capacitor to charge up (ie store energy) when conducting and to discharge (ie deliver energy ) during non-conduction cycle. when connected across a pulsating de voltage, ittends to smoothen out or filter out voltage pulsations (or ripples).

During positive half cycle of rectified AC output the diode is forward biased and hence turned ON. This allows (to quickly charge up to Vm. During the negative half cycle the capacitor attempts to discharge. The discharging time is usually 100 times more than charging time, so C does not have sufficient time to discharge and so the ripple are removed.

### 2.2.3 OPTO -- COUPLER

The optocoupler basically consists of a light emitting diode (LED) and a photo transistor.

A 5V supply from the sensing circuit is enough for the diode to emit light. This light is sensed by the photo transistor and switches on the transistor.

The main advantage of this optocoupler are

(i). ISOLATION PURPOSE

It isolates the sensing circuit and the microprocessor.

(ii). REMOVES FLUCTUATIONS

The output produced by the photo transistor is exactly 5 volts. There is no fluctuations in this voltage. This 5 volts is given to the AND gate.

### 2.2.4 RELAYS

Static Relays are used in these circuits for controlling purposes. The main advantage of using these static relays instead of electromagnetic relays are

(i). low power consumption

(ii). no-moving contacts. so no problem of contract bounce arcing. contact errosion etc. There is no gravity effect on static relays.

(iii). Restting time and overshoots time are reduced, thereby the selectivity can be improved.

(iv). Repeated operations are possible in static relatys.

(v). Static relay ar compact.

(vi). A variety of characteristics can be obtained with statis relays. Thereby selectivity, stability and adequateness can be achieved.

(vii). Most of the componentes in static relays, including the auxillary relays in the output stage are relatively indifferent to vibrations and shocks.

The signals from the microprocessor are sent to relays via the portC of 8255A. It basically consists of a Freewheeling diode with inductance and a transistor. The excess sudden change of current is stored in the Inductance and when there is signal to the relay the stored current is discharged through the free wheeling diode.

The power supply to each part of the PCB is reffered in 2.7.

The complete circuit diagram is shown in fig. 2.8

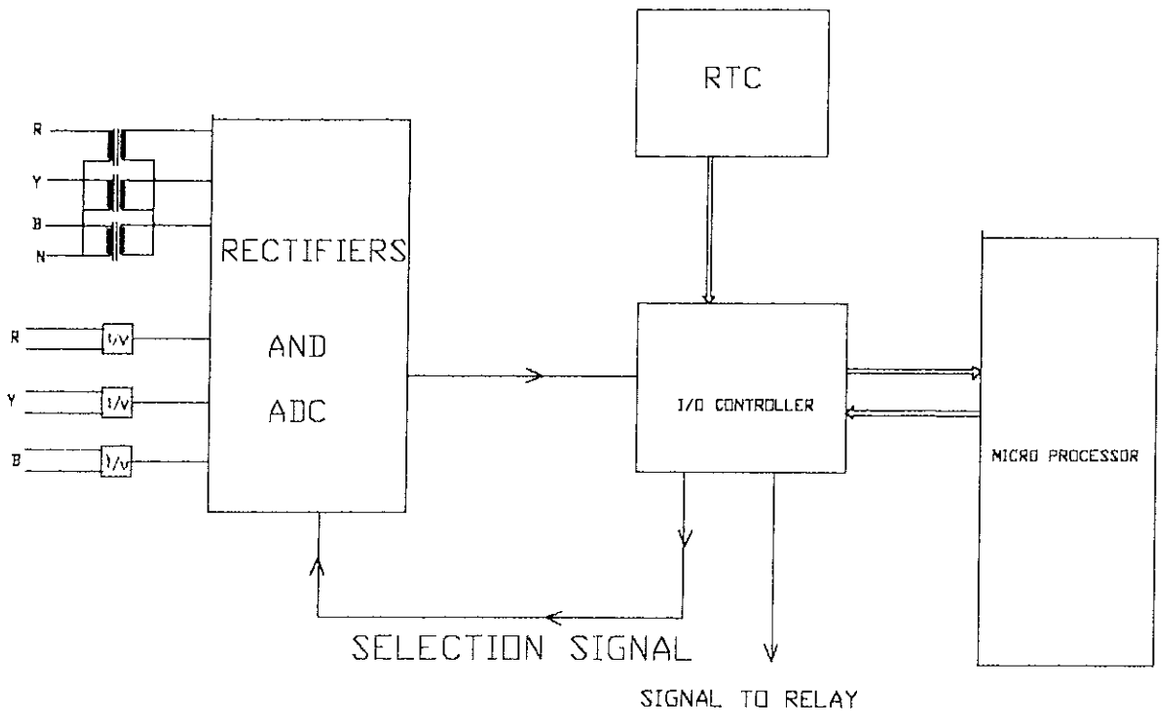



FIG. 2.1. BLOCK DIAGRAM OF MAXIMUM DEMAND MONITOR AND CONTROLLER

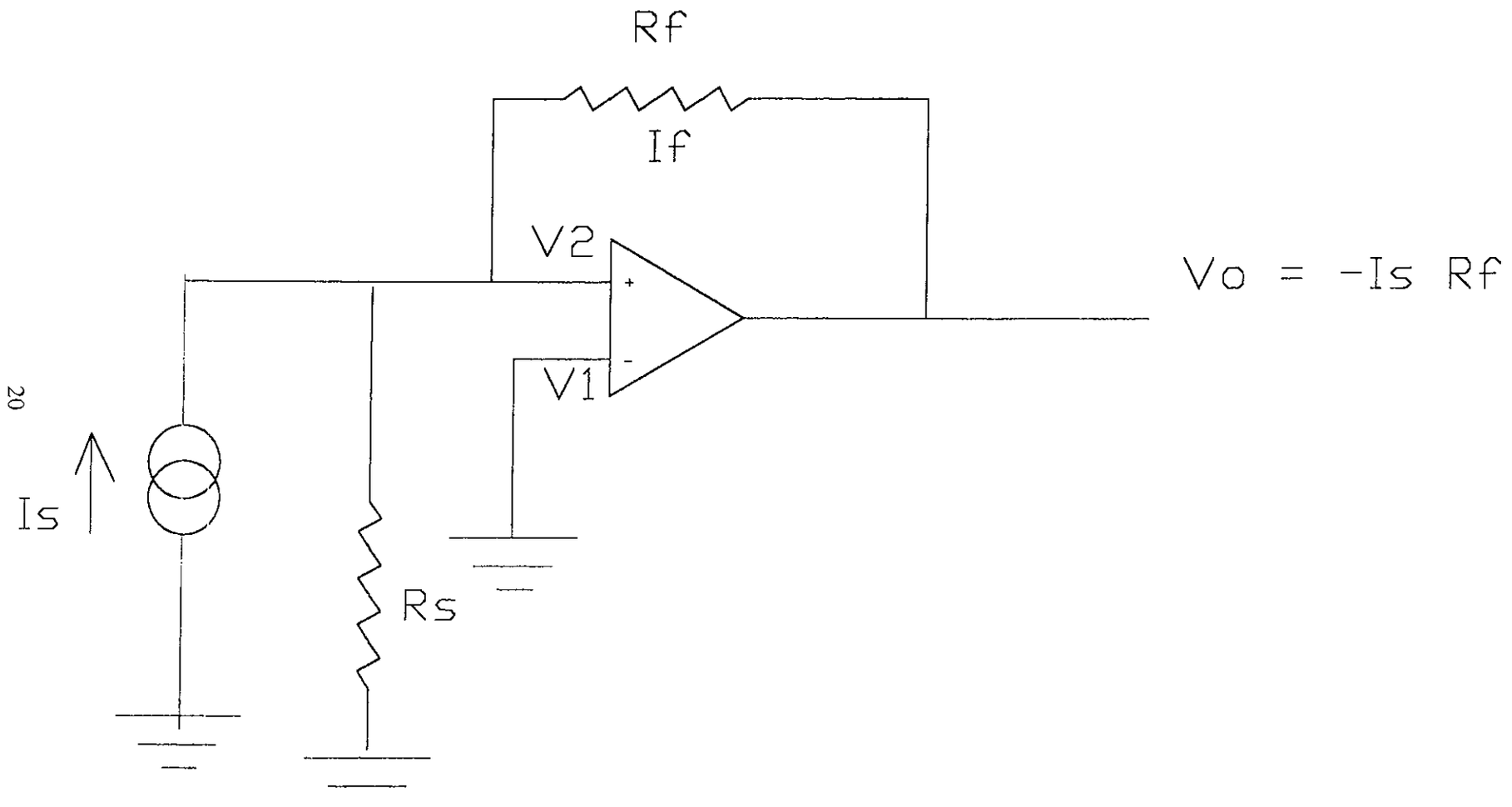



Fig.2.2 CURRENT TO VOLTAGE CONVERTER

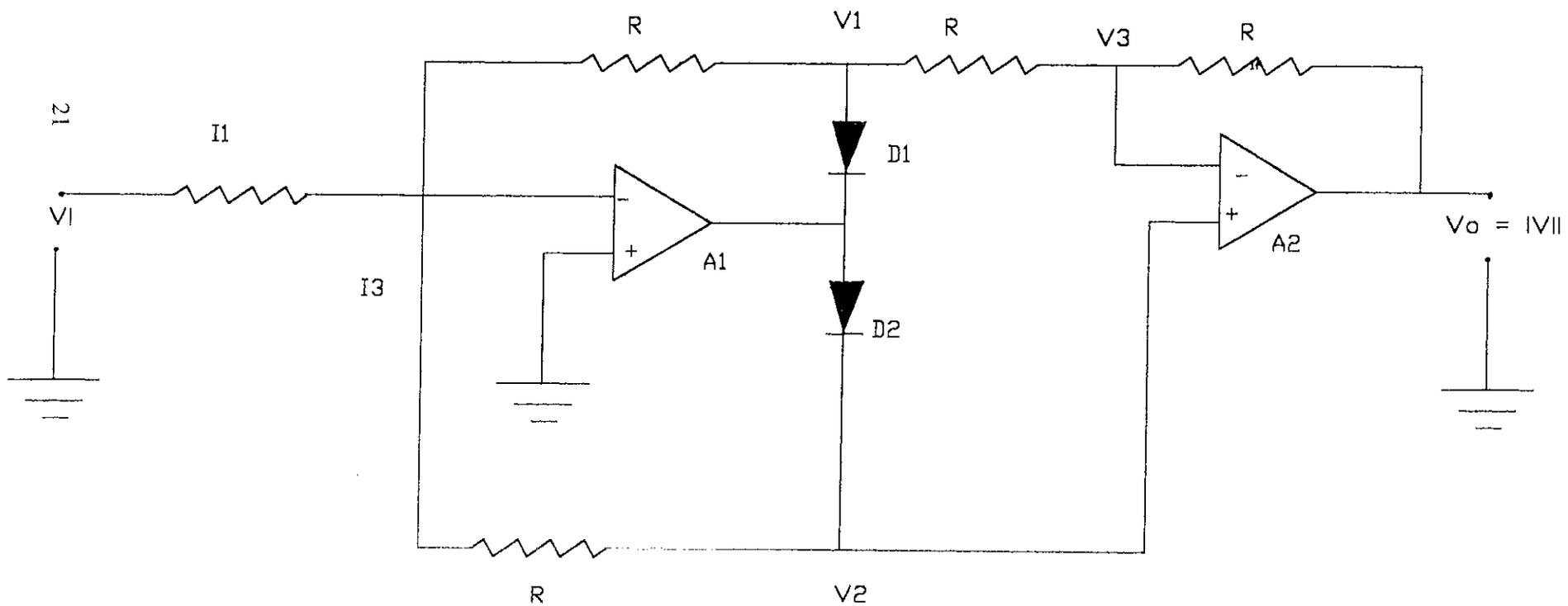



Fig.2.3 FULL WAVE RECTIFIER CIRCUIT USING OP-AMP

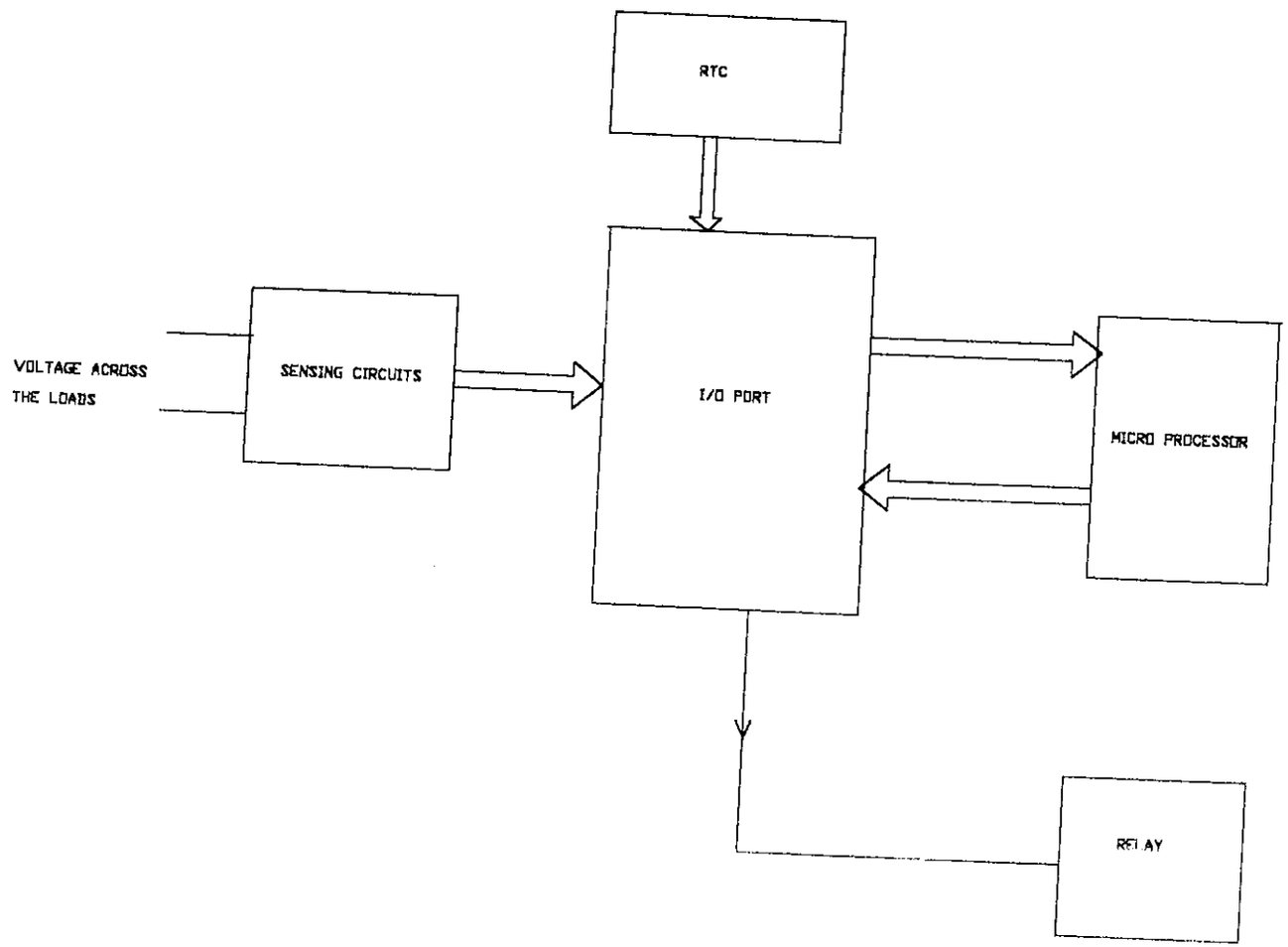



FIG. 2.4.BLOCK DIAGRAM OF MAXIMUM DEMAND MONITOR AND CONTROLLER

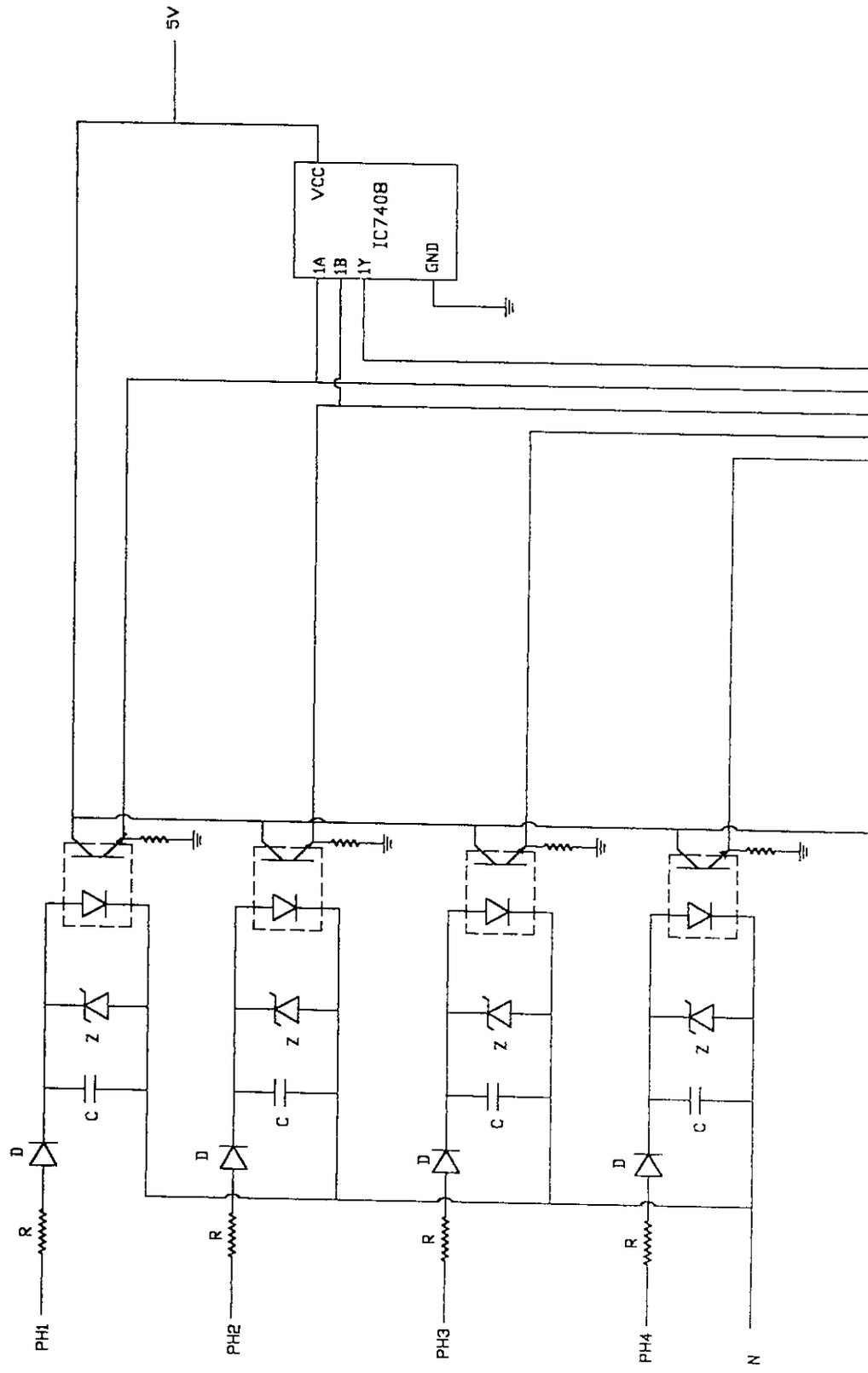



FIG 2.5 HARDWARE OF MAXIMUM DEMAND MONITOR AND CONTROLLER

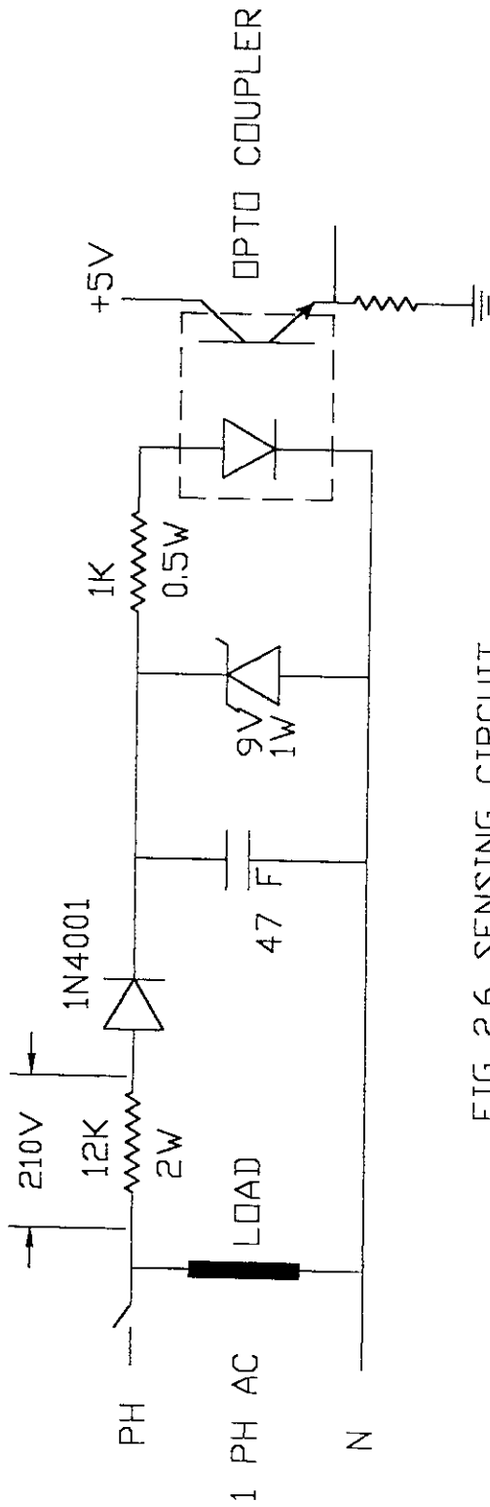



FIG 2.6 SENSING CIRCUIT

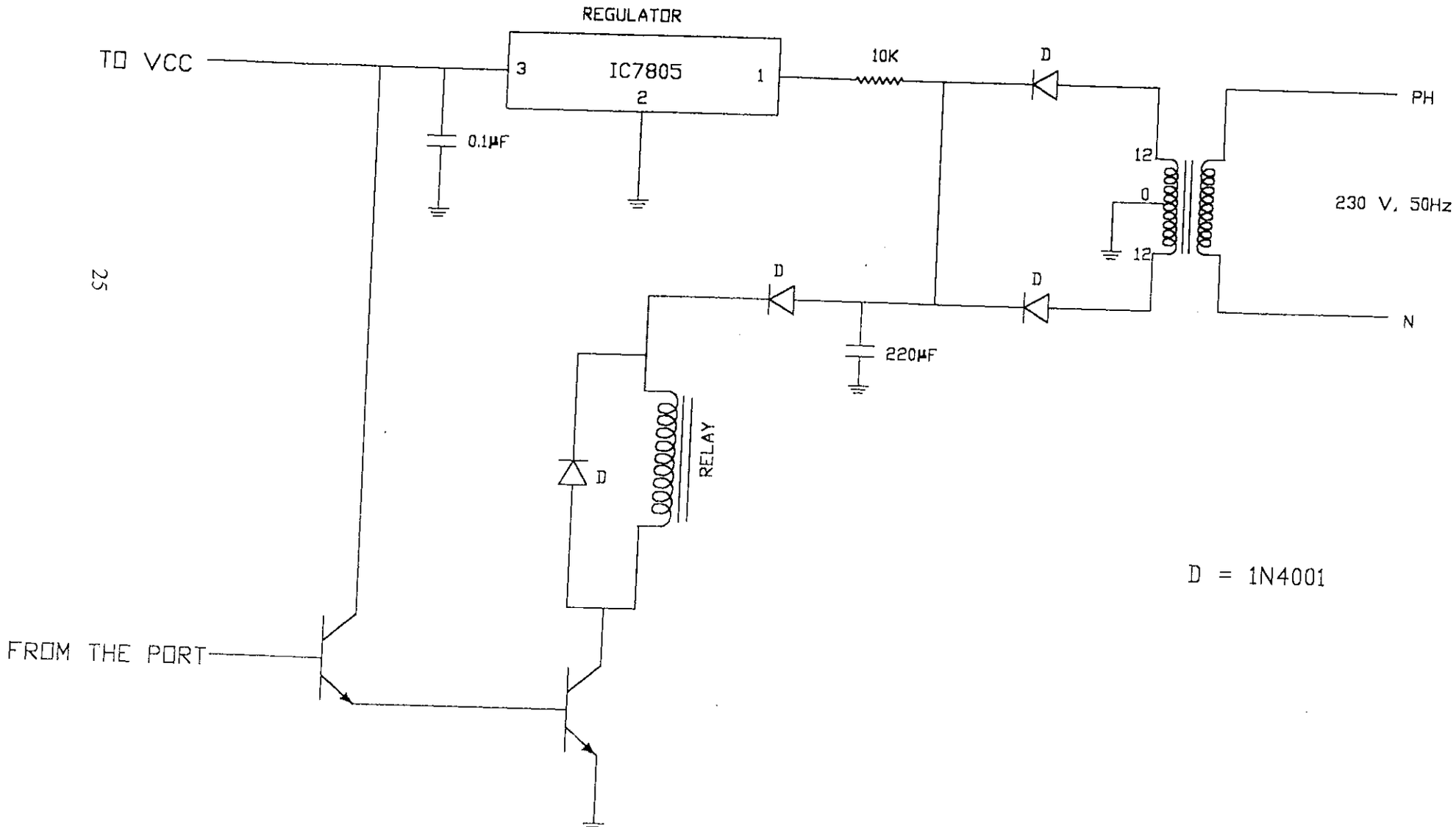



Fig. 2.7 POWER SUPPLY CIRCUIT

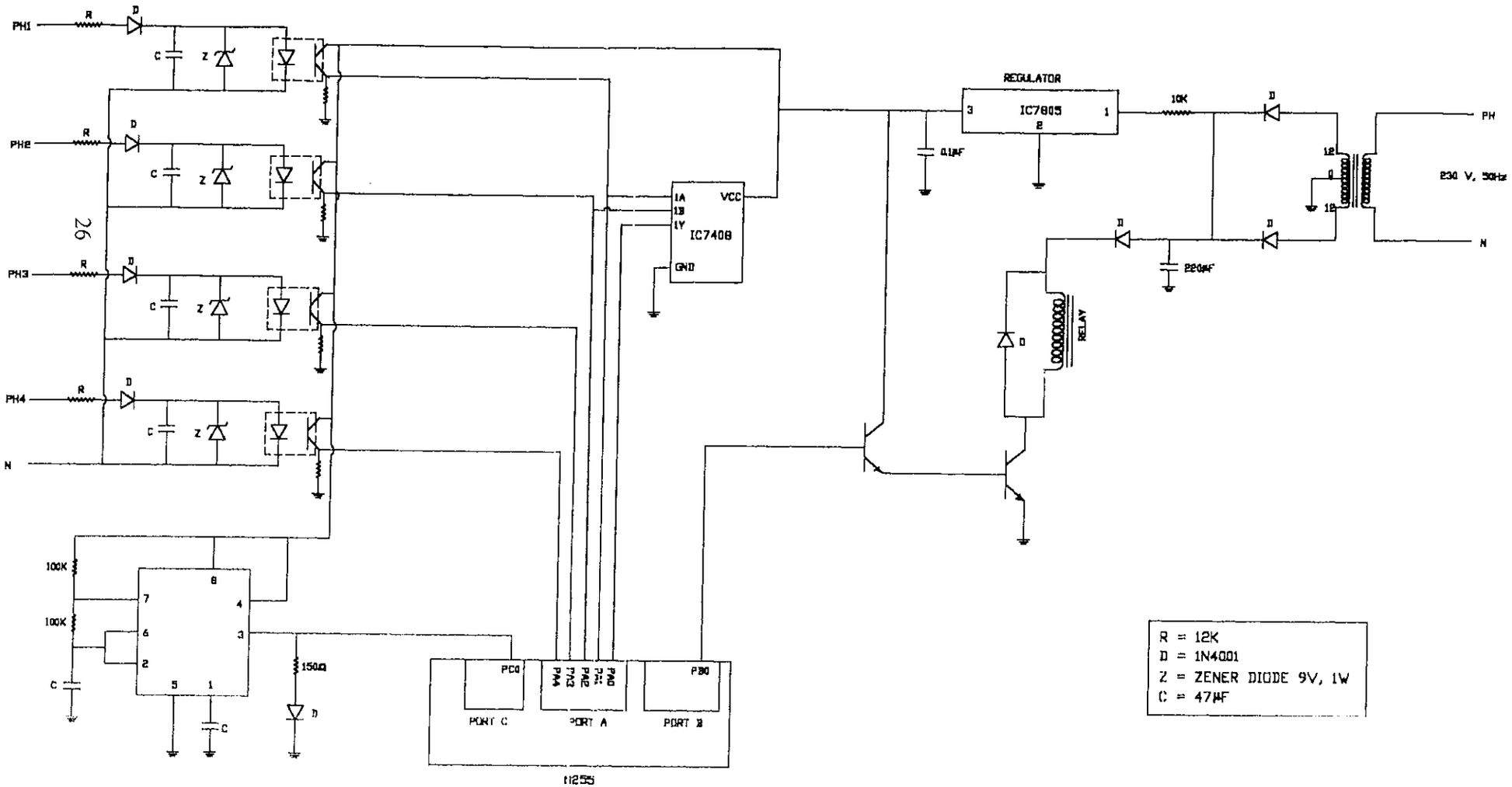
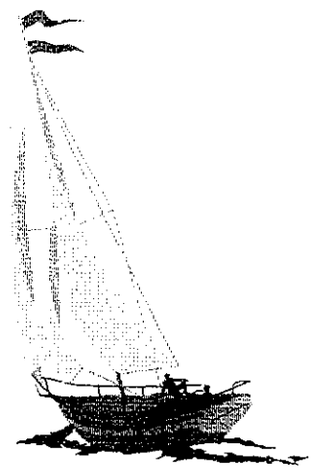



FIG-2.8 COMPLETE CIRCUIT DIAGRAM



# MICROPROCESSOR BASED DESIGN

# CHAPTER-III

# MICROPROCESSOR BASED SYSTEM DESIGN

The microprocessor is a "programmable logic device" and with reference to the field of computer. The term "Microprocessor" refers to the central processing unit of a small computer system. The microprocessor is an electronic integrated circuit of LSI level. Although a microprocessor chip cannot function by itself, the addition of a few memories and I/Odevices make a typical computer system.

## 3.1. MERITS OF A MICROPROCESSOR BASED SYSTEM DESIGN.

### COST OF SAVINGS IN HARDWARE:

A single chip on LSI basis replaces several discrete logic gates resulting in reduction of cost as well as the size of the system

### RELIABILITY:

As the number of gates decreases the probability of malfunctioning decreases. This enhances the system performance.

### FLEXIBILITY:

To modify a system one has to merely reprogram the memory elements without redesigning.

**EXPANDABILITY:**

Additional Interfaces can be added to the system bus and software can be suitably modified to system growth.

## 3.2. MICROPROCESSOR ARCHITECTURE:

The 8085 is and 8 bit microprocessor available as a 40 pin Dual Inline Package (DIP). The data bus is 8-bits wide which implies that 8 bits(1byte) of data can be transferred to or from the 8085 parallel. There are 8 pins which are dedicated to transmit the most significant 8 bits of the memory address. The least significant 8 bits of the address are transmitted on the 8 lines on which data is transmitted over a set of shared lines. This is known as multiplexing. Thus, effectively the 8085 has a 16 bit address transmission capability. This implies that a total of $2^{16}$ (65536) memory locations can be addressed directly by 8085. Each location is a byte as 8 bits of data are transferred iln parallel between the 8085 and the memory. Therefore, the 8085 can directly address 64k(1k=1024bytes)byte of memory.

## 3.3. REGISTERS IN 8085

Inside the 8085 there are several registers which are used during the execution of the program. There is one 8 bit register known as Accumulator. It is used in various arithmetic and logic operations. There are six general prupose 8 bit registers that can be used by a programmer

for a variety of applications. These registers are B,C,D,E,H and L. They can be used individually (for 8 bit data ) or in pairs (for 10 bit address). There is a 16 bit register which is used by the 8085 to keep track of the address of the instruction (in the memory) that has to be executed next, this register is called the program counter. The contents of the program counter are automatically updated by the 8085 during the execution of an instruction. So that at the end of execution of this instruction in the memory the program counter points to the memory address from which the next byte is to be fetched. The stack pointer is also a 16 bit register used as a memory pointer. It points to a memory location in R/W memory, called the stack. The beginning of the stack is defined by loading a 16 bit address in the stack pointer.

### 3.4 FLAGS

The Arithmetic logic unit includes five flip flops that are set or reset according to data conditions in the accumulator and other registers. The microprocessor uses them to perform the third operation: namely testing for data conditions.

For example, after an addition of two numbers if the number in the accumulator is larger than 8 bits, the flip flop that isused to indicate a carry called the carry(cy)flag,is set to one. When an arthimatic operation results in zero, the flip flop called the zero(z) flag is set to one. The 8085 has five flags to indicate five different types of data conditions . They are

zero(z) , carry(cy), signs(s), parity(p) and auxillary carry(ac) flags. There are address and data bus through which communication between different units is done. Interrupts control may be utilised for interrupt subroutines.

### 3.5 PERIPHERAL OR EXTERNALLY INITIATED OPERATIONS.

External devices (or signals) can initiate the following operations for which individual pins on the microprocessor chip are assigned: Reset,Interrupt, Ready, Hold.

**RESET**: When the reset is activated, all internal operations are suspended and the program counter is cleared (it holds 0000H). Now the program execution can again begin at the zero memory address.

**INTERRUPT**: The microprocessor can be interrupted from the normal execution of the instruction and asked to execute some other instructions called service routine. The microprocessor resumes its operation after completing the service rountine.

**READY**: The 8085 has a pin called ready if the signal at this ready pin is low, the microprocessor enters into the wait state. This signal is used primarily synchronize slower peripherals with the microprocessors.

**HOLD**: When the HOLD pin is activated bya an external signal, the microprocessor relinquishes control of buses and allows the external peripheral to use them. For example, the HOLD signal is used in direct memory access (DMA) data transfer.

Microprocessor based systems needs a sequence of instructions i.e.,the program which is fed to the microprocessor based system for an effective operation. A sequence of instructions designed to perform a particular task is known as program. A set of program written for a microprocessor based system is known as software of that system. Before the microprocessor can be made to perform a task, it has to be programmed and stored in a semiconductor memory that is accessible to the microprocessor based system design involves interfacing of the processor with one or more peripheral devices for the purpose of communication with external system. The MPU communicates with only one peripheral at a time by enabling tyhe peripheral through its control signal. The output device latches and displays data.

### 3.6 THE 8255A PROGRAMMABLE PERIPHERAL INTERFACE

The 8255 is widely used, programmable parallel I/O devices. It can be programmed to transfer data under various conditions from simple I/O to interrupt I/O It is flexible versatile and economical.

The 8255A has two 8 bit ports (A and B) two 4 bits ports (Cu and Cl), the data bus buffer and control logic. Port C performs

functions similar to that of the status register in addition to providing handshake signals. The interfacing port is reffered in fig.3.1.

### 3.6 CONTROL LOGIC

The control section has six lines.

**READ :** This control signal enables the read operation, when the signal is low, the MPU reads from a selected I/O port of the 8255A.

**WRITE:** This control signal enables the write operation when the signal goes low, the MPU writes into a selected I/O port or the control regilster.

RESET(reset): This is an active high signal; it clears the cdontrol register and sets all ports in the input mode.

**$\overline{CS}$, $A_0$, and $A_1$:** These are device select signals. CS is connected to a decoded address and $A_0$ and $A_1$ are generally connected to MPU address lines $A_0$ and $A_1$ respectively.

The $\overline{CS}$ signal is the master chip select, and $A_0$ and $A_1$ specify one of the I/O ports or the control register as given below:

| $\overline{CS}$ | $A_1$ | $A_0$ | SELECTED |
|---|---|---|---|
| 0 | 0 | 0 | Port A |
| 0 | 0 | 1 | Port B |
| 0 | 1 | 0 | Port C |
| 0 | 1 | 1 | Control register |
| 1 | X | X | 8255A is not selected |

### 3.62 CONTROL WORD

Control word specify an I/O function for eachport. The control register can be accessed to write a control word when $A_0$ and$A_1$ are logic 1. The register is not accessible for a read operation.

Bit $D_7$ of the control register specifies either the I/O function or the bit set/reset function. If bit $D_7$ =1 , bits $D_6$ - $D_0$ determines I/O functions in varius modes. If bit $D_7$ = 0 portC operates in the bit set/reset (BSR) mode. The BSR control word does not affect the functions of ports A and B.

### 3.7 OPERATING MODES OF 8255

There are 3 major modes of operation of 8255 namely mode0, mode1 and mode2 which comes under the major category of I/O mode

**MODE 0:** Simple output or input:

In this mode, port A and port B are used as two simple 8 bit I/O ports and port C as two 4 bit ports. Each port (or half port, in case of c) can be programmed to function as simply an input port or an output port.

### 3.7.1 THE INPUT/OUTPUT FEATURES IN MODE 0 ARE AS FOLLOWS:

1. Outputs are latched
2. Inputs are not latched
3. Ports do not have handshake or interrupt capability.

**MODE 1**: Input or output with handshake:

In mode1, handshake signals are exchanged between the MPU and perpherals prior to data transfer, the features of this mode include the following:

1. Two ports (A and B) function as 8 bit I/O ports. They can be configured either as input or output ports.
2. Each port uses three lines from port c as handshake signals. The remaining two lines of port ca can be used for simple I/O functions.
3. Input and output data are latched.
4. Interrupt logic is supported.

In the 8255A, the specific lines from port c used for handshake signals vary according to the I/O function of a port.

### 3.7.2 MODE2 : BIDIRECTIONAL DATA TRANSFER

This mode is used primarily in applications such as data transfer between two computers or floppy disk controller interface:

1. Port A is configured as the bidirectional port.
2. Port B either in Mode 0 and Mode 1.
3. Port A uses five signals from port C as handshake signals for data transfer.
4. Both inputs and outputs are latched.

5. The 5 bit control port is used for control and status of the 8 bit bidirectional port

To communicate with peripherals through 8255, 3 steps are necessary.

1. Determine the port by chip select logic and address lines $A_0$ and $A_1$
2. Write a control word in the control register.
3. Write I/O instructions to communicate with peripherals through ports A,B and C

### 3.8 REAL TIME CLOCK CIRCUIT:

This circuit is necessary for the microprocessor to keep in pace with time inorder to findout the peak hours. In real time clock, 555 timer is used.

The 555 timer is a highly stable device for generating accurate time delay or oscillation. A single 555 timer can provide time delay ranging from microseconds to hours. In our project 555 timer are used to produce a time delay of 6 seconds.

### 3.8.1 DESCRIPTION OF FUNCTIONAL DIAGRAM

Fig (a) gives the pin diagram and Fig(b) gives the functional diagram for 555IC timer. Referring to fig(b) three 5 kiloohms resistors act as voltage divider, providing bias voltage of (2/3) Vcc to the upper comparator(uc) and 1/3 Vcc to the lower comparator (Lc), where Vcc is

the supply voltage, since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing inerval . It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin5) and ground to by-pass noise or ripple from the supply.

In the standby (stable) state, the output Q of the control flip flop(FF) is high. This makes the output low because of power amplifier which is basically an inverter. A negativae going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e.Vcc/3). At the negative going edge of the trigger, as the trigger passes through (Vcc/3), the output of the lower comparator goes high and sets the FF($Q = 1$, $\overline{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3)Vcc the output of the upper comparator goes High and resets the FF($Q = 0$, $\overline{Q} = 1$).

The reset (pin4) input provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 v . When this reset is not used, it is returned to Vcc. The transistor Q2 serves as a buffer to isolate the reset input from the FF and transistor Q1 The Q2 transistor is driven by an internal reference voltage Vref obtained from Vcc.

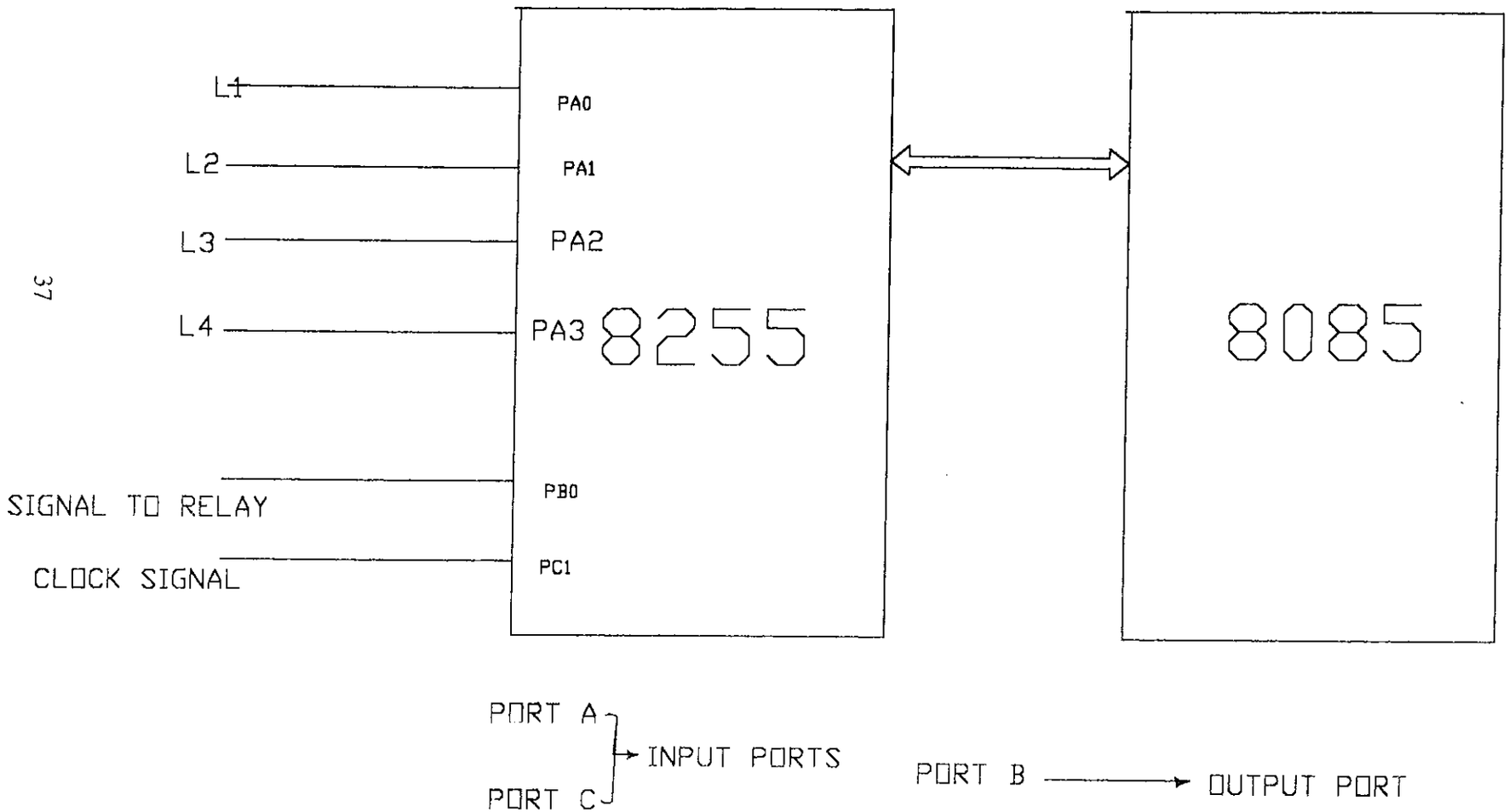
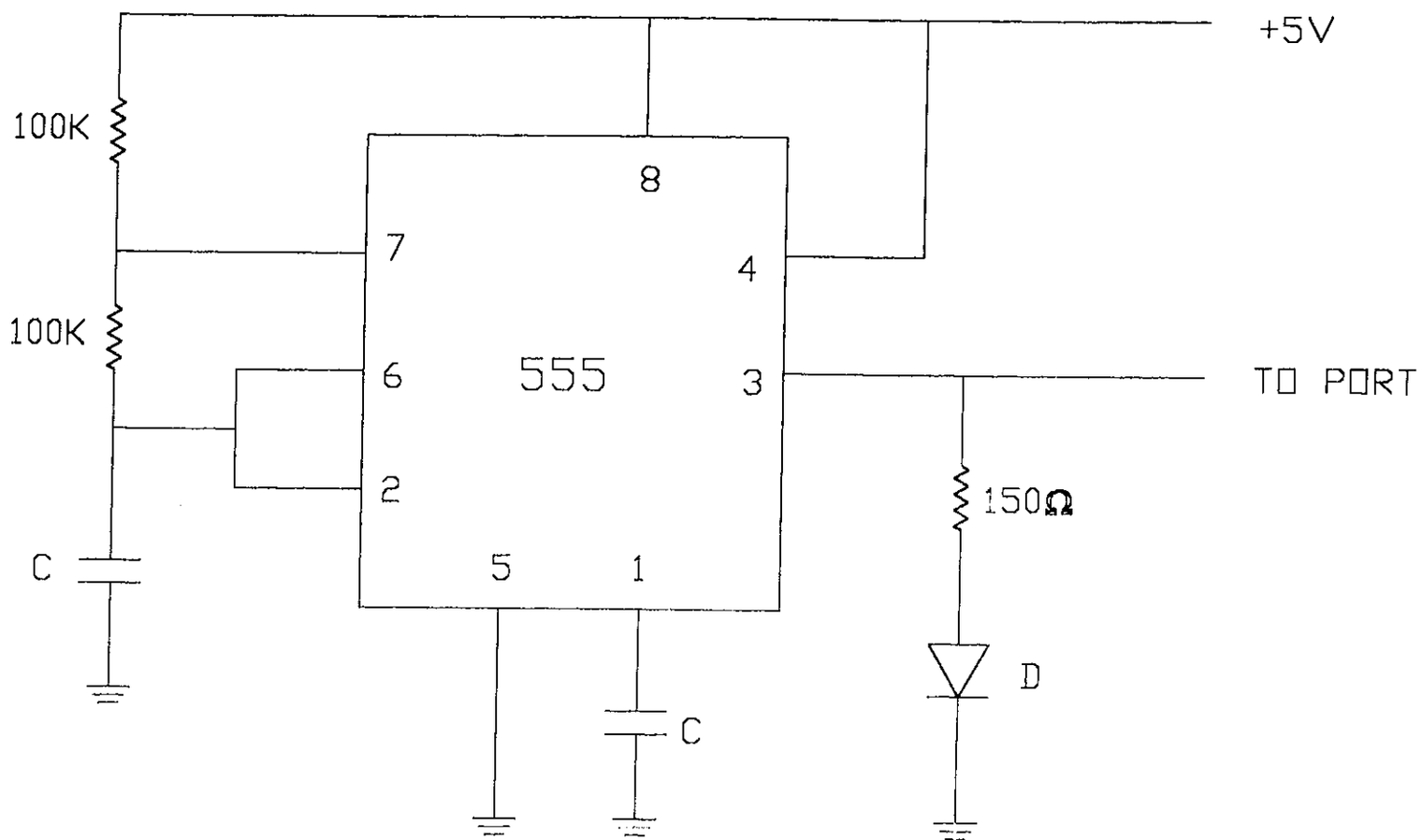



FIG. 3.1. PERIPHERAL INTERFACING OF 8255 WITH 8085




MONO STABLE MODE

FIG-3.2 REAL TIME CLOCK

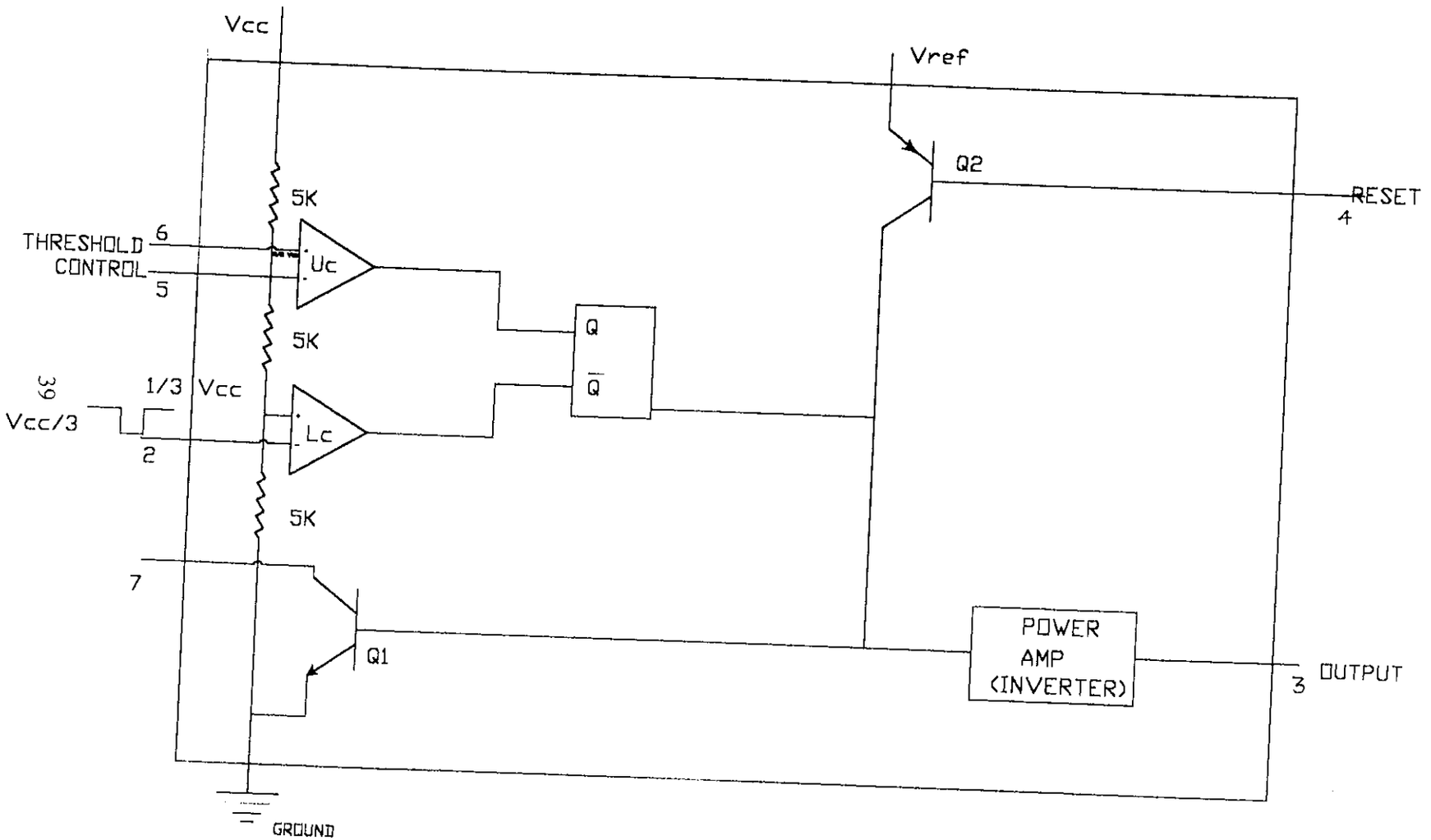
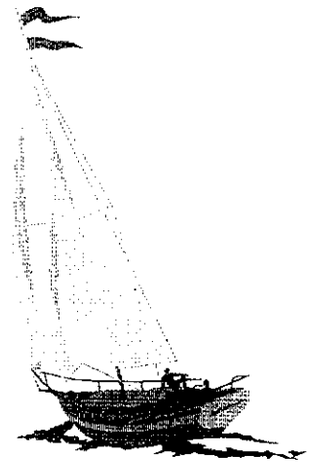



Fig. 3.3 Functional Diagram of 555 Timer



# SOFTWARE DEVELOPEMENT

# CHAPTER IV

# SOFTWARE DEVELOPEMENT

Microprocessor based maximum demand monitor and controller contains sensing of the peak time ie., timer calculatons, power on load, and programs to operate the relay conditions.

This software contains one main program and two subprograms. The subprograms are as follows:

i. Timing Calculation

ii. Power Measurement

## 4.1 MAIN PROGRAM

### ALGORITHM FOR MAIN PROGRAM

STEP 1 : Fixing the control word for selecting input ports and output ports.

STEP 2 : Call the subprogram of CLOCK

STEP 3 : Call the subprogram of CLOCK CHECK

STEP 4 : Call the subprogram of CALCULATION

STEP 5 : If the time is not in peak hour made relay OFF else to STEP 6.

STEP 6 : If gate signal is ZERO made relay OFF else ON the relay.

STEP 7 : Go to STEP 2:

The various steps involved in monitoring the load and controlling it is shown in the flow chart fig 4.1.

## SUBPROGRAMS

## 4.2 ALGORITHM FOR SUBPROGRAMS

### 4.2.1 TIMER CALCULATION

In the timer calculation in order to know the present time a timer called 555 timer is introduced. This timer is designed in such a way tht it sends pulses every 6 seconds. This given as an input through port C. The port C input is continuously checked and the relevant seconds value is incremented. Later after 60 seconds the seconds value is cleared and the minute value is incremented and this again happens in the case of hours. Thus the timer program acts as clock which is useful in carefully monitoring the peak hours.

**CLOCK**

STEP 1: INPUT PORT C

STEP 2 : If clock signal is high add 10 with SECOND else RET.

**CLOCK CHECKING**

STEP 1 : If second = 60 clear it and increment minute else RET.

STEP 2 : If minute = 60 clear it and increment HOUR else RET.

STEP 3 : If Hour = 24 clear it and RET else RET.

The flowchart for clock checking is refferred in fig 4.2.

### 4.2.2 POWER CALCULATION

STEP 1 : INPUT PORT A.

STEP 2: Calculate the power consumption of normal loads.

STEP 3 : If the excessload connected with EB line take it for power calculation.

STEP 4: RET.

The flow chart for calculation is reffered in fig. 4.3.

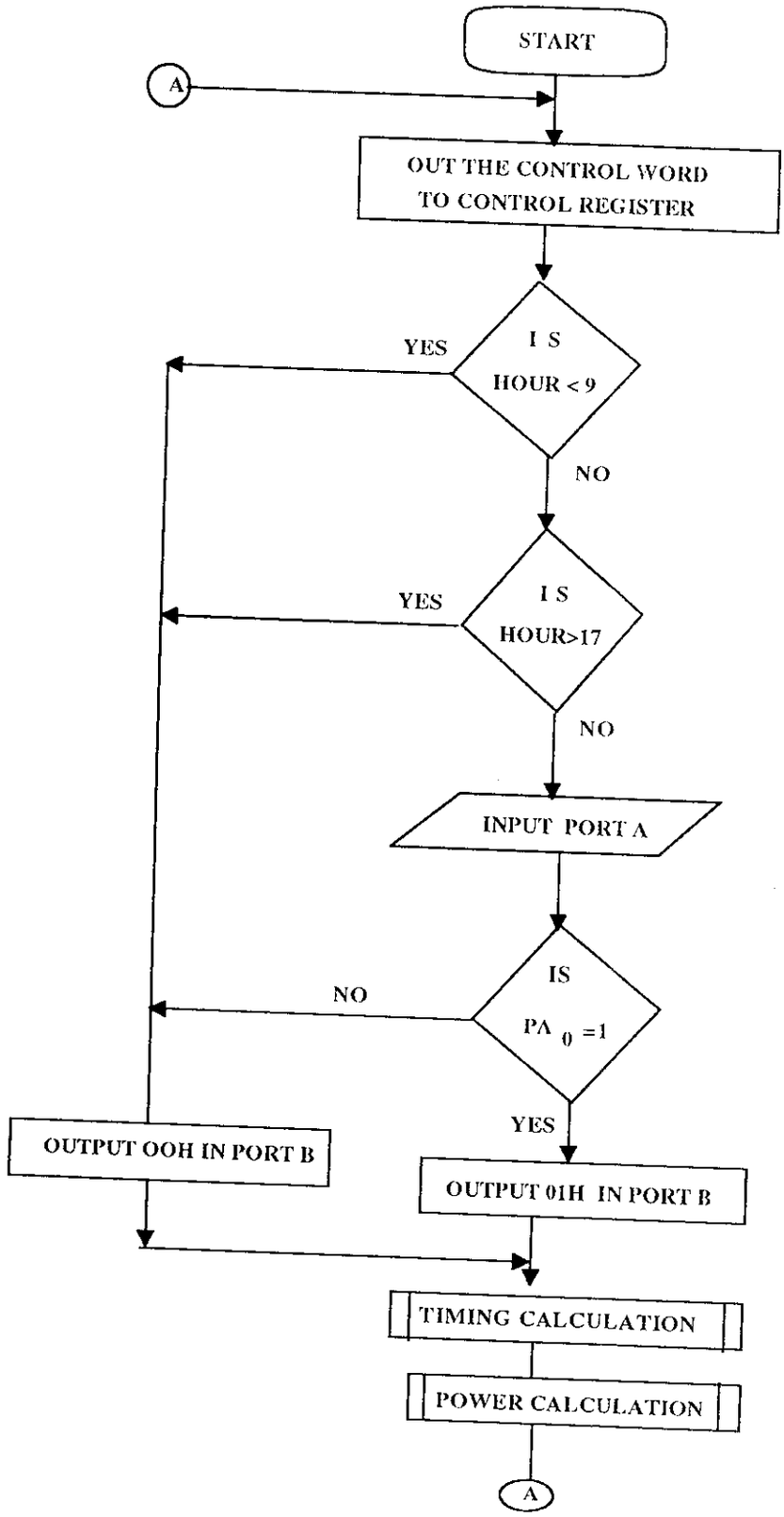
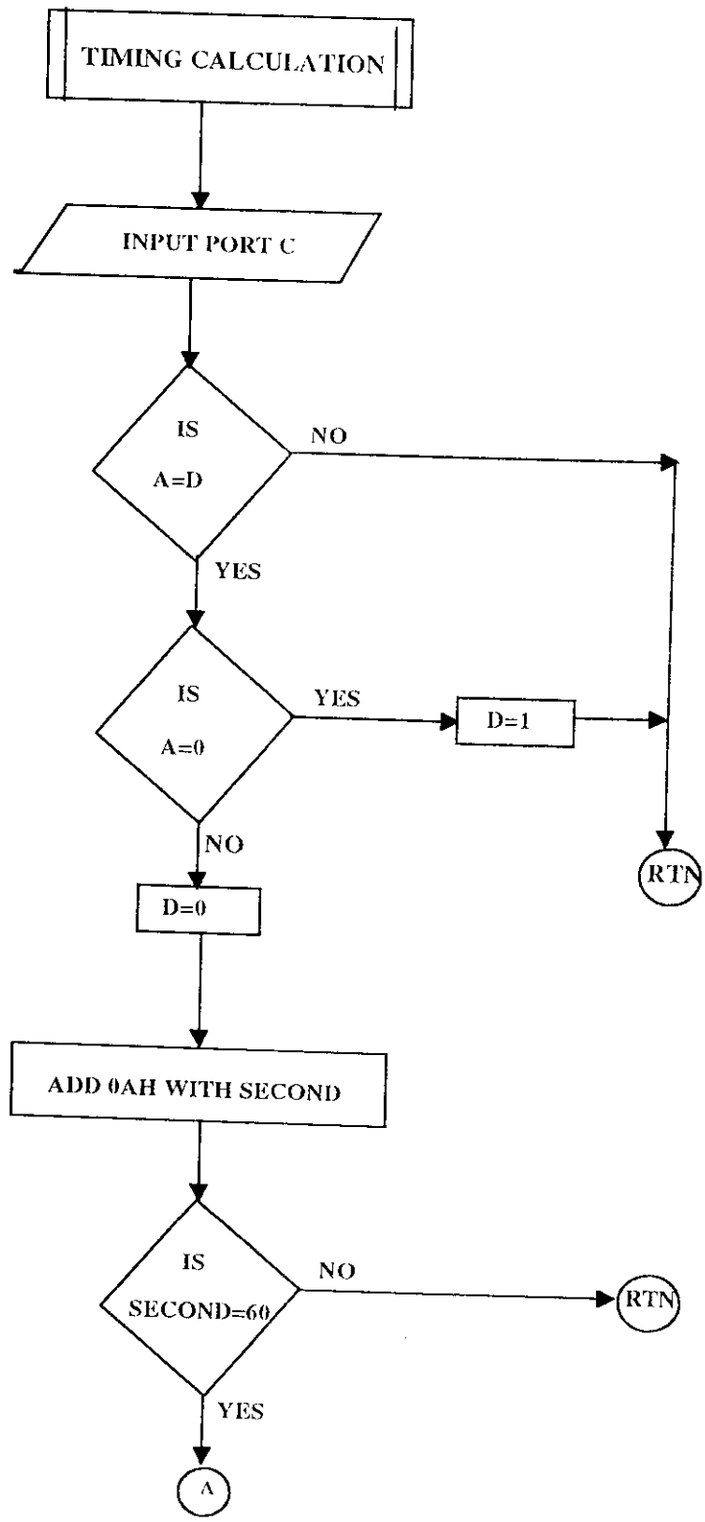



FIG.4.1 MAIN PROGRAM


TIMING CALCULATION
INPUT PORT C
IS
A=D
NO
YES
IS
A=0
YES
D=1
RTN
NO
D=0
ADD 0AH WITH SECOND
IS
SECOND=60
NO
RTN
YES
A

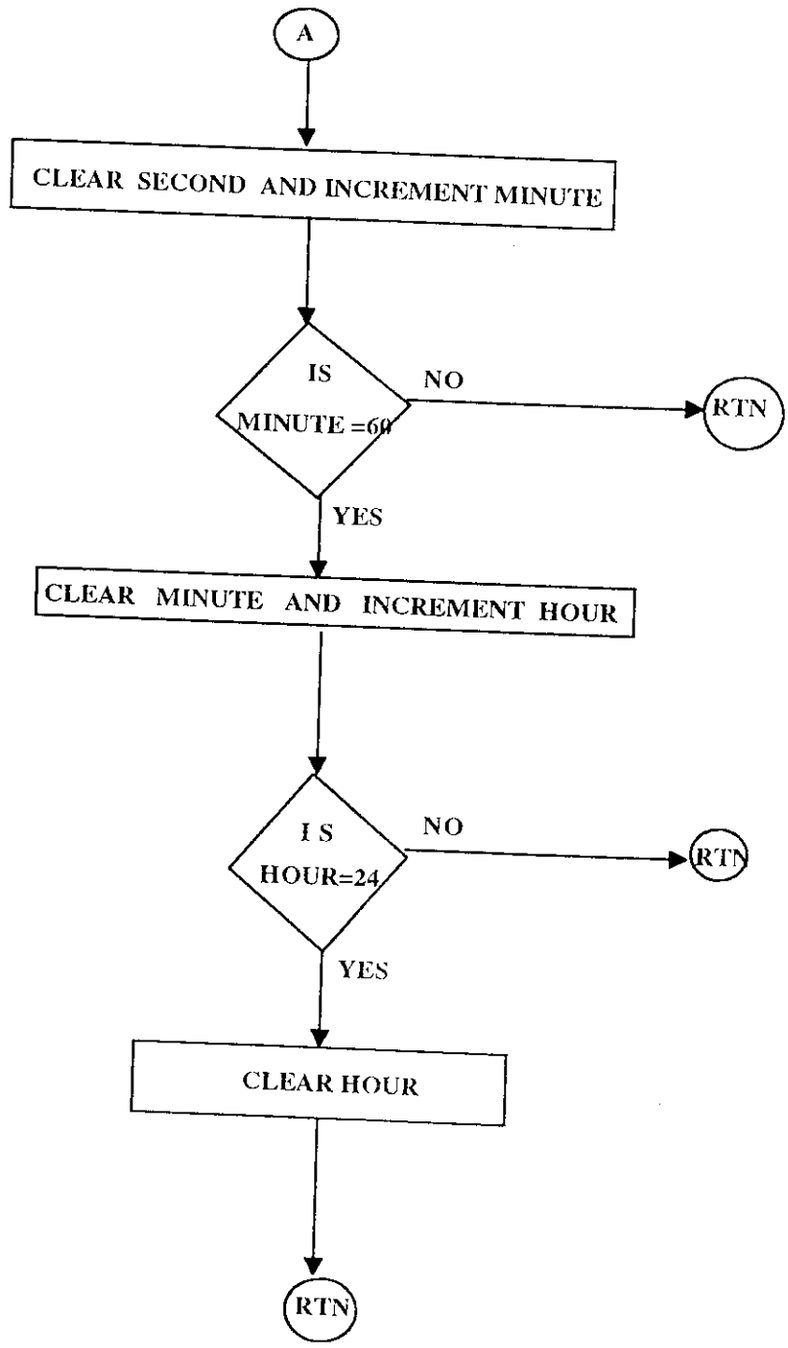
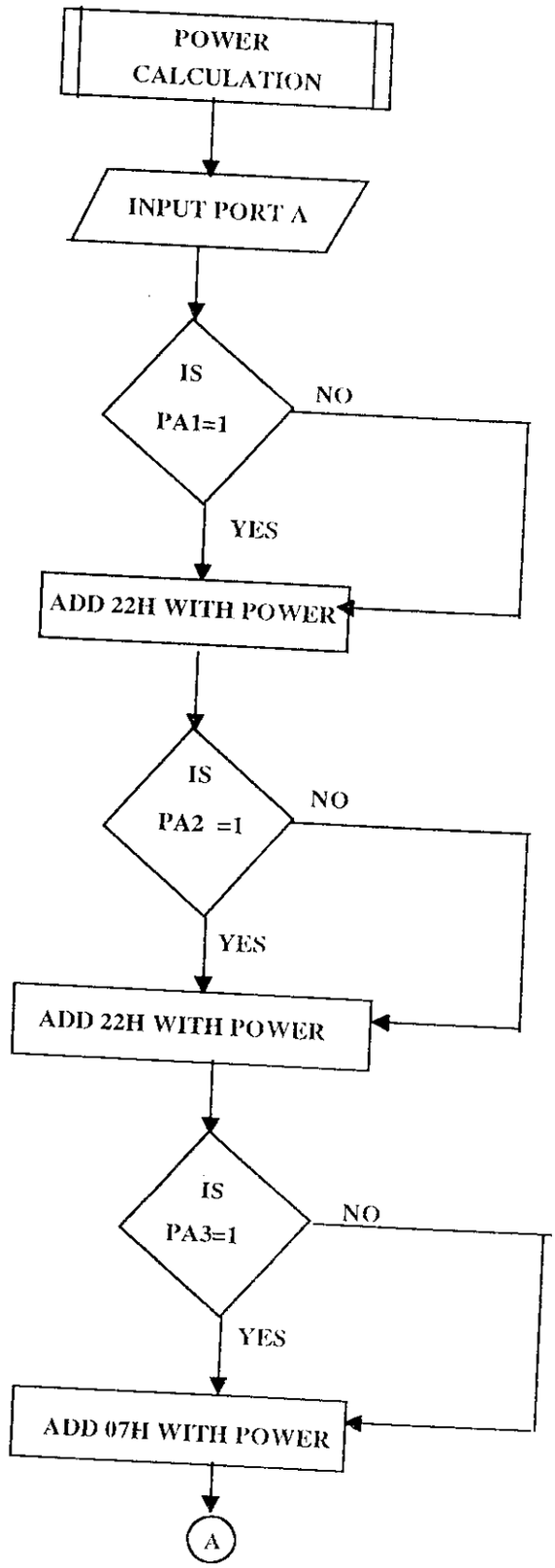



FIG. 4.2 TIMING CALCULATION


POWER CALCULATION
INPUT PORT A
IS PA1=1
NO
YES
ADD 22H WITH POWER
IS PA2 =1
NO
YES
ADD 22H WITH POWER
IS PA3=1
NO
YES
ADD 07H WITH POWER
A

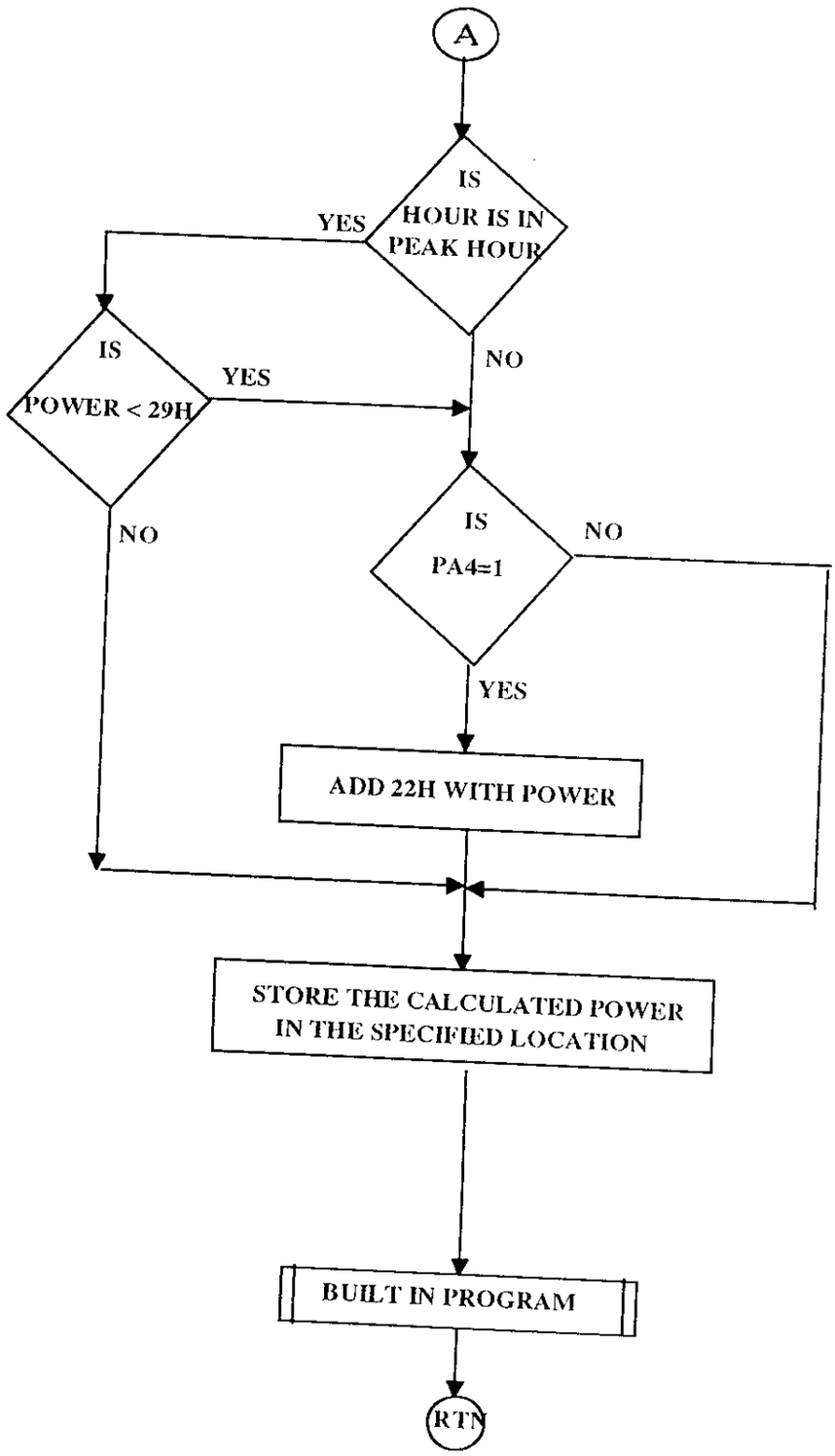



FIG.4.3 POWER CALCULATION

**MAIN PROGRAM**

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8400 | 16 | | MVI | D,01H |
| 8401 | 01 | | | |
| 8402 | 3E | | MVI | A,99H |
| 8403 | 99 | | | |
| 8404 | D3 | | OUT | CONTROL |
| 8405 | 03 | | | REGISTER |
| 8406 | CD | RETURN | CALL | CLOCK |
| 8407 | 00 | | | |
| 8408 | 83 | | | |
| 8409 | CD | | CALL | CLOCK |
| 840A | 00 | | | CHECKING |
| 840B | 85 | | | |
| 840C | CD | | CALL | POWER |
| 840D | 00 | | | CAL. |
| 840E | 89 | | | |
| 840F | 3A | | LDA | 8600H |
| 8410 | 00 | | | |

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8411 | 86 | | | |
| 8412 | FE | | CPI | 09H |
| 8413 | 09 | | | |
| 8414 | DA | | JC | OFF |
| 8415 | 00 | | | RELAY |
| 8416 | 82 | | | |
| 8417 | FE | | CPI | 17H |
| 8418 | 17 | | | |
| 8419 | D2 | | JNC | OFF |
| 841A | 00 | | | RELAY |
| 841B | 82 | | | |
| 841C | DB | | IN | PORT A |
| 841D | 00 | | | |
| 841E | E6 | | ANI | 01H |
| 841F | 01 | | | |
| 8420 | CA | | JZ | OFF |
| 8421 | 00 | | | RELAY |
| 8422 | 82 | | | |
| 8423 | CD | | CALL | ON RELAY |
| 8424 | 50 | | | |
| 8425 | 82 | | | |
| 8426 | C3 | BACK | JMP | RETURN |
| 8427 | 06 | | | |
| 8428 | 84 | | | |

## SUB PROGRAMS

### OFF RELAY

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8200 | 3E | | MVI | A,00H |
| 8201 | 00 | | | |
| 8202 | D3 | | OUT | PORT B |
| 8203 | 01 | | | |
| 8204 | C3 | | JMP | BACK |
| 8205 | 26 | | | |
| 8206 | 84 | | | |

### ON RELAY

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8250 | 3E | | MVI | A,FFH |
| 8251 | FF | | | |
| 8252 | D3 | | OUT | PORT B |
| 8253 | 01 | | | |
| 8254 | C9 | | RET | |

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8300 | DB | | IN | PORT C |
| 8301 | 02 | | | |
| 8302 | E6 | | ANI | 01H |
| 8303 | 01 | | | |
| 8304 | BA | | CPI | D |
| 8305 | C0 | | RNZ | |
| 8306 | FE | | CPI | A,00H |
| 8307 | 00 | | | |
| 8308 | C2 | | JNZ | JUMP |
| 8309 | 0E | | | |
| 830A | 83 | | | |
| 830B | 16 | | MVI | D,01H |
| 830C | 01 | | | |
| 830D | C9 | | RET | |
| 830E | 16 | JUMP | MVI | D,00H |
| 830F | 00 | | | |
| 8310 | 3A | | LDA | 8602H |
| 8311 | 02 | | | |
| 8312 | 86 | | | |
| 8313 | C6 | | ADI | 0AH |
| 8314 | 0A | | | |
| 8315 | 27 | | DAA | |
| 8316 | 32 | | STA | 8602H |
| 8317 | 02 | | | |
| 8318 | 86 | | | |
| 8319 | C9 | | RET | |

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8500 | 3A | | LDA | 8602H |
| 8501 | 02 | | | |
| 8502 | 86 | | | |
| 8503 | FE | | CPI | 60H |
| 8504 | 60 | | | |
| 8505 | C0 | | RNZ | |
| 8506 | 3E | | MVI | A,00H |
| 8507 | 00 | | | |
| 8508 | 32 | | STA | 8602H |
| 8509 | 02 | | | |
| 850A | 86 | | | |
| 850B | 3A | | LDA | 8601H |
| 850C | 01 | | | |
| 850D | 86 | | | |
| 850E | 3C | | INR | A |
| 850F | 27 | | DAA | |
| 8510 | 32 | | STA | 8601H |
| 8511 | 01 | | | |
| 8512 | 86 | | | |
| 8513 | FE | | CPI | 60H |
| 8514 | 60 | | | |
| 8515 | C0 | | RNZ | |
| 8516 | 3E | | MVI | A,00H |
| 8517 | 00 | | | |
| 8518 | 32 | | STA | 8601H |
| 8519 | 01 | | | |

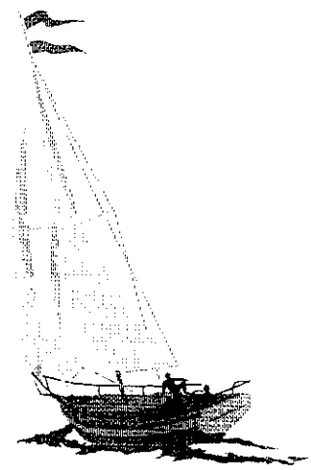
| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 851A | 86 | | | |
| 851B | 3A | | LDA | 8600H |
| 851C | 00 | | | |
| 851D | 86 | | | |
| 851E | 3C | | INR | A |
| 851F | 27 | | DAA | |
| 8520 | 32 | | STA | 8600H |
| 8521 | 00 | | | |
| 8522 | 86 | | | |
| 8523 | FE | | CPI | 24H |
| 8524 | 24 | | | |
| 8525 | C0 | | RNZ | |
| 8526 | 3E | | MVI | A,00H |
| 8527 | 00 | | | |
| 8528 | 32 | | STA | 8600H |
| 8529 | 00 | | | |
| 852A | 86 | | | |
| 852B | C9 | | RET | |

## POWER CALCULATION

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8900 | 06 | | MVI | B,00H |
| 8901 | 00 | | | |
| 8902 | DB | | IN | PORT A |
| 8903 | 00 | | | |
| 8904 | 4F | | MOV | C,A |
| 8905 | E6 | | ANI | 02H |
| 8906 | 02 | | | |
| 8907 | CA | | JZ | SKIP 1 |
| 8908 | 0F | | | |
| 8909 | 89 | | | |
| 890A | 78 | | MOV | A,B |
| 890B | C6 | | ADI | 22H |
| 890C | 22 | | | |
| 890D | 27 | | DAA | |
| 890E | 47 | | MOV | B,A |
| 890F | 79 | SKIP 1 | MOV | A,C |
| 8910 | E6 | | ANI | 04H |
| 8911 | 04 | | | |
| 8912 | CA | | JZ | SKIP 2 |
| 8913 | 1A | | | |
| 8914 | 89 | | | |
| 8915 | 78 | | MOV | A,B |
| 8916 | C6 | | ADI | 07H |
| 8917 | 07 | | | |
| 8918 | 27 | | DAA | |
| 8919 | 47 | | MOV | B,A |

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 891A | 79 | SKIP 2 | MOV | A,C |
| 891B | E6 | | ANI | 08H |
| 891C | 08 | | | |
| 891D | CA | | JZ | SKIP 3 |
| 891E | 25 | | | |
| 891F | 89 | | | |
| 8920 | 78 | | MOV | A,B |
| 8921 | C6 | | ADI | 22H |
| 8922 | 22 | | | |
| 8923 | 27 | | DAA | |
| 8924 | 47 | | MOV | B,A |
| 8925 | 3A | SKIP 3 | LDA | 8600H |
| 8926 | 00 | | | |
| 8927 | 86 | | | |
| 8928 | FE | | CPI | 09H |
| 8929 | 09 | | | |
| 892A | DA | | JC | SKIP 4 |
| 892B | 38 | | | |
| 892C | 89 | | | |
| 892D | FE | | CPI | 17H |
| 892E | 17 | | | |
| 892F | D2 | | JNC | SKIP 4 |
| 8930 | 38 | | | |
| 8931 | 89 | | | |
| 8932 | 78 | | MOV | |
| 8933 | FE | | CPI | |
| 8934 | 44 | | | |

| MEMORY ADDRESS | M/C CODE | LOOP | MNEMONICS | OPERAND |
|---|---|---|---|---|
| 8935 | D2 | | JNC | SKIP 5 |
| 8936 | 43 | | | |
| 8937 | 89 | | | |
| 8938 | 79 | SKIP 4 | MOV | A,C |
| 8939 | E6 | | ANI | 10H |
| 893A | 10 | | | |
| 893B | CA | | JZ | SKIP 5 |
| 893C | 43 | | | |
| 893D | 89 | | | |
| 893E | 78 | | MOV | A,B |
| 893F | C6 | | ADI | 22H |
| 8940 | 22 | | | |
| 8941 | 27 | | DAA | |
| 8942 | 47 | | MOV | B,A |
| 8943 | 78 | SKIP 5 | MOV | A,B |
| 8944 | 32 | | STA | 8FF0H |
| 8945 | F0 | | | |
| 8946 | 8F | | | |
| 8947 | 3E | | MVI | A,00H |
| 8948 | 00 | | | |
| 8949 | 32 | | STA | 8FEFH |
| 894A | EF | | | |
| 894B | 8F | | | |
| 894C | CD | | CALL | DISPLAY |
| 894D | 40 | | | (BUILT IN) |
| 894E | 04 | | | |
| 894F | C9 | | RET | |



# FABRICATION AND TESTING

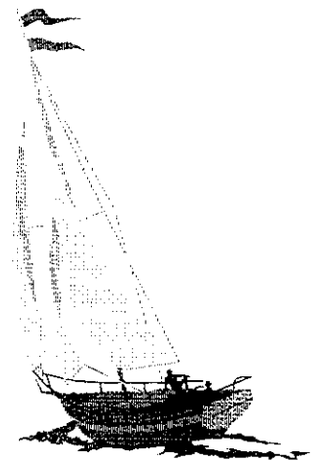
# CHAPTER V

## FABRICATION AND TESTING

The Hardware design is fabricated in a PCB. Testing of the project involves both hardware and software testing. The successful operation of the hardware depends upon the software.

Here initially 4 loads, one single phase Induction motor of 0.7kw and three three phase induction motors each of 2.2.kw were used. Here one motor 2.2.kw was connected to the relay. The maximum load limit and peak time was simulated and performance of the model was tested. During peakhours if the excess load is connected to the EB line then the relay activates and disconnects from th EB line and loads it to the generator.

Thus this project has been successfully tested and the performance is verifed.



# CONCLUSION

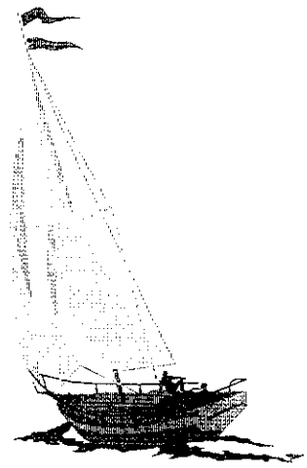
# CHAPTER VI

# CONCLUSION

A combined microprocessor based maximum Demand Monitor and controller has been developed. This unit is successfully tested on number of loads using a 8 bit microprocessor.

The novel advantage of this unit over conventional method is its flexibilities towards future expansion, minimum cost and the facility to introduce a timely protection to the industry against the excess load and avoids penalties to be paid.

This project can also be made as PC based where accessability with the printers is possible. The measurement of power, time can be displayed in the monitor simultaneously. Even an alarm can be fixed to indicate the peak hours. The data like power, frequency can also be maintained in charts.



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# REFERENCES


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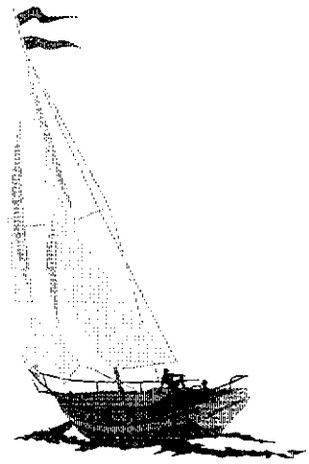
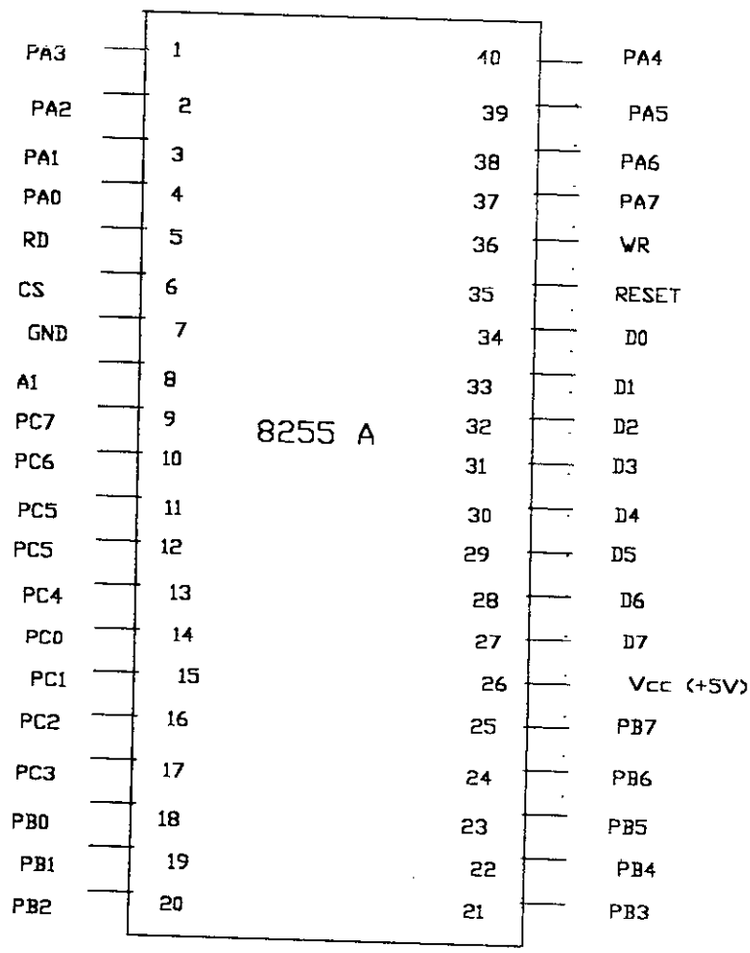
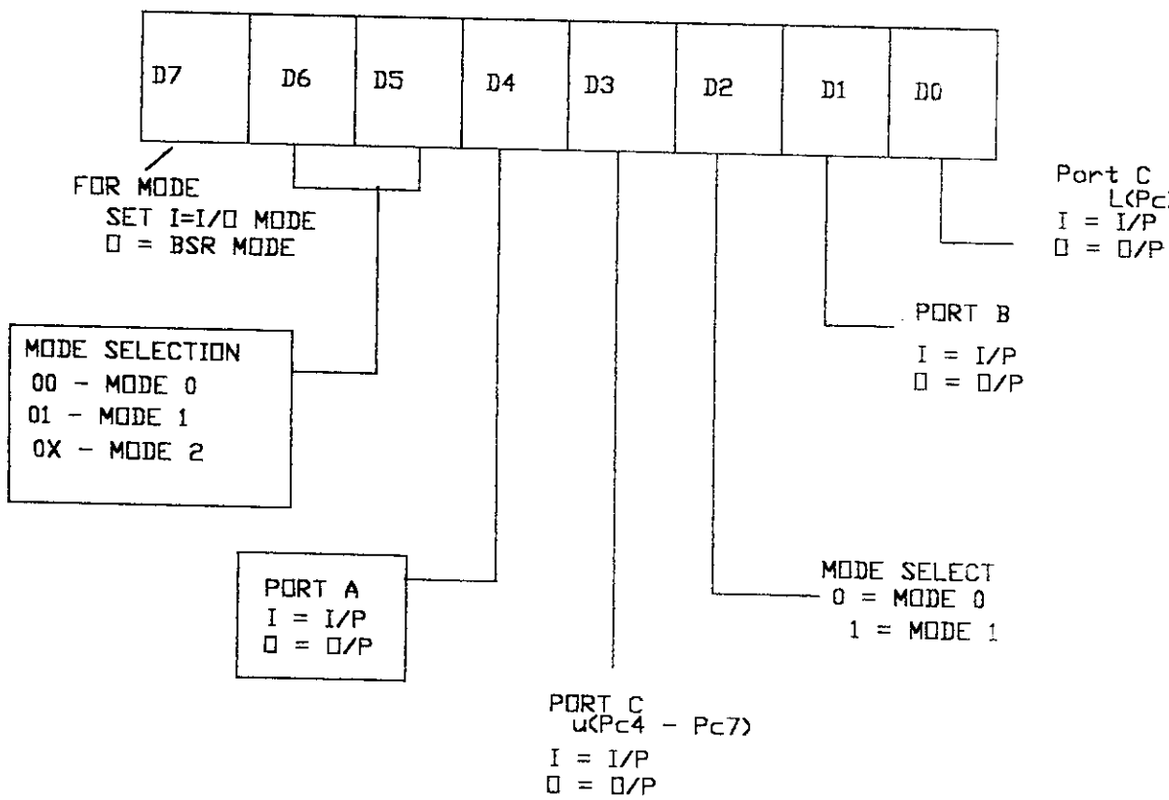
7. Users Manual of MPs 85.2 Manufactured by Electrosystem Associates Pvt. limited.



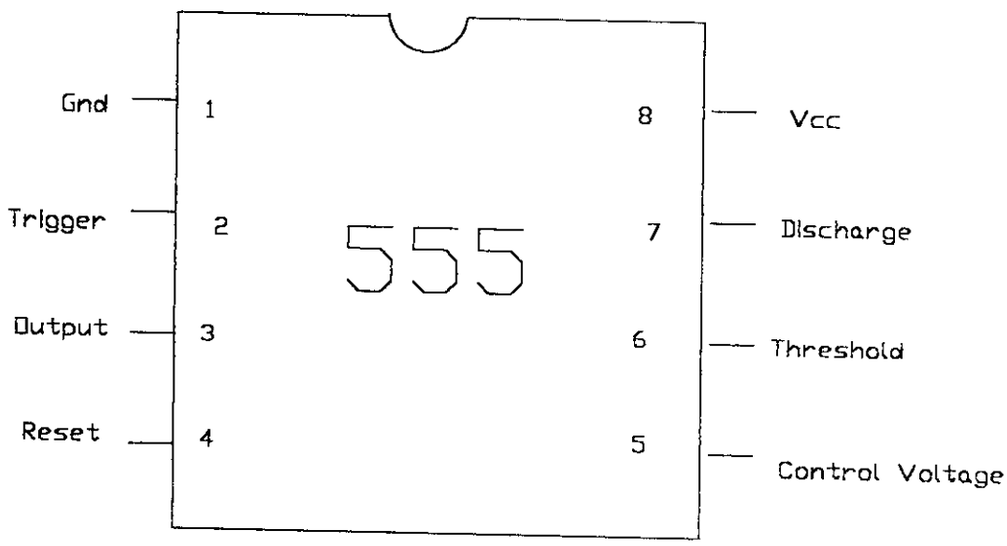
# APPENDIX




PIN CONFIGURATION OF 8255 A

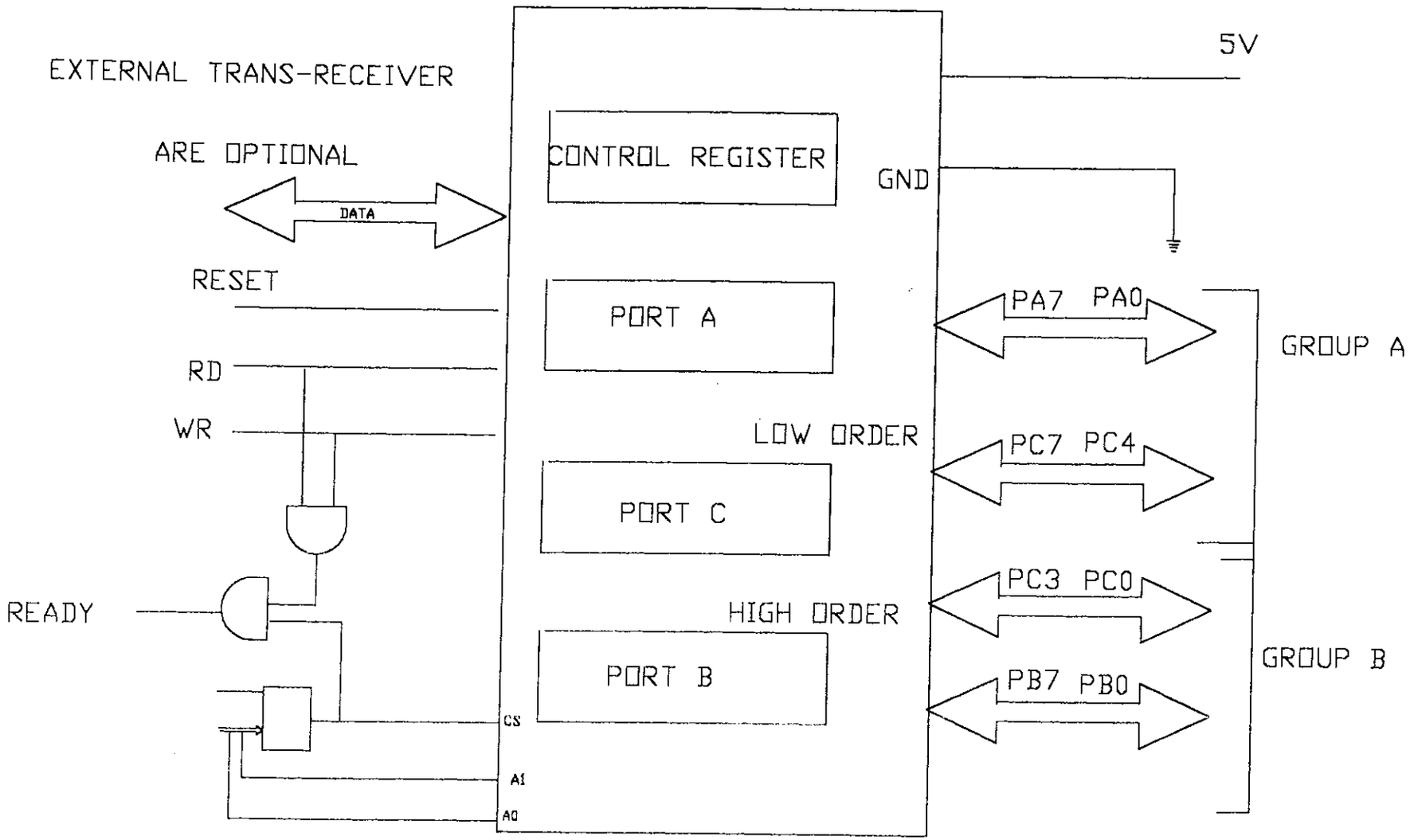



CONTROL WORD FORMAT FOR 8255A




PIN CONFIGURATION OF IC 555 TIMER

8255 A




SIGNAL CONFIGURATION OF 8255 A

ELECTRO SYSTEMS ASSOCIATES PRIVATE LIMITED

PB No 2139

BANGALORE-560021

INDIA

MPS 85-2

CONNECTOR DETAILS

(APPENDIX - B)

J1 & J2

I/O

| PIN No: | SIGNALS | PIN No: | SIGNALS |
|---|---|---|---|
| 1 | PC4 | 2 | PC5 |
| 3 | PC2 | 4 | PC3 |
| 5 | PC0 | 6 | PC1 |
| 7 | PB6 | 8 | PB7 |
| 9 | PB4 | 10 | PB5 |
| 11 | PB2 | 12 | PB3 |
| 13 | PB0 | 14 | PB1 |
| 15 | PA6 | 16 | PA7 |
| 17 | PA4 | 18 | PA5 |
| 19 | PA2 | 20 | PA3 |
| 21 | PA0 | 22 | PA1 |
| 23 | PC6 | 24 | PC7 |
| 25 | +5V | 26 | GND |

J3

ADDRESS

| PIN No: | SIGNALS | PIN No: | SIGNALS |
|---|---|---|---|
| 1 | BS0 | 2 | BS1 |
| 3 | RST 6.5 | 4 | KBRST IN |
| 5 | INTR | 6 | RDY |
| 7 | NC | 8 | BHOLD |
| 9 | BA15 | 10 | BA14 |
| 11 | BA13 | 12 | BA12 |
| 13 | BA11 | 14 | BA10 |
| 15 | BA9 | 16 | BA8 |
| 17 | GND | 18 | GND |
| 19 | BA7 | 20 | BA6 |
| 21 | BA5 | 22 | BA4 |
| 23 | BA3 | 24 | BA2 |
| 25 | BA1 | 26 | BA0 |

J4

DATA

| PIN No: | SIGNALS | PIN No: | SIGNALS |
|---|---|---|---|
| 1 | TCLK 1 | 2 | GATE 1 |
| 3 | OUT 2 | 4 | GATE 2 |
| 5 | CLK 2 | 6 | OUT 1 |
| 7 | RST 55 | 8 | GND |
| 9 | BIO/$\overline{M}$ | 10 | BCLK OUT |
| 11 | ALE | 12 | BRST OUT |
| 13 | $\overline{BWR}$ | 14 | BHLDA |
| 15 | $\overline{BRD}$ | 16 | $\overline{BINTA}$ |
| 17 | GND | 18 | GND |
| 19 | BD1 | 20 | BD0 |
| 21 | BD3 | 22 | BD2 |
| 23 | BD5 | 24 | BD4 |
| 25 | BD7 | 26 | BD6 |

J6

SERIAL

| PIN No: | SIGNALS |
|---|---|
| 1 | GND |
| 2 | $\overline{TXD}$ |
| 3 | RXD |
| 4 | $\overline{RTS}$ |
| 5 | $\overline{CTS}$ |
| 6 | $\overline{DSR}$ |
| 7 | GND |
| 20 | $\overline{DTR}$ |
| 8—19 | N.C |
| 21—25 | NC |

| | | | | | |
|---|---|---|---|---|---|
| DRN | Bharathi | DATE | 8-7-92 | VER No: | 1 2 3 4 5 6 7 8 |
| CKD | Surekha | | | | |
| APPD | Nagendra | SHEET | 1 OF 1 | DRG No: | 2121 |

## 5.2 CPU, ADDRESS BUS,DATA BUS AND CONTROL SIGNALS

MPS85-2 uses 8085A CPU operated with a 6.144 MHZ crystal. The on-board RESET key can provide a RST IN* signal to the CPU. Alternatively, the on-board RESET key can be disabled and an external RST IN* signal provided via the connector J3.

The RSTOUT from CPU is used to reset rest of the system. Also this signal is available after inversion, on connector J4, for resetting any off-board peripherals.

The clock out from CPU is buffered (by 74 LS 245 at U6 ) and is available on connector J4. This clock is divided by two (by 74 LS 74 at U16) to provide the peripheral clock PCLK.

The lower address bus is demultiplexed using a 74LS373 at U4 and the upper address bus is buffered using 74LS245 at U17. The data bus is buffered using a 74LS245 at U15. The control signals RD*,WR*,IO/M*,ALE,INTA*,HLDA and RST OUT are buffered by 74 LS 245 at U6 . All these buffered signals are available on the system connectors J3 and J4. (connector details are given at the end of this chapter.) The "enable" of these buffers is controlled by BHLDA signal. Thus these buffers are automatically disabled when another bus master gains control (through HOLD signal) to drive these signals.

## 5.3 MEMORY ADDRESSENG

MPS85-2 has three 28-pin JEDEC compatible slots (U1,U2 and U3) for accepting memory devices. The socket at U1 is populated with a 27128 which contains the system firmware. The socket at U3 is populated with a 6264 to provide 8K bytes of static RAM. Memory from 8F90H to 8FFFH is utilized by the system and the rest is available to the user. The socket at U2 is unpopulated. This socket can be configured to accept 2732/2764/27128 via jumper JP2 (Refer section 2.1.3). The memory map is as follows:

**TABLE 5.1 Memory Map**

| Device | Address Range |
|---|---|
| 27128 at U1 | 0000-3FFF |
| 6264 at U3 | 8000-9FFF (A000-BFFF) (C000-DFFF) (E000-FFFF) |
| 62256 at U3 | 8000-FFFF |
| 2732 at U2 | 4000-4FFF (5000-5FFF) (6000-6FFF) (7000-7FFF) |
| 2764 at U2 | 4000-5FFF (6000-7FFF) |
| 27128 at U2 | 4000-7FFF |

6264 RAM installed at U3 responds to four address ranges due to address foldback. However the user must use the address range 8000H- 9FFFH for program development. When 2732 is installed at U2 the device responds to four address ranges due to address foldback. Similarly when 2764 is installed at U2, the device responds to two address ranges 4000H to 5FFFH and 6000H to 7FFFH.

The three chip select signals are derived from BIO/M*, BA15 and BA14. The logic is implemented by 74LS 139 at U14 74 LS 00 at U22 and 74 HC 32 at U21.

### Battery Option:

The RAM provided at U3 can be backed up by an optional battery. Holder is provided for two AA type cells with quick charger circuit. User may use either Ni-Cd or dry cells. Care must be taken to remove the discharged cells immediately to prevent leakage of corrosive fluids from the cell that may damage the PCB and the nearby components.

## 5.4 I/O ADDRESSING

I/O decoding is implemented using a 74 LS 138 at U13. BIO/M*, BA7, BA6, BA5 and BA4 only are used to derive the chip select signals. Thus foldback exists over the unused address lines. The I/O devices, their addresses and their usage is summarized below:

TABLE 5.2

I/O ADDRESS MAP

| I/O Device | Address | Usage |
|---|---|---|
| 8255 - 1 at U23 (Programmable Peripheral Interface) | | |
| Port A | 00H | Available to user |
| Port B | 01H | |
| Port C | 02H | The signals are avail |
| Control Port | 03H | on connector J1 |
| 8255 - 2 at U12 (Programmable Peripheral Interface) | | |
| Port A | 40H | |
| Port B | 41H | The signals are available to user at |
| Port C | 42H | connector J2 |
| Control Port | 43H | |
| 8253 at U7 (Programmable Interval Timer) | | |
| Timer 0 | 10H | Timer 0 is required for Single Step facility. |
| Timer 1 | 11H | Timer 1 is used for baud clock generation. |
| Timer 2 | 12H | Timer 2 is available to user. The signals are available on connector J4. |
| Control Port | 13H | |
| 8251A at U9 (Programmable Communication Interface) | | |
| Data Port | 20H | Used for implementing serial communication. |
| Command port | 21H | |