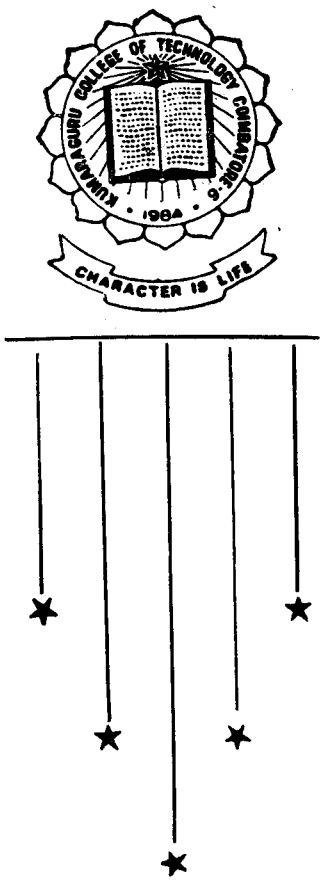
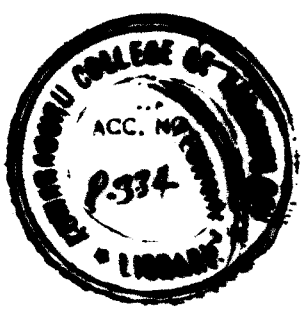
Electronic Synchronizer



Project Report



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This is to certify that the Project entitled

ELECTRONIC SYNCHRONIZER

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SYNOPSIS

Electronic synchronizer is a modern equipment which is meant for synchronization of two alternators. IT checks the conditions to be satisfied by the alternators before synchronizing, by means of electronic devices.

Nowadays in industries and power stations synchronization is done manually by using the existing methods. This requires analog meters and other devices. Also these existing methods are time consuming process and gives only approximate results.

In this project, we set a new trend in the process of synchronization. Electronic components play a major role for checking the conditions that should be satisfied before synchronization process. Conditions to be satisfied by the two alternators are that they must have the same voltage, frequency and phase sequence. Circuits for checking these three conditions are designed, fabricated and checked. After checking, the outputs can be seen visually. Electronic synchronizer gives the accurate result and predicts the exact point of synchronization.

CONTENTS

CHAPTER – 1

INTRODUCTION

SYNCHRONIZATION OF ALTERNATORS

The operation of connecting one alternator in parallel with another alternator or with common bus bar is known as parallel operation or synchronization of alternators.

1.1. NEED FOR SYNCHRONIZATION:

1.1.1. Reliability Of Supply

When two alternators are connected in parallel in case one of the alternator fails the other alternator keeps supplying the load so the continuity of supply to the load is not affected and the system is reliable.

1.1.2. Better Utility Of Machines

In case maximum demand of the power station decreases, some machines may be put off making better use of other machines.

1.1.3. Easy Maintenance And Repairs

It is easy to attend repairs and maintenance work on anyone of the machine without affecting the supply to the load when the alternators are connected in parallel.

1.1.4. Usage Of Older Machines

Due to ageing the capacity of the machine decreases. Because of that we cannot simply throw them away. In order to meet the load we have to synchronize these older machines with new ones or busbars.

1.1.5. Decrease In Reserve Capacity

By synchronizing two or more alternators the reverse capacity of the system is reduced and thereby capital cost is reduced.

1.1.6. Easy To Meet New Load

When there is an increase of load on the system it can be met by connecting alternators in parallel without any additional equipment.

Because of the above advantages we go for synchronizing process. For that purpose we need a device which synchronizes the alternators accurately.

1.2. CONDITIONS FOR SYNCHRONIZATION

For proper synchronization of alternators the following three conditions must be satisfied before they put into the synchronization process.

i) The terminal voltage of the incoming alternator must be the same as the voltage of the other alternator or busbar.

ii) Frequency of generated voltage of one alternator should be equal to frequency of other alternator or busbar.

iii) Phase sequence of existing alternator and incoming alternator must be identical.

1.3. EXISTING METHODS

1.3.1. Dark Lamp Method

Circuit is connected as shown in fig.1.1 first the field excitation of the alternator is so adjusted such that the voltmeter reading 'V2' should be equal to 'V1'. Now the terminal voltages are same.

Phase sequences are identical if the three lamps flicker in clockwise direction. It not the terminals are changed properly.

Speed of the incoming alternator is so adjusted such that the flickering of the lamps are slow. It is preferable the flickering is one dark period per second. Now the two frequencies are almost same. The synchronizing switch is closed. When the three are in dark period the alternator 'A2' is said to be synchronized with busbar. Now the alternator is ready to share the common load. Since the synchronizing switch is closed, when the three lamps are in dark period this method is known as **'DARK LAMP METHOD'**.

1.3.2. Bright And Dark Lamp Method

Circuit is connected as shown in fig. 1.2, first the field excitation of the alternators are so adjusted such that the voltmeter reading 'V2' should be equal to 'V1'. Now the terminal voltages are same.

Phase sequence of the incoming alternator is identified by using sequence indicator. The speed of the incoming alternator is so adjusted such that the frequency must be same as that of busbar frequency. It is adjusted by using three lamps i.e. the lamp L1 is in dark period, the lamp L2 and L3 are in maximum brightness. The synchronizing switches are closed under this condition. Now the alternator "2" is said to be synchronized with busbar.

Since the synchronizing switch is closed when two lamps are in bright period and one lamp is in dark period. So this method is known as **'BRIGHT AND DARK LAMP METHOD'.**

1.3.3. Synchroscope Method

In this method the given alternator is synchronized to the busbar by using synchroscope.

In this method of synchronizing the connection diagram is as shown in fig.1.3. The terminal voltage of the incoming alternator is so adjusted such that the readings of voltmeter 'V2' is equal to 'V1'.

The phase sequence of the incoming alternator and busbar is identified by using phase sequence indicator.

Condition two is verified by using synchroscope. It consists of a fixed coil stator and a rotating coil rotor. Stator is supplied from busbar and the rotor is supplied from incoming alternator as shown in fig. If the frequencies of the busbar and incoming alternator is not same then the rotor of the synchroscope will rotate. A pointer rotates in clockwise direction, then it means the speed of the incoming alternator is fast. If the pointer rotates in anti-clockwise direction then it means speed of the alternator is too slow. The speed of the incoming alternator is so adjusted such that the pointer will not rotate in either direction.

The synchronizing switch is closed position. Now 'A2' is said to be synchronized with busbar.

1.4. ADVANTAGES OF ELECTRONIC SYNCHRONIZATION

By using existing methods for synchronizing process, we have to face certain difficulties and it will give only approximate results. So we go for electronic synchronizer whose advantages are discussed below.

1.4.1. No Need For Meters

If we use electronic synchronizer for synchronizing purpose there is no need for meters i.e. voltmeters and frequency meters. Without these meters we can check terminal voltages of two alternators.

1.4.2. Accuracy

Electronic synchronizer gives accurate results than the existing methods. It senses very small variation in voltages in the range of 0 to 2v. Also it detects very small variation in frequencies in the range of 0 to 1Hz.

1.4.3. Lower Cost

Cost involved in the design and maintenance of the electronic synchronizer is very less when compared to other existing methods of synchronization.

1.4.4. Compact In Size

The size of the electronic synchronizer is very small and it is portable. It occupies very small space when compared to other methods.

1.4.5. Less Power Consumption

The power required for control circuits and checking circuits are very low. It does not require any high wattage lamps as in the case of dark and bright lamp methods. IT needs only 12v dc supply for control circuits.

1.4.6. Easily Understandable

Electronics synchronizer gives visual signal to the operator when after satisfying each condition. From this we can know which condition is not satisfied.

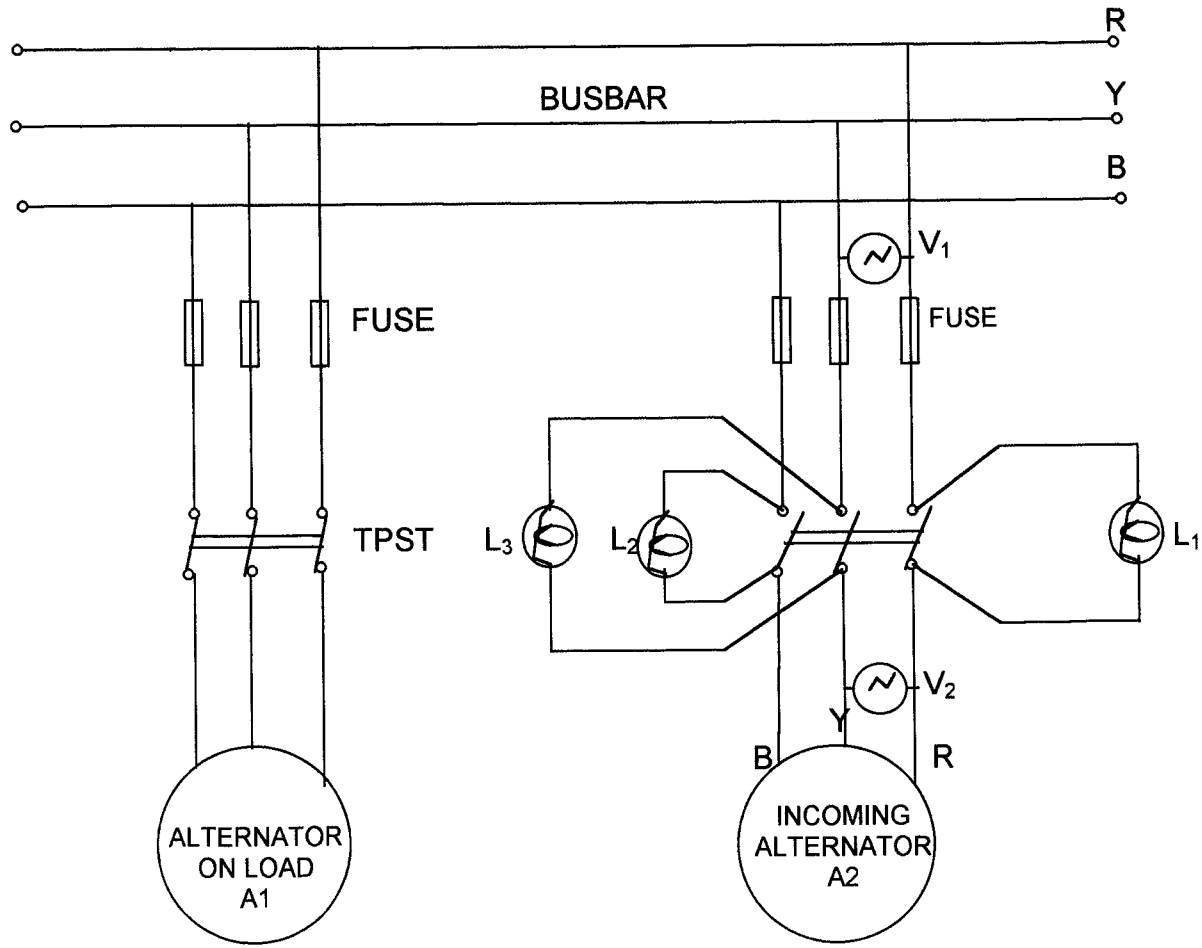


FIG. 1.1. DARK LAMP METHOD

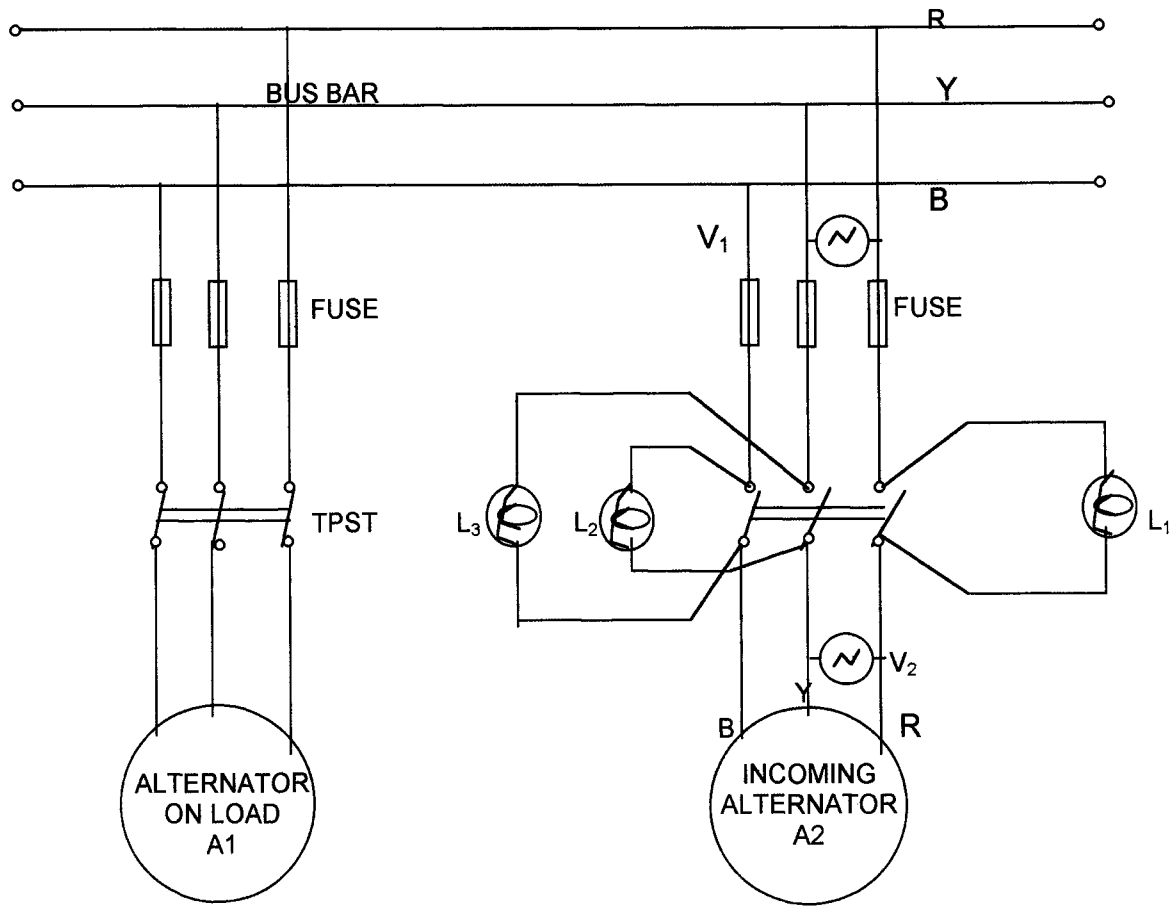


FIG. 1.2. DARK AND BRIGHT LAMP METHOD

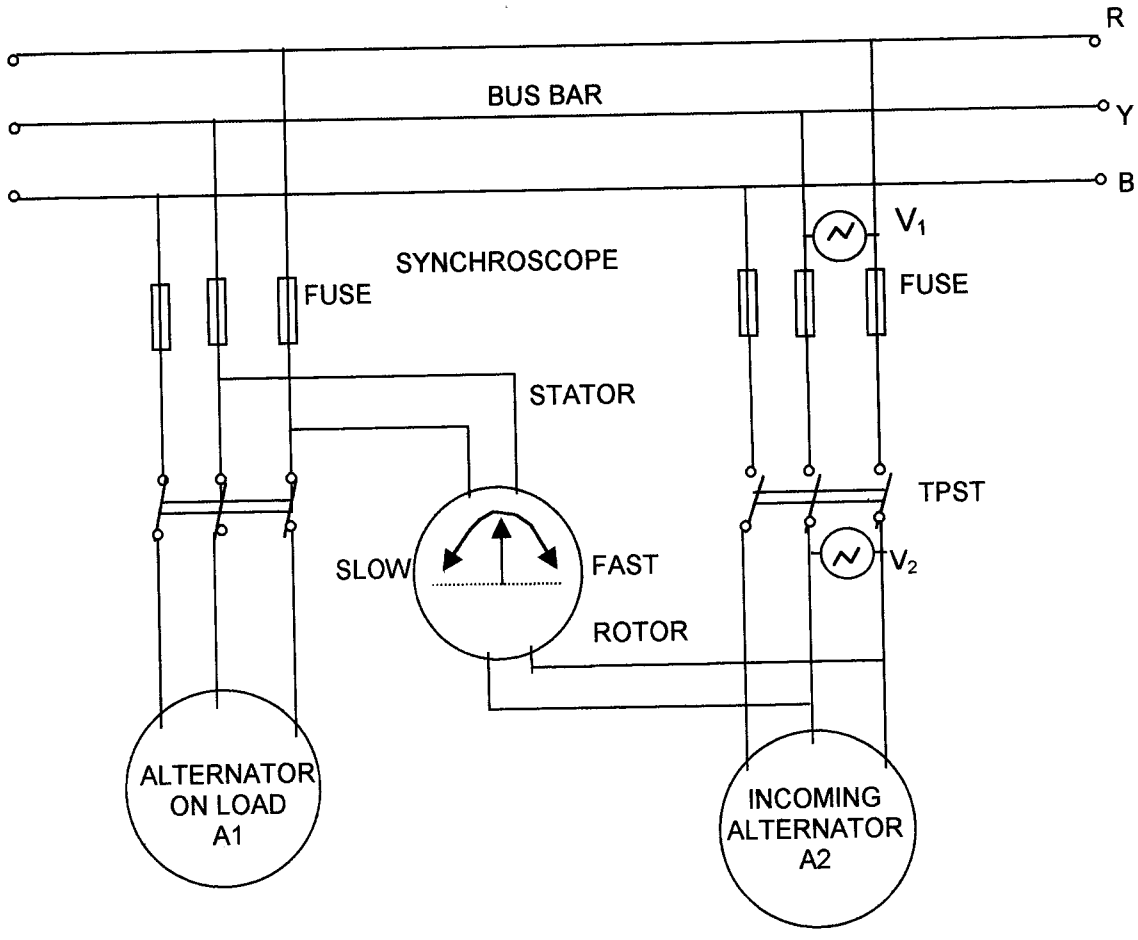


FIG. 1.3. SYNCHROSCOPE METHOD

CHAPTER – 2

BLOCK DIAGRAM AND MODULES

2.1 INTRODUCTION

General block diagram of our project is shown in fig. 2.1. Figure shows the arrangement of the control circuit and switching circuit. 'A1' is connected to 'A2' through a switching circuit. Control circuits are connected parallel to the supply mains.

Control circuits checks the conditions to be satisfied before synchronization. The necessary conditions are

i) Terminal voltages should be same.

ii) Frequency of two alternator voltages should be same.

iii) Phase sequence should be same.

Once the above mentioned conditions are checked and when these are satisfied control circuits gives signal to the switching circuits. Switching circuits connects the two alternators in parallel.

Once the two alternators are in parallel, they supply a common load. Electronic synchronizer gives the visual indication of conditions that are already checked.

2.2. MODULES OF THE PROJECT

Our project is divided into three modules. These three modules checks the different conditions that are to be satisfied before synchronization process. The three modules are listed below.

1. Voltage comparison circuit.
2. Frequency comparison circuit.
3. Phase sequence detection circuit.

Brief operation and performance of each and every module is described below.

2.2.1. Voltage Comparison Circuit

The first module of our project is voltage comparison circuit. This module compromises of rectifier circuit, filter circuit, subtractor circuit and relay driving circuit. First of all the step-down transformers reduce the voltage of alternators. This reduced voltage are rectified by means of bridge rectifier. This pulsating dc voltage is filtered by capacitor filter. Now these two alternator voltages are given to the subtractor circuit, Subtractor circuit gives zero output when two voltages are equal and then transistor operates the relay unit.

2.2.2. Frequency Comparison Circuit

The second module of our project is frequency comparison circuit. This circuit comprises of EX-OR gates, up-down counter and decoder. The two alternator frequencies are given to the EX-OR gates, these gates converts sine wave signal into square wave signal. Up-down counter counts according to the frequency signals of two alternators. When $F_1>F_2$ LED's present in the output circuit rotates in clockwise direction. $F_1<F_2$ LED's rotates in anti-clockwise direction. $F_1=F_2$ LED's donot rotate. After comparison of frequency, Visual indication will be given by electronic synchronizer.

2.2.3. Phase Sequence Detection Circuit

The third module of our project is phase sequence detection circuit. This circuit comprises of phase sequence detector circuit and anode display. It detects phase sequence for standard phase sequence ie., RYB phase sequence detector circuit produces zero output voltage. For non-standard phase sequence ie. RBY 0.886% of supply voltage will be produced at the detector circuit. This voltage is rectified by means of bridge rectifier circuit and then given to seven segment decoder through matching unit. For standard phase sequence '0' will be displayed, non standard phase sequence '1' will be displayed.

2.3. SPECIFICATIONS OF ALTERNATOR

We have designed electronic synchronizer for the alternator having following specifications.

AC Voltage	=	400v
Current	=	4.3 A
KVA	=	3
Speed	=	1500 rpm
Phase	=	3
Frequency	=	50Hz
Connection	=	Y (star)
Power factor	=	0.8
Class of insulation	=	B
DC excitation volts	=	200v
Current	=	1.9Amps

We can synchronize another alternator or busbar having specifications as the above existing alternator with the help of the electronic synchronizer.

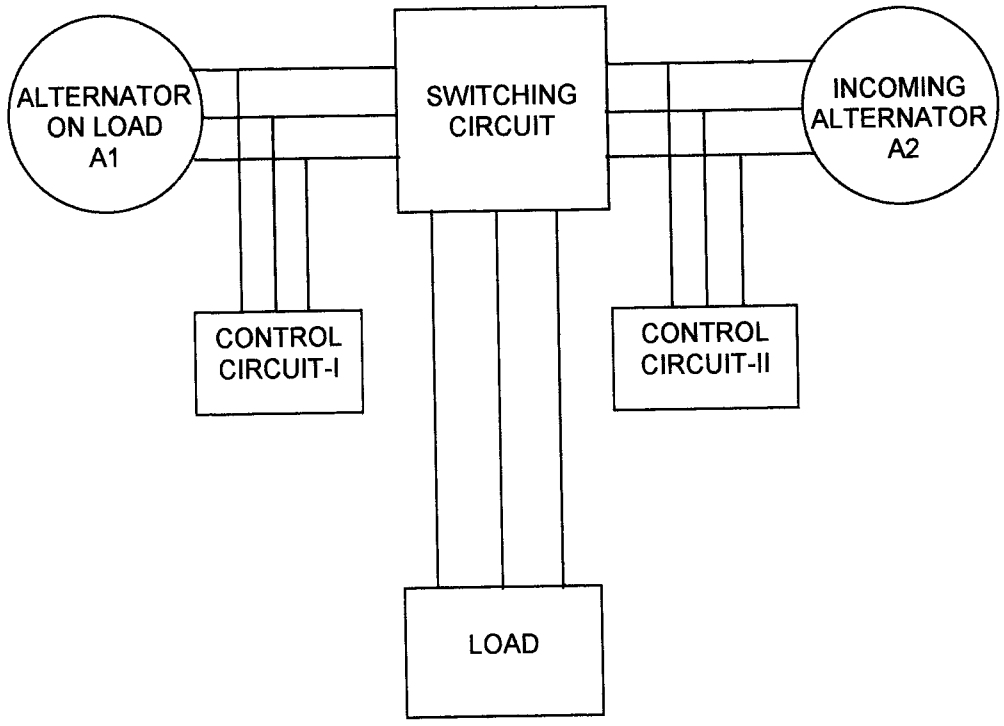


Fig. 2.1. GENERAL BLOCK DIAGRAM

CHAPTER – 3

VOLTAGE COMPARISON CIRCUIT

3.1. DIFFERENTIAL AMPLIFIER DESIGN

A circuit that amplifies the difference between two signals is called a differential amplifier circuit is shown in Fig.3.1. Since the differential voltage at the input terminals of the OP amp is zero, nodes 'a' and 'b' are at the same potential, designated as v3. The nodal equation at 'a' is,

$$\frac{V3 - V1}{R1} + \frac{V3 - V0}{R2} = 0 \longrightarrow (1)$$

and at 'b' is

$$\frac{V3 - V2}{R1} + \frac{V3}{R2} = 0 \longrightarrow (2)$$

Rearranging, we get

$$\left[\frac{1}{R1} + \frac{1}{R2}\right]V3 - \frac{V1}{R1} = \frac{V0}{R2} \longrightarrow (3)$$

$$\left[\frac{1}{R1} + \frac{1}{R2}\right]V3 - \frac{V2}{R1} = 0 \longrightarrow (4)$$

Subtracting equation (4) from (3), we get

$$\frac{1}{R1}(V2 - V1) = \frac{V0}{R2} \longrightarrow (5)$$

Therefore, $V0 = \frac{R2}{R1}[V2 - V1]$

If R1=R2, then V0=V2-V1

Then the output is the difference between the two voltages.

3.2. PRINCIPLE OF OPERATION

In voltage comparison circuit terminal voltages of two alternators are to be compared circuit connections are shown in Fig.3.2. Here we make use of subtractor circuit for voltage comparison. For the subtractor circuit first of all we have to design a differential amplifier circuit. From the differential amplifier circuit we can construct a subtractor circuit. As the subtractor circuit reads 12v dc first the alternators terminal voltages are stepped down by means of transformer. 415v is stepped sown to 12v and this is given to bridge rectifier where ac is converted to dc and then this is applied across capacitor filter which gives ripple free output. Now this can be applied to the inputs of subtractor circuit. The output of subtractor is given to transistor which acts as inverter. The collector terminal of the

transistor is connected to relay and a LED is connected parallel to it. When 'V1' and 'V2' are same LED does not glow. If LED is glowing then 'V2' is adjusted to match with 'V1' till it off. Thus two voltages are compared using the above circuit.

Now let us discuss the operation of bridge rectifier, capacitor filter, subtractor circuit and transistors in the following sections.

3.2.1. Bridge Rectifier

It converts AC voltage to DC voltage. It contains four diodes D1, D2, D3 and D4 connected to form a bridge. The Ac voltage to be rectified is applied to diagonally opposite ends of the bridge rectifier.

When the end 'a' becomes positive and 'b' is negative D1 and D3 are forward biased while D2 and D4 are reverse biased. Therefore only D1 and D3 will conduct. When end 'b' becomes positive and the 'a' negative, D1 and D3 are reverse biased. Hence conduction occurs through D2 and D4 resulting in a full wave rectified output across the capacitor filter whose operation follows.

3.2.2 Capacitor Filter

It converts pulsating DC voltage to continuous voltage without any ripples. As the rectifier voltage increases capacitor starts charging and also supplies current to the load.

At the end of quarter cycle, the capacitor is charged to the peak value of the rectified voltage. Now after the quarter cycle the rectifier voltage starts decreasing. But at the same time the capacitor discharges through the load. The voltage across the load decreases only slightly because the next peak voltage recharges the capacitor. This process is repeated again and again and hence the output waveform becomes ripple free continuous DC voltage.

3.2.3. Subtractor Circuit

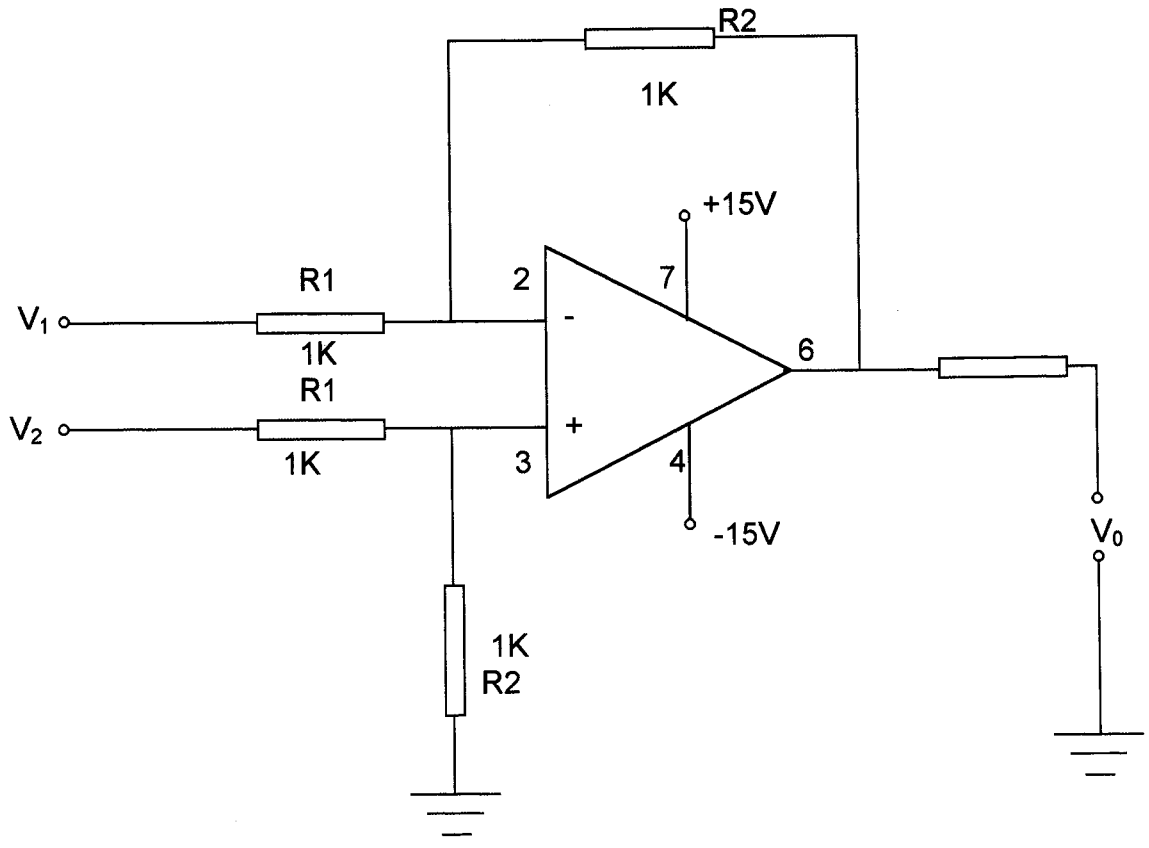
It gives the difference between two voltages. The filtered voltages of the two alternators are given to the inputs of the subtractor circuit. The subractor circuit is made of differential amplifies whose design is explained later. The output of differential amplifier is

If $R_2 = R_1$ then the circuit becomes subtractor circuit. Thus the output of the subtractor circuit is the difference between the two input voltages. First output voltage of 'A1' is on ie 12V DC voltage is applied to the 2nd pin. Voltage available at pin 3 is 'o'. So output at pin 6 is 12V. Now switch on 'A2' and vary its voltage such that the output at pin no.6 is zero.

3.2.4. Transistor Operation

Here transistor acts as a switch. Output of subractor is applied to the base of the transistor. Emitter is grounded and collector is connected to 5V supply through relay. LED is connected in parallel to the relay. When the output voltage of the subtractor is zero voltage available at the collector is 5V and thus LED not glows. When there is any difference in voltage at the output of subtractor then the voltage will be available at the collector the LED will glow.

Thus the difference in voltages of the two alternators are found using the voltage comparison circuit and the results displayed with the help of LED after checking.



$$V_0 = \frac{R1}{R2}[V2 - V1]$$

V1 – Inverting Input

V2 – Non inverting Input

If V1 = V2 then V0=0

FIG. 3.1. DIFFERENTIAL AMPLIFIER

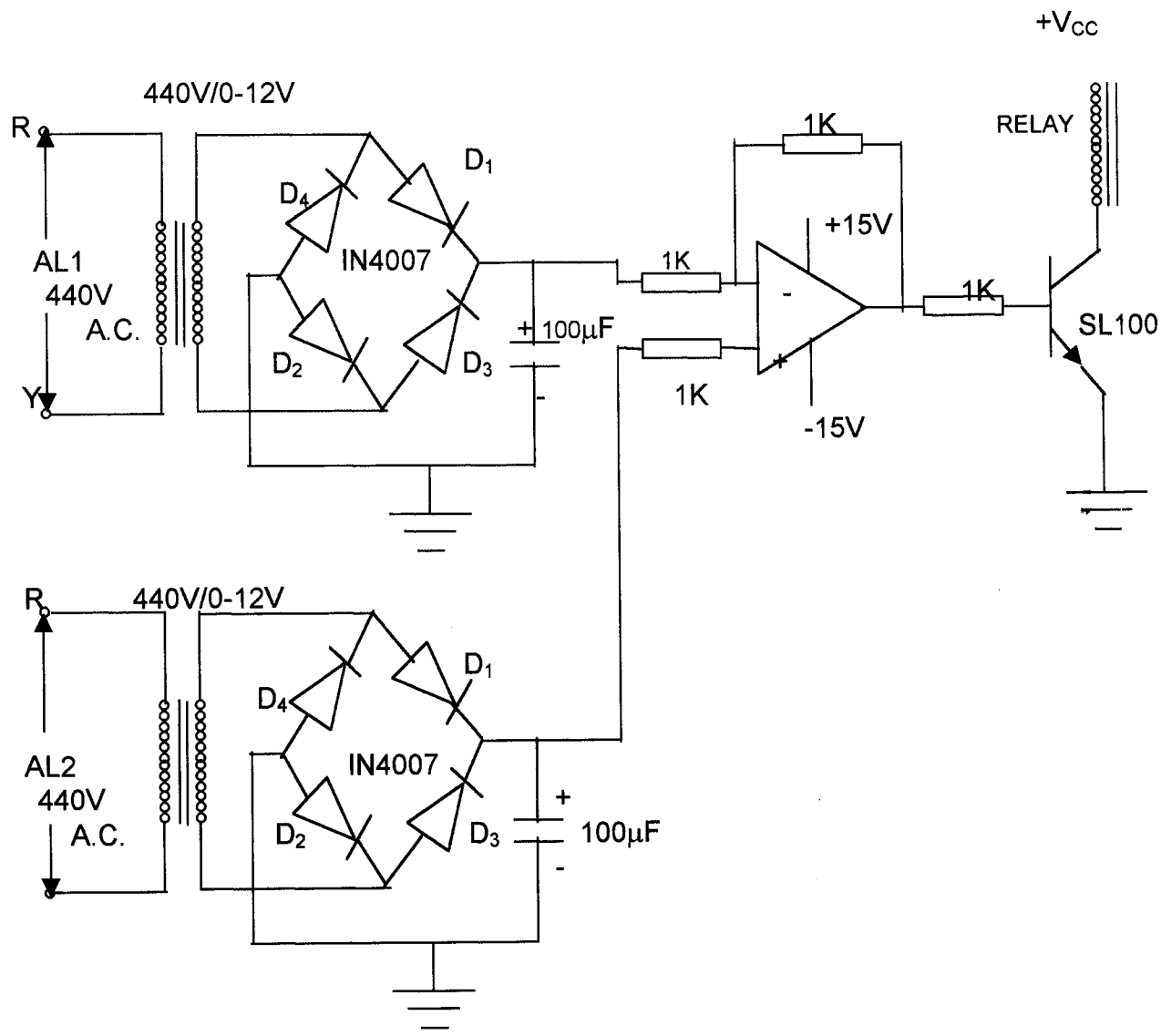


FIG. 3.2. CIRCUIT DIAGRAM FOR VOLTAGE COMPARISON

circuit counts up. When down input control is 1 and up input is 0 (ie. pin No. 4) the circuit counts down. When the up and down inputs are both '0'. The circuit does not change state but remains in the same count. When the up and down inputs are both 1, the circuit counts up. This ensures that only one operation is performed at any given time.

4.1.3 Decoder

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n bit decoded information has unused or do not care combinations, the decoder will have fewer outputs than normal 2^n. The decoder used here is called 'n' to 'm' line decoder where $m \leq 2^n$. Their purpose is to generate 2^n miniterms.

CHAPTER – 4

FREQUENCY COMPARISON CIRCUIT

4.1. CIRCUIT DESCRIPTION

Another important module of this project is frequency comparison circuit shown in fig. 4.1. It compares the two alternator frequencies, by means of Ex-OR gates, counter and decoder. When F1>F2 the LED's present in output rotates in clockwise direction. F1<F2 then LED's rotates in anti-clockwise direction. If F1=F2 dot does not rotate.

4.1.1 EX-OR Gates

EX-OR gates present in the input side converts sine wave to square wave. Output of gate No. 3 is given to the count up of counter and output of gate No. 4 is given to the count down of the counter circuit.

4.1.2 Up-Down Counter

Outputs of EX-OR gates are given to the counter circuit. This type of binary counter is capable of counting either up or down. The T-Flip flops employed in this circuit may be considered as JK flip flops with J and K terminals tied together. When up input control is 1 (ie. pin No. 5) the

4.2 PRINCIPLE OF OPERATION

Two alternator voltages are stopped down by means of transformer and is given to the input of the EX-OR gates. These EX-OR gates converts sine wave into square wave corresponding to the frequency of alternators.

Gate No. 3 produces a square wave ie. proportional to the frequency of A1. Gate No. 4 produces a square wave ie. proportional to the frequency of A2. Output of gate 3 is connected to count up control line, output of gate 4 is connected to count down line. When F1>F2 count up line is always at high level, so the counter states counting as an up counter. So LED's rotates in clockwise direction. When F1<F2 count down line is always at high level so the counter starts counting as down counter, so LED's rotates in anti-clockwise direction. When F1=F2 both up and down control lines are at low level so the output does not change and it remains in previous state. So the dot does not rotate. By observing this condition we can predict the exact point of synchronization.

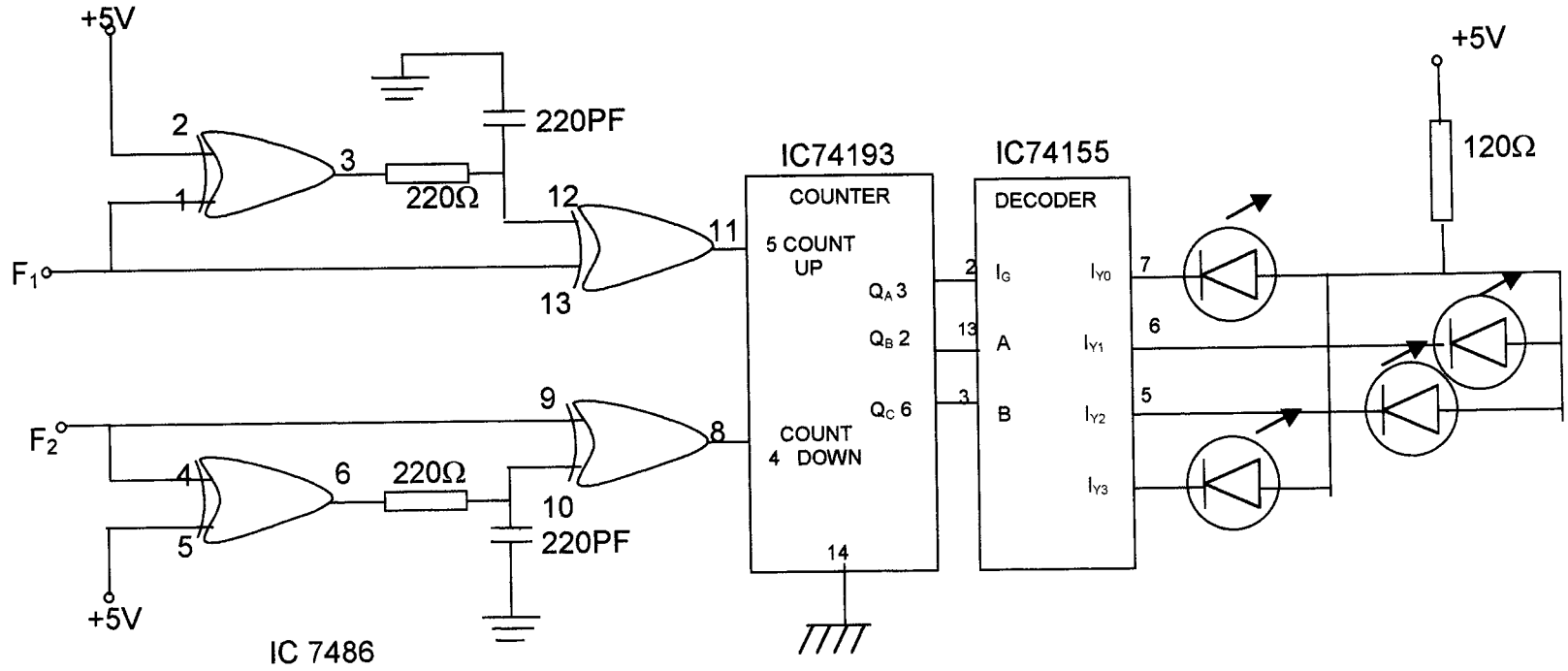


FIG. 4.1. CIRCUIT FOR FREQUENCY COMPARISON

CHAPTER – 5

PHASE SEQUENCE DETECTION CIRCUIT

5.1. NECESSITY OF PHASE SEQUENCE DETECTION

In a three phase supply system the order in which the three phases namely R, Y, B attain their maximum value is called the phase sequence.

If the sequence is R-Y-B, it is called correct sequence or if the sequence is R-B-Y it is called incorrect phase sequence.

Usually the phase sequence of the three phase system is detected by means of electric phase sequence meters. In this type there would be friction due to the moving system and heating due to the resistance of the coils. This is turn would lead to erroneous results. Also the electrical method of phase sequence meter is costlier.

Digital techniques have improved much nowadays and it gives accurate results irrespective of it period of use. Hence the design of a simple scheme of electronic phase sequence detector has been attempted and it is explained in the subsequent chapter.

5.2. DESCRIPTION OF CIRCUIT

The circuit connection of the static phase sequence detector is shown in the circuit.

5.2.1 Transformer

The potential difference between the output terminals (at the secondary winding terminals) of the phase sequence detector is designed to produce '0' voltage. When the primary terminals of the transformer is connected to a 440v, 50Hz supply with standard phase sequence R-Y-B. The phasor diagram is shown in fig.

The potential difference between the output terminals designed for 0.866% of the line voltage. When the phase sequence is non standard the nature of the phasor diagram is shown in Fig.5.1

5.2.2 Bridge Rectifier

The bridge rectifier is used to rectify the a.c. output voltage from phase sequence detector. The full wave rectified output voltage is applied to the matching circuit.

5.2.3 Purpose Of Matching Unit

The circuit diagram of the matching unit is shown in fig. 1. The base of the transistor T1 is connected to the positive end terminal of the bridge rectifier. The emitter of the transistor T1 is connected to the negative end terminal of the bridge rectifier as shown in Fig.5.2 The output from collector of T1 is connected to T2.

The purpose of introducing matching unit in the phase sequence detector circuit is expressed below.

Under non-standard phase sequence condition output of phase sequence detector is 5.7v. The capacitor does not attain the value quickly so as to get 1 indication from the display. The capacitor takes some time to attain the maximum value. Hence even under non standard sequence condition the display indicates '0' for some time. So, also when the phase sequence detector is connected to standard phase sequence system of power supply, the capacitor does not discharge immediately, to the level of the output voltage of phase sequence detector.

Under the circumstance, display shows indication, even when the phase sequence is standard. In order to avoid this difficulty and to get quick response, the matching unit is employed.

5.2.4. Seven Segment Decoder

The 7447 features active low outputs designed for driving common-anode LED.

It is designed to display only '0' and '1'. When phase sequence is RYB or RBY. It is seen the function table to get zero indication LT RB1 and B1/RB0 must be at high level and other inputs to seven segment decoder must be low. To get '1' indication LT, B1/RB0 and A should be logic high level and all other inputs of the seven segment decoder except RB! Which is irrelevant, should be at low level. To meet this requirement, input B(1), C(2) and D(6) are connected to ground as shown in Fig. 5.3. Pin 7 and 8 are connected to matching circuit.

By this arrangement, the display shows '0' when pin 7 of IC 7447 is at logic low level and FND 507 displays '1'. When pin 7 is at logic high level.

5.2.5. SEVEN SEGMENT LED DISPLAY

The Fig 5.3 shows seven segment LED display. It is connected to the output of IC 7447 such that it displays '0' or '1'. When phase sequenced is standard or non standard respectively.

In order to drive this segment A, B, C, D, Entrepreneurs and F should be 'ON', and to indicate 1 the segment B and C should be 'ON' and all other segments are 'OFF'. Pins 3 and 8 are common anode, hence these are connected to +5v dc supply.

5.3. PRINCIPE OF OPERATION

This chapter describes the operation of the static phase sequence detector. The phase sequence detector consists of two single phase transformers connected to form a three phase set down transformer, dull wave rectifier, a matching circuit, IC 7447 and a display LED FND 507. The circuit diagram of static phase sequence detector is shown in Fig. 5.3.

Two single phase transformers are connected to form a three phase Step-down transformer. The potential difference between the output terminals of the phase sequence detector is designed to produce '0' voltage when the phase sequence is standard that is RYB.

Similarly the potential difference between the output terminals designed for 0.866% of the line voltage, when the phase sequence is RBY.

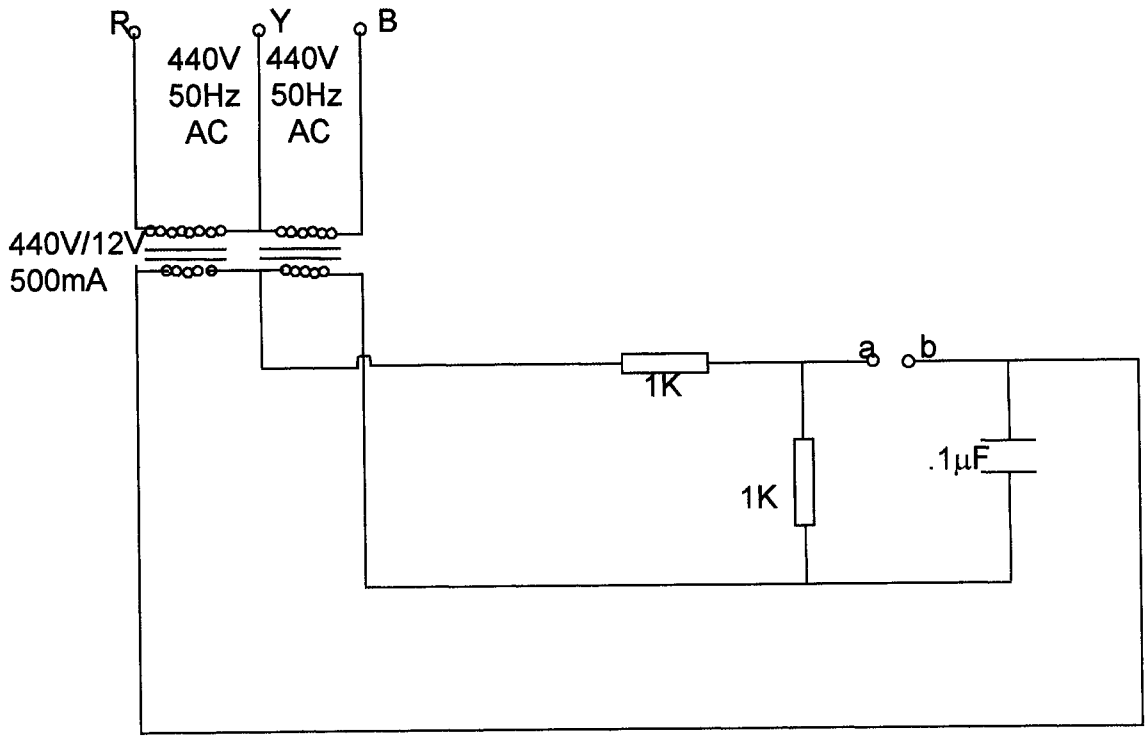


FIG. 5.1. PHASE SEQUENCE DETECTOR

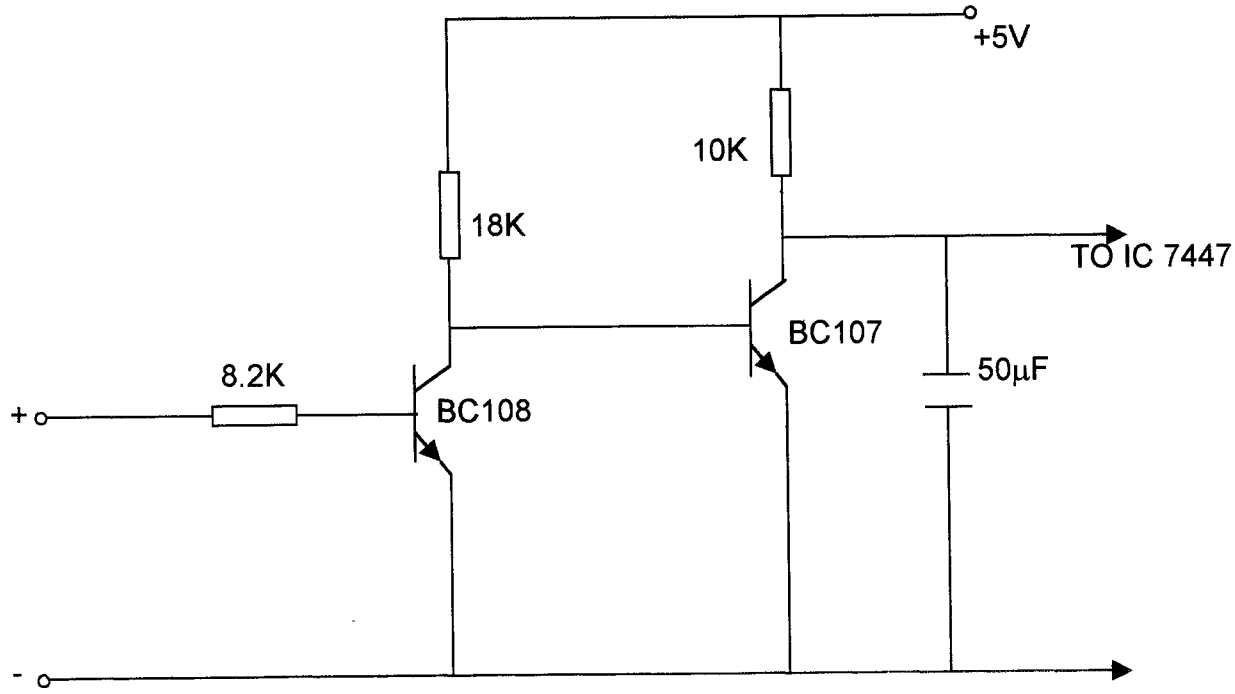


FIG. 5.2. MATCHING CIRCUIT

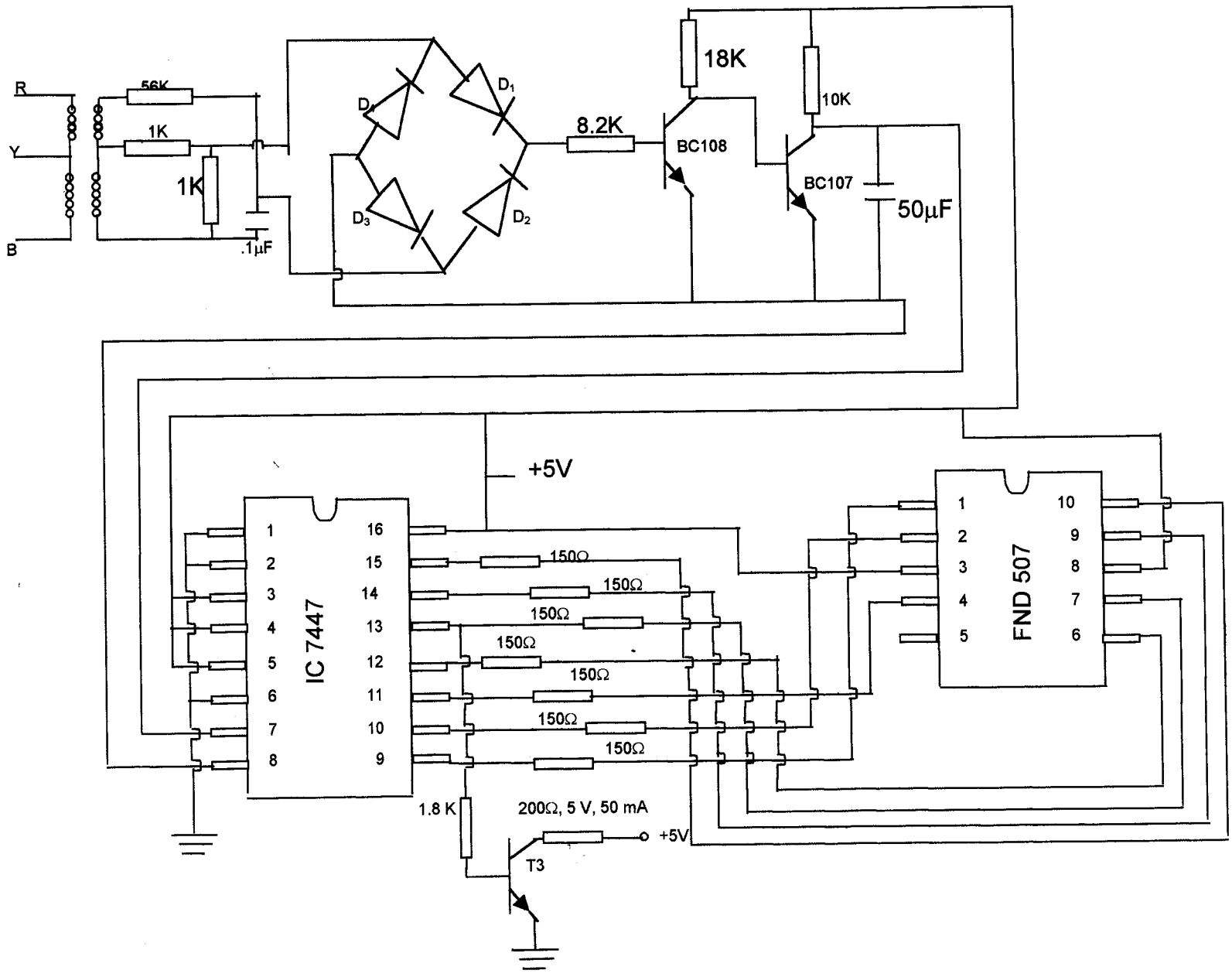


Fig.5.3 CIRCUIT FOR DIGITAL PHASE SEQUENCE DETECTOR

CHAPTER – 6

POWER SUPPLY UNIT

6.1. RECTIFIER OPERATION

Fig.6.1. shows the arrangement of power supply unit which supplies the power to the control circuits.

It consists of centre-tapped transformer of rating 230v/(15v–0–15v). A bridge rectifier circuit made up of semiconductor diodes are connected in between points A and B. The alternating voltage available at terminals A and B are 180^{o} out of phase with each other.

For an operational amplifier circuit we need +15v and –15v for proper operation. That can be obtained by using this circuit.

When the terminal 'A' is positive with respect to 'B' the diodes D1 and D2 are forward biased and thus they conduct. Diodes D3 and D4 are reverse biased and they are nor conducting. When the terminal 'B' is positive with respect to terminal 'A' diodes D3 and D4 are conducting and D1 and D2 are reverse biased. Thus entire cycle is rectified.

We can take +15v and –15v at the output terminals. These outputs are connected to the operational amplifier circuit.

For other control circuits we need +5v supply. This can be obtained by using the same circuit with some additional components. The existing +15v supply is applied to zener diode having breakdown voltage of 6.1v through the current circuiting resistors. The versatile IC regulator 7805 is connected across the zener diode for regulating purpose and gives constant 5v supply.

6.2. FILTER OPERATION

Filter circuits are employed to reduce the rectifier output ripple. This is achieved by either bypassing the ac output components around the load or by a shunt capacitance.

The capacitor filter circuit as shown in Fig.6.1. The capacitance is so chosen that $X_C << R_L$ and the alternating currents find a low resistance shunt in C. Only small alternating current component pairs in load, producing a small ripple voltage.

The capacitor filters the conditions under which the diode operates. When the diode output voltage is increasing the capacitors store energy, by charging to the peak of the input cycle with the falling source voltage. The diode disconnects the source from the load at the instant when the source voltage starts to fall faster than the capacitor voltage can fall as determined by the line constant of `C' and the load.

The capacitor continues to maintain the load voltage at a higher value and lower ripple than if the capacitor were not present.

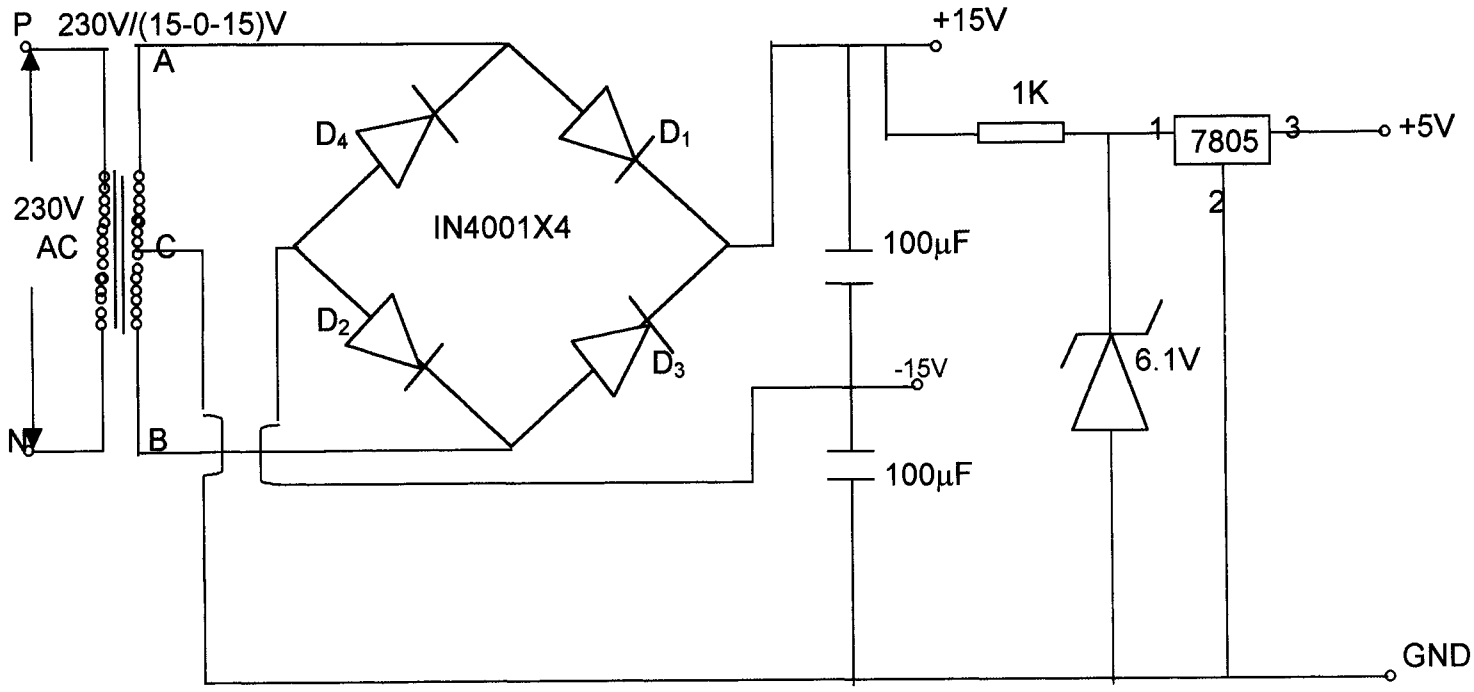


FIG. 6.1. POWER SUPPLY UNIT FOR CONTROL CIRCUITS

CHAPTER – 7

TESTING

7.1 TESTING OF VOLTAGE COMPARISION CIRCUIT

Comparison of voltage is one of the conditions to be satisfied before synchronization of two alternators. Voltage comparison circuit is one of the modules of electronic synchronizer. It has been designed and fabricated as per the circuit diagram shown in fig. 3.1. using electronic components.

When the circuit was tested by applying terminals voltages of the two alternators the LED in the output glowed when there is a difference in the two voltages. LED does not glow when the voltages are same.

From the test result it is seen that voltage comparison circuit compares voltage and gives visual display which helps in easy checking of the conditions. The circuit has a tolerance of $\pm$10volts.

REFERNCE VOLTAGE (in volts) (ALTERNATOR – 1)	COMPARISON VOLTAGE (in volts) (ALTERNATOR – 2)	STATUS OF LED
440	410	GLOWS
440	425	GLOWS
440	430	DOES NOT GLOW
440	440	DOES NOT GLOW

7.2. TESTING OF FREQUENCY COMPARISON CIRCUIT

Comparison of frequency is one of the conditions to be satisfied before synchronization of two alternators. Frequency comparison circuit is one of the modules of electronic synchronizer. It has been designed and fabricated as per the circuit diagram shown in Fig.4.1 using electronic components.

When the circuit was tested by applying the frequencies of the two alternators the LED's in the output glowed and the dot rotated in clockwise direction when frequency of 'A1' was greater, dot rotates in anti-clockwise direction frequency of 'A1' is lesser. When both the frequencies are same then the dot stopped rotation. From the test result it is seen that frequency comparison circuit compares frequency and gives visual display which helps in easy checking of the condition. The circuit helps synchronization at the same frequency and does not operate when there is a difference as small as 0.1Hz.

FREQUENCY OF ALTERNATOR 1 (in Hz)	FREQUENCY OF ALTERNATOR 2 (in Hz)	ROTATION OF LED'S
49	48	CLOCKWISE
49	48.9	CLOCKWISE
49	49	DOES NOT ROTATE
49	49.1	ANTICLOCKWISE
49	50	ANTICLOCKWISE

7.3. TESTING OF PHASE SEQUENCE DETECTOR CIRCUIT

Phase sequence of two alternators is to be checked before they put into the parallel operation. In this project digital phase sequence detector has been designed and fabricated as per the circuit diagram shown in Fig.5.3 using electronic components.

This circuit was tested by applying the step-down voltage through the two single phase transformers of rating of 440 / (0-12v), 500 mA. From the test results it is seen that for standard phase sequence ie. RYB the seven segment display shows '0'. For non standard phase sequence ie. RBY the seven segment display shows '1'.

PHASE SEQUENCE	OUTPUT OF DISPLAY
RYB	0
RBY	1

CHAPTER – 8

CONCLUSION

An effective equipment which could predict the exact point of synchronization using electronic components has been designed, fabricated and tested.

An "Electronic Synchronizer" checks all the three conditions that should be satisfied by alternators before they are synchronized. The first condition ie. terminal voltage of two alternators are checked by means of subtractor circuit designed by using operational amplifier. Frequency of two alternators are checked by means of XOR gates, up-down counter and decoder. Phase sequence of two alternators are checked by means of static phase sequence detector, transistors, seven segment decoder. These three modules give accurate results.

If these three conditions are satisfied, then the synchronizing switch is closed automatically or manually.

The developed system has the following advantages over existing methods.

i. No need for meters.

ii. Accuracy.

iii. Less time consumption.

iv. Low cost.

Electronic synchronizer finds its application in laboratories, industries and power stations where the alternators are to be synchronized.

FURTHER DEVELOPEMTNS

This project can be further improved as 'Automatic Synchronizer' by using closed loop control technique. Voltage module can be modified by sensing the output of subtractor circuit, if the output of subtrctor circuit is other than zero volts that this error signal is amplified and given to the field of alternator. Frequency module can also be modified by using some special type of sensors. Similarly phase sequence part can be modified by using phase sequence detector cum changer circuit.

REFERENCES

1. HERBERT TAUB "DIGITAL INTEGRATED ELECTRONICS" MCGRAW HILL BOOK COMPANY NEW DELHI 1986.

2. RAMANT A GAYAKWAD "OP-AMPS AND LINEAR INTEGRATED CIRCUITS" PRENTICE HALL OF INDIA NEW DELHI 1991.

3. M.CHILIKIN "ELECTRICAL DRIVES" MIR PUBLISHERS MOSCOW 1978.

4. ALEXANDER "ELECTRICAL INSTRUMENTS AND MEASUREMENTS" WILLIAM CHOWS AND SONS LTD LONDON 1951.

5. MILLMAN HALKIAS " INTEGRATED ELECTRONICS" 24^{TH} PRINTED DELHI 1982.

6. ALLEN MOTTERSHEAD "ELECTRICAL DEVICES AND CIRCUITS" PRINTICE HALL OF INDIA NEW DELHI 1982.

7. JOHN MARKUS "MODERN ELECTRONIC CIRCUITS MANUAL " MCGRAW HILL PUIBLISHERS NEW DELHI 1991.

8. B.L.THERAJA AND A.K.THERAJA "ELECTRICAL TECHNOLOGY" VOLUME-II, KHANNA PUBLISHERS NEW DELHI 1996.

APPENDIX

OPERATIONAL AMPLIFIER DETAILS

ADVANTAGES

An op-Amp has many advantages such as small size, high reliability, reduced cost, temperature tracking and low offset voltage and current.

It has a differential input, with voltages V1 and V2 applied to the inverting and non inverting terminals respectively.

IDEAL OP-AMP CHARACTERSTICS

- Input Resistance R_{in} =High
- Output Resistance R_o = 0
- Voltage Gain AOL = ∞
- Bandwidth = ∞
- Perfect balance; V_0 = 0 when V1=V2
- Characteristics do not drift with temperature.

BASIC INFORMATION OF OP-AMP

The circuit schematic of an op-amp is a triangle. It has two input terminals and one output terminal. The terminal with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

OP-AMP TERMINALS

Op-amp have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp.

The mini dip has eight pins. The top pin on the left of the notch locates pin 1. The other pins are numbered counter clockwise from pin1, beginning with pin1. Pin2 is called the inverting input terminal and pin3 is the non-inverting input terminal, pin6 is the output terminal and pins 7 and 4 are the power supply terminals labeled as V^+ and V^- respectively. Terminals 1 and 5 are used for dc offset. The pin8 marked NC indicates (No connection). Internal connections and pin details of operational amplifier circuit is shown in Fig.A.1.

1. The current drawn by either of the input terminals (non-inverting and inverting) is negligible.

2. The differential input voltage V_d between non-inverting and inverting input terminals is essentially zero.

OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

Commercially integrated circuit op-amps usually consist of four cascaded blocks as shown in Fig.A.3, The first two stages are cascaded difference amplifiers used to provide high gain to the difference mode signal and cancel the common-mode signal, that is, it should have high CMRR. The third stage is a buffer and the last stage is the output drover. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics. The output voltage should swing symmetrically with respect to ground. To a low such symmetrical swing, the amplifier is provided with both positive and negative supply voltages. Power supply voltages of +15V are common. The buffer stage along with the output stage also acts as a level shifter so that output voltage is zero for zero inputs. Additionally, an op-amp generally incorporate circuitry to provide drift compensation and frequency compensation.

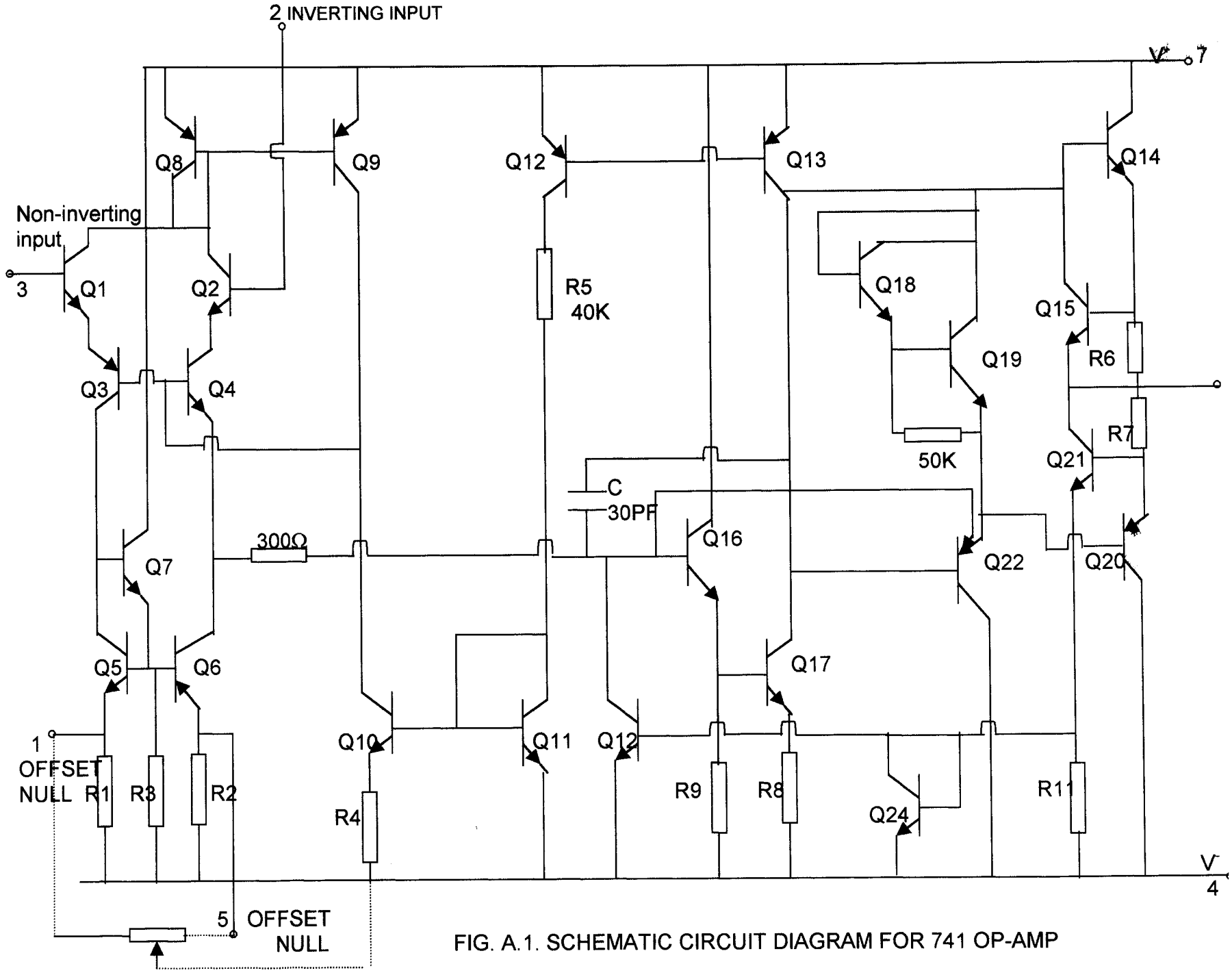


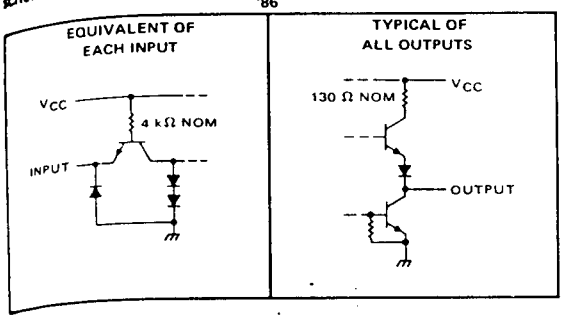
FIG. A.1. SCHEMATIC CIRCUIT DIAGRAM FOR 741 OP-AMP

TYPES SN5486, SN54L86, SN54LS86A, SN54S86, SN7486, SN74LS86A, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

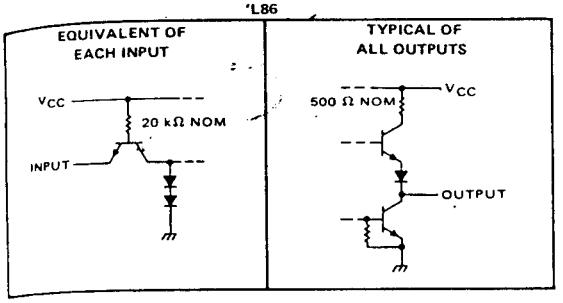
DECEMBER 1972 – REVISED DECEMBER 1983

schematics of inputs and outputs

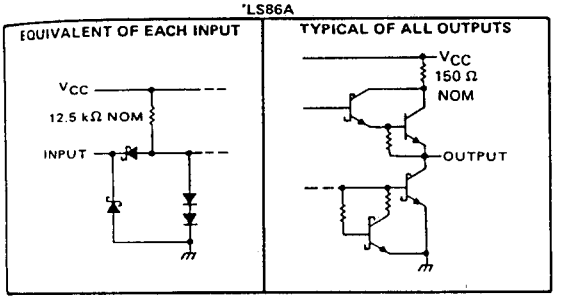
'86



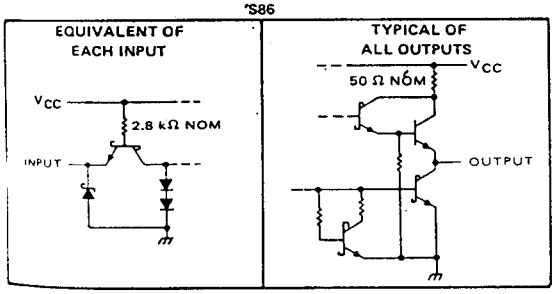
'L86



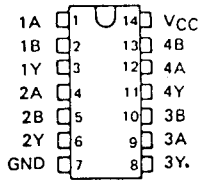
'LS86A



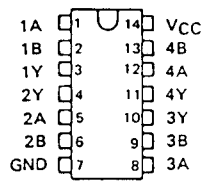
'S86



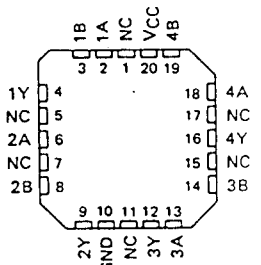
SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE
SN7486 . . . J OR N PACKAGE
SN74LS86A, SN74S86 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54L86 . . . J PACKAGE
(TOP VIEW)



SN54LS86A, SN54S86 . . . FK PACKAGE
SN74LS86A, SN74S86 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLES

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86A	10 ns	30.5 mW
'S86	7 ns	250 mW

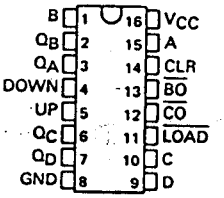
TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193, SN74192, SN74193, SN74LS192, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

DECEMBER 1972–REVISED DECEMBER 1983

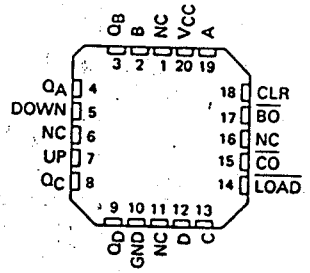
- **Cascading Circuitry Provided Internally**
- **Synchronous Operation**
- **Individual Preset to Each Flip-Flop**
- **Fully Independent Clear Input**

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'L192, 'L193	7 MHz	43 mW
'LS192, 'LS193	32 MHz	95 mW

SN54192, SN54193, SN54LS192, SN54LS193 . . . J OR W PACKAGE
SN54L192, SN54L193 . . . J PACKAGE
SN74192, SN74193 . . . J OR N PACKAGE
SN74LS192, SN74LS193 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS192, SN54LS193 . . . FK PACKAGE
SN74LS192, SN74LS193 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

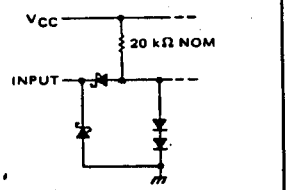
	SN54*	SN54L*	SN54LS*	SN74*	SN74LS*	UNIT
Supply voltage, V_{CC} (see Note 1)	7	8	7	7	7	V
Input voltage	5.5	5.5	7	5.5	7	V
Operating free-air temperature range	− 55 to 125			0 to 70		°C
Storage temperature range	− 65 to 150			− 65 to 150		°C

NOTE 1: Voltage values are with respect to network ground terminal.

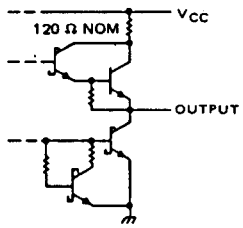
schematics of inputs and outputs (continued)

'LS155A, 'LS156 | 'LS155A | 'LS156

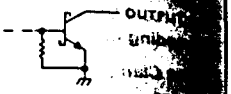
EQUIVALENT OF EACH INPUT



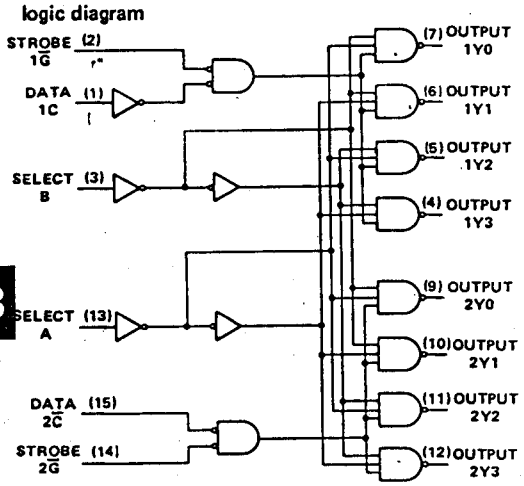
TYPICAL OF ALL OUTPUTS



TYPICAL OF ALL OUTPUTS

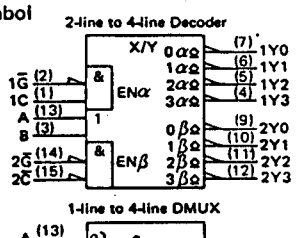


logic diagram

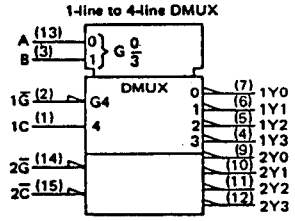


logic symbol

2-line to 4-line Decoder



1-line to 4-line DMUX



Pin numbers shown on logic notation are for D, J or N packages.

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS		
SELECT		STROBE	DATA			
B	A	$1\overline{G}$	1C	1Y0	1Y1	1Y2
X	X	H	X	H	H	H
L	L	L	H	L	H	H
L	H	L	H	H	L	H
H	L	L	H	H	H	L
H	H	L	H	H	H	H
X	X	X	L	H	H	H

INPUTS				OUTPUTS		
SELECT		STROBE	DATA			
B	A	$2\overline{G}$	$2\overline{C}$	2Y0	2Y1	2Y2
X	X	H	X	H	H	H
L	L	L	L	L	H	H
L	H	L	L	H	L	H
H	L	L	L	H	H	L
H	H	L	L	H	H	H
X	X	X	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)		
C†	B	A	$\overline{G}$‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and $2\overline{C}$ connected together
‡$\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together
H = high level, L = low level, X = irrelevant

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155A, 'LS156 . . . . . 7 V
Off-state output voltage: '156 . . . . . 5.5 V
'LS156 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

Recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54155 SN74155			UNIT
			MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			V
V_{IL} Low-level input voltage					0.8	V
V_{IC} Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS} Short-circuit output current§	V_{CC} = MAX	SN54155	−20		−55	mA
		SN74155	−18		−57	
I_{CC} Supply current	V_{CC} = MAX, See Note 2	SN54155		25	35	mA
		SN74155		25	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

Switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}	A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

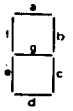
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
¶ See General Information Section for load circuits and voltage waveforms.

escription

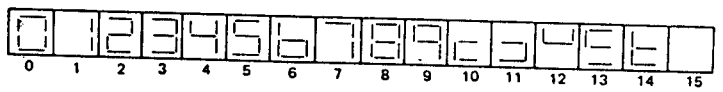
The '46A, 'L46, '47A, 'L47, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or common-cathode VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a lamp test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'L46, 'L47, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ($\overline{BI}$) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the 6 and the 9 with tails and have been designed to offer the designer a choice between two indicator fonts. The SN54249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the '249 circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is not available in the '49 or 'LS49 circuit.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'L46, 'L47, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

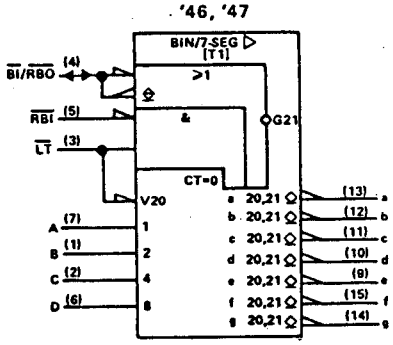
†This wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$).

- All Circuit Types Feature Lamp Intensity Modulation Capability

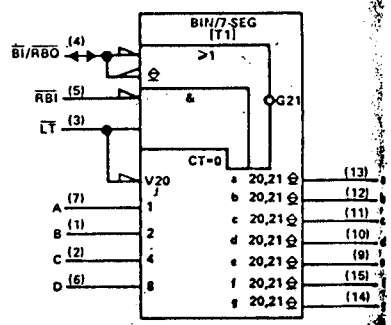
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, W
SN5449	high	open-collector	10 mA	5.5 V	165 mW	W
SN54L46	low	open-collector	20 mA	30 V	160 mW	J
SN54L47	low	open-collector	20 mA	15 V	160 mW	J
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols

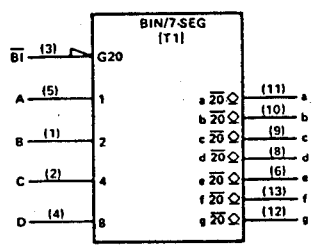
'46, '47



'48



'49



Pin numbers shown on logic notation are for D, J or N packages.