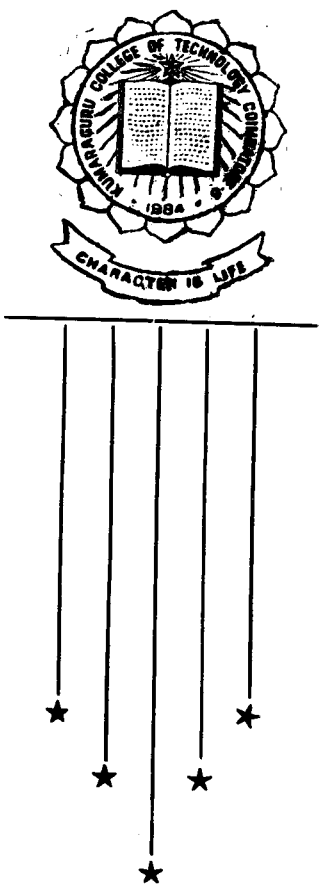
Microprocessor Based Power Factor Measurement and Improvement

Project Report



1997-'98

Submitted in partial fulfilment of the requirements for the award of the Degree of **BACHELOR OF ENGINEERING** in Electrical and Electronics Engineering of the Bharathiar University

Submitted by

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CERTIFICATE

This is to certify that the following students of **KUMARAGURU COLLEGE OF TECHNOLOGY, BHARATHIYAR UNIVERSITY, COIMBATORE** has done project work on **'MICROPROCESSOR BASED POWER FACTOR MEASUREMENT AND IMPROVEMENT'** in our Electrical Department from DECEMBER '97 to MARCH '98 for their partial fulfillment of the requirement for the award of 'Bachelor Degree in ELECTRICAL & ELECTRONICS ENGINEERING'.

Ms. A. G. VANITHA MAHESWARI

Ms. M. VANITHA

Mr. V. KANDASAMY

They have been regular in their attendance during the above period. Their performance and conduct are excellent. We wish them all success.

Place : COIMBATORE

Date : 31.03.98

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We also thank all other associates of m/s ***ELGI EQUIPMENTS*** *also our friends who helped us project both directly and indirectly to do the project .*

We also like to express our heartfelt gratitude to the staff who helped us to complete this project .

We are also grateful to our parents who showered their blessings on us to complete this project in a successful manner.

SYNOPSIS

Power factor of the load in any industry or in any system should be continuously controlled. Electricity board charges penalty for the decrease of power factor below the required value. So continuous control over the power factor becomes a must for any system.

This project provides the provision of measuring the power factor of the system continuously and if the power factor reduces below the required value a set of capacitor banks can be switched ON through the relay circuit automatically and connected across the supply so as to improve the power factor .

The comparison of the power factor of the system and required value are compared using the software designed in the 8085 microprocessor unit based on the signal obtained from the power factor sensing unit.

Power factor of the system is displayed in display unit for every ten seconds. A separate indicating system is also provided to indicate the power factor below the required value.

CONTENTS

CHAPTER - 1

INTRODUCTION

Power factor is the important factor which is to be considered during any electrical operation. Power factor varies with load. E. B. has laid some restriction for this power factor variation. It ranges between 0.90 to 0.98 for industries.

For a constant output motor if the power factor reduces with no change in the voltage the motor draws more current. The Transformers and Cables have to carry this additional amount of current. Thus the Cross sectional area of the Transmission lines should be increased, which leads to increase in cost. Thus in order to avoid these problems the power factor should be maintained within the limit. Failing of which a penalty should be paid by the industry to the supply authority.

The power factor which is determined by the load

drawn by the industry, lags whenever the inductive load goes high and leads whenever the capacitive load goes high.

The power used in KW by the industry is always less than the apparent power KVA.

Thus,

$$KW \ / \ KVA \ = \ power\ factor$$

To utilize most of the energy supplied to the industry, power factor should be high.

The power factor can be increased by the following methods,

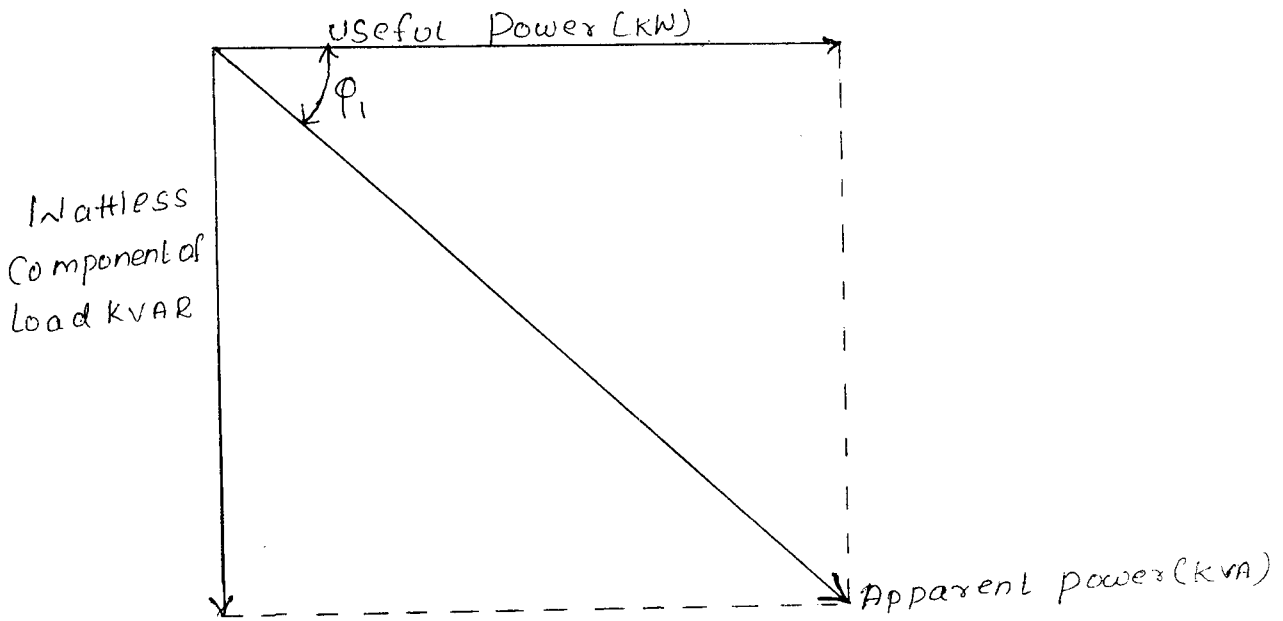
1. *Use of static capacitors.*
2. *By using synchronous compensators or phase modifiers.*
3. *By using phase advancers.*

Among which the first two methods injects a leading current to neutralize the lagging current. The third method

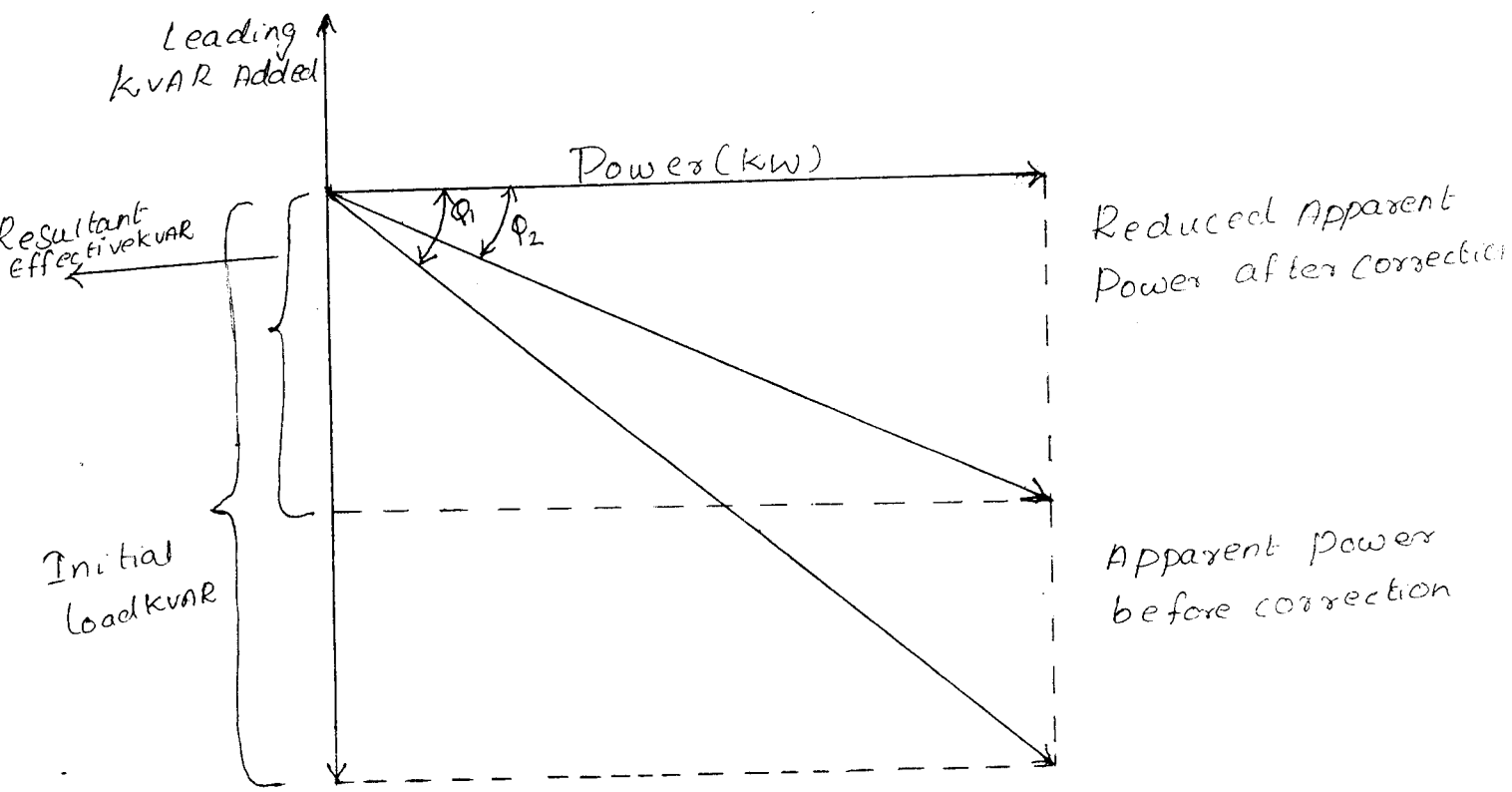
reduces the amount of lag but it doesn't neutralizes the it or cause a lead.

Thus the best method to improve the power factor is to add some leading KVAR to the supply whenever the power factor lags. This can be done by including the capacitor bank to the supply line. Thus the power factor is improved by the magnitude of the KVAR added.

This is clear from the phasor diagram shown in the fig 1.1.



Lagging power factor



Corrected PF by adding Leading KVAR

FIG 1.1 EFFECT OF KVAR ON PF

CHAPTER - 2

GENERAL DESCRIPTION OF THE PROJECT

2.1.Working principle

Our Project injects a leading current (KVAR) to the supply whenever the power factor lags below 0.9 lag. The power factor is sensed and compared with the required limit and correspondingly the capacitor banks are included by switching on the relay connected to the capacitor bank.

The Basic Block Diagram is shown in fig 2.0.

The power factor sensing unit senses the power factor of the supply and gives to the Microprocessor unit in the form of pulses. This unit compares and checks for the limit and gives an output to switch ON or OFF the Relay. This Relay activates the Capacitor bank and includes it to the supply.

This procedure continues repeatedly and the system is in operation for all the 24 hours. The monitored power factor is displayed at equal intervals in the Display unit and the power factor is improved automatically whenever it lags.

2.2.General block diagram

The general block diagram of the project is given in the fig 2.0. The various units in the block diagram is explained below.

2.2.1. Power factor sensing unit

This unit senses the power factor of the supply and converts it in the form of pulses so that it is easy to manipulate. The detailed description of this unit is given in the chapter 3.

2.2.2.Microprocessor unit

This unit with the help of the software designed checks for the desired power factor from the supply and gives out an output signal for the operation of the relay. The detailed description is given in the chapters 4 & 5.

2.2.3. Relay

The relay part helps in including the capacitor from the capacitor bank across the supply . The description of this unit is given in the chapter 7 .

2.2.4.Capacitor bank

This unit contains the capacitors of different KVAR rating which is included across the supply to improve the power factor whenever necessary . The unit is explained in chapter 7 .

2.2.5.Display unit

This unit indicates the monitored power factor at equal intervals for easy noticing . The unit is explained in the chapter 5.

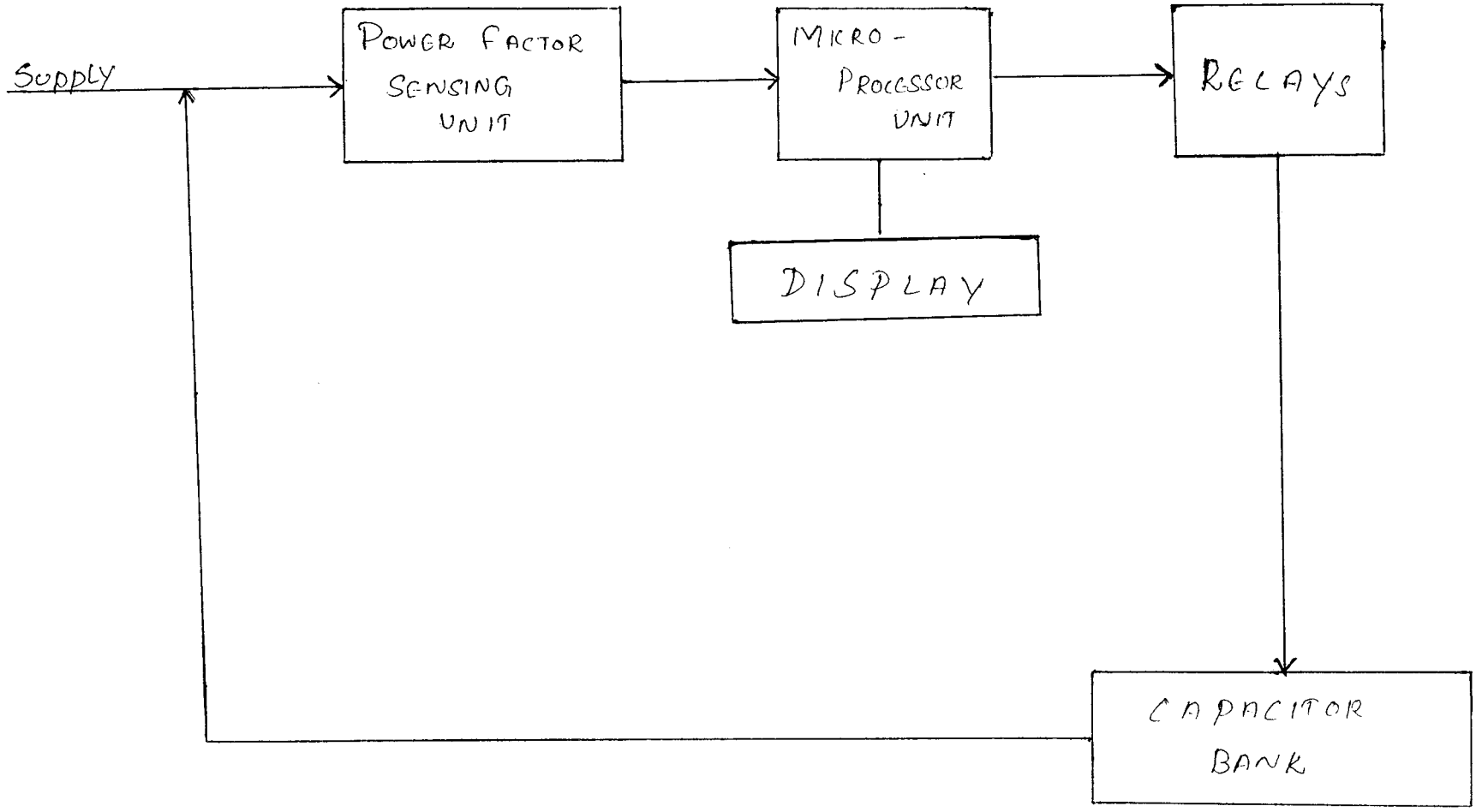


Fig 2.0 Block Diagram of P.F Controller

CHAPTER - 3

POWER FACTOR SENSING UNIT

This unit is the root of the project. The main factor, power factor, which is to controlled is sensed by this unit. This unit converts the power factor in a form of pulses which can be used for further processing.

The circuit is shown in fig 3.1.

For the conversion of the power factor to pulses the first to be done is to step down the supply value to a value that can be used by the ICs . The Power factor is nothing but the phase difference between the voltage and current. Thus to measure the power factor the voltage and current signals are obtained separately by using voltage and current transformers respectively.

CURRENT TRANSFORMER :

The Current Transformer is used with its primary winding connected in series with line carrying the current that is to be stepped down . Thus , the primary current is dependent upon the load connected to the system and is not determined by the load connected to the secondary of the current transformers . The primary winding consists of very few turns , and therefore there is no appreciable voltage drop across it . The secondary winding of the current transformer has larger number of turns , the exact number being determined by the turns ratio . Thus the stepped down current signals are obtained at the secondary .

The fig 3.2. gives the details about the connection of the current transformer to the supply and about the output terminals .

The rating of the current transformer used here is 75A / 5

POTENTIAL TRANSFORMER :

The potential transformers are used to step down the supply

voltage. The primary winding of the transformer is connected across the line carrying the voltage to be stepped down and the voltage circuit is connected across the secondary winding. The loading of a potential transformer is always small, sometimes only a few volt-ampere.

The rating of potential transformer used here is 230V / 5V

Next to the transformer section comes the Conversion section which converts the incoming current and voltage signals to pulses. For this purpose the IC 741 Comparator is used to whose reference input is zero thus it acts as a zero crossing detector.

The IC 741 is an Operational amplifier. In this case it is operated in open loop configuration in a non-linear manner. In this mode it works as a comparator.

A comparator is a circuit which compares a signal voltage applied at one input of an operational amplifier with a known reference voltage at the other input. It is basically an open loop operational amplifier with output +Vsat 0r -Vsat (Vcc).

The characteristics shown in fig 3.4 *are the ideal transfer characteristics and commercial operational amplifier transfer characteristics of practical comparators respectively. There are basically 2 types of comparators,*

1. *Non-Inverting comparator*
2. *Inverting comparator*

The type of comparator used here is the Non-Inverting comparator. The 10Kohms potentiometer is used to obtain the Vref practically. It is applied to the Non-Inverting terminal of the operational amplifier. A practical Inverting comparator and its corresponding input and output waveforms for Vref > 0 and Vref < 0 are given in fig 3.5.

As Vi in this circuit is zero the input and output wave forms are given in fig 3.6.

Next to this conversion section the two outputs of the voltage and current wave forms in pulse form is given to the X-OR gate

The IC has 4 X-OR gates within a single chip. Among

which we use only one set. It has two input terminals to which pulses ranging within 5V are given. The output from the gate depends upon the inputs given. The Truth Table is as given.

$$F = XY' + X'Y$$

X	Y	F
L	L	L
L	H	H
H	L	H
H	H	L

Thus the output will be high whenever the two inputs are at opposite levels. Thus the output of the X-OR gate will be the difference between the current and voltage pulses at its input. Thus the output pulse width from the X-OR gate is proportional to power factor.

Thus the pulse whose width is proportional to the power factor is the output of this whole section which is given as the input to the next section which is the Microprocessor unit.

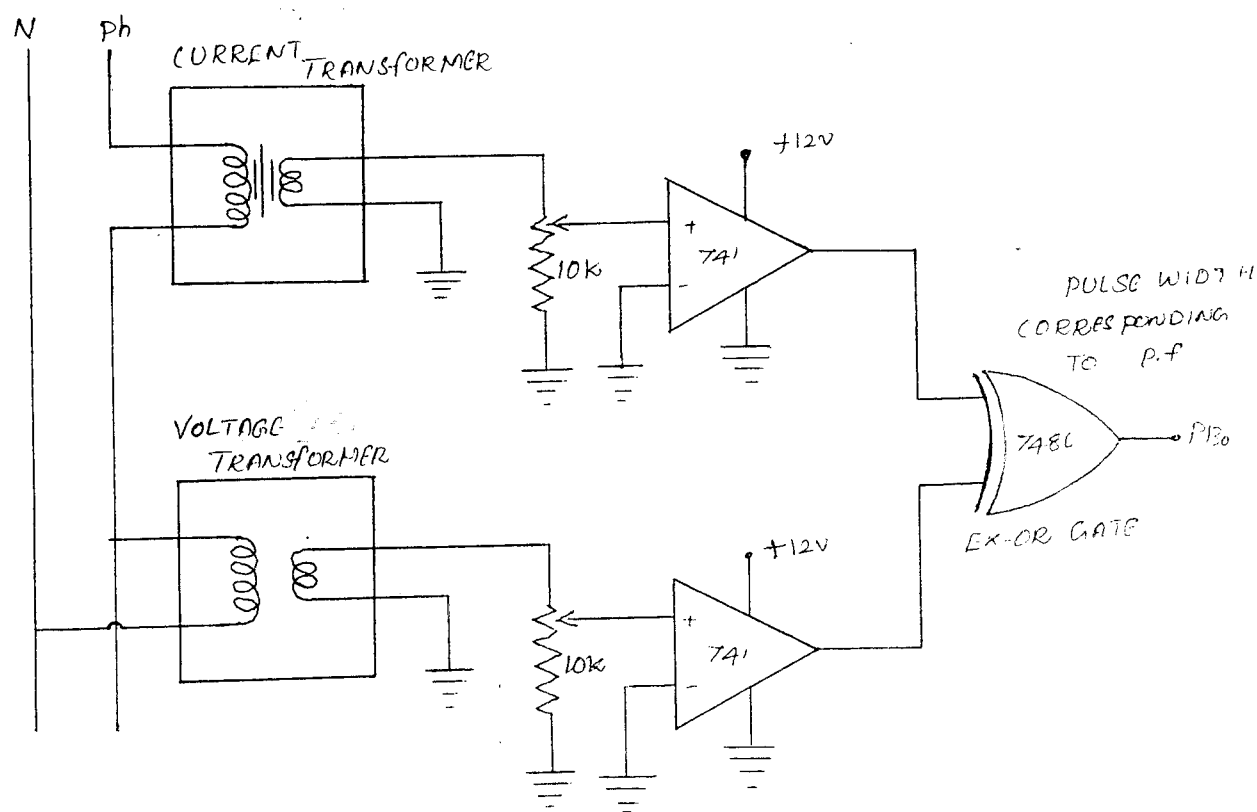


FIG. 3.1 POWER FACTOR SENSING UNIT

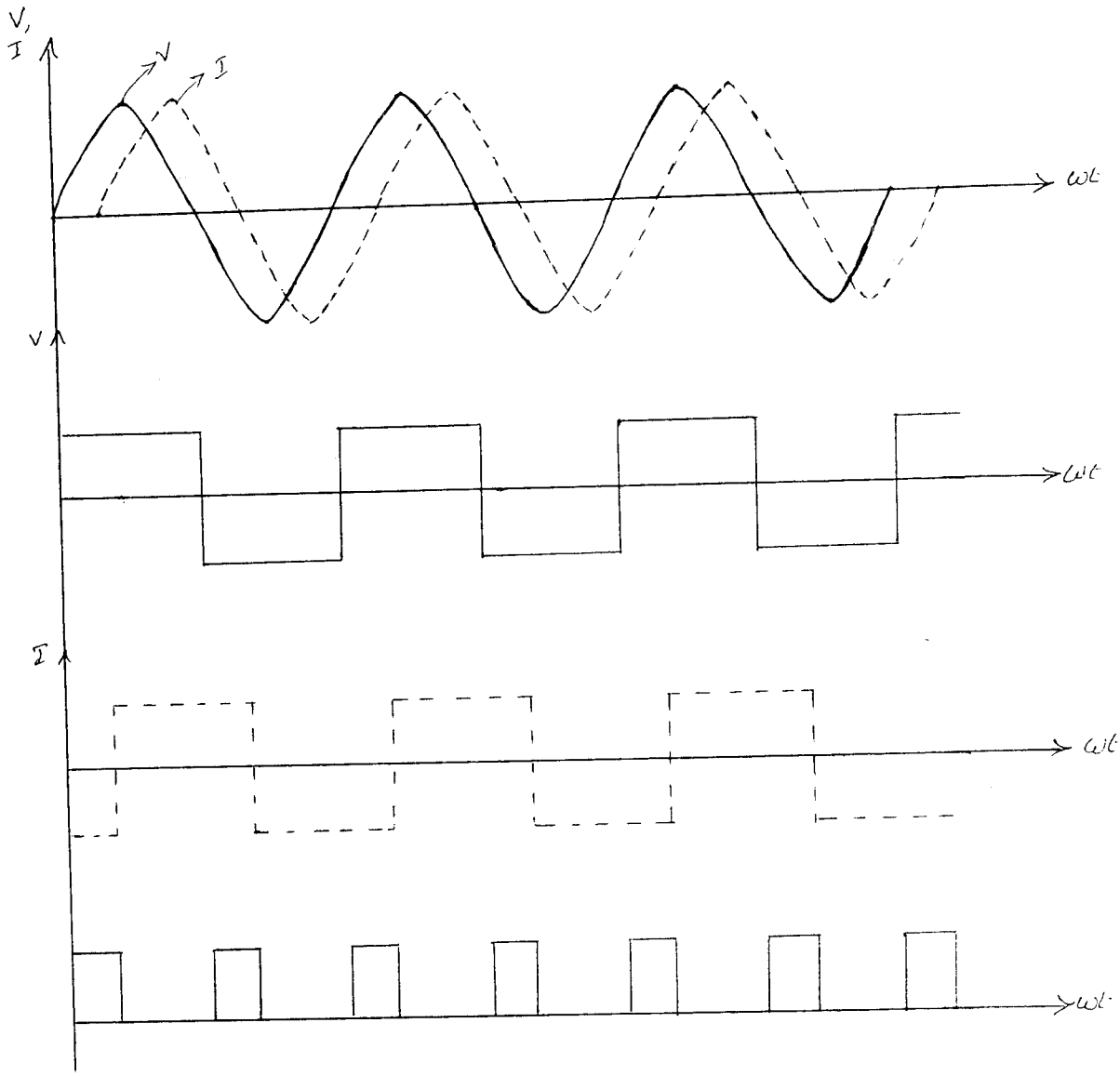
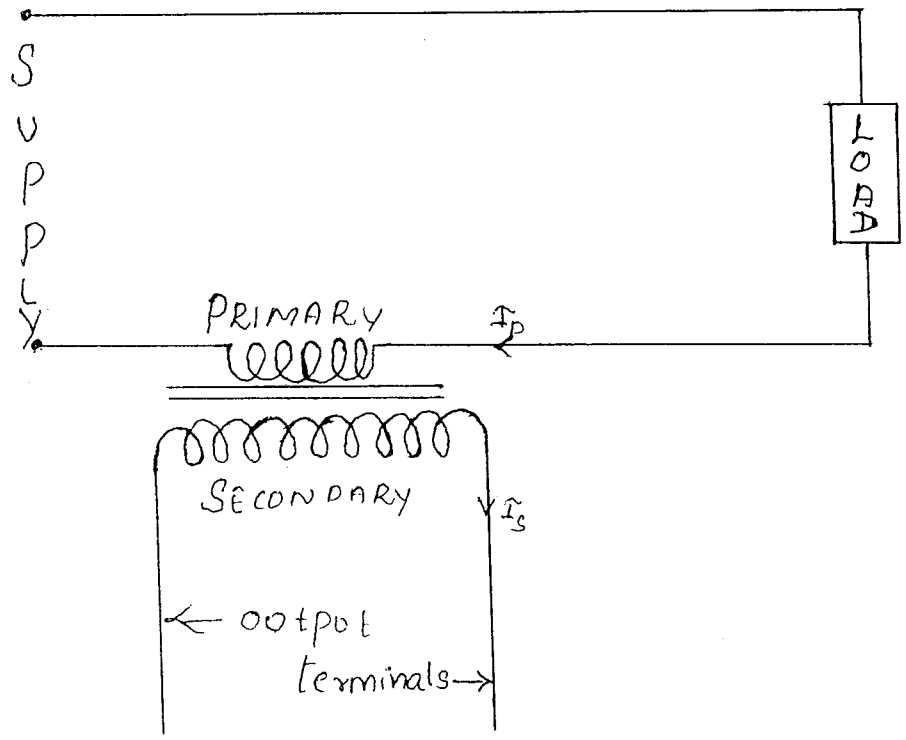
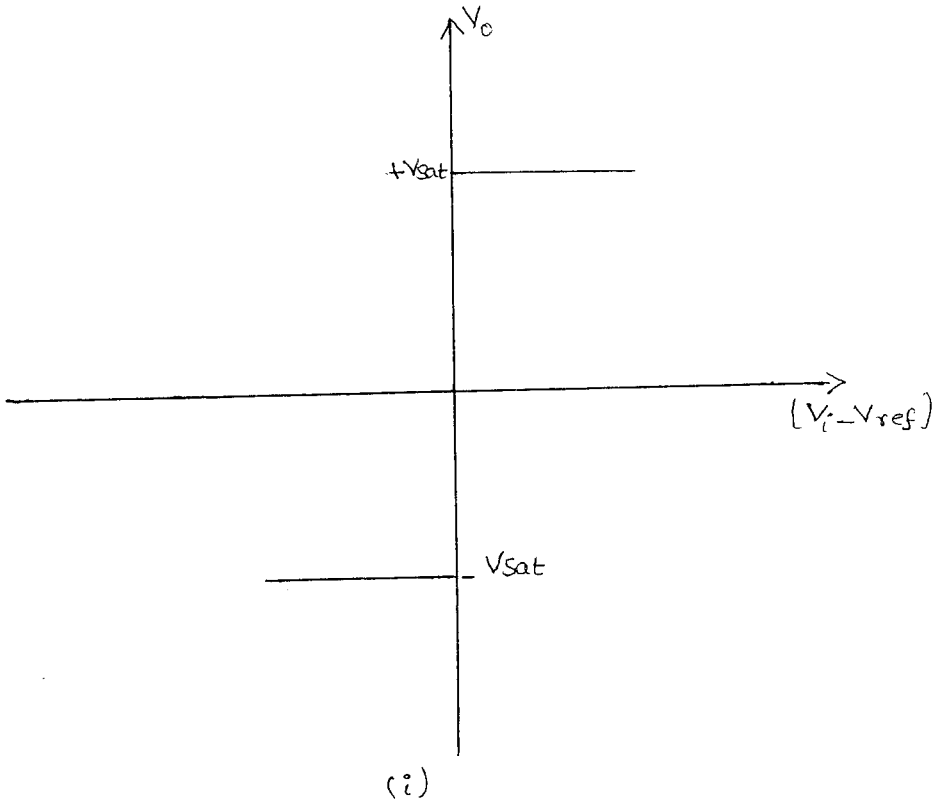


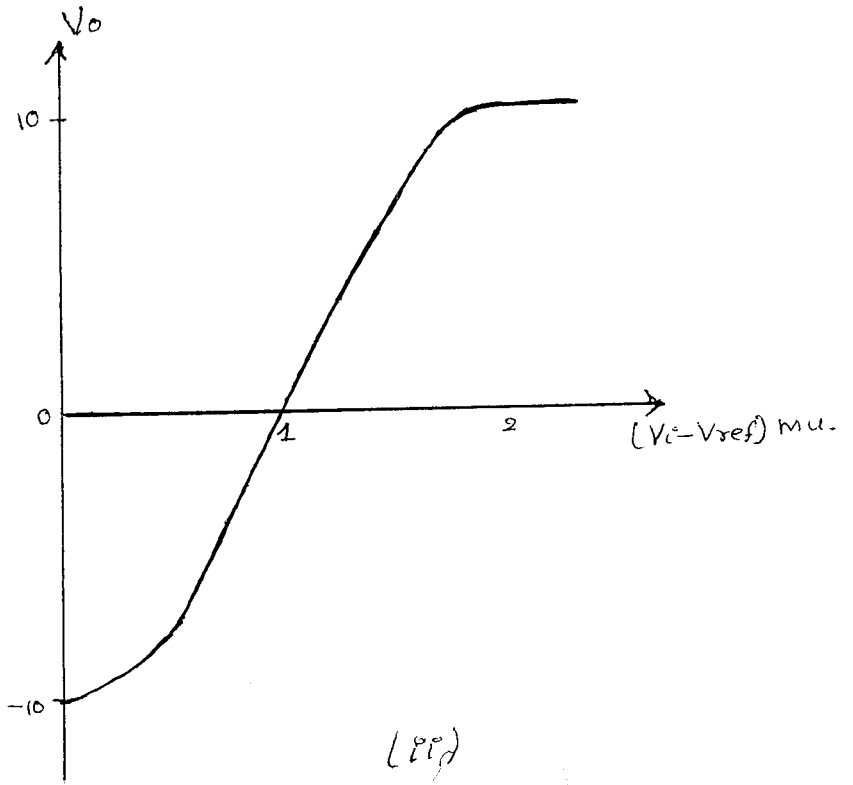
FIG 3.1 INPUT AND OUTPUT WAVEFORMS



3.2. CONNECTION OF CT TO THE SUPPLY

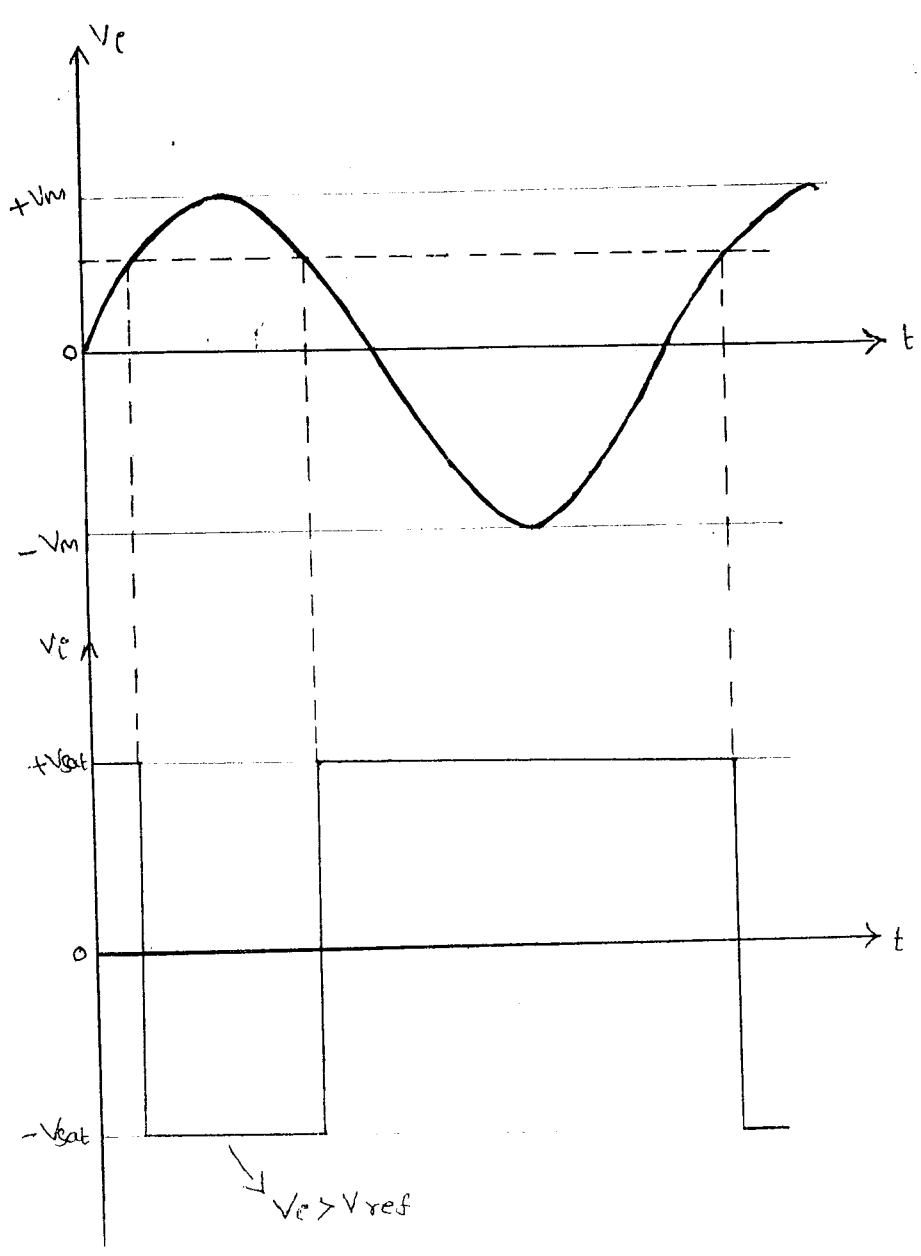


(i)

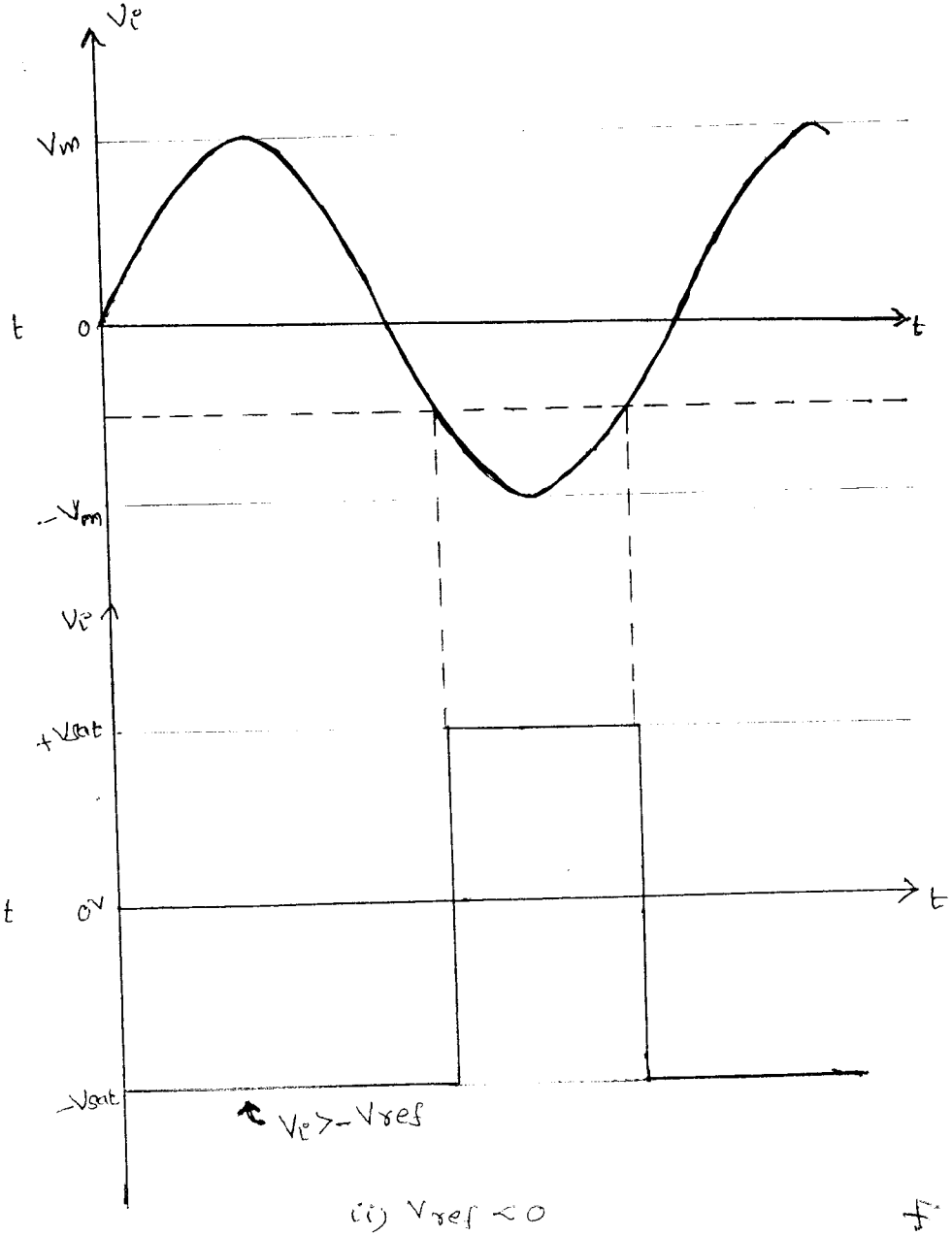


(ii)

FIG 3.4. IDEAL AND PRACTICAL COMPARATOR CHACTERISTICS

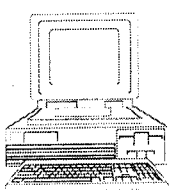


i) $V_{ref} > 0$

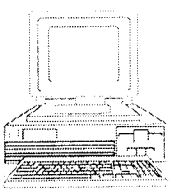


ii) $V_{ref} < 0$

FIG 3.6. INPUT & OUTPUT WAVEFORMS OF NI COMPARATOR



Microprocessor based design



CHAPTER - 4

MICROPROCESSOR BASED DESIGN

The 8085 is an 8-bit general purpose micro processor capable of addressing 64K of memory. The device has 40 pins, requires a +5V single power supply, and can operate with a 3MHz single phase clock. The 8085 is an enhanced version of its predecessor, the 8080A; Its instruction set is upward-compatible with that of the 8080A, meaning that the 8085 instruction set includes all the 8080A instructions plus some additional ones. Programs written for the 8080A will be executed by the 8085, but the 8085 & 8080A are not pin compatible.

4.1. INTRODUCTION

Supply	*Single +5V power supply with 10% voltage margins*
Clock time	*3MHz,5MHz & 6MHz selections available. 1.3micro second instruction cycle (8085AH); 0.8micro second (8085AH-2); 0.67micro second (8085AH-1). On chip clock generator.*

ALU	*Decimal , Binary & Double Precision Arithmetic .*
Memory	*Direct Addressing capability of 64KB of memory .*
Interrupts	*4 vectored interrupt inputs (one is non maskable) plus an 8080A compatible interrupts .*
Ports	*Serial In / Serial Out ports .*

4.2. HARDWARE FEATURES

The central processing unit is the group of circuit that processes data and provides control signals and timing . It includes the Arithmetic logic unit , Registers , Instruction decoder , and a control unit .

Registers

The 8085 has 6 general purpose registers to performs the operation of storing data during program execution .These registers are identified as B,C,D,E,H&L as shown in fig 4.1. *They can be combined as register pairs - BC , DE & HL - to perform some 16-bit operations .*

These registers are programmable, meaning that a programmer can use them to load or transfer data from the registers by using instructions. conceptually, the registers can be viewed as memory locations, except they are built inside the microprocessor and identified by specific names.

Accumulator

The accumulator is 8-bit register that is part of the ALU. This register is used to store 8-bit data and to perform arithmetic & logical operations. The result of an operation is stored in the ACC. The accumulator is also identified as register A.

Flags

The ALU includes 5 flip-flops that are set or reset according to the data conditions in the accumulator and other registers The Microprocessor uses them to perform the operation of testing for data conditions.

The 8085 has 5 flags to indicate 5 different types of data

conditions . They are called zero(Z) , carry(CY) , sign (S) , parity(P) & auxiliary carry (AC) flags . The most commonly used flags are Z & CY .

An 8-bit register , called the flag register is adjacent to the accumulator . It is not really a register ; 5-bit positions, out of 8 , are used to store the outputs of the 5 flip-flops . The flags are stored in the 8-bit register so that the programmer can examine these flags (data conditions) by accessing the register through an instruction . In the instruction set , the term PSW (Program Status Word) refers to the accumulator and flag register .

These flags have critical importance in the decision makin process of the microprocessor . The conditions (Set or Reset) of the flags are tested through software instructions. The bit positions occupied by these flags are as given below

D7	D6	D5	D4	D3	D2	D1	D0
S	**Z**		**AC**		**P**		**CY**

Program Counter

This 16-bit register deals with the operation of sequencing the execution of instructions. This register is a memory pointer. Memory locations have 16-bit address hence it is a 16-bit register.

The Microprocessor uses this register to sequence the execution of instructions. The function of the PC is to point to the memory address from which the next byte is to be fetched. When a byte (Machine Code) is being fetched the PC is incremented by 1 to point to the next memory location.

Stack Pointer (SP)

The Stack Pointer is also a 16-bit register used as a memory pointer; initially, it will be called the SP to emphasize that it is a register. It points to a memory location in R / W memory, called the stack. The beginning of the stack is defined by loading a 16-bit address in the SP (register).

STACK

The stack in an 8085 Microcomputer system can be described as a set of memory locations in the R/W memory, specified by a programmer in a main program. These memory locations are used to store binary information (bytes) temporarily during the execution of the program.

MICROPROCESSOR

The Microprocessor includes all the logic circuitry (including the control unit) on one chip. The microprocessor can be divided into 3 segments as shown in figure 4.2: Arithmetic / Logic unit (ALU), Register unit, and control unit.

ALU

In this area of the microprocessor, computing functions are performed on data. The ALU performs Arithmetic operations such as additions and subtraction, and logic operations such as AND, OR and X-OR. Results are stored either in register or in memory or sent to output devices.

Register unit

This area of the microprocessor consists of various registers. The registers are used primarily to store data temporarily during the execution of a program. Some of the registers are accessible to the user through instructions.

Control unit

The control unit provides the necessary timings and control signals to all the operations in the microcomputer. It controls the flow of data between the microprocessor and peripherals (including memory).

4.3. INTERRUPTS

The 8085 has 5 interrupt signals that can be used to interrupt a program execution. Some of the signals are INTR (Interrupt Request), $\overline{INTA}$ (Interrupt Acknowledge).

INTR (Input) : This is used as a general purpose interrupt.

$\overline{INTA}$ (output) : This is used to acknowledge an interrupt.

TRAP (Input) : This an non-maskable interrupt and has the highest priority .

The interrupt I / O is the process of data transfer where by an external device or a peripheral can inform the processor that it is ready for communication and its requests attention . The process is initiated by an external device and is asynchronous , meaning that it can be initiated at any time without reference to the system clock . However , the response to an interrupt request is directed or controlled by the microprocessor .

The interrupt request are classified in two categories : Maskable and Non-Maskable interrupts . A Maskable interrupt request can be ignored or delayed by the microprocessor if it is performing some critical tasks ; however , the microprocessor has to respond to a non-maskable request immediately .

The interrupt process allows the microprocessor to respond to these external requests for attention or service on a demand basis a

leaves the microprocessor free to perform other tasks .

4.4. PORTS

The 8085 has two signals to implement the serial transmission : SID (Serial Input Data) and SOD (Serial Output Data) .

BUS DETAILS

The 8085 MPU performs all functions using three sets of communication lines called buses : the Address bus , Data bus & control bus . These buses are combinely called as system bus .

Address bus

The address bus is a group of 16 lines generally identified as A0 - A15 . This bus is unidirectional : bits flow in one direction - from the MPU to Peripheral devices . The MPU uses the address bus to perform the operation of identifying the peripheral or the memory location .

Data bus

The data bus is a group of 8 lines used for data flow. These lines are bi-directional: data flows in both directions between the MPU & Peripheral devices. The MPU uses the data bus to perform the operation of data transfer.

Control bus

The control bus is comprised of various single lines that carry synchronization signals. The MPU such lines to provide timing or synchronization signals.

CHAPTER - 5

MICRO PROCESSOR INTERFACING & DISPLAY UNIT

The microprocessor unit is the heart of this project. It performs almost all important functions of this setup. The unit compare the current power factor with the desired power factor and gives out signals to the relays either to switch it ON or OFF.

The microprocessor is a programmable logic device, designed with registers, flip-flops and timing elements. The micro processor has a set of instructions designed internally, to manipulate data and communicate with peripherals.

The microprocessor along with the Interfacing units are given in fig 5.1.

5.1.8085 unit

The 8085 is an 8-bit general purpose microprocessor

capable of addressing 64K of memory. The device has 40 pins, requires a +5V single power supply, and can operate with a 3MHz single phase clock.

The hardware details of the 8085 microprocessor is already explained in the previous chapter.

5.2. INTERFACING UNIT

The primary function of the microprocessor is to accept data from input devices such as keyboards and A / D converters, read instructions from memory, process data according to the instructions, and send the results to output devices such as LEDs, Printers and video monitors. These input and output devices are called either peripherals or I / O devices; memory can be viewed as a special type of I / O. Designing logic circuits and writing instructions to enable the microprocessor to communicate with these peripherals is called ***Interfacing*** *and the logic circuits are called interfacing devices.*

5.2.1.Programmable Interface

The 8155 is a multipurpose programmable device specifically designed to be compatible with the 8085 microprocessor. Some signals from the 8085 can be connected directly to these device. The 8155 includes 256 bytes of R / W memory, 3 I / O ports & a Timer.

The 8155 is a device with 2 sections : the first is 256 bytes of R / W memory, second is a Programmable I / O. Functionally, these 2 sections can be viewed as 2 independent chips. The I / O section includes 2 eight-bits parallel I / O ports (A & B), one 6-bit port [C and a timer. All the ports can be configured simply as I / O ports. The ports A & B also can be programmed in the handshake mode, each port using 3 signals as handshake signals from port C. The Timer is a 14-bit down counter and has 4 modes.

The control logic of the 8155 is specifically designed to eliminate the need for externally demultiplexing lines AD7 - AD0 and

generating separate control signals for memory and I/O. The fig 5.3. shows 5 control signals ; all except the chip enable are input signals directly generated by the 8085.

$\overline{CE}$ (Chip Enable) : This is a master chip select signal connected to th decoder high-order bus.

$IO/\overline{M}$: When this signal is low, the memory section is selected, and when it is high, the I/O section (including Timer) is selected.

ALE (Address Latch Enable): This signal latches the low-order address AD7 - AD0, $\overline{CE}$ and $IO/\overline{M}$ into the chip.

$\overline{RD}$ and $\overline{WR}$: These are control signals to read from and write into the chip registers and memory.

RESET : This is connected to the RESET OUT of the 8085 and this resets the chip and initializes I/O ports as input.

To communicate with peripherals through the 8155 the following steps are necessary :

1. *Determine the addresses (Port numbers of the registers and I / O s) based on the chip enable logic and address lines AD0 , AD1 & AD*
2. *Write a control word in the control register to specify I / O functions of the ports and the Timer characteristics .*
3. *Write I / O instructions to port addresses to communicate with peripherals.*
4. *Read the status register , if necessary , to verify the status of the I / O ports and the Timer .*

The I / O Ports and the Timer can be configured by writing a control word in the control register . The control register bits are defined as shown below.

In this control word , outputs are defined with logic 1 & Inputs with logic 0 . The first 2 LSBs , D0 & D1 , determine I / O function of ports A & B ; and the MSBs , D7 & D6 , determines Timer functions .Bit D2 & D3 determines the functions of port C ; and their combinations specifies one of the four alternatives , from simple I / O to interrupt

I / O , as shown in the figure . Bits D4 & D5 are used only in the interrupt mode to enable or disable internal flip-flops of 8155 . These bits do not have any effect on the interrupt enable flip-flop (INTE) of the MPU .

D7 & D6 ---------- *TIMER COMMANDS*

00 = NOP - no effect on timer

01 = stop - stop counting if timer is running ; else no effect on timer

10 = stop after TC (Terminal Count) - stop after at en of the count if timer is running ;else no effec on timer

11 = start - start timer if it is not running - if timer i running , stop at end of the count . Reload new mode and count , and start again

D5 ---------- IEB = Interrupt Enable Port B , 1 – Enable & 0 – Disable

D4 ---------- IEA = Interrupt Enable Port A , 1 – Enable & 0 – Disable

D3 & D2 --------- *PORT C*

00 = ALT 1
11 = ALT 2
01 = ALT 3
10 = ALT 4

D1 ---------- Port B , 0 = Input , 1 = Output

D0 ---------- Port A , 0 = Input , 1 = Output

ALT	*D3*	*D2*	*PC5*	*PC4*	*PC3*	*PC2*	*PC1*	*PC0*
ALT1	*0*	*0*	*I*	*I*	*I*	*I*	*I*	*I*
ALT2	*1*	*1*	*O*	*O*	*O*	*O*	*O*	*O*
ALT3	*0*	*1*	*O*	*O*	*O*	*STBA*	*BFA*	*INTRA*
ALT4	*1*	*0*	*STBB*	*BFB*	*INTRB*	*STBA*	*BFA*	*INTRA*

I = Input
O = output
STB = Strobe
BF = Buffer Full
Subscript A = Port A
Subscript B = Port B
INTR = Interrupt Request

5.2.2. Latch

In its simplest form , a latch is a D Flip - Flop . Two types of D flip-flop are available , as shown in fig 5.5 ; a transparent latch

when the clock signal is high , the output Q changes according to the input D . When a clock signal goes low , the output Q will latch (hold) the last value of the input D (figure C) .

A latch is used commonly to interface output devices . When the MPU sends an output , data are available on data bus for only a few microseconds , and therefore , a latch is used to hold data for display . The Transparent latch used here is 74LS373 . The function table is given below

Output control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

This octal latch is suitable to latch 8-bit data . The devices include 8 D latches with Tri-state buffers . They require 2 input signals ,Enable (E) and Output Enable ($\overline{OE}$) control gates

The data on the D inputs are transferred to the latch outputs when the latch enable (E) input is high. The latch remains transparent to the data inputs while E is high, and stores data present one set-up time before the high - to - low enable transition. The enable gate has hysteresis built-in to help minimize problems that signal and ground noise can cause on the latch operation.

The Tri-state output buffers are designed to drive heavily loaded Tri-state buses, MOS memories, or MOS microprocessor The active low output enable controls all 8 Tri-state buffers independent of the latch operation. When Output Enable is low, the latched or transparent data appears at the outputs. When Output Enable is high, the outputs are in the high impedance " OFF " state, which means they will neither drive nor load the bus.

5.2.3. EPROM

The information stored in this memory is semi-permanent. All information can be erased by exposing the memory to ultra-violet

light through a quartz window installed on the chip. Then the memory chip can be reprogrammed again and again. This memory is commonly used in product development and experimental projects.

Like the R / W memory chip, the EPROM also has 256 bytes of memory and requires eight address lines, A7 - A0, to identify 256 locations. Its mapping ranges between 0000 - 00FF, as shown belo

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000H
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	= 00FF

This memory chip requires the control signal $\overline{MEMR}$. The figure 4.7. shows the logic diagram of 2716. It is a 2048 8 memory chip with two control signals :

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$).

It requires 11 address lines (A10 - A0), and the $\overline{RD}$ signal to enable the output buffers. The Vpp pin should be connected to +25V during the programming mode; otherwise, it is connected to +5V.

The 2716, with its single 5V supply and with an access time up to 350 nano seconds, is ideal for use with the newer hig performance +5V microprocessor such as INTEL 8085.

5.2.4. Decoder

The decoder is a logic circuit that identifies each combination of the signals present at its input. The fig 5.8. shows the symbolic representation for a hypothetical 3-to-8 decoder. The decoder is a commonly used device in interfacing I/O peripherals or memory. The decoders are built also internally to a memory chip to identify individual memory locations.

The fig 5.9. shows the diagram of 74138. It is also called 1-out-of-8 binary decoders or demultiplexers. The 74LS138 has thre input lines and active low output lines. It requires 3 enable inputs : 2

are active low and one is active high ; these 3 enable inputs are ANDed together internally , generating a single enable signal for the decoder . Thus all 3 enable lines should be activated so that the device can function as a decoder .

The 74138 decoder accepts 3 binary weighted inputs (A0 , A1 ,A2) and when enabled , provides 8 mutually exclusive , active-lo outputs ($\overline{0}$ - $\overline{7}$) . The device features 3 enable inputs : 2 active low ($\overline{E1}$, $\overline{E2}$ and one active high (E3) . Every output will be high unless $\overline{E1}$ & E2 a low and E3 is high . This multiple enable function allows easy parallel expansion of the device to a 1 - of - 32 (5 lines to 32 lines) decoder with just four 74138s and 1 inverter .

The device can be used as an 8 output demultiplexer by using one of the active low enable inputs as the data input and the remaining enable inputs as strobes . Enable inputs not used must be permanently tied to their approximate active high or active low state

5.2.4. RAM

The RAM is a Read / Write (R / W) memory also known a user memory. It is used to store user programs and data in single board microcomputers, in which instructions and data are entered through a HEX Keyboard, the monitor program monitors the keys and stores those instructions and data in the R / W memory. This informatio stored in this memory can be read and altered easily.

The RAM is made of registers and each register has a group flip-flops that stores bits of information. The number of bits stored in the register is called a ***memory word****; memory devices (chips) are available in various word sizes. The MPU can read from or write into this memory.*

To read from or write into a memory location the microprocessor places the address on the address bus. The decoder decodes the address and identifies the register. The control signal $R / \overline{W}$

enables the I/O lines the one also known as Chip Enable ($\overline{CE}$), is. necessary to select one particular memory chip from among several memory chips in a system.

The RAM used here is HM6116. The special features of this type of RAM are

Single 5 V Supply and High Density 24 pin package

High speed : fast access time — *120 ns / 150 ns / 200 ns (max)*

Low power standby and — *Standby : 100 micro watts (typ)*

Low power operation — *Operation : 180mW (typ)*

Completely static RAM : no clock or timings strobe required

Directly TTL compatible : All input and output

Pin output compatible with standard 16K EPROM / MASK ROM

Equal access and cycle time

5.3. DISPLAY UNIT

This unit gives an output for the manual viewers in digital

displayed by this unit in digital form in the seven segment LED display interfaced with the 8085 chip. This unit receives its input signal from the programmable interface 8155.

5.3.1. *Seven Segment LED*

A seven segment LED consist of 7 Light Emitting Diode segments and one segment for the decimal point. These LEDs are arranged as shown in fig 5.11. To display a number, the necessary segments are lit by sending an approximate signal for current flow through diodes.

Seven segment LEDs are available in 2 types: Common Cathode and Common Anode. They can be represented schematically as in figure 5.12. Current flow in these diodes should be limited to 20mA.

The seven segments, A through G, are usually connected to data lines D0 through D6, respectively. If the decimal point segment is being used, data line D7 is connected to DP, otherwise it is left ope The binary code required to display a digit is determined by the type of the seven segment LED, the connections of the data lines, and the logic required to light the segment.

5.3.2. BCD - to - Seven Segment decoder

A BCD - to - Seven Segment Decoder is a type of decoder which decodes the BCD input to codes (Seven Segment) and sends to the Seven Segment display unit for manual understanding. The type used here is the 7447 IC. This IC accepts 4 lines of BCD (8421) input data, generates their compliments internally and decodes the data with seven segment AND / OR gates having open collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40mA in the ON (low) state and with stand 15V in the OFF(high) state within a maximum leakage current of 250microA The Hardware Design of the microprocessor unit is given in fig 5.14.

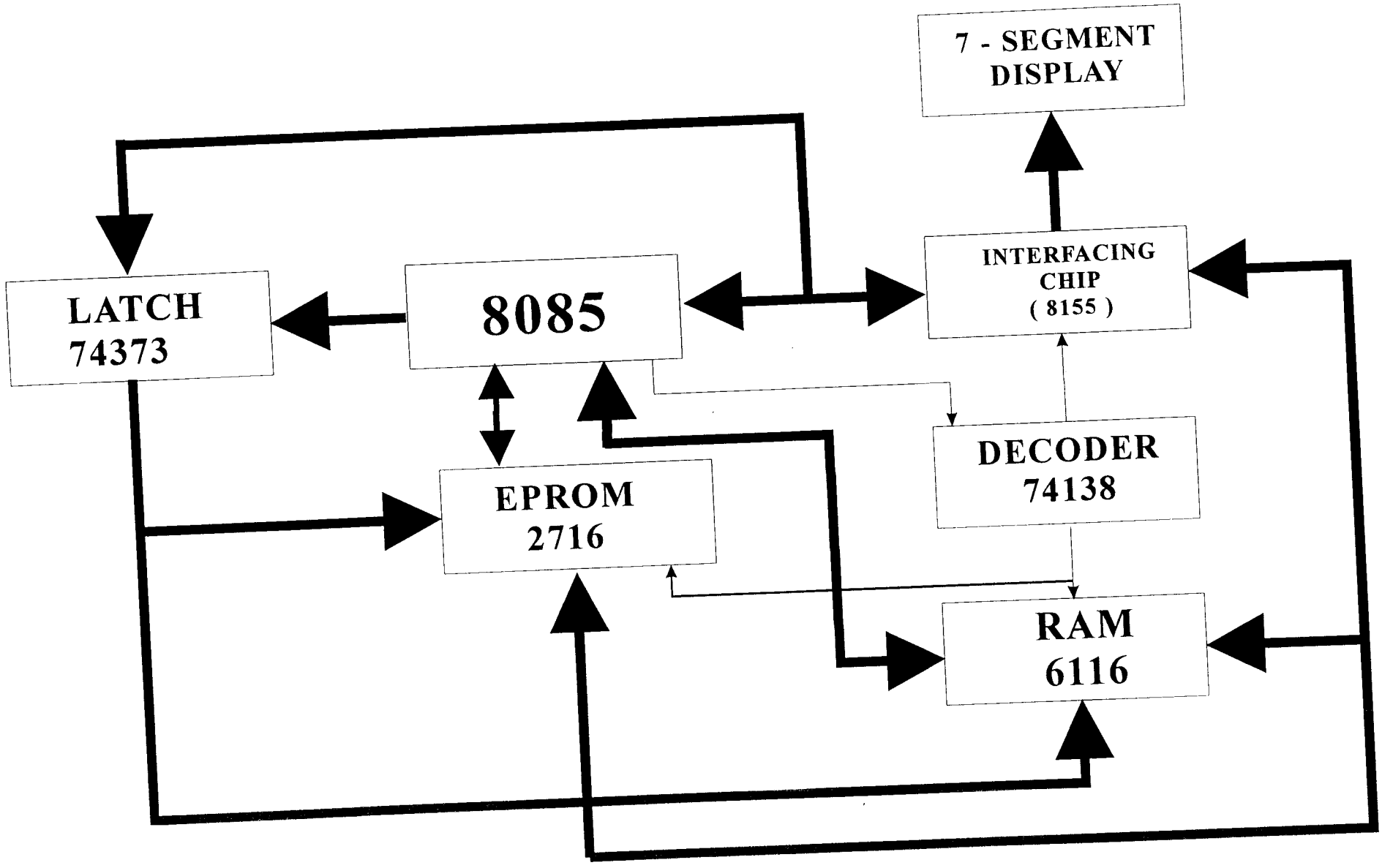


FIG : 5.1 INTERFACING UNITS WITH MICROPROCESSOR 8085

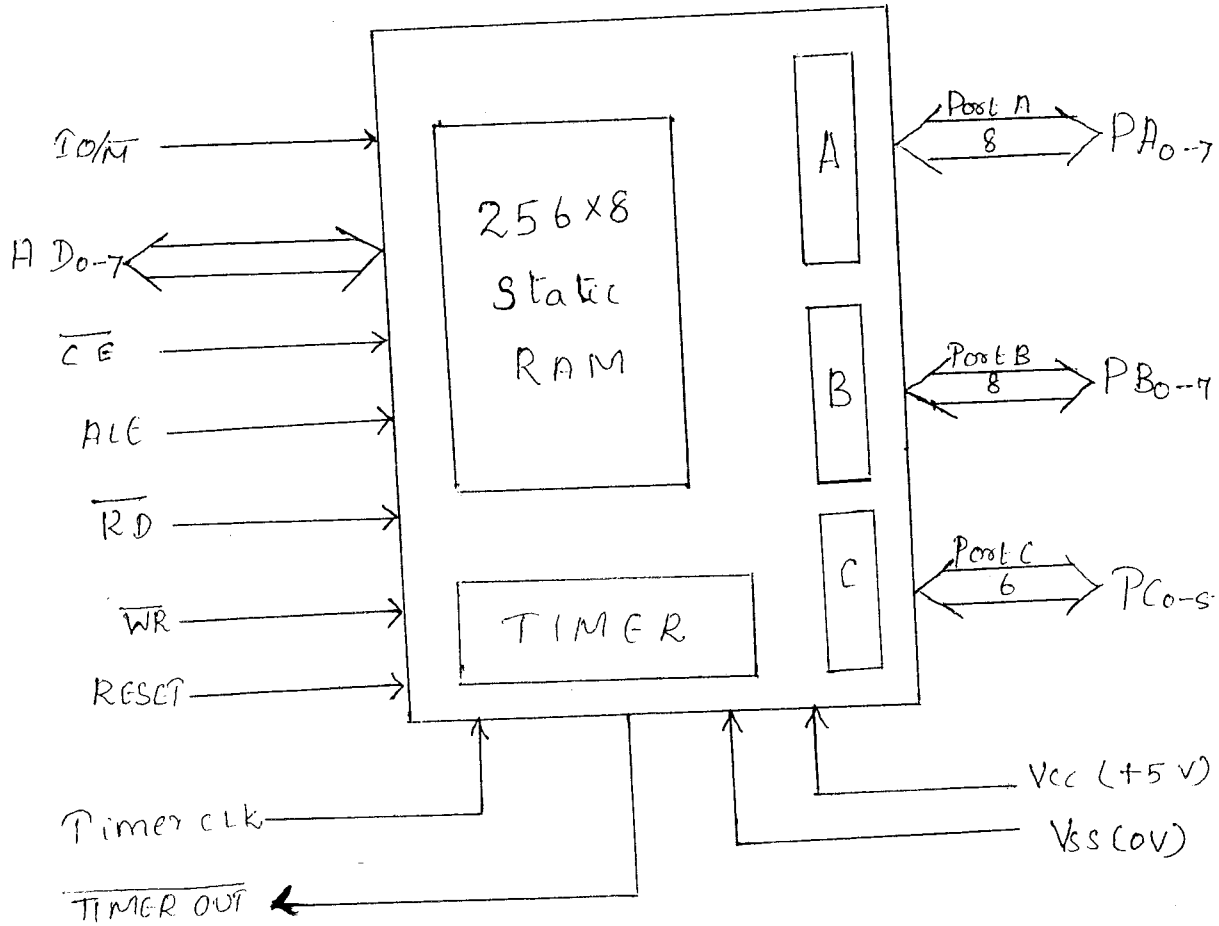


FIG 5.3 BLOCK DIAGRAM of 8155

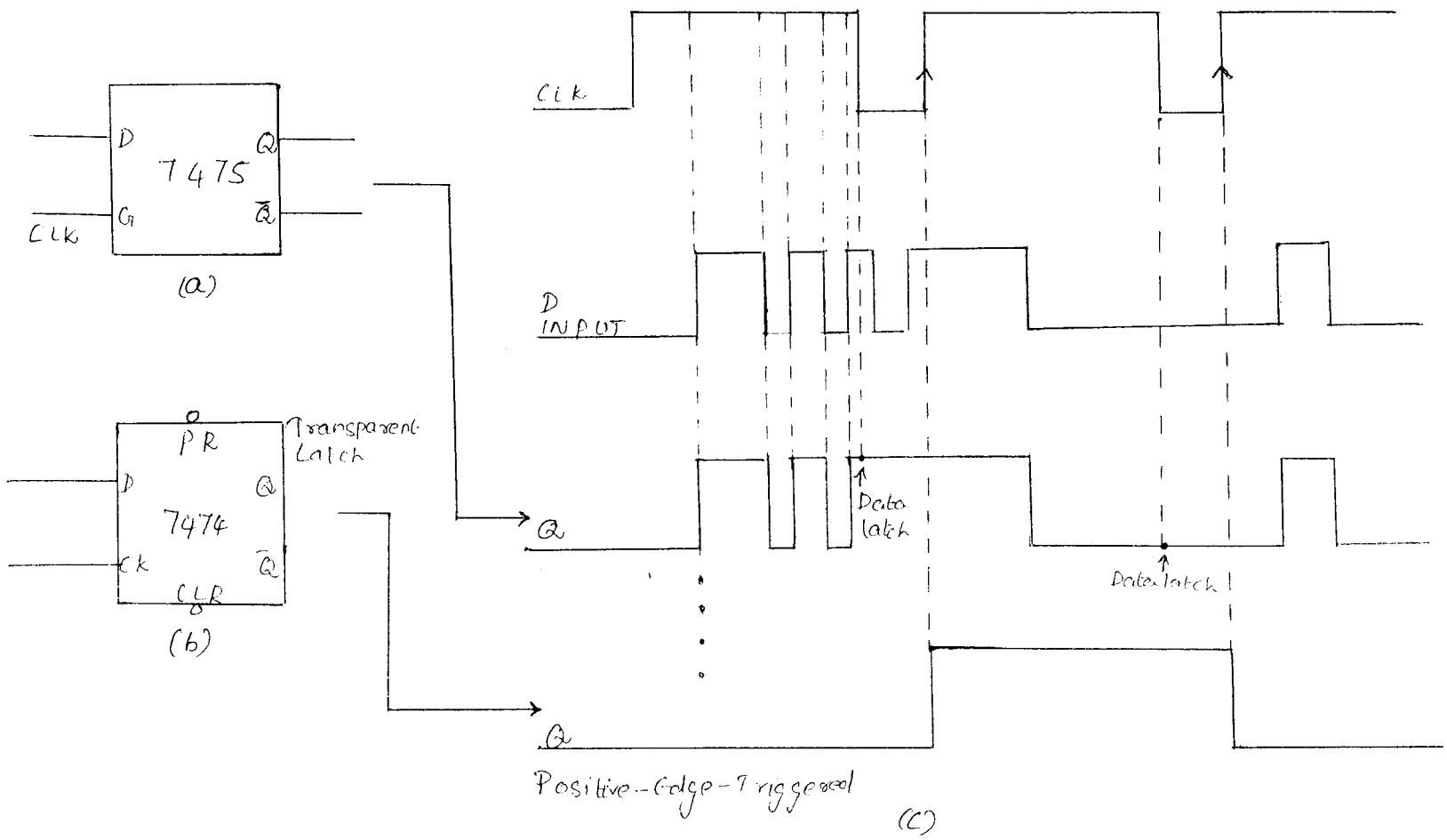


FIG: 5.3 D flip-flops and Output Waveforms

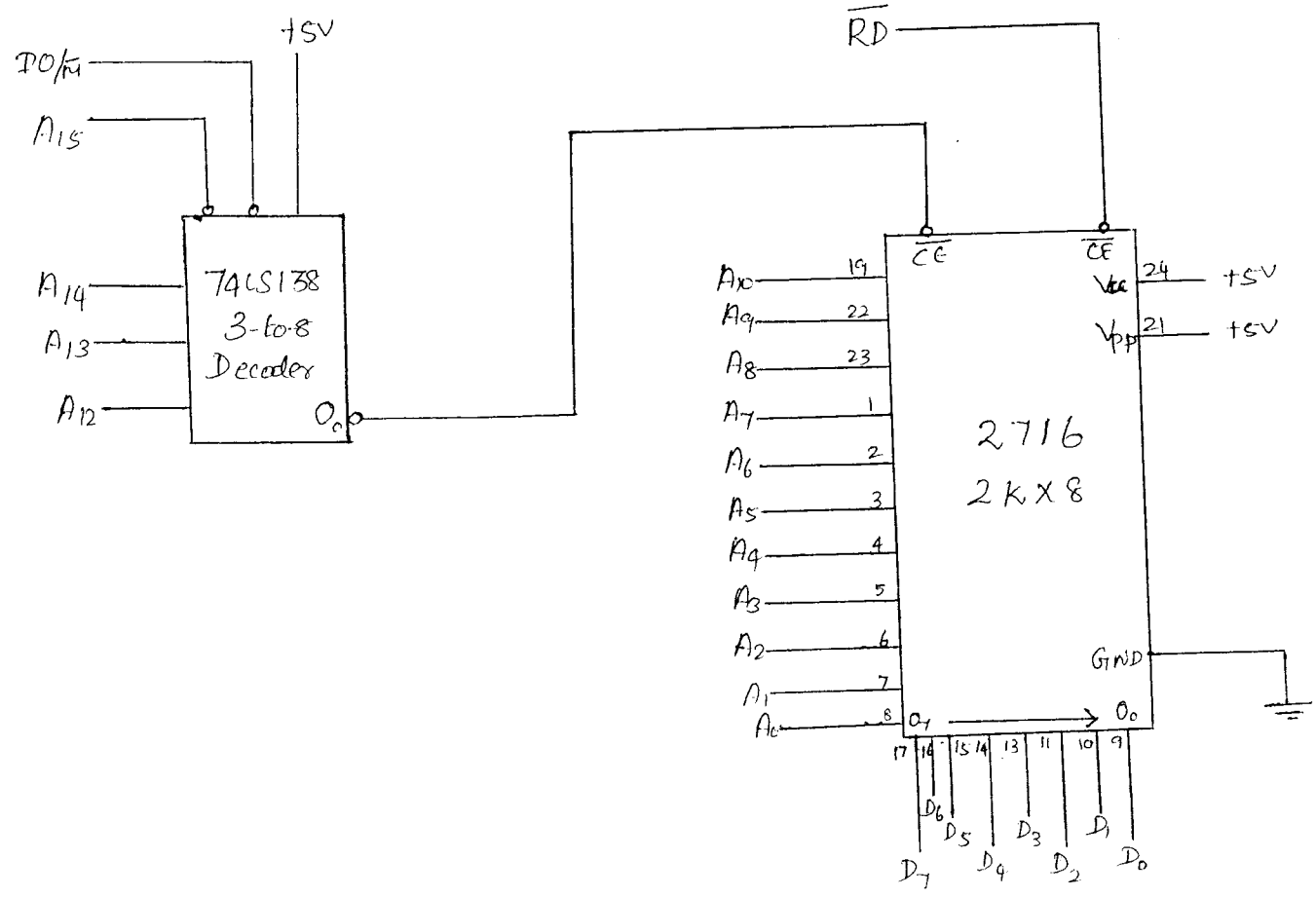
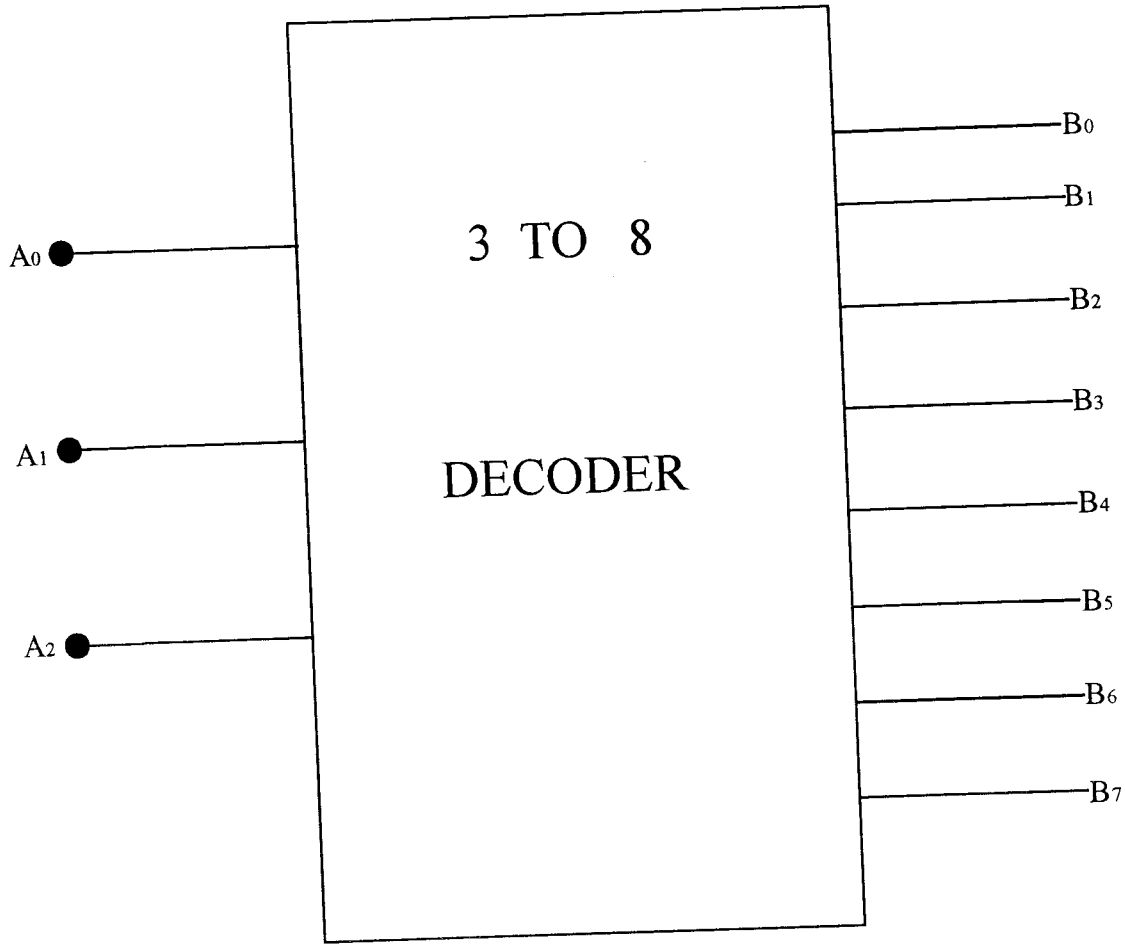
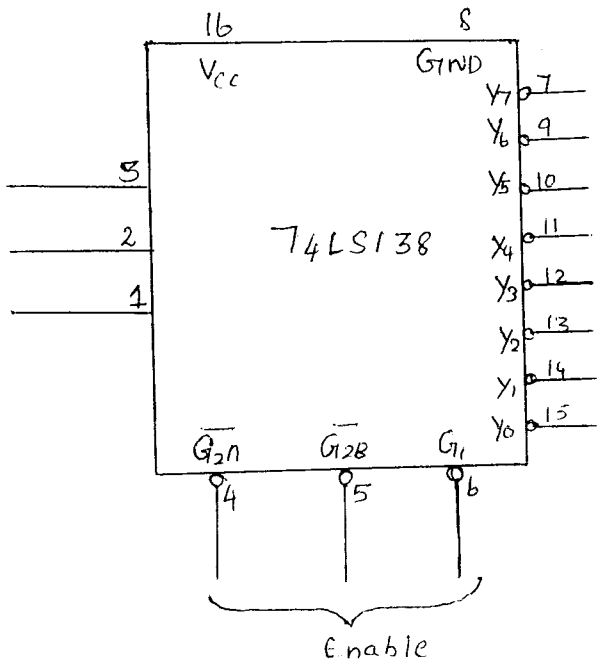


FIG: 4-7 INTERFACING EPROM: THE 2716



Representation of hypothetical

Figure : 5.8



Function table

Inputs					Outputs							
Enable		Select										
G_1	G_2	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevent

FIG. 5.9 LOGIC DIAGRAM & FUNCTION TABLE OF 74138

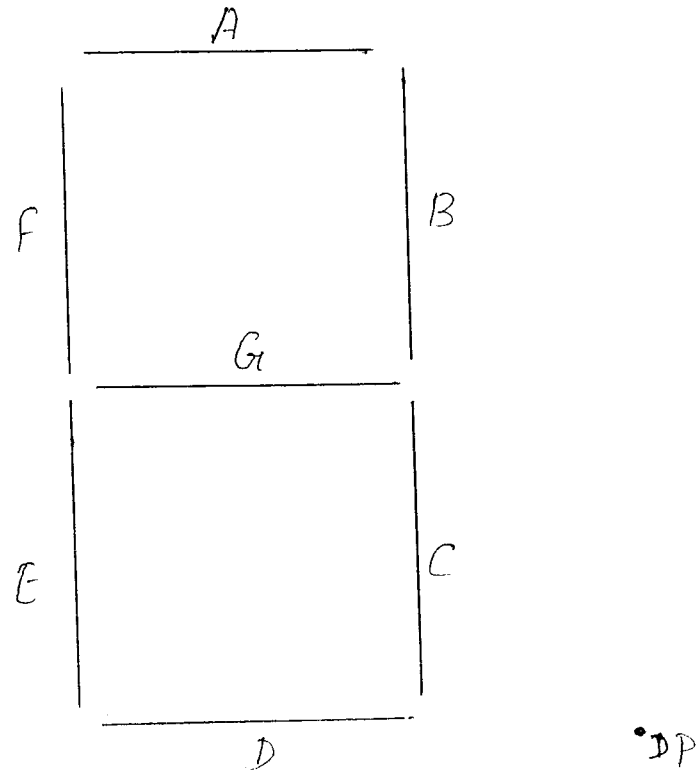
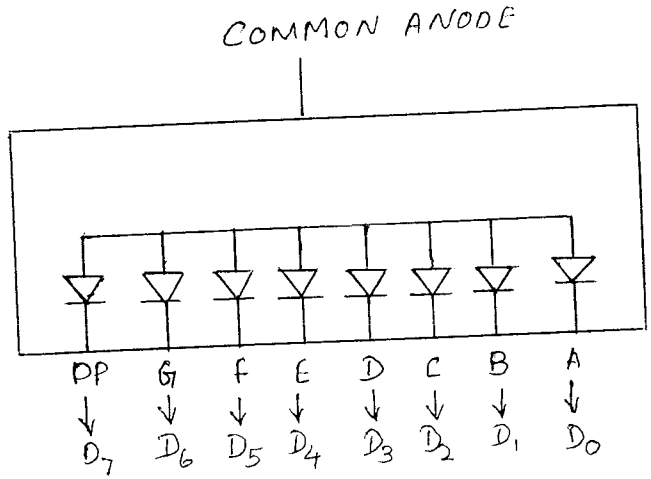


FIG 5.11. SEVEN SEGMENT LED.



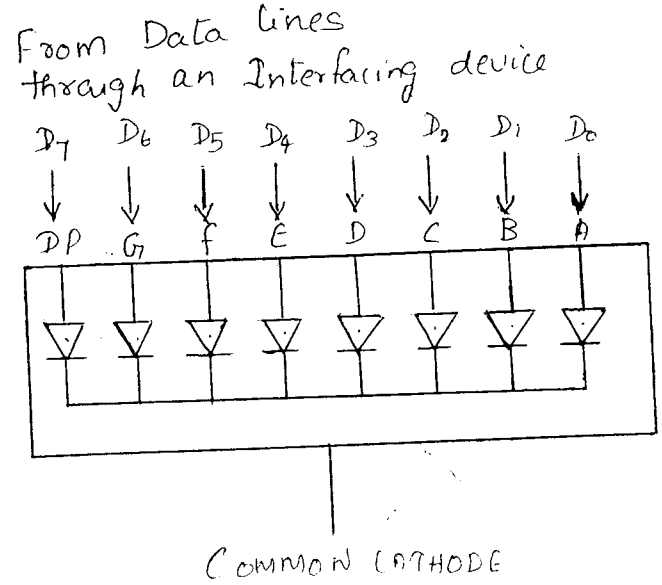


FIG. 5.12. COMMON ANODE LED & COMMON CATHODE LED

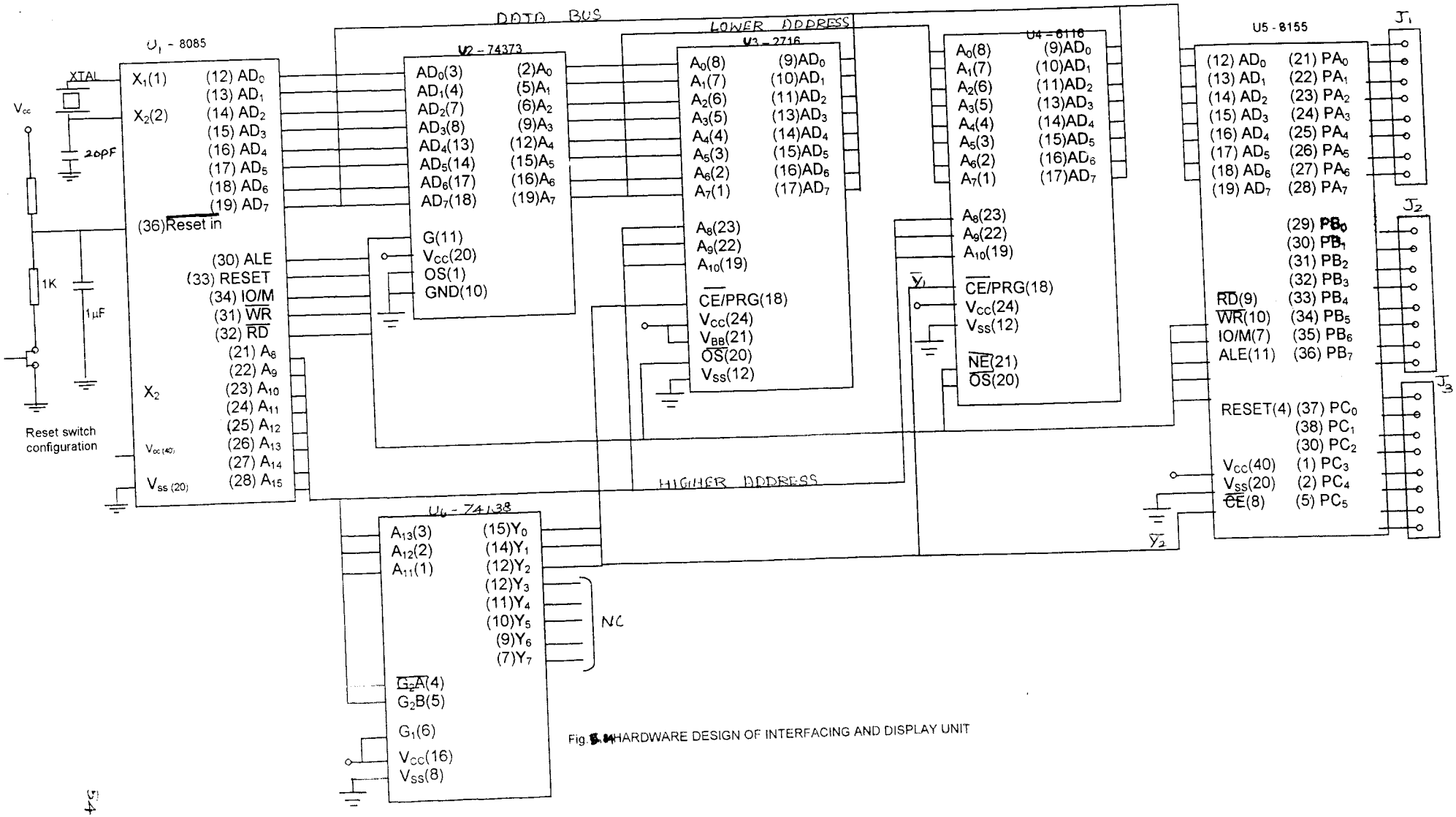


Fig. 5.14 HARDWARE DESIGN OF INTERFACING AND DISPLAY UNIT

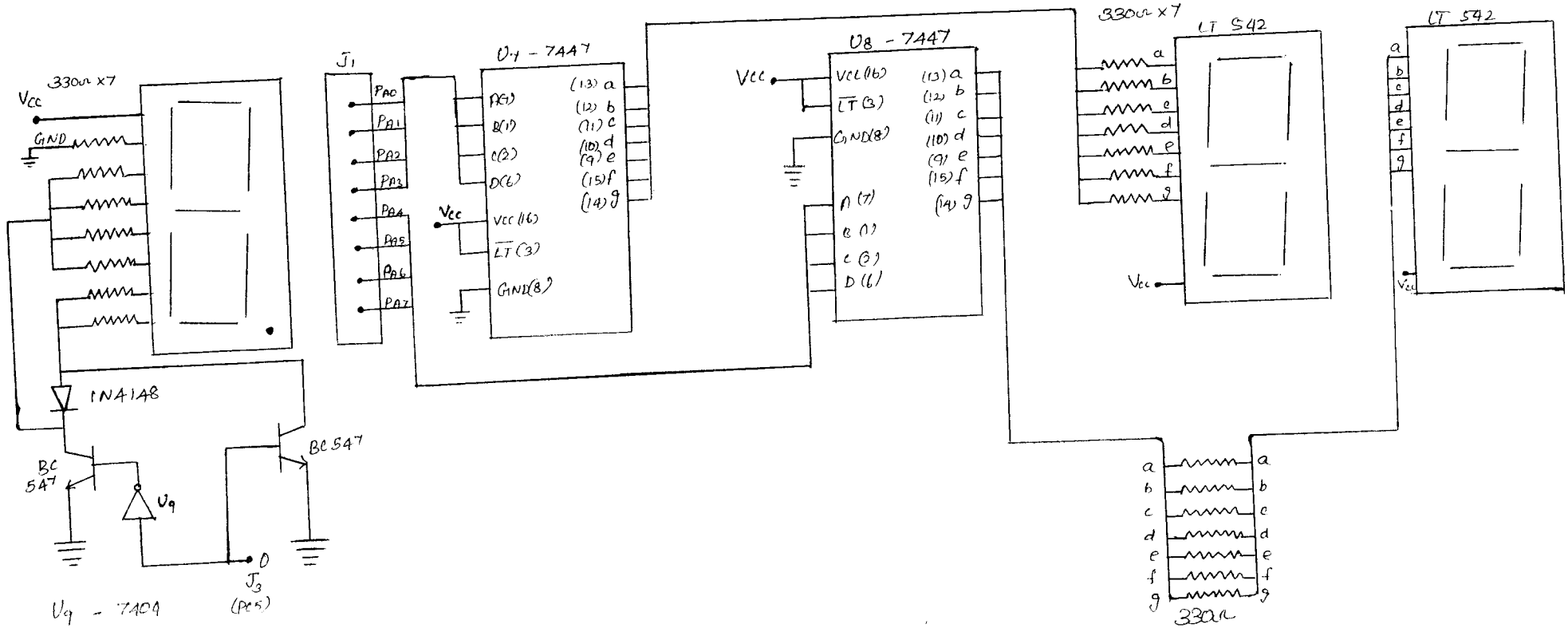


FIG 5.14 DISPLAY UNIT

CHAPTER - 6

SOFTWARE

ALGORITHM

Store the power factor and the corresponding count values in registers R1 & R2 respectively.

Step 1 : Initialize the stack pointer.

Step 2 : Initialize the ports in the 8155 for the output & Input ports

Step 3 : Initialize the count register to zero.

Step 4 : Input the pulse to the input port.

Step 5 : Is the pulse in the low state. IF so go to Step 3 else step 6.

Step 6 : Increment the count register by (1)10

Step 7 : Give a delay for few seconds to input port.

Step 8 : Compare the MSB of present count value stored in the count register along with the count stored in register R1.

Step 9 : Check for unity power factor. If so go to Step 26 (SPL).

Step 10 : If power factor lies in the range of 0.99 to 0.7 go to Step 1

Step 11 : If power factor lies in the range of 0.69 to 0.5 go to Step 1

Step 12 : If power factor lies in the range of 0.49 to 0.3 go to Step 1

Step 13 : Point the index to the first value of this range .

Step 14 : Compare the LSB of the present count value along with this range .

Step 15 : If this count value = First value in the this range go to Step 18 .

Step 16 : Increment the index of R1 .

Step 17 : Go to step 14 .

Step 18 : Display the power factor value corresponding to this count value .

Step 19 : Let the required power factor = 0.99 & let x = 0000

Step 20 : If current power factor = Required power factor go to step 24

Step 21 : Increment x by (01)b

Step 22 : Decrement required power factor by 0.01.

Step 23 : Go to Step 20 .

Step 24 : Output the x value through the output port to switch ON the relay .

Step25 : Go to Step 3 .

SPL

Step 26 : Output '00' to the output port to switch OFF the relays if any in operation .

Step 27 : Display '1' in the display .

Step28 : Switch ON the GREEN LED .

Step 29 : Go to step 3 .

PROGRAM

LABEL	MNEMONICS	OPERANDS	COMMENTS
	LXI	SP 0FFF	Initializing the stack point
	MVI	A 0D	Control word for 8155
	OUT	1010	Initializing the ports of 8155
START	LXI	D 0000	Initializing the count register
	NOP		
LOOP	IN	PORT B0	Input port
	ANI	01	Check for input pulse
	JZ	LOOP	
XX1	INX	D	Count for the input pulse
	IN	PORT B0	
	ANI	01	
	JNZ	XX1	
	NOP		
	MVI	A 03	Check for D value
	ANA	D	Check for D = 00
	JNZ	XX2	
	LXI	H 0500	
RRT	JMP	SPL	
XX2	JMP	YY1	
	MVI	A 01	
	ANA	D	Check for D value = 01
	JZ	XX3	
	LXI	H 0519	
	JMP	YY1	Check for D = 02
XX3	LXI	H 052A	
	NOP		
YY1	MOV	A , M	
	CMP	E	
	JZ	DISP	
	JNC	DISP	
	INX	H	
	JMP	YY1	
DISP	INR	H	Increment H register from 05 to 06
	MOV	A , M	
	OUT	PORT A	
	NOP		

LABEL	MNEMONICS	OPERANDS	COMMENTS
	NOP		
	MOV	*A,M*	*Relay checking*
	MVI	*C,90*	
	CMP	*C*	
	JZ	*A111*	
	JNC	*A111*	
	MVI	*C,80*	
	CMP	*C*	
	JZ	*B111*	
	JNC	*B111*	
	MVI	*C,70*	
	CMP	*C*	
	JZ	*C111*	
	JNC	*C111*	
	MVI	*C,60*	
	CMP	*C*	
	JZ	*D111*	
	JNC	*D111*	
	MVI	*C,50*	
	CMP	*C*	
	JZ	*E222*	
	JNC	*E222*	
	MVI	*C,40*	
	CMP	*C*	
	JZ	*F222*	
	JNC	*F222*	

LABEL	MNEMONICS	OPERANDS	COMMENTS
	MVI	*C,30*	
	CMP	*C*	
	JZ	*LLLL*	
	JNC	*LLLL*	
	MVI	*C,20*	
	CMP	*C*	
	JZ	*LHLH*	
	JNC	*LHLH*	
	MVI	*C,10*	
	CMP	*C*	
	JZ	*HHLL*	
	JNC	*HHLL*	
	JMP	*PPPP*	
A111	*MVI*	*A,01*	*Relay operation*
	OUT	*PORT C*	
	JMP	*DELAY*	
B111	*MVI*	*A,12*	
	OUT	*PORT C*	
	JMP	*DELAY*	
C111	*MVI*	*A,13*	
	OUT	*PORT C*	
	JMP	*DELAY*	
D111	*MVI*	*A,14*	
	OUT	*PORT C*	
	JMP	*DELAY*	

LABEL	MNEMONICS	OPERANDS	COMMENTS
E222	*MVI*	*A,15*	
	OUT	*PORT C*	
	JMP	*DELAY*	
F222	*MVI*	*A,16*	
	OUT	*PORT C*	
	JMP	*DELAY*	
LLLL	*MVI*	*A,17*	
	OUT	*PORT C*	
	JMP	*DELAY*	
LHLH	*MVI*	*A,18*	
	OUT	*PORT C*	
	JMP	*DELAY*	
HHLL	*MVI*	*A,19*	
	OUT	*PORT C*	
	JMP	*DELAY*	
PPPP	*MVI*	*A,1F*	
	OUT	*PORT C*	
	JMP	*DELAY*	
DELAY	*PUSH*	*H*	*Delay subroutine*
	PUSH	*D*	
	PUSH	*B*	
	PUSH	*PSW*	
	MVI	*C,05*	
LOOP Y	*LXI*	*D,DE14*	
LOOP X	*DCX*	*D*	

LABEL	MNEMONICS	OPERANDS	COMMENTS
	MOV	*A,D*	
	ORA	*E*	
	JNZ	*LOOP X*	
	DCR	*C*	
	JNZ	*LOOP Y*	
	POP	*PSW*	
	POP	*B*	
	POP	*D*	
	POP	*H*	
	JMP	*START*	
SPL	*MVI*	*A,05*	*Check and display for unity pf.*
	CMP	*E*	
	JZ	*DDPL*	
	JNC	*DDPL*	
	JMP	*RRT*	
DDPL	*MVI*	*A,00*	
	OUT	*PORT A*	
	MVI	*A,20*	*Indication for unity pf.*
	OUT	*PORT C*	
	JMP	*DELAY*	

LOOK - UP TABLE

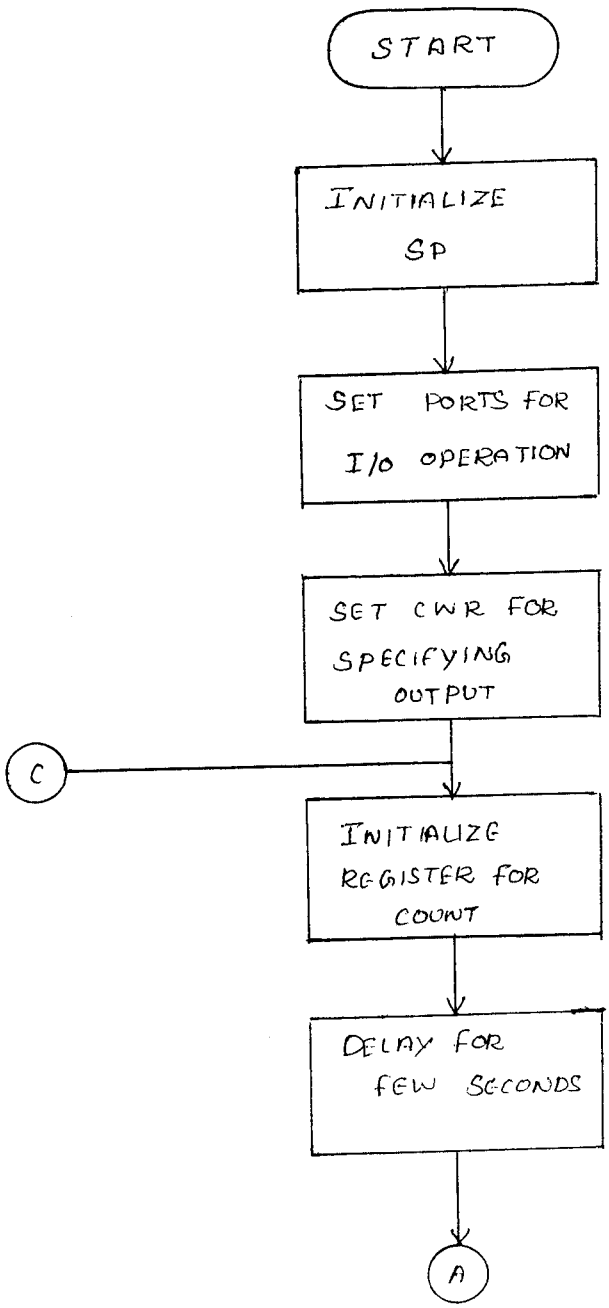
ADDRESS	*DISPLAY VALUE*
0600	*99*
0601	*99*
0602	*98*
0603	*97*
0604	*96*
0605	*95*
0606	*94*
0607	*93*
0608	*92*
0609	*91*
060A	*90*
060B	*89*
060C	*88*
060D	*87*
060E	*86*
060F	*85*
0610	*84*
0611	*83*
0612	*82*
0613	*81*
0614	*80*
0615	*78*
0616	*76*
0617	*74*
0618	*72*
0619	*70*

ADDRESS	*DISPLAY VALUE*
061A	*68*
061B	*66*
061C	*64*
061D	*62*
061E	*60*
061F	*55*
0620	*50*
0621	*45*
0622	*40*
0623	*35*
0624	*30*
0625	*25*
0626	*20*
0627	*15*
0628	*10*
0629	*05*
062A	*00*
062B	*00*

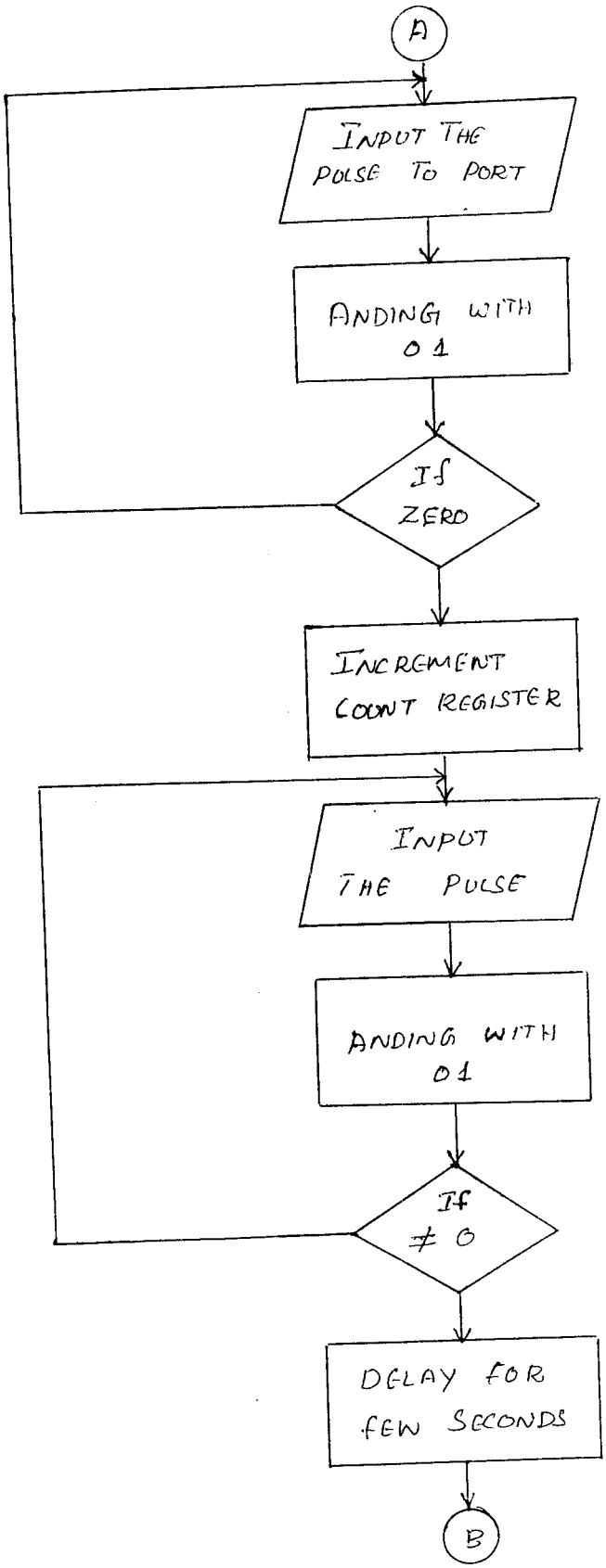
ADDRESS	*DISPLAY VALUE*
0500	*0006*
0501	*002D*
0502	*0041*
0503	*0050*
0504	*005B*
0505	*0066*
0506	*0072*
0507	*007A*
0508	*0083*
0509	*008B*
050A	*0093*
050B	*0099*
050C	*00A1*
050D	*00A7*
050E	*00AF*
050F	*00B4*
0510	*00BB*
0511	*00C0*
0512	*00C7*
0513	*00CC*
0514	*00D1*
0515	*00DC*
0516	*00E6*
0517	*00F0*
0518	*00FA*
0519	*0103*

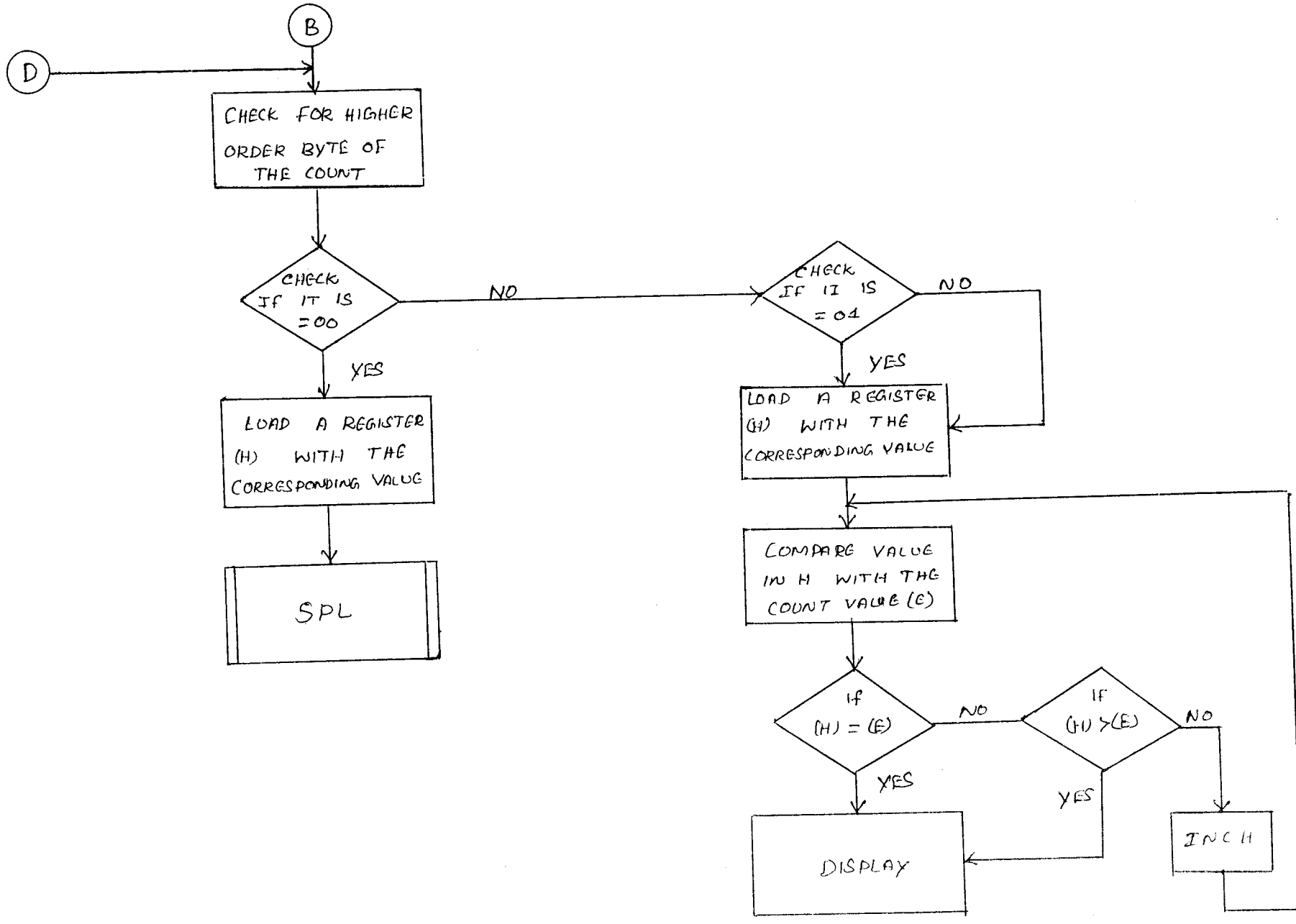
ADDRESS	*DISPLAY VALUE*
051A	*0107*
051B	*0115*
051C	*011E*
051D	*0126*
051E	*012E*
051F	*0142*
0520	*0155*
0521	*0168*
0522	*017A*
0523	*018B*
0524	*019C*
0525	*01AE*
0526	*01BE*
0527	*01CF*
0528	*01DF*
0529	*01F0*
052A	*0201*
052B	*02FF*

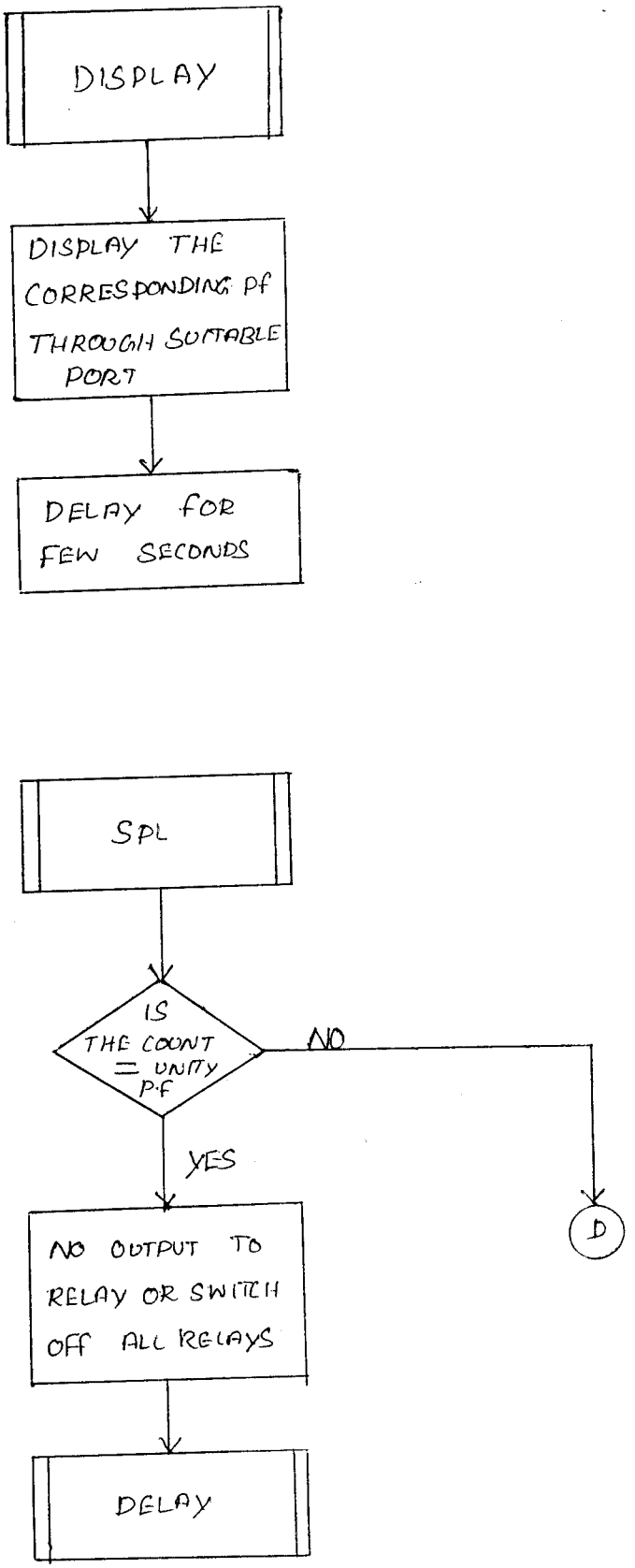
4.3 : FLOWCHART:



COUNT FOR PULSES




B
D
CHECK FOR HIGHER ORDER BYTE OF THE COUNT
CHECK IF IT IS =00
NO
YES
LOAD A REGISTER (H) WITH THE CORRESPONDING VALUE
SPL
CHECK IF IT IS =01
NO
YES
LOAD A REGISTER (H) WITH THE CORRESPONDING VALUE
COMPARE VALUE IN H WITH THE COUNT VALUE (E)
IF (H) = (E)
NO
IF (H) > (E)
NO
YES
YES
DISPLAY
INC H


DISPLAY
DISPLAY THE CORRESPONDING Pf THROUGH SUITABLE PORT
DELAY FOR FEW SECONDS
SPL
IS THE COUNT = UNITY P.F
NO
YES
D
NO OUTPUT TO RELAY OR SWITCH OFF ALL RELAYS
DELAY

CHAPTER - 7

POWER FACTOR IMPROVEMENT UNIT

This unit is final unit of this project which includes the Relays , capacitors and also the LEDs . This unit performs the function of improving the power factor of the system whenever it lags by including the required KVAR to the supply .

7.1. RELAY UNIT

This unit receives signals for its switching ON & OFF from the 8155 ports interfaced with the 8085 microprocessor . The connection diagram is as shown in the figure 7.1(a). The output of this relay includes or discludes the capacitors in the capacitor bank whenever necessary .

A protective relay is an electrical relay used for the protection of the electrical devices . It is a device which closes its

contacts , when an operating quantity reaches certain pre determined magnitude or phase . closing of the relay contacts initiates an alarm circuit or trip circuit .

The protective relays are classified as follows

Electromagnetic relays
Electromagnetic induction relays
Electrothermal relays
Physico - thermal relays
Static relays

The relays used here are Electromagnetic relays . These relays are actuated by either AC or DC . They are of different types . They are Moving plunger , Moving iron , Attracted armature type , Hinged and Balanced beam types . The operating torque is produced by electro - magnetic attraction effects of electric current . They operate by the virtu of a plunger being drawn into a solenoid , or an armature being attracted to the poles of an electromagnet .

A relay is said to operate whenever it opens or closes its contact depending upon the circumstances. A relay is said to have a 'closed' contact when its contact attains the closed position when it is completely de-energised and if it is open it is said to have 'open' contact.

7.2. Capacitor bank unit

This unit consists of the capacitors of different KVARs which are to be included across the supply in order to improve the power factor in the system whenever it lags. The designing of the KVAR in the capacitor bank is given below

For a given load of 100 H.P.

$$\text{Corresponding } KW = 100 \times H.P.$$

$$= 74.6 \; KW$$

$$\text{Present Power factor} = 0.9$$

$$\text{Multiplication Factor} = 0.36$$

$$\text{Desired power factor} = 0.96$$

Capacitor rating required (KVAR) = KW X M.F

= 74.6 X..0.36

= 26.85

For power factor between 0.85 & 0.9 the capacitor rating is 30 KVAR for which Relay 1 is operated.

For power factor 0.8

Multiplication factor = 0.46

KVAR = 74.6 X..0.46

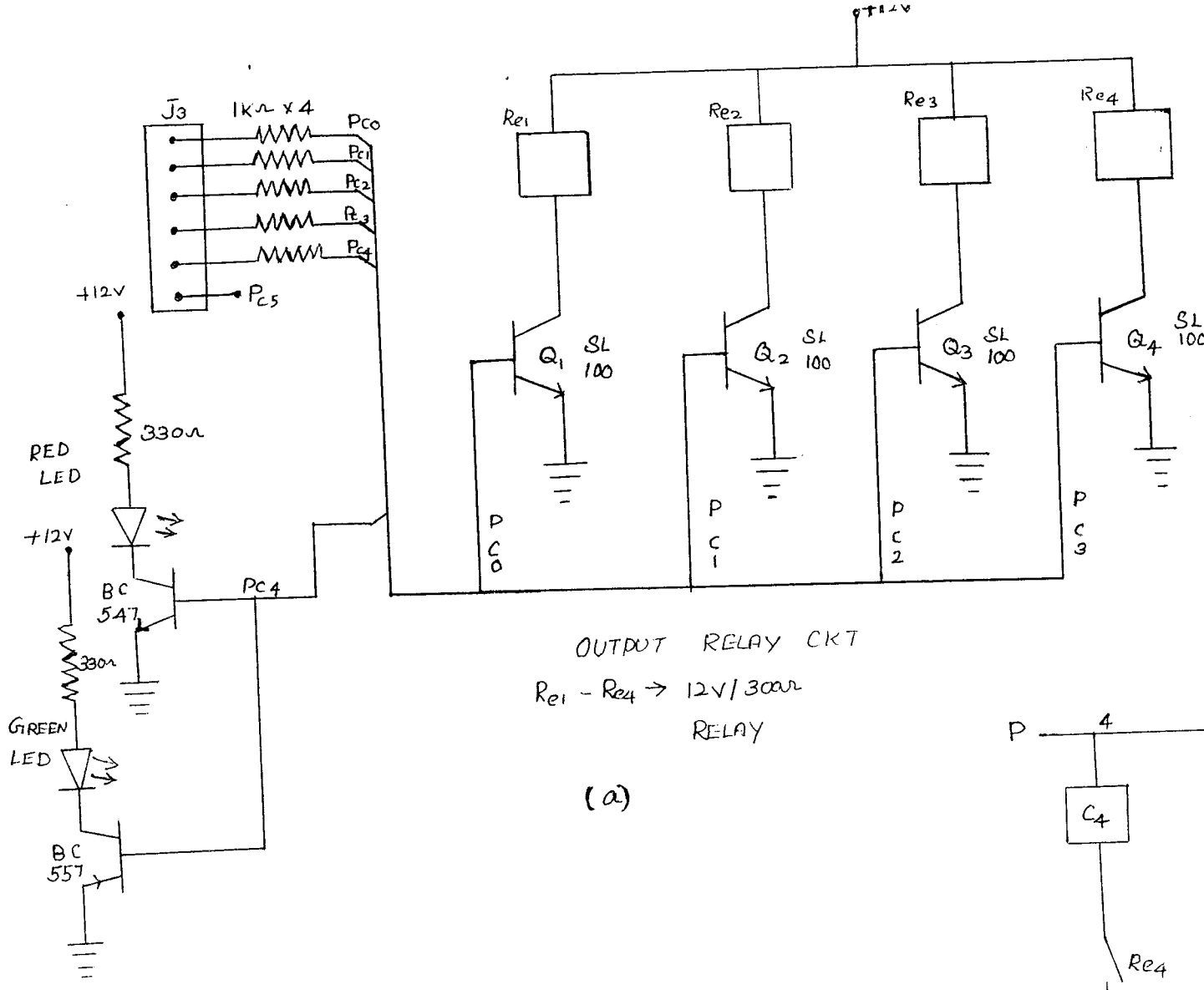
= 34.3

= 17 KVAR for which Relay 2 is operated

7.3. Alarm and indication unit

This unit helps in understanding or knowing the power actor coming at the supply just at a glance. Here we use LEDs for indication. An alarm may also be used in the place of the LEDs.

Two LEDs -- green & red are being used. Glowing of the green LED denotes the unity power factor or power factor in the desired limit. Glowing of red LED indicates lagging power factor for which measures should be taken. The LEDs are connected along with the relay circuit. They get signals from the 8155 output ports. The software for sending signals to the LEDs are written accordingly.



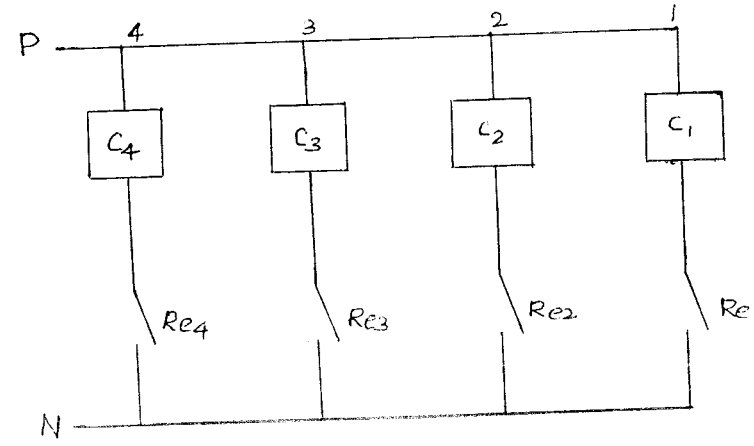


FIG: 7.1 POWER FACTOR IMPROVEMENT UNIT

CHAPTER - 8

TESTING

Power factor sensing unit have been tested for different load conditions and corresponding power factor were measured.

Relay circuit have been replaced by LEDs to indicate switching operation of the capacitor bank.

This model can be extended to measure power factor in 3Phas circuit and also to improve it.

CHAPTER - 9

CONCLUSION

The Power factor controller designed has been used to switch on the set of capacitor bank whenever the power factor lags below the set value.

The software designed helps to compare the current power factor with limiting value of power factor and trigger the relay circuit.

The display unit consists of LEDs. It helps to indicate the low power factor and improved power factor.

This model can be extended to measure power factor in 3 Phas circuit also to improve it.

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12 . FREDRICK J . HILL , GERALD R .PETERSON " INTRODUCTION TO SWITCHING THEORY AND LOGICAL DESIGN " PUBLISHED BY JOHN WILEY AND SONS , NEW YORK , THIRD EDITION .

13. PRICE L. ROGERS ,JOHN WILEY " POWER FACTOR ECONOMICS " JOHN WILEY AND SONS , NEW YORK , 1950 .

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7490, LS90
Counters

Decade Counter
Product Specification

Logic Products

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1·MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set (MS_1·MS_2) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain a divide-by-five operation at the Q_3 output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7490N, N74LS90N

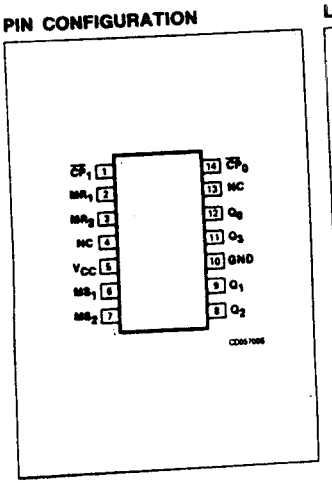
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

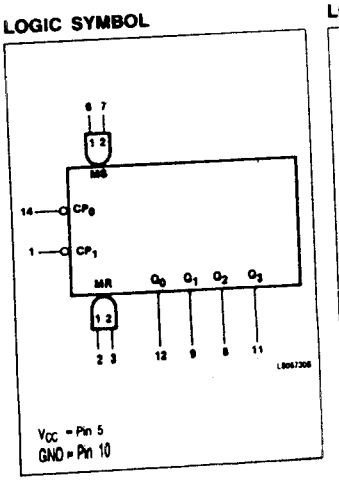
PINS	DESCRIPTION	74	74LS
$\overline{CP}_0$	Input	2ul	6LSul
$\overline{CP}_1$	Input	4ul	8LSul
MR, MS	Inputs		1ul
$Q_0 - Q_3$	Outputs	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

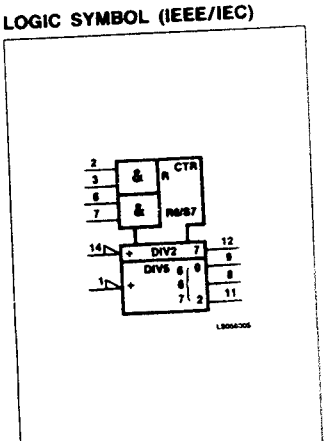
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

The 8085AH family includes memory components, which are directly compatible to the 8085AH CPU. For example, a system consisting of the three chips, 8085AH, 8156H, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 7.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 8 shows the system configuration of Memory Mapped I/O using 8085AH.

The 8085AH CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 9.

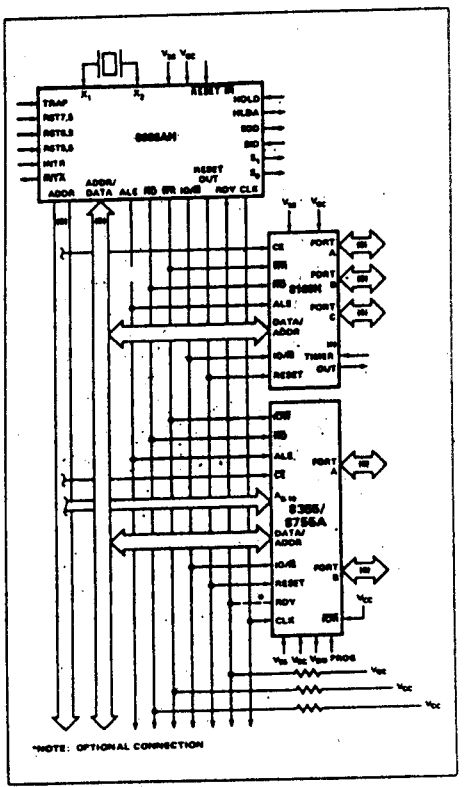


Figure 7. 8085AH Minimum System (Standard I/O Technique)

7486, LS86, S86
Gates

Quad Two-Input Exclusive-OR Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7486N, N74LS86N, N74S86N
Plastic SO	N74LS86D, N74S86D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

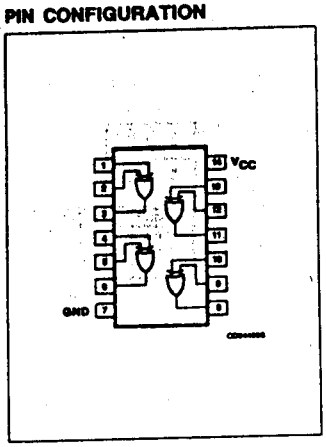
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

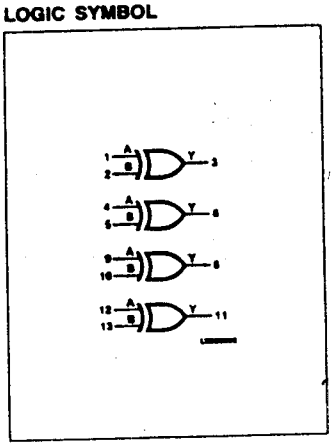
PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

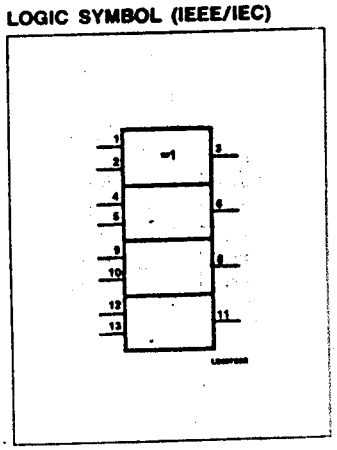


Table 1. Pin Description

Symbol	Type	Name and Function
A_8–A_{15}	O	**Address Bus:** The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_0–$_7$	I/O	**Multiplexed Address/Data Bus:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles
ALE	O	**Address Latch Enable:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$	O	**Machine Cycle Status:** IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge · 0 0 Halt · X X Hold · X X Reset · = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	O	**Read Control:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	**Write Control:** A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY	I	**Ready:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	**Hold:** Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	**Hold Acknowledge:** Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR	I	**Interrupt Request:** Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$	O	**Interrupt Acknowledge:** Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	**Restart Interrupts:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

Table 1. Pin Description (Continued)

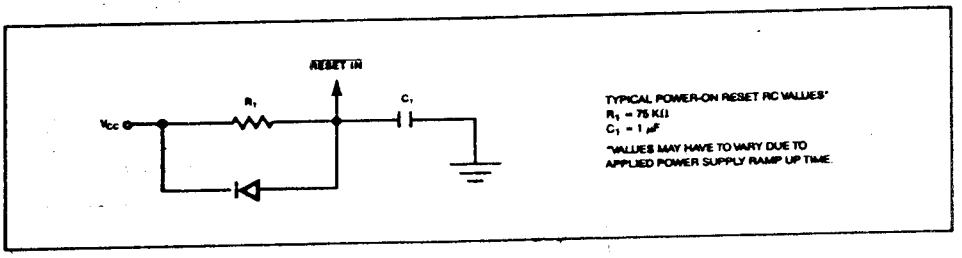
Symbol	Type	Name and Function
TRAP	I	**Trap:** Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
RESET IN	I	**Reset In:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, RESET IN must remain low for at least 10 ms after minimum V_{CC} has been reached. For proper reset operation after the power-up duration, RESET IN should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as RESET IN is applied.

Symbol	Type	Name and Function
RESET OUT	O	**Reset Out:** Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2	I	**X_1 and X_2:** Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK		**Clock:** Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	**Serial Input Data Line:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	**Serial Output Data Line:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**Power:** +5 volt supply.
V_{SS}		**Ground:** Reference.

Table 2. Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.



intel

8155H/8156H/8155H-2/8156H-2
2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

- **Single +5V Power Supply with 10% Voltage Margins**
- **30% Lower Power Consumption than the 8155 and 8156**
- **100% Compatible with 8155 and 8156**
- **256 Word x 8 Bits**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8-Bit I/O Ports**
- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Compatible with 8085AH, 8085A and 8088 CPU**
- **Multiplexed Address and Data Bus**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085AH-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

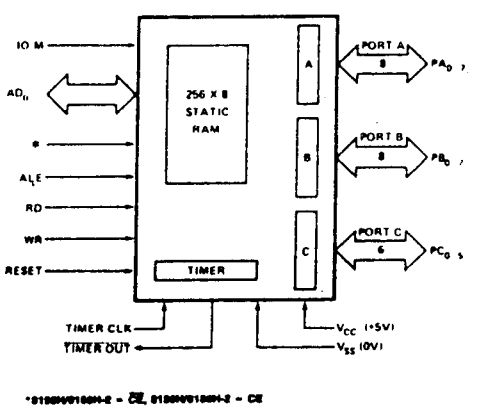


Figure 1. Block Diagram

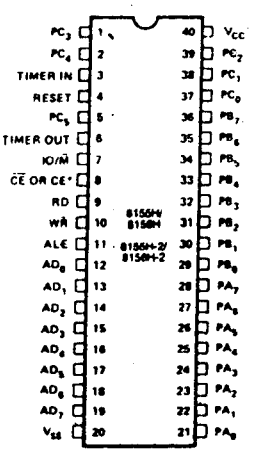


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	**Reset:** Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times.
AD_{0-7}	I/O	**Address/Data:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/56H on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$	I	**Chip Enable:** On the 8155H, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — ABF (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — B BF (Port B Buffer Full) PC_5 — $\overline{B\ STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
V_{CC}		**Voltage:** +5 volt supply.
V_{SS}		**Ground:** Ground reference.

FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit tim... coun...

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

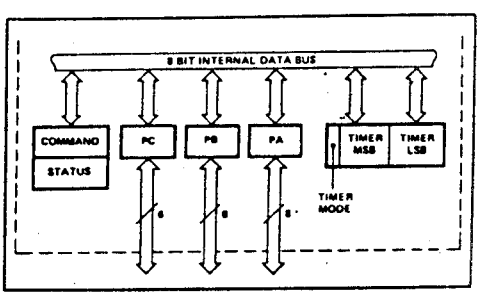


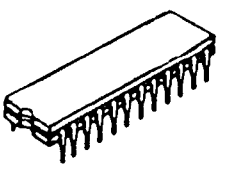
Figure 3. 8155H/8156H Internal Registers

2048-word×8-bit High Speed Static CMOS RAM

■FEATURES

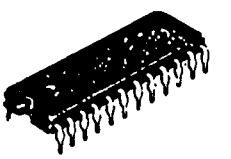
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation Standby: 100μW (typ.) Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116-2, HM6116-3, HM6116-4



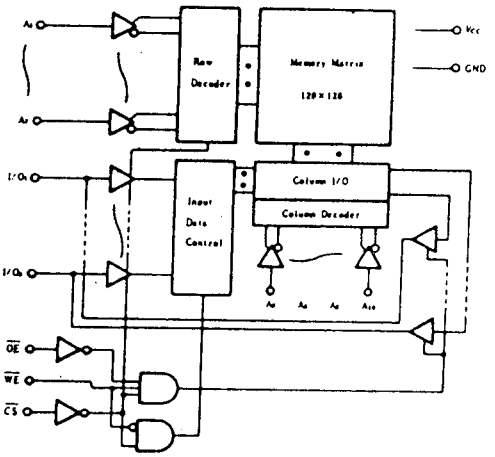
(DG-24)

HM6116P-2, HM6116P-3, HM6116P-4

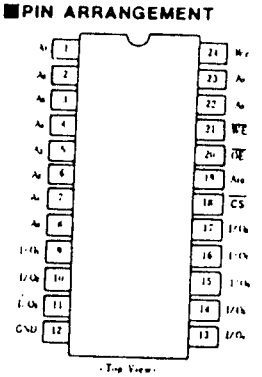


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −1.5 V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)–(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

intel

2716
16K (2K x 8) UV ERASABLE PROM

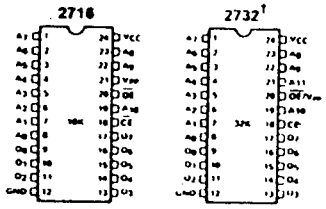
- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
  - **— 490 ns Max. 2716-5**
  - **— 650 ns Max. 2716-6**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

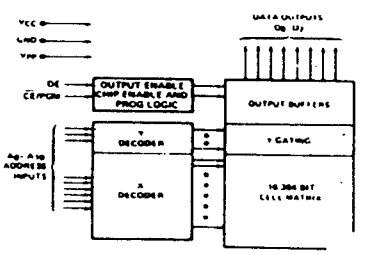
PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



Logic Products

74LS373, 74LS374, S373, S374
Latches/Flip-Flops

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs
Product Specification

FEATURES
- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION
The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS373N, N74S373N, N74LS374N, N74S374N
Plastic SOL-20	N74LS373D, N74S373D, N74LS374D, N74S374D

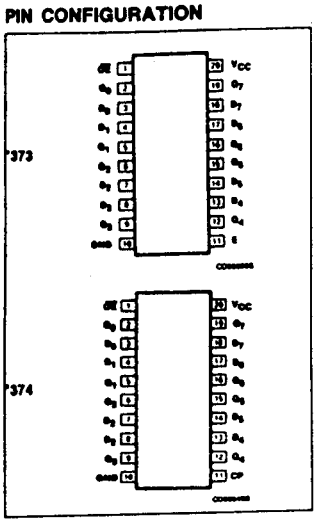
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

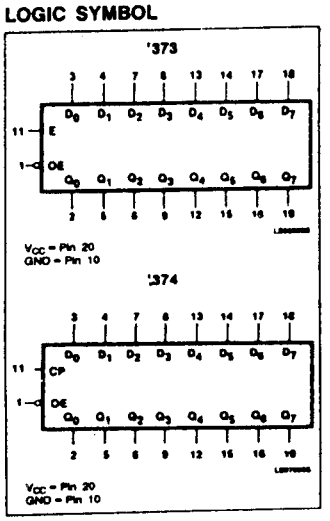
PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE:
Where a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

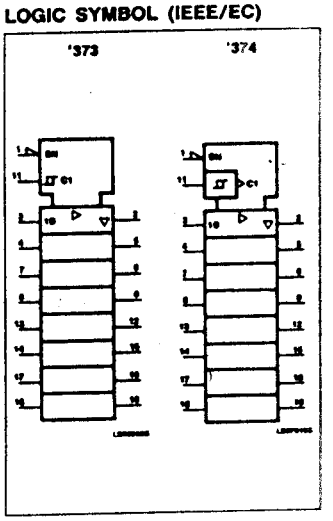
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/EC)



The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

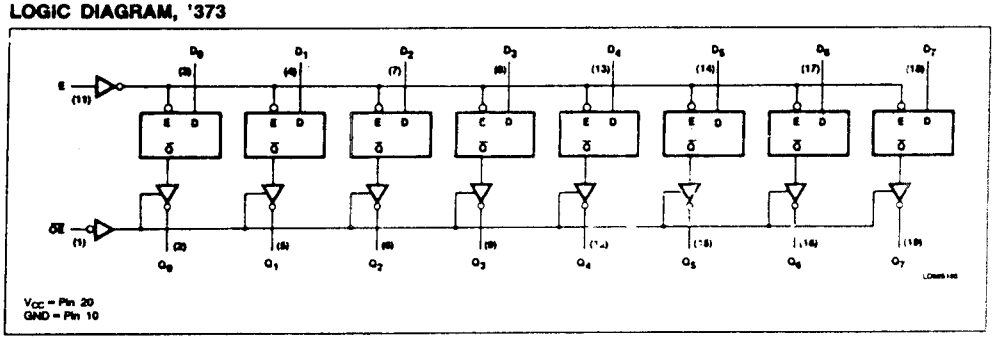
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

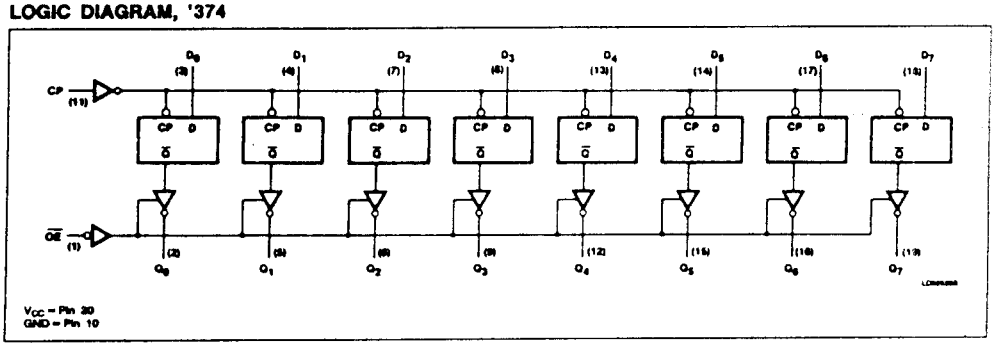
The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT — FUNCTION TABLE '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

74LS138, S138
Decoders/Demultiplexers

1-Of-8 Decoder/Demultiplexer
Product Specification

Logic Products

FEATURES
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

DESCRIPTION
The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0}-\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS138	20ns	6.3mA
74S138	7ns	49mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74S138N, N74LS138N
Plastic SO	N74LS138D, N74S138D

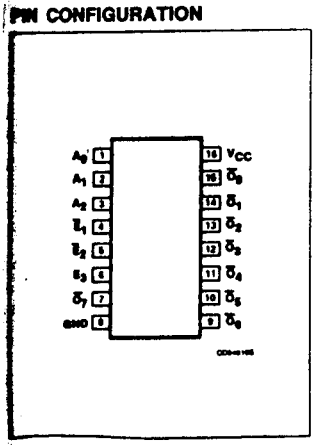
NOTE:
For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

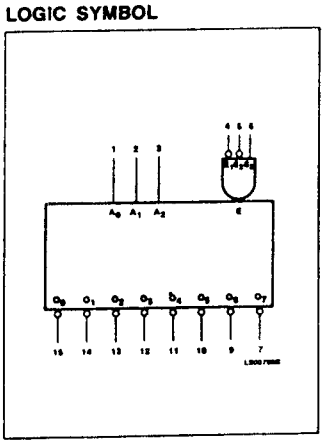
PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE:
Where a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

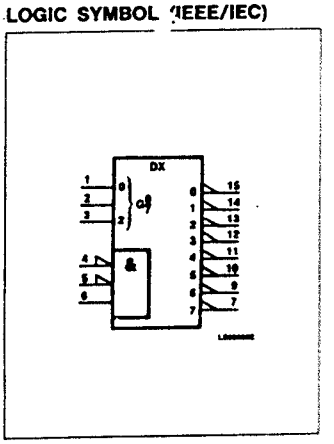
PIN CONFIGURATION



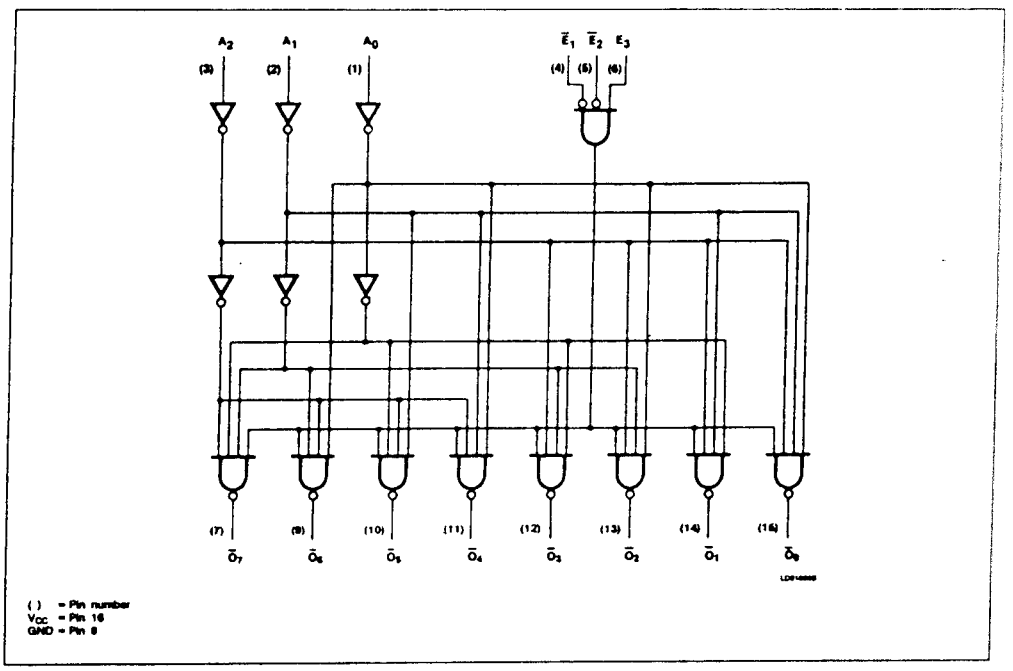
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



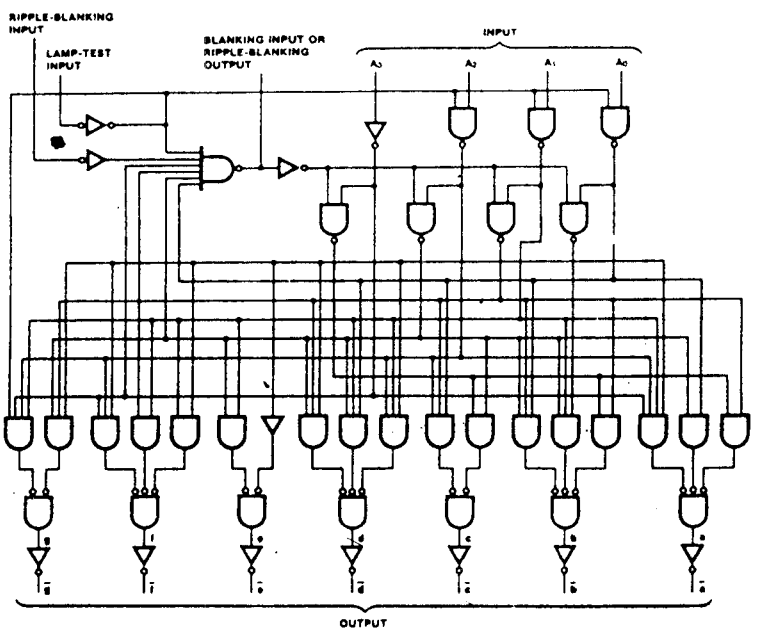
FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTIONAL DESCRIPTION — The '46A, '47A and 'LS47 decode the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, ie: by driving $\overline{RBI}$ of an intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $\overline{BI/RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by enternal means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

LOGIC DIAGRAM



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS