P-3390

ANTI-COLLISION SYSTEM IN TRAINS USING RFID

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A PROJECT REPORT

Submitted to the

FACULTY OF ELECTRONICS AND COMMUNICATION ENGINEERING

In partial fulfillment of the requirements
for the award of the degree

of

BACHELOR OF ENGINEERING
in
ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

This is to be certified that this project report "**ANTI-COLLISION SYSTEM IN TRAINS USING RFID**" is the bonafide work of "**DANNY GEORGE, GAUTAM SUNDER, M.GOWRI SHANKAR, and YUVARAJ.S.V** " who carried out the project work under my supervision.

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ACKNOWLEDGEMENT

We extend our heartfelt gratitude towards our revered chairman **Arutselvar Dr. N. Mahalingam, Chairman, Dr.B.K.Krishnaraj Vanavarayar, Co-Chairman** for having provided us with the necessary infrastructure to undertake this project.

We are extremely grateful to **Dr. J.Shanmugam, Director,** Kumaraguru College of Technology for having given us a golden opportunity to embark on this project.

We are extremely grateful to **Dr.Ramachandran, Principal,** Kumaraguru College of Technology for having given us a golden opportunity to embark on this project

We are deeply obliged to **Dr.Rajeswari Mariappan, M.E.,Ph.D.,** Head of the Department of Electronics& Communication for her concern and implication during the project course.

We extend our heartfelt thanks to our Project Coordinator **V.Jeyasri Arokiamary, M.E.,Associate Prof,** and **Prof.K.Ramprakash, M.E.,** Professor, Department of Electronics and Communication and our respectable Guide **Ms.G.Amirtha Gowri, M.E.,Ph.D.,Associate Prof** Department of Electronics and Communication for their helpful guidance and valuable support given to us throughout this project. Our thanks to all **Teaching and Non-teaching staffs** of our department for providing us the technical support for our project.

We also thank **our family and friends** who helped us to complete this project with flying colours.

ABSTRACT

The prevalence of accidents happening with concern to trains/ railway networks is quite high these days due to natural occurrences like fog, mist, rain, storms and other unfortunate mishaps like server missignalling, etc.

Due to improper or invalid communication between two approaching trains, the consequences may include the trains derailing off the tracks, or crashing into each other due to lack of prior warning.

Several attempts to raise security concerns regarding this issue have been met with failure-prone methods. The main objective of this project is to prevent accidents caused on railway tracks using the concept of RFID (Radio Frequency Identification) tags. This method is cost-effective and easy to implement wherever required. The working of this design is fool-proof and less susceptible to any type of signal failure problems. These tags are attached to the tracks at regular intervals throughout the length of the distance.

The trains are equipped with a RF reader implemented with a RF transceiver. These RF readers are placed underneath the train, so that it receives information from the RF tags immediately when the train runs over the tracks.

Thus, when the microcontroller in the reader receives information, it is transmitted via the RF transceiver so that the location of the train on the specific track is known to all trains in motion within the span of 5km at that point of time.

So if two trains are found to be in danger of collision on the same track then both the trains will come to halt immediately. A buzzer on the train also automatically alerts the need for such a scenario. Thus, further accidents can be avoided by using this simple mechanism. As a RF tag is complementary to the bar code system, it is fool-proof as well. Also, this project gives scope to expand the horizon of design and create a new technology network in railway departments that will be solely dedicated to ensuring the safety of the passengers and machinery.

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CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

A significant increase in the number of accidents happening every year due to train collisions has been noticed on a quite regular basis. This is due to unpredictable occurrences such as storms, fogs, mist, etc. which blindside the operators, disrupt signals, as well as cause havoc among the detection systems. Sometimes even the railway tracks are damaged or ruined, and without any prior warning; train accidents are easily prone to happen.

Though a number of initiatives have been taken to prevent such accidents, news of such incidents continue to be heard of often. GPS system, satellite navigation methods, etc. have all been implemented, but none have been fool-proof thus.

Our project is an attempt to rectify the discrepancies in foretelling a collision, and to ensure safe travel on trains. The concept of this project is based on the property and uses of RFID (Radio Frequency Identification) . Using the information pre-stored in these RFID tags(Track number) that are placed at strategic location in the tracks, and the consequent data from the RFID readers that are on the moving train, the location of any train at any particular track can be determined. This information is relayed to all trains in motion that are in the nearby vicinity, using a RF Transceiver. If any danger of collision on the same track is determined, then both the trains automatically come to a halt, as well as give out a buzzer warning.

Our project is explained is explained in detail in this report with the contents block diagrams, implementation, practical usage

and data specifications, etc. We hope this brings out a clear idea of our vision and the capacity for this initiative to be expanded on a wider canvas in the near future.

1.2 BLOCK DIAGRAM

The block diagram of this project mainly consist of

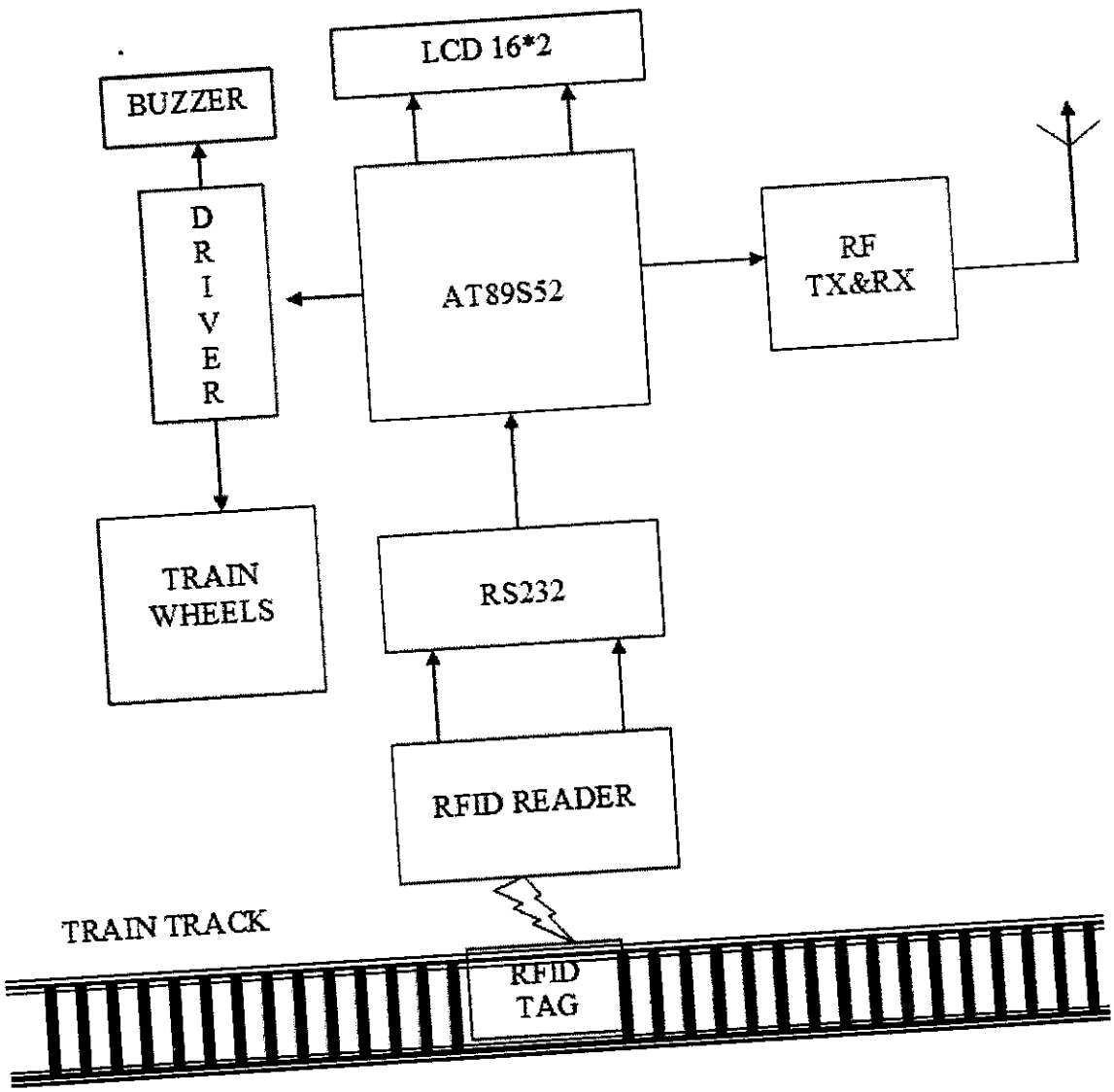


Fig 1.1 Overall Block Diagram

The block diagram comprises of the overview of Microcontroller AT89s52),RFID, RF transceiver which are shown in Fig 1.1

1.2.1 Overview of RFID Reader block

Radio Frequency identification (RFID) card readers provide a low-cost Solution to read passive RFID transponder tags. The RFID card reader read the RFID tag range and outputs unique identification code of the tag at baud rate of 9600. The data from RFID reader is interfaced to be read by the microcontroller.

1.2.2 Overview of AT89S52 Microcontroller

The Microcontroller used is AT89S52, it is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The Unique RFID tag numbers are stored in the microcontroller. The device is manufactured using Atmel's high-density non-volatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non-volatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

1.2.3 Overview of IC MAX232 Block

RS-232 is an important part in interfacing a peripheral device with microcontroller. The output of the microcontroller is usually in TTL format but the peripheral devices require a RS-232 input. Hence RS-232 serves the part of serial communication.

2.4 RF Transceiver

The RF transceiver Available for operation between 433.075 and 434.725 MHz in 50KHz steps these modules give the possibility of 34 different frequency channels and are able to transmit at distances of up to 400m.

1.2.5 RELAY

. 12A at 120VAC for RW & 12A at 240VAC for RWH are UL approved. to comply with user's wide selection.

. RW Series Relay covers switching capacity by 10A is spite of miniature size

. The employment of suitable plastic materials is applied under high temperature condition and various chemical solutions.

. Complete protective construction is designed form dust and soldering flux. If required, plastic sealed type is available for washing procedure.

. RWH is approved C-UL & TÜV safety standard.

1.2.6 BATTERY

The rechargeable batteries are lead-lead dioxide systems. The dilute sealed and is, therefore, maintenance-free, leak proof and usable in any position. immobilized. Should the battery be accidentally overcharged producing hydrogen and oxygen, special one-way valves allow the gases to escape thus avoiding excessive pressure build-up. Otherwise, the battery is completely sulphuric acid electrolyte is absorbed by separators and plates and thus

3 OVERALL CIRCUIT DIAGRAM

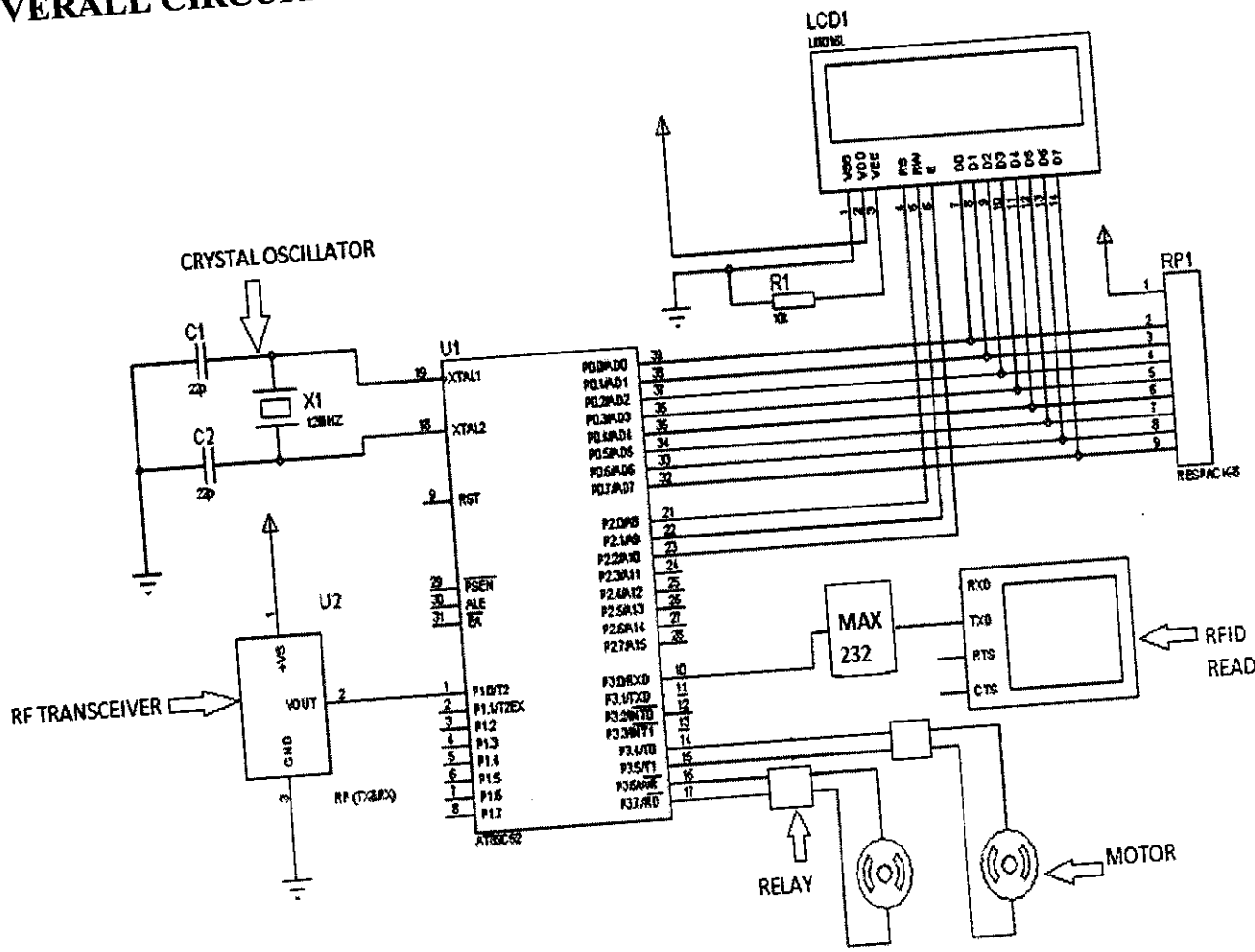


Fig 1.2 Microcontroller with RFID reader and RF transceiver

CHAPTER 2

RFID READER MODULE

.1 RFID SYSTEM

Although it may seem like a new technology, Radio Frequency dentification (RFID) has been around since the 1940's. In fact the United States Air Force first used RFID technology to track friendly aircraft in world war II.

Today, RFID has the potential to dramatically improve many applications in the industrial, transportation and service industries through automatic detection, identification, and control of products and assets. The expectation for RFID is to provide supply chain efficiencies, reduced labour costs, and accurate real-time resource information.

2.2 DEFINITION

RFID is a term used for any device that can be sensed at a distance by radio frequencies or thereabouts, with a few problems from obstruction or mis-orientation . The origins of the term lie in the invention of tags that reflect or re-transmit a radio frequency signal. In its current usage, those working below 300 Hz and those working above 300 MHz, such as microwave (GHz) tags, are included. For example, one type of chip less tag works at 100 Hz and one recent type of battery-driven chip tag works across 5.7-7.0 GHz, rather than at one frequency. Higher frequencies such as visible and infrared devices are excluded as these systems have very different properties and are frequently sensitive to obstruction, heat, light, and orientation. The term "tag" is used to describe any small device-the shapes vary from pendants to beads, nails, labels, or micro wires and fibres-that can be incorporated into paper and even special printed inks on, for example, paper.

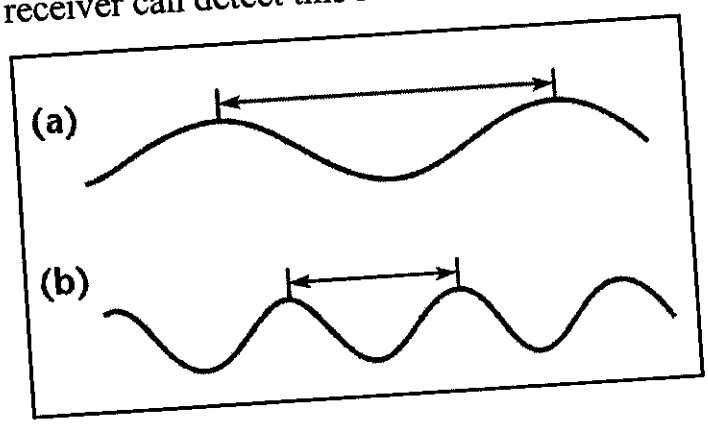
2.3 UNDERSTANDING THE RADIO FREQUENCY

Radio Frequency (RF) is all about physics. RF communication works by creating electromagnetic waves at a source and picking up those electromagnetic waves at a specified destination.

These electromagnetic waves travel through the air at near the speed of light. The wavelength of an electromagnetic signal is inversely proportional to the frequency; the higher the frequency, the shorter the wavelength.

Frequency is measured in Hertz (cycles per second) and radio frequencies are measured in kilohertz (KHz or thousands of cycles per second), megahertz (MHz or millions of cycles per second) and gigahertz (GHz or billions of cycles per second). Higher frequencies result in shorter wavelengths. The wavelength for a 900 MHz device is longer than that of a 2.4 GHz device.

In general, signals with longer wavelengths travel a greater distance and penetrate through, and around objects better than signals with shorter wavelengths. Imagine an RF transmitter wiggling an electron in one location, this wiggling electron causes a ripple effect, somewhat akin to dropping a pebble in a pond. The effect is an electromagnetic wave that travels out from the initial location in electrons wiggling in remote locations. An RF receiver can detect this remote electron wiggling.



(a) A long wavelength

(b) A short wavelength

affects the frequency of waves

.4 ABOUT RFID

RFID uses wireless technology operating with 50 kHz to 2.5 GHz frequency range. A RFID system consists of a RFID tag or transponder that contains data about the tagged item/object, and antenna, a RF transceiver to generate RF signals, and a RFID used for collecting RFID data, which it passes to a host system for processing.

RFID does not require line-of-sight to operate for communications between a tagged object(on the track) and a reader(on the train).

Data encoded on the RFID tag can contain a variety of information about the object, in this case the track number, using electronic product code (EPC).

2.5 WORKING PRINCIPLE OF RFID

The combined antenna and microchip are called an "RFID transponder" or "RFID tag" and work in combination with an "RFID reader" (sometimes called an "RFID interrogator"). An RFID system consists of a reader and one or more tags. The reader's antenna is used to transmit radio frequency (RF) energy. Depending on the tag type, the energy is "harvested" by the tag's antenna and used to power up the internal circuitry of the tag. The tag will then modulate the electromagnetic waves generated by the reader in order to transmit its data back to the reader. The reader receives the modulated waves and converts them into digital data. In the case of the Parallax RFID Reader Module, correctly received digital data is sent serially through the SOUT pin. There are two major types of tag technologies.

"**Passive tags**" are tags that do not contain their own power source or transmitter. When radio waves from the reader reach the chip's antenna, the energy is converted by the antenna into electricity that can power up the microchip in the tag (known as "parasitic power"). The tag is then able to send

ack any information stored on the tag by reflecting the electromagnetic waves
s described above.

"**Active tags**" have their own power source and transmitter.
The power source, usually a battery, is used to run the microchip's circuitry and to broadcast a signal to a reader. Due to the fact that passive tags do not have their own transmitter and must reflect their signal to the reader, the reading distance is much shorter than with active tags. However, active tags are typically larger, more expensive, and require occasional service. The RFID Reader Module is designed
specifically for low-frequency (125 kHz) passive tags. Frequency refers to the size of the radio waves used to communicate between the RFID system components. Just as you tune your radio to different frequencies in order to hear different radio stations, RFID tags and readers have to be tuned to the same frequency in order to communicate effectively. RFID systems typically use one of the following frequency ranges: low frequency (or LF, around 125 kHz), high frequency (or HF, around 13.56 MHz), ultra-high frequency (or UHF, around 868 and 928 MHz), or microwave (around 2.45 and 5.8 GHz). It is generally safe to assume that a higher frequency equates to
a faster data transfer rate and longer read ranges, but also more sensitivity to environmental factors such as liquid and metal that can interfere with radio waves. There really is no such thing as a "typical" RFID tag. The read range of a tag ultimately depends on many
factors: the frequency of RFID system operation, the power of the reader, and interference from other RF
devices.

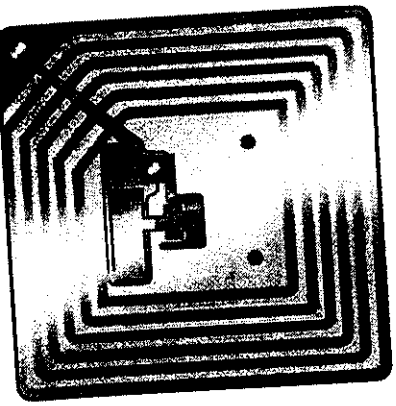


Fig 2.2 RFID tag

2.6 RFID TAGS

Tag options include the following:

.Passive or active

.Read only, Read-write, or write once

.Short range or long range

Active, semi-passive and passive RFID tags are making RFID technology more accessible and prominent in our world. These tags are less expensive to produce, and they can be made small enough to fit on almost any product.

Active and semi-passive RFID tags use internal batteries to power their circuits. An active tag also uses its battery to broadcast radio waves to a reader, whereas a semi-passive tag relies on the reader to supply its power for broadcasting. Because these tags contain more hardware than passive RFID tags, they are more expensive. Active and semi-passive tags are reserved for costly items that are read over greater distances -- they broadcast high frequencies from 850 to 950 MHz that can be read 100 feet or more away. If it is necessary to read the tags from even farther away, additional batteries can boost a tag's range to over 300 feet (100 meters) .

Passive RFID tags rely entirely on the reader as their power source. These tags are read up to 20 feet away, and they have lower production costs, meaning that they can be applied to less expensive merchandise. These tags are manufactured to be disposable, along with the disposable consumer goods on which they are placed. Whereas a railway car would have an active RFID tag, a bottle of shampoo would have a passive tag.

Another factor that influences the cost of RFID tags is data storage. There are three storage types: **read-write, read-only** and **WORM (write once, read many)**. A read-write tag's data can be added to or overwritten. Read-only tags cannot be added to or overwritten -- they contain only the data that is stored in them when they were made. WORM tags can have additional data (like another serial number) added once, but they cannot be overwritten.

CHAPTER 3

MICROCONTROLLER AT89S52

3.1 INTRODUCTION

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density non-volatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non-volatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

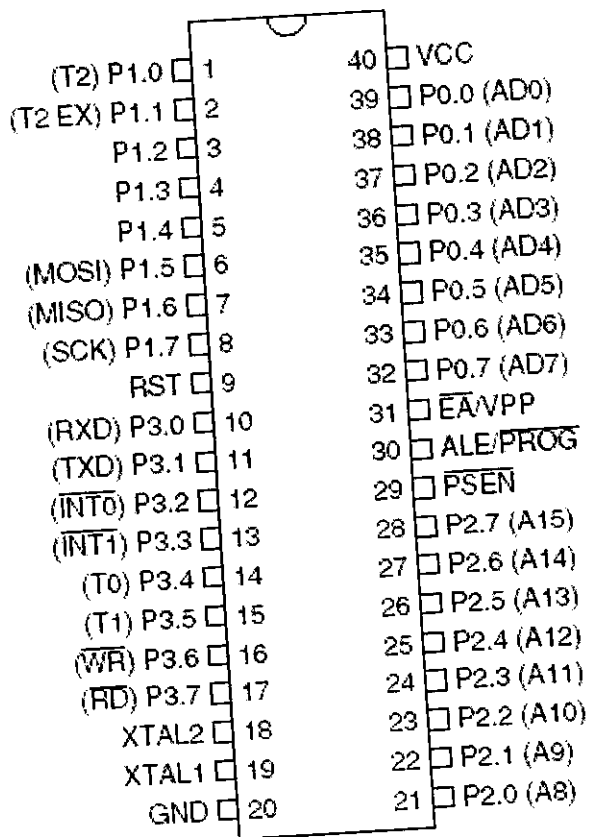
The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM con-tents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

3.2 FEATURES

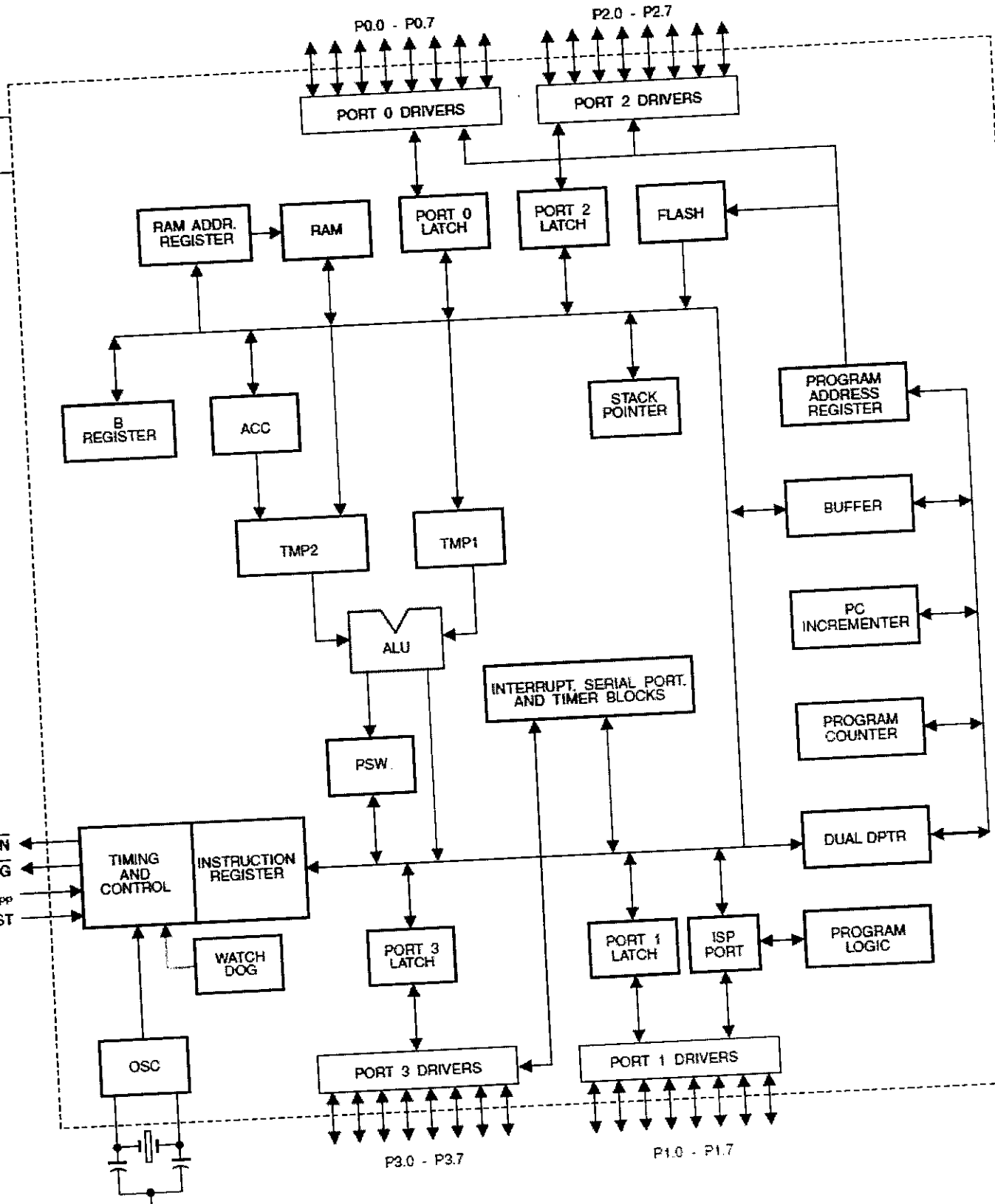
- Compatible with MCS®-51 Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory

– Endurance: 10,000 Write/Erase Cycles

- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option



3.3 INTERNAL ARCHITECTURE



.4 Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

3.4.1 Program Memory

If the EA pin is connected to GND, all program fetches are directed to external memory. On the AT89S52, if EA is connected to VCC, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

3.4.2 Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2). MOV 0A0H, #data Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H). MOV @R0, #data Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

3.5 UART

A universal asynchronous receiver/transmitter, abbreviated UART , is a type of "asynchronous receiver/transmitter", a piece of computer hardware that [illegible] and serial forms. UARTs are commonly used in

485. The universal designation indicates that the data format and transmission speeds are configurable and that the actual electric signalling levels and methods typically are handled by a special driver circuit external to the UART.

It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically second receive register.

3.6 INTERRUPTS

The AT89S52 has a total of six interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once. Note that Table 13-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products. Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

3.7 OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 16-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clock-ing circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

CHAPTER 4

SERIAL COMMUNICATION

4.1 MAX-232

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232 voltage levels from a single 5V supply. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V and can accept ±30V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232 levels.

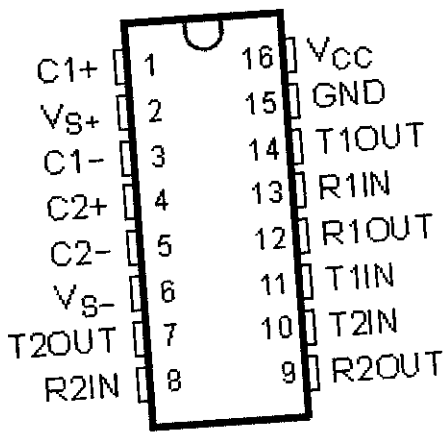


Fig 4.1 Pin configuration of MAX 232

PIN NO	DESCRIPTION
1	The positive terminal of capacitor C1 is connected.
2	A supply voltage of +5V
3	Negative terminal of C1
4	Positive terminal of C2

6	Negative supply of -5V
7	Driver 2 output(RS 232)
8	Receiver 2 input(RS 232)
9	Receiver 2 output(TTL)
10	Driver 2 input(TTL)
11	Driver 1 input(TTL)
12	Receiver 1 output(TTL)
13	Receiver 1 input(TTL)
14	Driver 1 output (RS 232)
15	ground
16	VCC (+5V)

Table 4.1 Pin description of MAX 232

4.2 RS-232 STANDARDS

1.Most widely used serial I/O interfacing standard.

2.Used in PC's and numerous types of equipments.

3.it is not compatible with I/O voltage levels of TTL logic family.

VOLTAGE LEVELS IN RS-232

1.Logic high(1) represented as -3 to -25

2.Logic low(0) represented as +3 to +25

3.-3 to +V not defined.

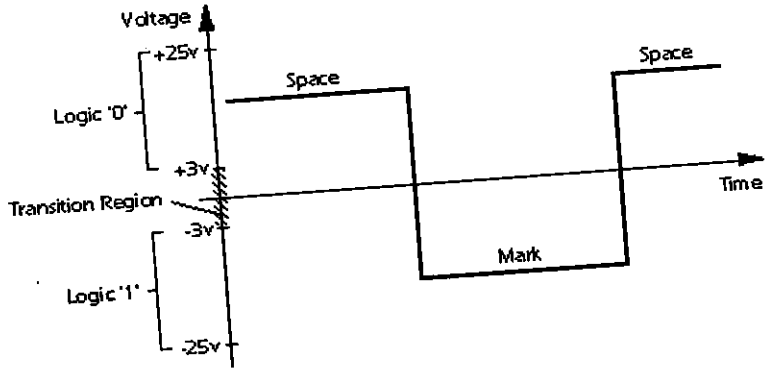


Fig 4.2 Figure of voltage levels of RS 232

4.3 RS-232 LEVEL CONVERTERS

Usually all the digital ICs work on TTL or CMOS voltage levels which cannot be used to communicate over RS-232 protocol. So a voltage or level converter is needed which can convert TTL to RS232 and RS232 to TTL voltage levels.

The most commonly used RS-232 level converter is MAX232. This IC includes charge pump which can generate RS232 voltage levels (-10V and +10V) from 5V power supply. It also includes two receiver and two transmitters and is capable of full-duplex UART/USART communication.

4.4 RS 232 INTERFACE

1. RS=232 was introduced in 1960, and is currently the most widely used communication protocol. It is simple, inexpensive to implement, and though relatively slow it is more than adequate for most simple serial communication devices such as keyboards and mice.

2. 232 is a single-ended data transmission system,which means that it uses a single wire for data transmission.

3. since useful communication is generally two way,a two wire system is

4.5 RS 232 PINS

The table provides the pins and the labels for the RS 232 cable,commonly reffered to as DB-25 connector

The standard for RS 232 and similar interfaces usually restrict RS 232 to 20Kbps or less and line length of 15m or less.RS 232 is fair more robust than the traditional limits of 20Kbps over a 15m line would imply RS 232 as oerfectly adequate at speed upto 200Kbps Most RS 232 ports on mainframe and midrange computers are capable of far higher speeds than their rated 19.2Kbps. Usually these 1000 speed parts will run error free at 56Kbps and above 15m limitations for enable length can be strtched to about 20m for ordinary cable if well scanned and grounded, and about 100m if the cable is 10m capacity.

4.6 FEATURES OF RS 232

The essential features of RS 232 is the signals are carried as signla voltages referred to a common earth and print data to a common earth pin data is transmitted and received on pins 2&3 respectively. Data Set Ready (DSR) is an indication for the data set. i.e, the modem DSU/CSU i.e, it is on. Similarly, DTR indicates to the data set that the DTE is on. Data carrier (DCD) indicates that the carrier for transmit data is on. Pins 4&5 carry the RTS and CTS signals. In most situations RTS and CTS constantly go throughtout the communication session. However when the DTE is connected to a turn carrier on the modem on and off. On a multipoint linear, it is imperative that only one station is tranmitting at a line when a station wants to transmit, it raises RTS the modem turns on carrier.

The truth table for RS 232

Signal>+3V=0

Signal <-3V=1

signal level usually swings between +12V and -12V, the

CHAPTER 5

LCD DISPLAY

5.1 INTRODUCTION

LCD's also are used as numerical indicators, especially in digital watches where their much smaller current needs than LED displays (microamperes compared with mill amperes) prolong battery life. Liquid crystals are organic (carbon) compounds, which exhibit both solid and liquid properties. A 'cell' with transparent metallic conductors, called electrodes, on opposite daces, containing a liquid crystal, and on which light falls, goes 'dark' when a voltage is applied across the electrodes. The effect is due to molecular rearrangement within the liquid crystal. The LCD display used in this project consists of 2 rows. Each row consists of maximum 16 characters. So using this display only maximum of 32 characters can be displayed

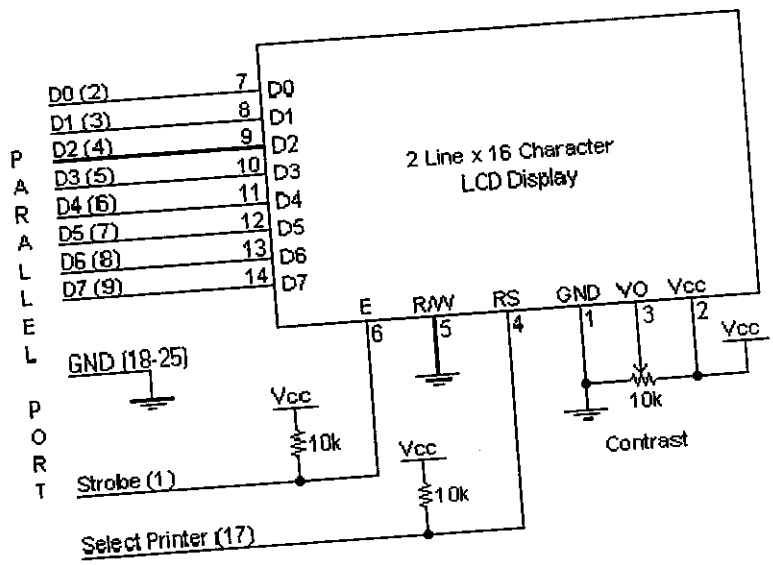


Fig 5.1 Schematic diagram of LCD display

5.2 CIRCUIT DESCRIPTION

- The LCD panel's Enable (E) of pin (6) and Register Select (RS) of pin (4) are connected to the Control Port (port 2).
- The Control Port is an open collector / open drain output. While all ports except port 0 have internal pull-up resistors, hence we incorporate the two 10K external pull up resistors, the circuit is more portable for a wider range of devices, some of which may have no internal pull up resistors.
- There is no need to make the Data bus into reverse direction. Hence hard wire the R/W line pin (5) of the LCD panel, into write mode. This will cause no bus conflicts on the data lines. As a result, read back the LCD's internal Busy Flag is not possible, which tells us if the LCD has accepted and finished processing the last instruction. This problem is overcome by inserting known delays into our program.
- The 10k Potentiometer controls the contrast of the LCD panel through V0 of pin (3). Pin (1) is ground.

The lines D0-D7 are called data lines they are connected with the port 0 through internal pull up resistors. They belong to the pins (7-14) .pin (12) forms the supply VCC.

5.3 FEATURES OF LCD DISPLAY

- 16 Characters x 2 Lines.
- 5 x 7 Dots with Cursor.
- Built in Controller.
- +5v Power Supply (Also Available for +3V).

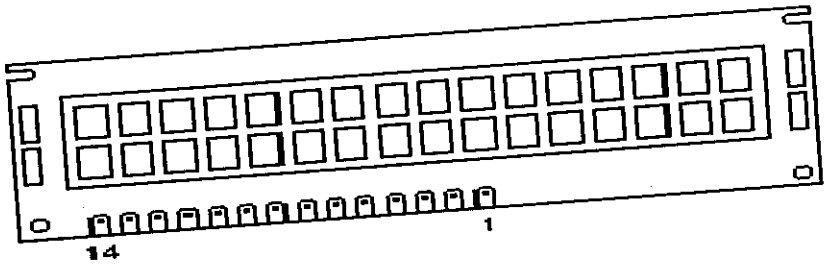


Fig 5.2 Schematic view of LCD display

5.4 MAJOR STEPS IN LCD DISPLAY

Major task in LCD interfacing is the initialization sequence. In LCD initialization you have to send command bytes to LCD. Here you set the interface mode, display mode, address counter increment direction, set contrast of LCD, horizontal or vertical addressing mode, color format. This sequence is given in respective LCD driver datasheet. Studying the function set of LCD lets you know the definition of command bytes. It varies from one LCD to another. If you are able to initialize the LCD properly 90% of your job is done.

Next step after initialization is to send data bytes to required display data RAM memory location. Firstly set the address location using address set command byte and then send data bytes using the DDRAM write command. To address specific location in display data RAM one must have the knowledge of how the address counter is incremented.

5.5 COMMANDS AND INSTRUCTION SET

Only the instruction register (IR) and the data register (DR) of the LCD can be controlled by the MCU. Before starting the internal operation of the LCD, control information is temporarily stored into these registers to allow

gnals sent from the MCU. These signals, which include register selection gnal (RS), read/write signal (R/W), and the data bus (DB0 to DB7), make up ne LCD instructions (Table 3). There are four categories of instructions that:

- Designate LCD functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

COMMANDS	D7	D6	D5	D4	D3	D2	D1	D0	HEXADECIMAL VALUE
CLEAR DISPLAY	0	0	0	0	0	0	0	1	01
DISPLAY & CURSOR HOME	0	0	0	0	0	0	1	X	02 or 03
CHARACTER ENTRY MODE	0	0	0	0	0	0	1/D	S	04 to 07
DISPLAY ON AND OFF	0	0	0	0	1	D	U	B	08 to 0F
DISPAY/ CURSOR SHIFT	0	0	0	1	D/C	R/L	X	X	10 to 1F
FUNCTION SET	0	0	1	8/4	2/1	10/7	X	X	20 to 3F
SET DDRAM ADDRESS	0	1	A	A	A	A	A	A	40 to 7F
SET DISPLAY ADDRESS	0	A	A	A	A	A	A	A	80 to FF

Table 5.1 LCD commands table

1/D - '**1**' corresponds to increment

'**0**' corresponds to decrement

S - '**1**' display on

U - '**1**' corresponds to cursor underline on

'**0**' cursor underline off

B -'**1**' corresponds to cursor blink on

'**0**' corresponds to cursor underline off

R/L -'**1**' corresponds to right shift

'**0**' corresponds to left shift

8/4 -'**1**' corresponds to 8bit interface

'**0**' corresponds to 4 bit interface

2/1 -'**1**' corresponds to 2 line mode.

'**0**' corresponds to 4 line mode.

10/7 -'**0**' corresponds to 5*10 dot frame format

'**1**' corresponds to 5*7 display format

CHAPTER 6

RF TRANSCEIVER

6.1 INTRODUCTION

The 433.92 MHz RF Transmitter allows users to easily send serial data, robot control, or other information wirelessly. When paired with the matched RF Receiver, reliable wireless communication is as effortless as sending serial data. The power-down (PDN) pin may be used to place the module into a low power state (active low), or left floating (it is tied high internally).

6.2 FEATURES

- High-speed data transfer rates (1200 ~ 19.2k Baud depending on controller used)
- SIP header allows for ease of use with breadboards
- Compatible with all BASIC Stamp® modules (including BS1 and Javelin Stamp) and SX chips
- As easy to use as simple SEROUT/SERIN PBASIC instructions
- Power-down mode for conservative energy usage (longer battery life)
- Line-of-sight range of 500 feet (or greater depending on conditions)

6.3 THEORY OF OPERATION

Short for Radio Frequency, RF refers to the frequencies that fall within the electromagnetic spectrum associated with radio wave propagation. When applied to an antenna, RF current creates electromagnetic fields that propagate the applied signal through space. Any RF field has a wavelength that is inversely proportional to the frequency. This means that the frequency of an RF signal is inversely proportional to the wavelength of the field. The Parallax RF modules utilize a frequency of 433.92 MHz, this works out to be a (2.26 feet, or 7.3e-17 light-years).

433.92 MHz falls into the Ultra High Frequency (UHF) designation, which is defined as the frequencies from 300 MHz ~ 3 GHz. UHF has free-space wavelengths of 1 m ~ 100 mm (3.28 ~ 0.33 feet or 1.05e-16 ~ 1.05e-17 light-years).

6.4 RF TRANSMITTER

6.4.1 Overview

The STT-433 is ideal for remote control applications where low cost and longer range is required. The transmitter operates from a 1.5-12V supply, making it ideal for battery-powered applications. The transmitter employs a SAW-stabilized oscillator, ensuring accurate frequency control for best range performance. Output power and harmonic emissions are easy to control, making FCC and ETSI compliance easy. The manufacturing-friendly SIP style package and low-cost make the STT-433 suitable for high volume applications.

6.4.2 Features

- 433.92 MHz Frequency
- Low Cost
- 1.5-12V operation
- 11mA current consumption at 3V
- Small size
- 4 dBm output power at 3V

N DESCRIPTION

ig 6.1

Pin Name	Description
ANT	50 ohm antenna output. The antenna port impedance affects output power and harmonic emissions. An L-C low-pass filter may be needed to sufficiently filter harmonic emissions. Antenna can be single core wire of approximately 17cm length or PCB trace antenna.
VCC	Operating voltage for the transmitter. VCC should be bypassed with a .01uF ceramic capacitor and filtered with a 4.7uF tantalum capacitor. Noise on the power supply will degrade transmitter noise performance.
DATA	Digital data input. This input is CMOS compatible and should be driven with CMOS level inputs.
GND	Transmitter ground. Connect to ground plane.

Table 6.1

6.4.4 SPECIFICATION

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Voltage	Vcc	1.5	3.0	12	Volts DC
Operating Current Data = VCC	Icc	-	11mA @3V 59mA @5V	-	mA
Operating Current Data = GND	Icc	-	100	-	uA
Frequency Accuracy	TOL fc	-75	0	+75	Khz
Center Frequency	Fc	-	433	-	Mhz
RF Output Power		-	4 dBM@3V (2 mW) 16 dBM@5V (39 mW)		dBm / m
Data Rate		200	1K	3K	BPS
Temperature		-20		+60	Deg. C
Power up delay			20		ms

Table 6.2

6.4.5 OPERATION

OOK(On Off Keying) modulation is a binary form of amplitude modulation. When a logical 0 (data line low) is being sent, the transmitter is off, this state the transmitter current is very low,

tate, the module current consumption is at its highest, about 11mA with a 3V power supply.

OOK is the modulation method of choice for remote control applications where power consumption and cost are the primary factors. Because OOK transmitters draw no power when they transmit a 0, they exhibit significantly better power consumption than FSK transmitters.

OOK data rate is limited by the start-up time of the oscillator. High-Q oscillators which have very stable center frequencies take longer to start-up than low-Q oscillators. The start-up time of the oscillator determines the maximum data rate that the transmitter can send.

6.5 RF RECEIVER

6.5.1 Overview

The STR-433 is ideal for short-range remote control applications where cost is a primary concern. The receiver module requires no external RF components except for the antenna. It generates virtually no emissions, making FCC and ETSI approvals easy. The super-regenerative design exhibits exceptional sensitivity at a very low cost. The manufacturing-friendly SIP style package and low-cost make the STR-433 suitable for high volume applications.

6.5.2 Features

- Low Cost
- 5V operation
- 3.5mA current drain
- No External Parts are required
- Receiver Frequency: 433.92 MHZ
- Typical sensitivity: -105dBm
- IF Frequency: 1MHz

6.5.3 PIN DESCRIPTION

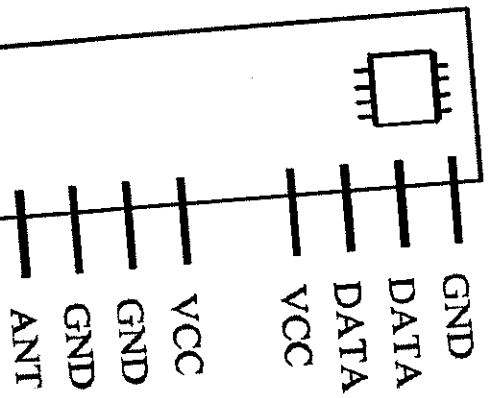


Fig 6.2

Pin Name	Description
ANT	Antenna input.
GND	Receiver Ground. Connect to ground plane.
VCC(5V)	VCC pins are electrically connected and provide operating voltage for the receiver. VCC can be applied to either or both. VCC should be bypassed with a .1µF ceramic capacitor. Noise on the power supply will degrade receiver sensitivity.
DATA	Digital data output. This output is capable of driving one TTL or CMOS loa It is a CMOS compatible output.

Table 6.3

6.5.4 SPECIFICATION

Parameter	Symbol	Min	Typ.	Max	Uni
Operating Voltage	Vcc	4.5	5.0	5.5	VDC
Operating Current	Icc	-	3.5	4.5	mA
Reception Bandwidth	BW rx	-	1.0	-	MHz
Center Frequency	Fc	-	433.92	-	MHz
Sensitivity	-	-	-105	-	dBm
Max Data Rate	-	300	1k	3K	Kbit/
Turn On Time	-	-	25	-	ms
Operating Temperature	T op	-10	-	+60	°C

3.5.5 OPERATION

The STR-433 uses a super-regenerative AM detector to demodulate the incoming AM carrier. A super-regenerative detector is a gain stage with positive feedback greater than unity so that it oscillates. An RC-time constant is included in the gain stage so that when the gain stage oscillates, the gain will be lowered over time proportional to the RC time constant until the oscillation eventually dies. When the oscillation dies, the current draw of the gain stage decreases, charging the RC circuit, increasing the gain, and ultimately the oscillation starts again. In this way, the oscillation of the gain stage is turned on and off at a rate set by the RC time constant. This rate is chosen to be super-audible but much lower than the main oscillation rate. Detection is accomplished by measuring the emitter current of the gain stage. Any RF input signal at the frequency of the main oscillation will aid the main oscillation in restarting. If the amplitude of the RF input increases, the main oscillation will stay on for a longer period of time, and the emitter current will be higher. Therefore, we can detect the original base-band signal by simply low-pass filtering the emitter current.

The average emitter current is not very linear as a function of the RF input level. It exhibits a 1/ln response because of the exponentially rising nature of oscillator start-up. The steep slope of a logarithm near zero results in high sensitivity to small input signals.

CHAPTER 7

DECODER AND ENCODER UNIT

7.1 DECODER

7.1.1 Features

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- Low standby current
- Capable of decoding 12 bits of information
- Binary address setting
- Received codes are checked 3 times
- Address/Data number combination
- HT12D: 8 address bits and 4 data bits
- HT12F: 12 address bits only
- Built-in oscillator needs only 5% resistor
- Valid transmission indicator
- Easy interface with an RF or an infrared transmission medium
- Minimal external components
- Pair with Holtek_s 212 series of encoders
- 18-pin DIP, 20-pin SOP package

7.1.2 DESCRIPTION

The 212 decoders are a series of CMOS LSIs for remote control system applications. They are paired with Holtek_s 212 series of encoders (refer to the encoder/decoder cross reference table). For proper operation, a pair of encoder/decoder with the same number of addresses and data format should be chosen.

The decoders receive serial addresses and data from a programmed 212 series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. They compare the serial input data three times continuously with their local addresses. If no error or unmatched codes are found, the input data codes are decoded and then transferred to the output pins. The VT pin also goes high to indicate a valid transmission.

The 212 series of decoders are capable of decoding information's that consist of N bits of address and 12_N bits of data. Of this series, the HT12D is arranged to provide 8 address bits and 4 data bits, and HT12F is used to decode 12 bits of address information.

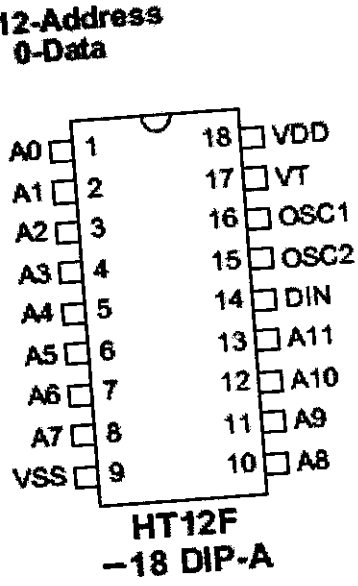


Fig 7.1 Decoder Pin

7.2 ENCODER

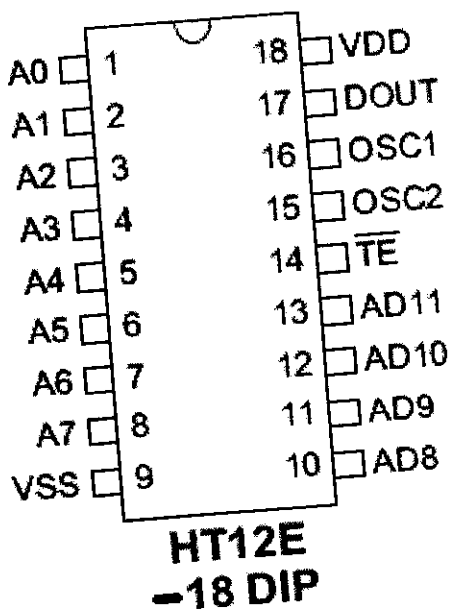
7.2.1 FEATURES

- Operating voltage
- 2.4V~5V for the HT12A
- 2.4V~12V for the HT12E
- Low power and high noise immunity CMOS technology
- Low standby current: 0.1_A (typ.) at VDD=5V
- HT12A with a 38kHz carrier for infrared Transmission medium
- Minimum transmission word
- Four words for the HT12E

- Built-in oscillator needs only 5% resistor
- Data code has positive polarity
- Minimal external components
- HT12A/E: 18-pin DIP/20-pin SOP package

7.2.2 DESCRIPTION

The 212 encoders are a series of CMOS LSIs for remote control system applications. They are capable of encoding information which consists of N address bits and 12_N data bits. Each address/ data input can be set to one of the two logic states. The programmed addresses/data are transmitted together with the header bits via an RF or an infrared transmission medium upon receipt of a trigger signal. The capability to select a TE trigger on the HT12E or a DATA trigger on the HT12A further enhances the application flexibility of the 212 series of encoders. The HT12A additionally provides a 38kHz carrier for infrared systems.



7.2 Encoder Pin

CHAPTER 10

SOFTWARE

10.1 KEIL-C

The Keil C51 C Compiler for the 8051 microcontroller is the most popular 8051 C compiler in the world. It provides more features than any other 8051 C compiler available today.

The C51 Compiler allows you to write 8051 microcontroller applications in C that, once compiled, have the efficiency and speed of assembly language. Language extensions in the C51 Compiler give you full access to all resources of the 8051.

The C51 Compiler translates C source files into relocatable object modules which contain full symbolic information for debugging with the μVision Debugger or an in-circuit emulator. In addition to the object file, the compiler generates a listing file which may optionally include symbol table and cross reference information.

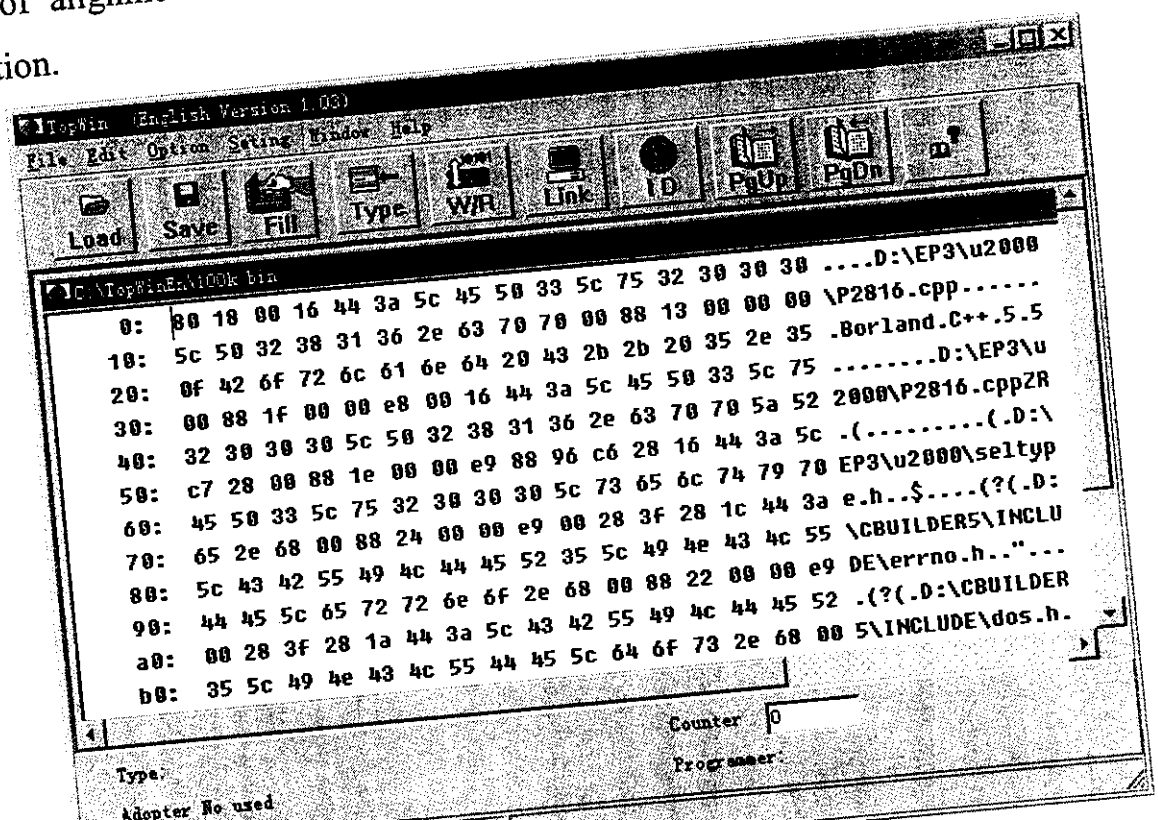
10.1.1 FEATURES

- Nine basic data types, including 32-bit IEEE floating-point,
- Flexible variable allocation with **bit**, **data**, **bdata**, **idata**, **xdata**, and **pdata** memory types,
- Interrupt functions may be written in C,
- Full use of the 8051 register banks,
- Complete symbol and type information for source-level debugging,
- Use of **AJMP** and **ACALL** instructions,
- Bit-addressable data objects,

0.2 TOPWIN

TopWin, a type of software developed for TOP series programmers, adapts to the TOP hardware products of a new generation. TopWin has abandoned its method of one type of software matching for one mode of TOP product by operating different mode of hardware units. TopWin supports automatic identification of hardware mode and function. Once TopWin connects to hardware unit successfully, the name of hardware unit will appear at the bottom of window. The current basic modes that TopWin supported include TOP853, TOP2004, TOP2005 and TOP2048. Product of new mode developed in the future will be supported by new version of TopWin software.

TopWin supports multi-window operation, namely, it can connect multiple programmers on a computer to write device without any interference. Mode of programmer can be same or different. TopWin opens all devices in order of alignment. In theory, the number of connected devices is out of limitation.



CHAPTER 11

CODING AND FLOWCHART

11.1 CODING FOR TRAIN A

```
#include<reg52.h>

#include<8lcd.h>


 sbit rx0=P1^0;

 sbit rx1=P1^1;

 sbit rx2=P1^2;

 sbit rx3=P1^3;


  sbit tx0=P1^4;

  sbit tx1=P1^5;

  sbit tx2=P1^6;

  sbit tx3=P1^7;


   sbit buzzer=P2^7;


   sbit m1p=P3^4;
```

```
bit m2p=P3^6;
bit m2n=P3^7;

void main()
{
        unsigned char i=0,rfid[16];
        unsigned char condition=0;
         SCON=0x50;
         TMOD=0x20;
         TH1=0xFD;
         TR1=1;
         lcd_init();
         lcd_data('S');
          m1p=0;
          m1n=0;
          m2p=0;
          m2n=0;
          tx0=0;
          tx1=0;
```

```
tx3=0;
SBUF='S';
while(1)
{
        buzzer=1;
        lcd_command(0x80);
        lcd_display("RFID CARD NO:");
        for(i=0;i<8;i++)
        {
                RI=0;
                while(RI==0)
                {
                        if(rx0==1&&rx1==0&&rx2==0&&rx3==0)//1000----
--->track 1 train a
                        {
                                if(condition=='1')
                                {
                                        m1p=0;
                                        m1n=0;
                                        m2p=0;
```

```
                buzzer=0;

            }

        }

        else
(rx0==1&&rx1==0&&rx2==1&&rx3==0)//1010------->track 2 train a

        {

            if(condition=='2')

            {

                m1p=0;

                m1n=0;

                m2p=0;

                m2n=0;

                buzzer=0;

            }

        }

        else

        {

            m1p=1;

            m1n=0;

            m2p=0;
```

```
            }
        }
        rfid[i]=SBUF;
}
lcd_command(0xC0);
 lcd_display(rfid);
  if(rfid[i-1]=='1')
   {
          tx0=0;
           tx1=1;
            tx2=0;
             tx3=0;
              condition='1';
       }
        else if(rfid[i-1]=='2')
         {
              tx0=0;
               tx1=1;
                tx2=0;
```

```
        condition='1';
}
else if(rfid[i-1]=='6')
 {
        tx0=0;
        tx1=1;
        tx2=1;
        tx3=0;
        condition='2';
    }
    else if(rfid[i-1]=='7')
     {
          tx0=0;
          tx1=1;
          tx2=1;
          tx3=0;
          condition='2';
       }
}
```

1.2 CODING FOR TRAIN B

```
include<reg52.h>

include<8lcd.h>


sbit rx0=P1^0;

sbit rx1=P1^1;

sbit rx2=P1^2;

sbit rx3=P1^3;


sbit tx0=P1^4;

sbit tx1=P1^5;

sbit tx2=P1^6;

sbit tx3=P1^7;


sbit buzzer=P2^7;


sbit m1p=P3^4;

sbit m1n=P3^5;

sbit m2p=P3^6;
```

```
d main()

    unsigned char i=0,rfid[16];
    unsigned char condition=0;
     SCON=0x50;
     TMOD=0x20;
     TH1=0xFD;
      TR1=1;
      lcd_init();
       lcd_data('S');
        m1p=0;
         m1n=0;
          m2p=0;
           m2n=0;
            tx0=0;
             tx1=0;
              tx2=0;
               tx3=0;
```

```
while(1)
 {
        lcd_command(0x80);
        lcd_display("RFID CARD NO:");
         for(i=0;i<8;i++)
         {
                RI=0;
                 while(RI==0)
                 {
                        if(rx0==0&&rx1==1&&rx2==0&&rx3==0)//0100----
--->track 1 train b
                        {
                                if(condition=='1')
                                {
                                        m1p=0;
                                        m1n=0;
                                        m2p=0;
                                        m2n=0;
                                        buzzer=0;
                                }
```

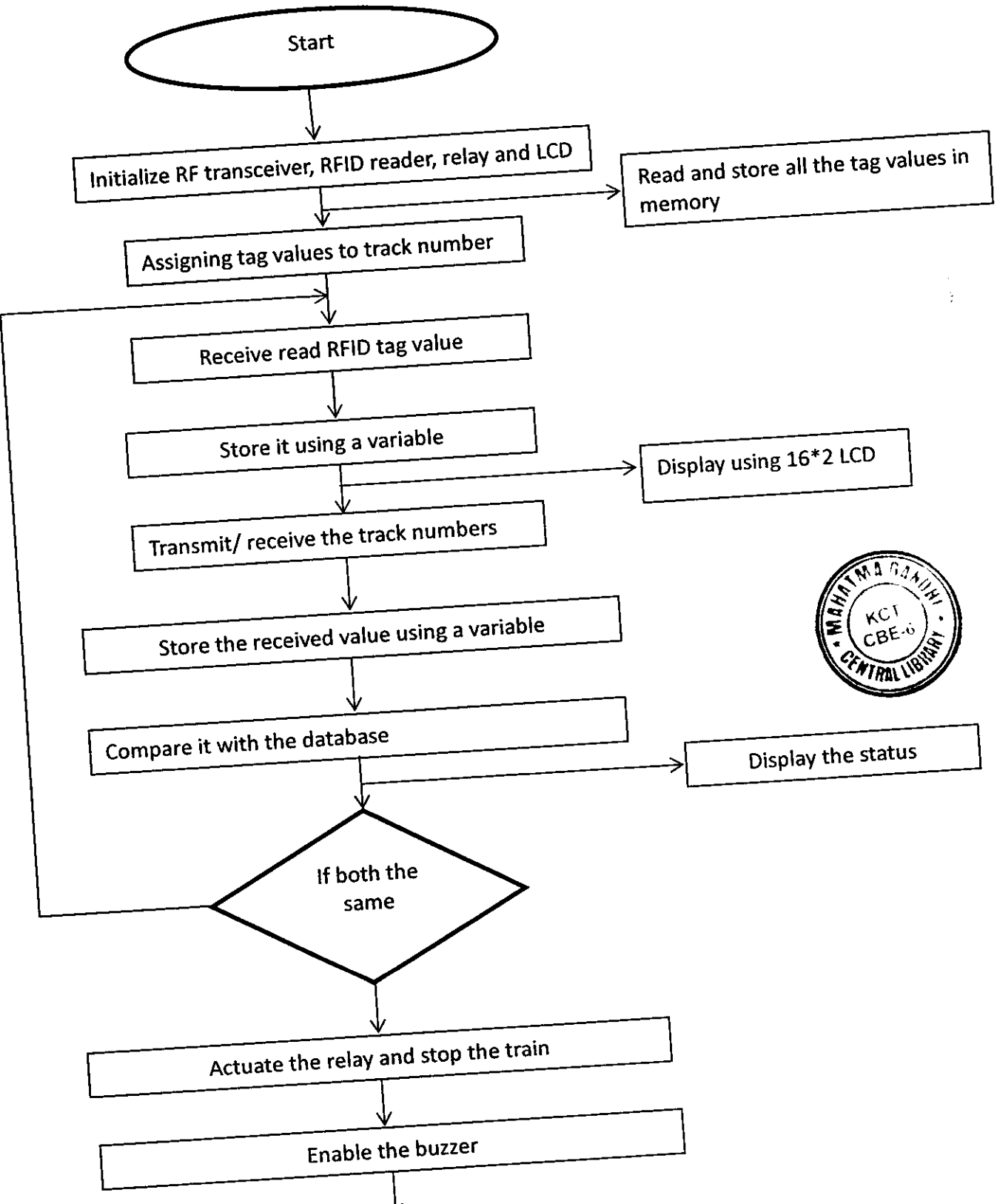
```
                else
x0==0&&rx1==1&&rx2==1&&rx3==0)//0110------->track 2 train b
                {
                    if(condition=='2')
                    {
                        m1p=0;
                        m1n=0;
                        m2p=0;
                        m2n=0;
                        buzzer=0;
                    }
                }
                else
                {
                        m1p=1;
                        m1n=0;
                        m2p=0;
                        m2n=1;
                    }
                }
```

```
}
lcd_command(0xC0);
 lcd_display(rfid);
 if(rfid[i-1]=='1')
  {
          tx0=1;
           tx1=0;
           tx2=0;
           tx3=0;
            condition='1';
     }
     else if(rfid[i-1]=='2')
      {
             tx0=1;
              tx1=0;
              tx2=0;
              tx3=0;
               condition='1';
         }
```

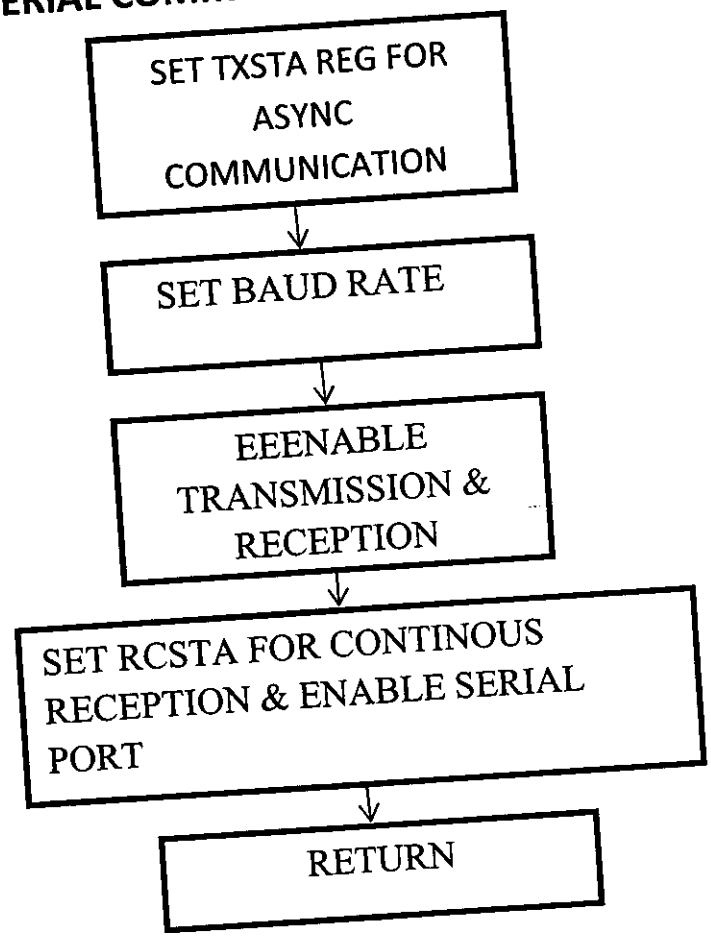
```
{
        tx0=1;
        tx1=0;
        tx2=1;
        tx3=0;
        condition='2';
    }
    else if(rfid[i-1]=='7')
    {
        tx0=1;
        tx1=0;
        tx2=1;
        tx3=0;
        condition='2';
    }
}
}
```

11.3 FLOWCHARTS

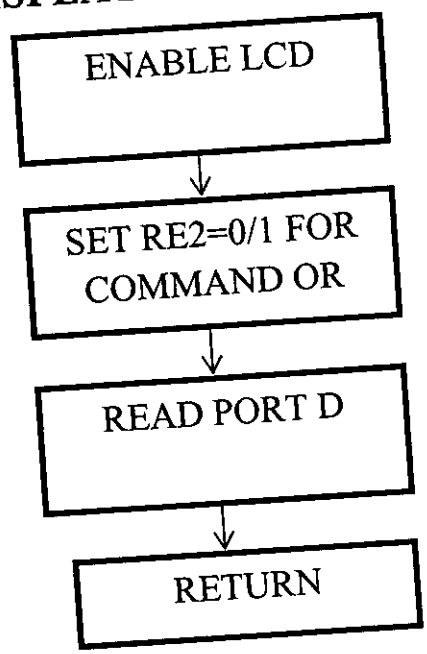
LOWCHART OF ENTIRE PROCESS



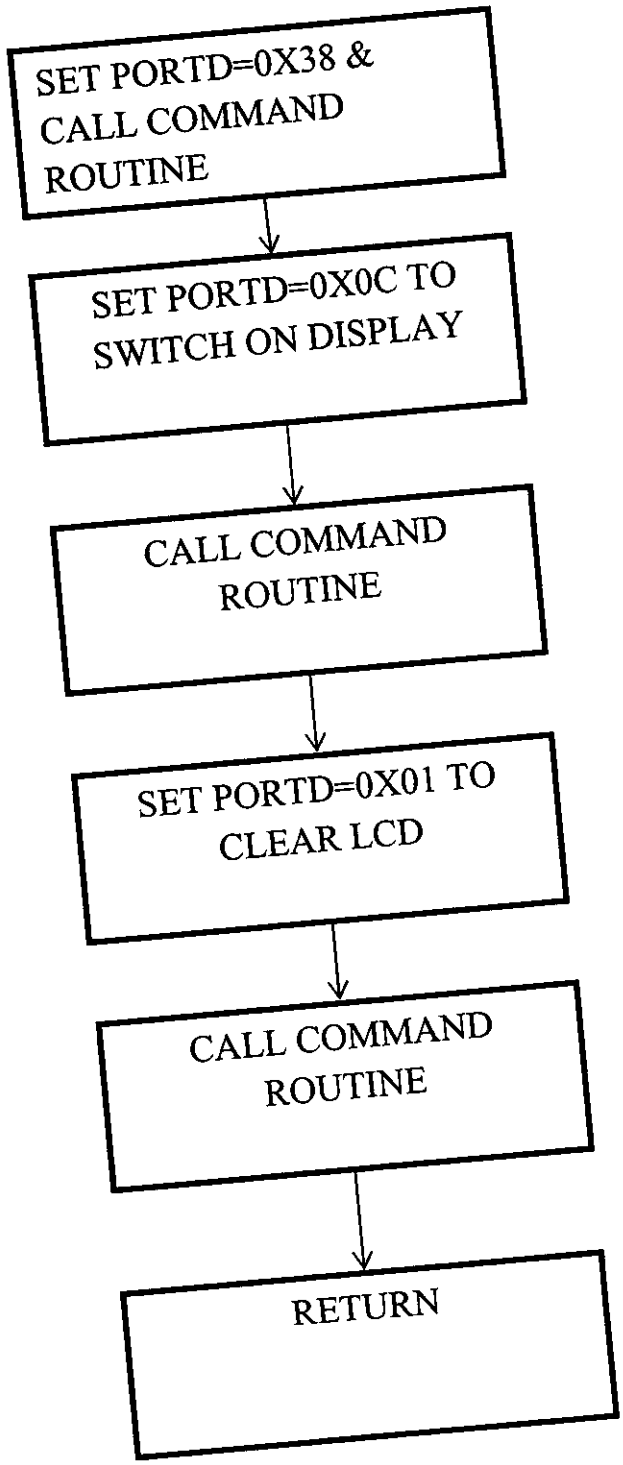
ITIALISE SERIAL COMMUNICATION



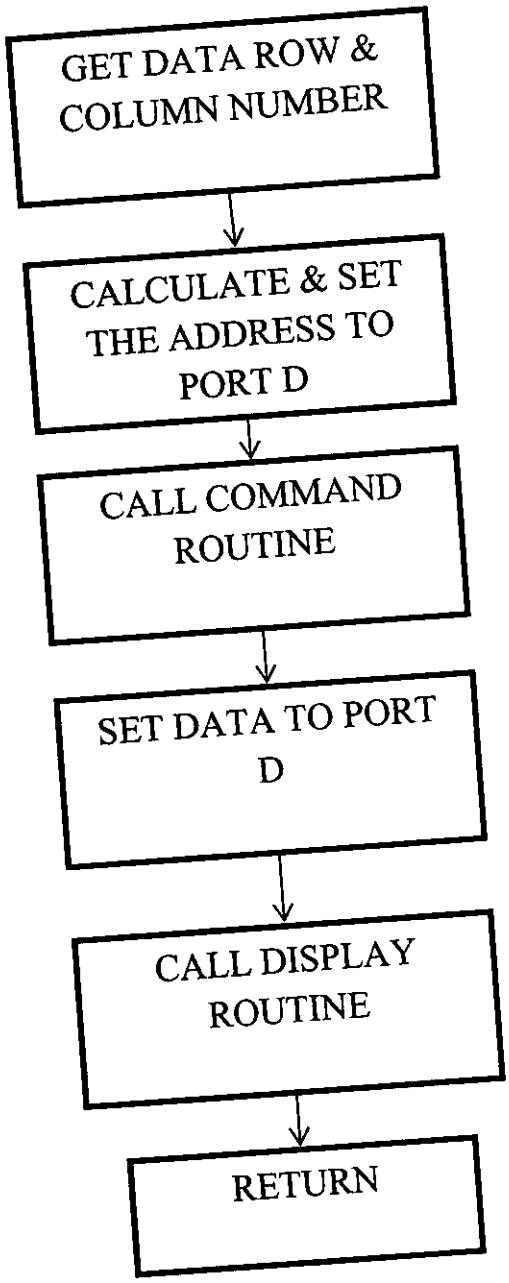
SCOMMAND/DISPLAY LCD



ITIALISING LCD



RITE LCD


GET DATA ROW & COLUMN NUMBER
CALCULATE & SET THE ADDRESS TO PORT D
CALL COMMAND ROUTINE
SET DATA TO PORT D
CALL DISPLAY ROUTINE
RETURN

CONCLUSION

Thus, if the concept of Anti-collision in Trains using RFID is implemented, system is accurate and does not raise any false alarms. Some of the number of Train collisions can be reduced or avoided altogether. The Automated important advantages that can be obtained by implementing this system are listed below.

- Man power error is reduced due to automation
- Cost of system is low compared to other systems

FUTURE EXPANSION

RF Transceivers can be placed at level crossings, as the train approaches, ıe gates of the level cross can close automatically without the need for any ıanual labour. The presences of trains entering and exiting the gates can also be ıetected consequently.

RFID tags will be able to detect the arrival of a train at a particular station and ılerts/ buzzers can be sounded to inform the passengers.

The same concept can be used to keep track of the number of trains in a terminal. Since the cost-cutting rate of RFID tags have been enormously significant in the last few years, their usage will go a long way into helping maintaining financial stability as well.

APPENDIX A

atures

- ompatible with MCS®-51 Products
- K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 10,000 Write/Erase Cycles
- .0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

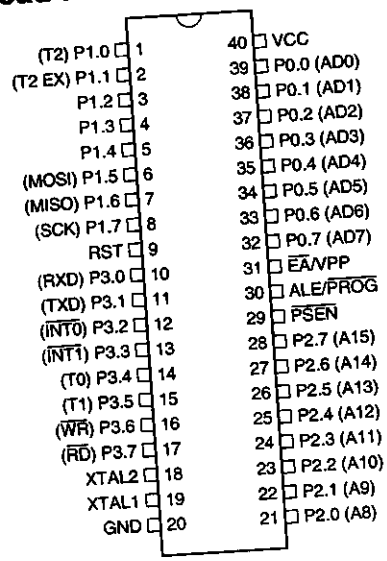
The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

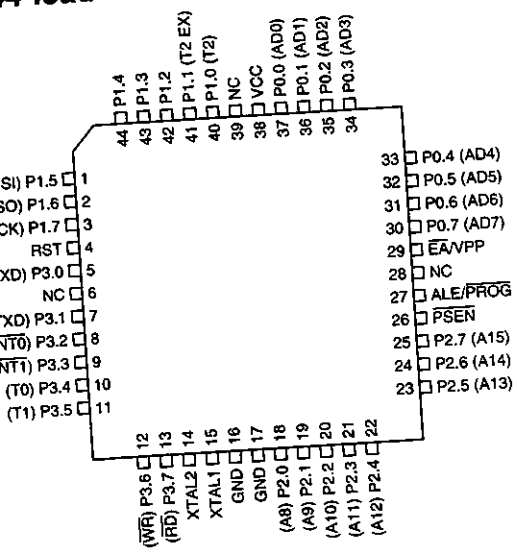
AT89S52

onfigurations

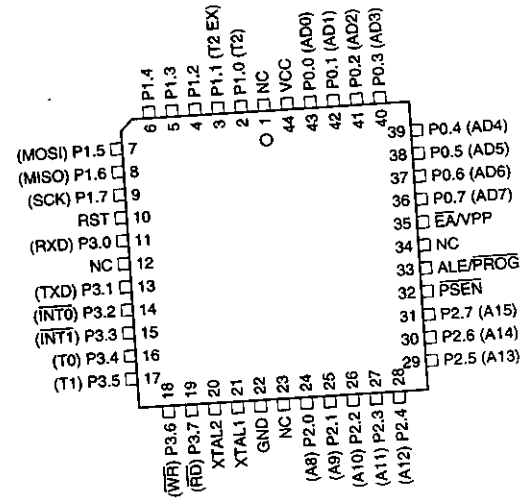
ead PDIP



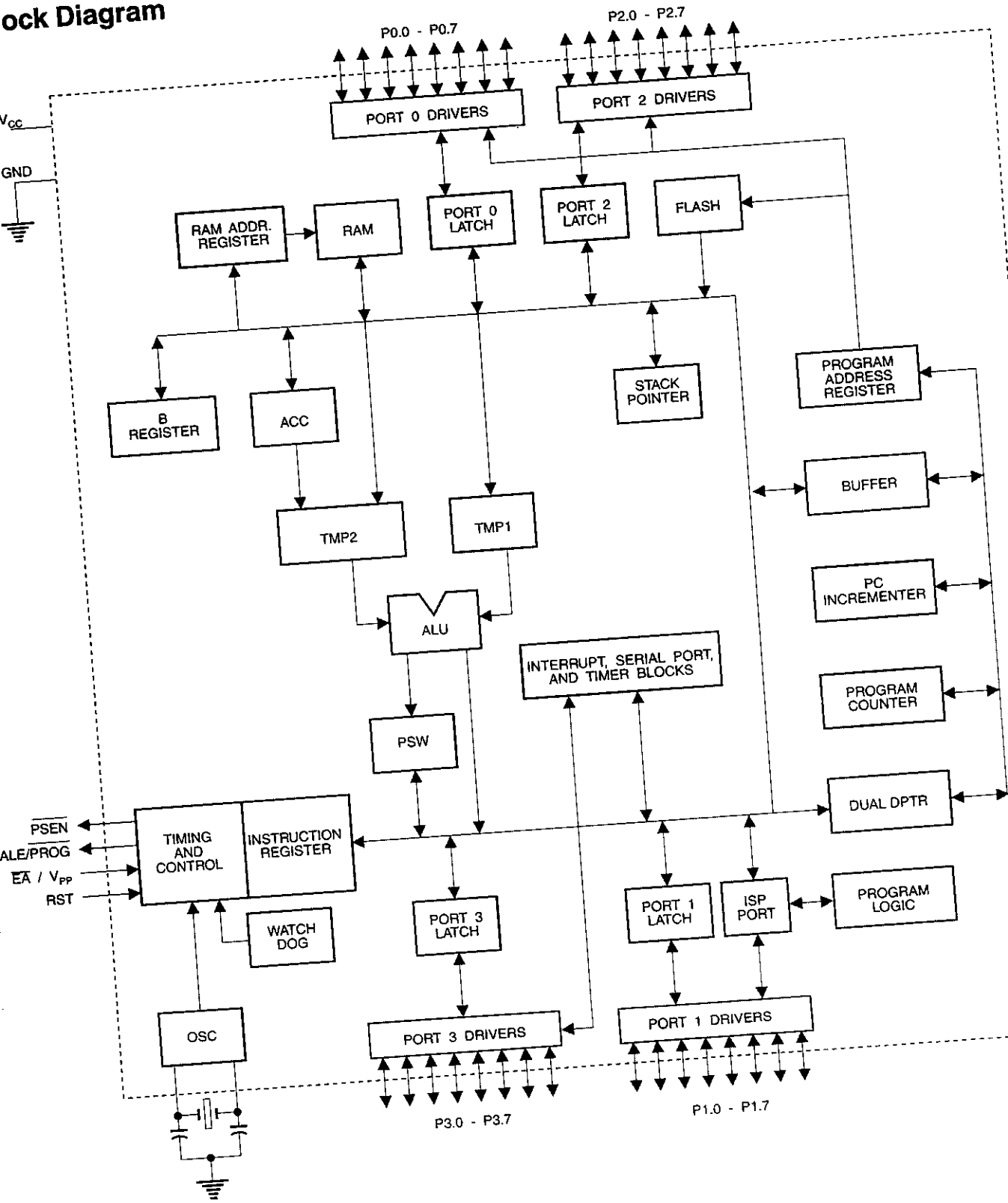
4-lead TQFP



2.3 44-lead PLCC



ock Diagram


P0.0 - P0.7
P2.0 - P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
V_{CC}
GND
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
DUAL DPTR
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

n Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

1.5 Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

...receives the high-order address bits and some control signals during Flash

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets th device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRT bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address dur accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Fla programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped ing each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled h Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode

PSEN

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown i Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be impl mented on the chip. Read accesses to these addresses will in general return random data, ar write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in futu products to invoke new features. In that case, the reset or inactive values of the new bits w always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 10-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are t Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities c be set for each of the six interrupt sources in the IP register.

AT89S52 SFR Map and Reset Values

								0FFH
								0F7H
B 00000000								0EFH
								0E7H
ACC 00000000								0DFH
								0D7H
PSW 00000000								0CFH
T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0C7H
								0BFH
IP XX000000								0B7H
P3 11111111								0AFH
IE 0X000000								0A7H
P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		9FH
SCON 00000000	SBUF XXXXXXXX							97H
P1 11111111								8FH
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		87H
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	

e 5-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H

Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

mbol	Function
2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = or TCLK = 1.
XF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must b cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
CLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial por Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
CLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial p Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
XEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Ti 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
R2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge trigge
P/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. W either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

e 5-3. AUXR: Auxiliary Register

XR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

Reserved for future expansion

SALE Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

ISRTO Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

VDIDLE Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

ual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit
ointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR A
elects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value b
ccessing the respective Data Pointer Register.

ower Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during
p. It can be set and rest under software control and is not affected by reset.

Table 5-4. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

APPENDIX B

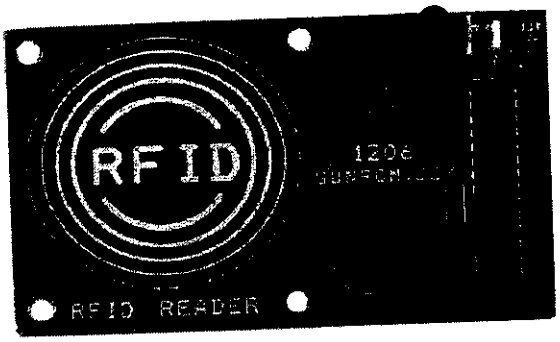
SUNROM TECHNOLOGIES
Your Source for Embedded Systems

Email: info@sunrom.com or sunrom@gmail.com
Visit us at http://www.sunrom.com

Document: Datasheet | Date: 4-Jan-10 | Model #: 1206 | Product's Page: www.sunrom.com/p-859.html

RFID Reader

Radio Frequency Identification (RFID) Card Readers provide a low-cost solution to read passive RFID transponder tags up to 7 cm away. This RFID Card Reader can be used in a wide variety of hobbyist and commercial applications, including access control, automatic identification, robotics navigation, inventory tracking, payment systems, and car immobilization. The RFID card reader read the RFID tag in range and outputs unique identification code of the tag at baud rate of 9600. The data from RFID reader can be interfaced to be read by microcontroller or PC.



Features

- Low-cost method for reading passive RFID transponder tags
- 9600 bps serial interface at 5V TTL level for direct interface to microcontrollers
- Buzzer & LED indicate valid RFID Tag detection
- Range up to 7 cm for 125 Khz RFID Cards or Keychains

Specification

Parameter	Value
Input Voltage	5V DC regulated
Output Data Speed	9600 BPS 8 Bit Data/No-Parity/1 Stop Bit
Output Data Level	5V TTL level
Detection Range	7 cm contact-less
Valid Tag in Range	Indicated by Buzzer and LED

Information

Each transponder tag contains a unique identifier (one of 2^{40}, or 1,099,511,627,776 possible combinations) that is read by the RFID Card Reader and transmitted to the host via a simple serial interface.

Communication

When the RFID Card Reader is active and a valid RFID transponder tag is placed within range of the activated reader, the unique ID will be transmitted as a 12-byte printable ASCII string serially t the host in the following format:

rt Byte x0A)	Unique ID Digit 1	Unique ID Digit 2	Unique ID Digit 3	Unique ID Digit 4	Unique ID Digit 5	Unique ID Digit 6	Unique ID Digit 7	Unique ID Digit 8	Unique ID Digit 9	Unique ID Digit 10	Stop B (0x0D

e start byte and stop byte are used to easily identify that a correct string has been received from e reader (they correspond to a line feed and carriage return characters, respectively). The middl n bytes are the actual tag's unique ID.

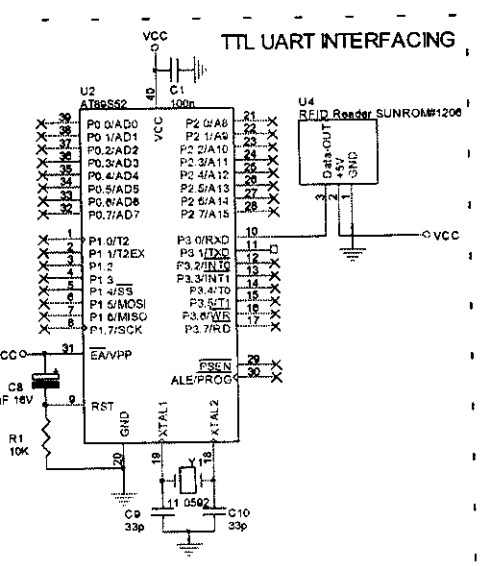
r example, for a tag with a valid ID of 0F0184F07A, the following ASCII data would be sent F0184F07A
ame data in HEX bytes can be interpreted as:
x0A, 0x30, 0x46, 0x30, 0x31, 0x38, 0x34, 0x46, 0x30, 0x37, 0x41, 0x0D

l communication is 8 data bits, no parity, 1 stop bit, and least significant bit first (8N1). The baud te is configured for 9600 bps, a standard communications speed supported by most any icroprocessor or PC, and cannot be changed. The RFID Card Reader initiates all communicatio his allows easy access to the serial data stream from any programming language that can open OM port.

sing RFID Reader

/hen powered on the RFID reader will activate a RF field waiting for a tag to come into its ran nce tag is detected, its unique ID number is read and data is sent via serial interface. The valid etecting is indicated by LED blink and Buzzer beep. The face of the RFID tag should be h arallel to the front of the antenna (where the majority of RF energy is focused). If the tag is h deways (perpendicular to the antenna) you may have difficulty getting the tag to be read. Only ansponder tag should be held up to the antenna at any time. The use of multiple tags at one ti ill cause tag collisions and confuse the reader. The tags available with us have a read distance pproximately 7 cm. Actual distance may vary slightly depending on the size of the transponder nd environmental conditions of the application.

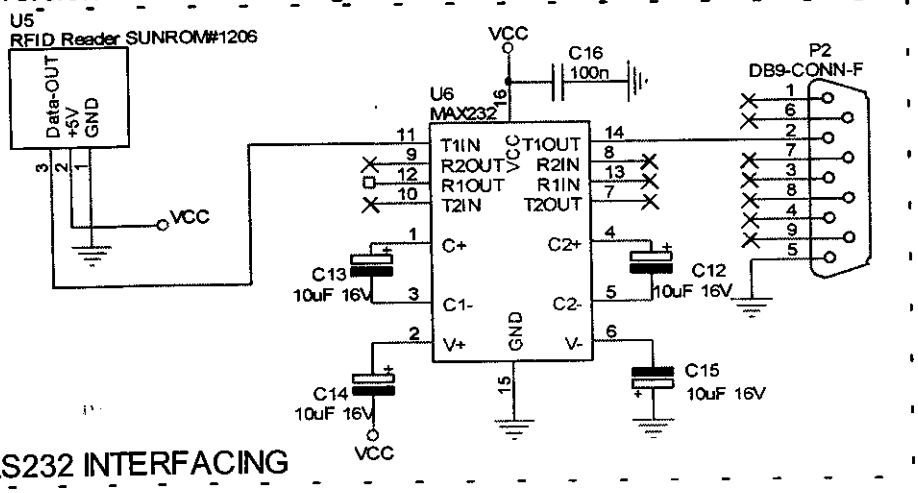
Connecting to Microcontroller



Connect data output pin of RFID reader to RXD pin of any microcontroller and configure your MCU to receive data at 9 baud rate. You also have to keep common ground signal between RFID reader and microcontroller.

onnecting to PC Using Serial Port

nce the PC uses RS232 level you cannot directly connect the data output of RFID reader. Th
ght damage the reader. The reader outputs 5V level signal. You can use a MAX232 lev
nversion to convert 5V signal to RS232 level signal. Reference diagram is given below.



RS232 INTERFACING

se Hyperterminal software which comes with Windows XP or use any other Terminal software w
llowing settings.

ata Rate: 9600 Data Bits: 8 Parity: None Stop Bit: 1 Flow Control: No

ne of the Terminal software can be downloaded from http://www.sunrom.com/files/Terminal.exe

FID Technology Overview

adio Frequency Identification (RFID) is a generic term for non-contacting technologies that u
adio waves to automatically identify people or objects. There are several methods of identificati
ut the most common is to store a unique serial number that identifies a person or object ou
icrochip that is attached to an antenna. The combined antenna and microchip are called an "RI
ansponder" or "RFID tag" and work in combination with an "RFID reader" (sometimes called
RFID interrogator").

n RFID system consists of a reader and one or more tags. The reader's antenna is used
ansmit radio frequency (RF) energy. Depending on the tag type, the energy is "harvested" by
ag's antenna and used to power up the internal circuitry of the tag. The tag will then modulate
lectromagnetic waves generated by the reader in order to transmit its data back to the reader.
eader receives the modulated waves and converts them into digital data.

here are two major types of tag technologies. "Passive tags" are tags that do not contain their o
ower source or transmitter. When radio waves from the reader reach the chip's antenna,
nergy is converted by the antenna into electricity that can power up the microchip in the
known as "parasitic power"). The tag is then able to send back any information stored on the tag
eflecting the electromagnetic waves as described above. "Active tags" have their own po
ource and transmitter. The power source, usually a battery, is used to run the microchip's circu
nd to broadcast a signal to a reader. Due to the fact that passive tags do not have their
ransmitter and must reflect their signal to the reader, the reading distance is much shorter than

ve tags. However, active tags are typically larger, more expensive, and require occasiona
vice. The Sunrom RFID Card Reader is designed specifically for passive tags.

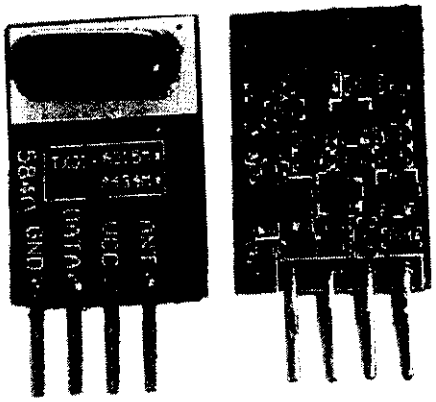
equency refers to the size of the radio waves used to communicate between the RFID syste
mponents. Just as you tune your radio to different frequencies in order to hear different rad
tions, RFID tags and readers must be tuned to the same frequency in order to communica
ectively.

ere really is no such thing as a "typical" RFID tag. The read range of a tag ultimately depends
any factors: the frequency of RFID system operation, the power of the reader, environment
nditions, physical size of the tags antenna and interference from other RF devices. Balancing
mber of engineering trade-offs (antenna size v. reading distance v. power v. manufacturing cos
e Sunrom RFID Card Reader's antenna was designed with a RFID operation at a tag re
stance of around 7 cm.

APPENDIX C

SUNROM TECHNOLOGIES
Your Source for Embedded Systems

433 MHz RF Transmitter STT-433



1. Overview

The STT-433 is ideal for remote control applications where low cost and longer range is required. The transmitter operates from a 1.5-12V supply, making it ideal for battery-powered applications. The transmitter employs a SAW-stabilized oscillator, ensuring accurate frequency control for best range performance. Output power and harmonic emissions are easy to control, making FCC and ETSI compliance easy. The manufacturing-friendly SIP style package and low-cost make the STT-433 suitable for high volume applications.

2. Features

- 433.92 MHz Frequency
- Low Cost
- 1.5-12V operation
- 11mA current consumption at 3V
- Small size
- 4 dBm output power at 3V

3. Applications

- Remote Keyless Entry (RKE)
- Remote Lighting Controls
- On-Site Paging
- Asset Tracking
- Wireless Alarm and Security Systems
- Long Range RFID
- Automated Resource Management

4. Specification

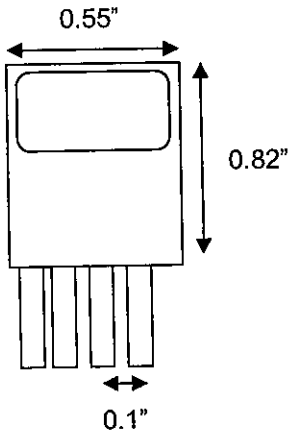
Parameter	Symbol	Min	Typ.	Max	Unit
Operating Voltage	Vcc	1.5	3.0	12	Volts DC
Operating Current Data = VCC	Icc	-	11mA @3V 59mA @5V	-	mA
Operating Current Data = GND	Icc	-	100	-	uA
Frequency Accuracy	TOL fc	-75	0	+75	Khz
Center Frequency	Fc	-	433	-	Mhz
RF Output Power		-	4 dBM@3V (2 mW) 16 dBM@5V (39 mW)		dBm / mW
Data Rate		200	1K	3K	BPS
Temperature		-20		+60	Deg. C
Power up delay			20		ms

Pin Description

Pin Name	Description
ANT	50 ohm antenna output. The antenna port impedance affects output power and harmonic emissions. An L-C low-pass filter may be needed to sufficiently filter harmonic emissions. Antenn can be single core wire of approximately 17cm length or PCB trace antenna.
VCC	Operating voltage for the transmitter. VCC should be bypassed with a .01uF ceramic capacitor and filtered with a 4.7uF tantalu capacitor. Noise on the power supply will degrade transmitter noise performance.
DATA	Digital data input. This input is CMOS compatible and should b driven with CMOS level inputs.
GND	Transmitter ground. Connect to ground plane.

Mechanical Drawing

nsions in Inches



Operation

7.1. Theory

K(On Off Keying) modulation is a binary form of amplitude modulation. When a logical 0 (dat is being sent, the transmitter is off, fully suppressing the carrier. In this state, the transmitter cu ery low, less than 1mA. When a logical 1 is being sent, the carrier is fully on. In this state, the m ent consumption is at its highest, about 11mA with a 3V power supply.

K is the modulation method of choice for remote control applications where power consumptio are the primary factors. Because OOK transmitters draw no power when they transmit a 0 bit significantly better power consumption than FSK transmitters.

K data rate is limited by the start-up time of the oscillator. High-Q oscillators which have very

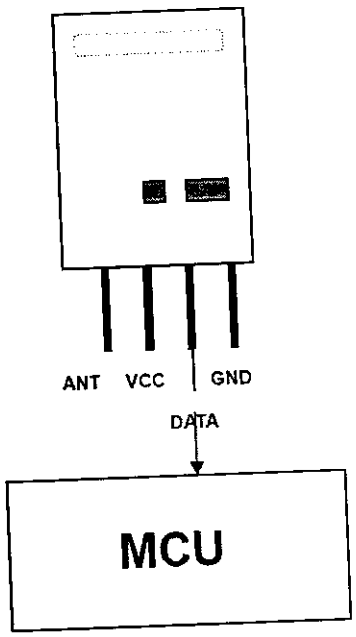
2. *Data Rate*

scillator start-up time is on the order of 40uSec, which limits the maximum data rate to 4.8 kbit/s

3. *SAW stabilized oscillator*

ransmitter is basically a negative resistance LC oscillator whose center frequency is tig
olled by a SAW resonator. SAW (Surface Acoustic Wave) resonators are fundamental freque
es that resonate at frequencies much higher than crystals.

Typical Application

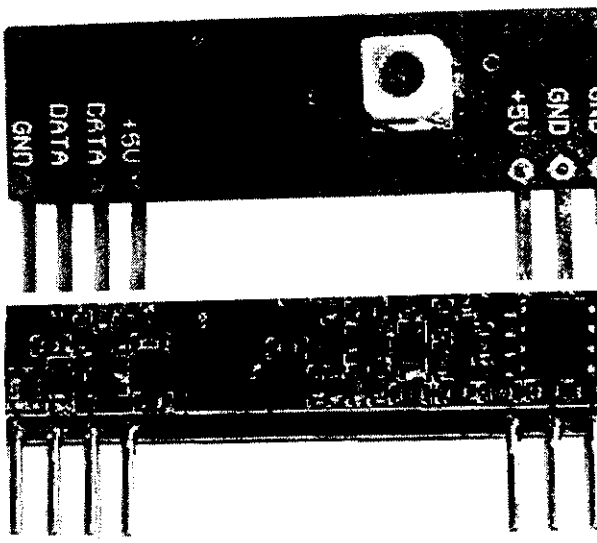


Ordering Information

rt Number	Description
T-433	433 MHz RF Transmitter

SUNROM
TECHNOLOGIES
Source for Embedded Systems

MHz RF Receiver STR-433



Overview

STR-433 is ideal for short-range remote control cations where cost is a primary concern. The ver module requires no external RF components ot for the antenna. It generates virtually no sions, making FCC and ETSI approvals easy. The r-regenerative design exhibits exceptional tivity at a very low cost. The manufacturing-friendly style package and low-cost make the STR-433 ble for high volume applications.

Features

- Low Cost
- 5V operation
- 3.5mA current drain
- No External Parts are required
- Receiver Frequency: 433.92 MHZ
- Typical sensitivity: -105dBm
- IF Frequency: 1MHz

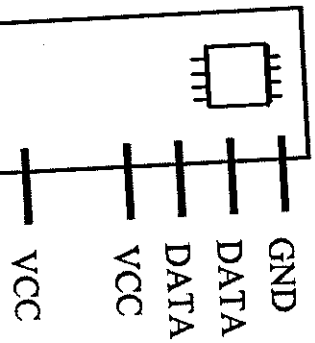
3. Applications

- Car security system
- Sensor reporting
- Automation system
- Remote Keyless Entry (RKE)
- Remote Lighting Controls
- On-Site Paging
- Asset Tracking
- Wireless Alarm and Security Systems
- Long Range RFID
- Automated Resource Management

Specification

ameter	Symbol	Min	Typ.	Max	Unit
erating Voltage	Vcc	4.5	5.0	5.5	VDC
erating Current	Icc	-	3.5	4.5	mA
ception Bandwidth	BW rx	-	1.0	-	MHz
nter Frequency	Fc	-	433.92	-	MHz
nsitivity	-	-	-105	-	dBm
x Data Rate	-	300	1k	3K	Kbit/s
rn On Time	-	-	25	-	ms
erating Temperature	T op	-10	-	+60	°C

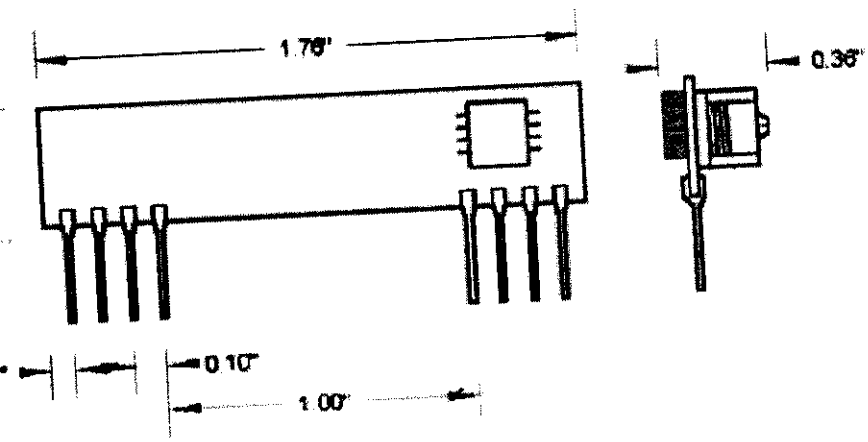
Outs



e	Description
	Antenna input.
	Receiver Ground. Connect to ground plane.
')	VCC pins are electrically connected and provide operating voltage for the receiver. VCC can be applied to either or both. VCC should be bypassed with a .1µF ceramic capacitor. Noise on the power supply will degrade receiver sensitivity.
	Digital data output. This output is capable of driving one TTL or CMOS load. It is a CMOS compatible output.

echanical Drawing

al Drawing (Dimensions in Inches)



eration

Super-Regenerative AM Detection

33 uses a super-regenerative AM detector to demodulate the incoming AM carrier. A super-
e detector is a gain stage with positive feedback greater than unity so that it oscillates. An
onstant is included in the gain stage so that when the gain stage oscillates, the gain will be
er time proportional to the RC time constant until the oscillation eventually dies. When the
dies, the current draw of the gain stage decreases, charging the RC circuit, increasing the
ultimately the oscillation starts again. In this way, the oscillation of the gain stage is turned on
a rate set by the RC time constant. This rate is chosen to be super-audible but much lower
nain oscillation rate. Detection is accomplished by measuring the emitter current of the gain
y RF input signal at the frequency of the main oscillation will aid the main oscillation in
If the amplitude of the RF input increases, the main oscillation will stay on for a longer period
nd the emitter current will be higher. Therefore, we can detect the original base-band signal by
v-pass filtering the emitter current.

age emitter current is not very linear as a function of the RF input level. It exhibits a 1/In
because of the exponentially rising nature of oscillator start-up. The steep slope of a logarithm
o results in high sensitivity to small input signals.

Data Slicer

a slicer converts the base-band analog signal from the super-regenerative detector to
TL compatible output. Because the data slicer is AC coupled to the audio output, there is
n data rate. AC coupling also limits the minimum and maximum pulse width. Typically, data
d on the transmit side using pulse-width modulation (PWM) or non-return-to-zero (NRZ).

ost common source for NRZ data is from a UART embedded in a micro-controller. Applicatio
e NRZ data encoding typically involve microcontrollers. The most common source for PWM da
a remote control IC such as the HC-12E from Holtek or ST14 CODEC from Sunro
logies.

sent as a constant rate square-wave. The duty cycle of that square wave will generally be eithe
a zero) or 66% (a one). The data slicer on the STR-433 is optimized for use with PWM encoded
hough it will work with NRZ data if certain encoding rules are followed.

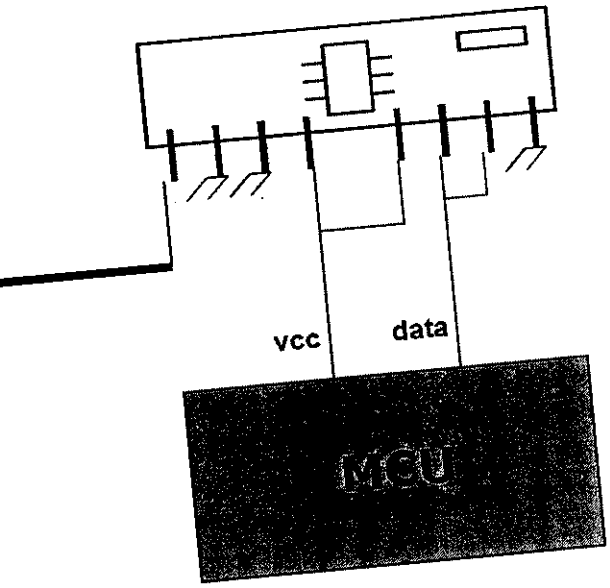
3. *Power Supply*

TR-433 is designed to operate from a 5V power supply. It is crucial that this power supply be
The power supply should be bypassed using a 0.1uF low-ESR ceramic capacitor and a 4.
um capacitor. These capacitors should be placed as close to the power pins as possible. The S
s designed for continuous duty operation. From the time power is applied, it can take u
nSec for the data output to become valid.

.4. *Antenna Input*

support most antenna types, including printed antennas integrated directly onto the PCB and
single core wire of about 17cm. The performance of the different antennas varies. Any time a
of the frequency it is carrying, it should be a 50 ohm micros

cal Application



: Antenna length about: 17cm for 433MHz

Ordering Information

	Description
33	433 MHz RF Receiver

APPENDIX D

HOLTEK

HT12A/HT12E
2^{12} Series of Encoders

Features

- Operating voltage
  - 2.4V~5V for the HT12A
  - 2.4V~12V for the HT12E
- Low power and high noise immunity CMOS technology
- Low standby current: 0.1μA (typ.) at V_{DD}=5V
- HT12A with a 38kHz carrier for infrared transmission medium
- Minimum transmission word
  - Four words for the HT12E
  - One word for the HT12A
- Built-in oscillator needs only 5% resistor
- Data code has positive polarity
- Minimal external components
- HT12A/E: 18-pin DIP/20-pin SOP package

Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

General Description

The 2^{12} encoders are a series of CMOS LSIs for remote control system applications. They are capable of encoding information which consists of N address bits and 12–N data bits. Each address/data input can be set to one of the two logic states. The programmed addresses/data are transmitted together with the header bits via an RF or an infrared transmission medium upon receipt of a trigger signal. The capability to select a $\overline{TE}$ trigger on the HT12E or a DATA trigger on the HT12A further enhances the application flexibility of the 2^{12} series of encoders. The HT12A additionally provides a 38kHz carrier for infrared systems.

Selection Table

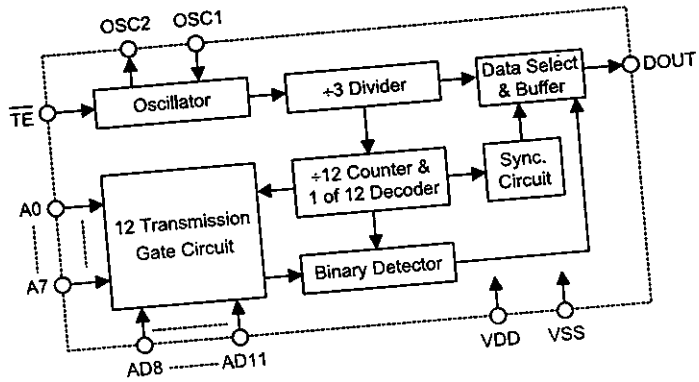
Function / Part No.	Address No.	Address/ Data No.	Data No.	Oscillator	Trigger	Package	Carrier Output	Negative Polarity
HT12A	8	0	4	455kHz resonator	D8~D11	18 DIP 20 SOP	38kHz	No
HT12E	8	4	0	RC oscillator	$\overline{TE}$	18 DIP 20 SOP	No	No

Note: Address/Data represents pins that can be address or data according to the decoder requirement.

Block Diagram

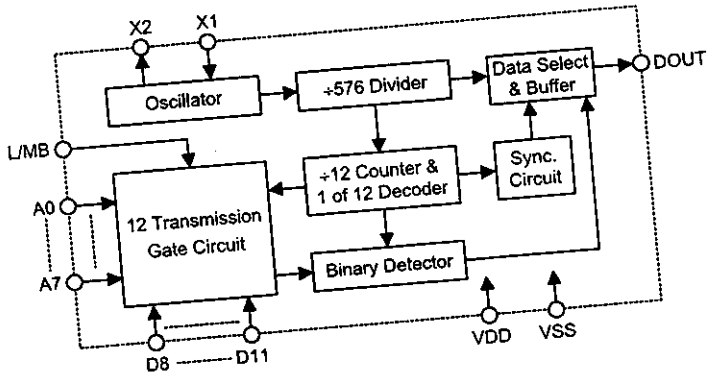
$\overline{TE}$ trigger

HT12E



DATA trigger

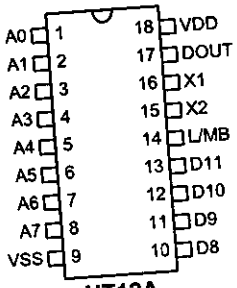
HT12A



Note: The address data pins are available in various combinations (refer to the address/data table).

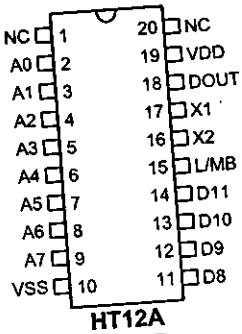
Pin Assignment

8-Address 4-Data



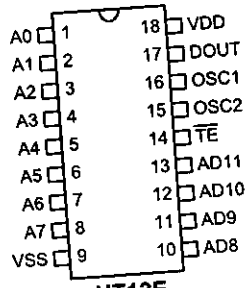
HT12A
–18 DIP

8-Address 4-Data



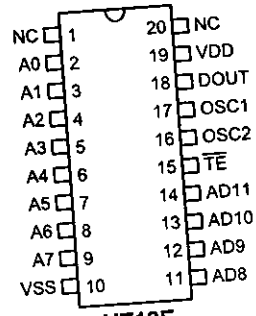
HT12A
– 20 SOP

8-Address 4-Address/Data



HT12E
–18 DIP

8-Address 4-Address/Data



HT12E
–20 SOP

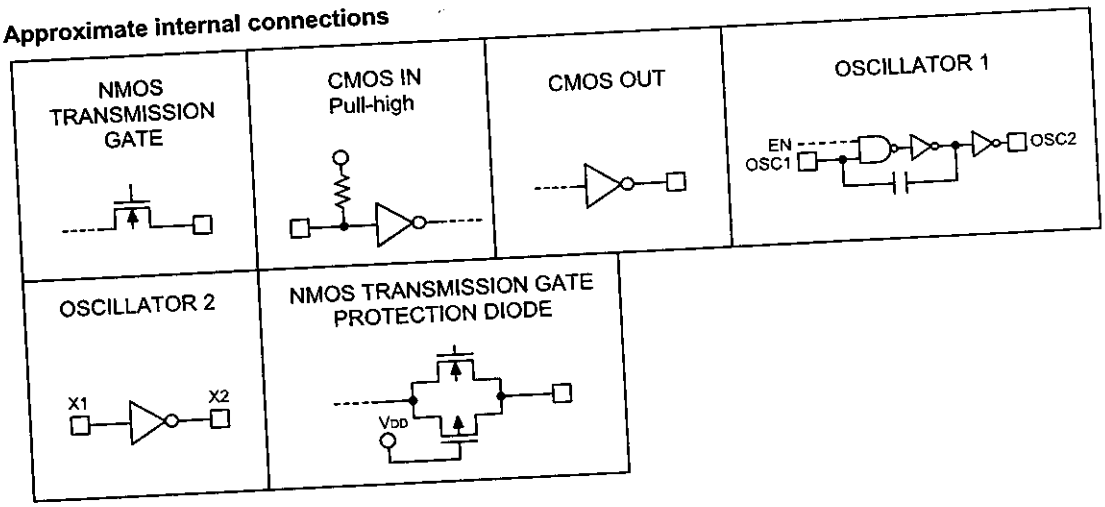
Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A7	I	CMOS IN Pull-high (HT12A) NMOS TRANSMISSION GATE PROTECTION DIODE (HT12E)	Input pins for address A0~A7 setting These pins can be externally set to VSS or left open
AD8~AD11	I	NMOS TRANSMISSION GATE PROTECTION DIODE (HT12E)	Input pins for address/data AD8~AD11 setting These pins can be externally set to VSS or left open
D8~D11	I	CMOS IN Pull-high	Input pins for data D8~D11 setting and transmission enable, active low These pins should be externally set to VSS or left open (see Note)
DOUT	O	CMOS OUT	Encoder data serial transmission output
L/MB	I	CMOS IN Pull-high	Latch/Momentary transmission format selection pin: Latch: Floating or VDD Momentary: VSS

Pin Name	I/O	Internal Connection	Description
$\overline{TE}$	I	CMOS IN Pull-high	Transmission enable, active low (see Note)
OSC1	I	OSCILLATOR 1	Oscillator input pin
OSC2	O	OSCILLATOR 1	Oscillator output pin
X1	I	OSCILLATOR 2	455kHz resonator oscillator input
X2	O	OSCILLATOR 2	455kHz resonator oscillator output
VSS	I	—	Negative power supply, grounds
VDD	I	—	Positive power supply

Note: D8~D11 are all data input and transmission enable pins of the HT12A.
$\overline{TE}$ is a transmission enable pin of the HT12E.

Approximate internal connections



Absolute Maximum Ratings

Supply Voltage (HT12A) .....–0.3V to 5.5V
Input Voltage.....V_{SS}–0.3 to V_{DD}+0.3V
Operating Temperature.....–20°C to 75°C
Supply Voltage (HT12E) .....–0.3V to 13V
Storage Temperature.....–50°C to 125°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Ta=25°C

HT12A

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	3	5	V
I_{STB}	Standby Current	3V	Oscillator stops	—	0.1	1	μA
		5V		—	0.1	1	μA
I_{DD}	Operating Current	3V	No load f_{OSC}=455kHz	—	200	400	μA
		5V		—	400	800	μA
I_{DOUT}	Output Drive Current	5V	V_{OH}=0.9V_{DD} (Source)	−1	−1.6	—	mA
			V_{OL}=0.1V_{DD} (Sink)	2	3.2	—	mA
V_{IH}	"H" Input Voltage	—	—	0.8V_{DD}	—	V_{DD}	V
V_{IL}	"L" Input Voltage	—	—	0	—	0.2V_{DD}	V
R_{DATA}	D8~D11 Pull-high Resistance	5V	V_{DATA}=0V	—	150	300	kΩ

Ta=25°C

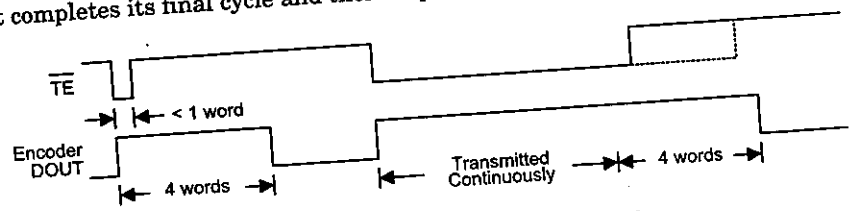
HT12E

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5	12	V
I_{STB}	Standby Current	3V	Oscillator stops	—	0.1	1	μA
		12V		—	2	4	μA
I_{DD}	Operating Current	3V	No load f_{OSC}=3kHz	—	40	80	μA
		12V		—	150	300	μA
I_{DOUT}	Output Drive Current	5V	V_{OH}=0.9V_{DD} (Source)	−1	−1.6	—	mA
			V_{OL}=0.1V_{DD} (Sink)	1	1.6	—	mA
V_{IH}	"H" Input Voltage	—	—	0.8V_{DD}	—	V_{DD}	V
V_{IL}	"L" Input Voltage	—	—	0	—	0.2V_{DD}	V
f_{OSC}	Oscillator Frequency	5V	R_{OSC}=1.1MΩ	—	3	—	kHz
$R_{\overline{TE}}$	$\overline{TE}$ Pull-high Resistance	5V	$V_{\overline{TE}}$=0V	—	1.5	3	MΩ

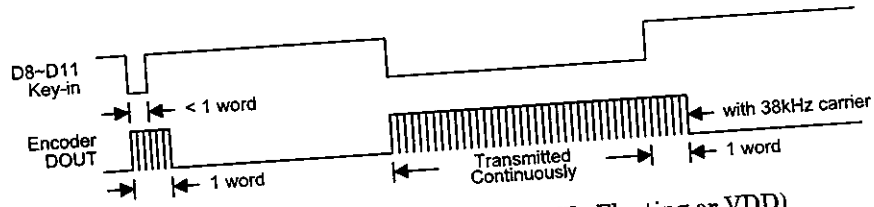
Functional Description

Operation

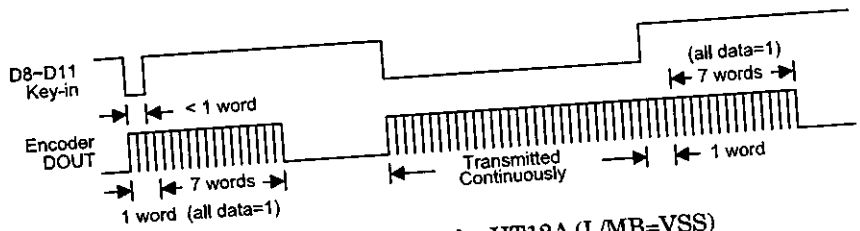
The 2^{12} series of encoders begin a 4-word transmission cycle upon receipt of a transmission enable ($\overline{TE}$ for the HT12E or D8~D11 for the HT12A, active low). This cycle will repeat itself as long as the transmission enable ($\overline{TE}$ or D8~D11) is held low. Once the transmission enable returns high the encoder output completes its final cycle and then stops as shown below.



Transmission timing for the HT12E



Transmission timing for the HT12A (L/MB=Floating or VDD)

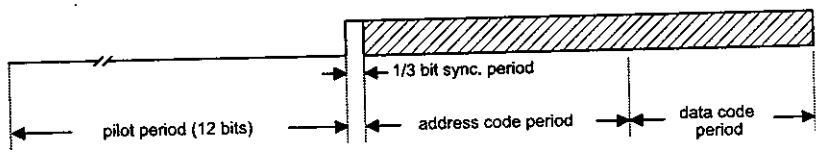


Transmission timing for the HT12A (L/MB=VSS)

Information word

If L/MB=1 the device is in the latch mode (for use with the latch type of data decoders). When the transmission enable is removed during a transmission, the DOUT pin outputs a complete word and then stops. On the other hand, if L/MB=0 the device is in the momentary mode (for use with the momentary type of data decoders). When the transmission enable is removed during a transmission, the DOUT outputs a complete word and then adds 7 words all with the "1" data code.

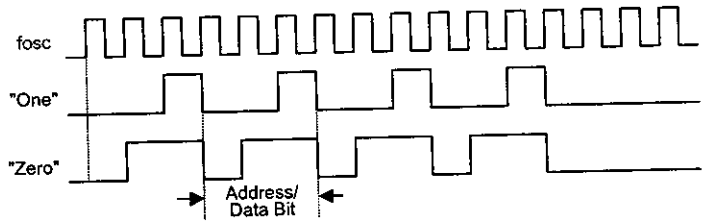
An information word consists of 4 periods as illustrated below.



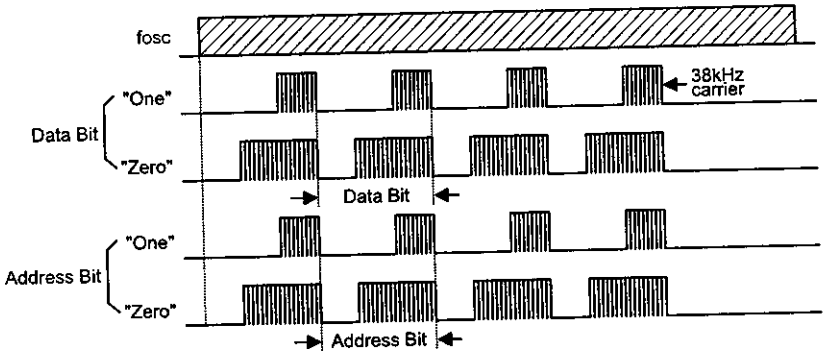
Composition of information

Address/data waveform

Each programmable address/data pin can be externally set to one of the following two logic states as shown below.



Address/Data bit waveform for the HT12E



Address/Data bit waveform for the HT12A

HT12D/HT12F
2^{12} Series of Decoders

Features

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- Low standby current
- Capable of decoding 12 bits of information
- Binary address setting
- Received codes are checked 3 times
- Address/Data number combination
  - HT12D: 8 address bits and 4 data bits
  - HT12F: 12 address bits only
- Built-in oscillator needs only 5% resistor
- Valid transmission indicator
- Easy interface with an RF or an infrared transmission medium
- Minimal external components
- Pair with Holtek's 2^{12} series of encoders
- 18-pin DIP, 20-pin SOP package

Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

General Description

The 2^{12} decoders are a series of CMOS LSIs for remote control system applications. They are paired with Holtek's 2^{12} series of encoders (refer to the encoder/decoder cross reference table). For proper operation, a pair of encoder/decoder with the same number of addresses and data format should be chosen.

The decoders receive serial addresses and data from a programmed 2^{12} series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. They compare the serial input data three times continuously with their local addresses. If no error or unmatched codes are found, the input data codes are decoded and then transferred to the output pins. The VT pin also goes high to indicate a valid transmission.

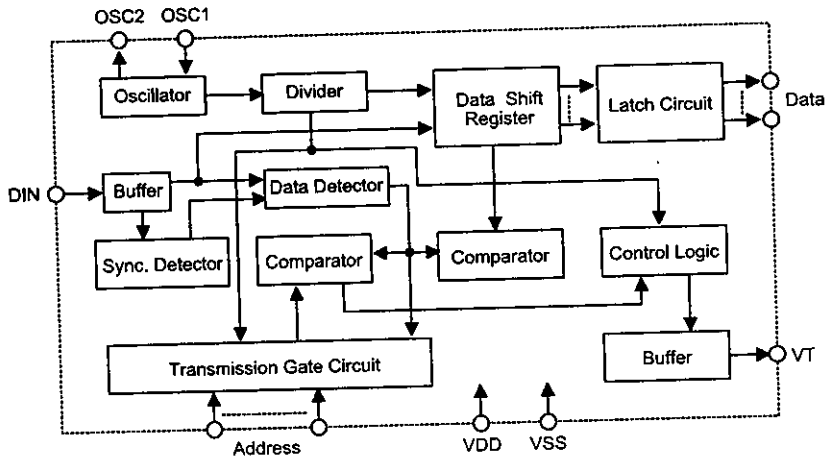
The 2^{12} series of decoders are capable of decoding informations that consist of N bits of address and 12–N bits of data. Of this series, the HT12D is arranged to provide 8 address bits and 4 data bits, and HT12F is used to decode 12 bits of address information.

Selection Table

Function / Part No.	Address No.	Data No.	Data Type	VT	Oscillator	Trigger	Package
HT12D	8	4	L	√	RC oscillator	DIN active "Hi"	18DIP, 20SOP
HT12F	12	0	—	√	RC oscillator	DIN active "Hi"	18DIP, 20SOP

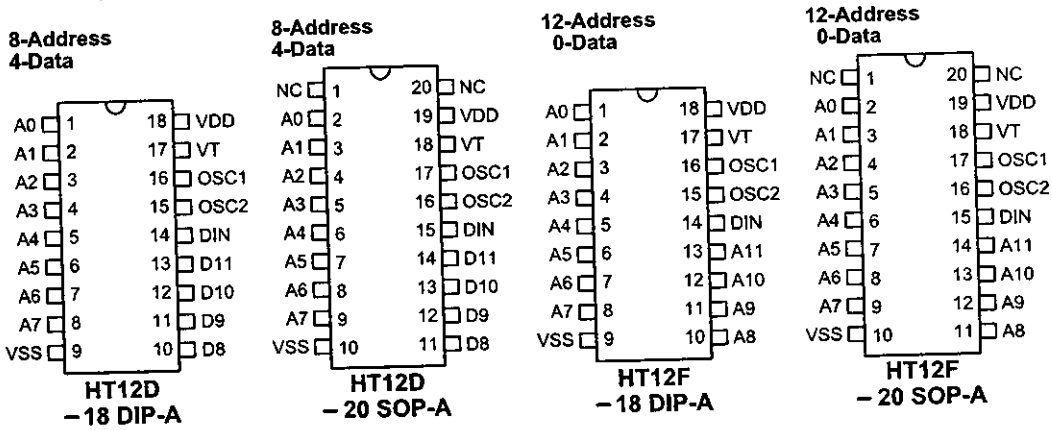
Notes: Data type: L stands for latch type data output.
VT can be used as a momentary data output.

Block Diagram



Note: The address/data pins are available in various combinations (see the address/data table).

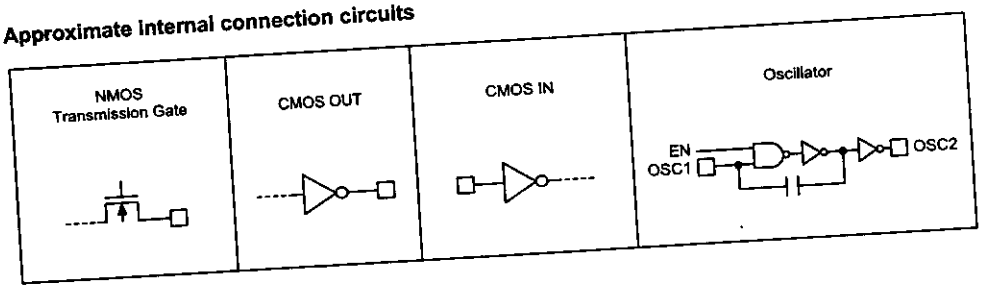
Pin Assignment



Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A11 (HT12F)	I	NMOS Transmission Gate	Input pins for address A0~A11 setting These pins can be externally set to VSS or left open.
A0~A7 (HT12D)			Input pins for address A0~A7 setting These pins can be externally set to VSS or left open.
D8~D11 (HT12D)	O	CMOS OUT	Output data pins, power-on state is low.
DIN	I	CMOS IN	Serial data input pin
VT	O	CMOS OUT	Valid transmission, active high
OSC1	I	Oscillator	Oscillator input pin
OSC2	O	Oscillator	Oscillator output pin
VSS	—	—	Negative power supply, ground
VDD	—	—	Positive power supply

Approximate internal connection circuits



Absolute Maximum Ratings

Supply Voltage ..... −0.3V to 13V

Input Voltage ..... V_{SS}−0.3 to V_{DD}+0.3V

Storage Temperature ..... −50°C to 125°C

Operating Temperature ..... −20°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Ta=25°C

Electrical Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5	12	V
I_{STB}	Standby Current	5V	Oscillator stops	—	0.1	1	μA
		12V		—	2	4	μA
I_{DD}	Operating Current	5V	No load, f_{OSC}=150kHz	—	200	400	μA
I_O	Data Output Source Current (D8~D11)	5V	V_{OH}=4.5V	−1	−1.6	—	mA
	Data Output Sink Current (D8~D11)	5V	V_{OL}=0.5V	1	1.6	—	mA
I_{VT}	VT Output Source Current	5V	V_{OH}=4.5V	−1	−1.6	—	mA
	VT Output Sink Current		V_{OL}=0.5V	1	1.6	—	mA
V_{IH}	"H" Input Voltage	5V	—	3.5	—	5	V
V_{IL}	"L" Input Voltage	5V	—	0	—	1	V
f_{OSC}	Oscillator Frequency	5V	R_{OSC}=51kΩ	—	150	—	kHz

Functional Description

Operation

The 2^{12} series of decoders provides various combinations of addresses and data pins in different packages so as to pair with the 2^{12} series of encoders.

The decoders receive data that are transmitted by an encoder and interpret the first N bits of code period as addresses and the last 12–N bits as data, where N is the address code number. A signal on the DIN pin activates the oscillator which in turn decodes the incoming address and data. The decoders will then check the received address three times continuously. If the received address codes all match the contents of the decoder's local address, the 12–N bits of data are decoded to activate the output pins and the VT pin is set high to indicate a valid transmission. This will last unless the address code is incorrect or no signal is received.

The output of the VT pin is high only when the transmission is valid. Otherwise it is always low.

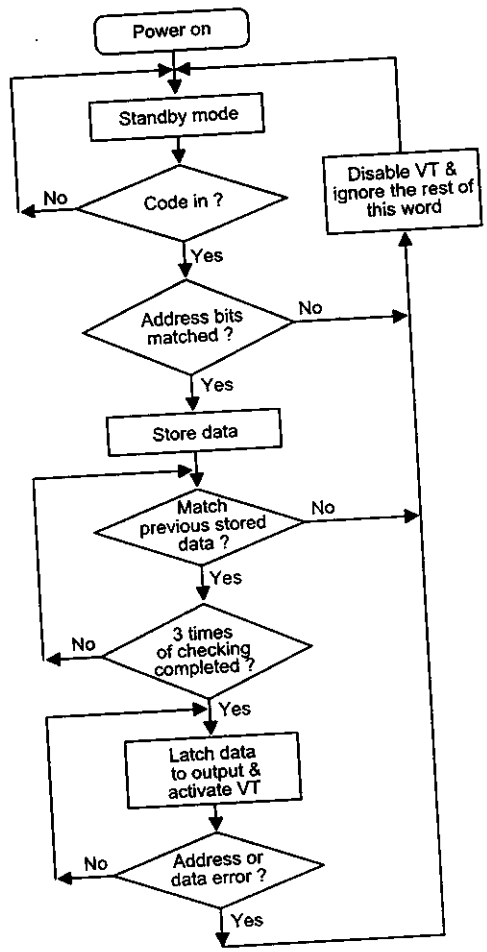
Output type

Of the 2^{12} series of decoders, the HT12F has no data output pin but its VT pin can be used as a momentary data output. The HT12D, on the other hand, provides 4 latch type data pins whose data remain unchanged until new data are received.

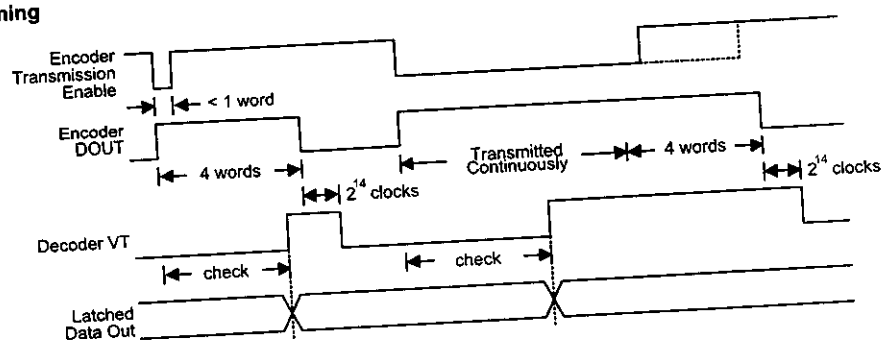
Part No.	Data Pins	Address Pins	Output Type	Operating Voltage
HT12D	4	8	Latch	2.4V~12V
HT12F	0	12	—	2.4V~12V

Flowchart

The oscillator is disabled in the standby state and activated when a logic "high" signal applies to the DIN pin. That is to say, the DIN should be kept low if there is no signal input.



Decoder timing



Encoder/Decoder cross reference table

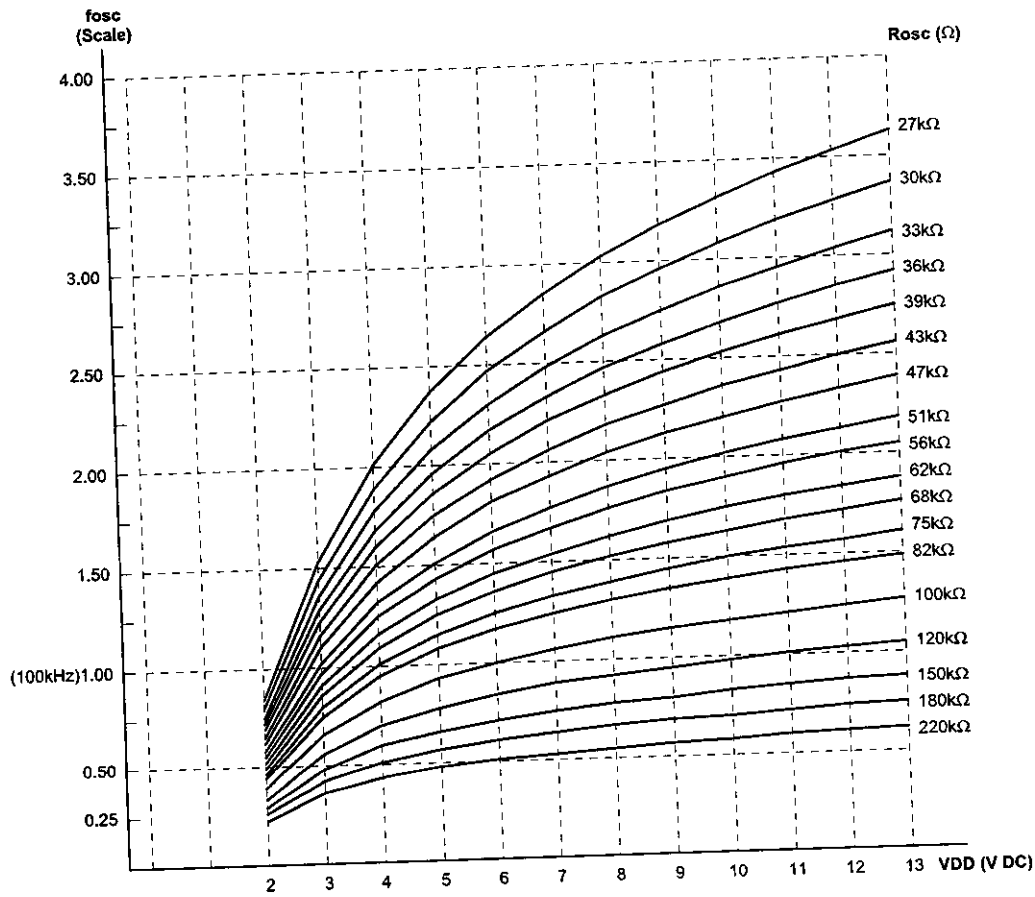
Decoders Part No.	Data Pins	Address Pins	VT	Pair Encoder	Package			
					Encoder		Decoder	
					DIP	SOP	DIP	SOP
HT12D	4	8	√	HT12A HT12E	18	20	18	20
HT12F	0	12	√	HT12A HT12E	18	20	18	20

Address/Data sequence

The following table provides address/data sequence for various models of the 2^{12} series of decoders.

Part No.	Address/Data Bits											
	0	1	2	3	4	5	6	7	8	9	10	11
HT12D	A0	A1	A2	A3	A4	A5	A6	A7	D8	D9	D10	D11
HT12F	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

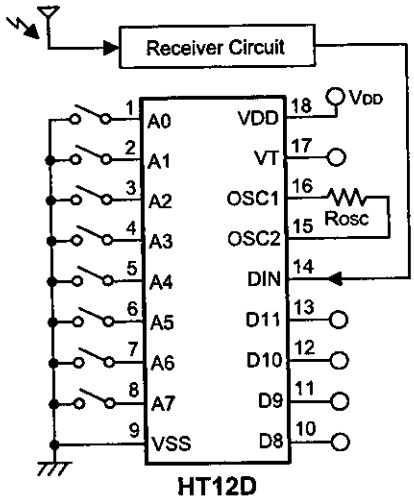
Oscillator frequency vs supply voltage



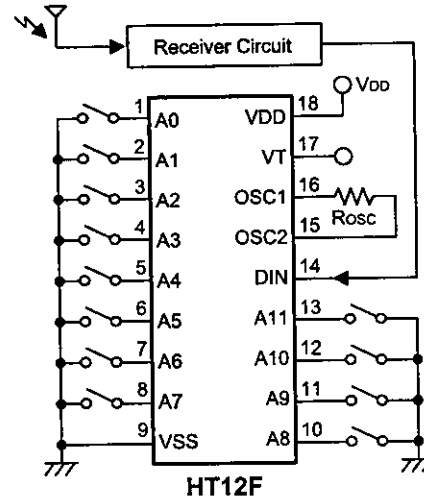
Note: The recommended oscillator frequency is f_{OSCD} (decoder) $\cong 50\ f_{OSCE}$ (HT12E encoder)

$\cong \frac{1}{3} f_{OSCE}$ (HT12A encoder).

Application Circuits



HT12D



HT12F

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