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IMPLEMENTATION OF THREE PHASE CASCADED MULTILEVEL INVERTER

A PROJECT REPORT

Submitted by

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ABSTRACT

One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices, etc. Load harmonics cause the overheating of the magnetic cores of transformer and motors. Source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives.

In order to overcome these harmonic problems, the multilevel inverter designed to produce stepped output with very low values of the low order Harmonics. The three phase cascaded multilevel inverter system synthesizes a desired AC output voltage waveform with lower THD, whereas the traditional inverter generates square wave output, it leads harmonic problems.

Total harmonic distortion is obtained using MATLAB for both normal and optimized angles and is compared for better harmonic minimisation. Various PWM techniques applied to cascaded H-Bridge MLI and outputs are simulated.

PIC microcontroller has been programmed to vary the duty cycle of the inverter.The PWM pulses are generated by the controller(IC 16F877). The hardware output voltage is maintaining constant 24V AC but the input voltage is a DC voltage (12V) with separate DC sources.

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The completion of our project can be attributed to the combined efforts made by us and the contribution made in one form or the other by the individuals we hereby acknowledge.

We express our heart-felt gratitude and thanks to the Dean / HoD of Electrical and Electronics Engineering, **Dr. Rani Thottungal** for encouraging us and for being with us right from beginning of the project and fine tuning us at every step.

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LIST OF SYMBOLS AND ABBREVIATIONS

S NO.	SYMBOLS	ABBREVIATIONS
01	AC	ALTERNATING CURRENT
02	DC	DIRECT CURRENT
03	PIC	PROGRAMMABLE INTERFACE CONTROL
04	MOSFET	METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
05	MC	MICRO CONTROLLER
06	IC	INTEGRATED CIRCUIT
07	CMOS	COMPLEMENTARY METAL OXIDE SEMICONDUCTOR

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CHAPTER 1

INTRODUCTION

1.1 OBJECTIVE

The traditional inverter generates square wave output, it leads harmonic problems. The proposed 3phase multilevel inverter gives stepped output instead of square wave o/p with minimised harmonics. Analysis of total harmonic distortion and various PWM techniques applied to cascaded H-Bridge MLI.

1.2 NEED FOR THE PROJECT

Harmonic minimisation can be obtained by using multilevel cascade H-bridge inverters and also by PWM techniques. In multilevel H-bridge inverters where N devices (each capable of operating at voltage Vdc) per-phase are used in the circuit to produce an output varying between ±(N/2)*(Vdc/2).

1.3 ADVANTAGES OVER THE EXISTING SYSTEM

Stepped output waveform with lesser harmonic distortion is obtained.Device voltage sharing is automatic because of the independent DC supplies. There is no restriction on switching pattern. By using a lot of H-bridges, very high voltage converters can be made this way. The circuit is modular –this is an advantage for manufacture and maintenance.

1.4 EXPECTED OUTPUT

The output for Three phase cascaded multilevel inverter is the five level stepped phase voltage output with reduced harmonic problem i.e. low total harmonic distortion.

1.5 METHODOLOGY

- Implementation of three phase two stage cascaded inverters.
- The simulation is carried out using MATLAB software.
- The Implementation is carried out using 8 bit micro controller.
- The total hardware consists of H-Bridge cells, Buffer, optoisolator and embedded controller.

CHAPTER 2

INVERTERS - AN OVERVIEW

2.1 INVERTER BASICS

A device that converts DC power into AC power at desired output voltage and frequency is called an Inverter. Phase controlled converters when operated in the inverter mode are called line commutated inverters. But line commutated inverters require at the output terminals an existing AC supply which is used for their commutation. This means that line commutated inverters can't function as isolated AC voltage sources or as variable frequency generators with DC power at the input. Therefore, voltage level, frequency and waveform on the AC side of the line commutated inverters can't be changed. On the other hand, force commutated inverters provide an independent AC output voltage of adjustable voltage and adjustable frequency and have therefore much wider application.

Inverters can be broadly classified into two types based on their operation:

- Voltage Source Inverters(VSI)
- Current Source Inverters(CSI)

Voltage Source Inverters is one in which the DC source has small or negligible impedance. In other words VSI has stiff DC voltage source at its input terminals. A current source inverter is fed with adjustable current from a DC source of high impedance, i.e; from a stiff DC current source. In a CSI fed with stiff current source, output current waves are not affected by the load.

From view point of connections of semiconductor devices, inverters are classified as under

- Bridge Inverters
- Series Inverters
- Parallel Inverters

2.1.1 CONVENTIONAL VOLTAGE SOURCE INVERTER:

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three phase ac systems. A half-bridge is the simplest topology, which is used to produce a two level square-wave output waveform. A centre-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the centre tap. The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig. 2.1 and 2.2, respectively. In a single-phase half-bridge inverter, only two switches are needed. To avoid shoot-through fault, both switches are never turned on at the same time. S1 is turned on and S2 is turned off to give a load voltage, V AO in Fig. 2.1, of V s/ 2. To complete one cycle, S1 is turned off and S2 is turned on to give a load voltage, V AO, of V s / 2. In full bridge configuration, turning on S1 and S4 and turning off S2 and S3 give a voltage of *VS* between point A and B (V AB) in Fig. 2.2, while turning off S1 and S4 and turning on S2 and S3 give a voltage of Vs.

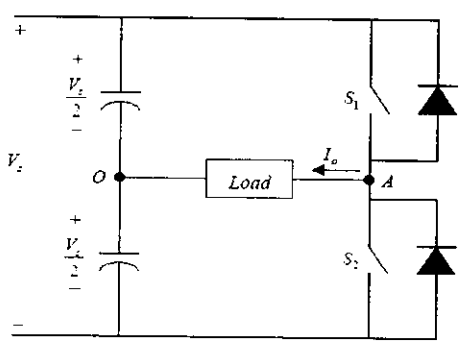


Figure 2.1 Half-bridge configuration

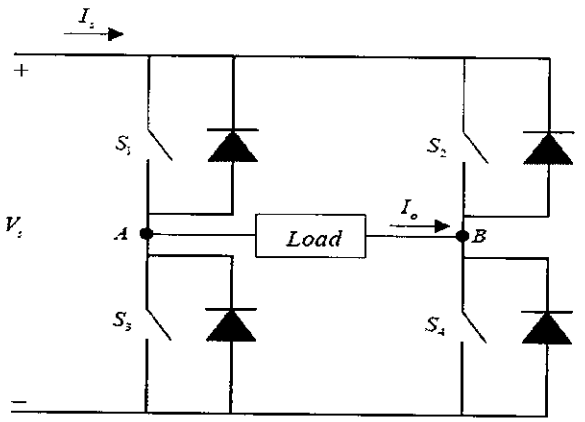


Figure 2.2 Full-bridge configuration

To generate zero level in a full-bridge inverter, the combination can be S1 and S2 on while S3 and S4 off or vice versa. The three possible levels referring to above discussion are shown in Table 2.1.

Table 2.1 Load voltage with corresponding conducting switches.

Conducting Switches	Load Voltage V_{AB}
S_1, S_4	$+V_s$
S_2, S_3	$-V_s$
S_1, S_2 or S_3, S_4	0

Note that S1 and S3 should not be closed at the same time, nor should S2 and S4. Otherwise, a short circuit would exist across the dc source. The output waveform of half bridge and full-bridge of single-phase voltage source inverter are shown in Fig. 2.3 and 2.4, respectively.

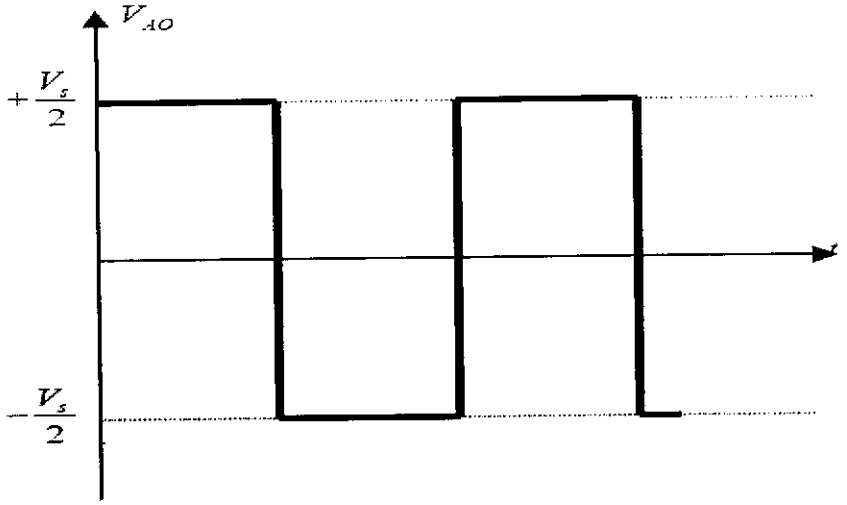


Figure 2.3 Output waveform of half-bridge configuration

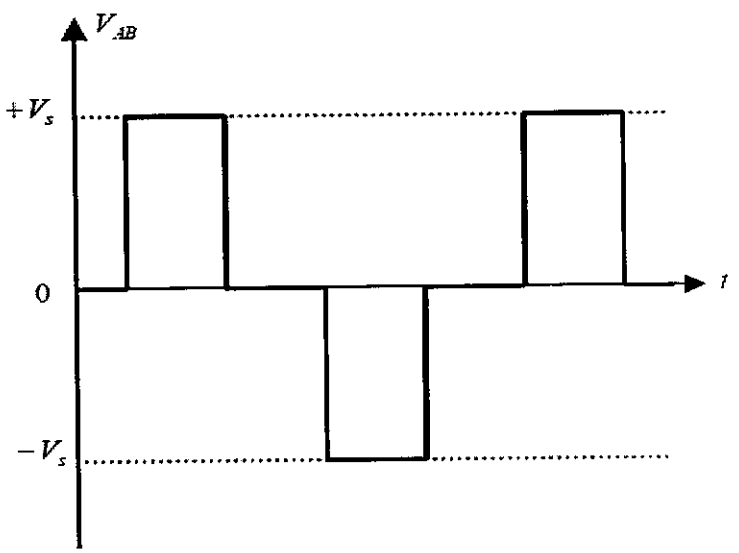


Figure 2.4 Output waveform of full-bridge configuration

2.2 FULL-BRIDGE OR "H-BRIDGE" VOLTAGE SOURCE INVERTER

The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Fig. 2.5. The inverter circuit consists of four main switches and four freewheeling diodes.

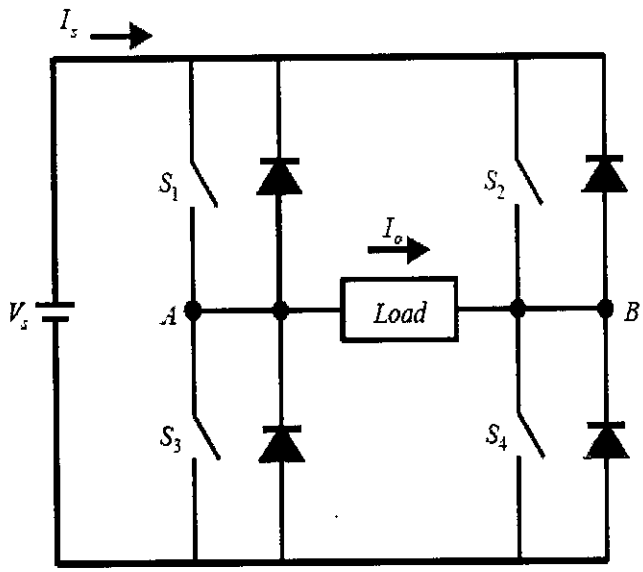


Figure 2.5 An H-bridge cell

2.2.1 GATE SIGNAL AND INVERTER OPERATION:

According to four-switch combination, three output voltage levels, +V, -V, and 0, can be synthesized for the voltage across A and B. During inverter operation shown in Fig. 2.5, switch of S1 and S4 are closed at the same time to provide VAB a positive value and a current path for Io. Switch S2 and S4 are turned on to provide VAB a negative value with a path for Io. Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes. In case of zero level, there are two possible switching patterns to synthesize zero level, for example, 1) S1 and S2 on, S3 and S4 off, and 2) S1 and S2 off and S3 and S4 on. A simple gate signal, repeated zero-level patterns, is shown in Fig. 2.6. All zero levels are generated by turning on S1 and S2.

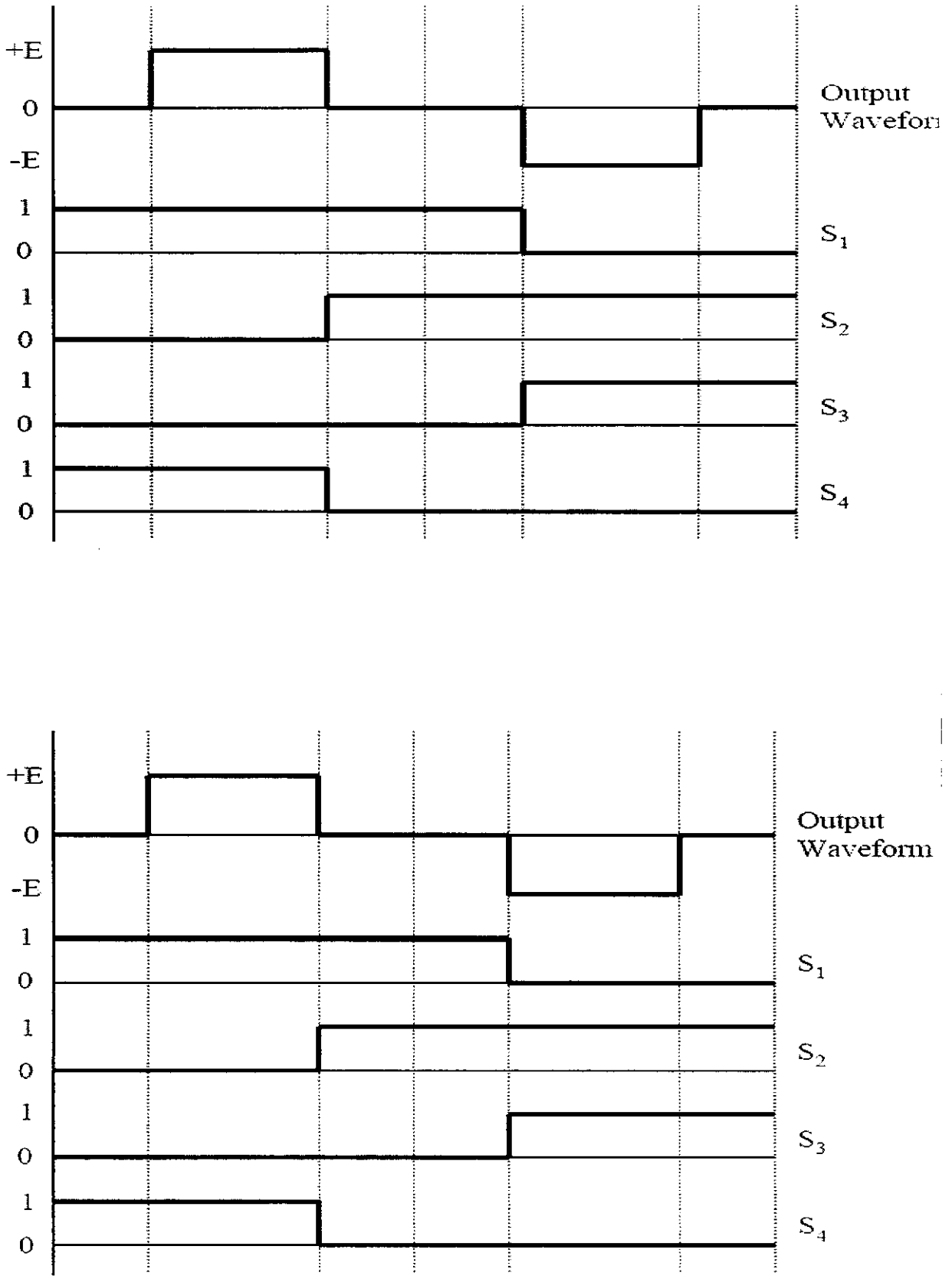


Figure 2.6 Repeated zero-level switching pattern

Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Fig. 2.5, S1 and S2 are turned on longer than S3 and S4 do in each cycle because the same zero level switching pattern is used. As a result, S1 and S2 are consuming more power and getting higher temperature than the other two switches. To avoid such a problem, a different switching pattern for zero level is applied. In the first zero stage, S1 and S2 are turned on; then, in the second zero stage, S3 and S4 are turned on in stead of S1 and S2. By applying this method, turn-on time for each switch turns out to be equal, a shown in Fig. 2.7.

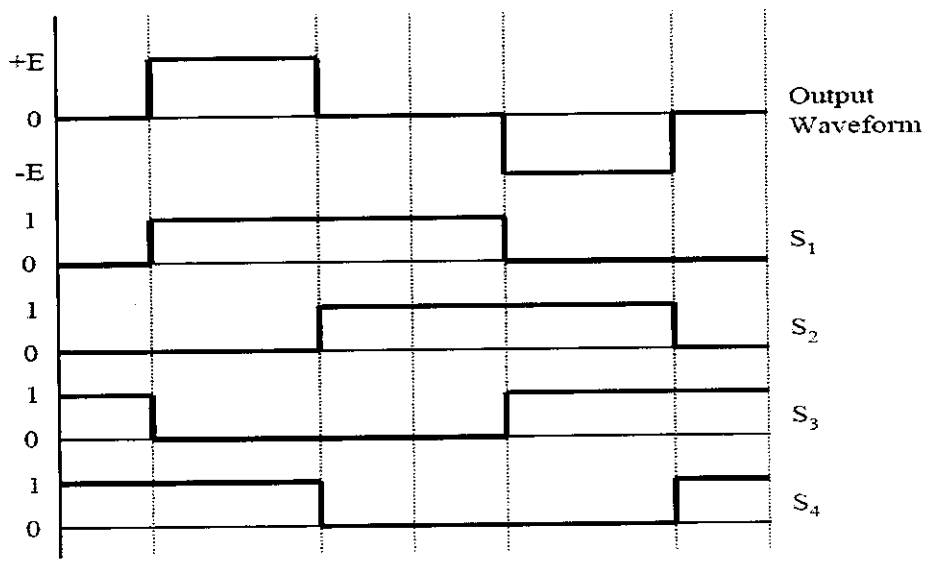


Figure 2.7 Swapped zero-level switching pattern

2.2.2 BLANKING TIME:

Another issue that has to be concerned is providing blanking time for gate signal. In 2.1.2, the switches were assumed to be ideal, which allowed the state of the two switches in an inverter leg to change simultaneously from on to off and vice versa. In practice, switching devices are not ideal. To completely turn-off the devices, a short period, which depends on the type of the device, is needed. Usually, because of the finite turn-off and turn-on times associated with any types of switch, a switch is turned off at the switching time instant. However, the turn-on of the other switching in that inverter leg is delayed by a blanking time, t, which is conservatively chosen to avoid cross conduction current through the leg. A blanking time concept is illustrated in Fig 2.8. The leg of S1 and S3 are used as an example.

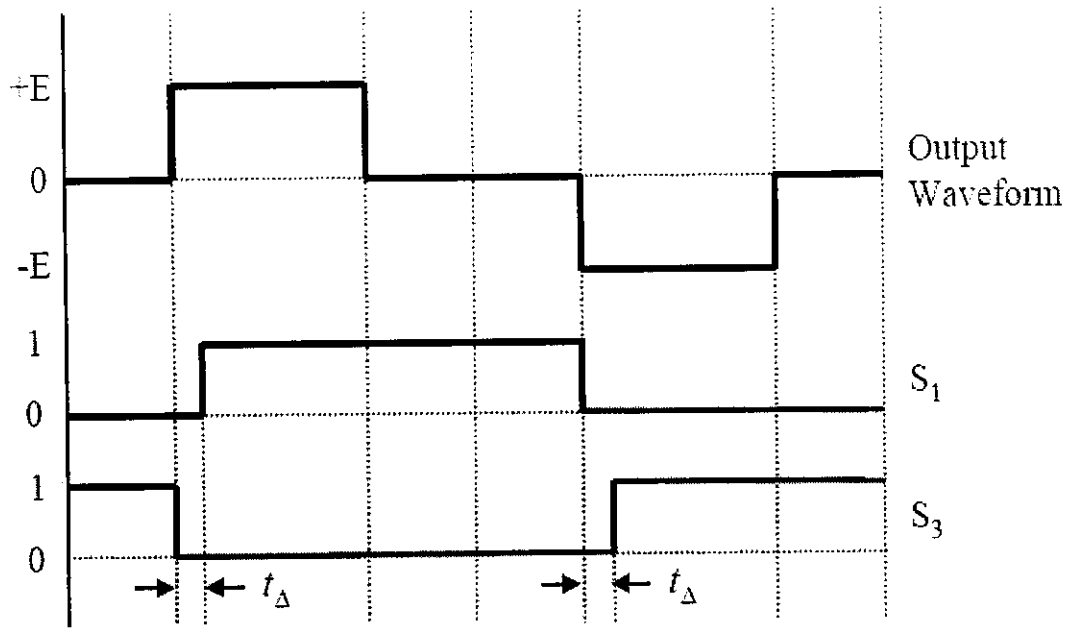


Figure 2.8 Apply blanking time to the gate signal

2.3 STRUCTURE OF H- BRIDGE MODULE AND OPERATION:

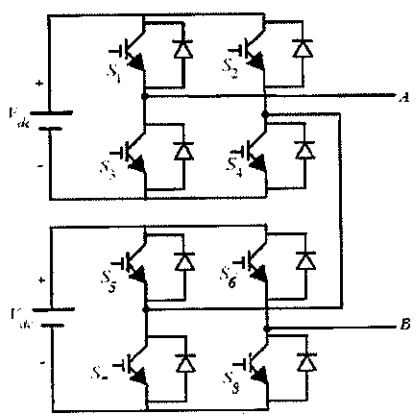


Figure 2.9 Cascaded H- bridge five level inverter

The structure of the single phase Cascaded H-bridge five level inverter is as shown in Figure 2.9, which consists of separate dc source (SDCS), eight semiconductor switching devices. The switching devices used are typically MOSFETs or IGBTs.MOSFETs are chosen for this project due to high forward conduction current density, low on-state voltage drop, low driving power and fast switching response.

Switches S1, S2, S3, S4, S5, S6, S7, and S8 are switched in different sequences to generate output voltages across AB of the H-bridge module. The switching pattern of the MOSFET's are

Mode 1 (Figure 2.10)

- MOSFETs S1, S6, S5 and S4 are turned on.
- Resultant voltage across AB is +Vdc

Mode 2 (Figure 2.11)

- MOSFETs S3, S2, S7 and S8 are turned on.
- Resultant voltage across AB is –Vdc

Mode 3 (Figure 2.12)

- MOSFETs S1, S4, S5 and S8 are turned on
- Resultant voltage across AB is +2Vdc

Mode 4 (Figure 2.13)

- MOSFETs S2, S3, S6 and S7 are turned on
- Resultant voltage across AB is -2Vdc

Mode 5

- None of the MOSFETs are turned on
- Resultant voltage across AB is Zero

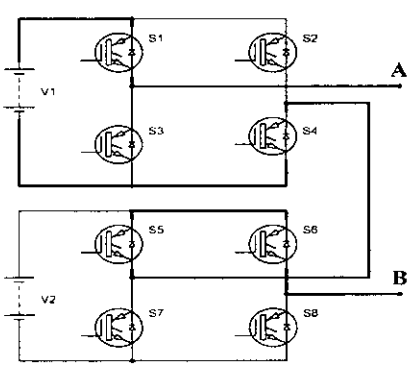


Figure 2.10 Mode 1

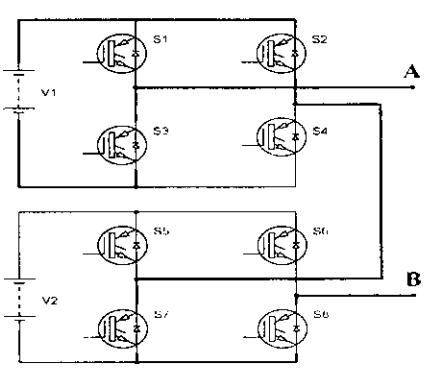


Figure 2.11 Mode 2

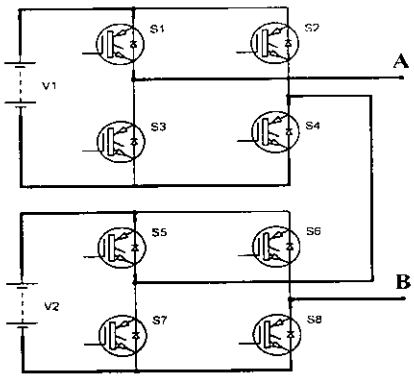


Figure 2.12 Mode 3

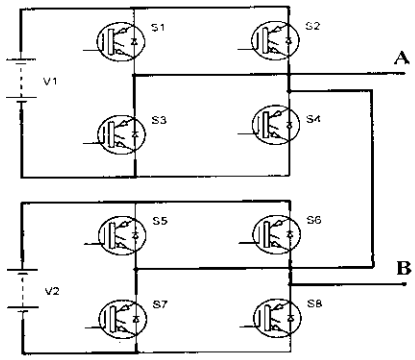


Figure2.13 Mode 4

Figure 2.10 Switching pattern of MOSFET

The output waveform produced by summing up the inverter outputs. The output voltage waveform consists of five voltage levels, which are +Vdc,-Vdc, +2Vdc, -2Vdc and zero In general, the Van output voltage is produced by summing up the output voltage of each module with different duty cycle. The output voltage is almost sinusoidal. The greater the number of H-bridge modules in a single-phase structure, the output voltage will contain more steps, be, therefore producing an ac waveform closer to a sinusoidal waveform. The phase voltage is Van = Va1+Va2.

2.4 APPLICATIONS OF MULTILEVEL INVERTER

Many multilevel converters find applications on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems. The multilevel voltage source inverters are recently applied in many industrial applications such as ac power supplies static VAR compensators, drive systems, and distributed energy resources area (DER). Especially in DER area, because several batteries, fuel cells, solar cells, or rectified wind turbines or micro turbine can be connected through a multilevel inverter to feed a load or interconnect to the ac grid without voltage balancing problem.

2.5 MULTILEVEL VOLTAGE SOURCE INVERTER

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc.

One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. There are three capacitor voltage synthesis-based multilevel inverters they are:

- Diode-Clamped Multilevel Inverter.
- Flying-Capacitor Multilevel Inverter.
- Cascaded-Inverters with Separated DC Sources.

2.5.1 Diode-Clamped Multilevel Inverter (DCMI):

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an mlevel diode-clamp inverter needs m-1 capacitors on the dc bus. The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level inverter there are five switch combinations to generate five level voltages across A and O.

2.5.2 Flying-capacitor Multilevel Inverter (FCMI):

A FCMI uses a ladder structure of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate m-level staircase output voltage, m-1 capacitors in the dc bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

It is obvious that three inner-loop balancing capacitors for phase leg A, Ca1, Ca2, and Ca3 are independent from those for phase leg B. All phase legs share the same dc link capacitors, C1-C4. In fact, there is more than one combination to produce output voltages V2, V3, andV4. That makes the FCMI more flexibility than DCMI.

2.5.3 MULTILEVEL INVERTER WITH SEPARATED DC SOURCES:

The last structure introduced in this thesis is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is the same as that of the other two previous inverters. The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors.

A single-phase m-level configuration of such an inverter is shown in Fig 2.16 Each SDCS is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S1-S4, each inverter level can generate three different voltage outputs, +Vdc, -Vdc, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by m = 2s+1, where s is the number of dc sources.

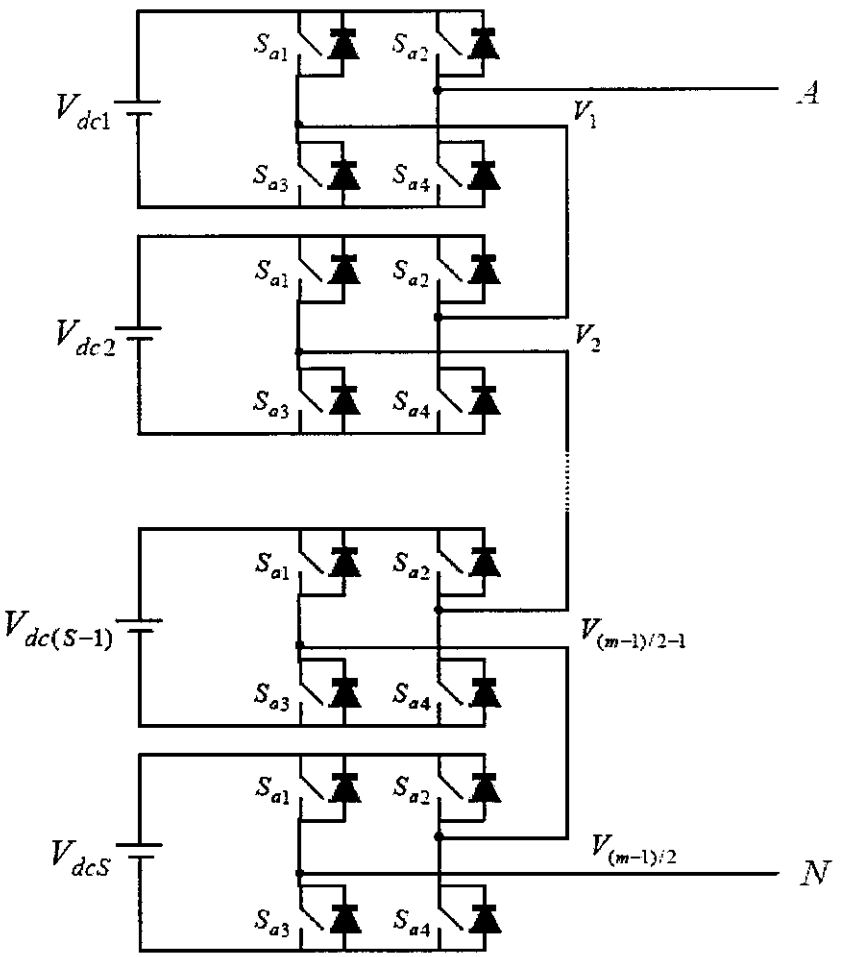


Figure 2.14 Single-phase structure of a multilevel cascaded inverter

A 7-level cascaded-inverters based inverter, for example, will have three SDCSs and three full-bridge cells. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter level. For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configuration.

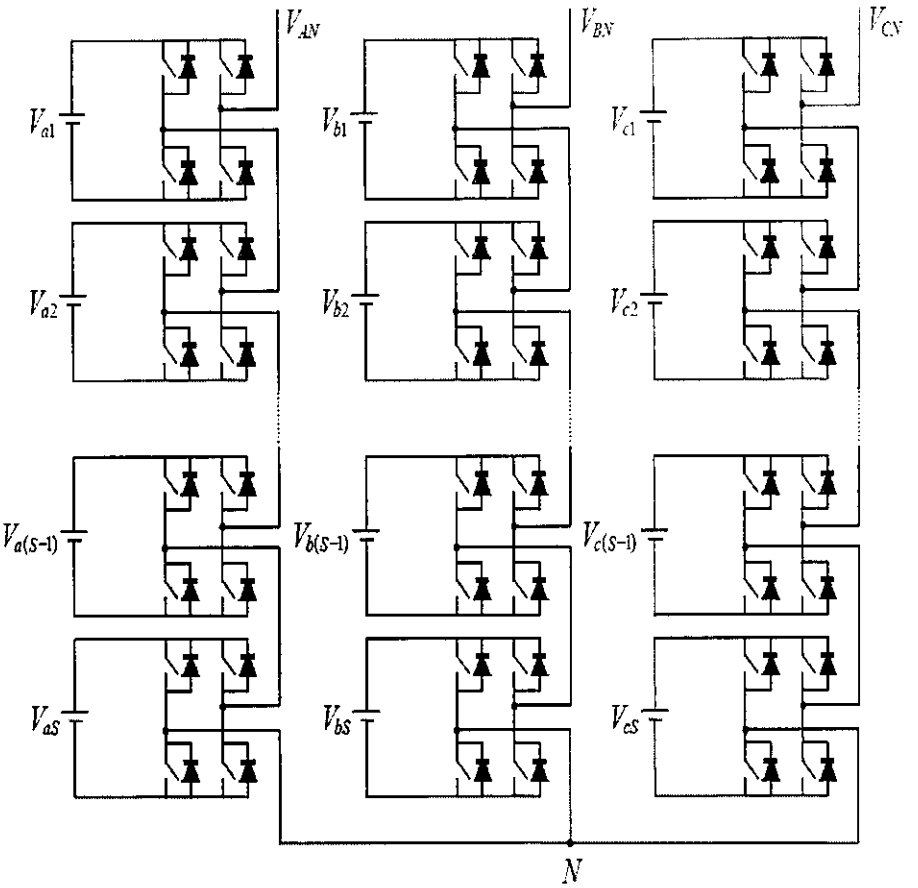


Figure 2.15 A general three-phase Wye-configuration cascaded-inverters based inverter

Another advantage of cascaded-inverter is circuit layout flexibility. Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitor. The number of output voltage levels can be easily adjusted by adding or removing the full-bridge cells.

NEED FOR MULTI-LEVEL INVERTERS-PRESENT PROBLEMS:

- Single devices can't handle the V and I.
- Device voltage rating required 8-10kV -not available.
- Voltage handling capability problem.
- Poor Power quality due to harmonic distortions.
- High Switching losses

2.6 CASCADE INVERTER CONFIGURATION

2.6.1 SINGLE-PHASE STRUCTURE:

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by m =2s+1 Where *s* is the number of dc sources.

For example, a nine-level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells. Fig 2.17 shows a general single-phase m-level cascaded inverter. From Fig. 2.16, the phase voltage is the sum of each H-bridge outputs and is given as

$$V_{AN} = V_{dc1} + V_{dc2} + \ldots + V_{dc(S-1)} + V_{dcS} \tag{2.2}$$

Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes $2s+1$. In this, all dc voltage are assumed to be equal, i.e.,

$$V_{dc1} = V_{dc2} = \ldots = V_{dc(S-1)} = V_{dcS} = V_{dc}$$

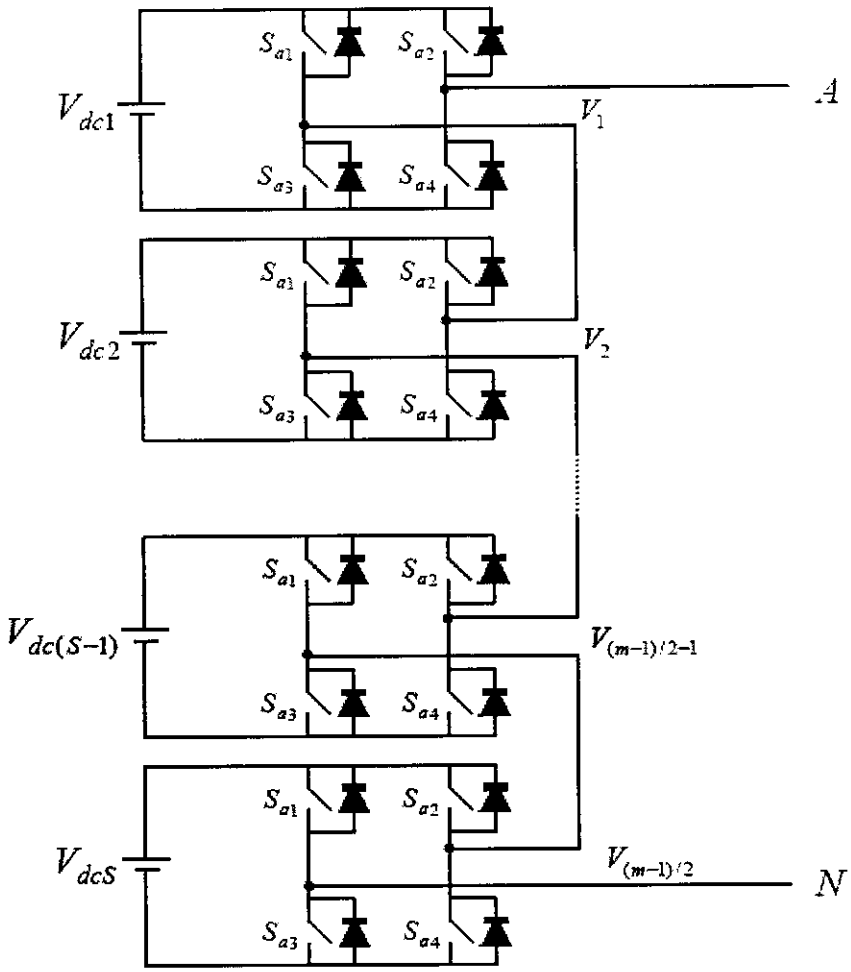


Figure 2.16 Single-phase configuration of an m-level cascaded inverter

2.6.2 THREE-PHASE STRUCTURE:

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. The same three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively. According to three-phase theory, line voltage can be expressed in term of two phase voltages. Where V AB is line voltage V AN is voltage of phase A with respect to point N and V BN is voltage of phase B with respect to point N.

Theoretically, the maximum number of line voltage levels is 2m-1, where m is the number of phase voltage levels. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated.

The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore, only non-triple harmonic components need to be eliminated from phase voltage.

2.6.3 SEPARATED DC SOURCES (SDCSS):

To avoid short circuit of dc sources, the separated dc source configuration is applied to the multilevel inverter using cascaded-inverter. This section will discuss about why cascaded inverter have to employ the separated dc sources (SDCSs). To explain this, two possible dc sources connections are assumed. In the first case, all H-bridge cells in the same leg share the same dc source. Another connection is that the same dc source is shared in the same level of each phase. Fig. 2.17 illustrates the first connection and the second connection of five-level cascaded inverter, respectively.

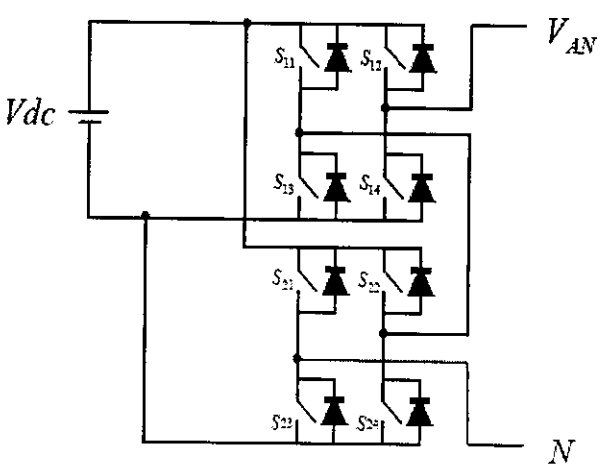


Figure 2.17(a) shows two possible dc source connections

To avoid confusing, both cases will be assumed that no self shoot-through described in 1.2 is possible. However, there are many combinations, which make short circuit happen. Therefore, one possibility of each case will be presented. In the first case, short circuit across the dc source exists when switches S11 and S24 are turned on simultaneously, which is illustrated in Fig. 2.17(a).

Likewise, in the second connection, when switch SA1 and SB3 are on at the same time, which is shown in Fig. 2.17(b), short circuit will be happened.

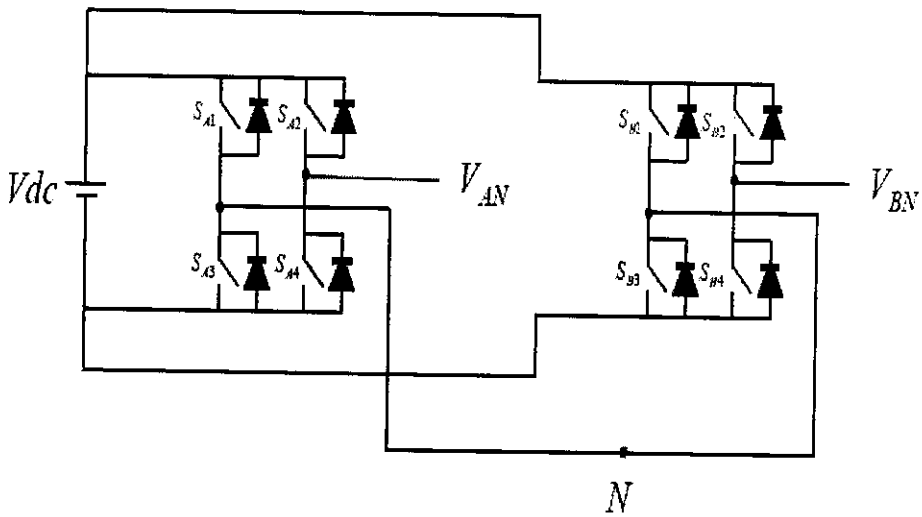


Figure 2.17(b) shows a short circuit possibility of each case

2.7 CONCLUSIONS

A full-bridge inverter or so-called H-bridge cell is introduced. Basically, an H-bridge Cell can generate up to three output voltage levels. The appropriate gate control signal and blinking time are presented. Multilevel inverter using cascaded-inverter with SDCSs is introduced in both single-phase and three-phase structure. The output voltage is the sum of the output voltage of each H-bridge cell. In three-phase system, the voltage THD can be improved in line voltage. Finally, the reason to use SDCSs is explained. In the next chapter, the concept of the optimized harmonic stepped-waveform technique will be presented. Also, the procedure to find the switching angles for such a waveform will be proposed.

CHAPTER 3

HARDWARE DESCRIPTION

3.1 BLOCK DIAGRAM

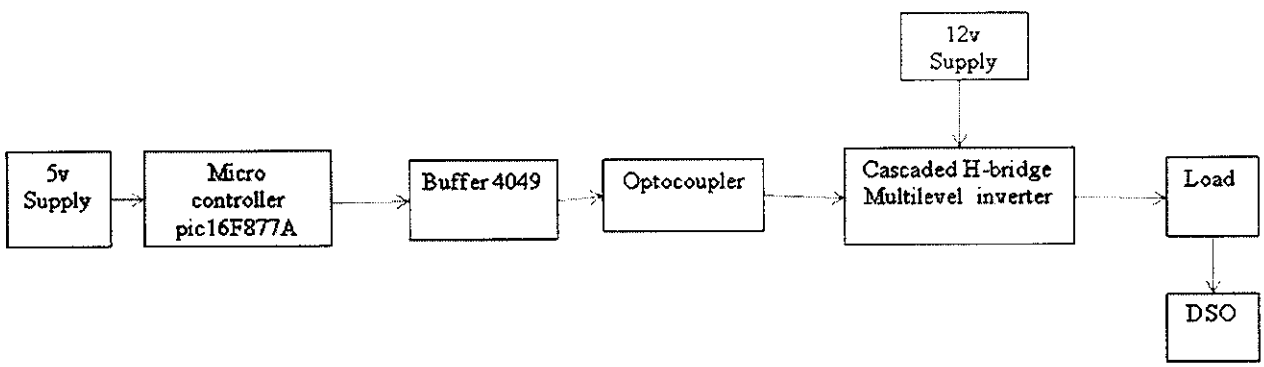


Figure 3.1

3.1.1 DESCRIPTION OF THE BLOCK DIAGRAM:

The block diagram of the Cascaded H-bridge 5 level inverter is shown in Figure 3.1. The 5 level inverter is powered from a 12 V supply. PIC16F877A is used to generate gate pulses to the IGBT. The optimized switching angle for the inverter circuit is found using Newton Raphson Method. A CMOS Hex inverting buffer 4049 is used to drive the optocoupler. Optocoupler uses a short optical transmission path to transfer the gate signal from the buffer circuit to the MOSFET thus it provides electrical isolation between microcontroller and the inverter circuit. The output waveform across the load is viewed with the help of Digital Storage Oscilloscope (DSO).

3.2 HARDWARE CIRCUIT DIAGRAM

3.2.1 POWER CIRCUIT:

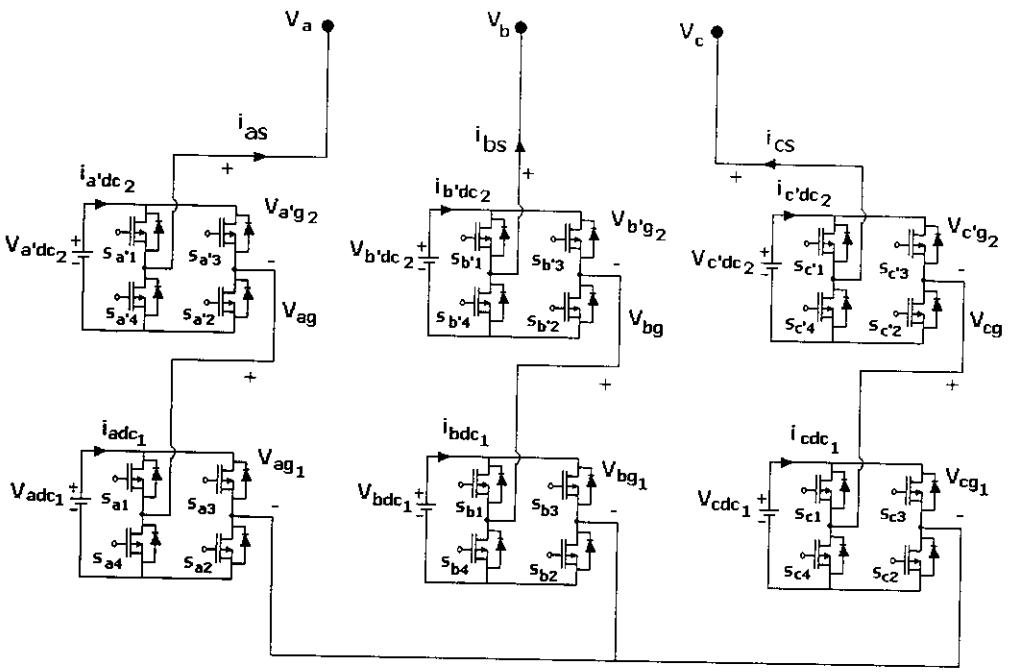


Figure 3.2

The structure of the three phase Cascaded H-bridge five level inverter can be connected in star configuration is shown in Fig 3.2 illustrates the schematic diagram of five-level inverter using two H-bridge cells and two SDCSs, eight MOSFETs per phase .MOSFETs are chosen for this project due to high forward conduction current density, low on-state voltage drop, low driving power and fast switching response.

Switches Sa'1, Sa'2, Sa'3, Sa'4 Sa1, Sa2, Sa3, Sa4 are switched in different sequences to generate output voltages across AN of the H-bridge module. To synthesize five-level phase voltage, three firing angles are required. The switching pattern of the MOSFET's for R phase alone is shown in Figure 2.4.Similarly the other two phases are same as such with 120,240 electrical degree phase shift.

3.2.2 CONTROL CIRCUIT:

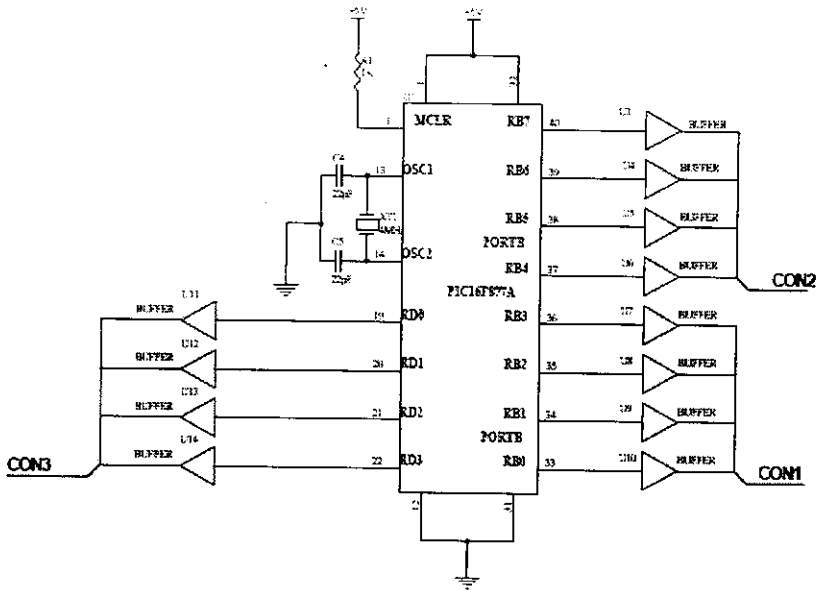
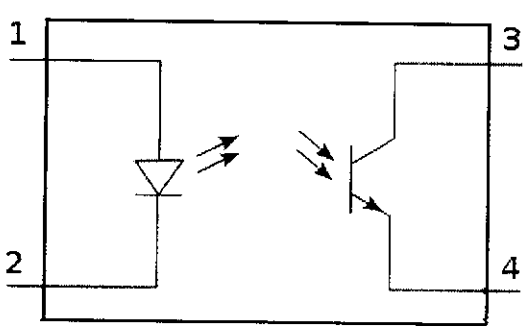


Figure 3.3

3.3 OPTOCOUPLER

Optocoupler is used to provide voltage isolation between the microcontroller and the MOSFET. An optocoupler is a combination of a light source and a photosensitive detector. Normally, a light emitting diode (LED) acts as the light source and a phototransistor acts as the light detector.



1. Anode
2. Cathode
3. Collector
4. Emitter

Figure 3.4 Schematic diagram of the optocoupler

The features of SFH615A-3are,

- Input-to-output isolation voltage.....2,800V_{RMS}.
- Forward DC current I_F =60mA;
- Current transfer ratio (CTR: min 100%).
- Compact dual-in-line package.

When an electrical signal is applied to the input of the optocoupler, its LED lights and illuminates the photo detector, producing a corresponding electrical signal in the output circuit. Unlike a transformer the opto-isolator allows DC coupling and can provide any desired degree of electrical isolation and protection from serious over voltage conditions.

As the output voltage of microcontroller is not sufficient to drive the MOSFET, optocoupler amplifies the output voltage of microcontroller. It is used for voltage amplification

3.4 BUFFER (CD4049UBC)

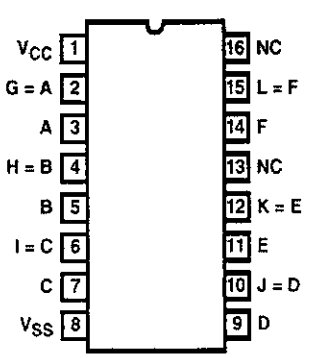


Figure 3.5 Pin diagram of the buffer

The buffer circuit is used to drive the optocoupler and to match the speed of operation of microcontroller and the power electronic devices. The CD4049UBC hex inverting buffer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- channel enhancement mode transistors. This device features, logic level conversion using only one supply voltage (V_{DD}). The maximum value of input signal (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. It is intended for use as hex buffers, CMOS to DTL/ TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

As the output current of microcontroller is not sufficient to drive the MOSFET, Buffer amplifies the output current of microcontroller. It is used for current amplification. The schematic diagram of the buffer circuit is shown in figure 3.3.The features of CD4049 are,

- Supply Voltage (V_{DD}) -0.5V to +18V.
- Input Voltage (V_{IN}) -0.5V to +18V.
- Voltage at Any Output Pin (V_{OUT}) -0.5V to VDD + 0.5V.

3.5 PIC MICROCONTROLLER:

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complimentary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory. The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

3.5.1 PIC (16F877):

Various microcontrollers offer different kinds of memories. EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

3.5.2 SPECIAL FEATURES OF PIC MICROCONTROLLER:

3.5.2.1 Microcontroller core features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed:
    - DC - 20 MHz clock input
    - DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory
- Up to 368 x 8 bytes of Data Memory (RAM)
- Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)

- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:

  < 2mA typical @ 5V, 4 MHz

  < 20mA typical @ 3V, 32 kHz

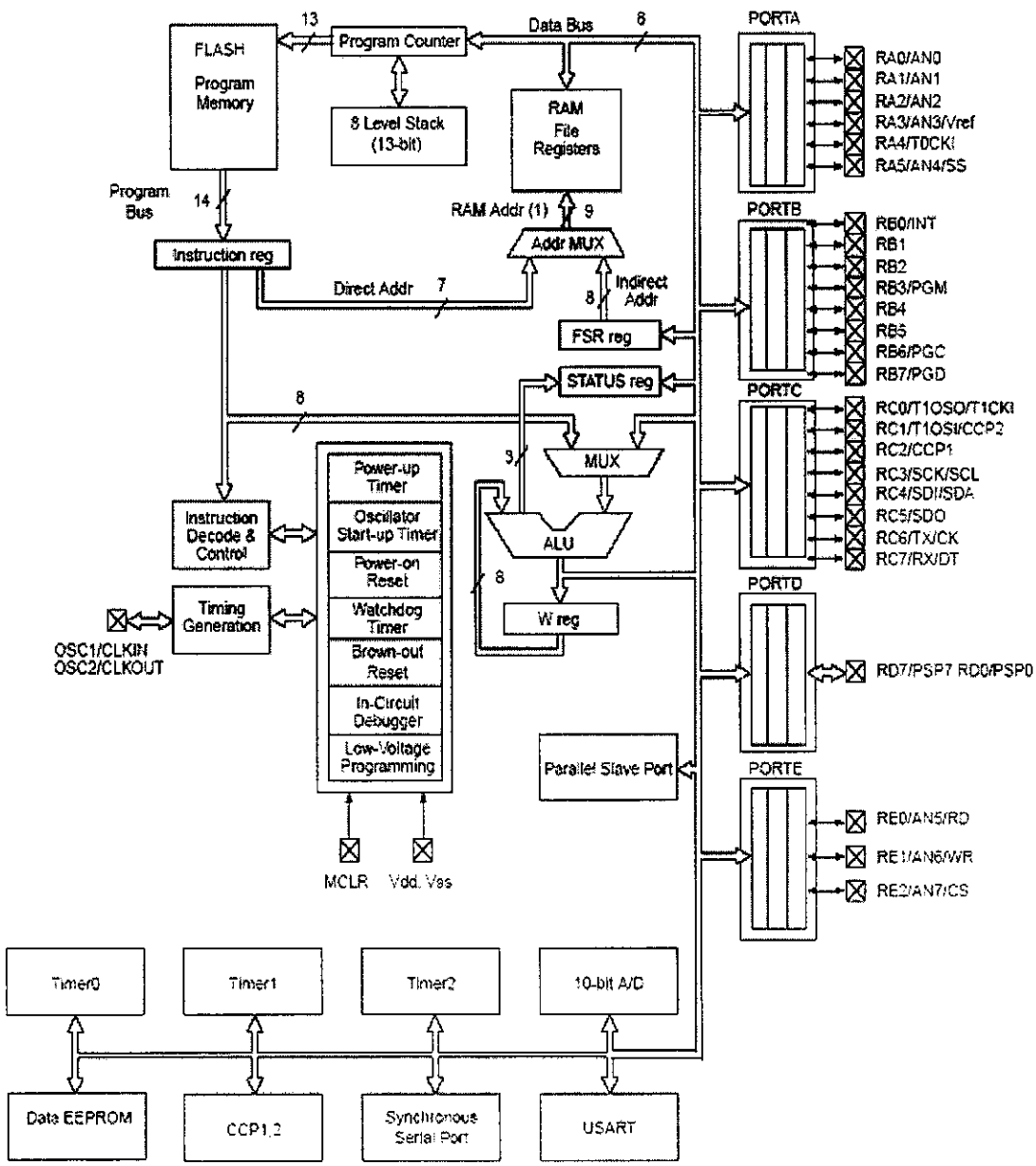
  < 1mA typical standby current

3.5.2.2 PERIPHERAL FEATURES:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
    - Capture is 16-bit, max resolution is 12.5 ns,
    - Compare is 16-bit, max resolution is 200 ns,
    - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with
- 9- bit address detection.
- Brown-out detection circuitry for Brown-out Reset (BOR)

3.5.4 ARCHITECTURE OF PIC 16F877:

The complete architecture of PIC 16F877 and details about the specifications of PIC 16F877 are shown. Fig 3.6 shows the complete pin diagram of the IC PIC 16F877.



Note 1: Higher order bits are from the STATUS register.

Figure 3.6 Architecture of PIC 16f877

Table 3.1 Specifications

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

3.5.5 Pin diagram of PIC 16F877A:

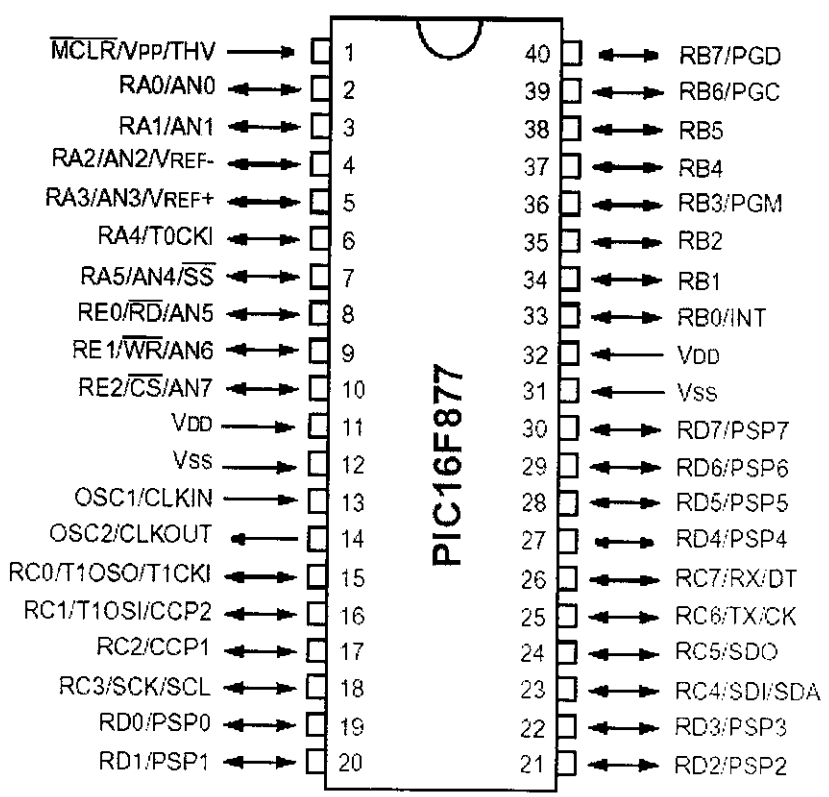


Figure 3.7 Pin Diagram of PIC 16F877

3.5.6 PIN OUT DESCRIPTION:

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP/THV	1	2	18	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/SS/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/ output for both SPI and I^2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
						PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	30	2	I/O	ST/TTL(3)	
RD5/PSP5	28	31	3	I/O	ST/TTL(3)	
RD6/PSP6	29	32	4	I/O	ST/TTL(3)	
RD7/PSP7	30	33	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/RD/AN5	8	9	25	I/O	ST/TTL(3)	RE0 can also be read control for the parallel slave port, or analog input5.
RE1/WR/AN6	9	10	26	I/O	ST/TTL(3)	RE1 can also be write control for the parallel slave port, or analog input6.
RE2/CS/AN7	10	11	27	I/O	ST/TTL(3)	RE2 can also be select control for the parallel slave port, or analog input7.
Vss	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input

O = output

I/O = input/output

P = power

TTL = TTL input

ST = Schmitt Trigger input

CHAPTER 4

SIMULATION RESULTS

4.1 THREE PHASE MODEL

The three single phase subsystems are star connected to obtain the three structure is shown in Fig 4.1.The single phase structure is shown in Fig 4.2.

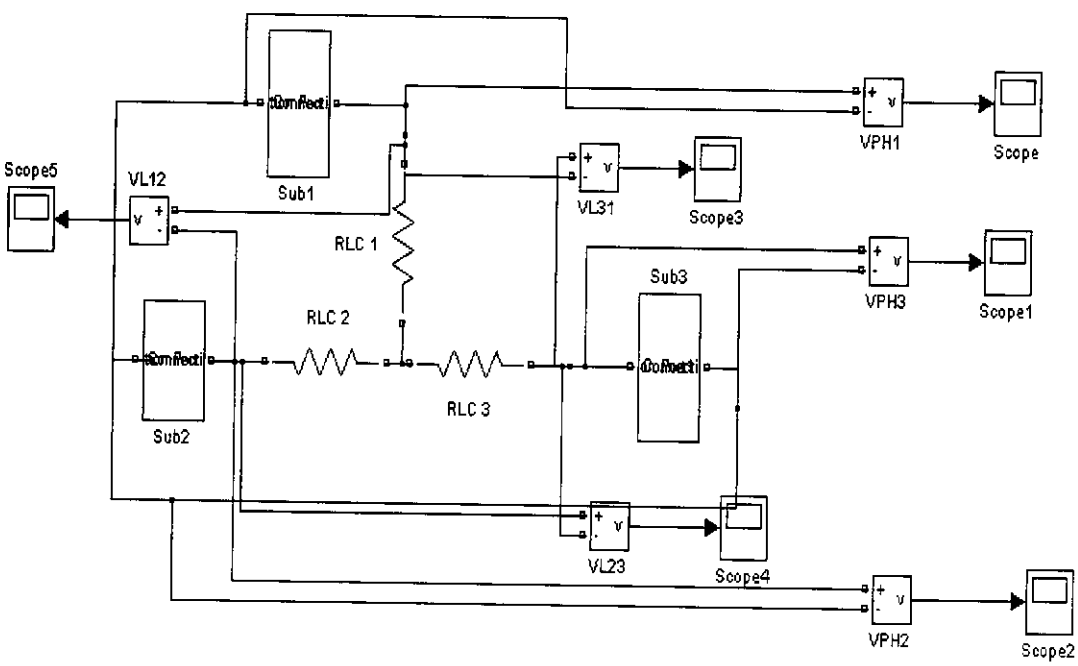


Figure 4.1

4.2 SINGLE PHASE MODEL

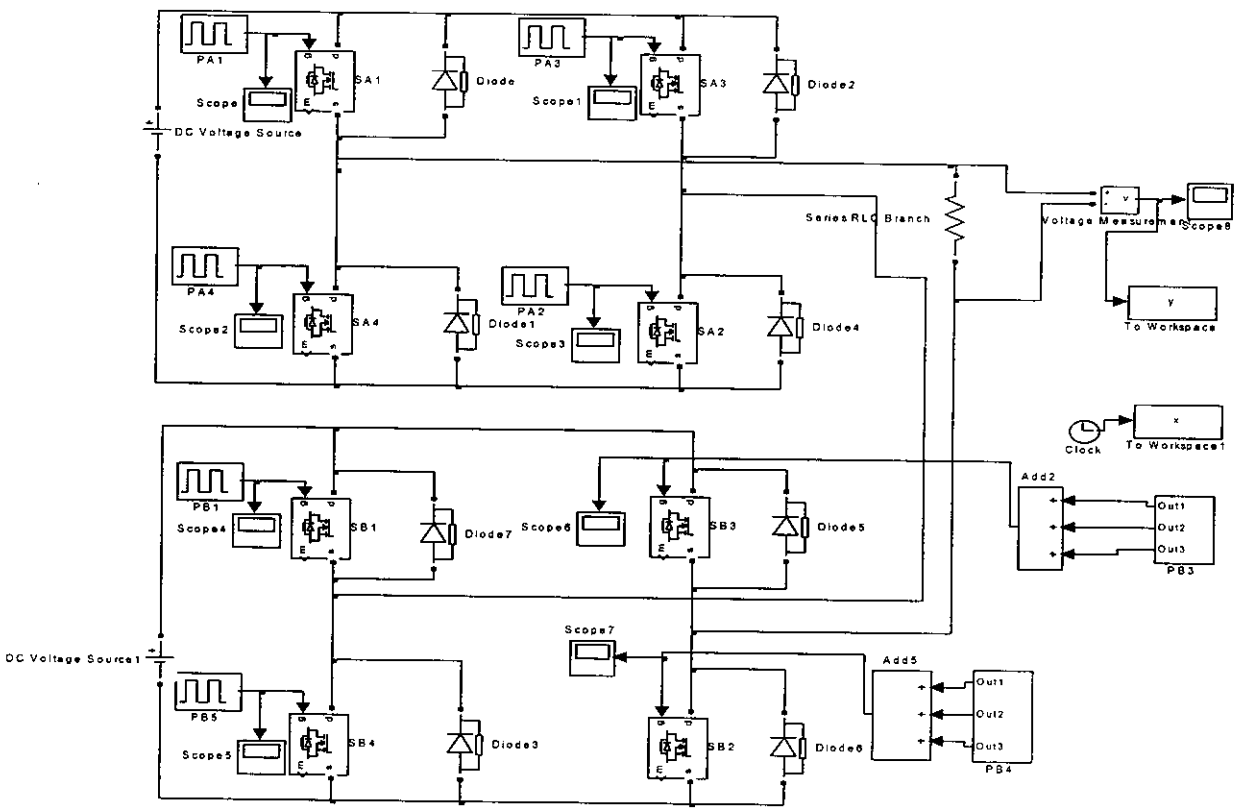
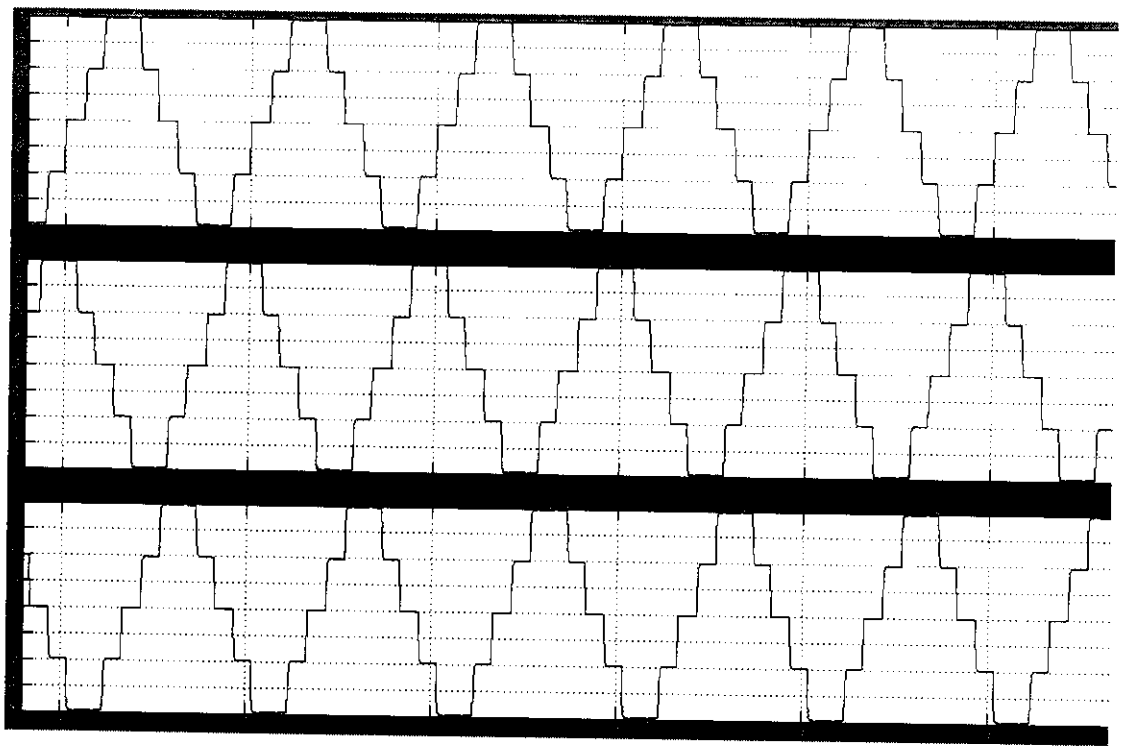


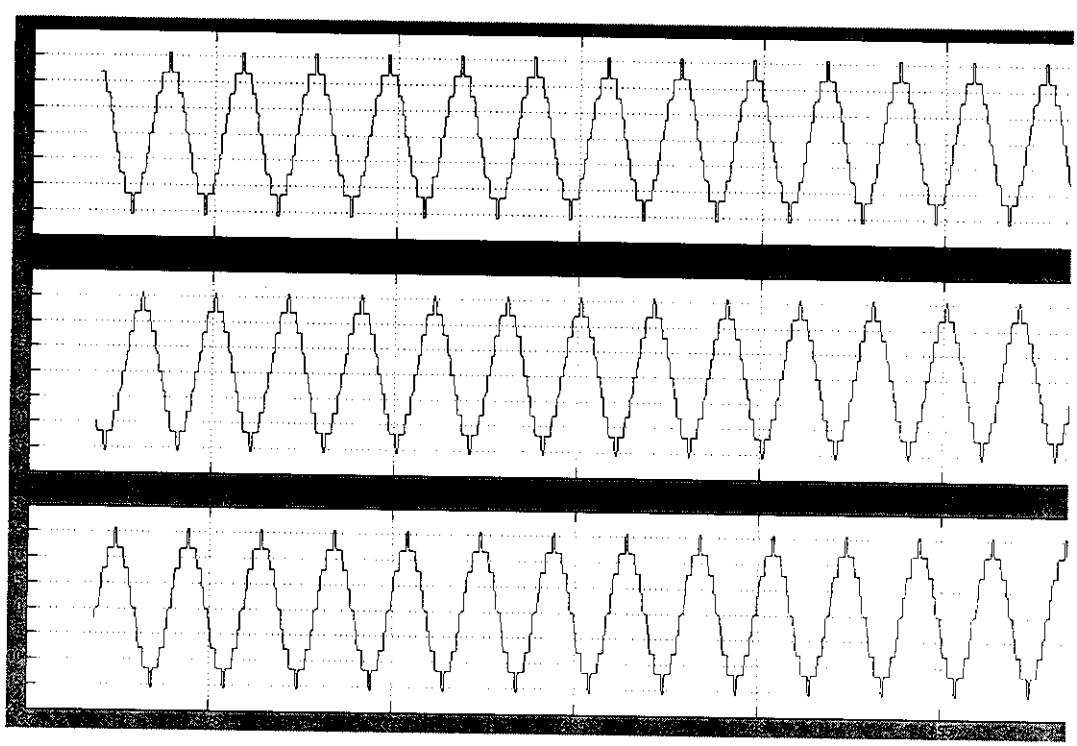
Figure 4.2

4.3 OUTPUT VOLTAGES

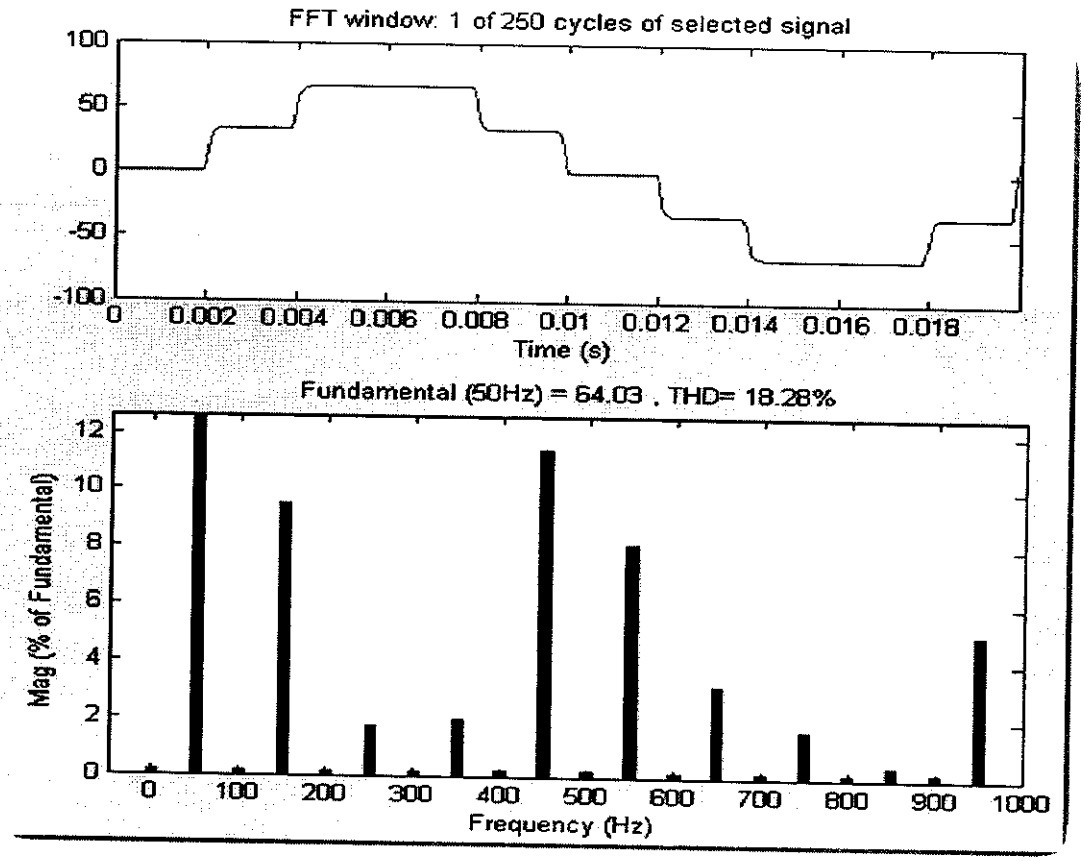
4.3.1 PHASE VOLTAGE:



4.3.2 LINE VOLTAGES:



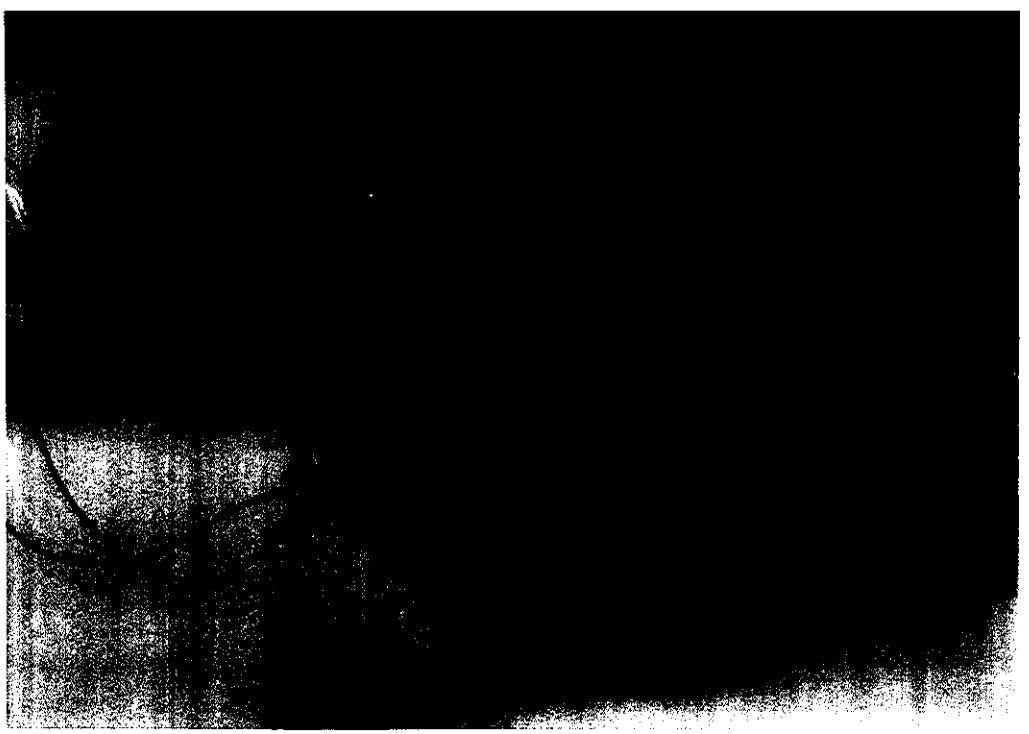
4.4 TOTAL HARMONIC DISTORTION (THD) ANALYSIS



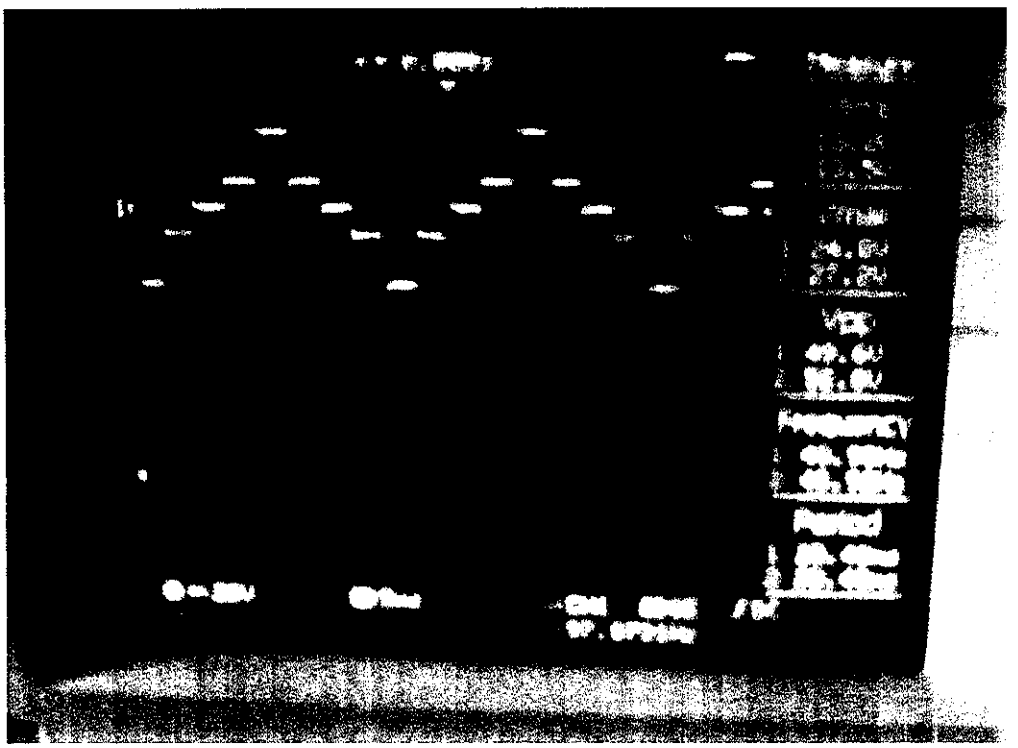
CHAPTER 5

HARDWARE

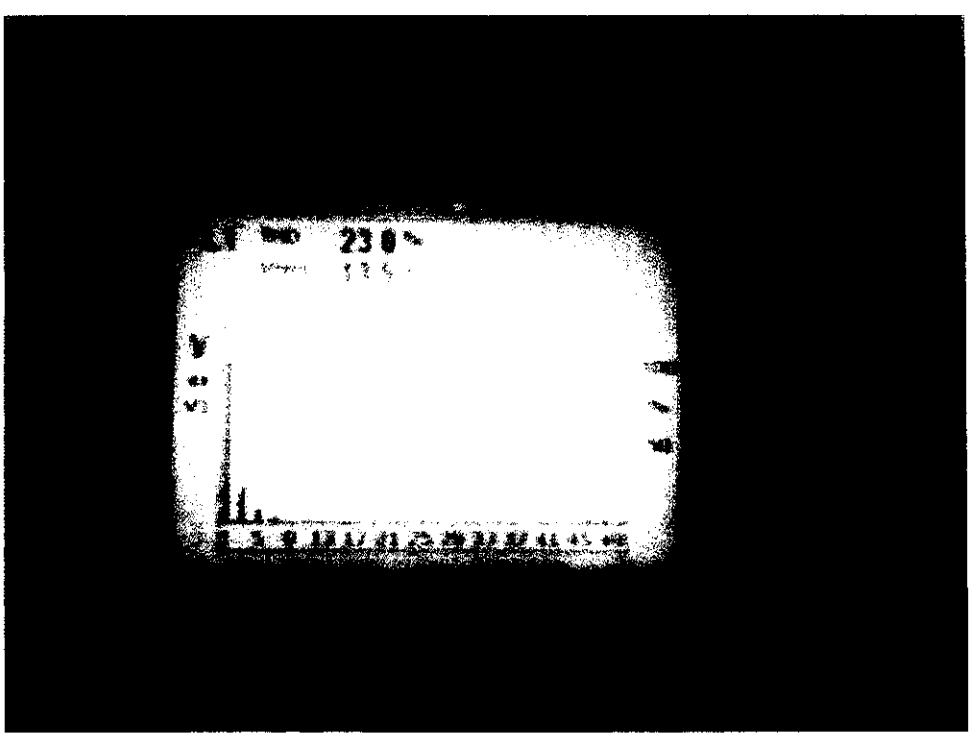
5.1 HARDWARE MODEL PHOTOGRAPHY



5.2 OUTPUT VOLTAGE WAVEFORM



5.3 HARDWARE – HARMONIC ANALYSIS



CHAPTER 6

CONCLUSION

6.1 CONCLUSION

The three phase cascaded multilevel inverter produces five level phase voltage output with very low values of the low order Harmonics.This system synthesizes a desired AC output voltage waveform with lower THD as PIC microcontroller has been programmed to vary the duty cycle of the inverter .The simulated waveforms and the experimental results have been and verified.

6.2 FUTURE SCOPE

- DSP processor can be used in place of PIC microcontroller for better performance and faster response.
- Further the space vector modulation techniques may be used in multilevel inverter to give a better harmonic profile.
- Seven, nine or eleven level inverter can be fabricated in order to obtain better harmonic profile.

CHAPTER 7

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- J. Wen and K. M. Smedley, "Synthesis of multilevel converters based on single- and/or three-phase converter building blocks"
- M. F. Escalante and J. J. Arellano, "Harmonics and reactive power compensation using a cascaded H-bridge multilevel inverter,"
- J. Watson, P. W. Wheeler, and J. C. Clare, "A complete harmonic elimination approach to DC link voltage balancing for a cascaded multilevel rectifier," IEEE Trans. Ind. Electron

APPENDIX A

DATASHEETS OF PIC16F877A

PIC16F87X

Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions

DATASHEET OF MOSFET - IRZ44

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	50*	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	36	
I_{DM}	Pulsed Drain Current ①	200	
P_D @ T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	100	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.060	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.028	Ω	V_{GS}=10V, I_D=31A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	15	—	—	S	V_{DS}=25V, I_D=31A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=60V, V_{GS}=0V
		—	—	250		V_{DS}=48V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	67	nC	I_D=51A
Q_{gs}	Gate-to-Source Charge	—	—	18		V_{DS}=48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	25		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD}=30V
t_r	Rise Time	—	110	—		I_D=51A
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		R_G=9.1Ω
t_f	Fall Time	—	92	—		R_D=0.55Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1900	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	920	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	170	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	50*	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	200		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_J=25°C, I_S=51A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	T_J=25°C, I_F=51A
Q_{rr}	Reverse Recovery Charge	—	0.53	0.80	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

DATASHEET OF BUFFER - CD4049

Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBC, CD4050BC	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−40°C		−25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.03	4.0		30	µA
		V_{DD} = 10V		8		0.05	8.0		60	µA
		V_{DD} = 15V		16		0.07	16.0		120	µA
V_{OL}	LOW Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	LOW Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 0.4V	4.6		4.0	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	9.8		8.5	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	29		25	40		20		mA
I_{OH}	HIGH Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 4.6V	−1.0		−0.9	−1.6		−0.72		mA
		V_{DD} = 10V, V_O = 9.5V	−2.1		−1.9	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−7.1		−6.2	−12		−5		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3		−0.3	-10^{-5}			−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V	0.3		0.3	10^{-5}			1.0	µA

APPENDIX B

CODE FOR GENERTING PWM PULSES

```
#include<pic.h>
//__CONFIG(0x1F71);

__CONFIG(0x20E4);
__CONFIG(0x3FFF);

unsigned int V1,V2;
void main()
{
ANSEL=0;
ANSELH=0;
ADCON1=0x80;

PR2=99;
CCPR1L=50;
CCP1CON=0X0C;
T2CON=0X04;

TRISD=0XF0;
TRISC=0XF0;
TRISB=0;
TRISA=0x0F;
PORTC=0;
PORTB=0xff;

OPTION=0x87;
TMR0=0;

//    GIE=PEIE=INTE=T0IE=TMR1IE=1;

//    T1CON =0x01;
//    TMR1L = 0x00;
//    TMR1H = 0x00;

      while(1)
```

```
{
        PORTB=0x00;
        PORTD=0x0F;
        while(TMR0<4);
        PORTB=0x39;
        PORTD=0x0C;
        while(TMR0<8);

        PORTB=0x96;
        PORTD=0x0C;
        while(TMR0<12);
        PORTB=0x93;
        PORTD=0x0C;
        while(TMR0<16);

        PORTB=0x99;
        PORTD=0x0C;
        while(TMR0<20);
        PORTB=0x66;
        PORTD=0x06;
        while(TMR0<24);

        PORTB=0x63;
        PORTD=0x06;
        while(TMR0<28);
        PORTB=0x69;
        PORTD=0x06;
        while(TMR0<32);

        PORTB=0x36;
        PORTD=0x06;
        while(TMR0<36);
        PORTB=0x33;
        PORTD=0x06;
        while(TMR0<40);

        PORTB=0x39;
        PORTD=0x06;
```

```
while(TMR0<44);
PORTB=0x96;
PORTD=0x06;
while(TMR0<48);

PORTB=0x93;
PORTD=0x06;
while(TMR0<52);
PORTB=0x99;
PORTD=0x06;
while(TMR0<56);

PORTB=0x99;
PORTD=0x06;
while(TMR0<60);
PORTB=0x93;
PORTD=0x06;
while(TMR0<64);

PORTB=0x96;
PORTD=0x06;
while(TMR0<68);
PORTB=0x39;
PORTD=0x06;
while(TMR0<72);

PORTB=0x33;
PORTD=0x06;
while(TMR0<76);
PORTB=0x36;
PORTD=0x06;
while(TMR0<80);

PORTB=0x69;
PORTD=0x06;
while(TMR0<84);
PORTB=0x63;
PORTD=0x06;
```

```
while(TMR0<88);

PORTB=0x66;
PORTD=0x06;
while(TMR0<92);
PORTB=0x99;
PORTD=0x0C;
while(TMR0<96);

PORTB=0x93;
PORTD=0x0C;
while(TMR0<100);
PORTB=0x96;
PORTD=0x0C;
while(TMR0<104);

PORTB=0x39;
PORTD=0x0C;
while(TMR0<108);
PORTB=0x00;
PORTD=0x0F;
while(TMR0<112);


PORTB=0x00;
PORTD=0x0F;
while(TMR0<116);
PORTB=0xC6;
PORTD=0x03;
while(TMR0<120);

PORTB=0x69;
PORTD=0x03;
while(TMR0<124);
PORTB=0x6C;
PORTD=0x03;
while(TMR0<128);
```

```
PORTB=0x66;
PORTD=0x03;
while(TMR0<132);
PORTB=0x99;
PORTD=0x09;
while(TMR0<136);

PORTB=0x9C;
PORTD=0x09;
while(TMR0<140);
PORTB=0x96;
PORTD=0x09;
while(TMR0<144);

PORTB=0xC9;
PORTD=0x09;
while(TMR0<148);
PORTB=0xCC;
PORTD=0x09;
while(TMR0<152);

PORTB=0xC6;
PORTD=0x09;
while(TMR0<156);
PORTB=0x69;
PORTD=0x09;
while(TMR0<160);

PORTB=0x6C;
PORTD=0x09;
while(TMR0<164);
PORTB=0x66;
PORTD=0x09;
while(TMR0<168);

PORTB=0x66;
PORTD=0x09;
while(TMR0<172);
```

```
PORTB=0x6C;
PORTD=0x09;
while(TMR0<176);

PORTB=0x69;
PORTD=0x09;
while(TMR0<180);
PORTB=0xC6;
PORTD=0x09;
while(TMR0<184);

PORTB=0xCC;
PORTD=0x09;
while(TMR0<188);
PORTB=0xC9;
PORTD=0x09;
while(TMR0<192);

PORTB=0x96;
PORTD=0x09;
while(TMR0<196);
PORTB=0x9C;
PORTD=0x09;
while(TMR0<200);

PORTB=0x99;
PORTD=0x09;
while(TMR0<204);
PORTB=0x66;
PORTD=0x03;
while(TMR0<208);

PORTB=0x6C;
PORTD=0x03;
while(TMR0<212);
PORTB=0x69;
PORTD=0x03;
while(TMR0<216);
```

```
                PORTB=0xC6;
                PORTD=0x03;
                while(TMR0<220);
                PORTB=0x00;
                PORTD=0x0F;
                while(TMR0<224);

                TMR0=0;

        }

while(1);
}

delay_adc()
{
unsigned int i;
for(i=0;i<=400;i++);
}
```