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SPACE VECTOR MODULATION FOR NINE SWITCH INVERTER

A Project Report

Submitted by

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BONAFIDE CERTIFICATE

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ABSTRACT

This paper presents a Nine-switch converter for industrial and traction application with Space Vector Modulation (SVM) scheme for induction motor drives. Developed algorithm has several advantages like z source boosting up, wide speed operation range, good dynamics, low torque ripples, constant switching and low sampling frequency. The SVM can be used in various applications like electric vehicles, where field-weakening operation is required. Drive operation ranges including field-weakening region are described. Selected experimental results are measured on the induction motor drive, which illustrates steady state and dynamic performances of the developed system.

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It is our bounden duty to thank contribution made in one from or the other be the individuals we hereby acknowledge.

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CHAPTER 1

INTRODUCTION

1.1 GENERAL

Nowadays, there is a demand of power supply. As an **electrical engineer**, it is necessary to design system with low cost, reduced losses and higher efficiency. This paper proposes nine-switch converter with single controller, rather than using 12 switches for operation of drives separately. In electrical vehicle drives mostly AC motors are used.

It is because of its well known advantages like simplicity, reliability, lack of mechanical commutator and brushes, ability to work under unfriendly conditions (dust, humidity, etc.) and low cost. The most popular AC machines are induction motors - IM and permanent magnet synchronous motors - PMSM. These motors can be supplied from power electronics converters (like VSI inverters).

Therefore, are used in various applications like hybrid electric vehicles HEV, public transport, machine tools drives, etc. Some of these applications have to work above nominal speed. This is essential in EV and public transport drives. High-speed operation can be achieved either by increasing supply voltage (not always possible) or by field weakening. In the IM field-weakening operation can be easily performed.

The above requirements are not fulfilled in scalar control, where only angular speed (frequency) and magnitudes of flux, current and voltage vectors are adjusted. Instantaneous positions of these vectors are not controlled.

Therefore, space vector control methods have been strongly developed. In this case, not only angular speed (frequency) and magnitudes of flux, current and voltage vectors, but also instantaneous position of these vectors is controlled. This ensures excellent dynamic and stable steady state operation of space vector control methods.

1.2 OBJECTIVE

The aim of this project is to develop the space vector modulation (SVM) of nine-switch inverter and nine-switch-z-source inverter. Develop a method to increases the sum of modulation indices up to 15% in contrast with the conventional scheme in which the sum of modulation indices is less than the one by using Z source dc/dc inverter.

Also, in order to further reduce the cost of power devices and also thermal heat effect and to reduce the number of semiconductor switching, specific SVM switching pattern is presented. This feature will be advantageous for high-power inverter applications where cost and efficiency are key decision factors.

1.3 ORGANISATION OF THE REPORT

This report has been organized into the following chapters.

Chapter 1: Gives the introduction and objective of the project and the way the various chapters are organized.

Chapter 2: Focuses on the basic principle of PWM based inverters and operation of nine-switch inverter and implementation of space vector modulation in it.

Chapter 3: Explains the impedance source inverter and its advantages over the conventional inverters

Chapter 4: Describes the simulation model and results.

Chapter 5: Describes the hardware implementation of the project.

Chapter 6: Concludes the project with the scope for improvement.

CHAPTER 2

CHAPTER 2

PULSE WIDTH MODULATION

2.1 GENERAL:

The advent of the transformerless multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters.

In this method, a fixed dc input voltage is supplied to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers.

This is because: (1) such inverters are well adapted to high-speed self turn-off switching devices that, as solid-state power converters, are provided with recently developed advanced circuits; and (2) they are operated stably and can be controlled well.

The PWM control has the following advantages:

(i) The output voltage control can be obtained without any additional components.

(ii) With this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control.

(iii) The filtering requirements are minimized as higher order harmonics can be filtered easily.

The commonly used PWM control techniques are:

(a) Sinusoidal pulse width modulation (sin PWM)

(b) Space vector PWM

The performance of each of these control methods is usually judged based on the following parameters: a) Total harmonic distortion (THD) of the voltage and current at the output of the inverter, b) Switching losses within the inverter, c) Peak-to-peak ripple in the load current, and d) Maximum inverter output voltage for a given DC rail voltage.

From the above all mentioned PWM control methods, the Space vector modulation (SVM) is applied in the proposed inverter since it has various advantages over other techniques. SVM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage.

2.2 IMPLEMENTATION IN NINE-SWITCH INVERTER:

The carrier-based PWM control method for nine-switch inverter is shown in Fig2.1. There are two reference signals (upper and lower) for each phase. The upper and lower reference signals are related to upper and lower outputs respectively. The gate signal for upper switch of a leg is generated by comparing the carrier signal and upper reference signal of the related phase (VrefUJ).

Similarly, the gate signal for lower switch is generated from the carrier signal and lower reference signal of the related phase (VrefLJ). The gate signal for mid switch is generated by the logical XOR of the gate signals for upper and lower switches. With this method, always two switches are ON in each leg.

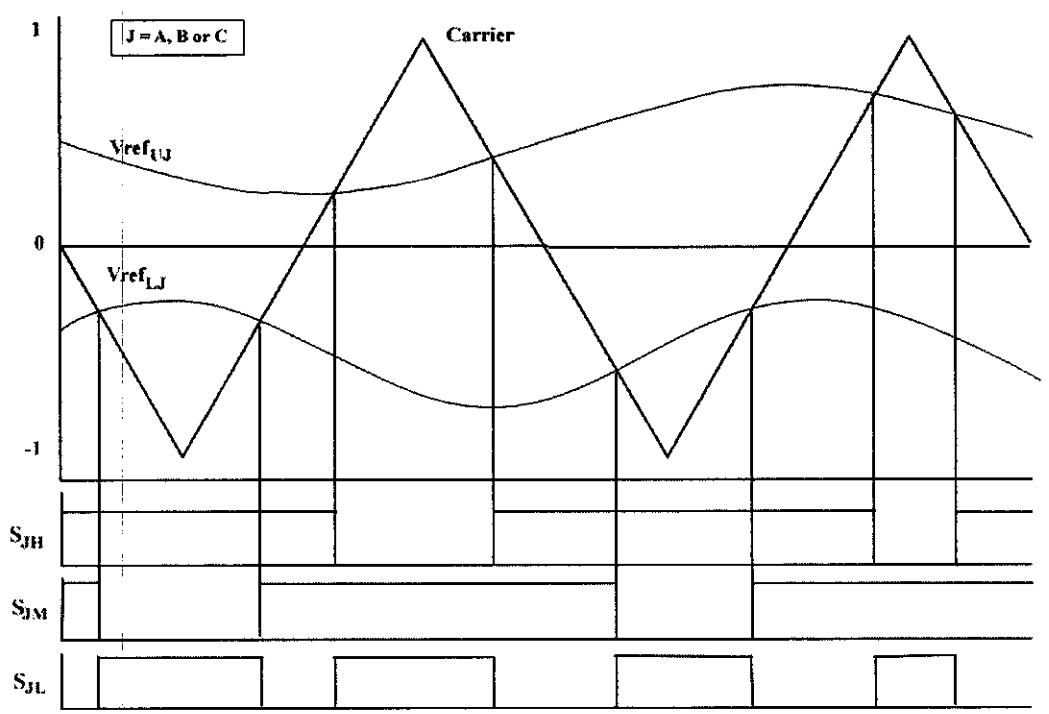

Fig2.1 Carrier based PWM

The fig 2.2 shows carrier-based PWM method switching vectors. There are six vectors in each switching cycle for both outputs: two nonzero vectors, one zero vector 0 0 0, two nonezero vectors and one zero vector 1 1 1 {two active—short zero (0 0 0)—two active—long zero (1 1 1)}. In an active vector, output load is connected to the dc input source, while in a zero vector, the output load is short-circuited. When one of the outputs has an active or short zero (0 0 0) vector, the other output has long zero (1 1 1) vector.

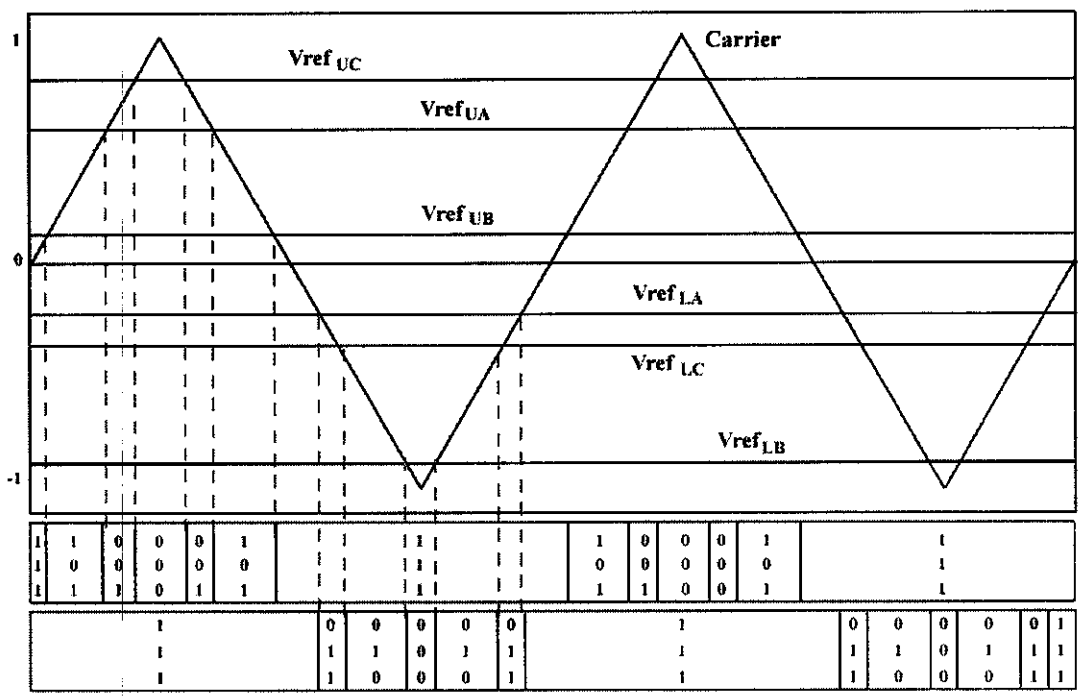

Fig2.2 Carrier based PWM for nine-switch converter

2.3 FORMING SWITCHING SEQUENCE

In regard to Fig2.3, each leg can be in three different semi- conductors ON-OFF position. These position can be called {1}, {0}, and {−1}, as is illustrated in Table I. In Table I, J refers to leg A, B, or C and U, M, L refers to upper, mid, and lower semiconductor, respectively.

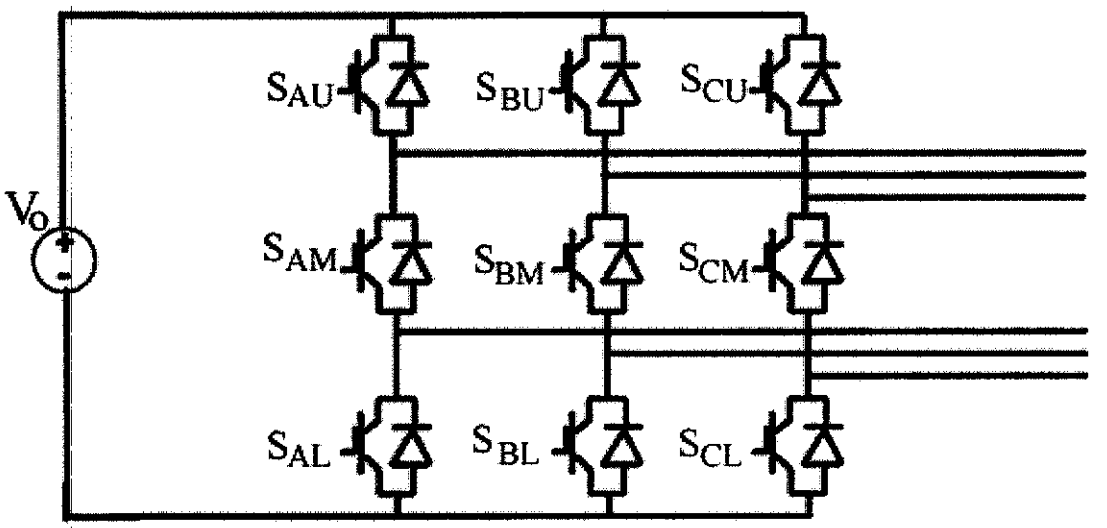

Fig 2.3 Nine-switch inverter

The combination of switching vector of both outputs in Fig 2.2 creates a specific sequence as shown in table 2. This sequence is used to design SVM method. There are 12 vectors in each switching cycle: {two upper active (V_{AU})-zero (V_Z)-two upper active (V_{AU})-zero (V_Z)-two lower active (V_{AL})-zero (V_Z)-two lower active (V_{AL})-zero (V_Z)}. The switching vectors are listed in Table II. The vectors V1 –V6 are upper active vectors. In these vectors, the upper output is in active state, and the lower output is in zero state. There is an inverse logic in lower active vectors (V_7–V_{12}). In zero vectors (V_{13}–V_{15}), both outputs are in zero state.

Table 1. Semiconductors ON-OFF position of legs

	S_{JU}	S_{JM}	S_{JL}
1	ON	OFF	ON
0	OFF	ON	ON
-1	ON	ON	OFF

Table 2. SVM switching vectors

Vector	Leg A	Leg B	Leg C	Type
1	1	0	0	Upper Active
2	1	1	0	
3	0	1	0	
4	0	1	1	
5	0	0	1	
6	0	0	1	
7	-1	1	1	Lower Active
8	-1	-1	1	
9	1	-1	1	
10	1	-1	-1	
11	1	1	-1	
12	-1	1	-1	
13	1	1	1	Zero
14	0	0	0	
15	-1	-1	-1	

Table 2 does not include all possible variations of switching states {1}, {0}, and {−1}. Since a vector including {−1} and {0} connects both loads to the dc source at the same time, the loads lose their independence and they cannot have independent frequencies. This is the reason for avoiding a vector that includes combinations of {−1} and {0}.

In none of the switching vectors as listed in Table 2, both outputs are not in an active state at the same time. However, in vectors including both {−1} and {0} such as {−1, 1, 0}, both outputs are in active state. These vectors are ignored because there are not all combinations of active vectors for both outputs.

For example, if upper output be in active vector (1 1 0), lower output can be in vectors (000),(100),(010),or(110)as shown in Fig 2.4. However, vectors (0 1 1), (0 0 1), and (1 0 1) are not available for lower output. Therefore, outputs cannot be controlled independently.

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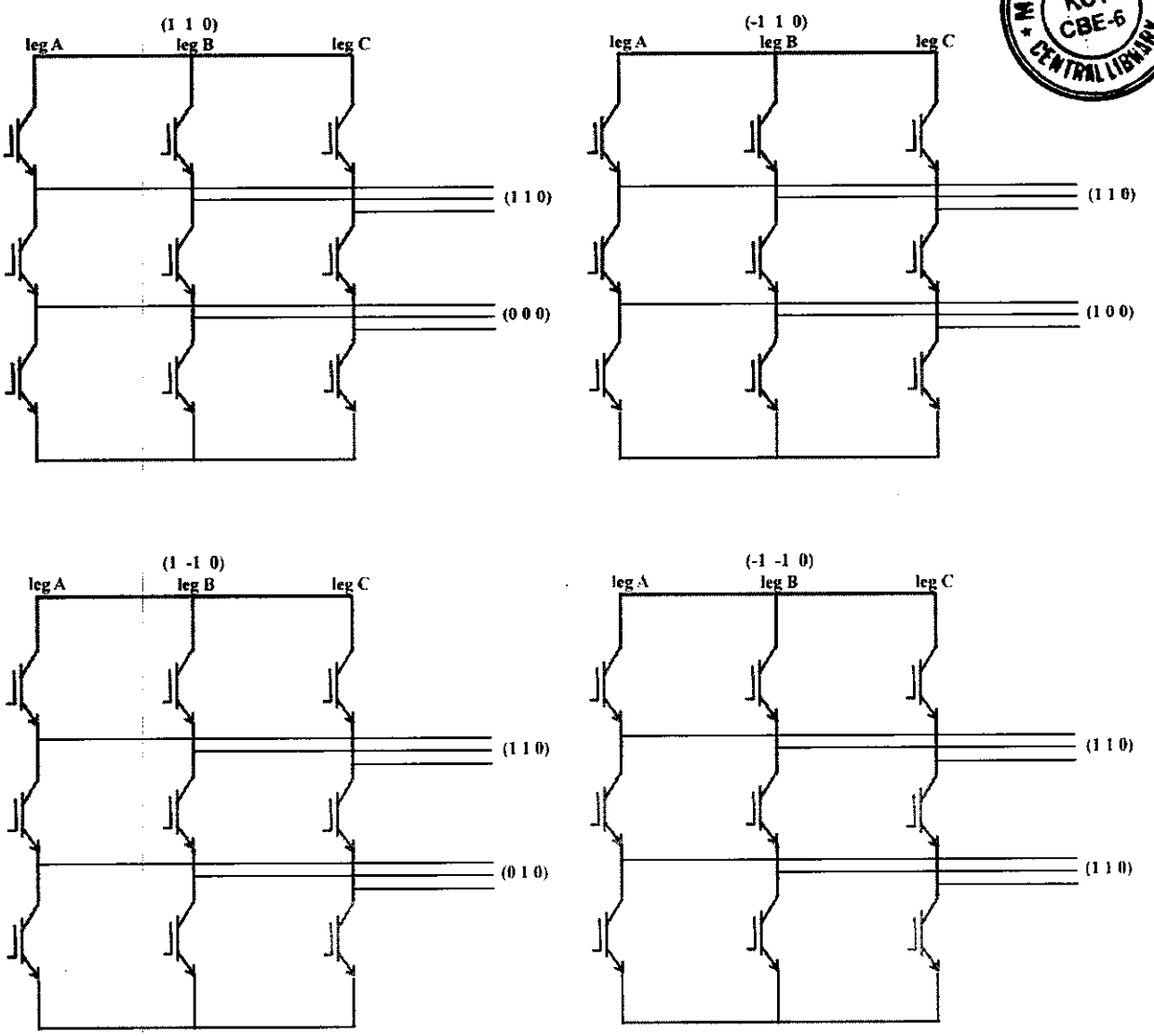


Fig 2.4 Available switching vectors of nine-switch inverter while upper output is in active vector (1 1 0).

2.3.1 DETERMING THE VECTORS

To determine the proper active vectors, two space vector diagrams are proposed as shown in Fig. 2.5.

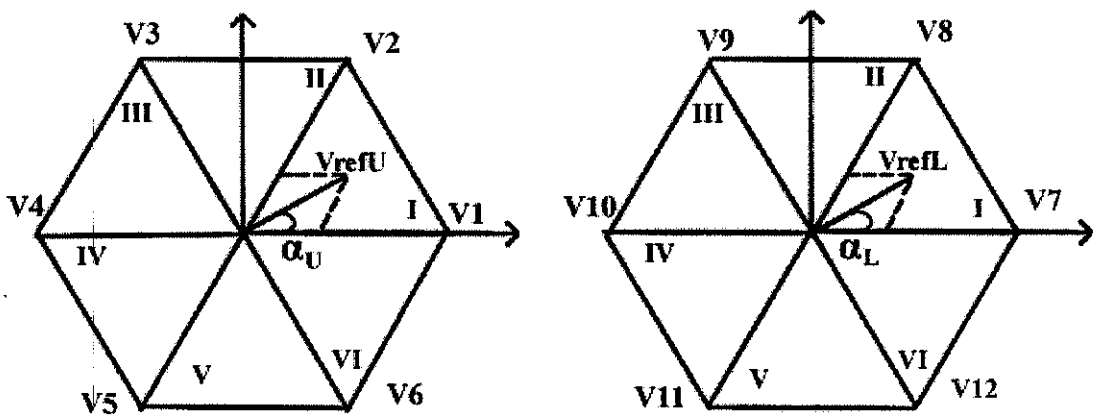


Fig 2.5 Space vector diagrams for nine-switch inverter. (a) Upper output. (a) Lower output.

The diagrams (a) and (b) are used to determine the upper and lower active vectors, respectively. The SVM active vectors are determined with regard to location of upper reference signal ($\bar{V}_{refU}$) in the diagram (a) and lower reference signal ($\bar{V}_{refL}$) in the diagram (b). The reference signals for the upper and lower outputs are defined as

$$V_{refU} = V_{refU}\alpha_U \qquad (1)$$

$$V_{refL} = V_{refL}\alpha_L \qquad (2)$$

$$\alpha_U = 2\pi f_U t + \varphi_U \qquad (3)$$

$$\alpha_L = 2\pi f_L t + \varphi_L \qquad (4)$$

where f_U , f_L are the frequencies, and φ_U , φ_L are the phases. All zero vectors V13 , V14, and V15 can be used for zero states. The type of zero vectors can be selected based on control goals and optimizations such as minimum number of semiconductor switchings.

The switching time intervals of vectors are calculated as

$T1=(\sqrt{3}/2)*(m_U*T*\sin\pi-\alpha_U)$ (5)

$T2= (\sqrt{3}/2)*m_U*T*\sin(\alpha_U)$ (6)

$T3= (\sqrt{3}/2)m_L*T*\sin(\pi/3-\alpha_L)$ (7)

$T4= (\sqrt{3}/2)m_L*T*\sin(\alpha_L)$ (8)

$T0=T-T1-T2-T3-T4$ (9)

Where T1, T2 arethetimeintervalofupperactivevectors, T3, T4 are time of lower active vectors, T0 is time of zero vectors and T is switching period. mU and mL are upper and lower modulation indices, respectively, and defined by

$m_U = 2V_{refU}/Vi$ (10)

$m_L = 2V_{refL}/Vi$ (11)

The sum of active vector time intervals must be less or equals to T . Thus, the following constrain must be satisfied

$$(m_U + m_L) \leq \sqrt{3}/2 \approx 1.155 \quad (12)$$

Equation (12) clearly indicates that in the proposed SVM scheme, sum of modulation indices increases about 15%—a very important feature to provide higher torque for a given input dc-voltage. In the case of washing machines, the above capability translates to higher machine capacity (in terms of cloth load) at high spin speed (e.g., 1800 r/min)—an important product feature in marketplace.

A switching vector sequence for the proposed SVM is shown in Fig. 2.7. This switching sequence is developed to reduce the number of semiconductor switching. The zero vectors are placed just between two upper and lower active vectors. In upper active vectors, legs are in state {1} or {0} and in lower active vectors, legs are in state {1} or {−1}. If V13 zero vector is placed between the active vectors, minimum number of switching is required. While if V14 or V15 zero vectors are used, number of switching is increased.

$V_{REF\,U}$ in I, III, or V $V_{REF\,L}$ in I, III, or V

V_{13}	V_{AU2}	V_{AU1}	V_{AU1}	V_{AU2}	V_{13}	V_{AL1}	V_{AL2}	V_{AL2}	V_{AL1}	V_{13}
$T_0/2$	T_2	T_1	T_1	T_2	T_0	T_3	T_4	T_4	T_3	$T_0/2$

$V_{REF\,U}$ in II, IV, or VI $V_{REF\,L}$ in I, III, or V

V_{13}	V_{AU1}	V_{AU2}	V_{AU2}	V_{AU1}	V_{13}	V_{AL1}	V_{AL2}	V_{AL2}	V_{AL1}	V_{13}
$T_0/2$	T_1	T_2	T_2	T_1	T_0	T_3	T_4	T_4	T_3	$T_0/2$

$V_{REF\,U}$ in I, III, or V $V_{REF\,L}$ in II, IV, or VI

V_{13}	V_{AU2}	V_{AU1}	V_{AU1}	V_{AU2}	V_{13}	V_{AL2}	V_{AL1}	V_{AL1}	V_{AL2}	V_{13}
$T_0/2$	T_2	T_1	T_1	T_2	T_0	T_4	T_3	T_3	T_4	$T_0/2$

$V_{REF\,U}$ in II, IV, or VI $V_{REF\,L}$ in II, IV, or VI

V_{13}	V_{AU1}	V_{AU2}	V_{AU2}	V_{AU1}	V_{13}	V_{AL2}	V_{AL1}	V_{AL1}	V_{AL2}	V_{13}
$T_0/2$	T_1	T_2	T_2	T_1	T_0	T_4	T_3	T_3	T_4	$T_0/2$

Fig 2.6 Space-vector modulation sequence vectors

There are two odd active vectors (V1, V3, V5, V8, V10, and V12) and two even active vectors (V2, V4, V6, V7, V9, and V11) in a switching sequence. In an even active vector, two legs are in state {1}, while in an odd active vector only one leg is in state {1}. If even active vectors are placed next to V13, number of switching will be reduced even more as in fig 2.6.

2.3.2 TOTAL HORMONIC DISTORTION REDUCTION:

There are other possible switch generation methods too, e.g., a switching method, to reduce THD. To minimize THD, active vectors for each output should be centrally placed within the switching period. Fig. 2.7 shows a switching vector sequence that shifts active vector into center of switching period, hence reducing THD. In this sequence, zero vectors are inserted between active vectors. In Fig.2.7 V14 is inserted between upper active vectors and V15 is inserted between lower active vectors.

$V_{REF\,U}$ in I, III, or V $V_{REF\,L}$ in I, III, or V

V_{AU2}	V_{AU1}	V_{14}	V_{AU1}	V_{AU2}	V_{AL1}	V_{AL2}	V_{15}	V_{AL2}	V_{AL1}
T_2	T_1	T_0	T_1	T_2	T_3	T_4	T_0	T_4	T_3

$V_{REF\,U}$ in II, IV, or VI $V_{REF\,L}$ in I, III, or V

V_{AU1}	V_{AU2}	V_{14}	V_{AU2}	V_{AU1}	V_{AL1}	V_{AL2}	V_{15}	V_{AL2}	V_{AL1}
T_1	T_2	T_0	T_2	T_1	T_3	T_4	T_0	T_4	T_3

$V_{REF\,U}$ in I, III, or V $V_{REF\,L}$ in II, IV, or VI

V_{AU2}	V_{AU1}	V_{14}	V_{AU1}	V_{AU2}	V_{AL2}	V_{AL1}	V_{15}	V_{AL1}	V_{AL2}
T_2	T_1	T_0	T_1	T_2	T_4	T_3	T_0	T_3	T_4

$V_{REF\,U}$ in II, IV, or VI $V_{REF\,L}$ in II, IV, or VI

V_{AU1}	V_{AU2}	V_{14}	V_{AU2}	V_{AU1}	V_{AL2}	V_{AL1}	V_{15}	V_{AL1}	V_{AL2}
T_1	T_2	T_0	T_2	T_1	T_4	T_3	T_0	T_3	T_4

Fig 2.7 SVM with reduced THD

CHAPTER 3

CHAPTER 3

IMPEDANCE SOURCE NETWORK

3.1 INTRODUCTION

TRADITIONAL SOURCE INVERTERS

Traditional source inverters are Voltage Source Inverter and Current Source Inverter. The input of Voltage Source Inverter is a stiff dc voltage supply, which can be a battery or a controlled rectifier both single phase and three-phase voltage source inverter are used in industry. The switching device can be a conventional MOSFET, Thyristor, or a power transistor.

Voltage source inverter is one which the dc source has small or negligible impedance. In other words a voltage source inverter has stiff dc source voltage at its input terminals. A current-fed inverter or current source inverter is fed with adjustable dc current source. In current source inverter the load does not affect output current waves.

Z-SOURCE INVERTER:

Z-Source Inverter (ZSI) is a novel inverter type that utilizes the traditional VSI or Current-Source Inverter (CSI) to achieve both buck and boost operations on voltage or current during inversion. The hardware circuit only requires two inductors, two capacitors and a diode in addition to the VSI. Furthermore, a significant change in switching pattern is also required to achieve this objective. The resulting single-stage boost type inverter saves cost, size and complexity over the conventional two-stage power-conditioning unit.

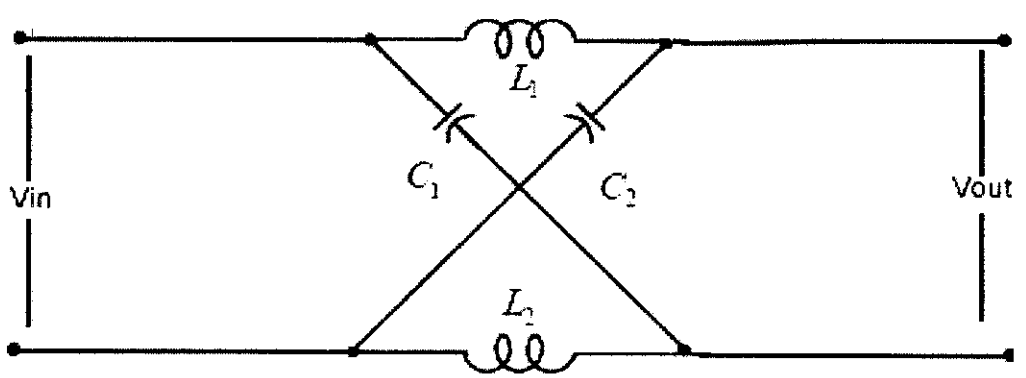


Fig 3.1 Z-source network

ADVANTAGES OF IMPEDANCE SOURCE NETWORK:

- The impedance source inverter concept can be applied to all ac-ac, dc-dc, ac-dc, dc-ac power conversion.
- The output voltage range is not limited.
- The impedance source inverter is used as a buck-boost inverter
- The impedance source inverter is immune to EMI noise
- The cost is low.
- It provides the buck-boost function by two stage power conversion.

3.2 IMPLEMETATION OF Z SOURCE NETWORK:

The nine-switch-z-source inverter is shown in Fig. 2. This inverter has an extra z-source network including two inductors (L1 and L2), two capacitors (C1 and C2) and a diode (D). The z-source network is similar to a dc/dc boost converter.

$$V_i = BV_O \qquad (13)$$

where V_O is input dc voltage and V_i is output of z-source network.

B is known as boost factor and is given by following equation:

$$B = 1/(1-2(T_{sc}/T)) \qquad (14)$$

where T_{sc} is shoot-through time. In the shoot-through times, the output of z-source network is shorted through the switches of the inverter. During shoot-through state, since the inverter (output of z-source network) is shorted, inverter cannot have an active vector. Therefore a shoot-through state can only occur when the inverter has a zero state.

Table 3. Shoot through vectors of nine-switch z-source inverter

Vector	Leg A	Leg B	Leg C
16	2	2	2
17	2	2	0
18	2	2	1
19	2	2	-1
20	2	0	2
21	2	1	2
22	2	-1	2
23	0	2	2
24	1	2	2
25	-1	2	2
26	2	0	0
27	2	1	1
28	2	-1	-1
29	0	2	0
30	1	2	1
31	-1	2	-1
32	0	0	2
33	1	1	2
34	-1	-1	2

Table 4. On-Off position of semiconductor switches in state (2)

	S_{JU}	S_{JM}	S_{JL}
2	ON	ON	ON

Table 3 shows all the vectors that the inverter includes zero state and the z-source network has a shoot-through state. These vectors are known as shoot- through vectors. There is a new state (state {2}) in Table 3. The ON-OFF position of switches of a leg in state {2} is shown in Table 4. All vectors of Table III can be used for generating a shoot-through state.

$V_{REF\,U}$ in I, III, or V

V_{13}	V_{SCU}	V_{AU2}	V_{AU1}	V_{AU1}	V_{AU2}	V_{SCU}	V_{13}	V_{SCL}	V_{AL1}	V_{AL2}	V_{AL2}	V_{AL1}	V_{SCL}	V_{13}
	$T_{SC}/2$					$T_{SC}/2$		$T_{SC}/2$					$T_{SC}/2$	
$T_0/2$		T_2	T_1	T_1	T_2		T_0		T_3	T_4	T_4	T_3		$T_0/2$

$V_{REF\,U}$ in II, IV, or VI $V_{REF\,L}$ in I, III, or V

V_{13}	V_{SCU}	V_{AU1}	V_{AU2}	V_{AU2}	V_{AU1}	V_{SCU}	V_{13}	V_{SCL}	V_{AL1}	V_{AL2}	V_{AL2}	V_{AL1}	V_{SCL}	V_{13}
	$T_{SC}/2$					$T_{SC}/2$		$T_{SC}/2$					$T_{SC}/2$	
$T_0/2$		T_1	T_2	T_2	T_1		T_0		T_3	T_4	T_4	T_3		$T_0/2$

$V_{REF\,U}$ in I, III, or V $V_{REF\,L}$ in II, IV, or VI

V_{13}	V_{SCU}	V_{AU2}	V_{AU1}	V_{AU1}	V_{AU2}	V_{SCU}	V_{13}	V_{SCL}	V_{AL2}	V_{AL1}	V_{AL1}	V_{AL2}	V_{SCL}	V_{13}
	$T_{SC}/2$					$T_{SC}/2$		$T_{SC}/2$					$T_{SC}/2$	
$T_0/2$		T_2	T_1	T_1	T_2		T_0		T_4	T_3	T_3	T_4		$T_0/2$

$V_{REF\,U}$ in II, IV, or VI $V_{REF\,L}$ in II, IV, or VI

V_{13}	V_{SCU}	V_{AU1}	V_{AU2}	V_{AU2}	V_{AU1}	V_{SCU}	V_{13}	V_{SCL}	V_{AL2}	V_{AL1}	V_{AL1}	V_{AL2}	V_{SCL}	V_{13}
	$T_{SC}/2$					$T_{SC}/2$		$T_{SC}/2$					$T_{SC}/2$	
$T_0/2$		T_1	T_2	T_2	T_1		T_0		T_4	T_3	T_3	T_4		$T_0/2$

Fig 3.2. Nine-switch z-source inverter SVM with reduced switching

Fig 3.2 shows a SVM vector sequence for nine-switch inverter with reduced number of switching. The sequence is a modified version of Fig. 8. Two shoot-through vectors are placed in both sides of zero vector (V13). Here, the shoot-through vector close to upper active vector is called upper shoot-through vector (V_{SCU}) and the shoot-through vector close to lower active vector is called lower shoot-through vector (V_{SCL}). All vectors listed in Table 3 can be used as the upper and lower shoot-through vectors.

However, vectors V27, V30, and V33 are preferred because those vectors have only one state {2} and need less switching. As shown in Fig.10, even active vectors are placed close to shoot-through vectors.

In even active vectors, two legs are in state {1} and one leg is in state {0} or {−1}. On other hand, in shoot- through vectors V27, V30, and V33, two legs are in state {1} and one leg is in state {2}. To reduce the number of switching, the two legs in state {1} must have the same state in an even active vector and shoot-through vector close to it. Table 5 can be used for shoot-through vectors selection.

Table5.Determining upper and lower shoot-through vector with reduced number of switching

Section of V_{refU}	V_{SCU}	Section of V_{refL}	V_{SCL}
I	V_{33}	I	V_{27}
II	V_{33}	II	V_{30}
III	V_{27}	III	V_{30}
IV	V_{27}	IV	V_{33}
V	V_{30}	V	V_{33}
VI	V_{30}	VI	V_{27}

Table 6. Determining upper and lower shoot-through vector with reduced THD

Section of V_{refU}	V_{SCU}	Section of V_{refL}	V_{SCL}
I	V_{26}	I	V_{34}
II	V_{29}	II	V_{34}
III	V_{29}	III	V_{28}
IV	V_{32}	IV	V_{28}
V	V_{32}	V	V_{31}
VI	V_{26}	VI	V_{31}

For reducing THD, switching sequence shown in Fig.3.3 is developed for nine-switch-z-source inverter. Similar to Fig.3.2, zero vectors and shoot-through vectors are inserted between similar active vectors. Table VI can be used for shoot-through vector selection with reduced THD.

$V_{REF\,U}$ in I, III, or V — $V_{REF\,L}$ in I, III, or V

V_{AU2}	V_{AU1}	V_{SCU}	V_{14}	V_{SCU}	V_{AU1}	V_{AU2}	V_{AL1}	V_{AL2}	V_{SCL}	V_{15}	V_{SCL}	V_{AL2}	V_{AL1}
T_2	T_1	$T_{SC}/2$	T_0	$T_{SC}/2$	T_1	T_2	T_3	T_4	$T_{SC}/2$	T_0	$T_{SC}/2$	T_4	T_3

$V_{REF\,U}$ in II, IV, or VI — $V_{REF\,L}$ in I, III, or V

V_{AU1}	V_{AU2}	V_{SCU}	V_{14}	V_{SCU}	V_{AU2}	V_{AU1}	V_{AL1}	V_{AL2}	V_{SCL}	V_{15}	V_{SCL}	V_{AL2}	V_{AL1}
T_1	T_2	$T_{SC}/2$	T_0	$T_{SC}/2$	T_2	T_1	T_3	T_4	$T_{SC}/2$	T_0	$T_{SC}/2$	T_4	T_3

$V_{REF\,U}$ in I, III, or V — $V_{REF\,L}$ in II, IV, or VI

V_{AU2}	V_{AU1}	V_{SCU}	V_{14}	V_{SCU}	V_{AU1}	V_{AU2}	V_{AL2}	V_{AL1}	V_{SCL}	V_{15}	V_{SCL}	V_{AL1}	V_{AL2}
T_2	T_1	$T_{SC}/2$	T_0	$T_{SC}/2$	T_1	T_2	T_4	T_3	$T_{SC}/2$	T_0	$T_{SC}/2$	T_3	T_4

$V_{REF\,U}$ in II, IV, or VI — $V_{REF\,L}$ in II, IV, or VI

V_{AU1}	V_{AU2}	V_{SCU}	V_{14}	V_{SCU}	V_{AU2}	V_{AU1}	V_{AL2}	V_{AL1}	V_{SCL}	V_{15}	V_{SCL}	V_{AL1}	V_{AL2}
T_1	T_2	$T_{SC}/2$	T_0	$T_{SC}/2$	T_2	T_1	T_4	T_3	$T_{SC}/2$	T_0	$T_{SC}/2$	T_3	T_4

Fig 3.3 Nine-switch z-source inverter SVM with reduced switching

CHAPTER 4

CHAPTER 4

SIMULATION AND RESULTS

The simulations for the project are carried out in Matlab simulink software. The simulation results verify that the proposed project reduces the number of switches used for controlling two three phase loads. The inverter is designed in the model window and the control system is designed as a separate subsystem with the following parameters.

4.1 SIMULATION PARAMETERS

Parameter	Value
Switching frequency	3 khz
Frequency for upper load	25 hz
Frequency for lower load	50 hz
Lf	1 mh
Cf	20 μF

4.2 SIMULINK DIAGRAM

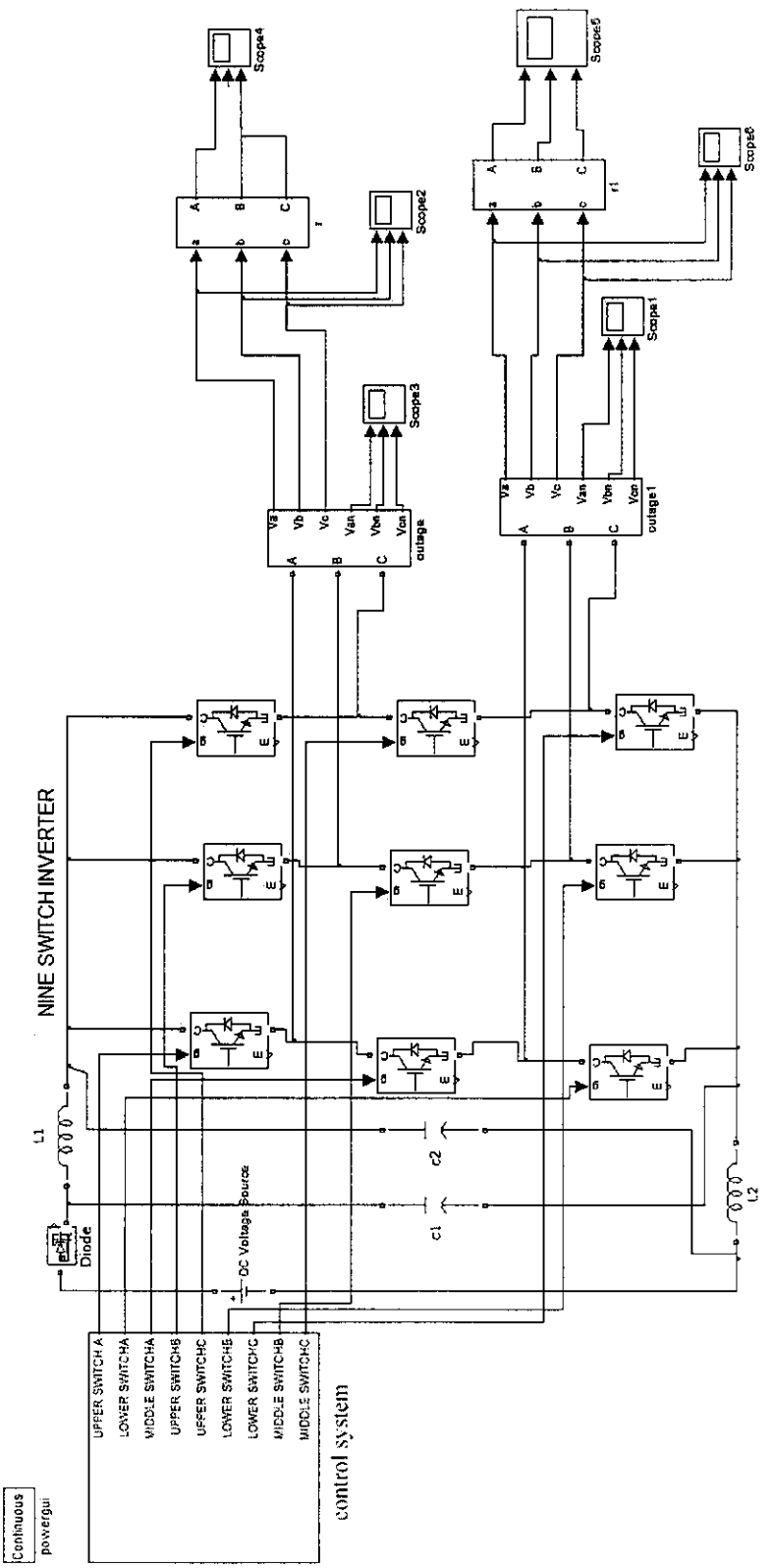
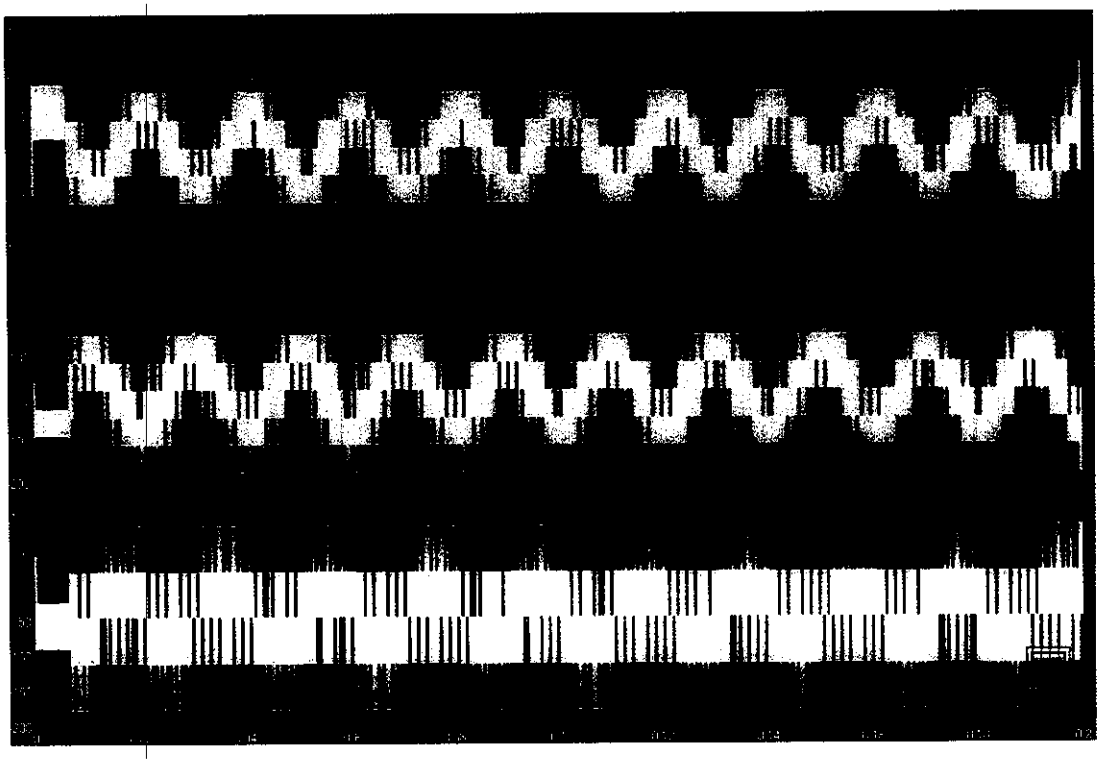


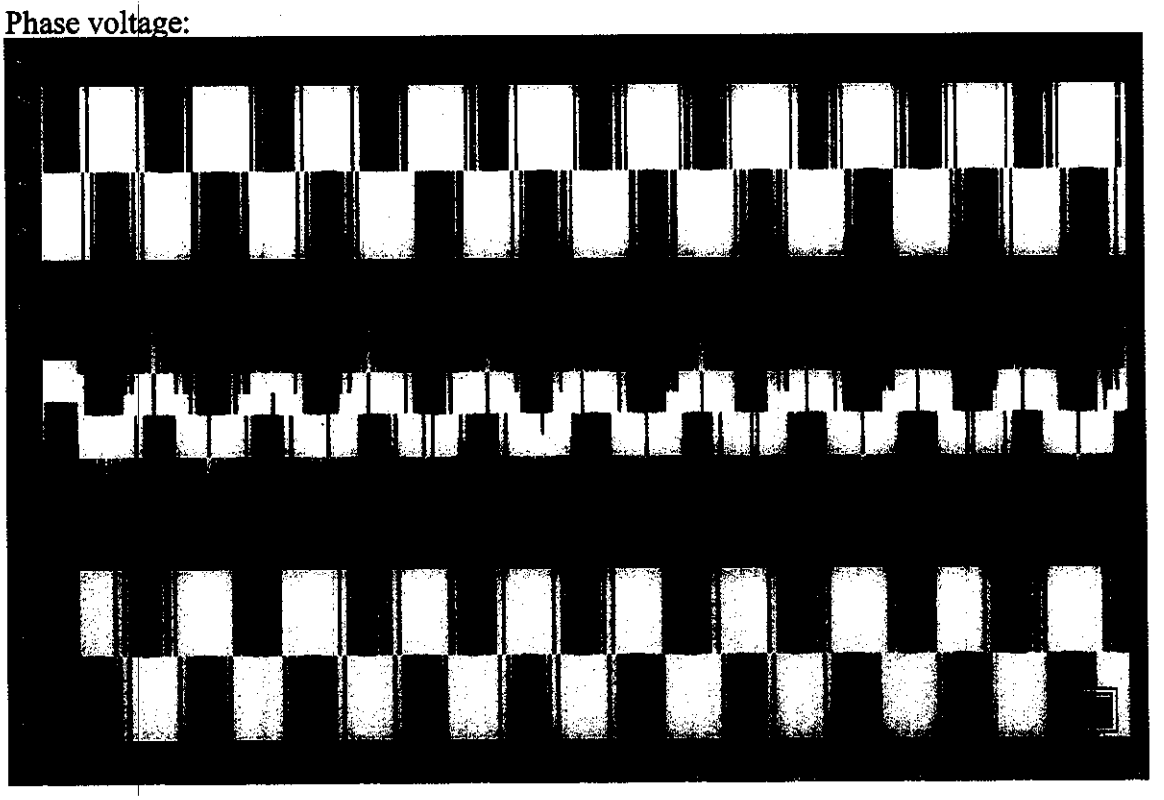
Fig 4.1 Simulink Diagram

4.3 SIMULATION RESULTS:

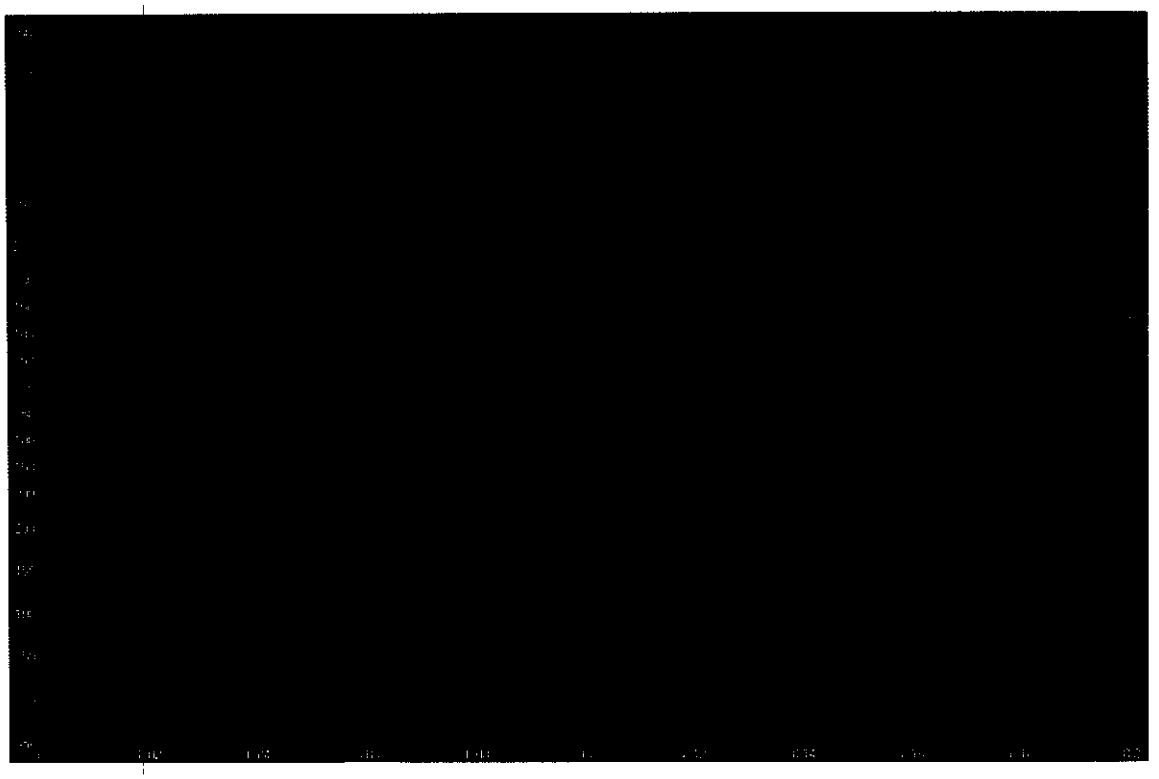
Line voltage:



Phase voltage:



Filtered Waveform:



CHAPTER 5

CHAPTER 5

HARDWARE IMPLEMENTATION

5.1 OVERALL BLOCK DIAGRAM

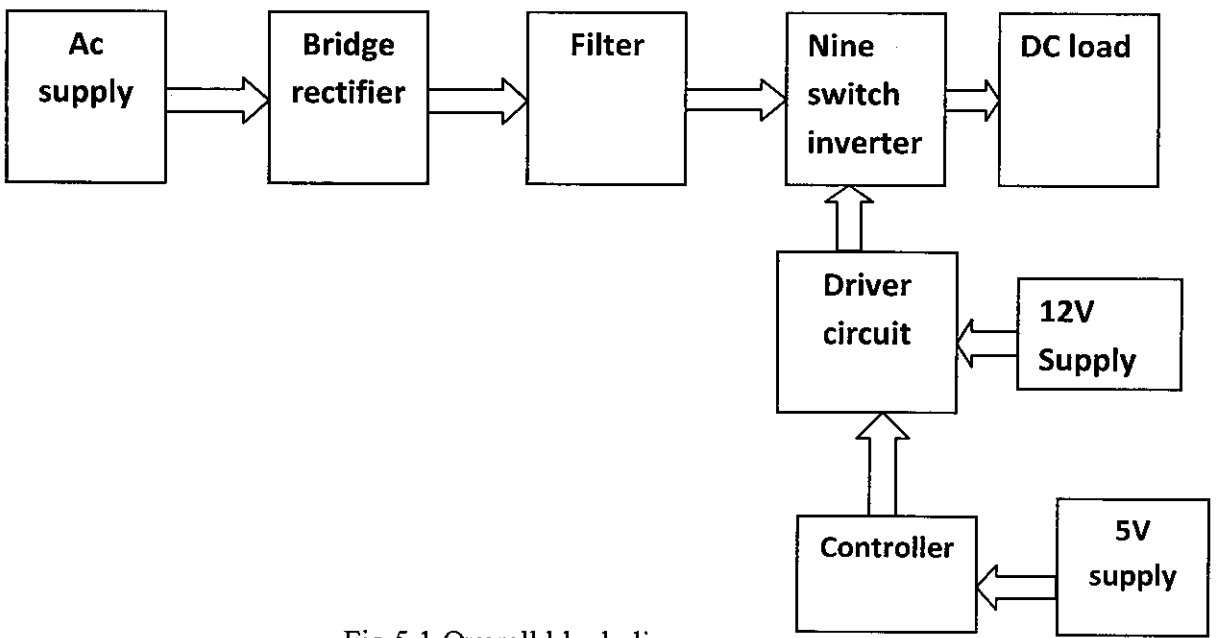


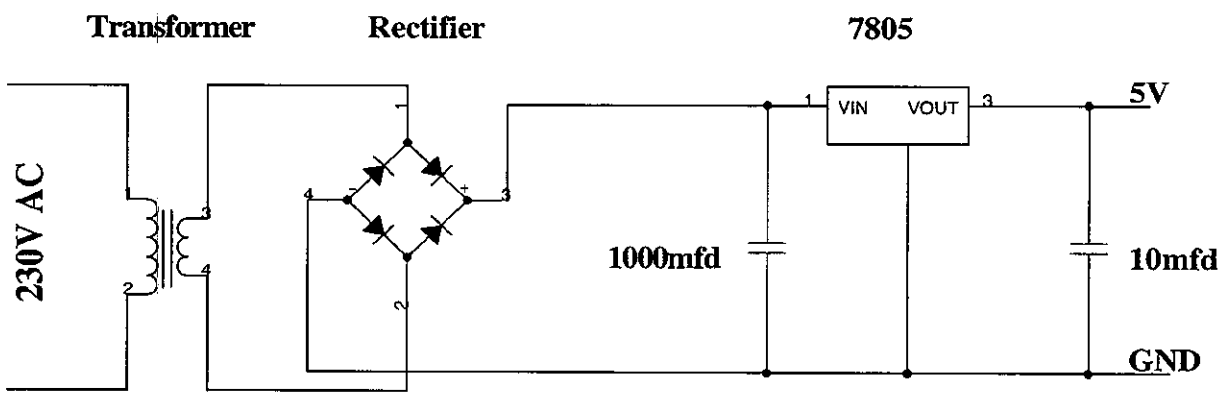
Fig 5.1 Overall block diagram

The circuit consists of the following blocks

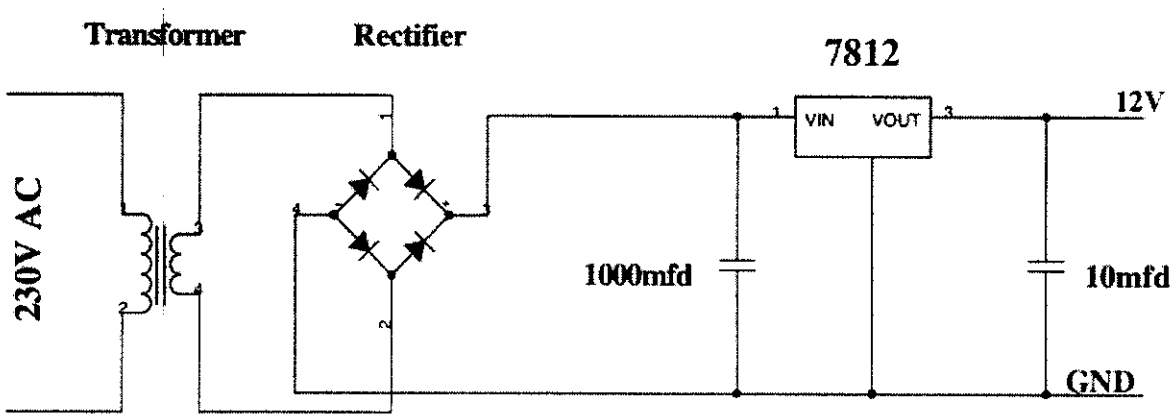
- Input transformer
- Power supply circuit
- Impedance source
- Inverter bridge
- PIC microcontroller

5.2 POWER SUPPLY:

Since all electronics circuits work only with low DC voltage, a power supply unit is needed to provide the approximate voltage supply. This unit consists of transformer, receiver, filter and regulator. AC voltage typically 230 V is connected to a step down transformer. The output of transformer is given to the bridge rectifier and then a simple capacitor filter to produce a DC voltage initially filters it. This DC voltage is given to regulator, which gives a constant DC voltage.



+5v power supply



+12V power supply

Fig 5.2 Power supply

5.2.1 TRANSFORMER

A transformer is a static piece of which electric power in one circuit is transformed into electric power of same frequency in another circuit. It can raise or lower the voltage in a circuit but with corresponding decrease or increase in current. Step down transformer have been used for providing a necessary supply for the electronic circuit.

5.2.2 RECTIFIER

Rectifier to be used is bridge rectifier. It is now available in a single entity. It is IR BR 6840. Here IR stands for INTERNATIONAL RECTIFIER that is the company manufacturing the product. BR stands for the bridge rectifier.6 stands for it's rating that is 600V, 6A. Rectifier is used for converting AC into pulsating DC. Here instead of using the DC source such as battery we are using the rectifier because those sources have fewer lifetimes.

Certain parameters of the IR BR 6840 are given below:

Maximum peak reverse voltage = 800V

Maximum RMS voltage = 560 V

Maximum DC blocking voltage = 500V

5.2.3 FILTER

Filtering should be done in order to reduce the harmonics and ripples. For this purpose we use capacitors for the filtering. They are rated at 100 V. Here output voltage from rectifier is 100V. The capacitors are used in two arms. They share this voltage equally. The capacitors are therefore rated at 1000 μf/100V. Each of the capacitors share 50V.The capacitors is electrolytic in nature.

5.2.4 REGULATOR

Regulator IC units contains the circuitry for reference source, comparator amplifier, control device and overload protection in a single IC. Although the internal construction of the IC is somewhat different from that described one, the external operation is the same. IC units provide regulation of a fixed positive voltage, a fixed

negative voltage or an adjustable set voltage. A power supply can be built using a transformer connected to the AC supply line to step the AC voltage to the desired amplitude. It is then rectified filtered with the capacitor and finally regulating the DC voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tones of amperes, corresponding to power rating from milli watts to tens of watts.

5.3 NINE SWITCH INVERTER:

A dual output inverter has been developed using only nine semiconductor switches (see Fig. 1). This inverter is known as nine-switch inverter. The nine-switch inverter is composed of two conventional inverters with three common switches. The switches used are MOSFETs.

In nine-switch inverter, sum of modulation index of two outputs must be less than or equal to one. Therefore, voltage amplitude of outputs is smaller, compared with two separate inverters. To remedy this problem, this paper proposes using an impedance source (z-source) network in front of nine-switch inverter as a dc/dc boost converter. Z-source network was used as front-end boost converter.

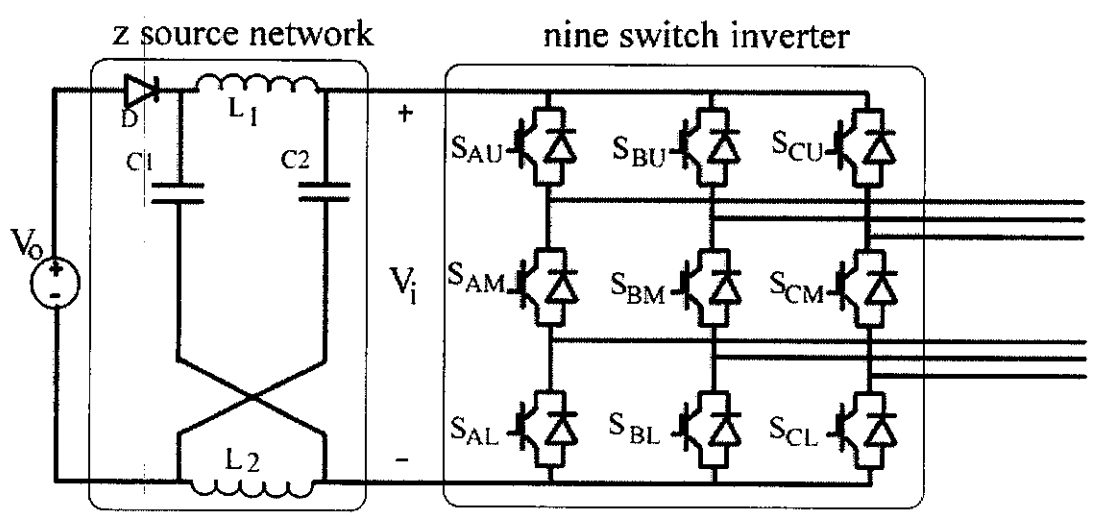


Fig 5.3 Nine switch inverter with impedance network

5.4 MOSFET:

MOSFET used is IRF P250. It's voltage rating is 250V, current rating is 20A.It has following advantages:

(1)Extremely high dv/dt capability

(2)Very low intrinsic capacitances

(3)Gate charge is minimized.

(4)Fast switching is possible.

(5)Ease of paralleling with other MOSFET.

The distance between the pins of IRFP460 is optimal and hence it meets the safety requirements. Certain absolute maximum ratings of various parameters are given below:

Drain current at V_{GS} =10V is 20A

Gate to Source voltage V_{GS} = 20V

dv/dt of IRFP6840 is = 3.5V/ns

It is used in following applications:

(1)High current switching.

(2)Uninterruptible power supply.

(3)Inverters such as this system

The internal schematic diagram of IRFP46 is shown in following figure.4.5

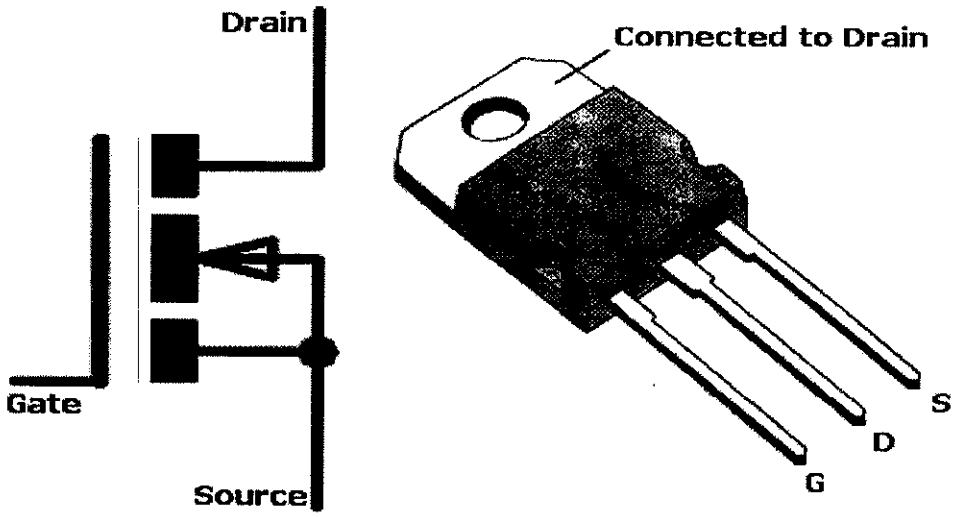


Fig 5.4 Schematic of a MOSFET

5.5 PIC MICROCONTROLLER:

The 16F877A PIC microcontroller is used for generating the pulses of the desired pulse width for driving the MOSFETs, by fixing either the frequency or voltage so that the MOSFETS are turned ON and OFF in the desired sequence.

The port C is used as the output port that gives the gate signals, whereas the port B is used as the input port, which receives the signals from the tact switch.

5.5.1 TACT SWITCH

A tact switch is type of switch that is only on when the button is pressed. Four of these switches are used to give input to the micro controller regarding choosing the speed of the motor. One of these four switches is a reset switch that is used to stop the motor.

Fig 5.5 Tact switch

5.2 FEATURES OF THE PIC 16F877A MICROCONTROLLER

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input

  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,

  Up to 368 x 8 bytes of Data Memory (RAM)

  Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack

- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:
  - ⇒ 2mA typical @ 5V, 4 MHz
  - ⇒ 20mA typical @ 3V, 32 kHz
  - ⇒ 1mA typical standby current

5.5.3 PIC 16F877A BASED CONTROL CIRCUIT

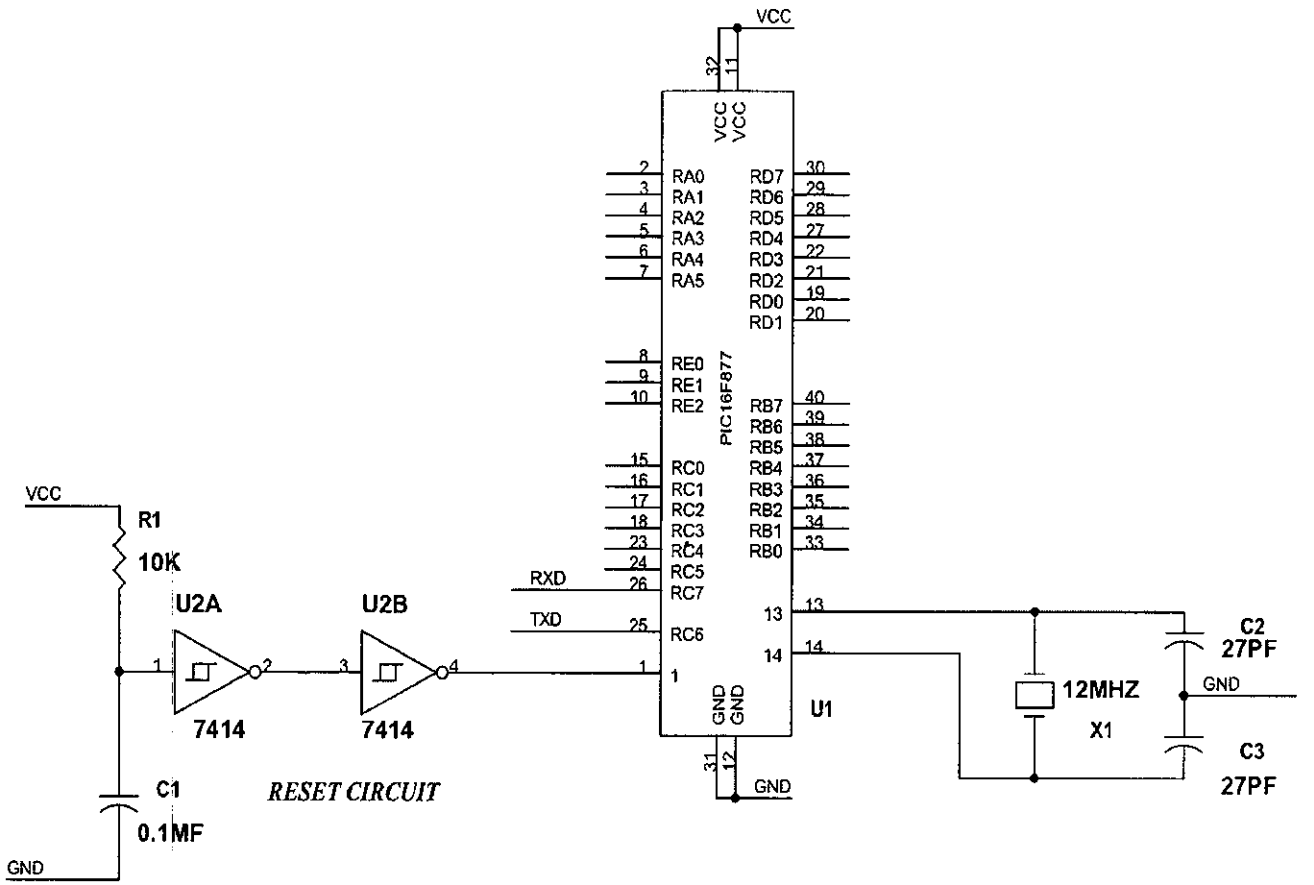
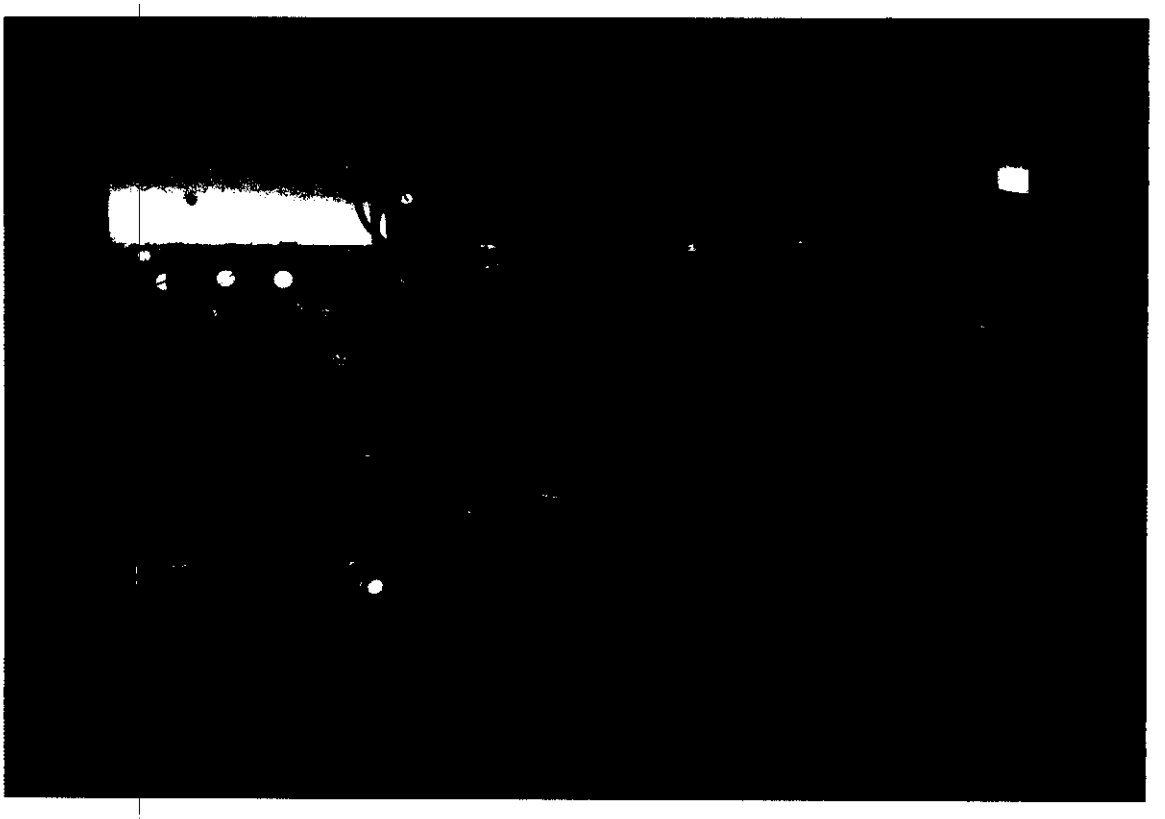
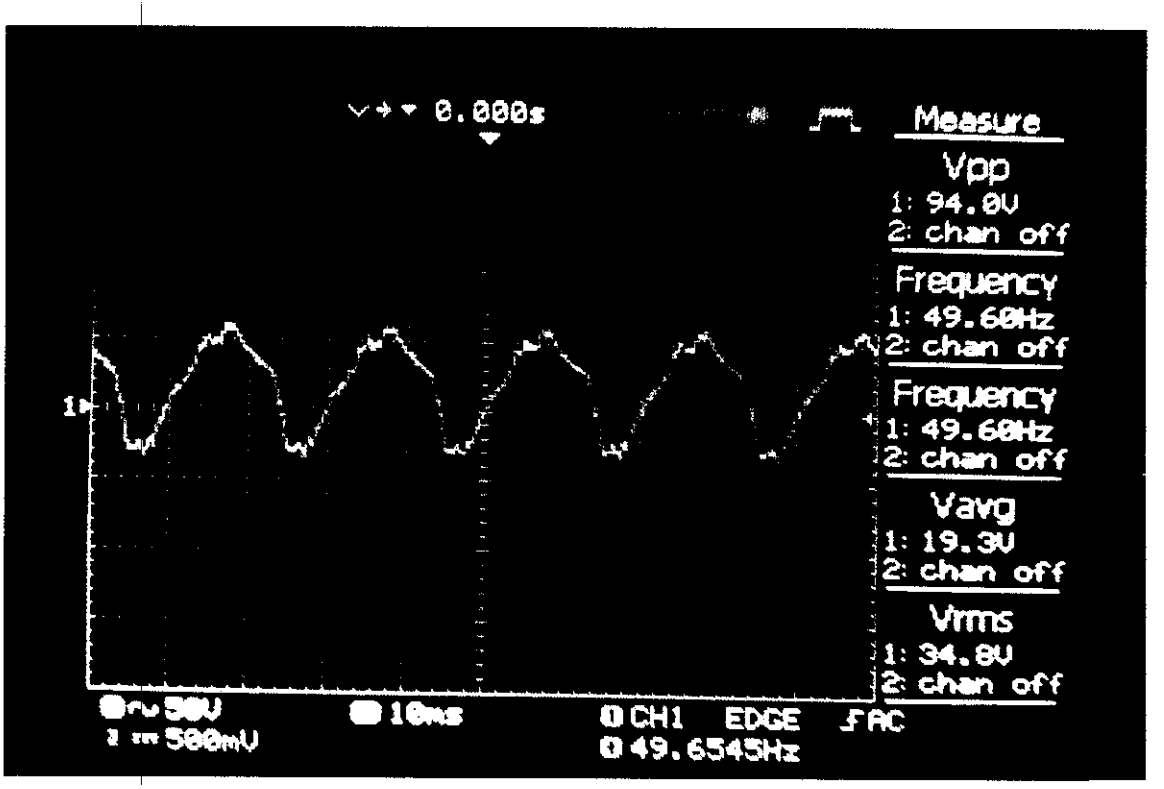


Fig 5.6 Pic Controller Circuit

5.6 EXPERIMENTAL SETUP



5.7 HARDWARE OUTPUT:



CHAPTER 6

CHAPTER 6

CONCLUSION AND SCOPE FOR FUTURE DEVELOPMENT

CONCLUSION:

- Switching sequence of the proposed SVM is composed of the upper active vectors, the lower active vectors and the zero vectors. The upper and lower active vectors are determined.

- For the impedance source inverter SVM algorithm is developed to reduce the number of switching and number of semiconductor switches.

- The performance of the proposed SVM was verified using computer simulation and it was validated using experimental data.

SCOPE FOR FUTURE IMPROVEMENT:

- Further in future an SVM algorithm for reduced total harmonic distortion can be implemented.

REFERENCE

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- C. Liu, B. Wu, N. Zargari, and D. Xu, "A novel three-phase three-leg AC/AC converter using nine IGBTs," IEEE Trans. Power Electron.,vol. 24, no. 5, pp. 1151–1160, May 2009.

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- K. Oka, Y. Nozawa, R. Omata, K. Suzuki, A. Furuya, and K. Matsuse, "Characteristic comparison between five-leg inverter and nine-switch inverter," in Proc. Power Convers. Conf., Nagoya, 2007, pp. 279–283.

- F. Z. Peng, "Z-source inverter," IEEE Trans. Ind. Appl., vol. 39, no. 2,pp. 504–510, Mar./Apr. 2003

APPENDIX

APPENDIX

16F877A PIC MICROCONTROLLER CODING AND DETAILS

Code:

```
#include<pic.h>                    //PIC16F Header File Declaration
#include<stdio.h>                  //Embedded C Header File Decleration
#include "delay.c"                 //Subroutine Declaration
__CONFIG(0x3f71);                  //IC Initialization
void main()                              //Main Program
{
      RBPU=0;
      TRISB=0XFF;
      TRISC=0x00;
      PORTC=0;
      PORTB=0xFF;
      while(1)                     // Continuous Operation
      {
            PORTC=0x11;            //Generate first part signal    1
            DelayMs(2);            //Call Delay
            DelayUs(500);
            PORTC=0x12;            //Generate second Part Signal 2
            DelayMs(2);            //Call Delay
            DelayUs(500);
            PORTC=0x06;            //Generate third part signal    3
            DelayMs(2);            //Call Delay
            DelayUs(500);
            PORTC=0x09;            //Generate fourth part signal   4
            DelayMs(2);            //Call Delay
            DelayUs(500);
```

```
                PORTC=0x0C;                 //Generate fifth part signal    5
                DelayMs(2);                 //Call Delay
                DelayUs(500);
                PORTC=0x1C;                 //Generate sixth part signal    6
                DelayMs(2);                 //Call Delay
                DelayUs(500);
                PORTC=0x01;                 //Generate seventh part signal 7
                DelayMs(2);                 //Call Delay
                DelayUs(500);
                PORTC=0x0C;                 //Generate eighth part signal   8
                DelayMs(2);                 //Call Delay
                DelayUs(500);
                PORTC=0x1C;                 //Generate ninth part signal    9
                DelayMs(2);                 //Call Delay
                DelayUs(500);
                }
}
```

APPENDIX B

PIC MICROCONTROLLER

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complementary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

PIN DIAGRAM OF PIC 16F877

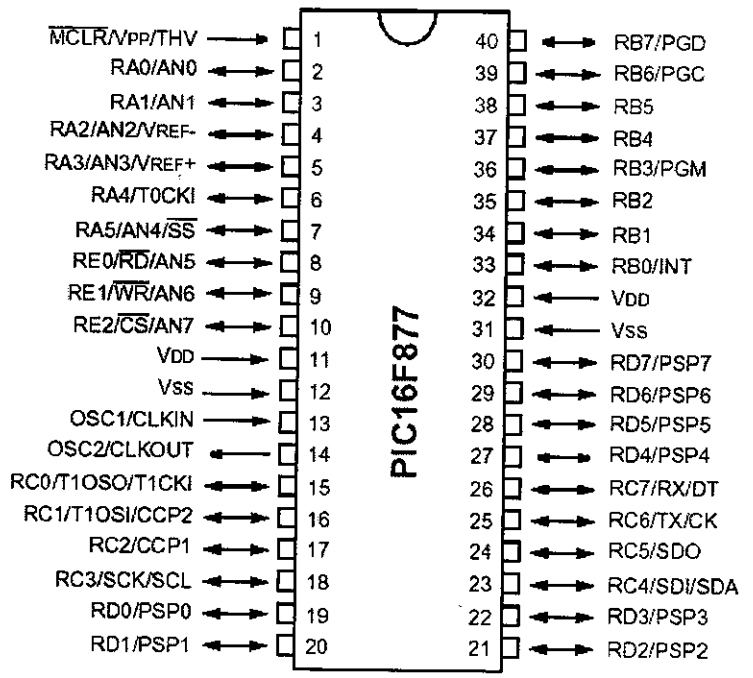


TABLE SPECIFICATIONS

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

PERIPHERAL FEATURES:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep

  Via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules

  Capture is 16-bit, max resolution is 12.5 ns,

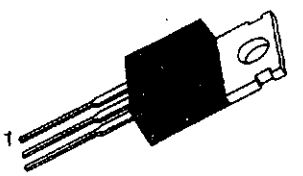
  Compare is 16-bit, max resolution is 200 ns,

  PWM max. Resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9- Bit addresses detection.
- Brown-out detection circuitry for Brown-out Reset (BOR).

FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF840	500V	0.85Ω	8.0A
IRF841	450V	0.85Ω	8.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRF840	IRF841	Unit
Drain-Source Voltage (1)	V_{DSS}	500	450	Vdc
Drain-Gate Voltage (R_{GS}=1.0MΩ)(1)	V_{DGR}	500	450	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Continuous Drain Current Tc=25 °C	I_D	8.0		Adc
Continuous Drain Current Tc=100 °C	I_D	5.0		Adc
Drain Current - Pulsed (3)	I_{DM}	32		Adc
Gate Current - Pulsed	I_{GM}	±1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	510		mJ
Avalanche Current	I_{AS}	8.0		A
Total Power Dissipation @ Tc=25 °C Derate above 25 °C	P_D	125 1.0		Watts W/ °C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150		°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		°C

Notes : (1) T_J=25°C to 150°C
(2) Pulse test : Pulse width ≤ 300μs, Duty Cycle ≤ 2%
(3) Repetitive rating : Pulse width limited by max. junction temperature
(4) L=1.4mH, V_{DD}=50V, R_G=25Ω , Starting T_J=25°C

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise specified)

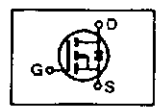
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF840 IRF841	 500 450	 - -	 - -	 V V	V_{GS}=0V, I_D=250μA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	V_{DS}=V_{GS}, I_D=250μA
I_{GSS}	Gate-Source Leakage Forward	-	-	100	nA	V_{GS}=20V
I_{GSS}	Gate-Source Leakage Reverse	-	-	-100	nA	V_{GS}=-20V
I_{DSS}	Zero Gate Voltage Drain Current	-	-	250	μA	V_{DS}=Max. Rating, V_{GS}=0V
		-	-	1000	μA	V_{DS}=0.8 Max. Rating, V_{GS}=0V, Tc=125°C
$R_{DS(on)}$	Static Drain-Source On Resistance (2)	-	-	0.85	Ω	V_{GS}=10V, I_D=4.0A
g_{fs}	Forward Transconductance (2)	4.0	6.5	-	℧	V_{DS}≥10V, I_D=4.0A
C_{iss}	Input Capacitance	-	1510	-	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{oss}	Output Capacitance	-	154	-	pF	
C_{rss}	Reverse Transfer Capacitance	-	66	-	pF	
$t_{d(on)}$	Turn-On Delay Time	-	14	21	ns	V_{DD}=0.5 BV_{DSS}, I_D=8.0A, Z_o=9.1Ω (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	-	23	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	-	49	74	ns	
t_f	Fall Time	-	20	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	-	-	74	nC	V_{GS}=10V, I_D=8.0A, V_{DS}=0.8 Max. Rating (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	-	9.0	-	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	-	27.0	-	nC	

THERMAL RESISTANCE

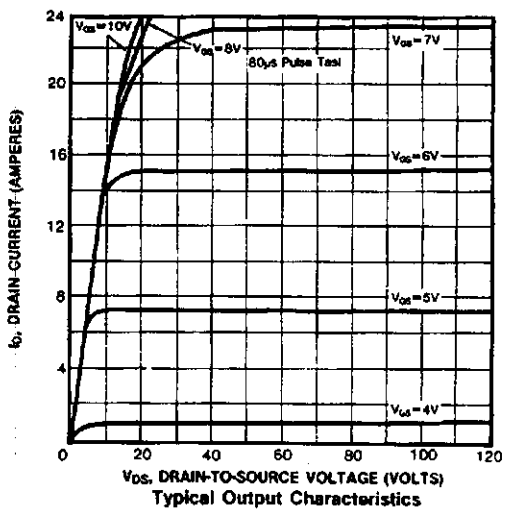
Symbol	Characteristics		All	Units	Remark
R_{thJC}	Junction-to-Case	MAX	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	62.5	K/W	Free Air Operation

Notes : (1) TJ=25°C to 150°C
(2) Pulse test : Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating : Pulse width limited by max. junction temperature

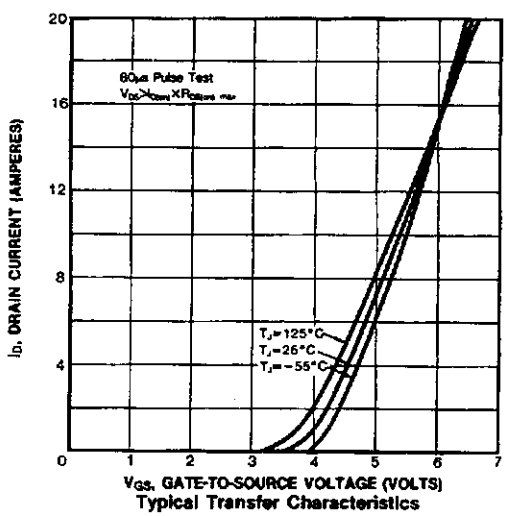
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	-	-	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	-	-	32	A	
V_{SD}	Diode Forward Voltage (2)	-	-	2.0	V	T_J=25°C, I_S=8.0A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	-	460	970	ns	T_J=25°C, I_F=8.0A, dI_F/dt=100A/μS

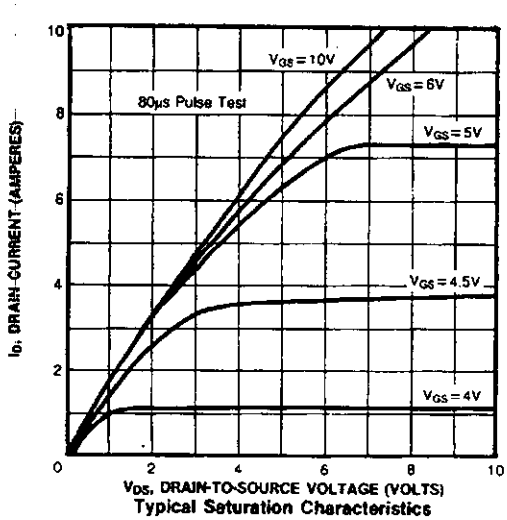
Notes : (1) T_J=25°C to 150°C
(2) Pulse test : Pulse width ≤ 300μs, Duty Cycle ≤ 2%
(3) Repetitive rating : Pulse width limited by max. junction temperature



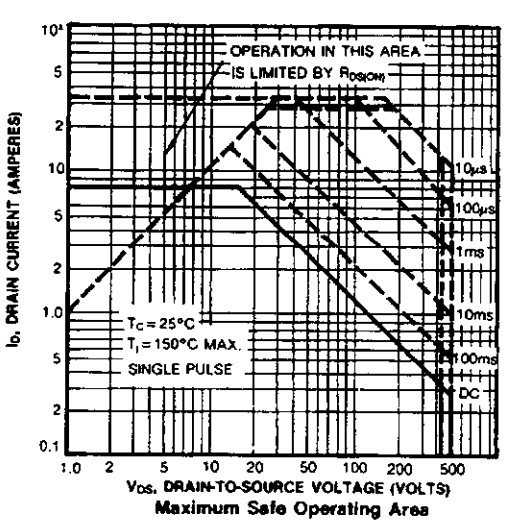
Typical Output Characteristics



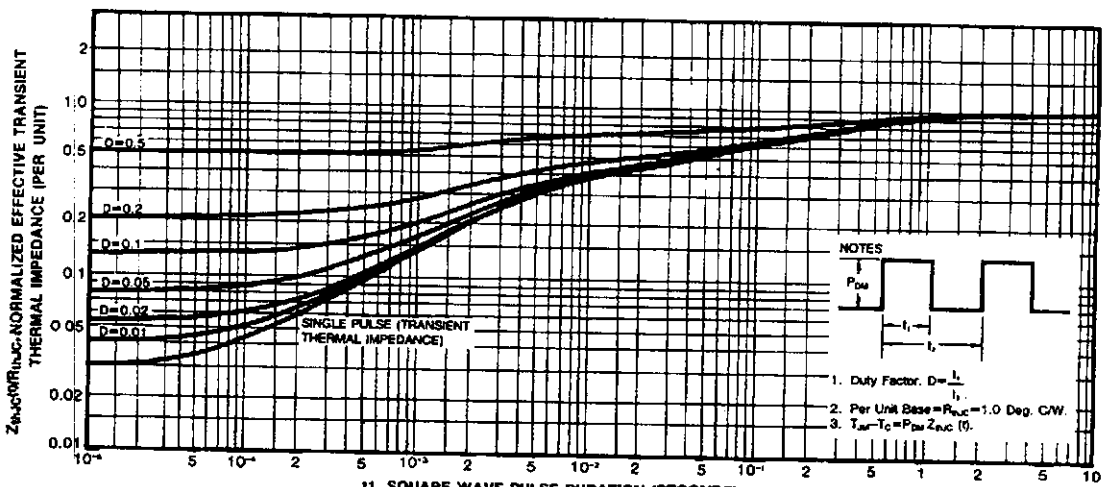
Typical Transfer Characteristics



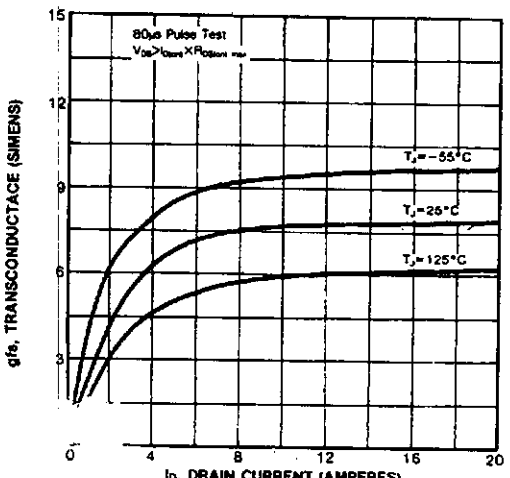
Typical Saturation Characteristics



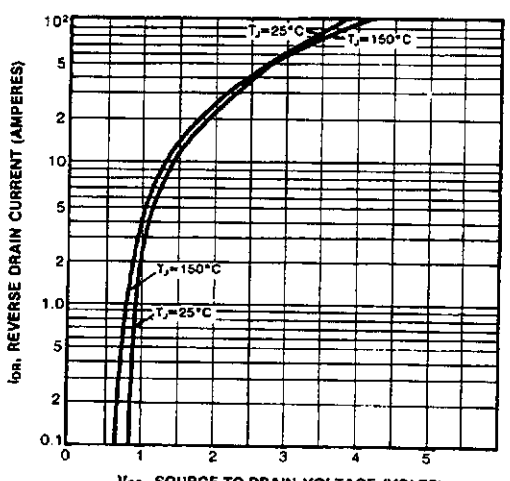
Maximum Safe Operating Area



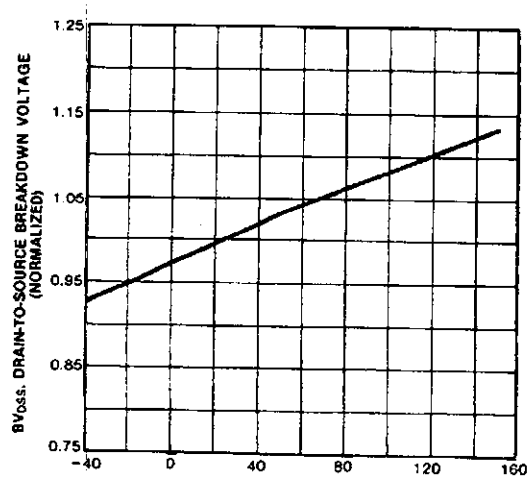
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



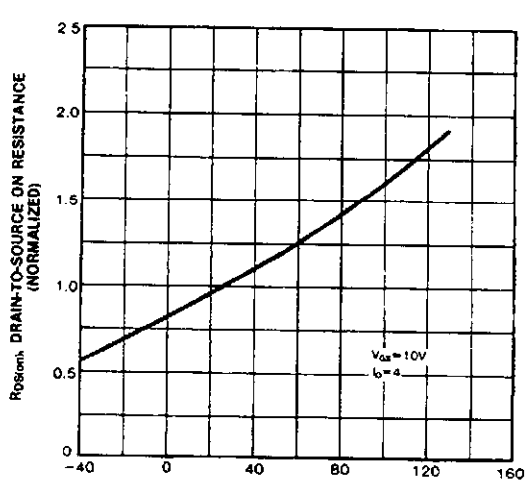
Typical Transcounductance Vs. Drain Current



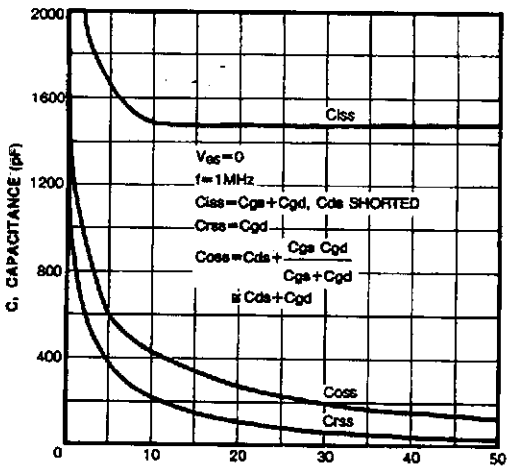
Typical Source—Drain Diode Forward Voltage



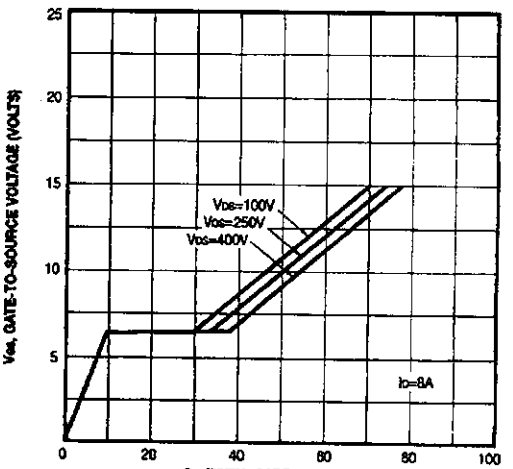
Breakdown Voltage Vs. Temperature



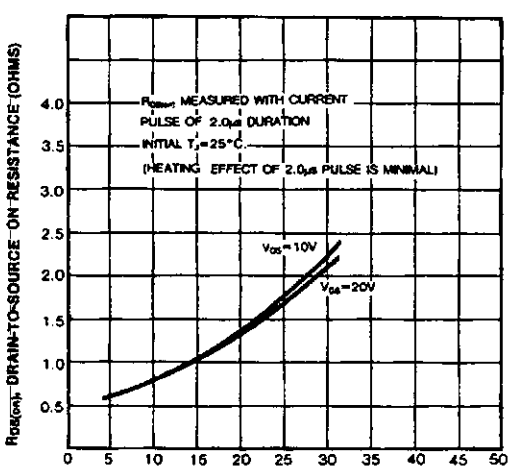
Normalized On-Resistance Vs. Temperature



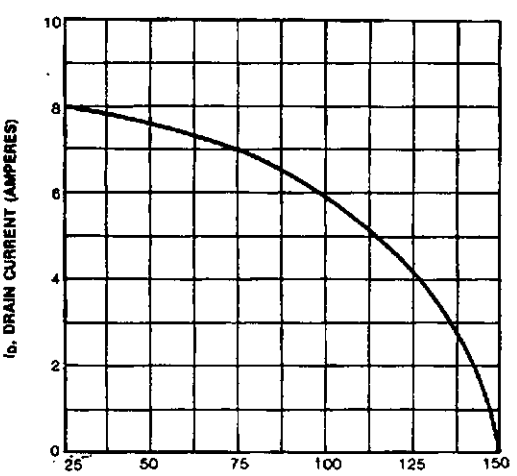
Typical Capacitance Vs. Drain to Source Voltage



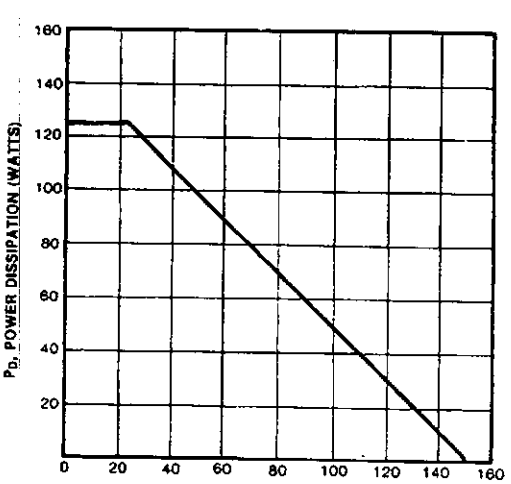
Typical Gate Charge Vs. Gate-to-Source Voltage



Typical On-Resistance Vs. Drain Current



Maximum Drain Current Vs. Case Temperature



Power Vs. Temperature Derating Curve