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"IMPLEMENTATION OF ZSI BASED POWER CONVERTER FOR WIND ENERGY CONVERSION SYSTEM"

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

Certified that this project report entitled **"IMPLEMENTATION OF ZSI BASED POWER CONVERTER FOR WIND ENERGY CONVERSION SYSTEM"** is the bonafide work of

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ABSTRACT

This project presents an impedance source power inverter and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. The Z-Source Inverter employs a unique impedance network to couple the inverter main circuit to the power source, thus providing unique features that cannot be obtained in the traditional Voltage-Source and Current-Source Inverters where a capacitor and inductor are used, respectively. The ZSI overcomes the conceptual and theoretical barriers and limitations of the traditional VSI and CSI and provides a novel power conversion concept. The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. Simulation and experimental results have been presented to demonstrate the new features.

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NO.	SYMBOLS		ABBREVATIONS
1.	ZSI	-	Impedance Source Inverter
2.	MC	-	Micro Controller
3.	MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
4.	PWM	-	Pulse Width Modulation
5.	DC	-	Direct Current
6.	AC	-	Alternating Current
7.	VSI	-	Voltage Source Inverter
8.	CSI	-	Current Source Inverter
9.	GTO	-	Gate Turn Off
10.	SCR	-	Silicon Controlled Rectifier
11.	EMI	-	Electro Magnetic Interference
12.	IPM	-	Intelligent Power Modules
13.	BB	-	Buck Boost Factor
14.	M	-	Modulation Index
15.	B	-	Boost Factor
16.	TTL	-	Transistor Transistor Logic

CHAPTER 1

1.1 INTRODUCTION:

The unpredicted development in industrial growth has increased the need for electricity day by day. To meet the power demand we are going for non-conventional energy resources. The proposed design is an efficient energy generation system using impedance source inverter(ZSI).

The wind sources are not constant hence we are applying the impedance source concept and the voltage is boost/buck based on the available source of input. The source can be buck/boost depending on wind velocity and given to the impedance source inverter and inject the generated voltage to the grid. Hence the power demand can be reduce by this concept.

Now a day's microcontroller(MC) based control in power convertes has become the intensive area of research due to its features of simple circuitry, software control and flexibility to adapt various applications. However, PWM generation and current control loop requires high sampling rate to achieve wide bandwidth performance. Therefore, most computational resources of the controller must be utilized for PWM gating signal generation and the execution of current control loop algorithms.

1.2 NEED FOR THE PROJECT:

Due to the development of more and more industries and human sophistication, the power demands are increasingly high. But the fossil fuel quantity are reducing day by day. The available conventional sources may be sufficient for another 100 years only. Hence we are moving to non-conventional sources and impedance source technique to stabilize the constant output supply to grid.

This can be achieved with help of impedance source inverter (ZSI) by available power switches like IGBT, MOSFET. The energy that a switching power converter delivers to a grid is controlled by Pulse Width Modulated (PWM) signals applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. When a PWM signal is applied to the gate of a power transistor, it causes the output voltage of the inverter to vary according to its turn on time. The inverter converts DC power to AC power at the required frequency and amplitude. The inverter consists of six power MOSFETs that turn on and off in a desired pattern to produce single phase AC output voltage. The control IC is programmed and implemented in Microcontroller to generate PWM gating pulses for the MOSFETs.

In this project we develop a embedded controller for inverter using microcontroller. The output voltage of the inverter is varied by varying the PWM switching frequency of the gating pulses given to the power transistors (MOSFETs) of the inverter. The PWM switching frequency can be varied to a maximum of 10KHz. High switching frequency is achieved which improves the performance by reducing total harmonics distortion and switching loss.

1.3 OBJECTIVE:

The main objective of this project is to design and develop an impedance source inverter(ZSI) to maintain constant output supply to grid. The project presents methodology to integrate wind energy with grid source by ZSI and also aims at supplementing the grid power to rural areas.

1.4 ORGANIZATION OF THE REPORT:

Chapter 1: Introduction to the project stating the need for this approach, objective and methodology

Chapter 2: PWM Inverter – Gives a brief idea about the types of inverter, their operation, Different types of PWM technique, applications and advantages. In this the impedance source inverters are being explained.

Chapter 3: Design of Impedance source inverter.(ZSI).

Chapter 4: Gives the details about simulation of MATLAB model and their results.

Chapter 5: Hardware description provides details about opto coupler, buffer, driver circuit.

Chapter 6: Microcontroller – Describes about PIC 16F877 design flow and applications. Details the architecture and features of the microcontroller used

Chapter 7: Conclusion – The project done and the scope for future work are discussed.

Appendices: Gives the features and the specification of the ICs and the PIC microcontroller Used.

1.5 METHODOLOGY:

1. Design of impedance source inverter module by Embedded -C.
2. The simulation is carried out using MPLAB software.
3. The Implementation is carried out using 8 bit micro controller.
4. The total hardware consists of impedance network, rectifier, inverter power module, driver, opto isolator, buffer and embedded controller.

CHAPTER 2

BASIC CONSIDERATION IN DESIGN:

2.1 INTRODUCTION:

The Z-Source Inverter (ZSI) system employs a unique LC network in the dc link and a small capacitor on the ac side of the diode front end. By controlling the Shoot-Through duty cycle, the Z-source can produce any desired output ac voltage, even greater than the line voltage. As a result, the new ZSI system provides ride-through capability during voltage sags, reduce line harmonics, improves power factor and reliability, and extends output voltage range.

2.1.1 LITERATURE SURVEY:

The following are the papers which we have referred:

From this paper "Z-Source Inverter", the Z-source concept can be applied to all dc-to-ac, ac-to-dc, dc-to-dc & ac-to-ac power conversion is referred. The operating states of impedance network and the guidelines to design the impedance network has been referred from "Designing Impedance network of Z-Source Inverters". The voltage boosting capability of ZSI is referred from "Z-Source Inverter for Motor Drives". A simple pulse width modulation of ZSI is referred from "Constant Boost Control of the Z-Source Inverter to Minimize Current Ripple and Voltage Stress". From the paper "Maximum boost control of the ZSI", the control technique for triggering circuit has been referred.

2.2 TRADITIONAL INVERTERS:

2.2.1 INVERTER:

An inverter is an electronic circuit for converting direct current (DC) to alternating current (AC). Inverters are used in a wide range of applications, from small switched power supplies for a computer to large electric utility applications to transport bulk power.

Traditionally, power inverters can be broadly classified as either the Voltage Source Inverter (VSI) or Current Source Inverter (CSI) type. For a VSI the inverter is fed from a dc voltage source usually with a relatively large capacitor connected in parallel. It is well known that the maximum ac voltage output of a VSI is limited to 1.15 times half the dc source voltage (using modulation strategies with triplen offsets added) before being over-modulated. The VSI can therefore only be used for buck (step-down) dc-ac power conversion or boost (step-up) ac-ac power rectification assuming that no additional dc-dc inverter is used to buck/boost the dc link voltage. On the other hand, a CSI is fed from a dc current source, which is usually implemented by connecting a dc source in series with a relatively large inductor and its ac voltage output is always greater than the dc source voltage that feeds the dc-side inductor. The CSI is therefore only suitable for boost dc-ac power conversion or buck ac-dc power rectification.

2.2.2 VOLTAGE SOURCE INVERTER:

Fig. 2.1 shows the traditional three-phase VSI structure. A dc voltage source supported by a relatively large capacitor feeds the main inverter circuit, a three-phase bridge. The dc voltage-source can be a battery, fuel-cell stack, diode rectifier and/or capacitor. Six switches are used in the main circuit; each is traditionally composed of a power transistor and an anti-parallel (or freewheeling) diode to provide bidirectional current flow and unidirectional voltages blocking capability.

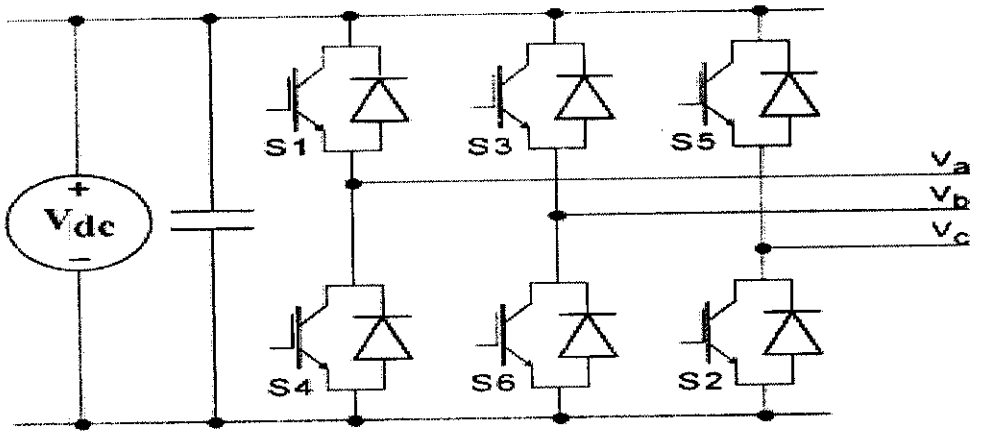

Fig. 2.1 Traditional Voltage Source Inverter

2.2.3 CURRENT SOURCE INVERTER:

Fig. 2.2 shows the traditional three-phase CSI structure. A dc current source feeds the main inverter circuit, a three-phase bridge. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel cell stack, diode rectifier, or thyristor inverter. Six switches are used in the main circuit, each is traditionally composed of a semiconductor switching device with reverse blocking capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking.

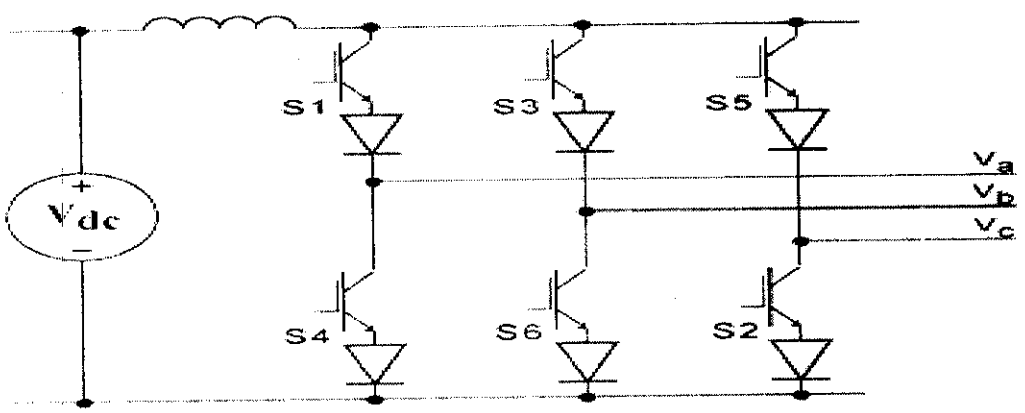

Fig. 2.2 Traditional Current Source Inverter

2.2.4 DRAWBACKS:

The VSI has the following conceptual and theoretical barriers and limitations.

1. The ac output voltage is limited below and cannot exceed the dc-rail voltage or the dc-rail voltage has to be greater than the ac input voltage. Therefore, the VSI is a buck (step-down) inverter for dc-to-ac power conversion and the VSI is a boost (step-up) rectifier (or boost converter) for ac-to-dc power conversion. For applications where over drive is desirable and the available dc voltage is limited , an additional dc-dc boost inverter is needed to obtain a desired ac output. The additional power inverter stage increases system cost and lowers efficiency.
2. The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a Shoot-Through would occur and destroy the devices. The shoot-Through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the converter's reliability. Dead time to block both upper and lower devices has to be provided in the VSI, which causes waveform distortion.
3. An output LC filter is needed for providing a sinusoidal voltage compared with the CSI, which causes additional power loss and control complexity.

The CSI has the following conceptual and theoretical barriers and limitations,

1. The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. Therefore the CSI is a boost inverter for dc-dc power conversion and the CSI is a buck rectifier for ac-ac power conversion. For applications where a over drive is desirable, an additional dc-dc buck (or boost) converter is needed. The additional power conversion stage increases system cost and lowers efficiency.
2. Atleast one of the upper devices and one of the lower devices have to be gated on and maintained on any time. Otherwise, an open circuit of the dc inductor would

occur and destroy the devices. The open circuit problem by EMI noise's mis gating is a major concern of the inverter's reliability.

3. Overlap time for safe current communication is needed in the CSI, which also causes waveform distortion.

4. The main switches of the CSI have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high-performance IGBT modules and intelligent power modules (IPMs).

In addition both the VSI and the CSI have the following common problems,

1. They are either a boost or a buck converter and cannot be a buck-boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage.

2. Their main circuits cannot be interchangeable. In other words, neither the VSI main circuit can be used for the CSI nor vice versa.

3. They are vulnerable to EMI noise in terms of reliability.

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2.3 IMPEDANCE SOURCE INVERTER:

To overcome the above problems of the traditional VSI and CSI, an impedance-source (or impedance-fed) power inverter and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion is proposed. Fig. 2.3 shows the general ZSI structure proposed. It employs a unique impedance network to couple the inverter main circuit to the power source, load, or another inverter, for providing unique features that cannot be observed in the traditional VSI and CSI where a capacitor and inductor are used, respectively.

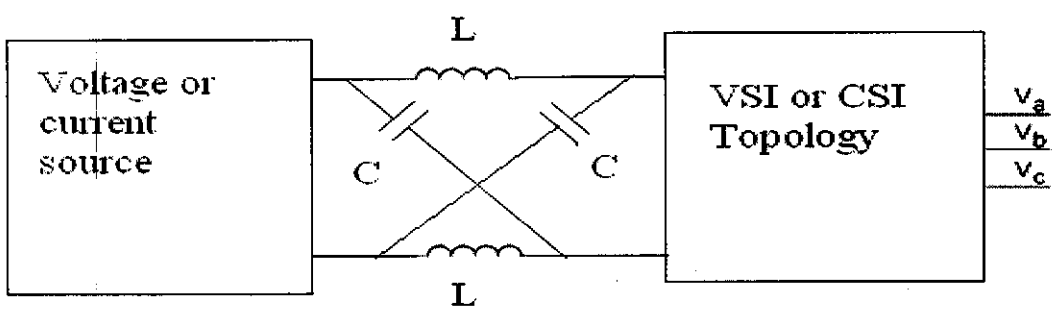


Fig. 2.3 Z-Source Inverter

2.3.1 ADVANTAGES:

The ZSI overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional VSI and CSI provides a novel power conversion concept.

Table 2.1 Comparison of ZSI with Traditional Inverters

Current Source Inverter(CSI)	Voltage Source Inverter (VSI)	Impedance Source Inverter(ZSI)
1. As inductor is used in the dc link, the source impedance is high. .A constant current	As capacitor is used in the dc link, it acts as a low impedance voltage source.	As capacitor and inductor are used in the dc link, it acts as a constant high impedance

source is realized.		voltage source.
2. A current source inverter is capable of withstanding short circuit across any two of its output terminals. Hence momentary short circuit on load and mis-firing of switches are acceptable.	A VSI leads to dangerous situation as the parallel capacitor could feed more power into the fault.	In ZSI mis-firing of the switches may be acceptable.
3. Used in buck or boost operation of the inverter.	Used in a buck mode of operation of inverter.	Used in both buck and boost operating modes of Inverter.
4. Affected by the EMI noise.	Affected by the EMI noise	Less affected by the EMI noise. ImpedanceSource act as a filter
5.Considerable amount of harmonic distortion	Considerable amount of harmonic distortion	Harmonics distortion is low
6.Low efficiency because of power loss	Low efficiency because of high power loss	Higher efficiency because of low power loss

2.3.2 Z-SOURCE NETWORK:

ZSI appears to be gaining popularity over the others mainly because it continues to employ a conventional VSI as the power inverter yet with a modified dc link. As illustrated in the Fig. 1.4 a diode (D_s) and an impedance network connected between the variable dc voltage source and the conventional VSI are the main differences in the power circuit. As seen in the figure, a symmetrical impedance network consists of two identical inductors and two identical capacitors connected in a specific manner to achieve the desired properties. The impedance network changes the circuit configuration from that of a voltage source to an impedance source.It allows the VSI to be operated in a new state called the Shoot-Through state in which the two switching devices in the same leg are simultaneously switched-on to effect a short-circuit of the dc link. During this state, energy is transferred from the capacitors to inductors, thereby giving rise to the voltage

boost capability of the ZSI. As the capacitors may be charged to higher voltages than the input source voltage, the diode D_s is necessary to prevent discharging of them through the input source.

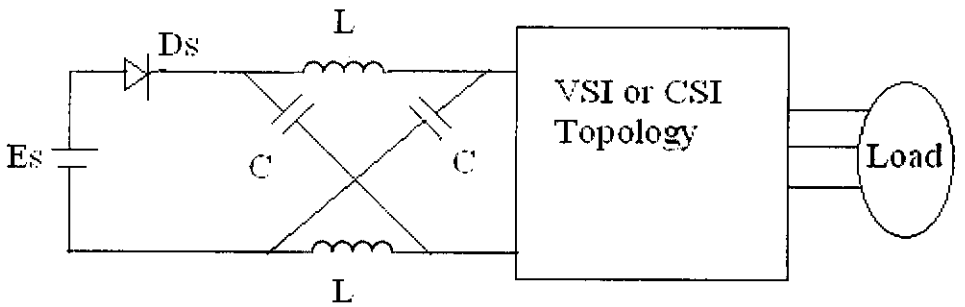


Fig.2.4 ZSI based on a conventional VSI

2.3.3 OPERATING STATES OF THE IMPEDANCE NETWORK:

The operating states of the impedance network at the dc link is decided by the switching states of the semiconductor devices on its input and output terminals. As illustrated in Fig.2.5, the diode D_s on its input side has two switching states as 'On' and ' Off ' and the VSI on its output side has three switching states as 1, 2& 3.

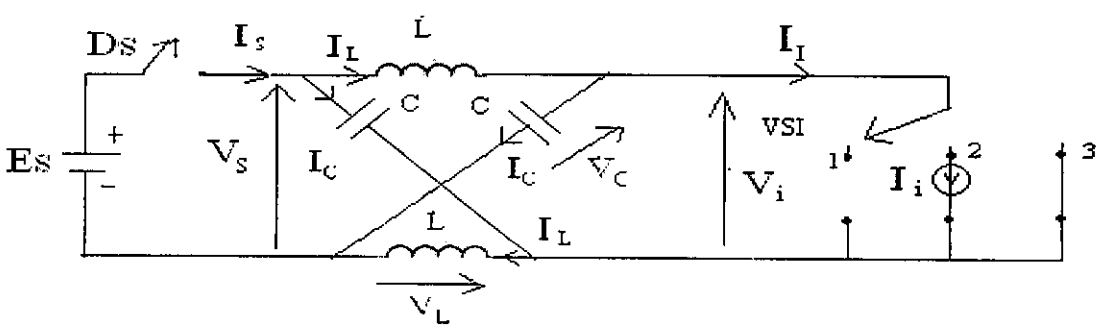


Fig.2.5 Switching equivalent of Z source Inverter

Thus, in general, the impedance network of the ZSI at a given time can operate in any one of the six possible states given in Table 2.2.

Table 2.2 Possible operating states of the Impedance Network

VSI Input State	Open		Active		Shoot-Through	
Diode Ds	On	Off	On	Off	On	Off
State of Impedance Network	Open-1	Open-2	Active-1	Active-2	Shoot-Through-1	Shoot-Through-2

A switching cycle of the ZSI may consist of any number of states ranging from two to six. However, as will be seen later in the following sections, the Open-1, Active-1, Shoot-Through-1 states are the desired states in practical applications. The three states, Open-2, Active-2, Shoot-Through-2 are undesirable and are to be avoided by proper sizing of the inductors and capacitors of the impedance network.The impedance network in general can be written as,

$$V_l = L\left(\frac{dI_l}{dt}\right); \qquad I_c = C\left(\frac{dV_c}{dt}\right)$$

$$V_s = V_c + V_l, \qquad I_s = I_c + I_l \tag{2.1}$$

$$V_i = V_c - V_l, \qquad I_i = I_l - I_c \tag{2.2}$$

A. Open -1 state:

Fig.2.6 illustrates the equivalent circuit of the ZSI during Open-1 state.

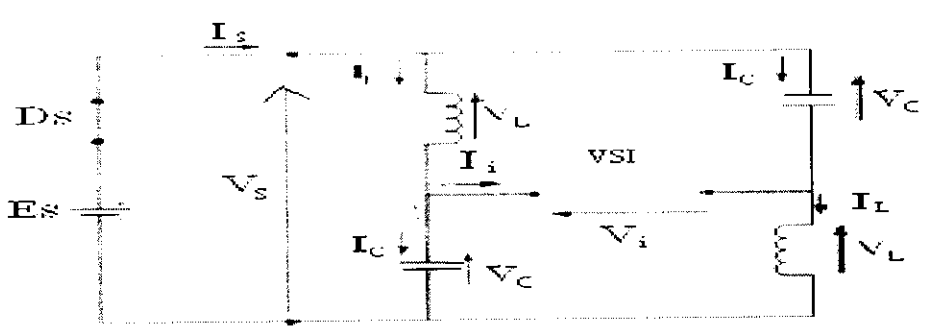


Fig. 2.6 Equivalent circuit of ZSI during Open-1 state

The equations that define the open-1 state are given by,

$$V_s=E_s; \quad I_i=0; \tag{2.3}$$

The inductor voltage and output voltage in this state are given by,

$$V_l = E_s-V_c; \quad V_i = 2V_c-E_s; \tag{2.4}$$

B. Open-2 state:

In the Open-2 state, the diode remains in the Off states and the VSI in the Open state. Therefore, the state defining equations can be written as,

$$I_s=0; \quad I_i=0;$$

In order to avoid this state, the necessary condition for the minimum value of inductor current (I_{lomin}) can be seen as,

$$I_{lomin}>0.$$

C. Active-1 state:

As seen in the equivalent circuit given in the Fig.2.7, the only difference between Open-1 state is the presence of the constant current source Io across the input terminals of the VSI.

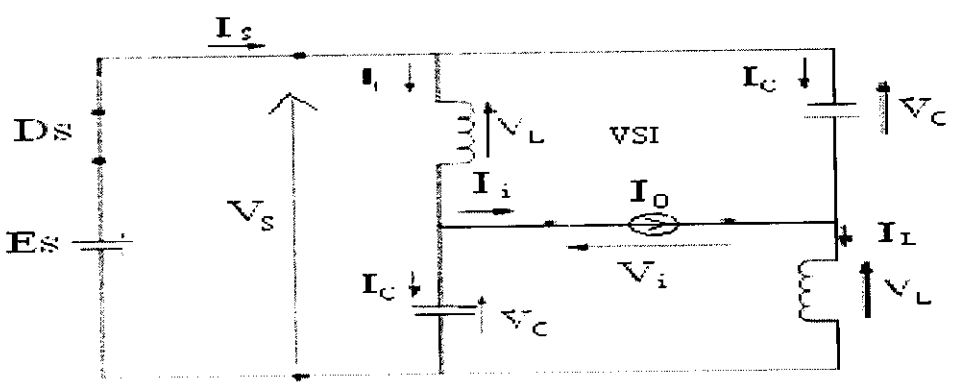


Fig.2.7 Equivalent circuit of ZSI during Active-1 state.

The state defining equations for Active-1 state are,

$$V_s = E_s; \quad I_i = I_o \tag{2.5}$$

It can be seen that the current through the diode, Is, will be zero and the diode will turn off when,

$$I_l = -I_c = \frac{I_o}{2} \tag{2.6}$$

This marks the end of Active-1 state and the beginning of Active-2 state.

D. Active-2 state:

The state defining equations for Active-2 state are

$$I_i = I_o; \quad I_s = 0 \tag{2.7}$$

Substituting (1.7) in (1.1) and (1.2), it can be seen that the currents remain constant at $I_l = -I_c = \frac{I_o}{2}$ and the capacitor discharges linearly with time at the rate of $\frac{I_o}{2C}$

In order to avoid Active-2 state in appearing during operation, the necessary condition for minimum inductor current in Active-1 period (I_{lAmin}) is

$$I_{lAmin} > \frac{I_o}{2} \tag{2.8}$$

E. Shoot-Through-1 state:

As seen from Fig. 1.8, the state defining equations for Shoot-Through-1 state are,

$$I_s = 0; \quad V_i = 0 \tag{2.9}$$

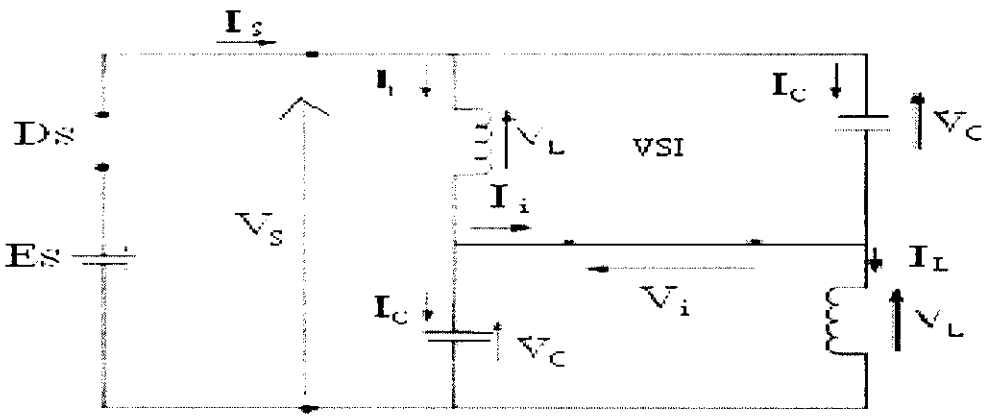


Fig. 2.8 Equivalent circuit of ZSI during Shoot-Through-1 state

The energy stored in the capacitors during Open and Active state is transferred to inductors during Shoot-Through-1 state, thereby allowing the boosting of the voltage applied to the VSI.

F. Shoot-Through-2 state:

The defining equations of Shoot-Through-2 state can be written as,

$$V_s=E_s; \qquad V_i=0 \tag{2.10}$$

In order to prevent appearing of Shoot-Through-2 state during operation the necessary condition for minimum capacitor voltage (V_{cmin}) is

$$V_{cmin}>\frac{E_s}{2} \tag{2.11}$$

From the preceding discussion it is clear that the Open-2, Active-2, Shoot-Through-2 states do not contribute to the power conversion process and should be avoided. Thus they are named as 'static states' .Practical inverters are operated only in two or three of the Open-1, Active-1, Shoot-Through-1 states. They are hereby named as 'dynamic states'. Since the three static states appear only when the capacitor voltage and inductor current fluctuate in a wide leading to the violation of conditions given in the Open-2, Active-2, Shoot-Through-2 states, it is necessary to limit the ripples of the

related voltage and current by increasing the sizes of the inductors and capacitors appropriately.

2.3.4 SHOOT-THROUGH TIME PERIOD, BOOST FACTOR,MODULATION INDEX :

a) SHOOT-THROUGH TIME PERIOD:

Shoot-Through time period is defined as the duration at which the two switches of the same-phase leg are gated on at the same time.

b) BOOST FACTOR:

$$V_i = \frac{T}{T_1 - T_0} V_s \qquad (2.12)$$

Where,

T0 is the Shoot-Through time period in seconds

T1 is the non Shoot-Through time period or Active state of ZSI

T is the Total time period in sec

V_s is the input source voltage

$V_i = B\ V_o$

Where B is the Boost factor resulting from the Shoot-Through zero state.

c) MODULATION INDEX:

On the other side the output peak phase voltage from the inverter can be expressed as,

$$V_{ac} = \frac{M.V_i}{2} \qquad (2.13)$$

Where ,

M is the Modulation Index.

V_{ac} is the output line voltage of ZSI.

Using equations (1.12) , (1.13) can be further expressed as ,

$$V_{ac} = \frac{M.B.V_o}{2} \qquad (2.14)$$

$$V_{ac} = \frac{B_b.V_o}{2} \qquad (2.15)$$

Where, B_b is the buck boost factor.

2.4 PULSE WIDTH MODULATION:

2.4.1 INTRODUCTION:

Pulse Width Modulation, abbreviated as PWM, is a modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal. It is a method of transmitting information on a series of pulses. The data that is being transmitted is encoded on the width of these pulses to control the amount of power being sent to a load.

In other words, pulse width modulation is a modulation technique for generating variable width pulses to represent the amplitude of an input analog signal or wave. Using digital pulses we can create some analog value other than just 'high' and 'low' signal levels. Many digital systems are powered by a 5-Volt power supply, so by filtering a signal that has a 50% duty cycle we get an average voltage of 2.5 Volts. Other duty cycles produce any voltage in the range of 0 to 100% of the 'high' voltage, depending upon the PWM resolution. The duty cycle is defined as the percentage of digital 'high' to digital 'low' signals present during a PWM period. The PWM resolution is defined as the maximum number of pulses that can pack into a PWM period. The PWM period is an arbitrarily time period in which PWM takes place. It is chosen to give best results for our particular use. The figure 3.8 shows the PWM pulse generated by comparing the sawtooth carrier and a reference signal.

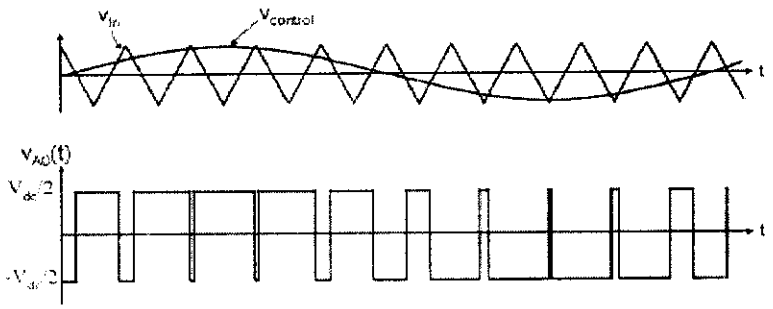


Fig 2.9 Pulse Width Modulation

2.4.2 TYPES OF PULSE WIDTH MODULATION:

There are many ways of generating a PWM output such as

- Single pulse width modulation
- Multiple pulse width modulation
- Sinusoidal pulse width modulation
- Space vector pulse width modulation
- Modified pulse width modulation

MULTIPLE PWM:

The harmonic content can be reduced by using several pulses in each half-cycle of the output voltage. It is generated by comparing a linear reference signal with a triangular carrier wave. The frequency of reference signal sets the output frequency and the frequency of the carrier determines the number of pulses per half cycle. By varying the on time of the pulses the output voltage can be controlled. This is also known as UNIFORM pulse width modulation.

SINUSOIDAL PWM:

The simplest analog form of generating fixed frequency PWM is by comparison with a linear slope waveform such as a sawtooth. As seen in Fig 3.9 the output signal

goes high when the sine wave is higher than the sawtooth. This is implemented using a comparator whose output voltage goes to logic HIGH when the input is greater than the other.

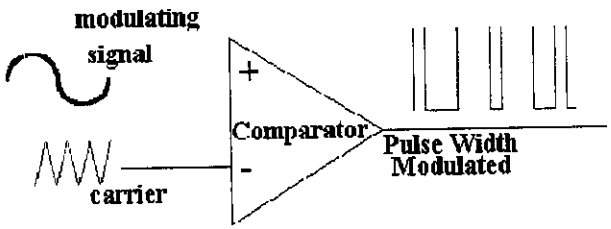


Fig. 2.10 Sine Saw tooth PWM

SPACE VECTOR PWM:

This PWM technique approximates the reference voltage Vref by a combination of the eight switching patterns (V0 to V7). The sinusoidal voltage is treated as a constant amplitude vector rotating at constant frequency. The vectors (V1 to V6) divide the plane into six sectors (each sector: 60 degrees) as shown in fig 3.10. Vref is generated by two adjacent non-zero vectors and two zero vectors. The switching pattern for a single sector is shown in figure 3.11. S1-S6 are the six power transistors of the inverter. The transistors are switched on and off in the specific pattern to produce the required output.

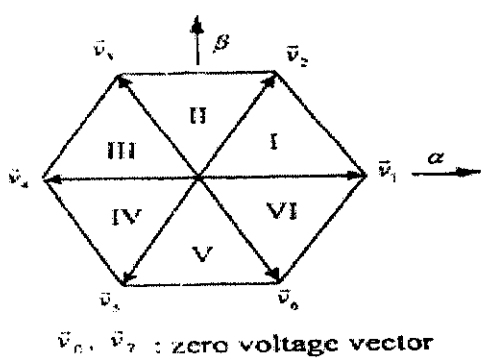


Fig 2.11 Basic switching vector

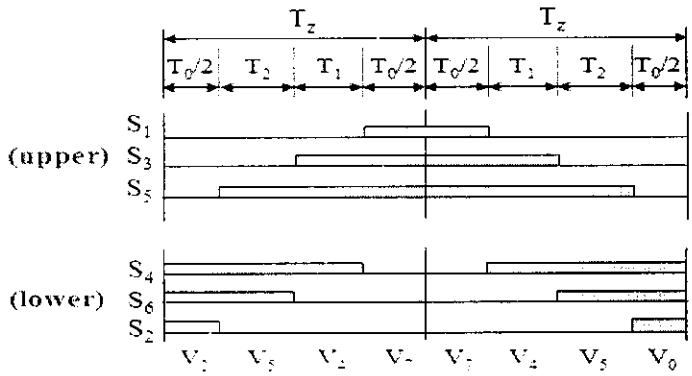


Fig 2.12 Switching pattern for sector-1

2.4.3. APPLICATIONS:

The popular applications of pulse width modulation are in power delivery, voltage regulation and amplification and audio effects.

POWER DELIVERY:

Pulse width modulation is used to reduce the total power delivered to a load without resulting in loss, which normally occurs when a power source is limited by a resistive element. The underlying principle in the whole process is that the average power delivered is directly proportional to the modulation duty cycle. If the modulation rate is high, it is possible to smooth out the pulse train using passive electronic filters and recover an average analog wave form.

VOLTAGE REGULATION:

High frequency pulse width modulation power control systems can be realized using semiconductor switches. Here, the discrete ON or OFF state of the modulation itself can be used to control the switches, thereby controlling the voltage or current across the load. The major advantage with these types of switches is that the voltage drop across it during conducting and non-conducting states is ideally zero. PWM's field of application includes Class D audio amplifiers, DC motor speed control, and light dimmers common in homes. Pulse width modulation is widely used in voltage regulators. It works by

switching the voltage to the load with the appropriate duty cycle; the output will maintain a voltage at the desired level.

AUDIO EFFECTS:

Pulse width modulation is also exploited in sound synthesis, especially subtractive synthesis. as the process gives a chorus effect or that of slightly detuned oscillators played together. Another application of PWM, as mentioned earlier, is the class D class D amplifier produces a PWM equivalent of the input analog signal, which is in turn fed to the loud speaker after filtering out the carrier wave by sending it through a suitable filter network. Due to the full on/off nature of PWM output, such amplifiers produce less heat than their conventional analog counterparts.

2.4.4.ADVANTAGES OF PWM:

PWM technique has the following advantages

- Suppresses lower order voltage and current harmonics
- Improved power factor.
- Include a simple drive circuit
- Good start-up characteristics and minimal heat dissipation in the pass transistor
- The signal remains digital all the way from the processor to the controlled system hence no digital-to-analog conversion is needed

2.4.5 PWM CONTROLLER VS RESISTIVE CONTROLLER:

At a 50 percent level, the PWM will use about 50 percent of full power, almost all of which is transferred to the load. A resistive controller at 50 percent load power would consume about 71 percent of full power; 50 percent of the power goes to the load, and the other 21 percent is wasted heating the dropping resistor. It takes a constant trickle of power to operate, so the efficiency improves with higher power loads.

The pulses are at the full supply voltage and will produce more torque in a motor by being able to overcome the internal motor resistances more easily. A resistive speed control will present a reduced voltage to the load, which can cause stalling in motor

applications. Finally, in a PWM circuit, common small potentiometers may be used to control a wide variety of loads, whereas large and expensive high power variable resistors are needed for resistive controllers.

Analog control scheme possesses the advantage of fast dynamic response, but suffers the disadvantages of complex circuitry, limited functions, and difficulty in circuit modification. The rapid development in high-performance low-cost microcontroller processors has encouraged research on digital PWM control. This control scheme has the advantages of simple circuitry, software control, and flexibility in adaptation to various applications.

CHAPTER 3

DESIGN OF Z SOURCE INVERTER:

3.1 CAPACITOR AND INDUCTOR REQUIREMENTS:

Impedance source network is a combination of two inductors and two capacitors. The impedance source network is the energy storage or filtering element for the Impedance source inverter. This impedance source network provides a second order filter. This is more effective to suppress voltage and current ripples. The inductor and capacitor requirement should be smaller compare than the traditional inverters. The two inductors (L1 and L2) are small and approach zero, the Impedance source network reduces to two capacitors (C1 andC2) in parallel and becomes traditional voltage source. Therefore, a traditional voltage inverter's capacitor requirements and physical size is the worst-case requirement for the Impedance source inverter. Considering additional filtering and energy storage provided by the inductors,
the Impedance source network should require less capacitance and smaller size compare with the traditional voltage source inverter. Similarly, when the two capacitors (C1 and C2) are small and approach zero, the Impedance source network reduces to two inductors (L1 and L2) in series and becomes a traditional current source. Therefore, a current source inverter's inductor requirements and physical size is the worst case requirement for the Impedance source inverter. The two capacitors are small; the Impedance source network reduces to two inductors in series and becomes a traditional current source. Considering additional filtering and energy storage by the capacitors, the Impedance source network should require less inductance and smaller size compared with the traditional current source inverters.

3.2 ANALYSIS OF IMPEDANCE NETWORK:

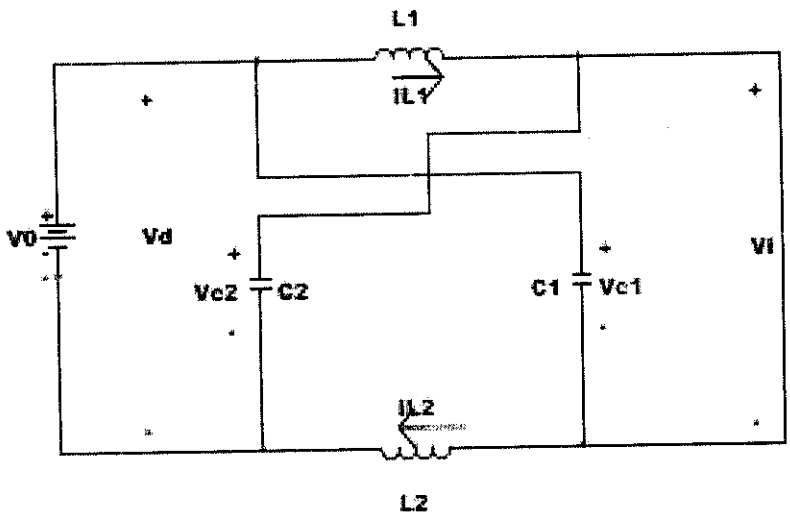


Fig.3.1 Equivalent circuit of impedance network.

Assume the inductors (L1&L2) and capacitors (C1&C2) have the same inductance and capacitance values respectively.

From the above equivalent circuit,

$Vc1 = Vc2 = Vc$ (1)

$VL1 = VL2 = VL$ (2)

$VL = Vc$, $Vd = 2Vc$
$Vi = 0$;

During the switching cycle T,

$VL = Vo - Vc$ (3)

$Vd = Vo$

$Vi = Vc - VL$ $Vc - (Vo - Vc)$

$Vi = 2Vc - Vo$ (4)

Where, Vo is the dc source voltage and

$T = To + T1$ (5)

The average voltage of the inductors over one switching period (T) should be zero in steady state

$VL = VL = To .Vc + T1(Vo-Vc)/T = 0$

$VL = (To .Vc + Vo.T1 - Vc.T1)/T=0$

$VL=(To-Tc)Vc/T + (T1.Vo)/T$

$Vc/Vo=T1/T1-T0$ (6)

Similarly the average dc link voltage across the inverter bridge can be found as follows.

From equation (4),

$Vi=Vi = (To .0+T1.(2Vc-Vo))/T$ (7)

$Vi = (2Vc. T1/T)-(T1Vo/T)$

$2Vc=Vo$

From equation (6),

$T1.Vo/(T1-To)=2Vc.T1/(T1-To)$

$Vc=Vo.T1/(T1-To)$

The peak dc-link voltage across the inverter bridge is

$Vi=Vc-Vl=2Vc-Vo$

$=T/(T1-To).Vo$
$=B.Vo$

Where,

$B=T/(T1-To)$ i.e., ≥ 1

B is the boost factor.

The output peak phase voltage from the inverter,

$Vac=M.vi/2$ (9)

Where,

M is the modulation index.

In this source, Vac=M.B.Vo/2 (10)

In the traditional sources,

Vac = M.Vo/2

For Z-Source,

Vac = M.B.Vo/2

The output voltage can be stepped up and down by choosing an appropriate buck - boost factor BB

BB= B.M (it varies from 0 to α) (11)

The capacitor voltage can be expressed as

Vc1=Vc2=Vc
= (1-To/T).Vo/(1-2To/T)

The buck-boost factor BB is determined by the modulation index M and the boost factor B. The boost factor B can be controlled by duty cycle of the shoot through zero state over the non shoot through states of the PWM inverter. The shoot through zero state does not affect PWM control of the inverter. Because it equivalently produce the same zero voltage to the load terminal. The available shoot through period is limited by the zero state periods that is determined by the modulation index.

3.2 DESIGN OF IMPEDANCE(Z) NETWORK:

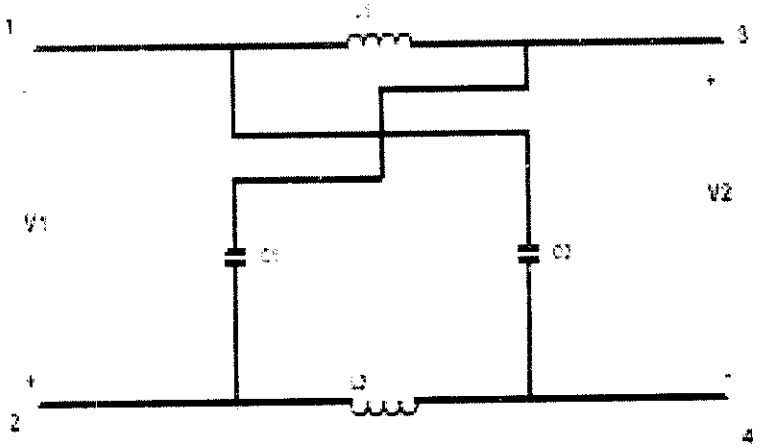


Fig 3.2 Impedance network.

Where,

L1 and L2 - series arm inductors
C1 and C2 - parallel arm capacitors
V1 is input voltage
V2 is output voltage

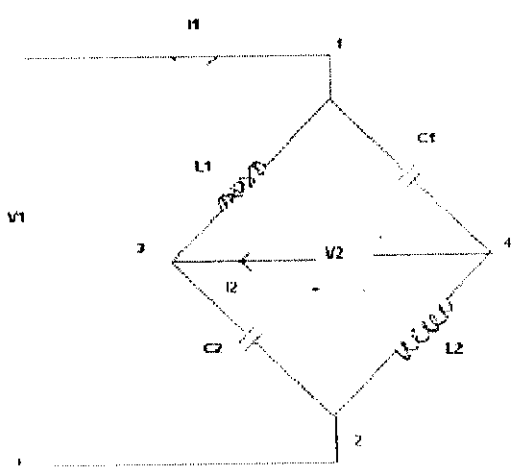


Fig 3.3 Impedance network – redrawn.

The impedance network circuit is redrawn as shown above.

Now assume,

I2 =0.

The current I1enters the bridge at point 1 and divides equally between the two arms of the bridge.

Using Kirchhoff's law,

I1.L/2+V2 = I1/2c

V2 = I1/2c - I1.L/2

V2 = I1/2 [1/c -L]

Assume,

c=5.5 mF

440 = 5/2 [1/5.5*10-3- L]

L = 5.8 H

Vdc=BV0

= (2B/B+1) Vc.

CHAPTER 4

SIMULATION:

INTRODUCTION TO MATLAB:

Simulink® is an environment for multidomain simulation and Model-Based Design for dynamic and embedded systems. It provides an interactive graphical environment and a customizable set of block libraries that let you design, simulate, implement, and test a variety of time-varying systems, including communications, controls, signal processing, video processing, and image processing. Simulink is integrated with MATLAB®, providing immediate access to an extensive range of tools that let you develop algorithms, analyze and visualize simulations, create batch processing scripts, customize the modeling environment, and define signal, parameter, and test data.

4.1.1 KEY FEATURES:

A) Extensive and expandable libraries of predefined blocks

B) Interactive graphical editor for assembling and managing intuitive block diagrams

C) Ability to manage complex designs by segmenting models into hierarchies of design components

D) Model Explorer to navigate, create, configure, and search all signals, parameters, properties, and generated code associated with your model

E) Application programming interfaces (APIs) that let you connect with other simulation programs and incorporate hand-written code

F) Matlab Function blocks for bringing MATLAB algorithms into Simulink and embedded system implementations

G) Simulation modes (Normal, Accelerator, and Rapid Accelerator) for running simulations interpretively or at compiled C-code speeds using fixed- or variable-step solvers

H) Graphical debugger and profiler to examine simulation results and then diagnose performance and unexpected behavior in your design

I) Full access to MATLAB for analyzing and visualizing results, customizing the modeling environment, and defining signal, parameter, and test data

J) Model analysis and diagnostics tools to ensure model consist ency and identify modeling errors

4.1.2 CREATING AND WORKING WITH MODELS:

With Simulink, you can quickly create, model, and maintain a detailed block diagram of your system using a comprehensive set of predefined blocks. Simulink provides tools for hierarchical modeling, data management, and subsystem customization, making it easy to create concise, accurate representations, regardless of your system's complexity.

SELECTING AND CUSTOMIZING BLOCKS:

Simulink software includes an extensive library of functions commonly used in modeling a system. These include:

1)Continuous and discrete dynamics blocks, such as Integration and Unit Delay.

2)Algorithmic blocks, such as Sum, Product, and Lookup Table .

3)Structural blocks, such as Mux, Switch, and Bus Selector.

You can customize these built-in blocks or create new ones directly in Simulink and place them into your own libraries.Additional blocksets (available separately) extend Simulink with specific functionality for aerospace, communications, radio frequency, signal processing, video and image processing, and other applications.

4.1.3 DEFINIG AND MANAGING SIGNALS AND PARAMETERS:

Simulink enables you to define and control the attributes of signals and parameters associated with your model. Signals are time-varying quantities represented by the lines connecting blocks. Parameters are coefficients that help define the dynamics and behavior of the system.

Signal and parameter attributes can be specified directly in the diagram or in a separate data dictionary. Using the Model Explorer, you can manage your data dictionary and quickly repurpose a model by incorporating different data sets. After building your model in Simulink®, you can simulate its dynamic behavior and view the results live. Simulink software provides several features and tools to ensure the speed and accuracy of your simulation, including fixed-step and variable-step solvers, a graphical debugger, and a model profiler.

ANALYSING RESULTS:

Simulink® includes several tools for analyzing your system, visualizing results, and testing, validating, and documenting your models.

4.1.4 VISUALIZING RESULTS:

You can visualize the system by viewing signals with the displays and scopes provided in Simulink software. Alternatively, you can build your own custom displays using MATLAB® visualization and GUI development tools. You can also log signals for post-processing.

4.1.5 TESTING AND VALIDATING THE MODELS:

Simulink includes tools to help you generate test conditions and validate your model's performance. These include blocks for creating simulation tests. For example, the Signal Builder block lets you graphically create waveforms to exercise models. Using the Signal & Scope Manager, you can inject signals into your model, as well as log and view signals, without adding blocks. Simulink also provides model verification blocks to check that block outputs conform to your design requirements.

MATLAB MODEL:

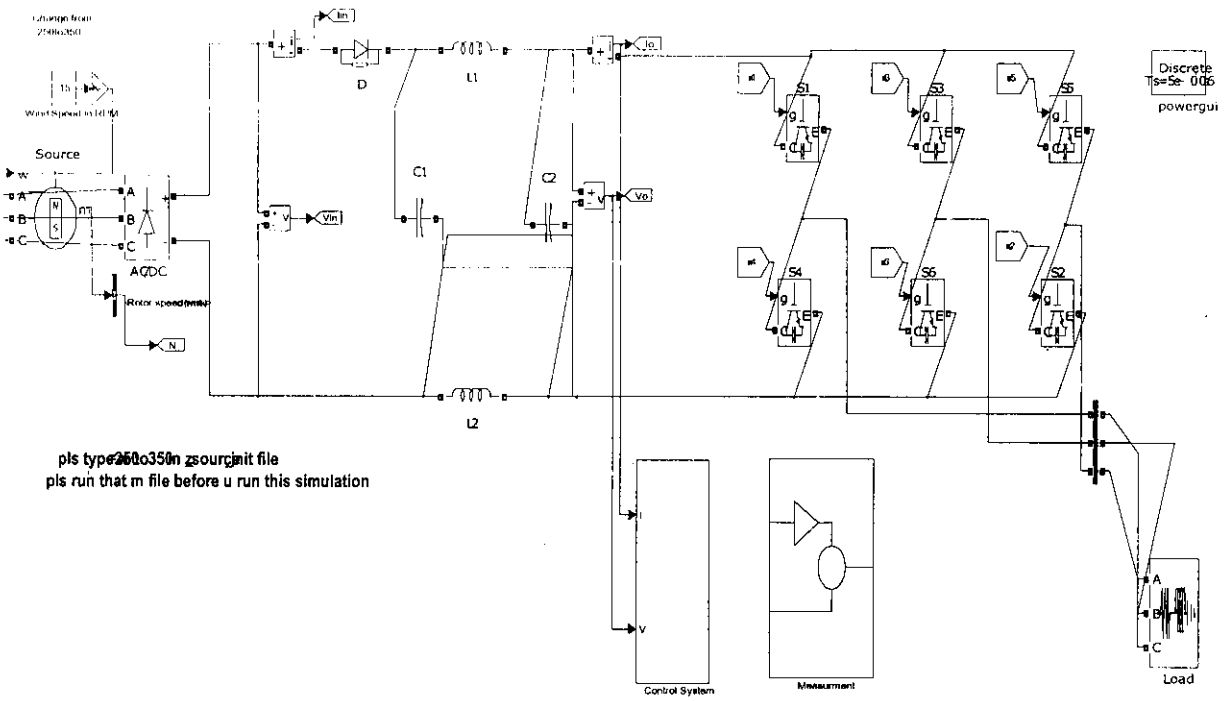


Fig 4.1 MATLAB model for the ZSI based power converter.

The MATLAB model is as shown in fig 4.1.The input voltage to the rectifier is from the wind turbine whose output voltage varies according to the wind velocity.the wind velocity is set here as n early 17m/s. Then after the rectifier block where the ac is converted into dc , is the inductor and capacitor connection which forms the impedance source.Then the voltage source inverter is built by the six power switches and here for MATLAB implementation IGBTs are used.they rare connected to the load.

The control signals given to the power switches are used for switching on and off the corresponding switches.The control signals are the PWM pulses given to operate the power switches and these control signals are generated from the control system block. The measurement block is used for the measurement of voltages and currents at various levels like rectifier output,Z source output and Z-source inverter

output.the clock is used for the application of clock pulse and scope block is used to view the output.

4.3 SIMULATION RESULTS:

4.3.1 TRIGGERING PULSES:

The triggering pulses for all the six power switches is shown along with the clock pulse.

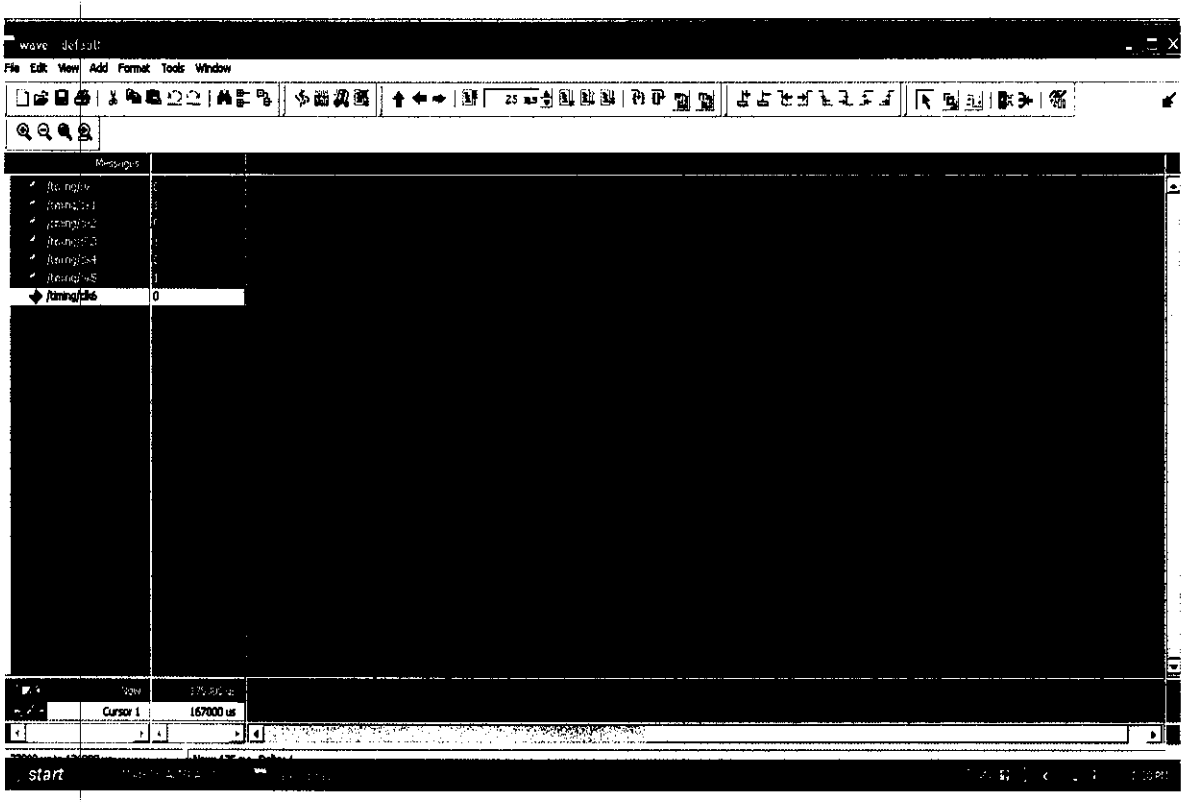


Fig 4.2 Triggering pulses for power switches

4.3.2 INPUT VOLTAGE:

The input voltage of around 580volts is shown and the output voltage is maintained constsnt irrespective of the changes in the input voltage.

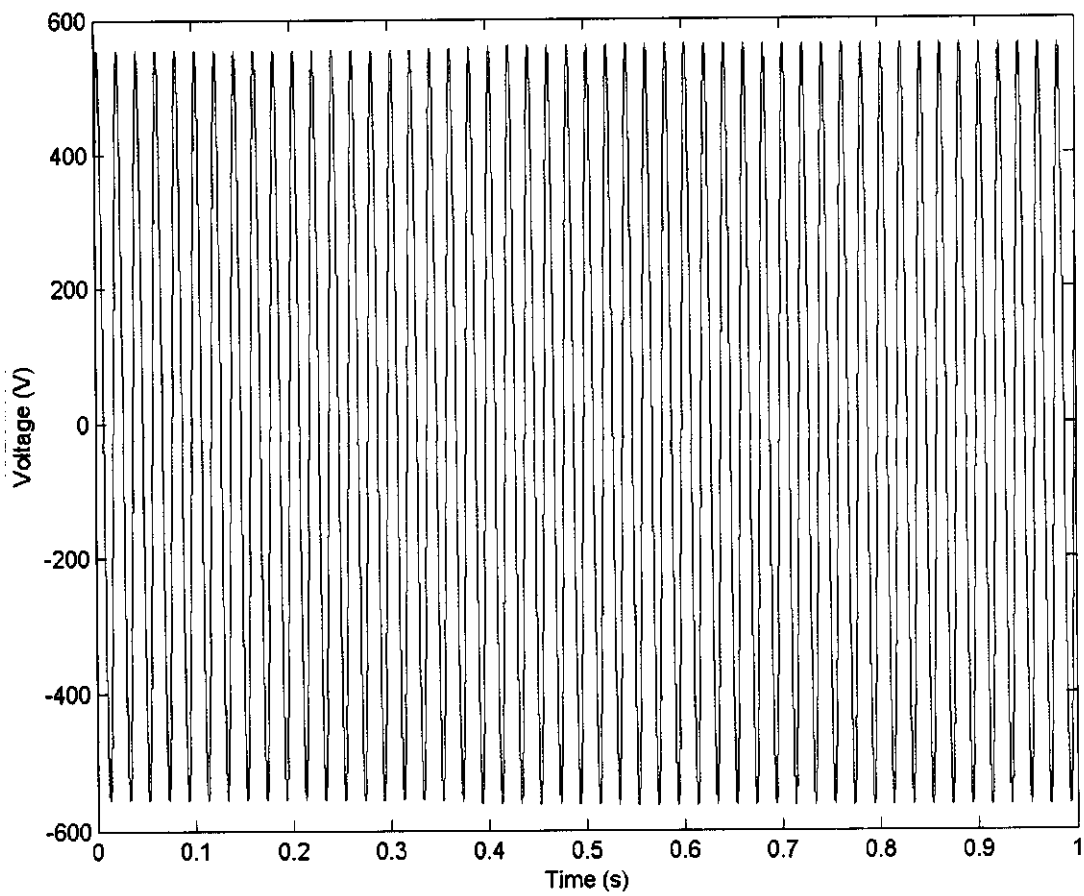


Fig 4.3 graph showing input voltage

4.3.3 OUTPUT VOLTAGE:

The output voltage is stabilized and maintained constant at 415volts to be integrated with the grid.

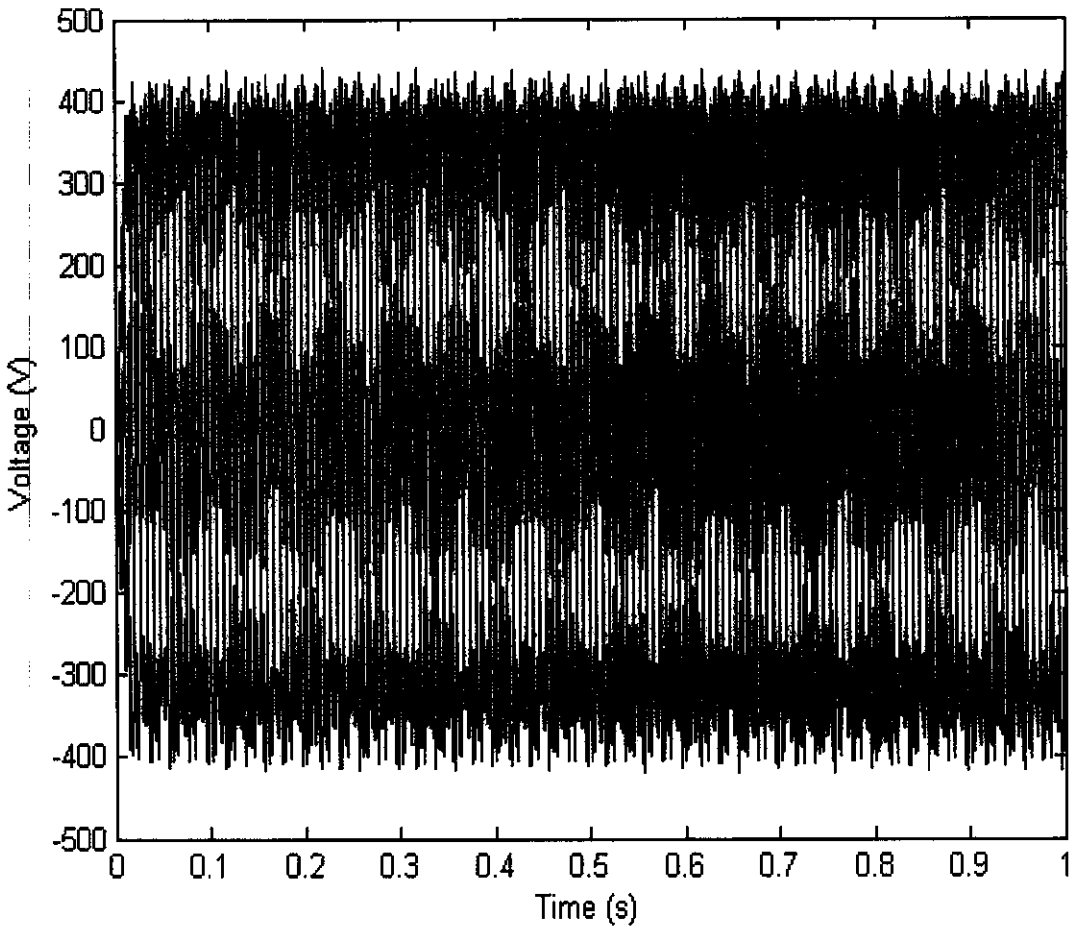


Fig 4.4 Output voltage

CHAPTER 5

HARDWARE DESCRIPTION:

5.1 BLOCK DIAGRAM:

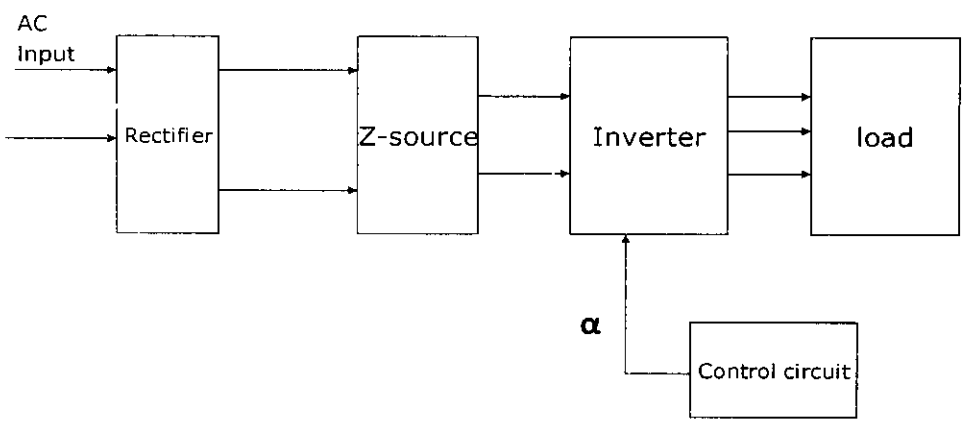
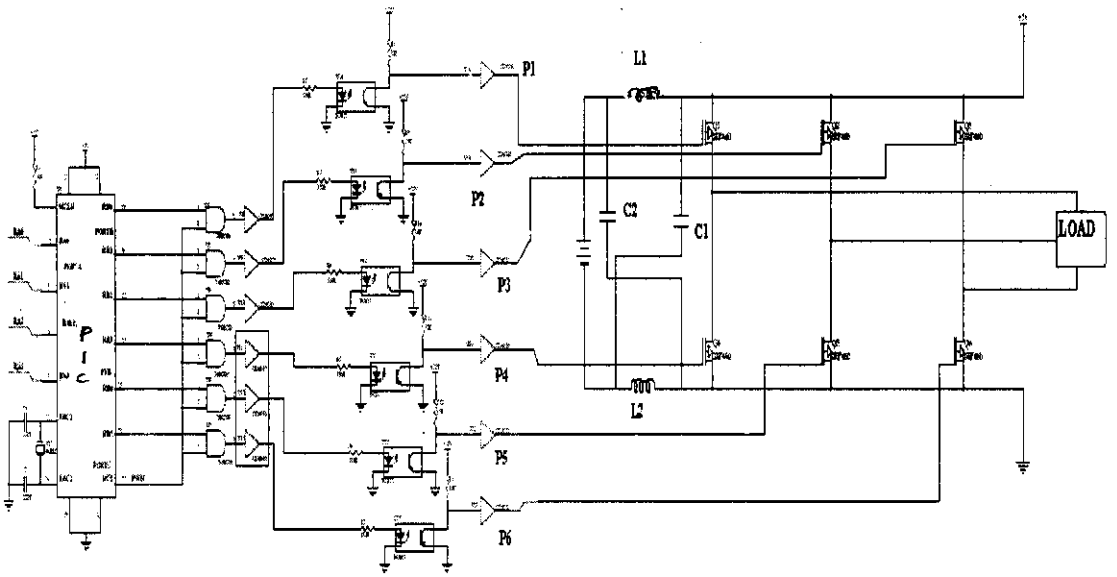


Fig 5.1 Block Diagram

5.2 HARDWARE CIRCUIT DIAGRAM:

Fig 5.2 Circuit Diagram



5.3 POWER SUPPLY CIRCUIT:

All the electronic components only work with a DC supply ranging from −12V to +12V. We are using the commonly available energy source of 230v-50Hz and stepping down , rectifying, filtering and regulating the voltage.

STEP DOWN TRANSFORMER:

When AC is applied to the primary winding of the power transformer it can either be stepped down or up depending on the value of DC needed. In our circuit the transformer of 230v/12-0-12v is used to perform the step down operation where a 230V AC appears as 12V AC across the secondary winding. The current rating of the transformer used in our project is 250mA.. Apart from stepping down AC voltages, it gives isolation between the power source and power supply circuitries.

RECTIFIER UNIT:

In the power supply unit, rectification is normally achieved using a solid state diode. Diode has the property that will let the electron flow easily in one direction at proper biasing condition. As AC is applied to the diode, electrons only flow when the anode and cathode is negative. Reversing the polarity of voltage will not permit electron flow. A commonly used circuit for supplying large amounts of DC power is the bridge rectifier. A bridge rectifier of four diodes (4*IN4007) are used to achieve full wave rectification.

Two diodes will conduct during the negative cycle and the other two will conduct during the positive half cycle. The DC voltage appearing across the output terminals of the bridge rectifier will be somewhat lass than 90% of the applied rms value. Normally one alteration of the input voltage will reverse the polarities. Opposite ends of the transformer will therefore always be 180 deg out of phase with each other.

For a positive cycle, two diodes are connected to the positive voltage at the top winding and only one diode conducts. At the same time one of the other two diodes conducts for the negative voltage that is applied from the bottom winding due to the forward bias for that diode. In this circuit due to positive half cycle D1 & D2 will conduct to give 10.8v pulsating DC. The DC output has a ripple frequency of 100Hz. Since each altercation produces a resulting output pulse, frequency = 2*50 Hz. The output obtained is not a pure DC and therefore filtration has to be done.

FILTERING UNIT:

Filter circuits which usually capacitor is acting as a surge arrester always follow the rectifier unit. This capacitor is also called as a decoupling capacitor or a bypassing capacitor, is used not only to 'short' the ripple with frequency of 100Hz to ground but also to leave the frequency of the DC to appear at the output. A load resistor R1 is connected so that a reference to the ground is maintained. 1000if/25v : for the reduction of ripples from the pulsating. 10if/63v : for maintaining the stability of the voltage at the load side.O.01if : for bypassing the high frequency disturbances.

VOLTAGE REGULATORS:

The primary purpose of a regulator is to aid the rectifier and filter circuit in providing a constant DC voltage to the device. Power supplies without regulators have an inherent problem of changing DC voltage values due to variations in the load or due to fluctuations in the AC liner voltage. With a regulator connected to the DC output, the voltage can be maintained within a close tolerant region of the desired output. IC7805 and IC7905 is used in this project for providing +5v and –5v DC supply.

5.4 OPTO COUPLER:

Optocoupler is also termed as optoisolator. They are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (light-emitting diode) and an optical receiver such as a phototransistor or light-triggered diac or a resistor that changes resistance with variations in light intensity or other device that conducts differently in the presence of light. These devices are used to isolate the control voltage from the controlled circuit. Optocouplers typically come in a small 6-pin or 8-pin IC package.. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. The basic idea is shown in Fig.6.5, along with the usual circuit symbol for an optocoupler.

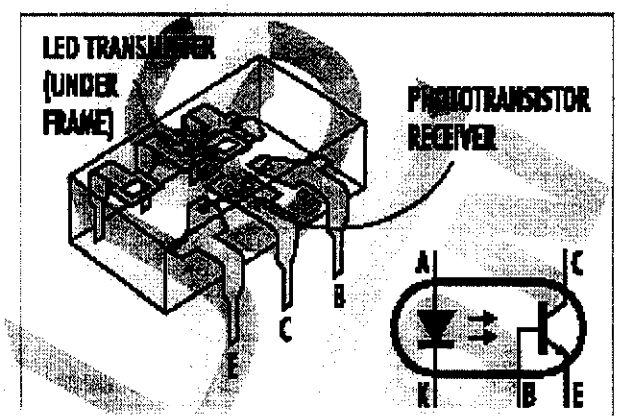


Fig 5.3 Construction of a typical optocoupler and the circuit symbol

Usually the electrical connections to the LED section are brought out to the pins on one side of the package and those for the phototransistor or diac to the other side, to physically separate them as much as possible. This usually allows optocouplers to withstand voltages of anywhere between 500V and 7500V between input and output. Optocouplers are essentially digital or switching devices, so they are best for transferring either on-off control signals or digital data. Analog signals can be transferred by means of

frequency or pulse-width modulation. Thus the triggering pulses are given to the inverter circuit.

The optocoupler used in our circuit is SFH615.This features a high current transfer ratio, low coupling capacitance and high isolation test voltage. They employ a GaAs led as emitter which is optically coupled with a silicon planar photo transistor as detector. The components are incorporated in a plastic plug-in DIP-4 package. The coupling devices are designed for signal transmission between two electrically isolated circuits. The potential difference between the circuits to be coupled is not allowed to exceed the maximum permissible reference voltages. The couplers are end stackable in a 2.54 mm and are considered as successor types for the couplers in metal case. Multi couplers can thus easily be implemented and conventional multicouplers can be easily replaced.

5.4.1 FEATURES:

- Isolation test voltage is 2800 volts.
- High current transfer ratio

  At 10 mA : 40-320 %

  At 1 mA : 60 %.
- Fast switching times
- Stable temperature
- Low saturation voltage
- High collector emitter voltage of 70v.

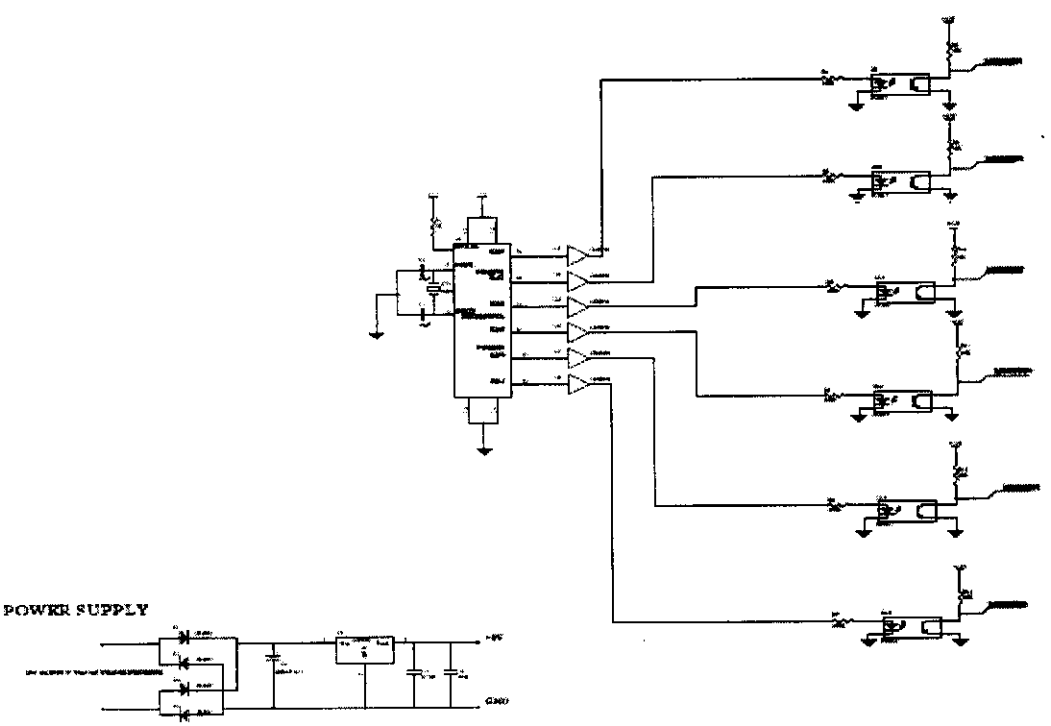


Fig 5.4 Controller and Optocoupler

5.5 DRIVER CIRCUIT:

The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter. It gives the triggering pulses to the switches in the proper sequence. The signal after being electrically isolated is given to the driver circuit. The diagram given below represents the driver unit with single channel. Similarly there are five other channels and each channel is used to drive the inverter circuit. The digital signal from the PIC 16f877a comes to this driver circuit.It forms the main part of the hardware developed. The driver unit contains the following important units.

A. Capacitor
B. Supply
C. Resistor
D. Buffer
E. MOSFETS

The signal from the microcontroller reaches the optocoupler where it is electrically isolated form the rest of the circuit to prevent damage to the microcontroller in case of improper or back firing. The 330 ohm resistor is used for current limiting(biasing). When the signal is electrically isolated, it is passed through the buffer cd 4050.This buffer is used increase the signal strength and then it is sent to the darlington pair. The Resistor and capacitor are used for pull down.

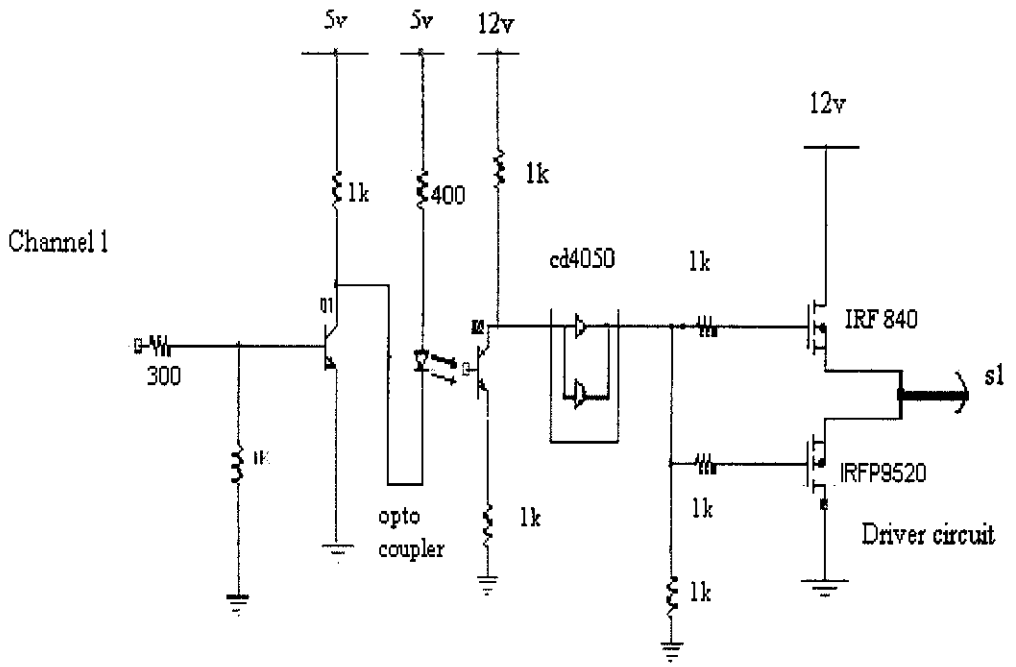


Fig 5.5 Driver circuit.

5.6 BUFFER:

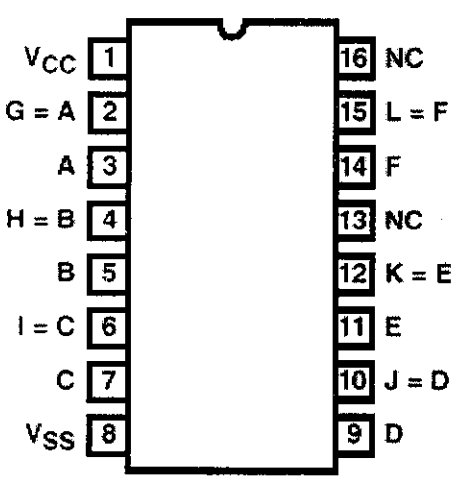


Fig5.6 Pin diagram of CD4050

SCHEMATIC DIAGRAM OF CD4050B:

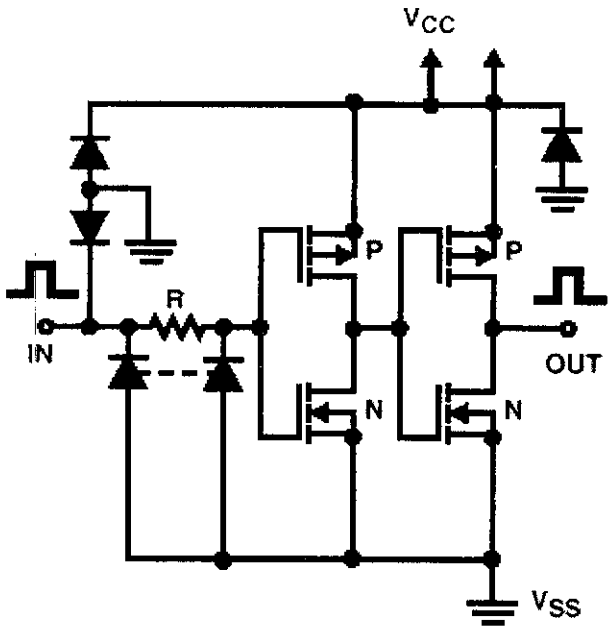


Fig 5.7 Schematic Diagram of CD4050B

CD4050B device is an inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (VCC). The input-signal high level (VIH) can exceed the VCC supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL / TTL converters and can drive directly two DTL/TTL loads. (V CC = 5V, V OL _ 0.4V, and I OL _ 3.3mA.).The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because CD4050B requires only one power supply, they are preferred over the CD4010B and should be used in place of CD4010B in all inverters, current drivers, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation.

5.7 MOSFETS:

The signal from the buffer amplifier is given to the MOSFET circuit. On top is the N channel IRF 840 and P channel IRFP 9520. When the input is 0v , P channel mosfet conducts which is connected to ground. So there is no output. When the input is 1v, then the N channel mosfet conducts and gives an output voltage of 12 v, which in turn is used to drive the inverter. The output obtained by this manner is sharp.

5.7.1 IRZ44 MOSFET:

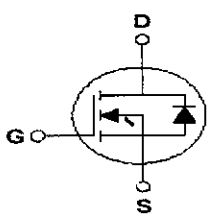


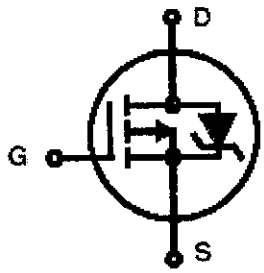
Fig 5.8 Symbol of IRZ44.

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, CMOS technology.This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

FEATURES:

- 8.0A, 500V, rds(on) = 0.8;VGS = 10 V.
- Fast switching.
- 100% avalanche tested.
- Improved dv/dt capability.

5.7.2 IRF9520 MOSFET:



P-3425

Fig 5.9 Symbol of IRF9520

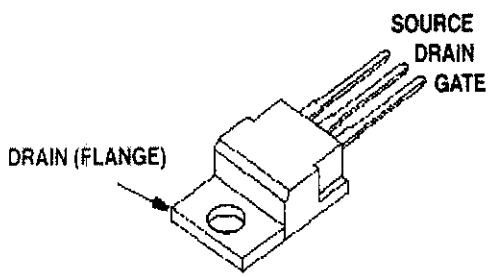


Fig 5.10 IRF9520 packaging.

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

FEATURES:

- rds(ON) = 0.600 ohm.
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics

- High Input Impedance

MOSFET

The component that is used as the switch in the inverter unit is the MOSFET which is a voltage controlled device. They are the power semi conductor devices that have a fast switching property with a simple drive requirement.

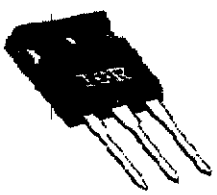


Fig 5.11 (a) MOSFET Switch

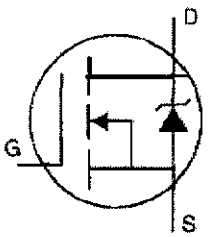


Fig 5.11 (b) MOSFET Symbol

V_{dss}= 500 V

Rds (on) = 0.27 ohm

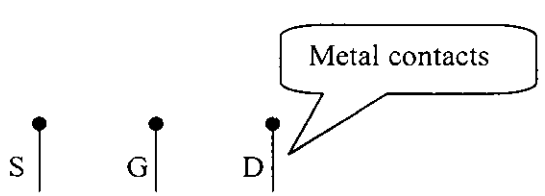
Id= 20 A

This MOSFET provides the designer with the best combination of fast switching, rugged device design, low on-resistance and cost-effectiveness. This package is preferred for commercial and industrial applications where higher power levels are to be handled.

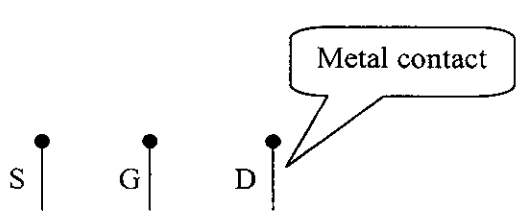
5.7.3 CONSTRUCTION AND OPERATION PRINCIPLE OF MOSFET:

There are two basic types of MOSFETs. They are N Channel depletion type and N Channel enhancement type.

A. N Channel depletion type type



B. N Channel enhancement



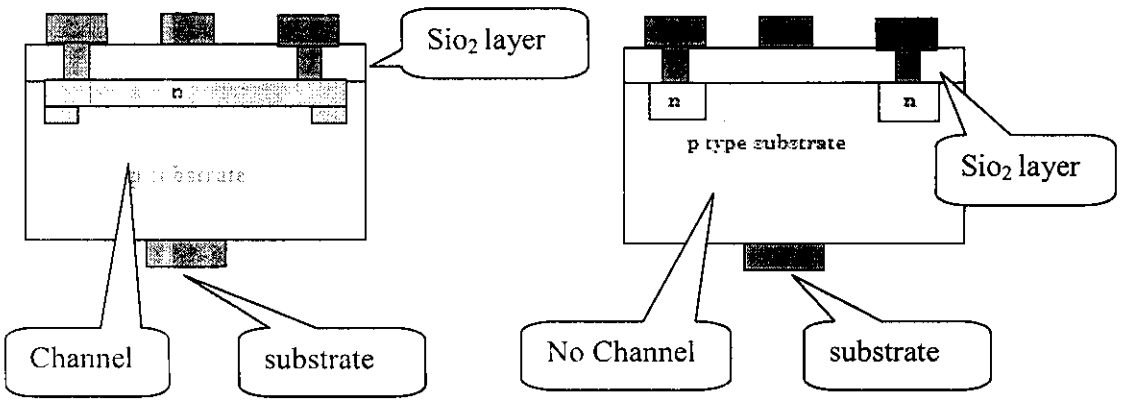


Fig 5.12 A, B MOSFET Types

A) N CHANNEL DEPLETION:

The N channel depletion type of MOSFET is constructed with p -Substrate. It has two n doped regions, which forms the drain and source. It has Sio_2 insulating layer between the channel and the metal layer. Thus it has three terminals namely drain source and gate.With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the N-channel is depleted of some of its electrons, thus by decreasing the channel conductivity.

When a positive voltage is applied between the gate and source, more electrons are induced in the channel by capacitor action. So there is a flow of current from drain to source. As the gate source voltage increases, the channel gets wider by accumulation of more negative charges and resistance to the channel decreases. Thus more current from flows from drain to source. As there is a current flow through device for zero gate source voltage, it is normally called as ON MOSFET.

B) N CHANNEL ENHANCEMENT:

The N channel enhancement MOSFET is similar to the depletion type in the construction except that there is no physical existence of the channel when it is unbiased.

When the positive voltage is applied between the gate and the source, the electrons get accumulated in the channel by capacitive induction in the channel formed out of electrons allowing the flow of current. This channel gets widened as more positive

voltage is applied between gate and source. There will not be any condition through the device if the gate source voltage is negative.

As the enhancement type MOSFET conduct only after applying positive gate voltage, it is also called as normally OFF MOSFET. For this reason it becomes easily controllable and is used in power electronics as a switch.

CHAPTER 6

CONTROL OF ZSI USING PIC MICRO CONTROLLER

6.1 INTRODUCTION:

The PIC16F877A CMOS FLASH-based 8-bit microcontroller is upward compatible with the PIC16C5x, PIC12Cxxx and PIC16C7x devices. It features 200 ns instruction execution, 256 bytes of EEPROM data memory, self programming, an ICD, 2 Comparators, 8 channels of 10-bit Analog-to-Digital (A/D) converter, 2 capture/compare/PWM functions, a synchronous serial port that can be configured as either 3-wire SPI or 2-wire I2C bus, a USART, and a Parallel Slave Port.

PIC16F877A is a small piece of semiconductor integrated circuits. The package type of this integrated circuits is DIP package. DIP stand for Dual Inline Package for semiconductor IC. This package is very easy to be soldered onto the stripboard. However using a DIP socket is much more easier so that this chip can be plugged and removed from the development board.

PIC16F877A is very cheap. Apart from that it is also very easy to be assembled. additional components that you need to make this IC work is just a 5V power supply adapter, a 20MHz crystal oscillator and 2 units of 22pF capacitors. This IC can be reprogrammed and erased up to 10,000 times. Therefore it is very good for new product development phase.

This IC can be reprogrammed and erased up to 10,000 times. Therefore it is very good for new product development phase.

6.2 PIN DESCRIPTION:

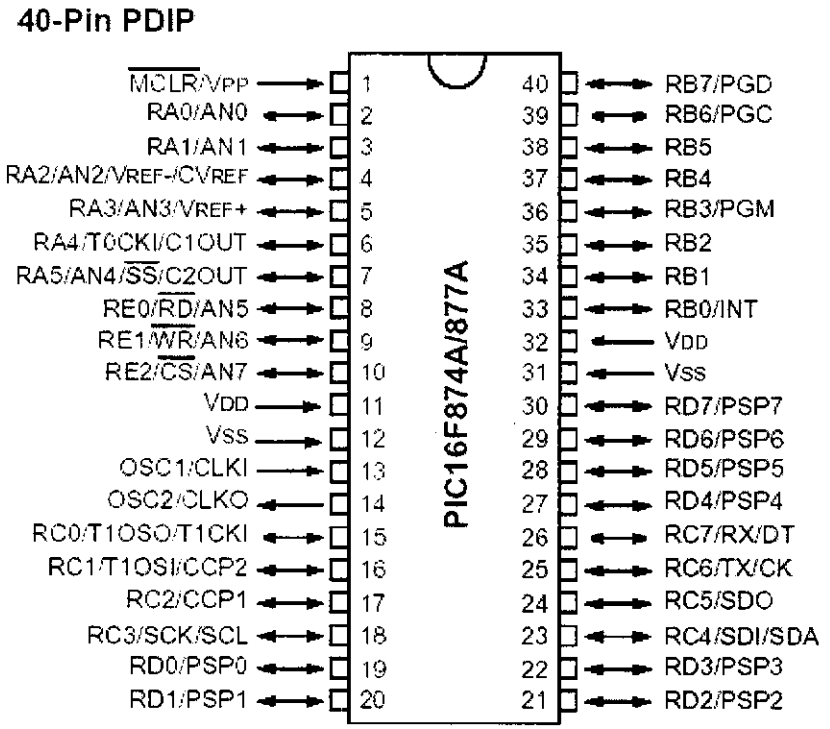


Fig 6.1 PIC micro controller

The input pulses to the switches of the inverter are taken from the pin 33, 34,35,36,37 and 38. The pin description for the Fig.5.1 is given in appendix 1.

6.3 OPERATION OF THE SYSTEM:

The design consists of a 24V power supply, rectifier, embedded module and impedance source inverter module. The voltage generated from wind turbine is given to the 24v rechargeable battery through a diode. The voltage input depends on the variations in wind velocity ,hence to maintain the constant AC voltage in the output side by impedance source technique. Based on the voltage generated from the wind turbine the duty cycle of z source inverter can be adjustable with help of PIC16F877A controller. The PWM

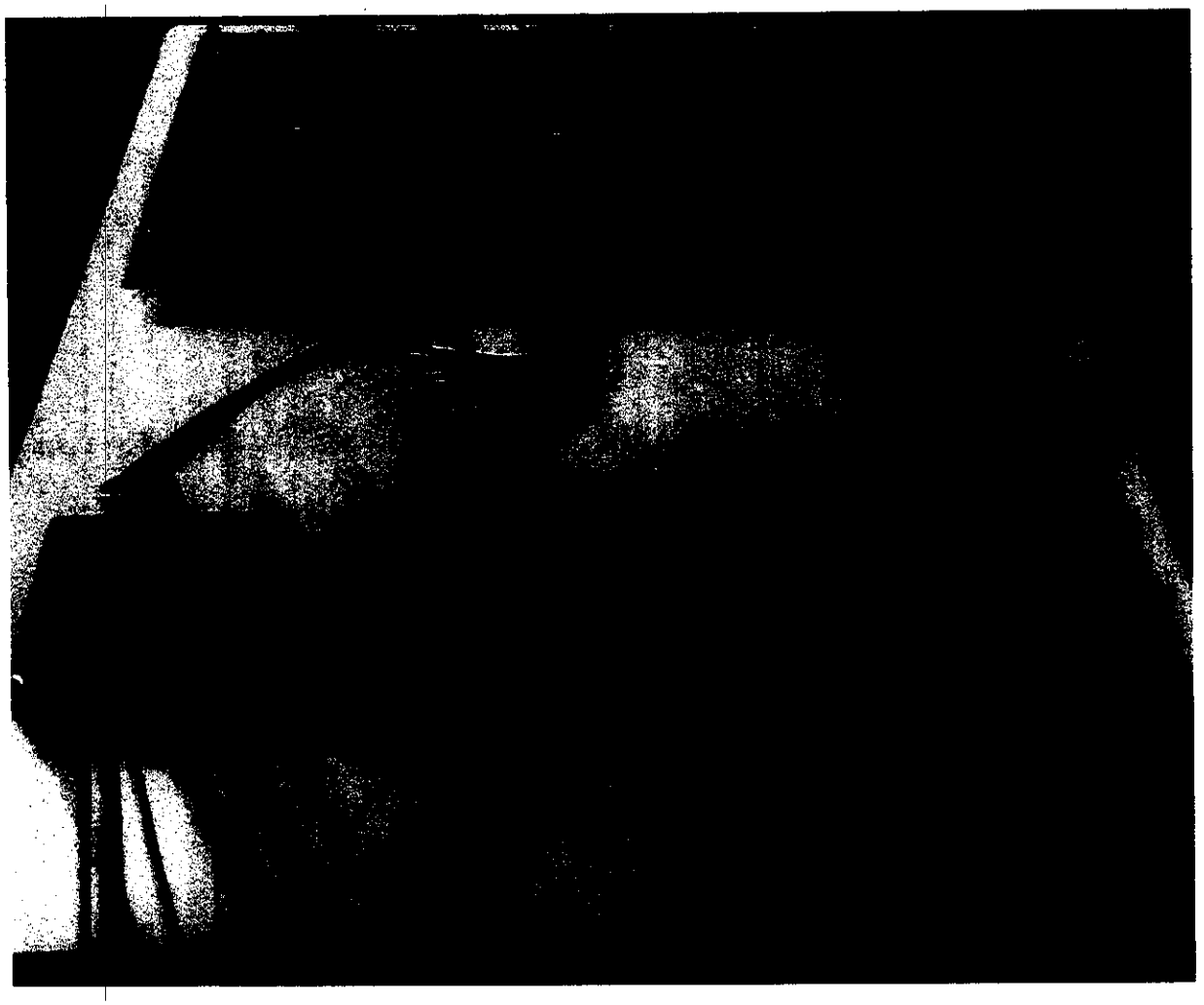
pulses are generated in the controller are 5V amplitude, this voltage is not sufficient to drive the MOSFET switching device.

Hence the driver module is essential to drive the switching device through opto isolator SFH615, the MOS FET is used to switch ON/OFF the circuit based on instruction coming from controller, the device name is IRFZ40.

The PIC16F877A controller is used to generate the switching pattern for the impedance source inverter. It is a 40 pin IC, having inbuilt analog to digital converters.

This design is interconnecting more than one sources to inject the supply to the grid, here interconnecting solar and battery sources.

6.4. HARDWARE PHOTOGRAPHY



CONCLUSION:

This project entitles as "Implementation of Z-Source Inverter for wind energy conversion system". The modeling of impedance source inverter was implemented in MATLAB environment at high voltage level. The hardware model was designed with help of MOSFET switch and PIC16F877A controller, these controller generate the PWM pulses for ZSI switches.

REFERENCES:

1. Fang Zheng Peng, Fellow, IEEE, Alan Joseph, JinWang, Student Member, IEEE,Miaosen Shen, Student Member, IEEE, Lihua Chen, Zhiguo Pan, Student Member,IEEE, Eduardo Ortiz-Rivera 'Z-Source Inverter for Motor Drives', *IEEE Transactions on Power Electronics* Vol. 20 ,No. 4 ,pp. 857-863, July 2005.

2. F. Z. Peng, M. Shen, and Z. Qian, 'Maximum boost control of the z-source inverter', in *Proc. 39th IEEE Industry Applications Conf.*, Vol. 1, Oct. 2004.

3. F. Z. Peng, 'Z-Source Inverter',*IEEE Trans. Industrial Applications,* Vol. 39, No. 2, pp. 504–510, Mar. /Apr. 2003.

4. Miaosen Shen, Student Member, IEEE ,Jin Wang, Member, IEEE, Alan Joseph ,Fang Zheng Peng ,fellow, IEEE, Leon M.Tolbert ,Senior Member, IEEE, and Donald J. Adams , Member, IEEE 'Constant Boost control of the Z-Source Inverter to Minimize Current Ripple and Voltage Stress', in *IEEE Transaction on Industrial Application* ,Vol. 42, No. 3, May/June 2006.

5. S.Rajakaruna, Member, IEEE and Y.R.L.Jayawickrama, 'Designing Impedance Network of Z-Source Inverters', *power engineering conference*,Vol. 2,No. 5,pp. 962-967 , Mar/Apr2005.

APPENDIX A

MICROCONTROLLER FEATURES:

HIGH-PERFORMANCE RISC CPU:

- Only 35 single-word instructions to learn
- All single-cycle instructions except for programbranches, which are two-cycle
- Operating speed: DC – 20 MHz clock input DC – 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,

  Up to 368 x 8 bytes of Data Memory (RAM),

  Up to 256 x 8 bytes of EEPROM Data Memory
- Pin out compatible to other 28-pin or 40/44-pin

  PIC16CXXX and PIC16FXXX microcontrollers

ANALOG FEATURES:

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (VREF) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

SPECIAL MICROCONTROLLER FEATURES:

- 100,000 erase/write cycle Enhanced Flash Program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single-supply 5V In-Circuit Serial Programming

• Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation

• Programmable code protection

• Power saving Sleep mode

• Selectable oscillator options

• In-Circuit Debug (ICD) via two pin

• Low-power, high-speed Flash/EEPROM technology

• Fully static design

• Wide operating voltage range (2.0V to 5.5V)

• Commercial and Industrial temperature ranges

• Low-power consumption

• Programmable code protection

• Power saving Sleep mode

4.3 MEMORY ORGANIZATION

There are three memory blocks in each of the PIC16F87XA devices. The program memory and datamemory have separate buses so that concurrent access can occur and they are as follows.

PROGRAM MEMORY ORGANIZATION

The PIC16F87XA devices have a 13-bit program counter capable of addressing an 8K word x 14 bit program memory space. The PIC16F876A/877A devices have 8K words x 14 bits of Flash program memory, while PIC16F873A/874A devices have 4K words x 14 bits. Accessing a location above the physically implemented address will cause a wraparound.

DATA MEMORY ORGANIZATION

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (Status<6>) and RP0 (Status<5>) are the bank select bits.

Table A.1 Data Memory Organization

RP1 : RP0	BANK
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

4.4 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly, through the File Select Register (FSR).

I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA AND THE TRISA REGISTER

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding

PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The TRISA register controls the direction of the port pins even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

PORTB AND THE TRISB REGISTER

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the In-Circuit Debugger and Low-Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in **"Special Features of the CPU"**.

PORTC AND THE TRISC REGISTER

PORTC is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). PORTC is multiplexed with several peripheral functions (Table 4-5). PORTC pins have Schmitt Trigger input buffers. When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin.

PORTD AND TRISD REGISTERS:

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTD can be configured as an 8-bit

wide microprocessor port (Parallel Slave Port) by setting control bit, PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

PORTE AND TRISE REGISTER

PORTE has three pins (RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7) which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers. The PORTE pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make certain that the TRISE<2:0> bits are set and that the pins are configured as digital inputs. Also, ensure that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

4.5 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE:

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the 40/44-pin devices. The conversion of an analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low-voltage reference input that is software selectable to some combination of VDD, VSS, RA2 or RA3. The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The

analog input model is shown in Figure 11-2. The source impedance (RS) and the internal sampling switch impedance (RSS) directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD); see Figure 11-2. **The maximum recommended impedance for analog sources is 2.5 kΩ.** As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D Result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To calculate the minimum acquisition time, Equation 11-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution

1: The reference voltage (VREF) has no effect on the equation since it cancels itself out.
2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
3: The maximum recommended impedance for analog sources is 2.5 kΩ. This is required to meet the pin
leakage specification

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0**: A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0**: Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

Note: The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/$\overline{\text{DONE}}$**: A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON**: A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

ADCON0 REGISTER (address: 1Fh):

Table A.2 ADCON0 REGISTER (address: 1Fh)

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D Result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time **"A/D Acquisition Requirements" is used.** After this acquisition time has elapsed, the A/D conversion can be started. To do an A/D Conversion, follow these steps:

1. Configure the A/D module:
    - Configure analog pins/voltage reference and digital I/O (ADCON1)
    - Select A/D input channel (ADCON0)
    - Select A/D conversion clock (ADCON0)
    - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
    - Clear ADIF bit
    - Set ADIE bit
    - Set PEIE bit
    - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
    - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete by either:
    - Polling for the GO/DONE bit to be cleared (interrupts disabled); OR
    - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL), clear bit ADIF if required.

7. For the next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD.A minimum wait of 2TAD is required before next acquisition starts.

APPENDIX B

CODING:

```
`timescale 1ms/100us;
module timing;
reg clk;
reg clk1,clk2,clk3,clk4,clk5,clk6;
initial
begin
clk=0;
clk6=0;
//clk1=1;
end
always
begin
# 10 clk=~clk;
clk1=~clk;
# 3.33 clk2=clk;
clk3=~clk2;
# 6.667 clk4=clk;
clk5=~clk4;
end
always
begin
# 0.6 clk6=~clk6;
# 0.4 clk6=~clk6;
end
endmodule
```

DATASHEETS

1.MOSFET DRIVER DATASHEET

FEATURES:

□□□Floating channel designed for bootstrap operation

2) Fully operational to +600V

3) □Tolerant to negative transient voltage

dV/dt immune

4) Gate drive supply range from 10 to 20V

5) 3.3V logic compatible

i. Separate logic supply range from 3.3V to 20V

ii. Logic and power ground ±5V offset

6) □CMOS Schmitt-triggered inputs with pull-down

7) Cycle by cycle edge-triggered shutdown logic

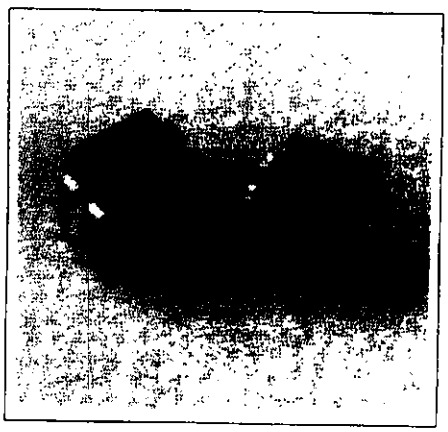
8) □Matched propagation delay for both channels

9) Outputs in phase with inputs

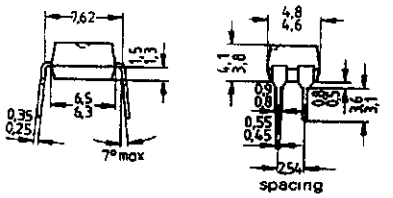
DESCRIPTION:

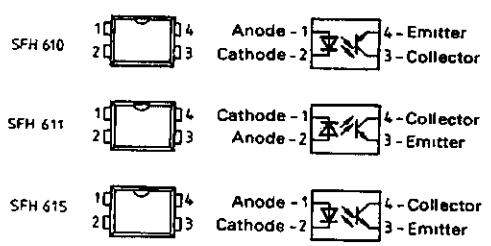
The IR2112(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volt.

2.SFH615OPTOCOUPLER:



Package Dimensions mm





FEATURES

- **Isolation Test Voltage: 2800 V**
- **High Current Transfer Ratios**
  at 10 mA: 40-320%
  at 1 mA: 60% typical (>13)
- **Fast Switching Times**
- **Minor CTR Degradation**
- **100% Burn-In**
- **Field-Effect Stable by TRIOS**
- **Temperature Stable**
- **Good CTR Linearity Depending on Forward Current**
- **High Collector-Emitter Voltage**
  V_{CEO}=70 V
- **Low Saturation Voltage**
- **Low Coupling Capacitance**
- **End-Stackable in 2.54 mm Spacing**
- **High Common-Mode Interference Immunity (Unconnected Base)**
- **UL Approval #52744**
- **VDE Approval 0883**
- **VDE Approval 0884 (Optional with Option 1)**

DESCRIPTION

The optically coupled isolators SFH 610, SFH 611 and SFH 615 a high current transfer ratio, low coupling capacitance and high isolation test voltage. They employ a GaAs LED as emitter, whicl optically coupled with a silicon planar phototransistor as detectc

The components are incorporated in a plastic plug-in DIP-4 pacl

The coupling devices are designed for signal transmission betw two electrically separated circuits. The potential difference betw circuits to be coupled is not allowed to exceed the maximum permissible reference voltages.

The couplers are end-stackable in a 2 54 mm spacing and are considered as successor types for the couplers in metal case. Tl SFH 610, SFH 611 and SFH 615 differ in their arrangement of the terminal pins. Multicouplers can thus easily be implemented and conventional multicouplers can be replaced.

*TRansparent IOn Shield

Maximum Ratings

Emitter (GaAs LED)

Reverse Voltage ..... 6 V
DC Forward Current ..... 60 mA
Surge Forward Current (t≤10 µs) ..... 2.5 A
Total Power Dissipation ..... 100 mW

Detector (Silicon Phototransistor)

Collector-Emitter Voltage ..... 70 V
Collector Current ..... 50 mA
Collector Current (t≤1 ms) ..... 100 mA
Total Power Dissipation ..... 150 mW

Optocoupler

Storage Temperature Range ..... -55°C to +150°C
Ambient Temperature Range ..... -55°C to +100°C
Junction Temperature ..... 100°C
Soldering Temperature (max. 10 s)[1] ..... 260°C
Isolation Test Voltage[2]
(between emitter and detector referred to standard climate 23/50 DIN 50014) ..... 2800 VDC
Isolation Resistance (V_{IO}=500 V) ..... 10^{11} Ω

Notes:

1 Dip soldering: minimum clearance from bottom edge of package 1.5 mm. Special soldering conditions apply when through-contacted circuit boards are used. Please request appropriate specification.
2 DC test voltage in accordance with DIN 57883, draft 4/78

Characteristics (T_A=25°C)

Emitter (GaAs LED)

Forward Voltage (I_F=60 mA)	V_F	1.25 (≤1.65)	V
Breakdown Voltage (I_R=10 µA)	V_{BR}	30 (≥6)	V
Reverse Current (V_R=6 V)	I_R	0.01 (≤10)	µA
Capacitance (V_R=0 V, f=1 MHz)	C_O	25	pF
Thermal Resistance	R_{thJA}	750	K/W

Detector (Silicon Phototransistor)

Capacitance (V_{CE}=5 V, f=1 MHz)	C_{CE}	6.8	pF
Thermal Resistance	R_{thJA}	500	K/W

Optocoupler

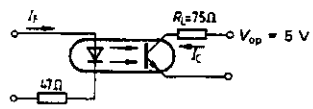
Collector-Emitter Saturation Voltage (I_F=10 mA, I_C=2.5 mA)	V_{CEsat}	0.25 (≤0.4)	V
Coupling Capacitance	C_K	0.25	pF

The optocouplers are grouped according to their current transfer ratio I_C/I_F at V_{CC}=5 V, marked by dash numbers

	–1	–2	–3	–4	
I_C/I_F (I_F=10 mA)	40–80	63–125	100–200	160–320	%
I_C/I_F (I_F=1 mA)	30 (>13)	45 (>22)	70 (>34)	90 (>56)	%
Collector-Emitter Leakage Current (V_{CE}=10 V) (I_{CEO})	2 (≤50)	2 (≤50)	5 (≤100)	5 (≤100)	nA

SWITCHING TIMES

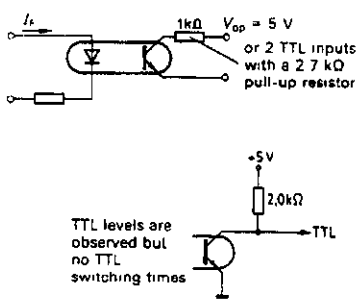
Linear Operation (without saturation)



I_F=10 mA, V_{OP}=5 V, T_A=25°C

Load Resistance	R_L	75	Ω
Turn-On Time	t_{ON}	3.0 (≤5.6)	µs
Rise Time	t_R	2.0 (≤4.0)	µs
Turn-Off Time	t_{OFF}	2.3 (≤4.1)	µs
Fall Time	t_F	2.0 (≤3.5)	µs
Cut-Off Frequency	F_{CO}	250	kHz

Switching Operation (with saturation)



Group	–1 (I_F=20 mA)	–2 and –3 (I_F=10 mA)	–4 (I_F=5 mA)	
Turn-On Time t_{ON}	3.0 (≤5.5)	4.2 (≤8.0)	6.0 (≤10.5)	µs
Rise Time t_R	2.0 (≤4.0)	3.0 (≤6.0)	4.6 (≤8.0)	µs
Turn-Off Time t_{OFF}	18 (≤34)	23 (≤39)	25 (≤43)	µs
Fall Time t_F	11 (≤20)	14 (≤24)	15 (≤26)	µs
V_{CEsat}	0.25 (≤0.4)			V