P-3426

FPGA BASED INVERTED SINE WAVE CARRIER PWM INVERTER FOR THD REDUCTION

A Project Report

Submitted by

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641 047

BONAFIDE CERTIFICATE

Certified that this project report entitled **"FPGA BASED INVERTED SINE WAVE CARRIER PWM INVERTER FOR THD REDUCTION"** is the bonafide work of

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ABSTRACT

Multilevel inverter is an effective and practical solution for increasing power and reducing harmonics of ac waveforms. Several multilevel topologies are reported and the most popular topology is Cascaded Multilevel Inverter (CMLI).

This project focuses on asymmetric cascaded multilevel inverter employing variable frequency inverted sine PWM technique (VFISPWM). This technique combines the advantage of inverted rectified sine wave and variable frequency carriers for a five level inverter for balancing the switch utilization.

A detailed study of the technique was carried out through MATLAB/SIMULINK for switching losses and THD.

The results were verified experimentally and FPGA processor is used for PWM. It was noticed that the proposed modulation strategy results in lower switching losses for a chosen THD as compared to the conventional strategies.

Keywords: Asymmetric Multilevel Inverter, ISPWM, Switching Loss.

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ABBREVIATION

SPWM	SINUSOIDAL PULSE WIDTH MODULATION
ISPWM	INVERTED SINUSOIDAL PULSE WIDTH MODULATION
MLI	MULTI LEVEL INVERTER
THD	TOTAL HARMONIC DISTORTION
AC	ALTERNATING CURRENT
DC	DIRECT CURRENT
IC	INTEGRATED CIRCUIT
GND	GROUND
FPGA	FIELD PROGRAMMABLE GATE ARRAY
RMS	ROOT MEAN SQUARE
MOSFET	METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
SPI	SERIAL PERIPHERAL INTERFACE
RAM	RANDOM ACCESS MEMORY
DDR	DOUBLE DATA RATE
PCI	PERIPHERAL COMPONENT INTERCONNECT
LVDS	LOW VOLTAGE DIFFERENTIAL SIGNALLING
RSDS	REDUCED SWING DIFFERENTIAL SIGNALLING
DSP	DIGITAL SIGNAL PROCESSING
IP	INTELLECTUAL PROPERTY
PC	PERSONAL COMPUTER
PDM	PULSE DURATION MODULATION

CHAPTER 1
INTRODUCTION

1.1. GENERAL

Multilevel inverters are mainly utilized to synthesize a desired voltage wave shape from several levels of dc voltages. Their main advantaged are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency capability to operate at high voltages and modularity.

Three topologies have been reported for multilevel inverters: Diode-clamped, flying capacitor and cascaded H-bridge. The topology considered for this work is the cascaded H bridge inverter which requires several independent dc sources. Normally, each phase of a cascaded multilevel inverter requires "n" dc sources for 2n+1 level.

For many applications, multiple dc sources are required demanding long cables and this could lead to voltage unbalance among the dc sources. With an aim to reduce the number of dc sources required for the cascaded multilevel inverter for a motor drive, this project focuses on asymmetric cascade MLI that uses two equal dc sources in each phase to generate a seven level equal step multilevel output.

This structure is favorable for high power applications since it provides higher voltage at higher modulation frequencies (where they are needed) with a low switching Implementation and Control of ISPWM Technique for an Asymmetric Multilevel Inverter (carrier) frequency. It means low switching loss for the same total harmonic distortion (THD). It also improves the reliability by reducing the number of dc sources. For the cascaded multilevel inverter there are several well known sinusoidal pulse width modulation strategies. Compared to the conventional triangular carrier based PWM, the inverted rectified sine carrier

PWM has a better spectral quality and a higher fundamental output voltage without any pulse dropping.

However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been suggested. This project however, presents a novel inverted rectified sine modulation technique (ISPWM) for a five level inverter. The ISPWM provides an enhanced fundamental voltage, lower total harmonic distortion (THD) and minimizes the switch utilization among the various levels in inverters. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The carrier frequencies are so selected that the number of switching in each band are equal. The proposed modulation technique maximizes the output voltage and gives a low THD of 29.00%.

A comparative evaluation between the ISPWM and the conventional modulation is also presented in terms of output voltage quality, power circuitry complexity, and total harmonic distortion (THD) and implementation cost. Both the MLI circuit topology and its new control scheme are described in detail and their performance is verified based on simulation and experimental results.

1.2. OBJECTIVE

To design and implement Inverted Sine Carrier PWM (ISCPWM) inverter for THD reduction, carry out comprehensive comparison with Sinusoidal PWM inverter and to obtain low switching losses.

1.3. ORGANISATION OF THE REPORT

This report has been organized into seven chapters.

Chapter 1: Gives introduction and the objective of the project and the way the various chapters are organized.

Chapter 2: Explains the conventional Sinusoidal PWM inverter (SPWM) with its SIMULINK model and Simulation results obtained.

Chapter 3: Explains the Inverted Sinusoidal PWM inverter (ISPWM) with its SIMULINK model and Simulation results obtained.

Chapter 4: Describes the hardware implementation of the project.

Chapter 5: Concludes the project with the scope for future work.

CHAPTER 2

CONVENTIONAL SINUSOIDAL PWM INVERTER

2.1. BLOCK DIAGRAM

Sinusoidal pulse width modulation is a method of pulse width modulation used in inverters. An inverter produces an AC output voltage from a DC input by using switching circuits to simulate a sine wave by producing one or more square pulses of voltage per half cycle. If the widths of the pulses are adjusted as a means of regulating the output voltage, the output is said to be pulse width modulated.

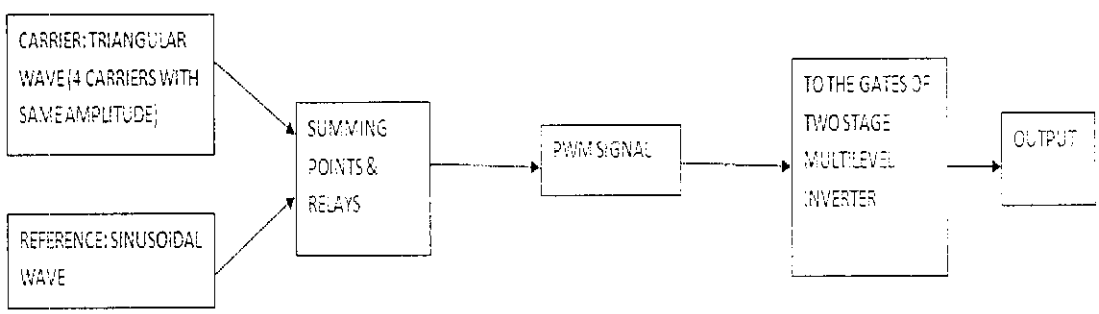

Fig 2.1 Block Diagram for SPWM Inverter

With sinusoidal or sine weighted pulse width modulation, several pulses are produced per half cycle. The pulses near the edges of the half cycle are always narrower than the pulses near the center of the half cycle such that the pulse widths are proportional to the corresponding amplitude of a sine wave at that portion of the cycle. To change the effective output voltage, the widths of all pulses are increased or decreased while maintaining the sinusoidal proportionality.

With pulse width modulation, only the widths (on-time) of the pulses are modulated. The amplitudes (voltage) during the "on-time" is constant unless a multi-step circuit is used. The line-to neutral voltage of a 3-phase inverter has two voltage levels.

2.2. SIMULINK MODEL

The cascaded five-level inverter is simulated using MATLAB/SIMULINK and switching signals are generated using function block by employing the sinusoidal modulation strategy. The simulation is carried out for fixed carrier frequency value of 4000Hz. The performance parameters considered for comparing the proposed PWM with the conventional method is the output voltage quality, THD, WTHD and switching loss.

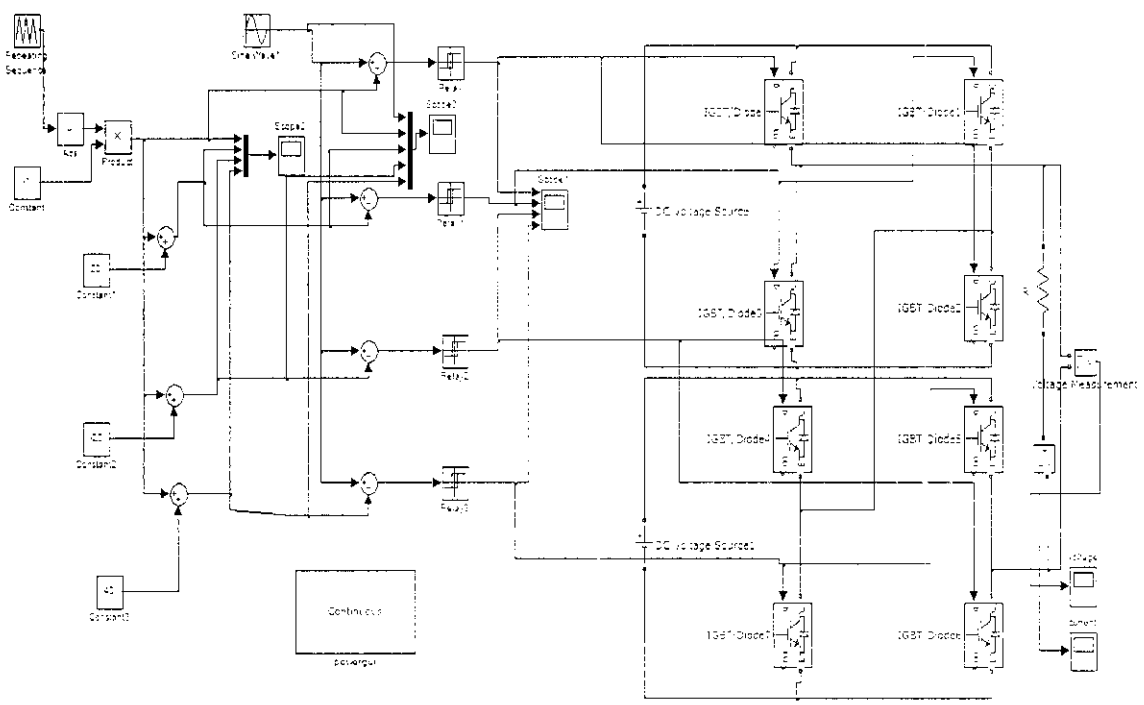

Fig 2.2 MATLAB Simulink Model for SPWM Inverter

Here four triangular carriers are generated with same amplitude. Those carriers are compared with a sine wave of frequency 50 Hz by relays. The relay outputs the PWM signals. Then these signals are carried out to the gates of the MOSFETs/ IGBTs. The carrier waveform and output wave form is shown below.

2.3. SIMULATION RESULTS

2.3.1. CARRIER WAVEFORM

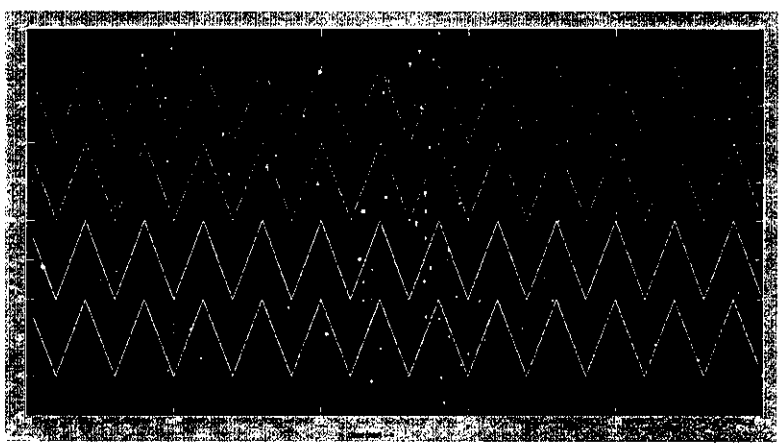

Fig 2.3 Triangular Carrier Signals.

The carrier frequencies are so selected that the number of switching in each band are equal. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been suggested. The triangular carriers have amplitude of 20volts each. The reference sine wave frequency is (2*pi*50Hz). Then the respective PWM signals obtained are taken to gates of the MOSFETs.

2.3.1. VOLTAGE WAVEFORM

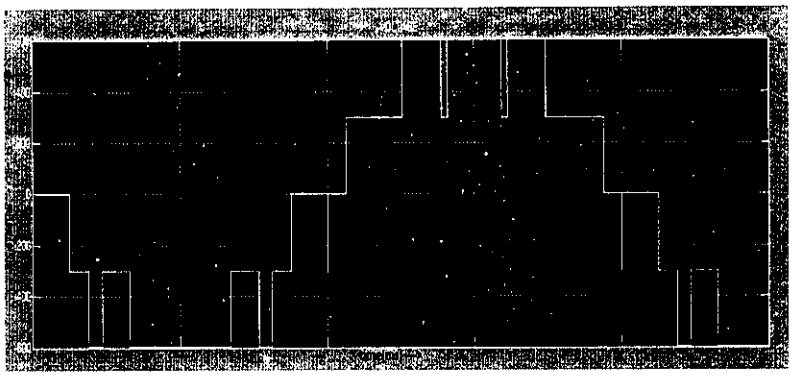

Fig 2.4 Output Waveform for SPWM Inverter

As it can be seen, the SPWM technique has some THD and the phase voltage waveform shows that the top and bottom level has high number of switching compared to the proposed ISPWM.

2.3.3. THD VALUE OBTAINED

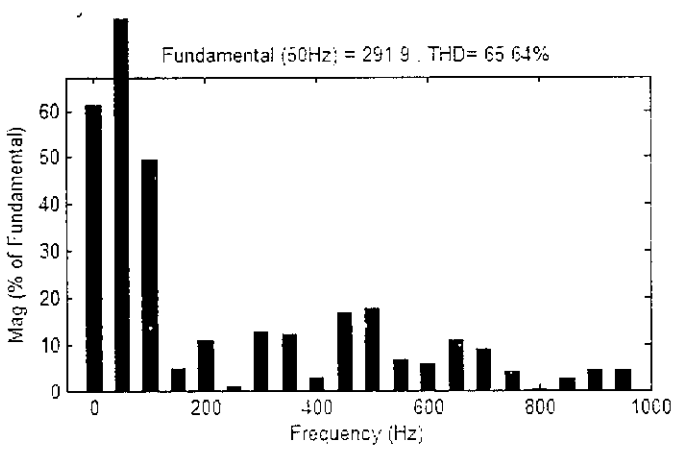

Fig 2.5 THD Waveform for SPWM Inverter

A detailed study of the technique was carried out through MATLAB/SIMULINK for switching losses and THD. The total harmonic distortion obtained from the MATLAB simulation is 65.64%.

CHAPTER 3

INVERTED SINUSOIDAL PWM INVERTER

3.1. BLOCK DIAGRAM

The inverted sine carrier PWM (ISCPWM) method uses a sinusoidal reference signal and an inverted sine carrier which has better spectral quality and higher output limit as compared to the conventional sinusoidal PWM (SPWM), without any pulse dropping.

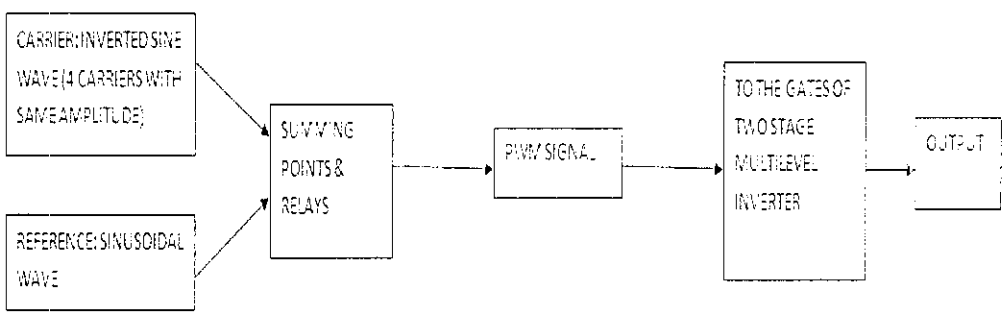

Fig 3.1 Block Diagram for ISCPWM Inverter

The ISCPWM strategy reduces the total harmonic distortion (THD) without hampering device switching losses. It also enhances the fundamental output voltage particularly at lower modulation index.

3.2. SIMULINK MODEL

The cascaded five-level inverter is simulated using MATLAB/SIMULINK and switching signals are generated using function block by employing the proposed Inverted Sinusoidal Pulse Width Modulation strategy. The simulation is carried out for fixed carrier frequency value of 4000Hz. The performance parameters

considered for comparing the proposed PWM with the conventional method is the output voltage quality, THD, WTHD and switching loss,

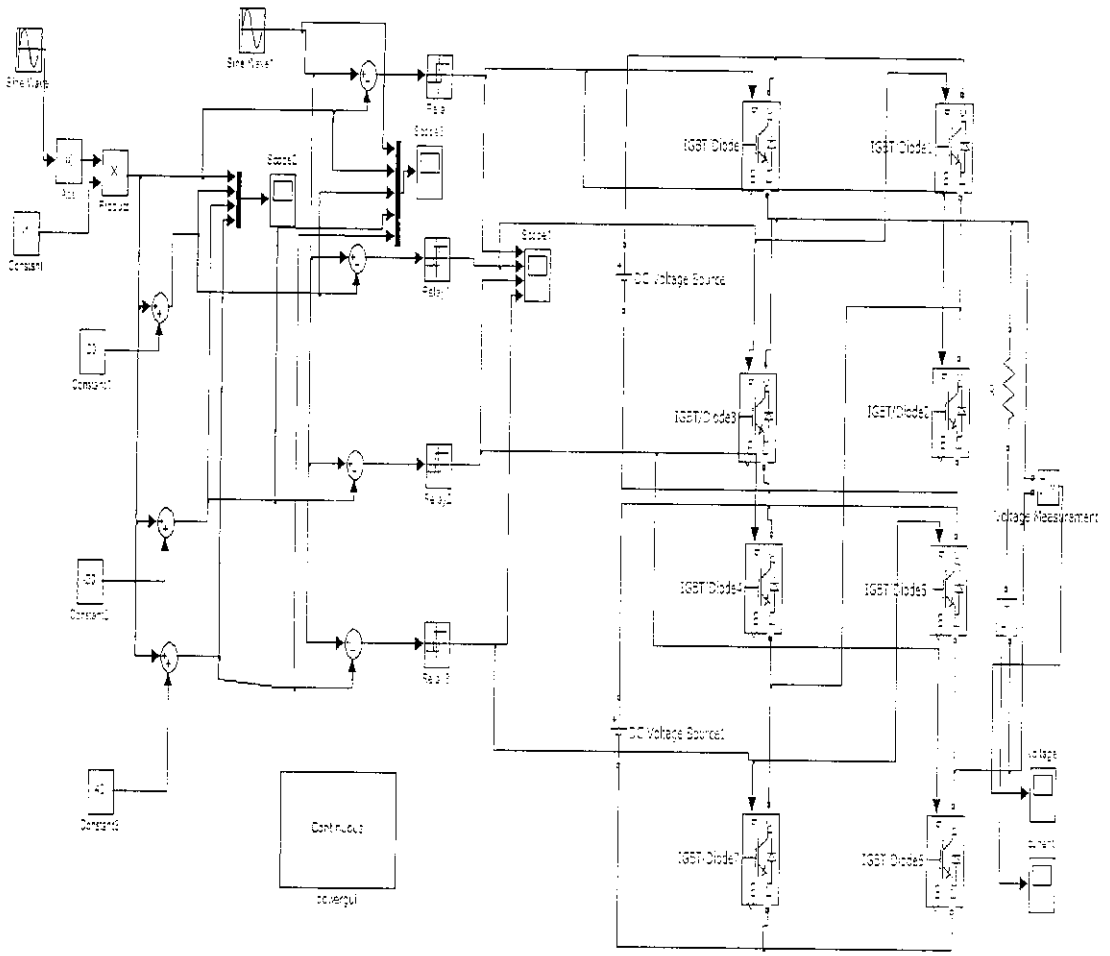

Fig 3.2 MATLAB Simulink Model for ISCPWM Inverter

Here four inverted sine carriers are generated with same amplitude. Those carriers are compared with a sine wave of frequency 50 Hz by relays. The relay outputs the PWM signals. Then these signals are carried out to the gates of the MOSFETs/ IGBTs. The carrier waveform and output wave form is shown below.

3.3. SIMULATION RESULTS

3.3.1. CARRIER WAVEFORM

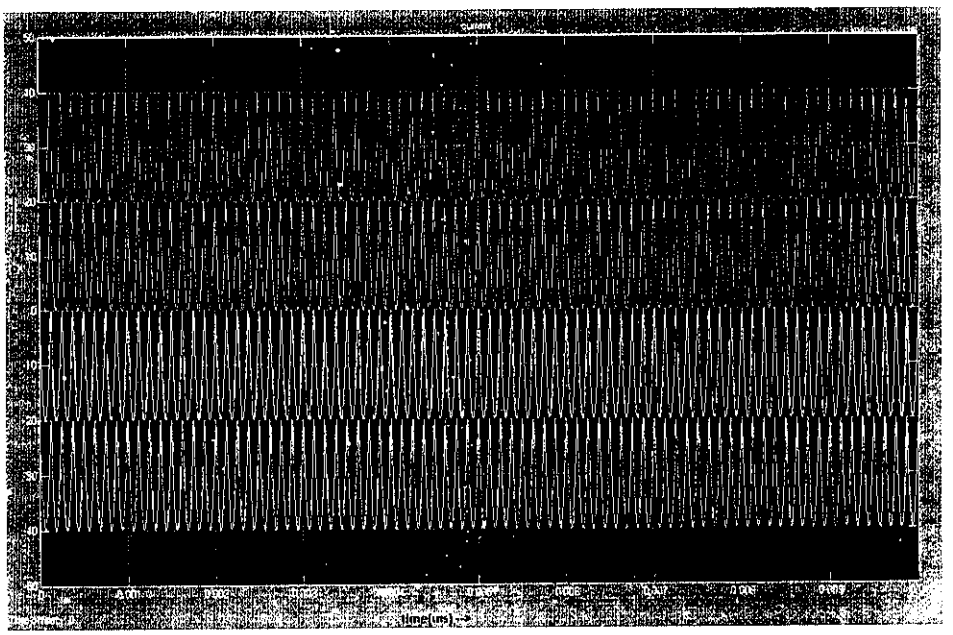

Fig 3.3 Four Inverted Sine Carriers.

The carrier frequencies are so selected that the number of switching in each band are equal. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been suggested. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The triangular carriers have amplitude of 20volts each. The reference sine wave frequency is (2*pi*50Hz). Then the respective PWM signals obtained are taken to gates of the MOSFETs.

3.3.2. VOLTAGE WAVEFORM

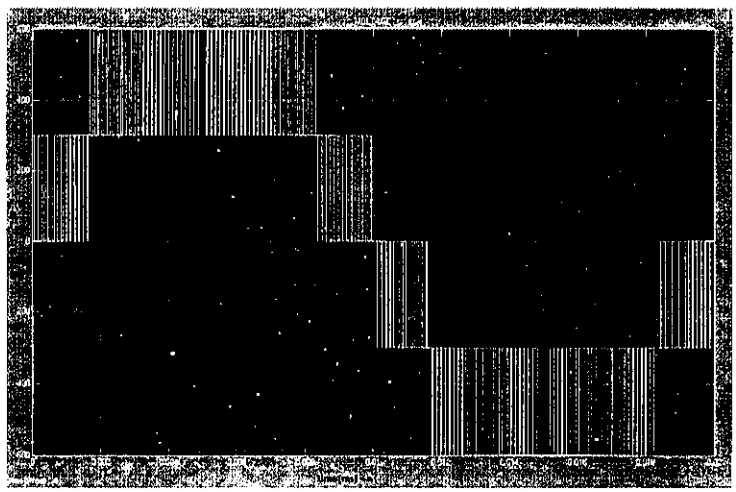

Fig 3.4 Output Waveform for ISCPWM Inverter

As it can be seen, the proposed ISPWM technique has always lower THD and the phase voltage waveform shows that the top and bottom levels has less number of switching compared to the conventional ISPWM.

3.3.3. THD VALUE OBTAINED

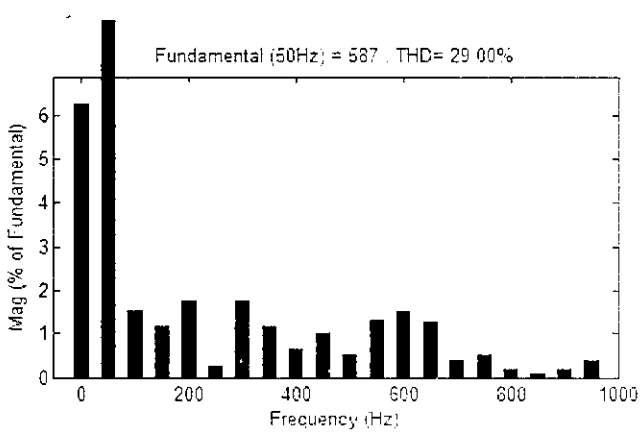

Fig 3.5 THD Waveform for ISCPWM Inverter

A detailed study of the technique was carried out through MATLAB/SIMULINK for switching losses and THD. An inverted sine wave

carrier frequency modulation strategy gives maximum fundamental voltage for a given THD. The total harmonic distortion obtained from the MATLAB simulation is **29.00%**.

3.4. CHOOSING ISPWM OVER SPWM

ISPWM has the following advantages over the conventional SPWM

1. Enhances the fundamental output voltage keeping THD value low.
2. Eliminates
    - the poor spectral quality of the output voltage.
    - The poor performance with regard to maximum output voltage.
3. High speed capability.
4. Low switching loss.

3.5. THD VALUES OBTAINED

CONVENTIONAL SINUSOIDAL PWM INVERTER	INVERTED SINE CARRIER PWM INVERTER
THD = 65.64%	THD = 29.00%

CHAPTER 4

HARDWARE DESCRIPTION

4.1. OVERALL BLOCK DIAGRAM

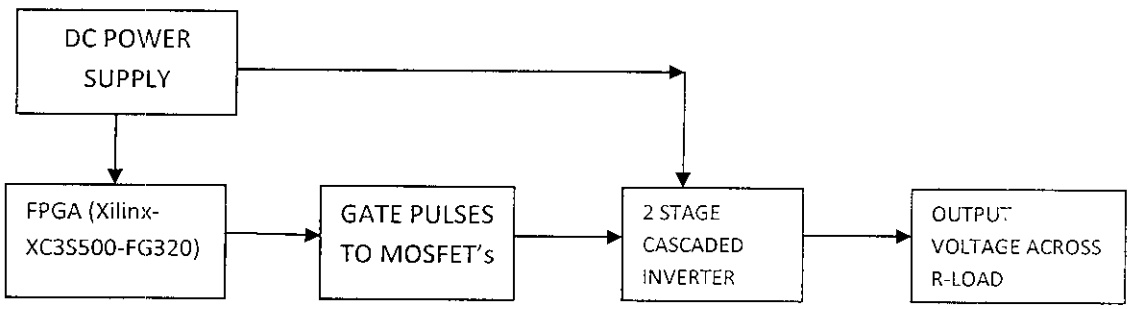

Fig 4.1 Overall Block Diagram

4.2. POWER SUPPLY CIRCUIT

Since all electronic circuits work only with low D.C. voltage we need a power supply unit to provide the appropriate voltage supply. This unit consists of transformer, rectifier, filter and regulator. A.C. voltage typically 230V rms is connected to a transformer which steps that AC voltage down to the level to the desired AC voltage. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple or AC voltage variations. regulator circuit can use this DC input to provide DC voltage that not only has much less ripple voltage but also remains the same DC value even the DC voltage varies somewhat, or the load connected to the output DC voltage changes. The power supply unit is a source of constant DC supply voltage. The required DC supply is obtained from the available AC supply after rectification, filtration and regulation.

4.2.1. TRANSFORMER

Here a step down transformer is used which steps down the voltage from 230V to 9V AC. Then the secondary of the transformer is connected to the precision rectifier, which is constructed with the help of op-amp. The advantages of using precision rectifier are it will give peak voltage output as DC, rest of the circuits will give only RMS output.

4.2.2. BRIDGE RECTIFIER

When four diodes are connected as shown in figure 4-8, the circuit is called a BRIDGE RECTIFIER. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners.

Let us assume the transformer is working properly and there is a positive potential at point A and a negative potential at point B. The positive potential at point A will forward bias D3 and reverse bias D4.

The negative potential at point B will forward bias D1 and reverse bias D2. At this time D3 and D1 are forward biased and will allow current flow to pass through them; D4 and D2 are reverse biased and will block current flow.

The path for current flow is from point B through D1, up through R_L, through D3, through the secondary of the transformer back to point B. This path is indicated by the solid arrows. Waveforms (1) and (2) can be observed across D1 and D3.

One-half cycle later the polarity across the secondary of the transformer reverses, forward biasing D2 and D4 and reverse biasing D1 and D3. Current flow will now be from point A through D4, up through R_L, through D2, through the secondary of T1, and back to point A. This path is indicated by the broken arrows.

Waveforms (3) and (4) can be observed across D2 and D4. You should have noted that the current flow through R_L is always in the same direction. In flowing through R_L this current develops a voltage corresponding to that shown in waveform (5). Since current flows through the load (R_L) during both half cycles of the applied voltage, this bridge rectifier is a full-wave rectifier.

One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit.

This may be shown by assigning values to some of the components shown in views A and B. Assume that the same transformer is used in both circuits. The peak voltage developed between points X and Y is 1000 volts in both circuits. In the conventional full-wave circuit shown in view A, the peak voltage from the center tap to either X or Y is 500 volts. Since only one diode can conduct at any instant, the maximum voltage that can be rectified at any instant is 500 volts. The maximum voltage that appears across the load resistor is nearly - but never exceeds 500 volts, as a result of the small voltage drop across the diode. In the bridge rectifier shown in view B, the maximum voltage that can be rectified is the full secondary voltage, which is 1000 volts. Therefore, the peak output voltage across the load resistor is nearly 1000 volts. With both circuits using the same transformer, the bridge rectifier circuit produces a higher output voltage than the conventional full-wave rectifier circuit.

4.2.3. IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device and

overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustable set voltage.

A power supply can be built using a transformer connected to the AC supply line to step the AC voltage to desired amplitude, then rectifying that AC voltage, filtering with a capacitor and a RC filter.

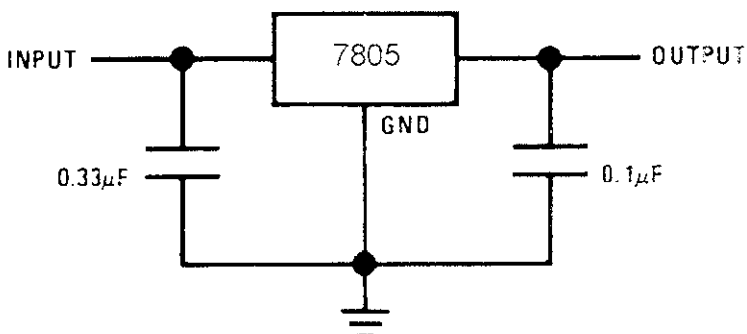

Fig 4.2. Fixed Positive Voltage Regulator

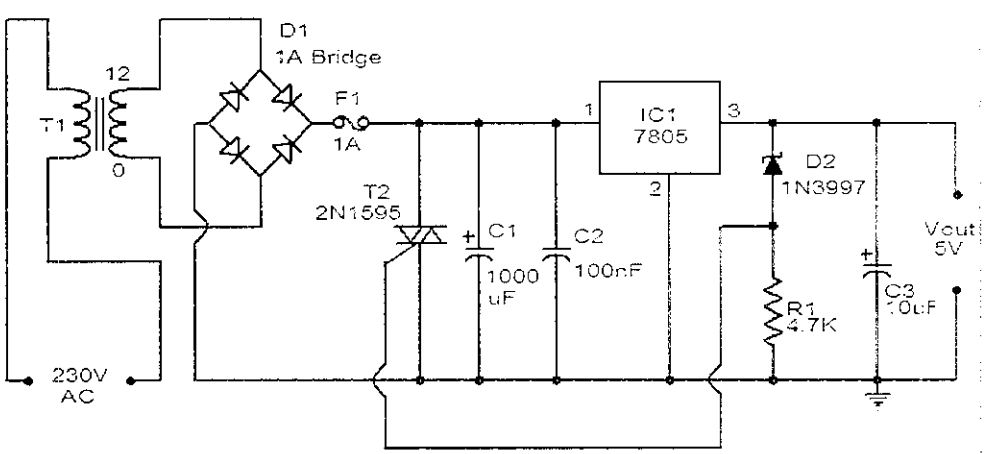

Fig 4.3 - Power Supply Circuit Diagram

The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

4.3. FPGA

Xilinx Spartan 3E FPGA IC is used for controlling the width of the pulses from PWM generator, by fixing either the frequency or voltage so that the MOSFET's are turned ON and OFF in the desired sequence.

- Ability to re-program in the field to fix bugs.
- Small size and increased speed.
- The inherent parallelism of the logic resources on an FPGA allows for considerable computational throughput even at a low MHz clock rates.

The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units.

4.3.1. FEATURES

The Spartan-3E family reduces system cost by offering the lowest cost-per-logic of any FPGA family, supporting the lowest-cost configuration solutions including commodity serial (SPI) and parallel flash memories, and efficiently integrating the functions of many chips into a single FPGA.

- Five devices with 100K to 1.6M system gates
- From 66 to 376 I/Os with package and density migration
- Up to 648 Kbits of block RAM and up to 231 Kbits of distributed RAM

• Up to 36 embedded 18x18 multipliers for high-performance DSP applications

• Up to eight Digital Clock Managers

• Support for Xilinx Platform Flash as well as commodity serial (SPI) and byte-wide flash

memory for configuration

• Easy-to-implement interfaces to DDR memory

• Support for 18 common I/O standards, including PCI 33/66, PCI-X, mini-LVDS, and RSDS

• ISE design tools to shorten design and verification time

• Hundreds of pre-verified, pre-optimized Intellectual Property (IP) cores and reference designs

• Includes XC3S500E FPGA, SPI Flash, 32Mb DDR memory and support for USB2.0

4.3.2. SPARTAN 3E –Xilinx (XC3S500-FG320) KIT BLOCK DIAGRAM:

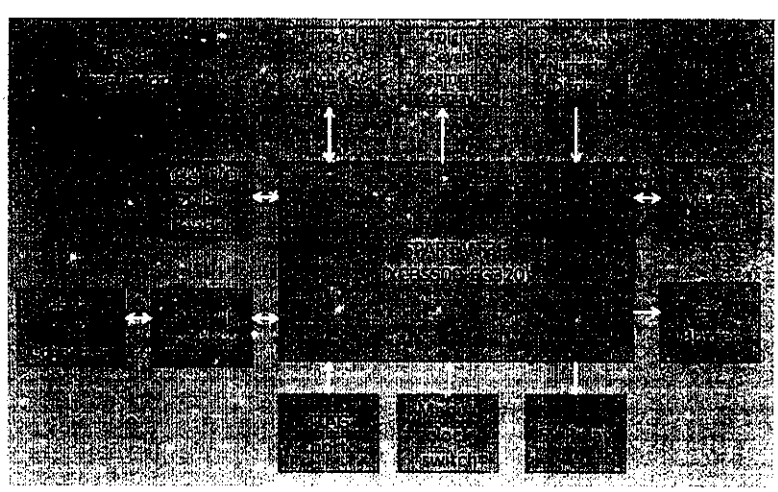

Fig 4.4 Spartan 3E –Xilinx (XC3S500-FG320) Kit Block Diagram

4.4. Pulse Width Modulation

Pulse-width modulation (PWM), or **pulse-duration modulation (PDM)**, is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is.

The PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power. Typically switching have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

The term *duty cycle* describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

4.4.1. Sinusoidal Pulse width Modulation

Sinusoidal pulse width modulation is a method of pulse width modulation used in inverters. An inverter produces an AC output voltage from a DC input by using switching circuits to simulate a sine wave by producing one or more square pulses of voltage per half cycle. If the widths of the pulses are adjusted as a means of regulating the output voltage, the output is said to be pulse width modulated.

With sinusoidal or sine weighted pulse width modulation, several pulses are produced per half cycle. The pulses near the edges of the half cycle are always narrower than the pulses near the center of the half cycle such that the pulse widths are proportional to the corresponding amplitude of a sine wave at that portion of the cycle. To change the effective output voltage, the widths of all pulses are increased or decreased while maintaining the sinusoidal proportionality.

With pulse width modulation, only the widths (on-time) of the pulses are modulated. The amplitudes (voltage) during the "on-time" is constant unless a multi-step circuit is used. The line-to neutral voltage of a 3-phase inverter has two voltage levels.

The advantages of this conventional sinusoidal PWM topology are:

- Reduced number of dc sources
- Low output switching frequency
- Low switching losses
- High conversion efficiency
- Flexibility to enhance

4.4.2. Proposed Inverted Sinusoidal Pulse Width Modulation

The inverted sine carrier PWM (ISCPWM) method uses a sinusoidal reference signal and an inverted sine carrier which has better spectral quality and higher output limit as compared to the conventional sinusoidal PWM (SPWM), without any pulse dropping.

The ISCPWM strategy reduces the total harmonic distortion (THD) without hampering device switching losses. It also enhances the fundamental output voltage particularly at lower modulation index.

Enhanced fundamental component demands greater pulse area. The difference in pulse widths (hence area) resulting from triangle wave and inverted sine wave with the low (output) frequency reference sine wave in different sections can be easily understood.

In the gating pulse generation of the proposed ISCPWM scheme, the triangular carrier waveform of SPWM is replaced by an inverter sine waveform. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM. For the ISCPWM pulse pattern, the switching angles may be computed as the same way as SPWM scheme.

The equation of inverted sine wave is given for its odd and even cycles respectively. But the main drawback is the marginal boost in the magnitude of lower order harmonics and unbalanced switch utilization. This is overcome by employing variable frequency inverted sine carrier signals.

4.5. EXPERIMENTAL SET-UP

FPGA belongs to the wide family of programmable logic components. Their densities are now exceeding 10 million gates. The architecture is composed of a matrix of CLB, which is bordered by a ring of configurable input/output blocks (IOB). All these resources communicate among themselves through a

programmable interconnection network and also fit to PWM signal, where it is subjected into certain hardware-oriented constraints. The algorithm uses the LUT for the sine reference and triangular/inverter sine carrier functions.

The system (board) clock is divided and adjusted with the data count in LUT's. The carrier data is repeatedly called for Mf times recursively and compared with the sine reference data based on TRR algorithm. When the reference is greater than the carrier data, a pulse will be produced.

The target technology uses one of the Xilinx series of FPGA. The circuit has been designed using VHDL, synthesized, placed and routed using the Xilinx integrated service environment. The functionality of the final net list/design verification for the pulse generation has been completed using ModelSim SEEE5.4e simulator in project navigator.

After verifying the design by simulation, synthesis is carried out. Finally placement, routing and timing optimizations are performed. The target technology uses one of the Xilinx series of FPGA. The circuit has been designed using VHDL, synthesized, placed and routed using the Xilinx integrated service environment.

A proto-type inverter has been constructed using IRF840 MOSFET. Both SPWM and ISCPWM modulators have been tested with the help of a SRAM-FPGA based Xilinx family spartan-3E XC3S500-FG320.

The XC3S500-FG320 has 400K logic gates, logic cells 8064, CLB is 896, distributed RAM bits 56K, and maximum user input/output is 264. The target technology uses one of the Xilinx series of FPGA. The representative downloaded pulses are captured using fluke scope (199C series) and are shown in Fig.

Fig 4.5.1 FPGA Kit Is Programmed With Xilinx ISE Tool

Here the Spartan 3E (XC3S500-FG320) is used. This kit is programmed through Xilinx ISE tool via PC through IMPACT port. The respective program coding for the generation of pulses is given in the Appendix A. The XC3S500-FG320 has 400K logic gates, logic cells 8064, CLB is 896, distributed RAM bits 56K, and maximum user input/output. The target technology uses one of the Xilinx series of FPGA. The circuit has been designed using VHDL, synthesized, placed and routed using the Xilinx integrated service environment.

After programming the kit switch on the inverter supply and note the waveforms. . The XC3S500-FG320 has 400K logic gates, logic cells 8064, CLB is 896, distributed RAM bits 56K, and maximum user input/output is 264. The representative downloaded pulses are captured using fluke scope (199C series).

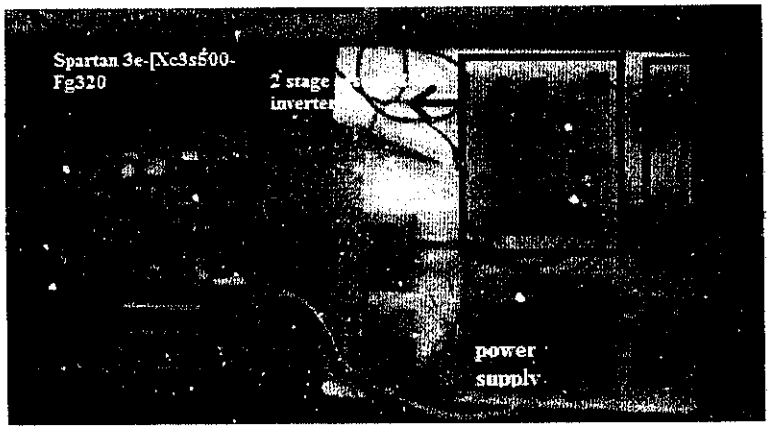

Fig 4.5.2 FPGA Kit (Spartan 3E-[XC3S500-FG320]) And Two Stage Cascaded Inverter.

After verifying the design by simulation, synthesis is carried out. Finally placement, routing and timing optimizations are performed. A proto-type inverter has been constructed using IRF840 MOSFET.

Both SPWM and ISCPWM modulators have been tested with the help of a SRAM-FPGA based Xilinx family spartan-3E XC3S500-FG320.

As per the program downloaded in the Spartan 3E-(XC3S500-FG320), it creates the gate signals for the MOSFETs used in the two stage cascaded inverter.

A proto-type inverter has been constructed using IRF840 MOSFET. Both SPWM and ISCPWM modulators have been tested with the help of a SRAM-FPGA based Xilinx family spartan-3E XC3S500-FG320.

If the gate pulses are given, the respective output is obtained as shown in the figure 4.6.1.

4.6. HARDWARE RESULTS

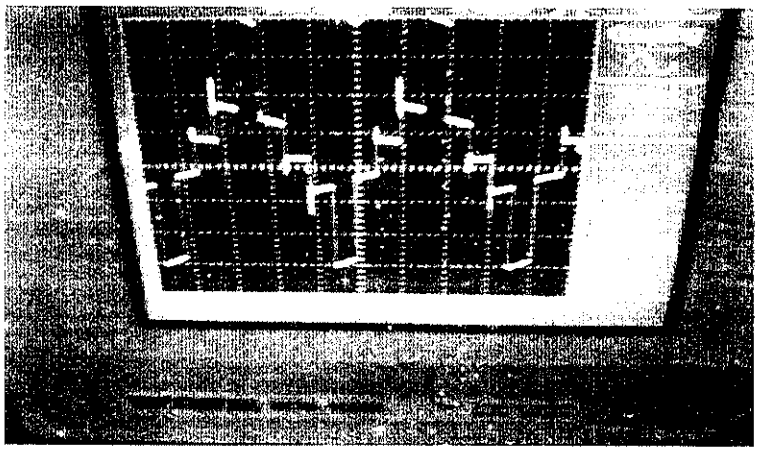

Fig 4.6.1 Output Voltage Waveform for Inverter Sine Wave Carrier PWM Inverter

SCALE: X-axis = time (ms); Y-axis = voltage (volts);

The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater pulse area. Thus, five level inverted waveforms are obtained from Digital Storage Oscilloscope as shown in the figure 4.6.1.

CHAPTER 5

CONCLUSION AND SCOPE

5.1. CONCLUSION

Asymmetric cascaded multilevel inverter using two unequal dc sources for each phase requires minimum number of switching devices. An inverted sine wave carrier frequency modulation strategy gives maximum fundamental voltage for a given THD. A variable frequency carrier modulation strategy results in reduced switching losses. Advantages of all the above three methods have been exploited in the proposed technique. The PI controller is tested for regulating output voltage and minimizing harmonics of the chosen five level inverter. The proposed system has lower THD and lower switching loss as compared to that of conventional multilevel inverter.

5.2. SCOPE FOR FUTURE

Switching losses and THD are also lower compared to the conventional PWM technique. This project also employs asymmetrical DC sources which reduces the number of bridges used thus decreasing the complexity and the cost of the circuit. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the dc voltage levels. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced. The proposed modulation strategy of the multilevel inverter with fuel cell in place of dc sources has a greater scope in applications involving electrical vehicles.

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APPENDIX A

VERILOG CODING FOR INVERTED SINE PWM PULSES:

```
module pulse(clk,rst,rb0,rb1,rb2,rb3,rb4,rb5,rb6,rb7);

  input clk,rst;

  output rb0,rb1,rb2,rb3,rb4,rb5,rb6,rb7;

  reg rb0,rb1,rb2,rb3,rb4,rb5,rb6,rb7;

  reg [7:0]count;


  always@(posedge clk or negedge rst)

  begin

    if(!rst)

    begin

      count<=8'd0;

      rb0<=0;

      rb1<=0;

      rb2<=0;

      rb3<=0;

      rb4<=0;

      rb5<=0;

      rb6<=0;
```

```
    rb7<=0;
end
else
begin
    count<=count+1;
    case(count)
        8'd0:begin
            rb0<=1;
            rb1<=1;
            rb2<=1;
            rb3<=1;
            rb4<=1;
            rb5<=0;
            rb6<=1;
            rb7<=0;
        end

            8'd1:begin
            rb0<=1;
```

```
rb1<=1;

rb2<=1;

rb3<=1;

rb4<=1;

rb5<=0;

rb6<=1;

rb7<=0;

 end


 8'd2:begin

rb0<=1;

rb1<=1;

rb2<=1;

rb3<=1;

rb4<=1;

rb5<=0;

rb6<=1;

rb7<=0;

 end
```

```
 8'd3:begin
rb0<=1;
rb1<=1;
rb2<=1;
rb3<=1;
rb4<=1;
rb5<=0;
rb6<=1;
rb7<=0;
 end

 8'd4:begin
rb0<=1;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
```

```
rb6<=1;

rb7<=0;

 end


 8'd5:begin

rb0<=1;

rb1<=1;

rb2<=0;

rb3<=1;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=0;

 end


 8'd6:begin

rb0<=0;

rb1<=1;
```

```
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=1;
rb7<=1;
 end

 8'd7:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=1;
rb7<=1;
 end
```

```
 8'd8:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=1;
rb7<=1;
 end

 8'd9:begin
rb0<=1;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=0;
```

```
rb7<=1;
 end

 8'd10:begin
rb0<=1;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=0;
rb7<=1;
 end

 8'd11:begin
rb0<=1;
rb1<=1;
rb2<=1;
rb3<=1;
```

```
rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd12:begin

rb0<=1;

rb1<=1;

rb2<=1;

rb3<=1;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd13:begin

rb0<=1;
```

```
rb1<=1;

rb2<=1;

rb3<=1;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd14:begin

rb0<=1;

rb1<=1;

rb2<=1;

rb3<=0;

rb4<=1;

rb5<=1;

rb6<=0;

rb7<=1;

 end
```

```
 8'd15:begin
rb0<=1;
rb1<=1;
rb2<=1;
rb3<=0;
rb4<=1;
rb5<=1;
rb6<=0;
rb7<=1;
 end

 8'd16:begin
rb0<=1;
rb1<=0;
rb2<=1;
rb3<=0;
rb4<=1;
rb5<=1;
```

```
rb6<=0;

rb7<=1;

 end


 8'd17:begin

rb0<=1;

rb1<=0;

rb2<=1;

rb3<=0;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=1;

 end


 8'd18:begin

rb0<=1;

rb1<=0;

rb2<=1;
```

```
rb3<=0;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=1;

 end


 8'd19:begin

rb0<=1;

rb1<=1;

rb2<=1;

rb3<=0;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=0;

 end


 8'd20:begin
```

```
rb0<=1;

rb1<=1;

rb2<=1;

rb3<=0;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=0;

 end


 8'd21:begin

rb0<=1;

rb1<=1;

rb2<=1;

rb3<=1;

rb4<=1;

rb5<=0;

rb6<=1;

rb7<=0;
```

```
end

8'd22:begin
rb0<=1;
rb1<=1;
rb2<=1;
rb3<=1;
rb4<=1;
rb5<=0;
rb6<=1;
rb7<=0;
end

8'd23:begin
rb0<=1;
rb1<=1;
rb2<=1;
rb3<=1;
rb4<=1;
```

```
rb5<=0;
rb6<=1;
rb7<=0;
 end

 8'd24:begin
rb0<=1;
rb1<=1;
rb2<=1;
rb3<=1;
rb4<=1;
rb5<=0;
rb6<=1;
rb7<=0;
 end

 8'd25:begin
rb0<=1;
rb1<=1;
```

```
rb2<=0;

rb3<=1;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=0;

 end


 8'd26:begin

rb0<=1;

rb1<=1;

rb2<=0;

rb3<=1;

rb4<=1;

rb5<=1;

rb6<=1;

rb7<=0;

 end
```

```
 8'd27:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=1;
rb7<=1;
 end

 8'd28:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=1;
```

```
rb7<=1;
 end

 8'd29:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=1;
rb5<=1;
rb6<=0;
rb7<=1;
 end

 8'd30:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
```

```
rb4<=1;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd31:begin

rb0<=0;

rb1<=1;

rb2<=0;

rb3<=1;

rb4<=1;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd32:begin

rb0<=0;
```

```
rb1<=1;

rb2<=0;

rb3<=1;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd33:begin

rb0<=0;

rb1<=1;

rb2<=0;

rb3<=1;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end
```

```
 8'd34:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=1;
rb4<=0;
rb5<=1;
rb6<=0;
rb7<=1;
 end

 8'd35:begin
rb0<=0;
rb1<=1;
rb2<=0;
rb3<=0;
rb4<=0;
rb5<=1;
```

```
rb6<=0;

rb7<=1;

 end


 8'd36:begin

rb0<=0;

rb1<=1;

rb2<=0;

rb3<=0;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd37:begin

rb0<=0;

rb1<=0;

rb2<=0;
```

```
rb3<=0;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd38:begin

rb0<=0;

rb1<=0;

rb2<=0;

rb3<=0;

rb4<=0;

rb5<=1;

rb6<=0;

rb7<=1;

 end


 8'd39:begin
```

APPENDIX C

FPGA- Xilinx Spartan 3E-FG320 DATASHEET

Component	Substance Description	CAS# or Description	% of Component	Use in Product	Component Weight/ Substance Weight (in grams)	Component % of Total
Silicon Die					0.0535	4.27%
	Silicon	7440-21-3	[illegible]		0.0535	
Die Attach Material					0.0057	0.45%
	Silver	7440-22-4	[illegible]		0.0044	
	Resin	Trade Secret	[illegible]		0.0013	
Mold Compound					0.5856	46.76%
	Epoxy Resins	Trade Secret	[illegible]		0.0703	
	SiO2	60676-86-0	[illegible]	Filler	0.5153	
Laminate					0.2586	20.65%
	Laminate	Trade Secret	[illegible]		0.1586	
	Solder Mask	Trade Secret	[illegible]		0.0492	
	Copper	7440-50-8	[illegible]	Metal Layer	0.0417	
	Nickel	7440-02-0	[illegible]	Metal Layer	0.0111	
	Gold	7440-57-5	[illegible]	Metal Layer	0.0029	
Bond Wire					0.0104	0.83%
	Gold	7440-57-5	[illegible]		0.010297129	
	Silver	7440-22-4	[illegible]		0.000000263	
	Copper	7440-50-8	[illegible]		0.00000052	
	Iron	7439-89-6	[illegible]		0.00000052	
	Calcium	7440-70-2	[illegible]		0.000000263	
	Palladium	7440-05-3	[illegible]		0.000102871	
	Magnesium	7439-95-4	[illegible]		0.00000052	
Solder Balls					0.3366	27.03%
	Tin	7440-31-5	[illegible]		0.3234	
	Silver	7440-22-4	[illegible]		0.0095	
	Copper	7440-50-8	[illegible]		0.0037	