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ADVANCED MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

A PROJECT REPORT

Submitted by

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Under the guidance of

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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APRIL 2011

BONAFIDE CERTIFICATE

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ABSTRACT

The multilevel inverter is a recent new development in the field of power electronics. The use of the multilevel inverters results in improved power quality. But the number of power semiconductor switches used in the multilevel inverters is very large. This increases the cost of employing these multilevel inverters in electrical drives. So there is a need for reducing the switch count.

Here a new topology of multilevel inverter is used where the multilevel output is obtained by using the minimum number of switches. Here the output can be obtained for any number of levels by increasing the number of sources or capacitors. With the number of switches reduced, this multilevel inverter also gives better a power quality than a normal conventional inverter.

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CHAPTER

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Solid-state inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries.

They are of two types

1. Single phase inverters
2. Three phase inverters

1.2 A LITERATURE SURVEY ON INVERTERS

As per literature these are different types of inverters existing in the current system. The general description of widely used inverters is explained below.

HALF BRIDGE INVERTERS:

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three phase ac systems. A half-bridge is the simplest topology, which is used to produce a two level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig. 1.1 and 1.3, respectively.

A single-phase half-bridge inverter, only two switches are needed. To avoid shoot-through fault, both switches are never turned on at the same time. S1 is turned on and S2 is turned off to give a load voltage, *AO V* in Fig. 1.1, of / 2 *s* +*V*. To complete one cycle, S1 is turned off and S2 is turned on to give a load voltage, *AO V*, of / 2 *s* -*V*. In full bridge configuration, turning on S1 and S4 and turning off S2 and S3 give a voltage of *VS* between point A and B (AB *V*) in Fig. 1.1, while turning off S1 and S4 and turning on S2 and S3 give a voltage of -*Vs*.

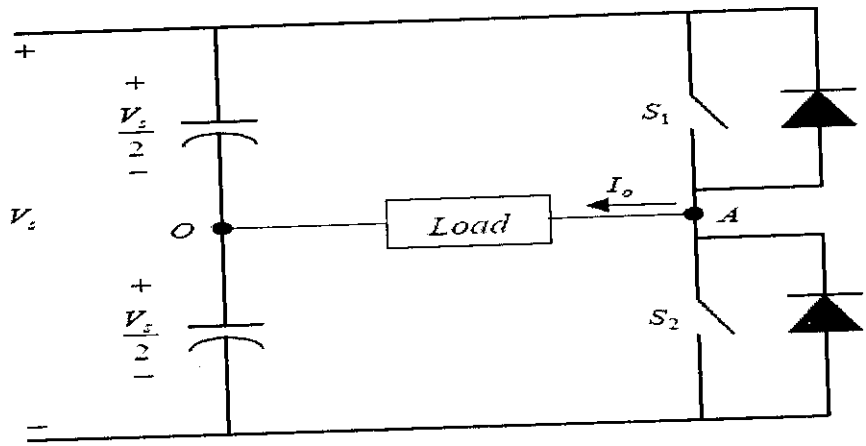


Fig 1.1. Half bridge inverter

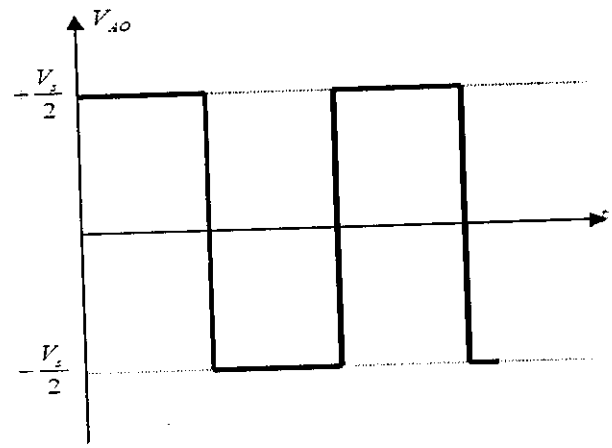


Fig 1.2. Output waveform of half bridge

FULL BRIDGE INVERTER:

The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Fig. 1.3. The inverter circuit consists of four main switches and four freewheeling diodes.

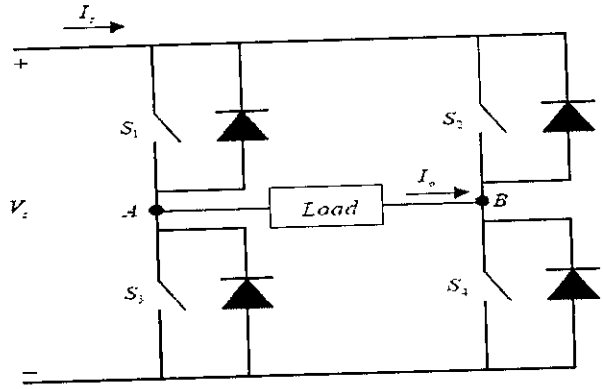


Fig 1.3. Full bridge configuration

To generate zero level in a full-bridge inverter, the combination can be S1 and S2 on while S3 and S4 off or vice versa. The three possible levels referring to above discussion are shown in Table 1.1.

Table 1.1. Possible levels of switches

Conducting Switches	Load Voltage V_{AB}
S_1, S_4	$+V_s$
S_2, S_3	$-V_s$
S_1, S_2 or S_3, S_4	0

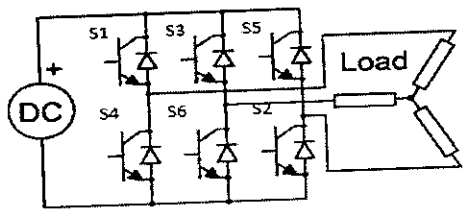


Fig 1.5 Three phase inverter

MODES OF CONDUCTION

A three phase output can be obtained from a configuration of six transistors and six diodes as shown in fig. Two types of control signals can be applied to transistors

- 180 degree conduction
- 120 degree conduction

180 degree conduction:

In this mode each transistor conducts for 180 degrees. Three transistors remain on at any instant of time. When S1 is switched on, terminal a is connected to the positive terminal of the dc input voltage. When S4 is switched on, terminal a is brought to the negative terminal of the dc source. There are six modes of operation in a cycle with duration of 60 degrees each.

The gating signals are provided such that the switching sequence is S6 S1 S2, S1 S2 S3 S2 S3 S4, S3 S4 S5, S4 S5 S6 and S5 S6 S1 as in fig. The gating signals are shifted by 60 degree to obtain three phase balanced voltage .

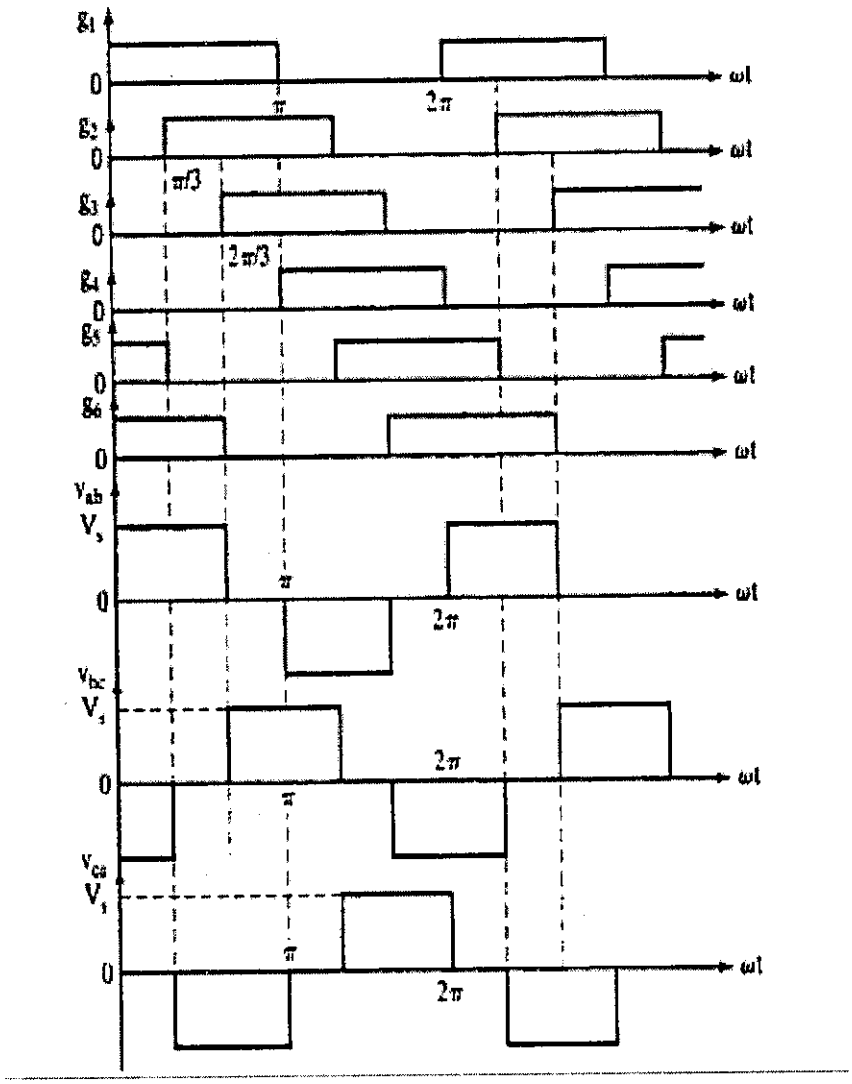


Fig 1.6. Waveform of 180 conduction mode

120 degree conduction mode:

In this mode each transistor conducts for 120 degrees. Three transistors remain on at any instant of time. There are six modes of operation in a cycle with duration of 60 degrees each. The

gating signals are provided such that the switching sequence is S6 S1, S1 S2, S2 S3, S3 S4, S4 S5 and S5 S6 as in fig. There is a delay of 30 degrees turning off of S1 and turning on of S4. Thus there is no possibility of short circuit of the dc supply through one upper and one lower transistor.

The voltage waveform is shown in figure 1.7.

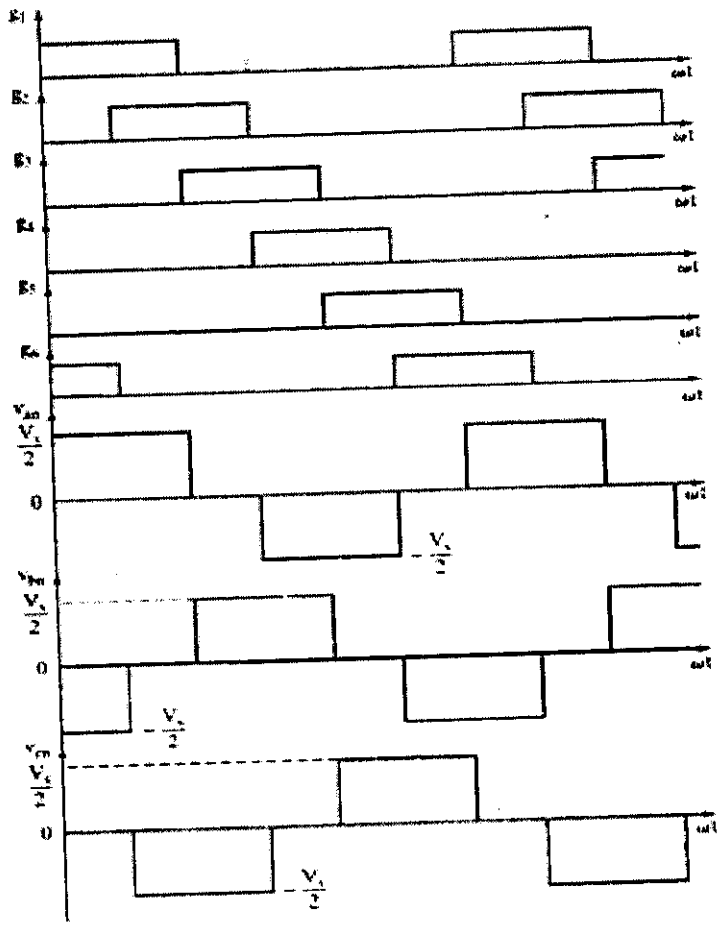


Fig 1.7. Waveform of 120 conduction mode

MULTILEVEL INVERTERS

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. There are three general configurations of multilevel inverter. They are

- Diode clamped
- Flying capacitor
- Cascaded H-bridge

But there are also other types of multilevel inverters existing. The generalized output of a multilevel inverter is shown below.

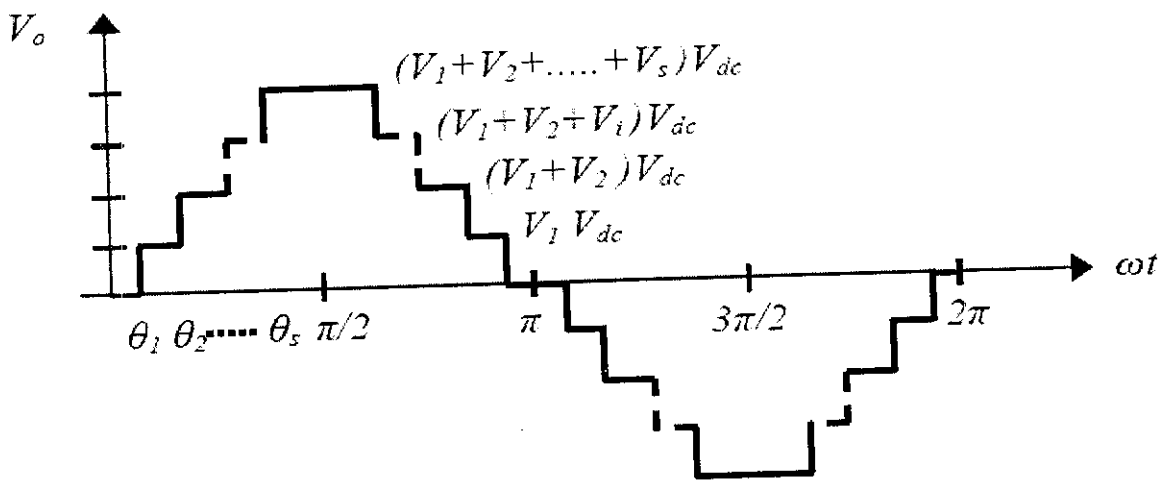


Fig 1.8. Generalized output of multilevel inverter

1.4 ORGANISATION OF THE PROJECT

Chapter 1:

It comprises of general introduction to basics of inverters, multilevel inverters and the proposed topology.

Chapter 2:

It includes fundamental configurations of multilevel inverters and also our proposed system with reduced number of switches.

Chapter 3:

Simulation results of five, seven, and nine level inverters are shown along with the THD values and THD comparisons of different levels of inverter.

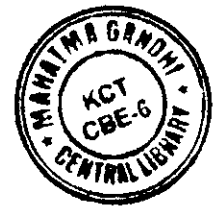
Chapter 4:

Hardware details of the proposed system.

Chapter 5:

It includes scope of the project and its future expansion.

CHAPTER



CHAPTER 2

MULTILEVEL INVERTER

2.1. MULTILEVEL INVERTER

Multilevel inverter is considered as one of the most significant recent advances in power electronics. Multilevel inverters have drawn tremendous interest in the field of high-voltage high-power applications such as laminators, mills, conveyors, compressors, large induction motor drives, UPS systems and static VAR compensation. Its concept is based on producing small output voltage steps, resulting in better power quality. Multilevel inverters accomplish the concept of power conversion using small voltage steps, then achieving better power quality. Although this requires a large number of semiconductor devices, which is considered as a primary disadvantage. They are of lower ratings and operate at the fundamental frequency so that the switching loss is reduced and better electromagnetic compatibility is achieved. The fundamental configurations of multilevel inverters include; the diode-clamp topology, the flying-capacitor topology, and the series H-bridge topology. Recently, there has been a great interest in cascaded hybrid topologies dedicated to large drive systems applications.

2.2. A LITERATURE SURVEY ON MULTILEVEL INVERTERS

As per literature there are three fundamental configurations of multilevel inverter. They are

- Diode clamped
- Flying capacitor
- Cascaded H-bridge

DIODE CLAMPLED MULTILEVEL INVERTER

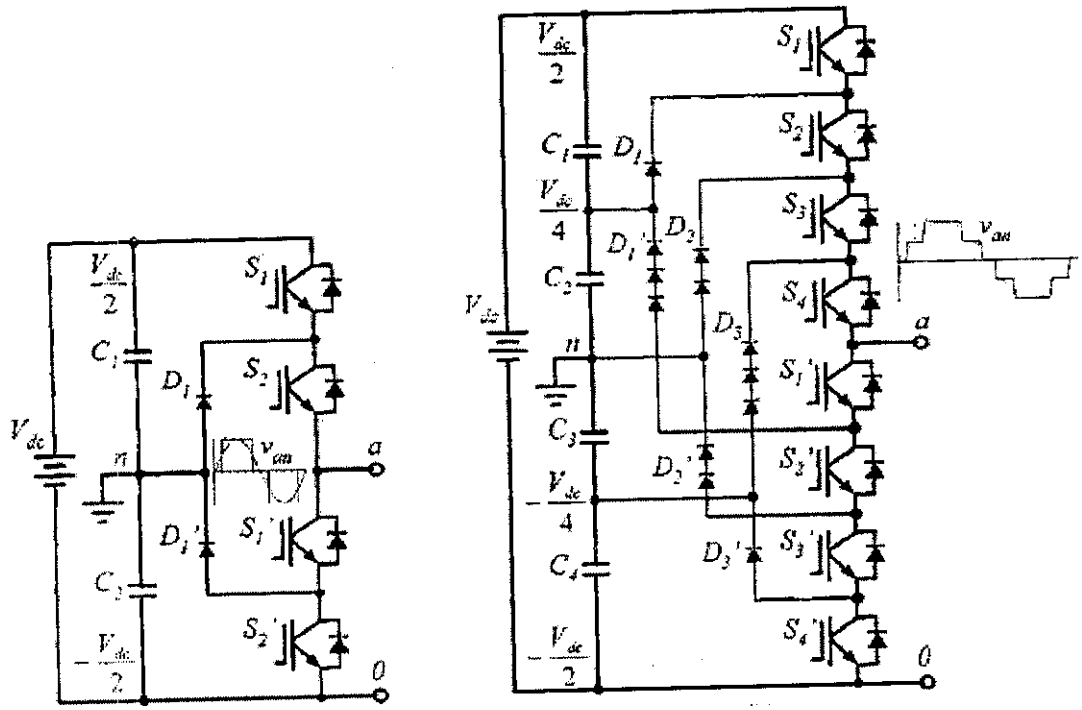


fig 2.1. Diode clamped inverters

The diode clamped multilevel inverter is can produce any number of levels of output voltage. An m-level inverter requires (m-1) capacitors, 2(m-1) switching devices and (m-1)(m-2) clamping diodes. The diode clamped multilevel inverter has the following characteristics:

- High voltage rating of the blocking diodes
- Unequal switching of devices
- Capacitor voltage unbalance

The following are the advantages of diode clamped multilevel inverter.

- Reduced harmonic content
- Control method is simple
- Inverter efficiency is high because all devices are switched at fundamental frequency

The following are the disadvantages of diode clamped multilevel inverter.

- More number of clamping devices are required when the number of level are increased
- It is difficult to control the real power flow in the system

FLYING CAPACITOR MULTILEVEL INVERTER

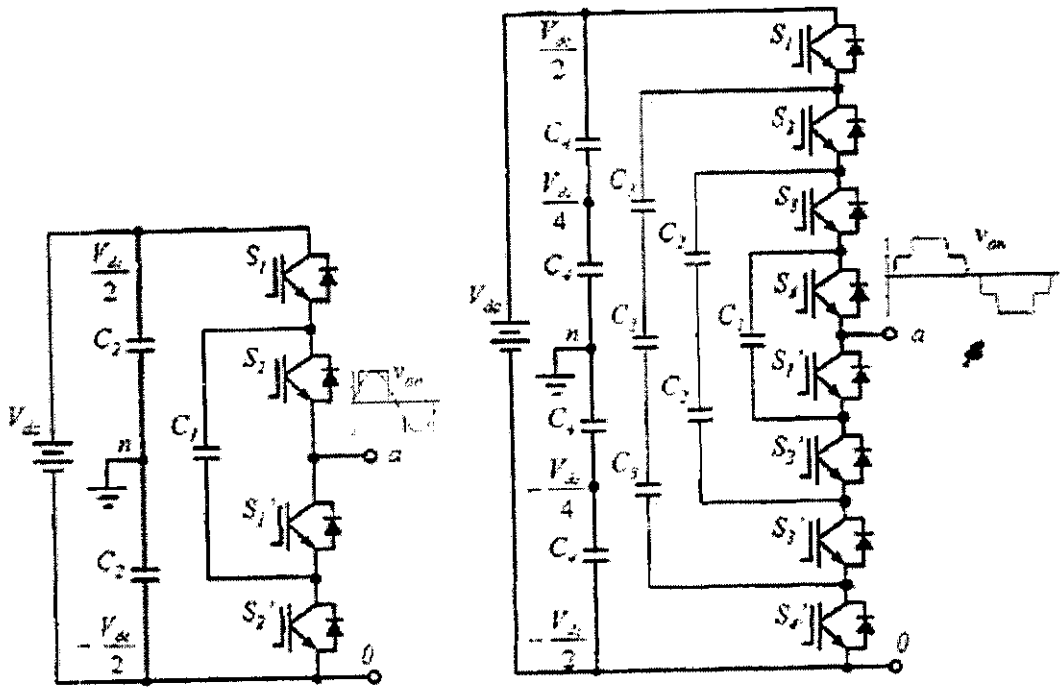


Fig 2.2. Flying capacitor inverters

The flying capacitor configuration multilevel inverter is shown in the figure. This topology requires large number of capacitors. For m-level inverter it requires (m-1)*(m-2)/2 auxiliary capacitors phase per leg in addition to (m-1) dc bus capacitors. This multilevel inverter has the following characteristics.

- This topology uses large number of capacitors
- There is balance in the voltages of the capacitors used

The following are the advantages of flying capacitor multilevel inverter.

- Large amount of storage capacitors are used which can provide capabilities during power outages.
- These inverters provide switch combination redundancy for balancing different voltage levels
- With the increase in the number of levels the harmonic content is reduced thus reduces the usage of filters
- Both active power and reactive power can be controlled

The following are the disadvantages of flying capacitor multilevel inverter.

- Usage of large number of capacitors
- Control of inverter is complicated
- Switching frequency and switching losses are high for real power transmission

CASCADED H-BRIDGE MULTILEVEL INVERTER

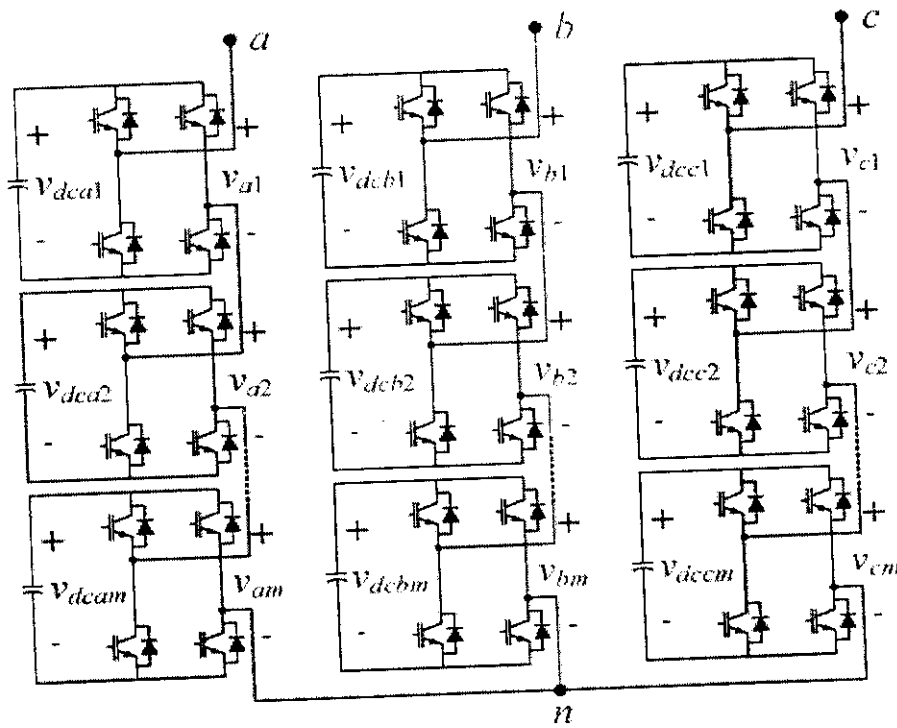


Fig 2.3. Cascaded H-bridge multilevel inverter

Cascaded multilevel inverters are based on a series connection of several single-phase inverters. This structure is capable of reaching medium output voltage levels using only standard low- voltage mature technology components. Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage. The general circuit diagram of a three phase cascaded H- bridge inverter is shown in fig. The cascaded multilevel structure has the following features.

- It requires separate dc source. So it is very useful in conversion process for renewable energy sources such as photovoltaic cell, biomass etc.
- Connecting two dc source back to back is not possible because short circuit may occur if not switched synchronously

The following are the advantages of cascaded multilevel inverter.

- It requires least number of switches when compared to the other two topologies
- Since it has the same structure connected together optimized circuit layout and packing is possible. There are no requirements of extra clamping diodes or voltage balancing capacitors.
- Soft switching techniques are used to reduce the switching losses anddevice stresses.

The following are the disadvantages of cascaded multilevel inverter.

- It needs separate dc sources for real power conversions thereby limiting its applications

2.3. PROPOSED MULTILEVEL INVERTER TOPOLOGY:

The principle objective of the proposed configuration of multilevel inverter power circuit is to reach at the minimum possible number of switching devices, without affecting thestaircase output voltage waveform characterized by conventional multilevel topologies. However, there is a small penalty have to be paid, which is the increased rating of the four main switches as they have to withstand the whole dc bus. The continued and increased advances in high power semiconductor technology allowed the working range of IGBTs to reach 6.5kV, which will indeed increase the popularity of the presented configuration. The generalized configuration of the proposed three-phase multilevel inverter is shown in Fig.1. Each phase consists of4 main switches in an H-bridge configuration connected across the dc bus. A group of capacitors are connected acrossthe dc bus to achieve voltage divider task for the differentnumber of inverter levels. A number of bi-directional switches are connected from the supply voltage dividerpoints to the phase voltage point of the main bridge. The generalized multilevel inverter can be developed for any required number of levels.

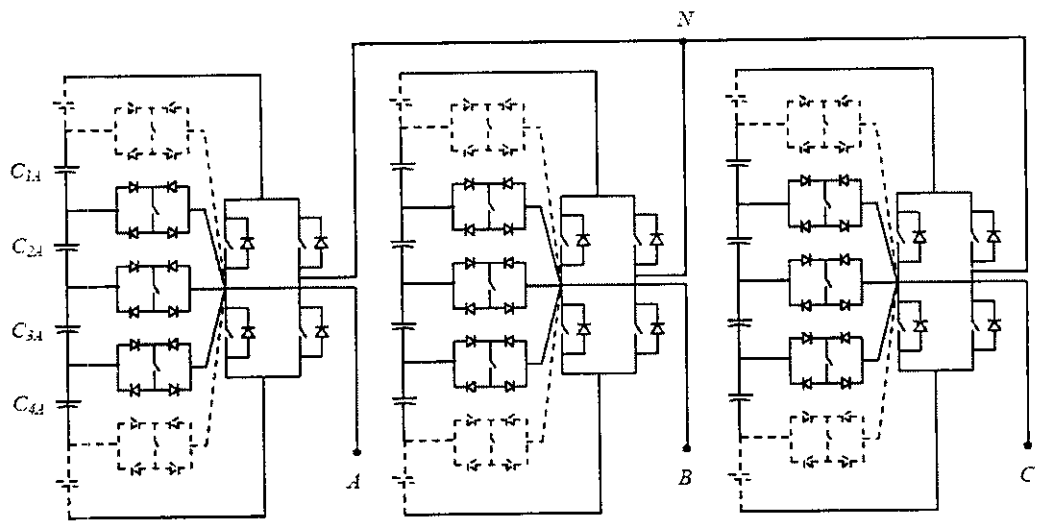


Fig 2.4. Generalized circuit diagram of proposed multilevel inverter

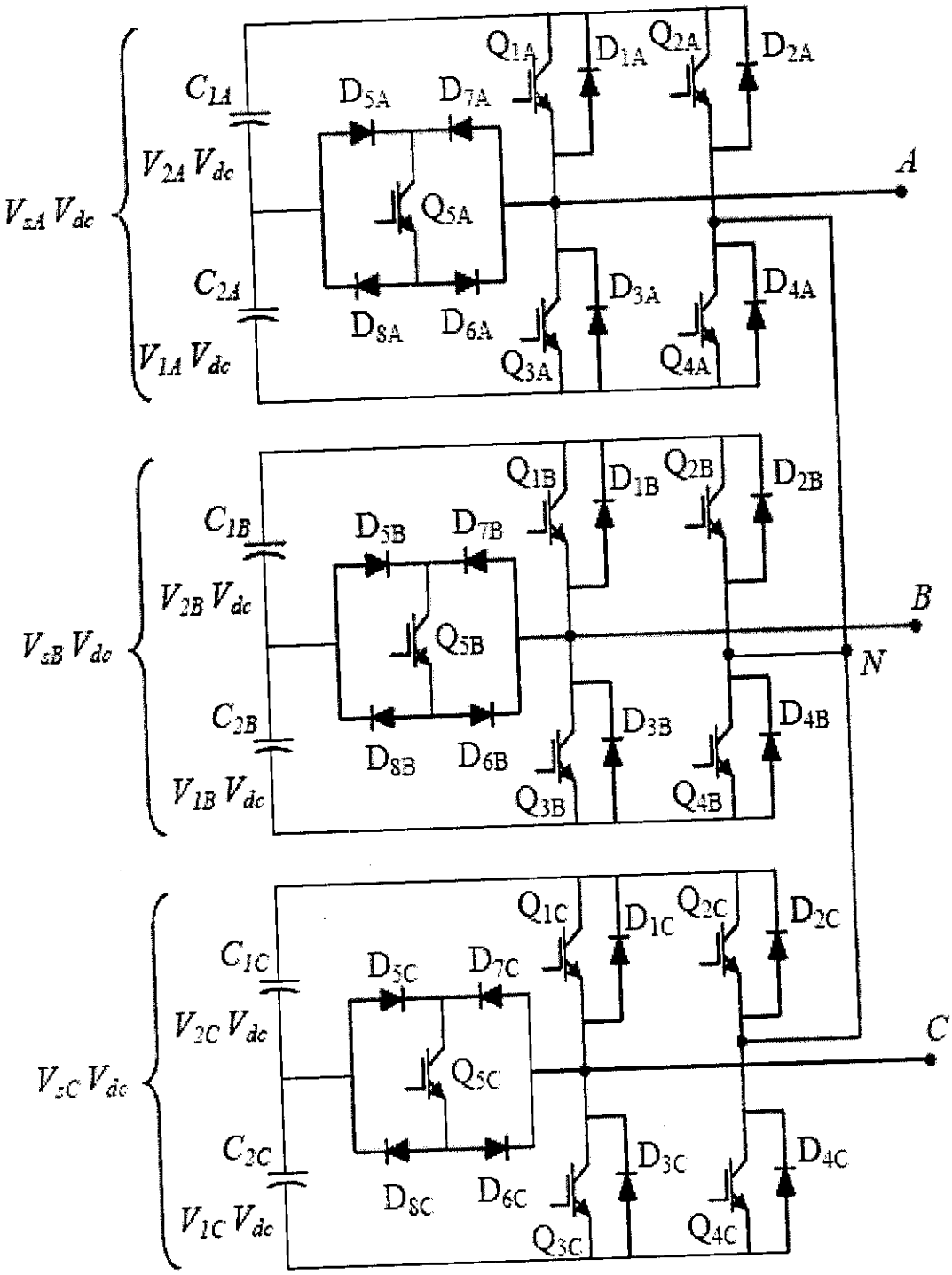


Fig 2.5. Power circuit of the proposed three-phase 5-level inverter

EXPECTED OUTPUT OF THE PROPOSED SYSTEM

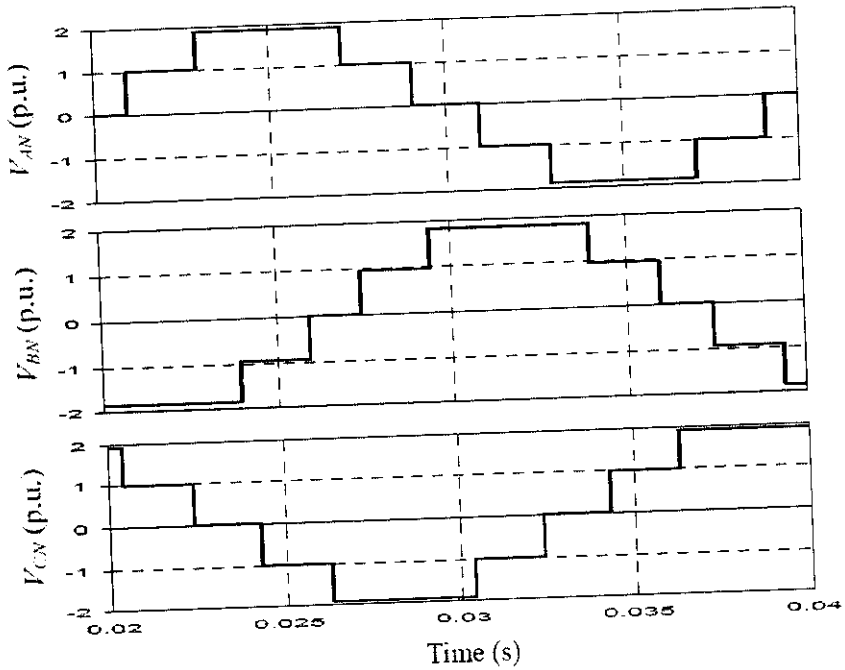


Fig 2.6. Output phase voltages

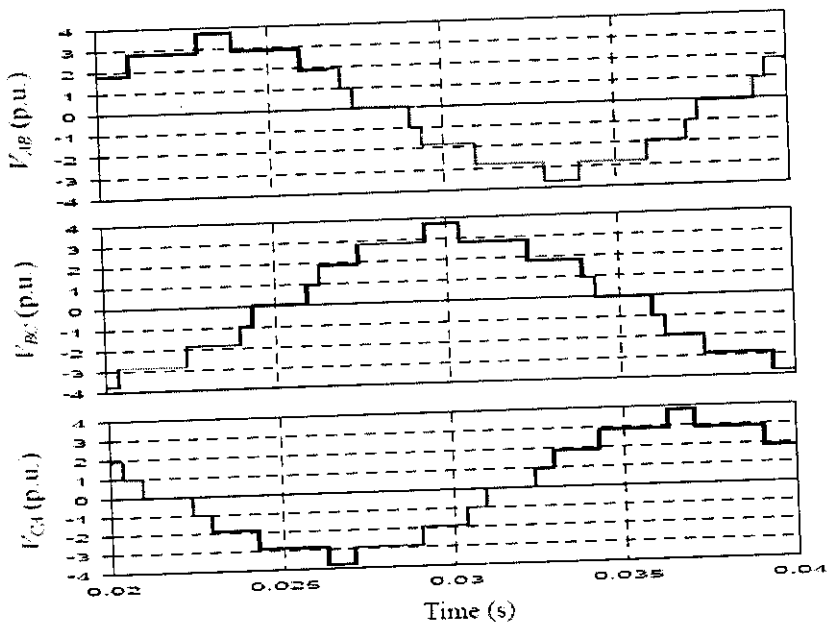


Fig 2.7. Output line voltage

2.4. COMPARISION BETWEEN CASCADED H-BRIDGE TOPOLOGY AND THE PROPOSED TOPOLOGY:

The graph following graph is plotted between number of levels and number of switches for each phase. Here the cascaded H-bridge inverter and proposed inverter topology are compared. And it can be seen that the number of switches used is very much reduced in the new inverter topology.

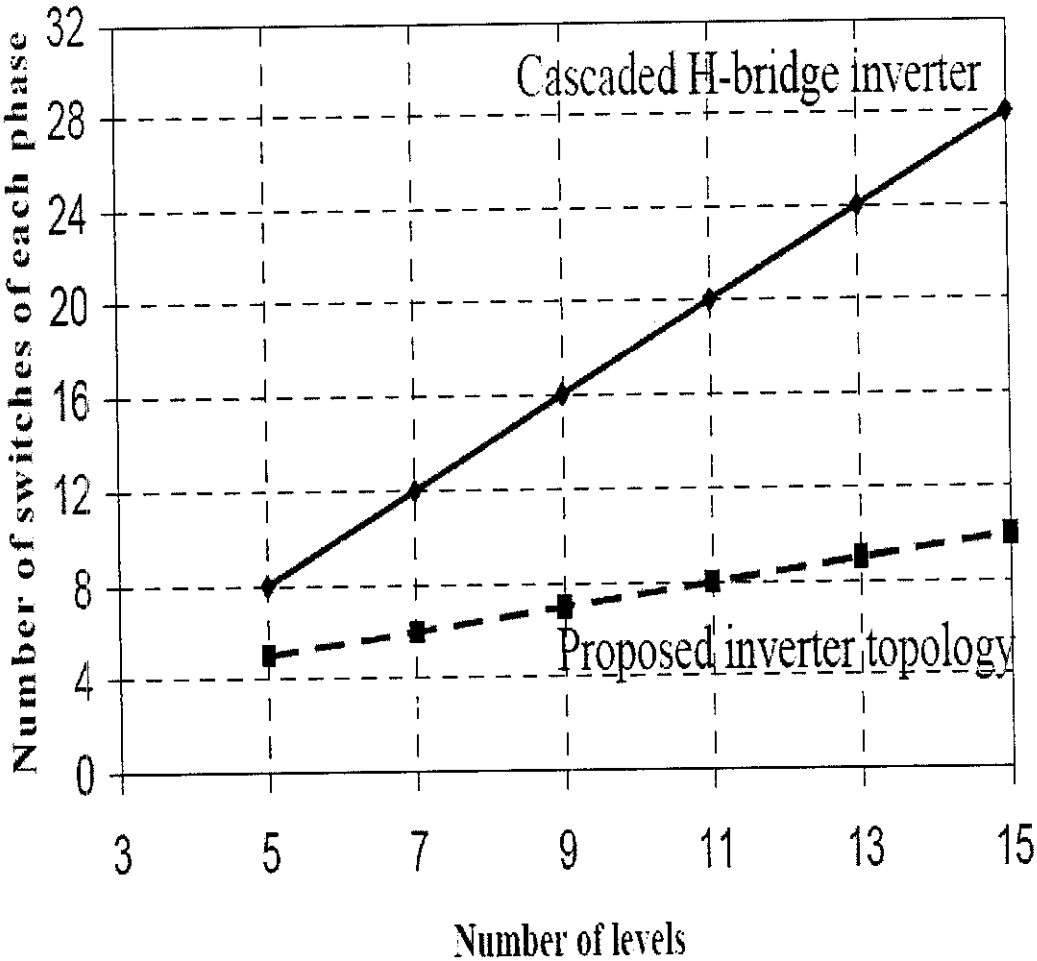


Fig 2.8. Comparison between cascaded H-bridge inverter and proposed topology

2.5. ADVANTAGES OF THE PROPOSED TOPOLOGY:

The new topology has some good advantages over other existing inverter topologies. They are.

- Substantial reduction in the number of switching devices used.
- Complexity of the circuit is reduced
- Reduction in the overall size of the hardware
- Multilevel output can be realized for any number of levels

Thus this is the most widely used topology of multilevel inverter because of these advantages it has over other topologies.

CHAPTER

CHAPTER 3

SIMULATION RESULTS

3.1. CONVENTIONAL THREE PHASE INVERTER

3.1.1. OUTPUT WAVEFORMS

CONVENTIONAL THREE PHASE INVERTER- PHASE VOLTAGE

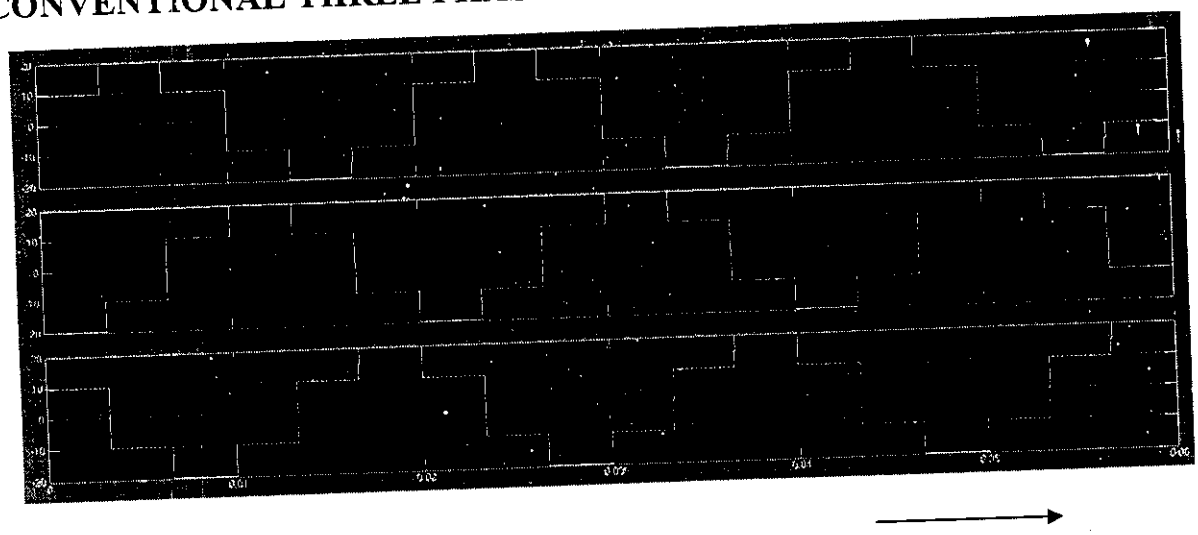


Fig 3.1. Phase Voltage of Three Phase Inverter

CONVENTIONAL THREE PHASE INVERTER- LINE VOLTAGE

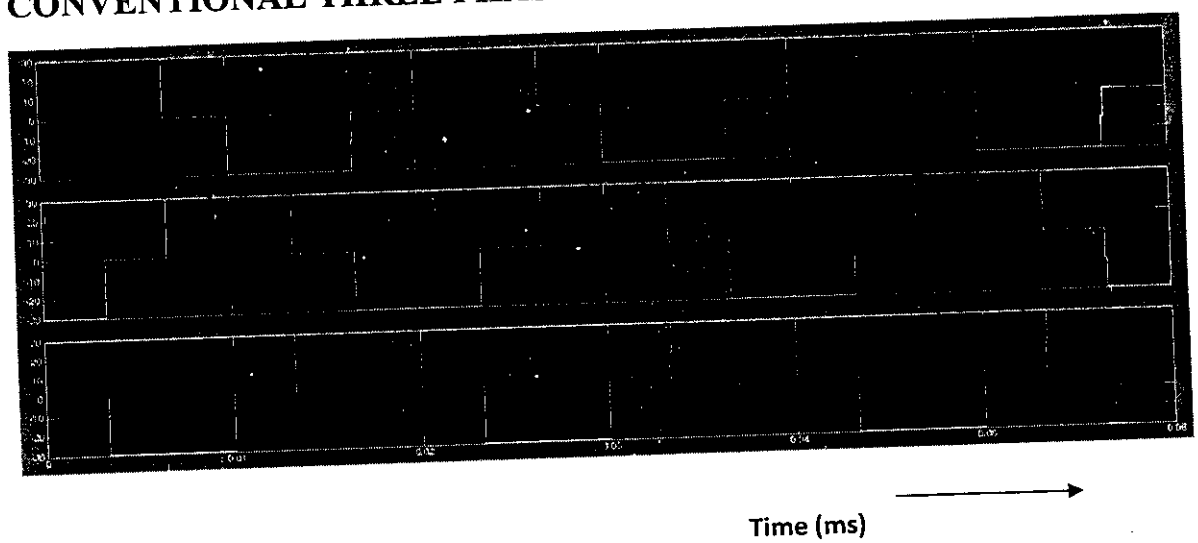


Fig 3.2. Line Voltage of Three Phase Inverter

CONVENTIONAL THREE PHASE INVERTER- CURRENT

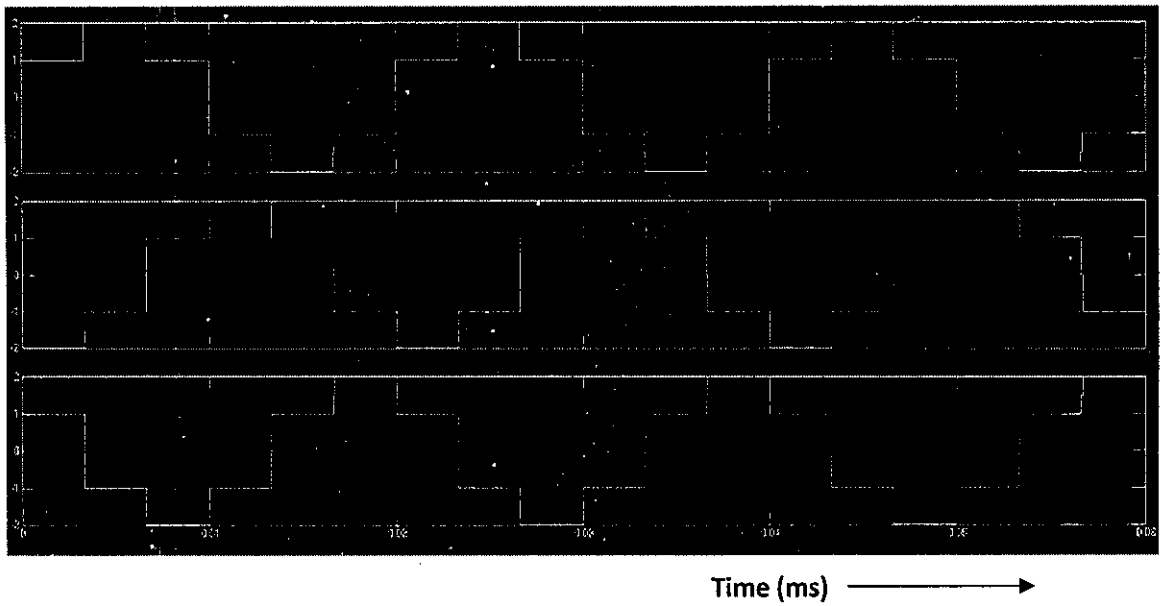
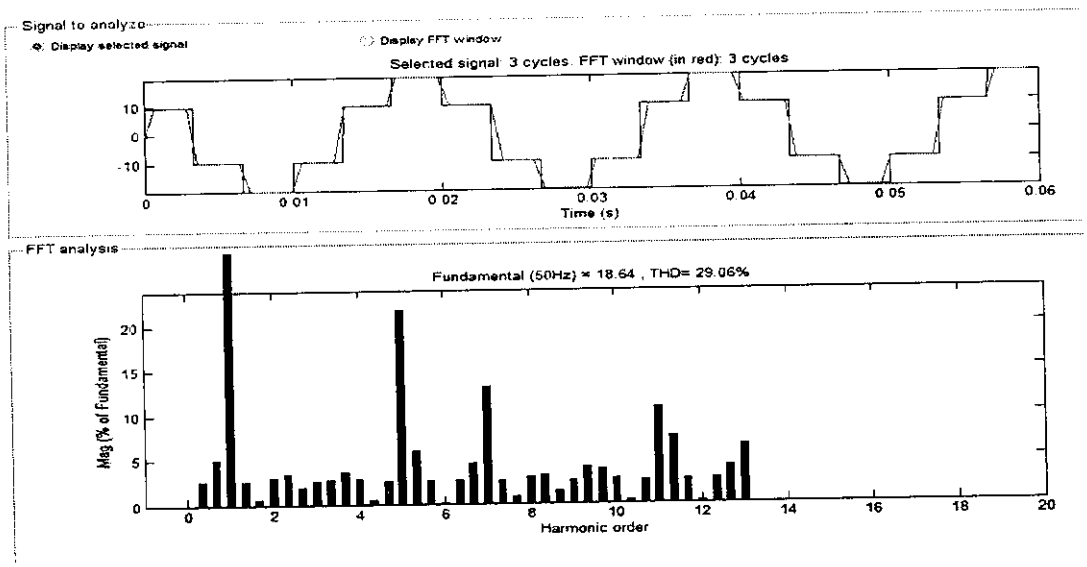


Fig 3.3. Current Waveform of Three Phase Inverter

3.1.2. FFT ANALYSIS

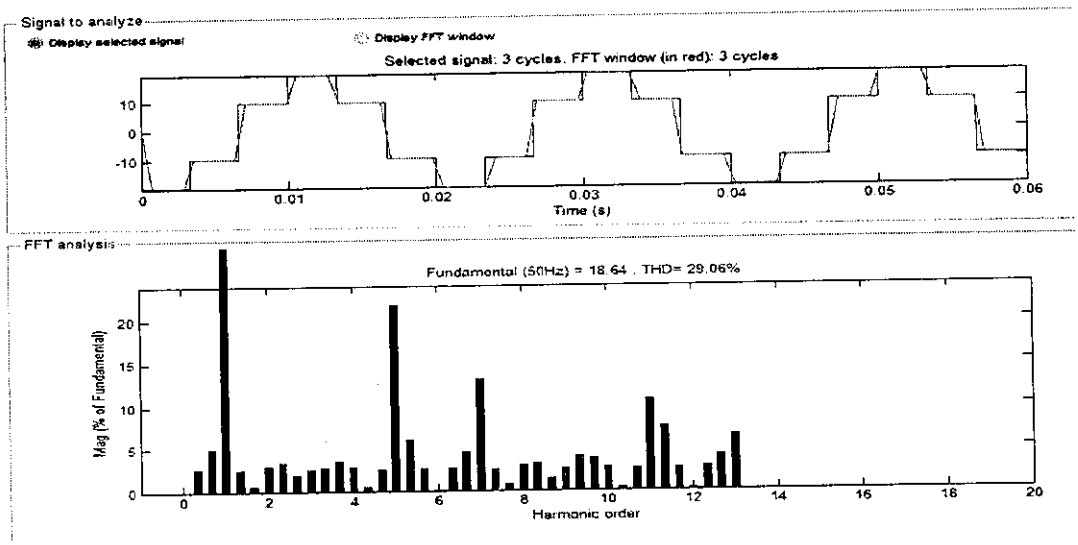
CONVENTIONAL THREE PHASE INVERTER- R PHASE FFT



THD=29.06%

Fig 3.4. FFT-R Phase

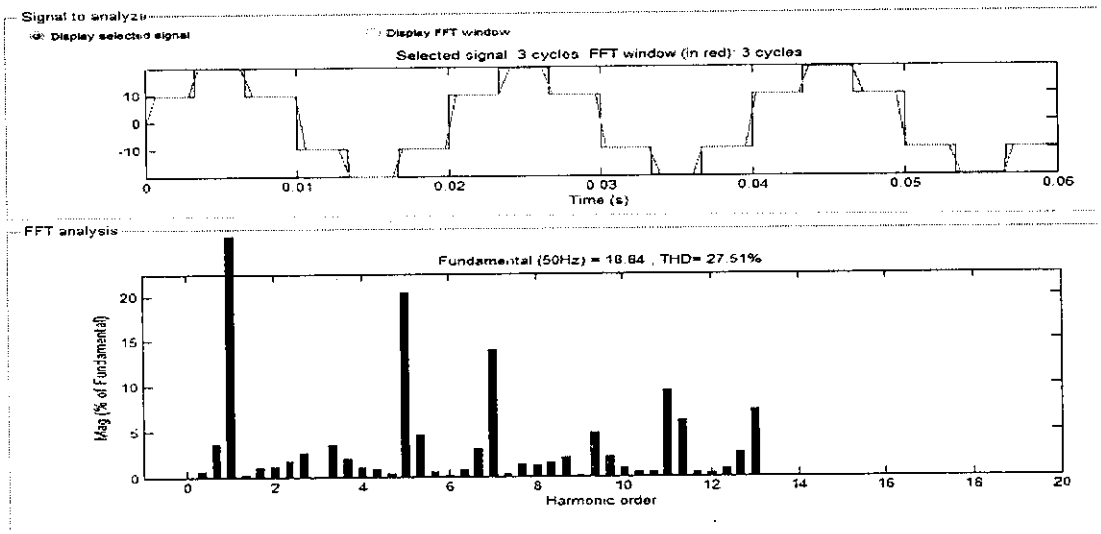
CONVENTIONAL THREE PHASE INVERTER- Y PHASE FFT



THD=29.06%

Fig 3.5. FFT-Y Phase

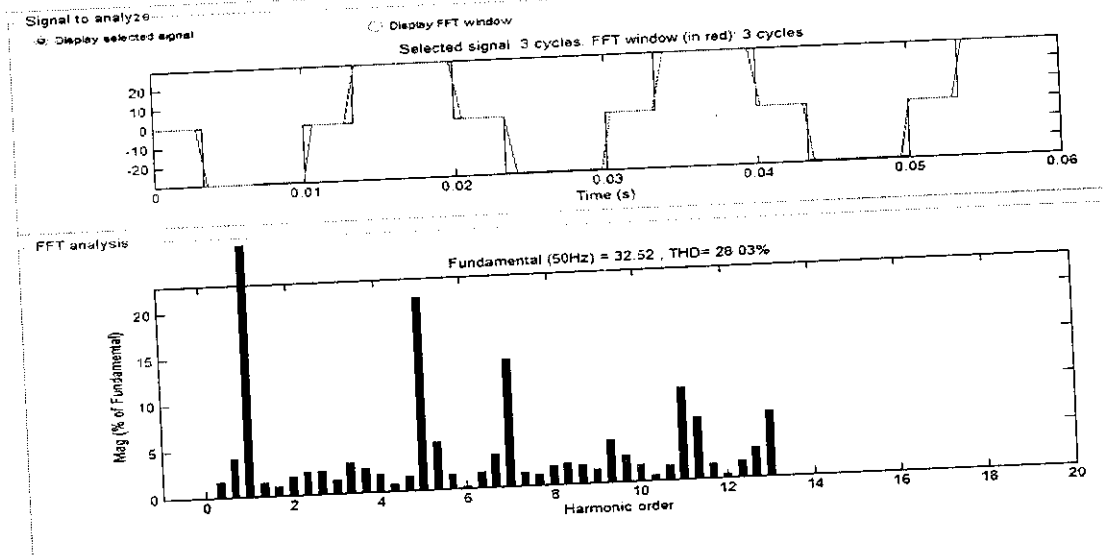
CONVENTIONAL THREE PHASE INVERTER- B PHASE FFT



THD=27.51%

Fig 3.6. FFT-B Phase

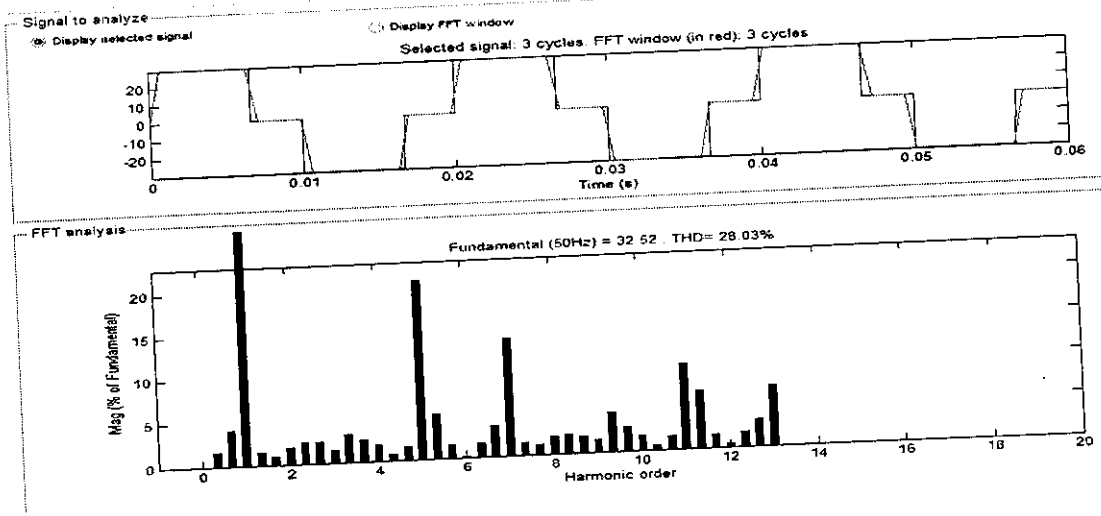
CONVENTIONAL THREE PHASE INVERTER- RY PHASE FFT



THD=28.03%

Fig 3.7. FFT-RY Line

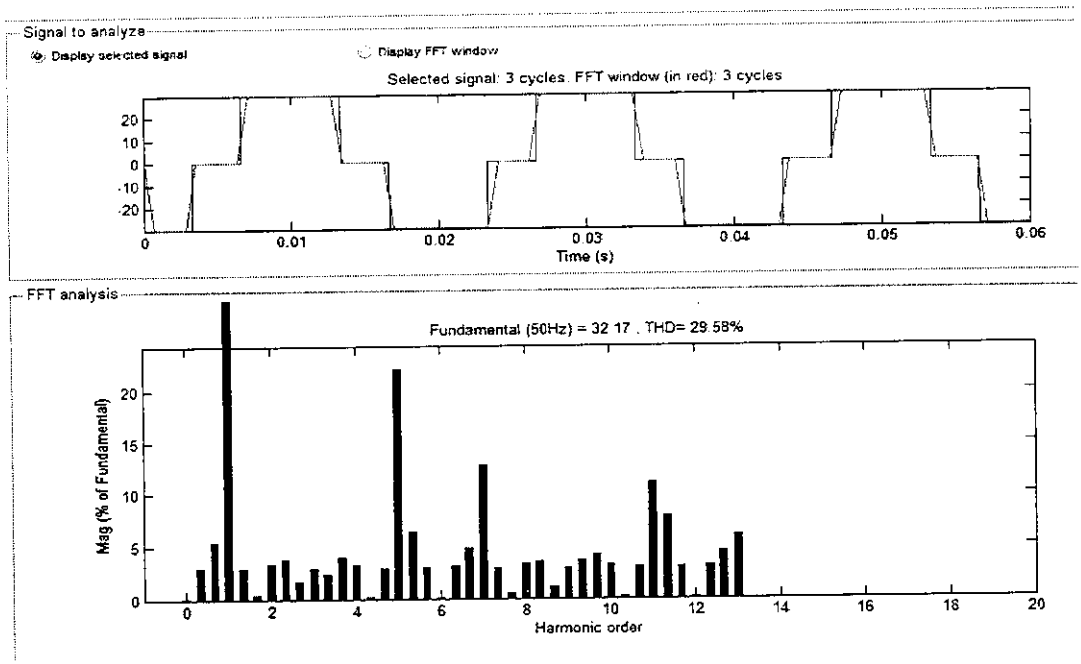
CONVENTIONAL THREE PHASE INVERTER- YB PHASE FFT



THD=28.03%

Fig 3.8. FFT-YB Line

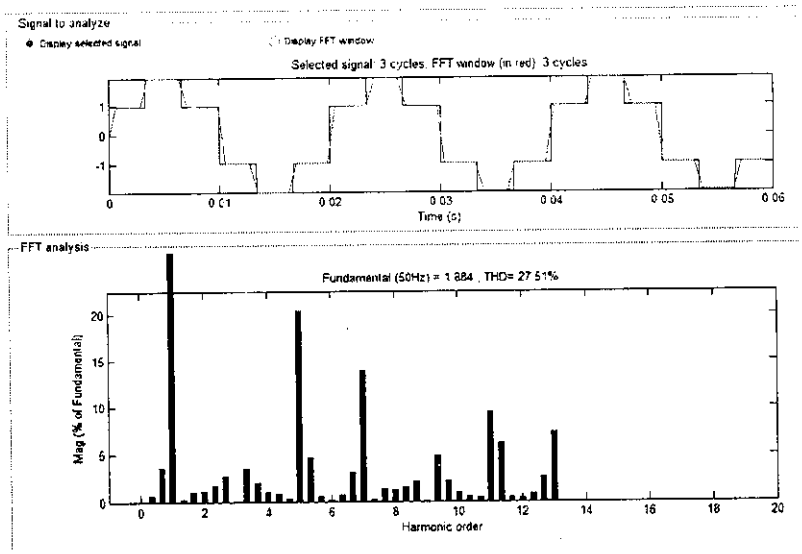
CONVENTIONAL THREE PHASE INVERTER- BR PHASE FFT



THD=29.58%

Fig 3.9. FFT-BR Line

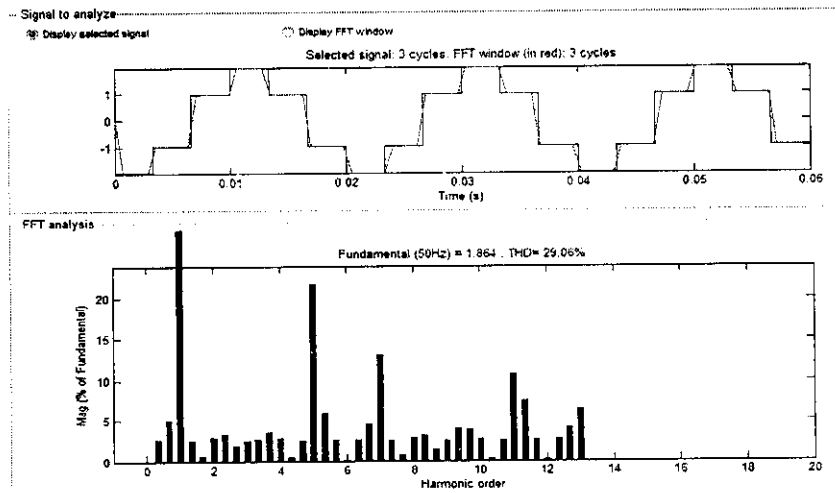
CONVENTIONAL THREE PHASE INVERTER- R PHASE CURRENT FFT



THD=27.51%

Fig 3.10 FFT-R Phase Current

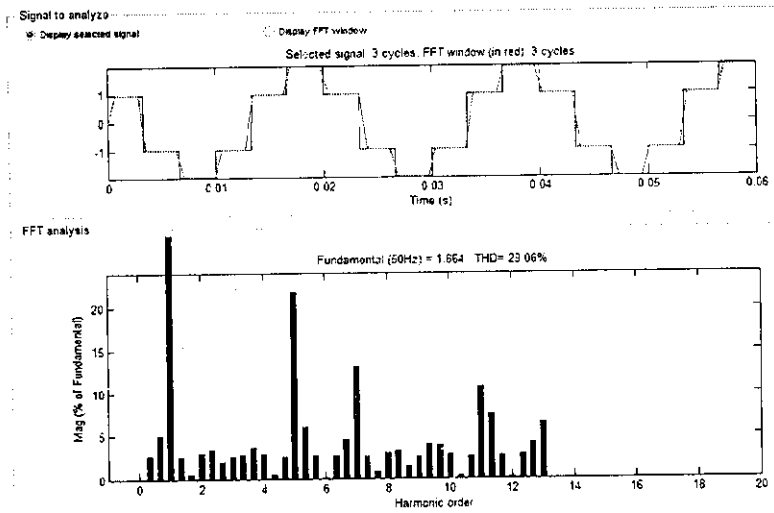
CONVENTIONAL THREE PHASE INVERTER- Y PHASE CURRENT FFT



THD=29.06%

Fig 3.11 FFT-Y Phase Current

CONVENTIONAL THREE PHASE INVERTER- B PHASE CURRENT FFT



THD=29.06%

Fig 3.12 FFT-B Phase Current

3.2. FIVE LEVEL INVERTER

3.2.1. OUTPUT WAVEFORMS

FIVE LEVEL INVERTER- PHASE VOLTAGE

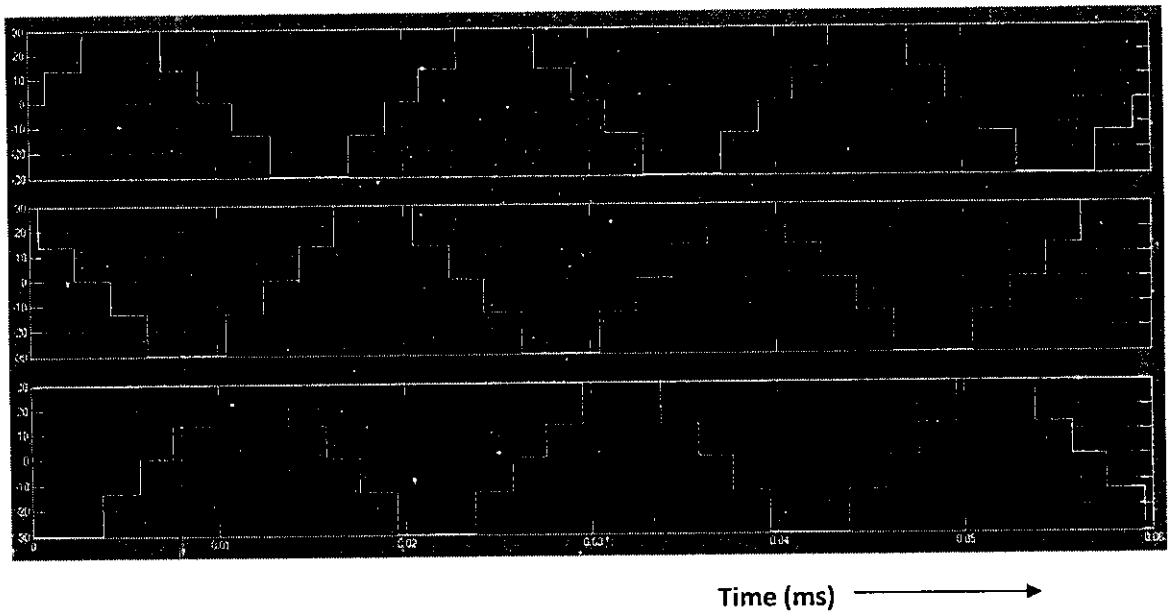


Fig 3.13. Phase Voltage Of Five Level Inverter

FIVE LEVEL INVERTER- LINE VOLTAGE

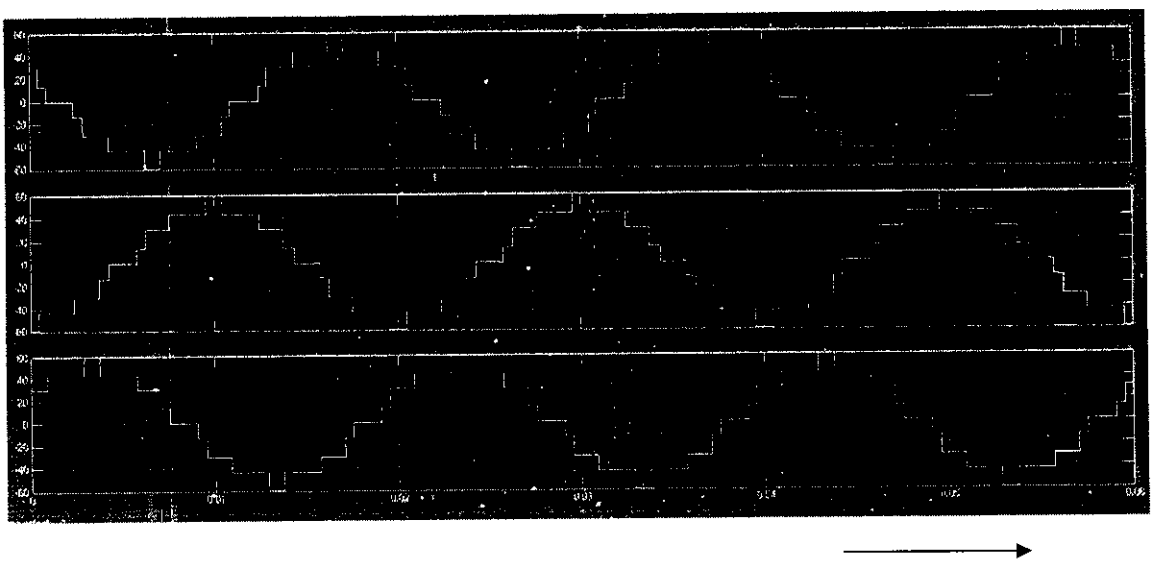


Fig 3.14. Line Voltage Of Five Level Inverter

FIVE LEVEL INVERTER- CURRENT

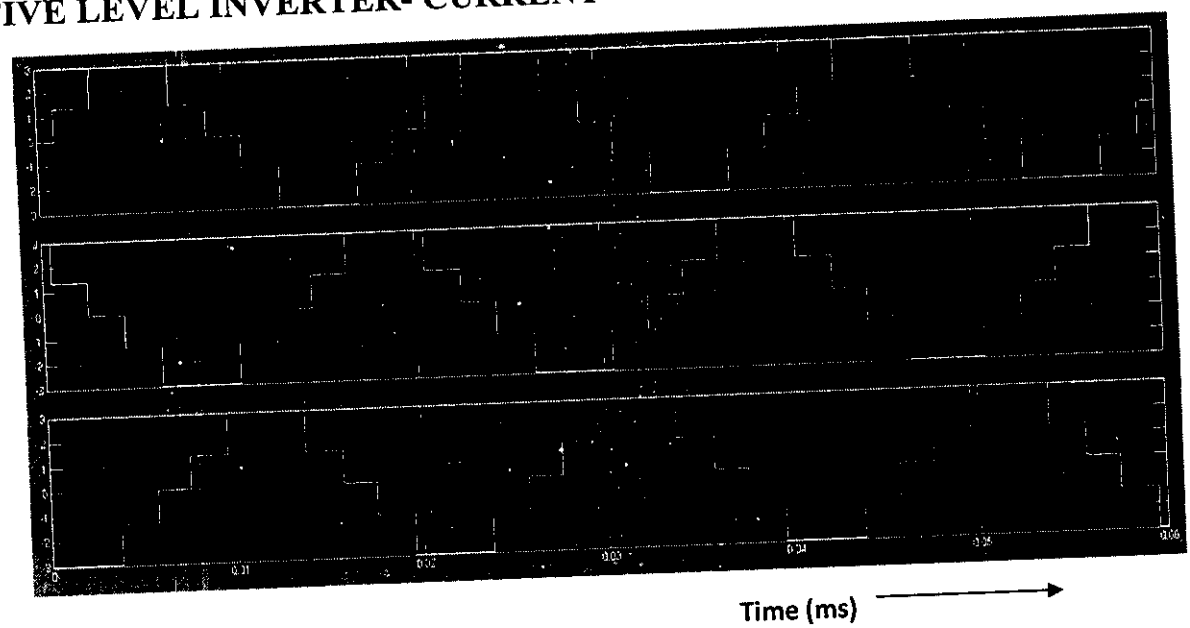
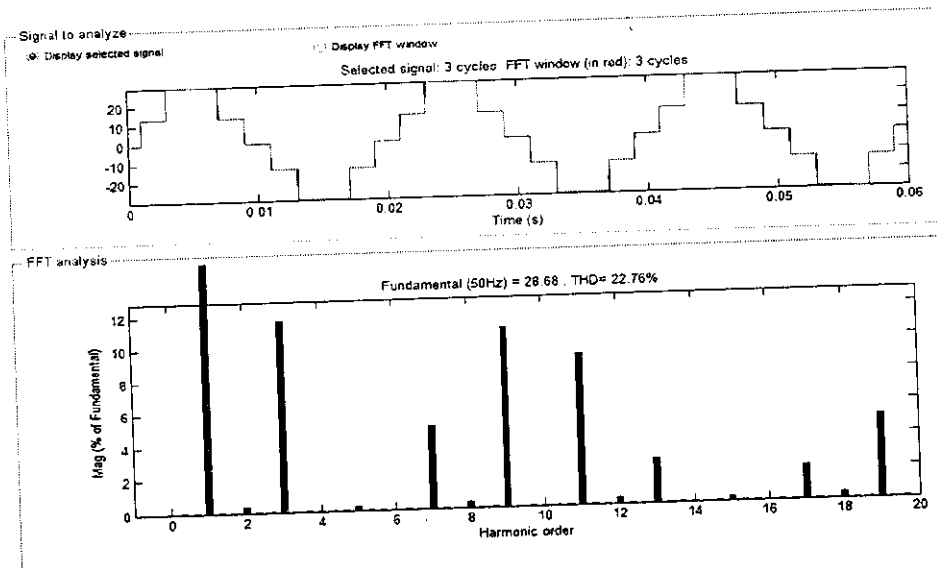


Fig 3.15. Current Waveforms of Five Level Inverter

3.2.2 FFT ANALYSIS

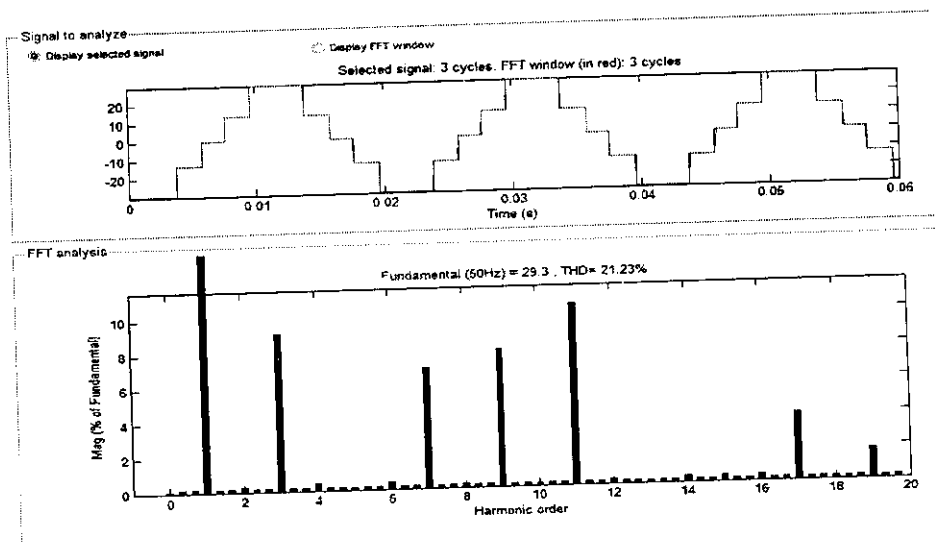
FIVE LEVEL INVERTER- R PHASE FFT



THD=22.76%

Fig 3.16. FFT-R Phase

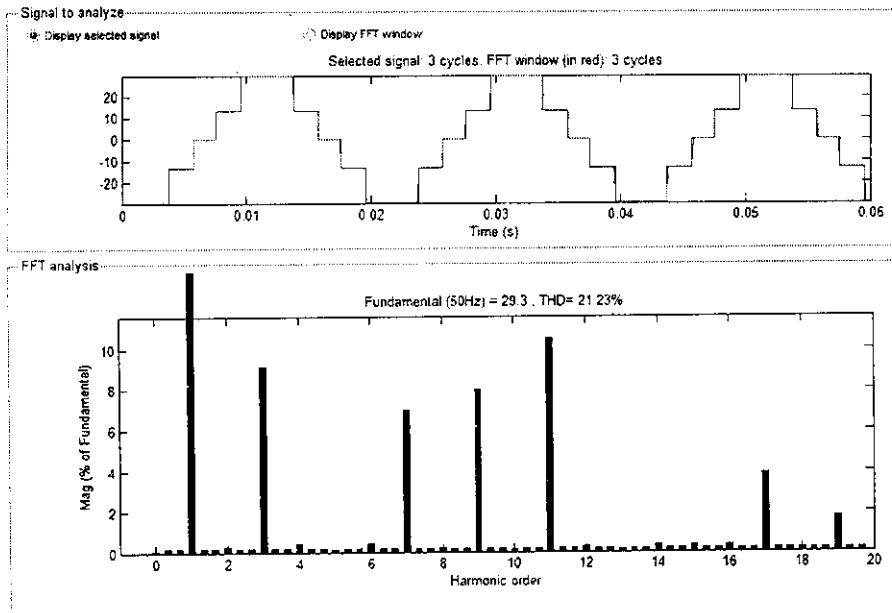
FIVE LEVEL INVERTER- Y PHASE FFT



THD=21.23%

Fig 3.17. FFT-Y Phase

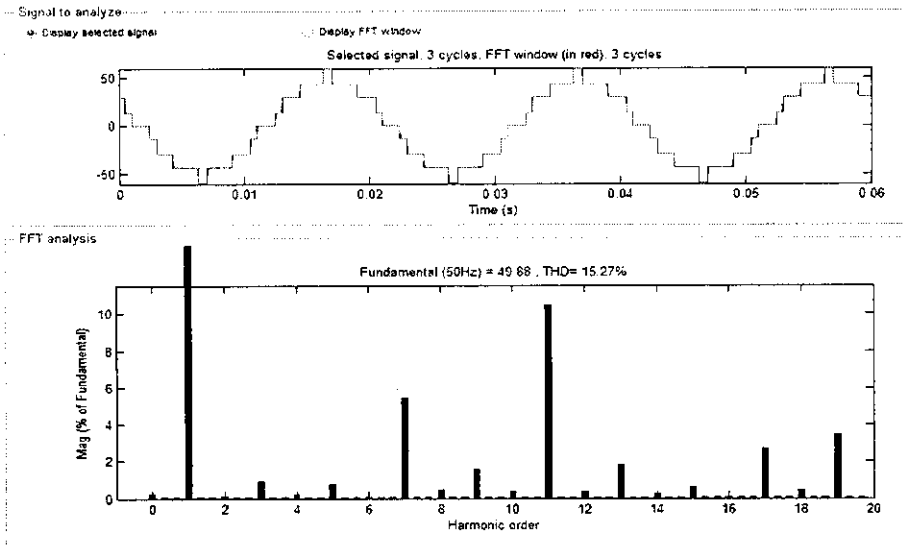
FIVE LEVEL INVERTER- B PHASE FFT



THD=21.23%

Fig 3.18. FFT-B Phase

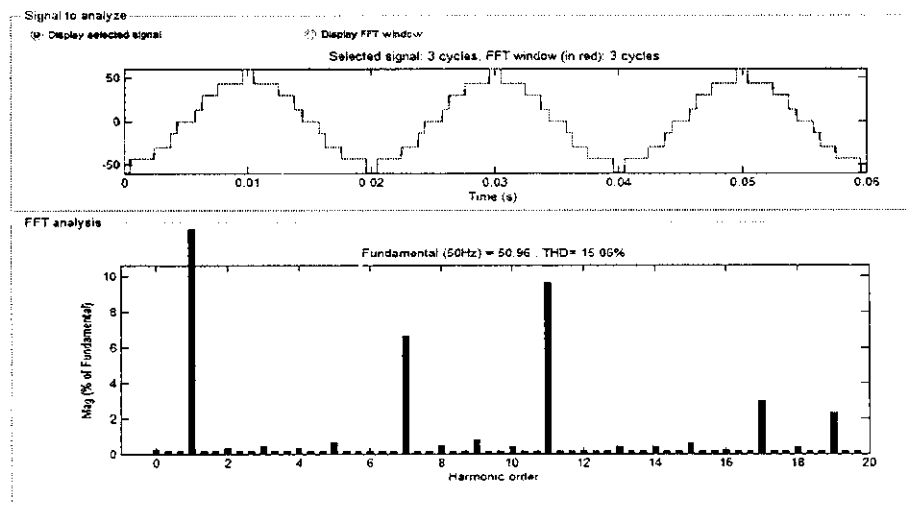
FIVE LEVEL INVERTER- RY LINE FFT



THD=15.27%

Fig 3.19. FFT-RY Line

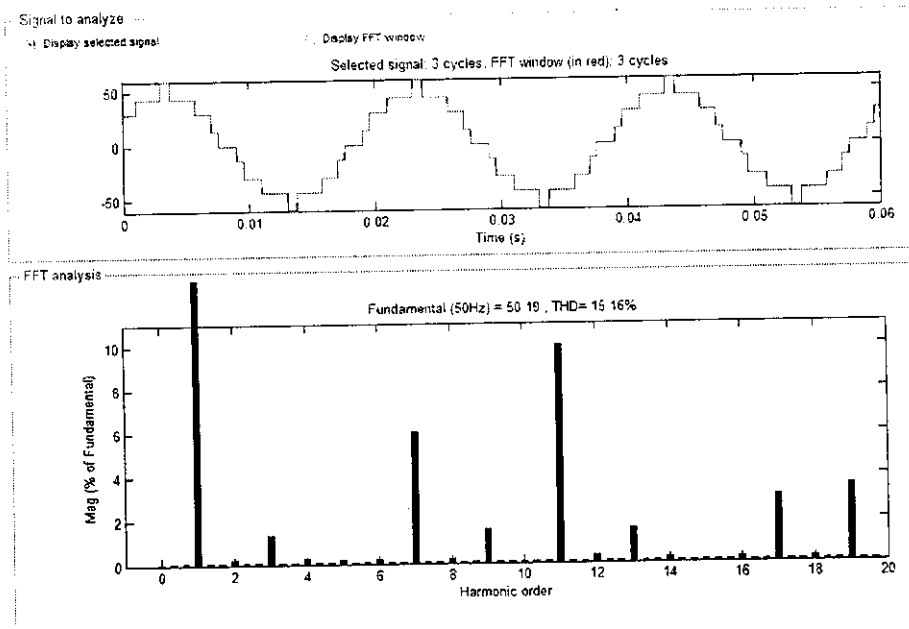
FIVE LEVEL INVERTER- YB LINE FFT



THD=15.06%

Fig 3.20. FFT-YB Line

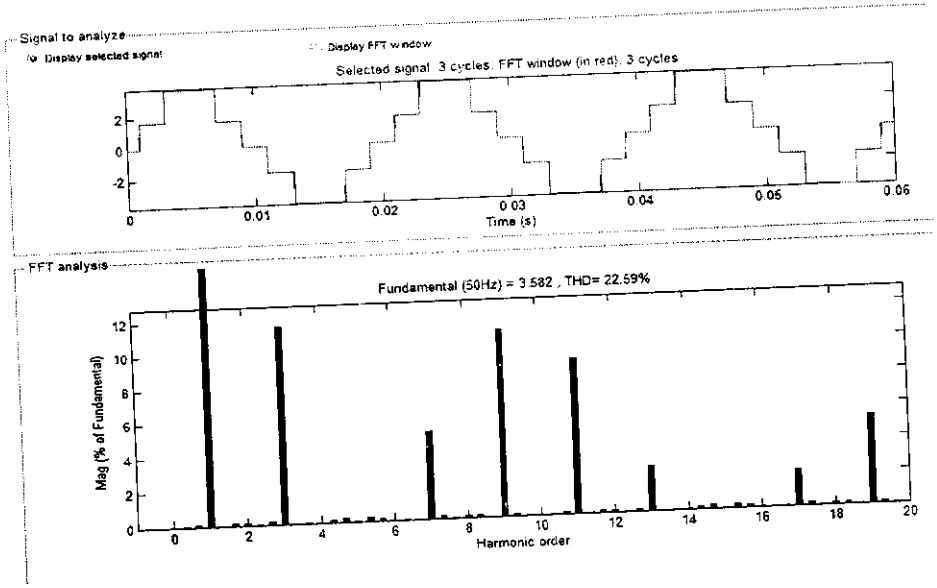
FIVE LEVEL INVERTER- BR LINE FFT



THD=15.16%

Fig 3.21. FFT-BR Line

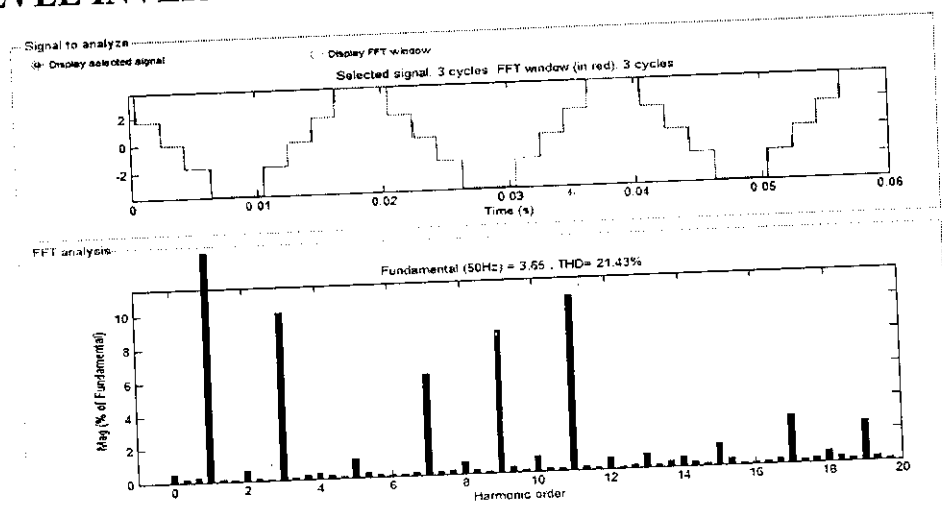
FIVE LEVEL INVERTER- R PHASE CURRENT FFT



THD=22.59%

Fig 3.22. FFT-R Phase Current

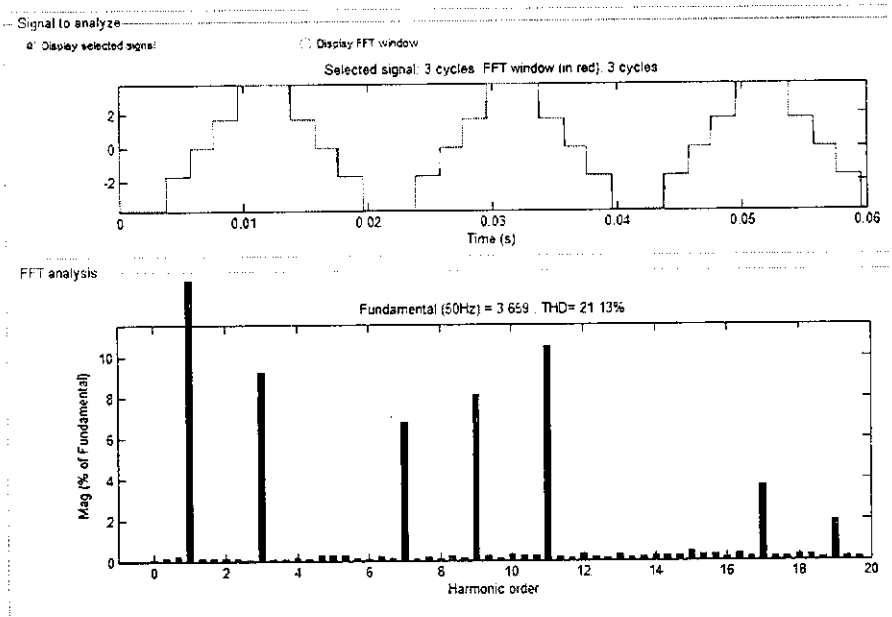
FIVE LEVEL INVERTER- Y PHASE CURRENT FFT



THD=21.43%

Fig 3.23. FFT-Y Phase Current

FIVE LEVEL INVERTER- B PHASE CURRENT FFT



THD=21.23%

Fig 3.24. FFT-B Phase Current

3.3. SEVEN LEVEL INVERTER

3.3.1 OUTPUT WAVEFORMS

SEVEN LEVEL INVERTER- PHASE VOLTAGE

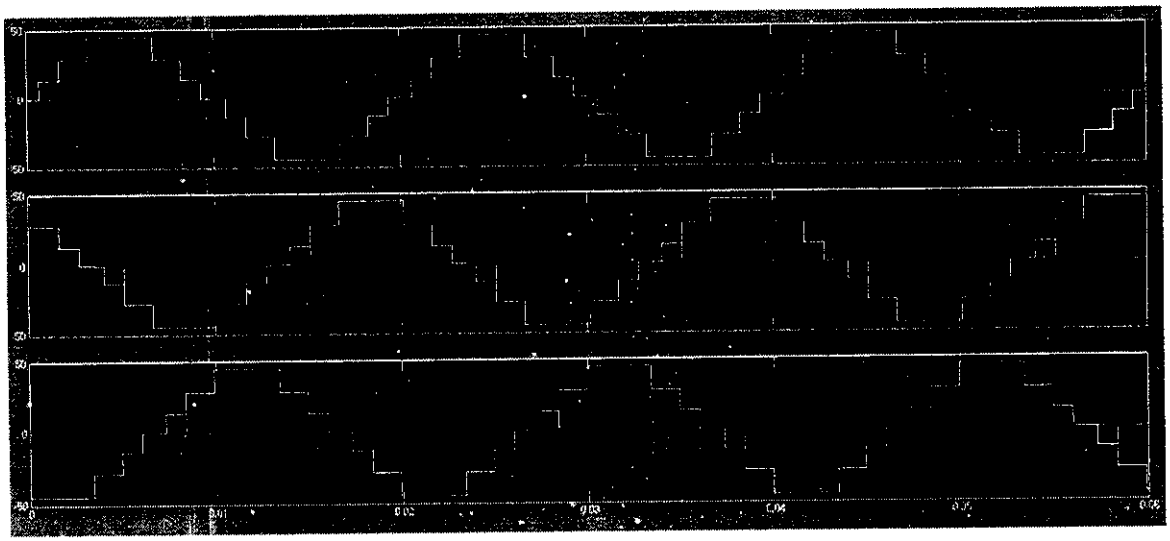


Fig 3.25. Phase Voltage Of Seven Level Inverter

SEVEN LEVEL INVERTER- LINE VOLTAGE

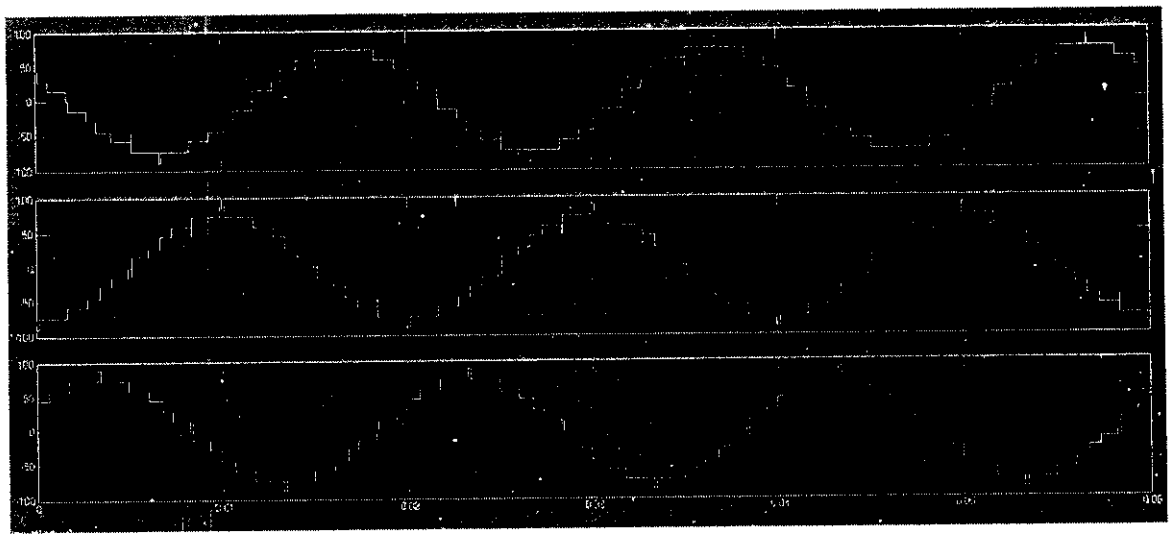


Fig 3.26.Line Voltage Of Seven Level Inverter

SEVEN LEVEL INVERTER- CURRENT

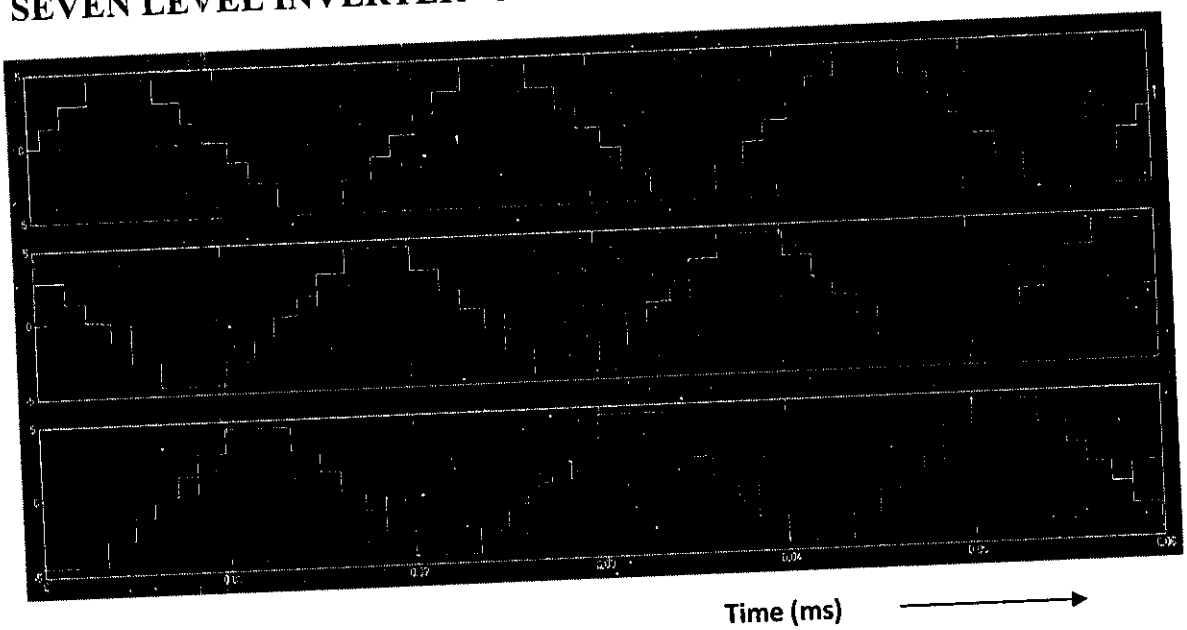
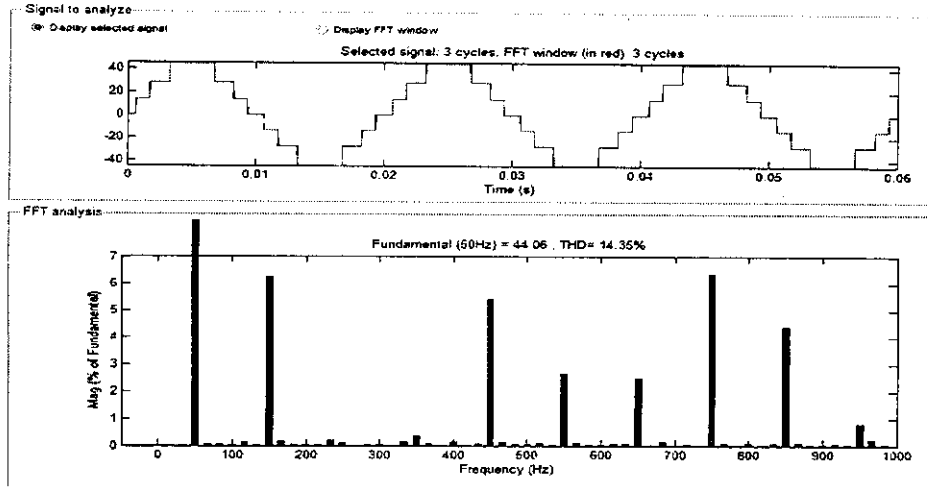


Fig 3.27. Current Waveforms of Seven Level Inverter

3.3.2 FFT ANALYSIS

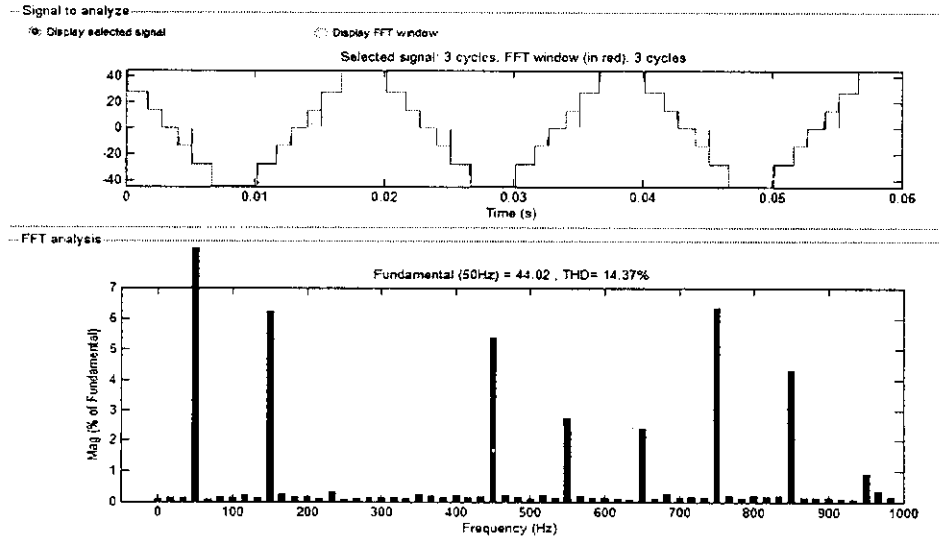
SEVEN LEVEL INVERTER- R PHASE FFT



THD=14.35%

Fig 3.28. FFT-R Phase

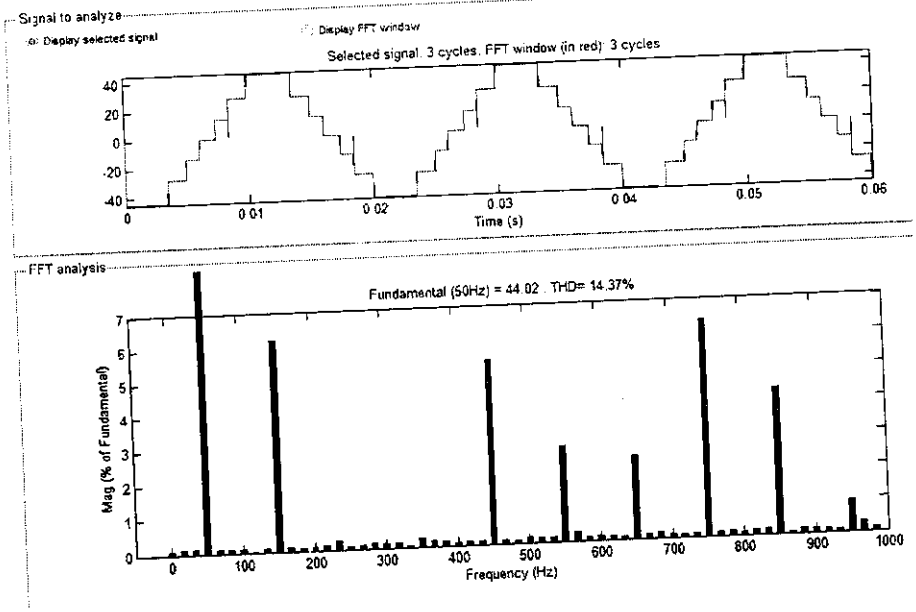
SEVEN LEVEL INVERTER- Y PHASE FFT



THD=14.37%

Fig 3.29. FFT-Y Phase

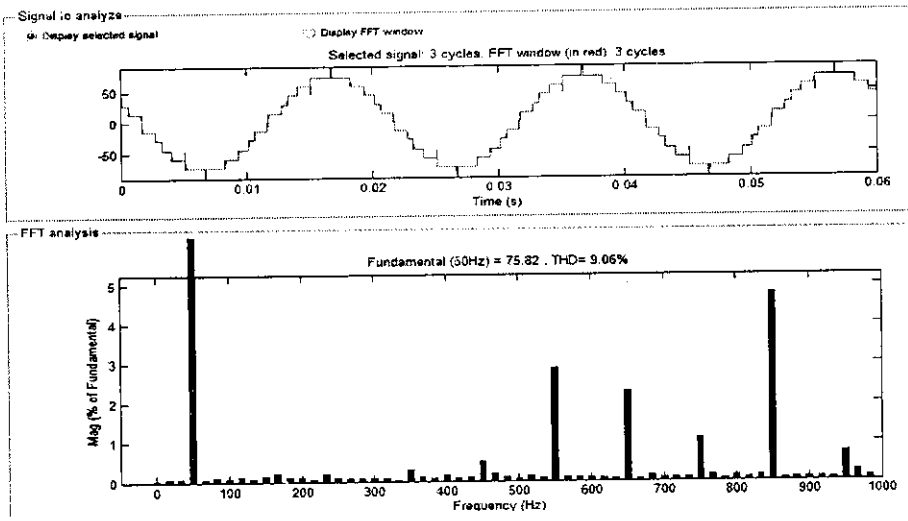
SEVEN LEVEL INVERTER- B PHASE FFT



THD=14.37%

Fig 3.30. FFT-B Phase

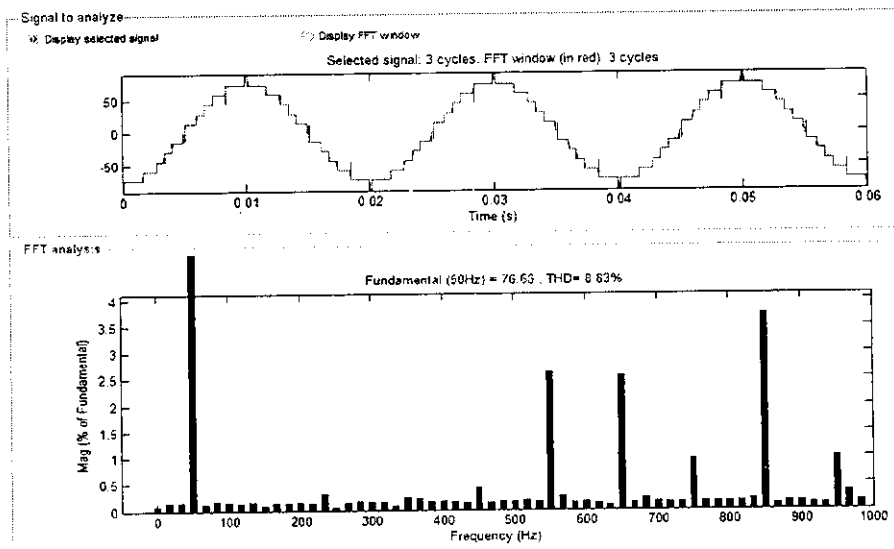
SEVEN LEVEL INVERTER- RY LINE FFT



THD=15.27%

Fig 3.31. FFT-RY Line

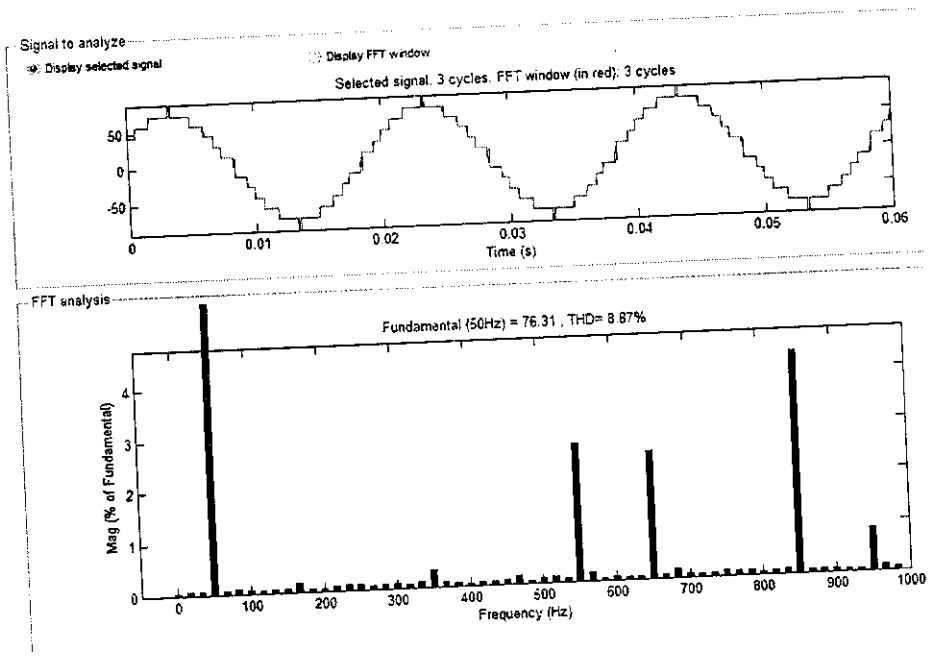
SEVEN LEVEL INVERTER- YB LINE FFT



THD=15.06%

Fig 3.32. FFT-YB Line

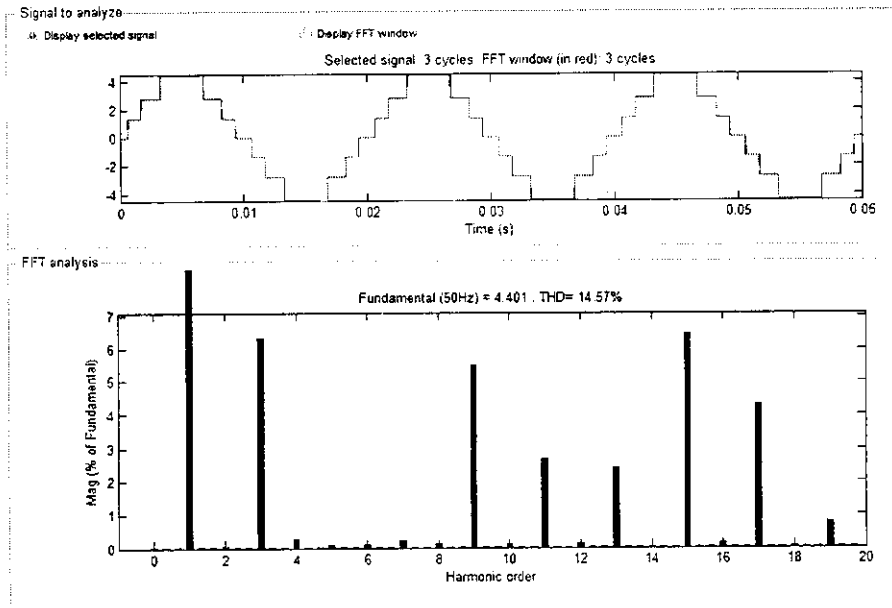
SEVEN LEVEL INVERTER- BR LINE FFT



THD=15.16%

Fig 3.33. FFT-BR Line

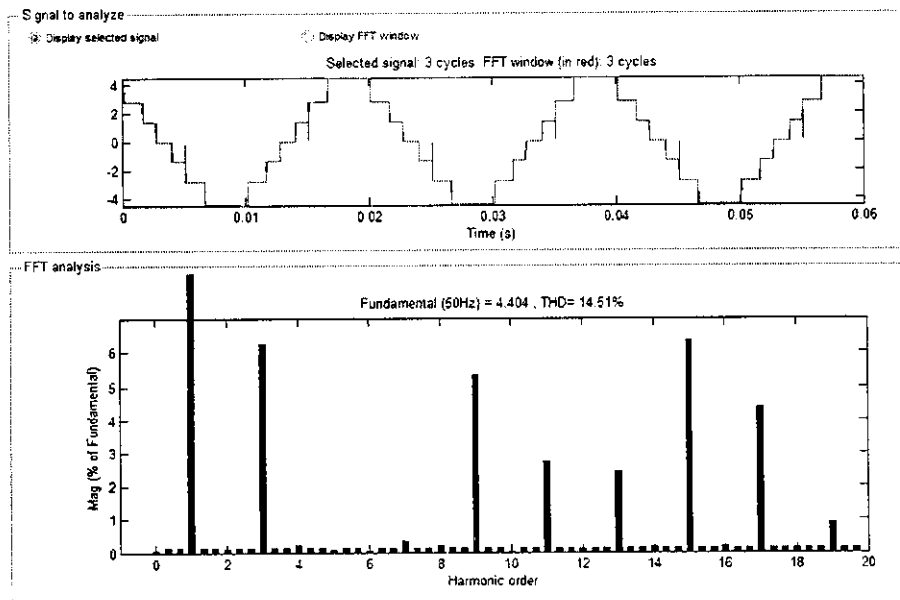
SEVEN LEVEL INVERTER -R PHASE CURRENT FFT



THD=14.57%

Fig 3.34. FFT-R Phase Current

SEVEN LEVEL INVERTER -Y PHASE CURRENT FFT



THD=14.51%

Fig 3.35. FFT-Y Phase Current

3.4. NINE LEVEL INVERTER

3.4.1. OUTPUT WAVEFORMS

NINE LEVEL INVERTER –PHASE VOLTAGE

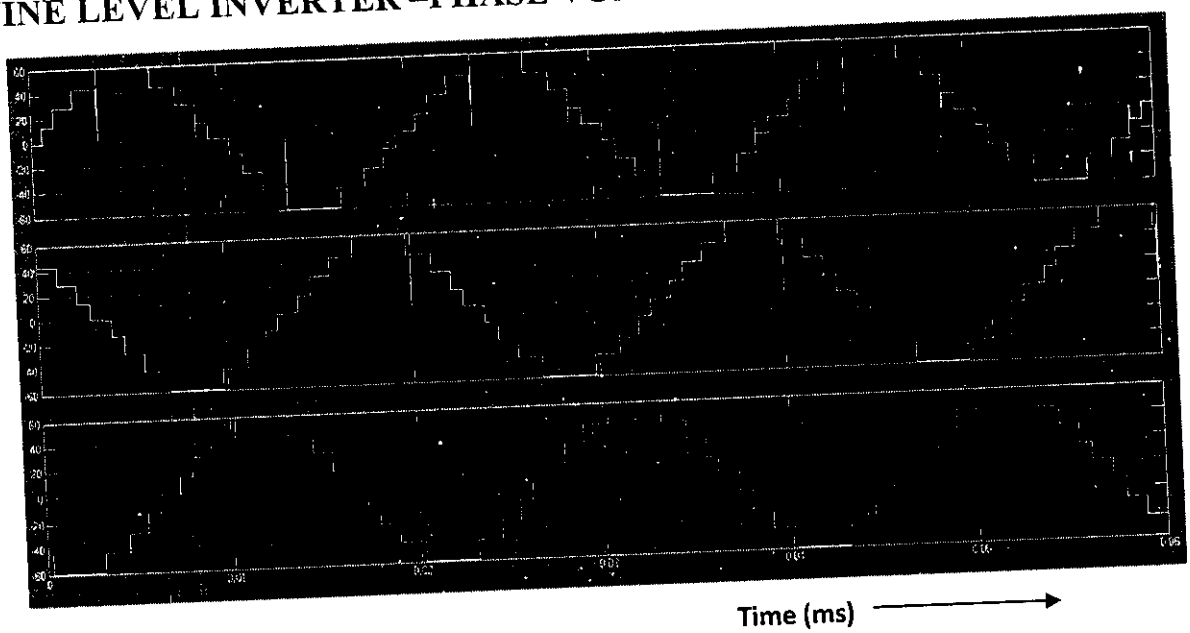


Fig 3.37. Phase Voltage Of Nine Level Inverter

NINE LEVEL INVERTER –LINE VOLTAGE

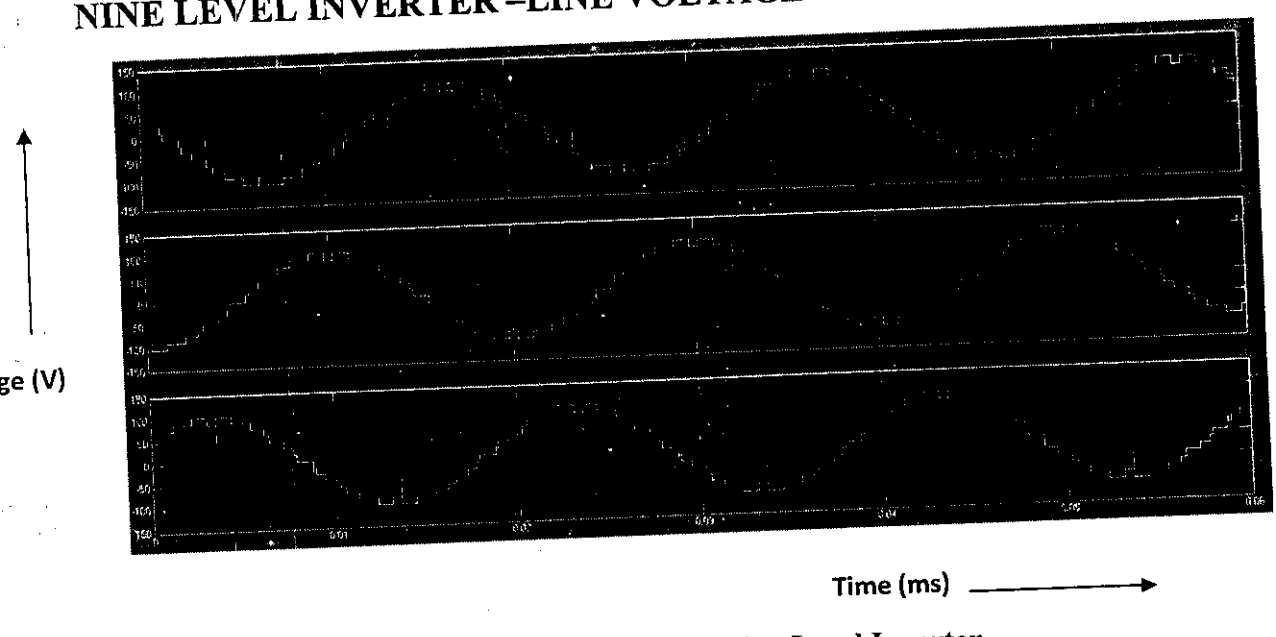


Fig 3.38. Line Voltage Of Nine Level Inverter

NINE LEVEL INVERTER –CURRENT

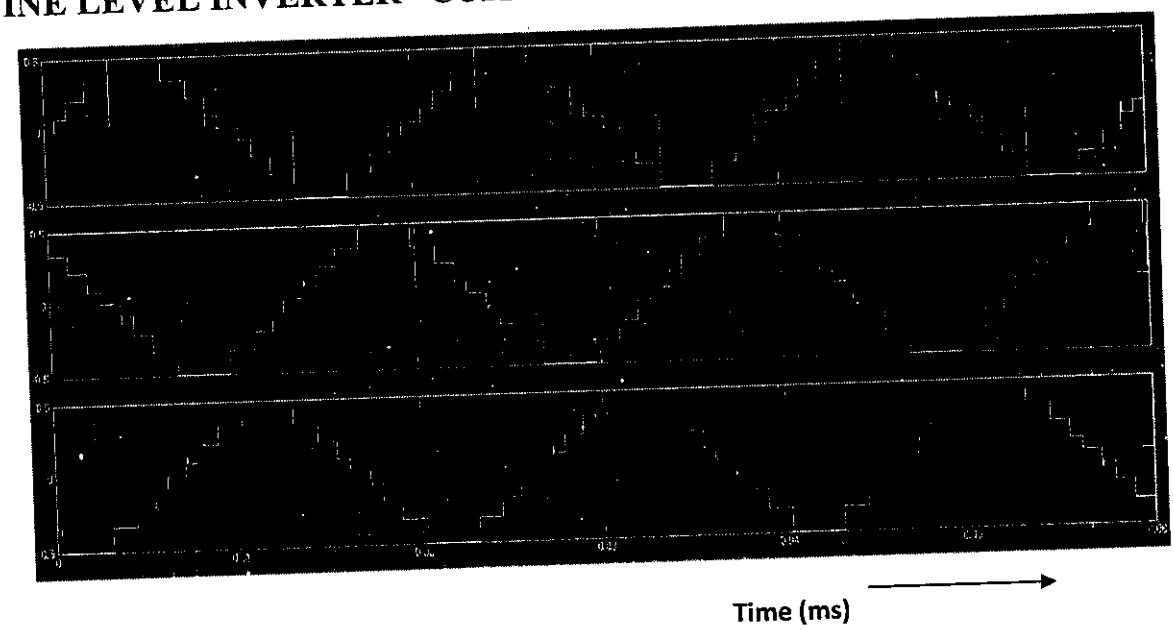
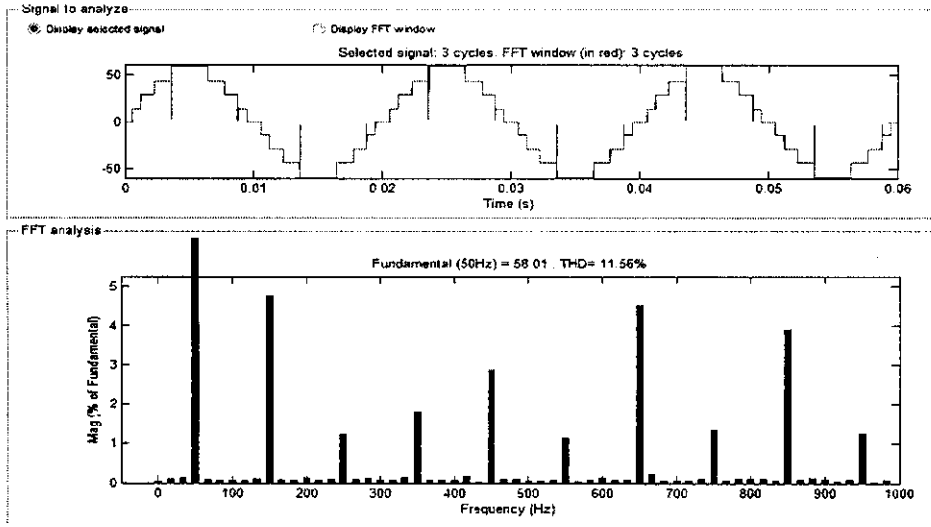


Fig 3.39. Current Waveforms Of Nine Level Inverter

3.4.2 FFT ANALYSIS

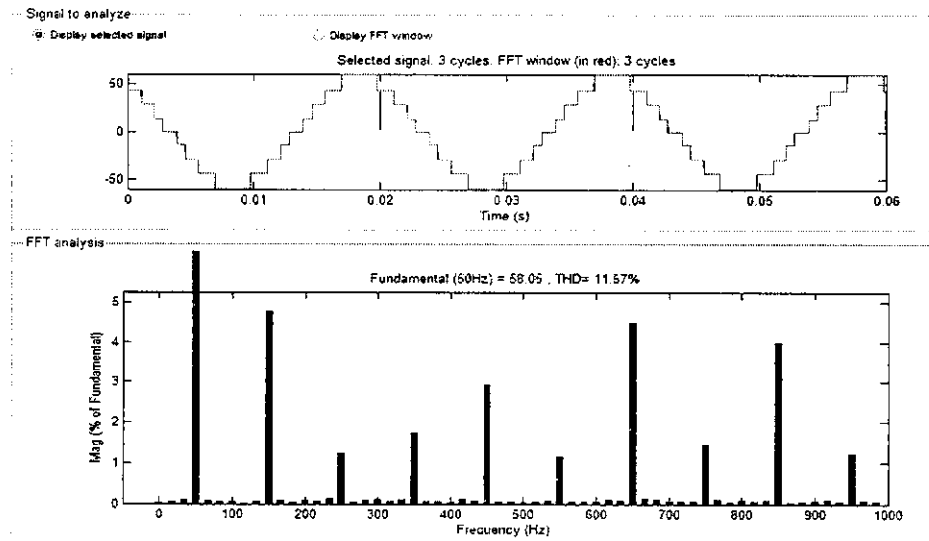
NINE LEVEL INVERTER –R PHASE FFT



THD=11.56%

Fig 3.40 FFT-R Phase

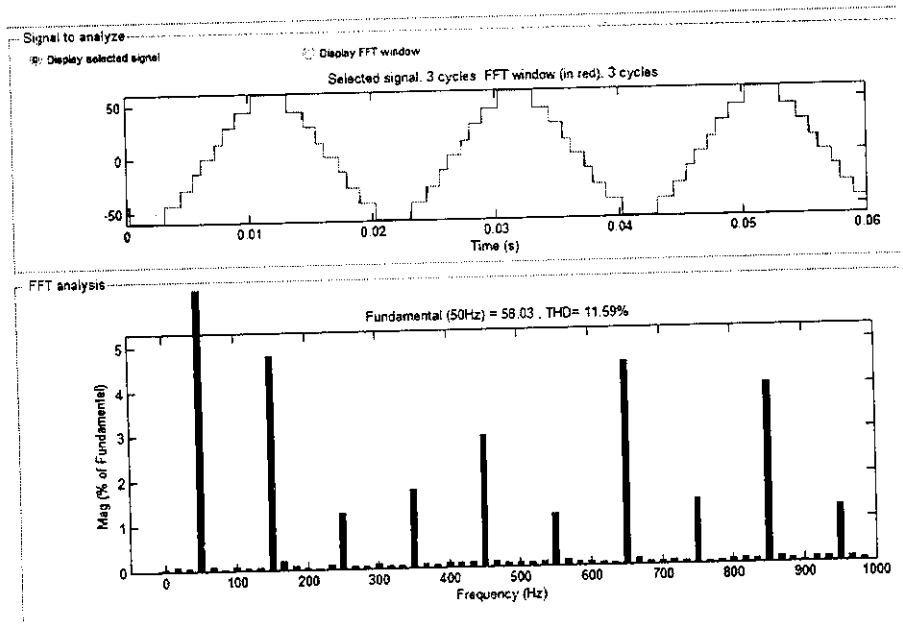
NINE LEVEL INVERTER –Y PHASE FFT



THD=11.57%

Fig 3.41 FFT-Y Phase

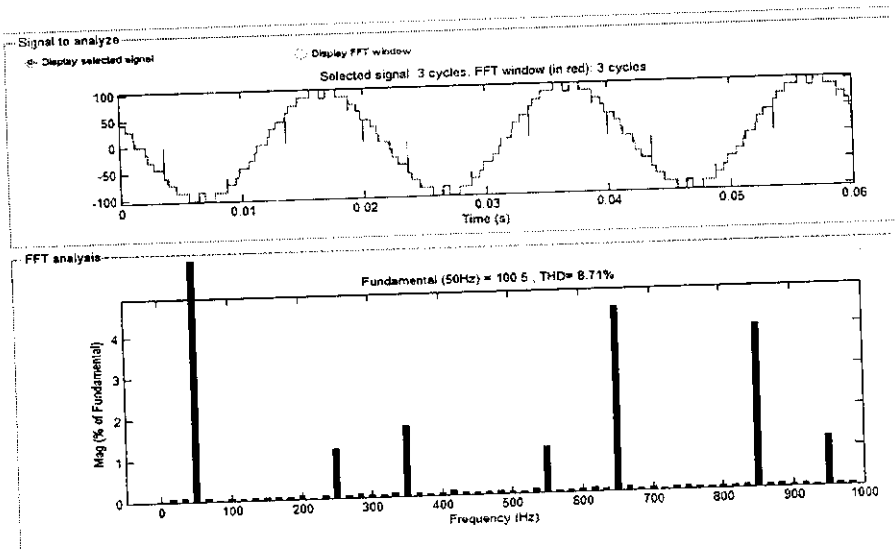
NINE LEVEL INVERTER –B PHASE FFT



THD=11.59%

Fig 3.42 FFT-B Phase

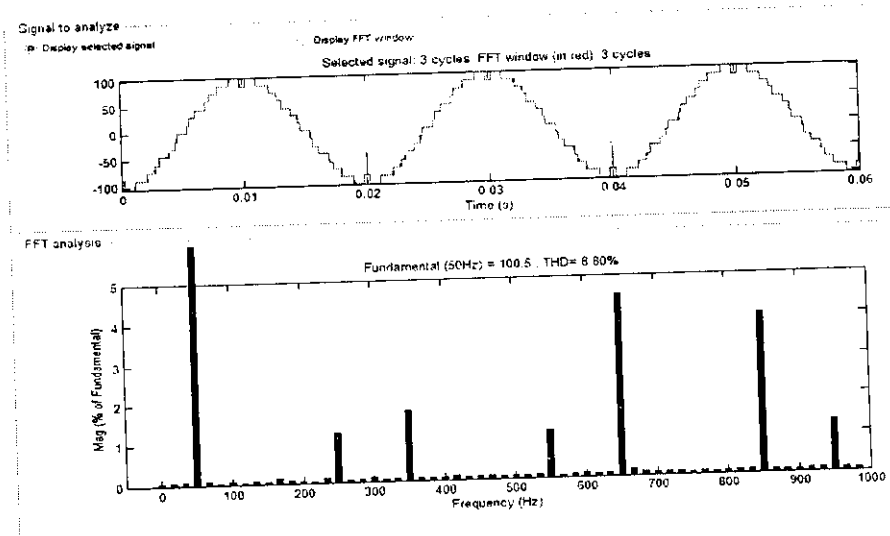
NINE LEVEL INVERTER –RY LINE FFT



THD=8.71%

Fig 3.43. FFT-RY Line

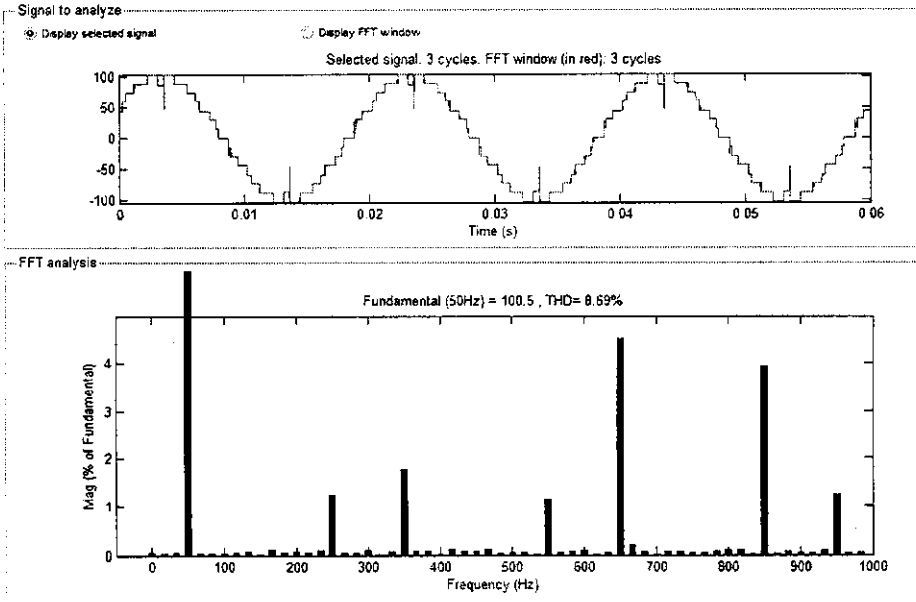
NINE LEVEL INVERTER –YB LINE FFT



THD=8.80%

Fig 3.44. FFT-YB Line

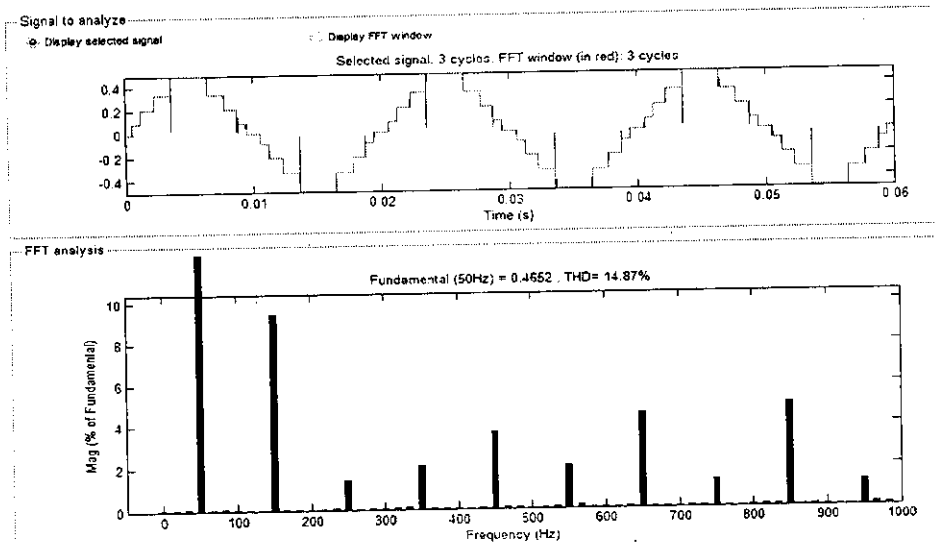
NINE LEVEL INVERTER –BR LINE FFT



THD=8.69%

Fig 3.45. FFT-BR Line

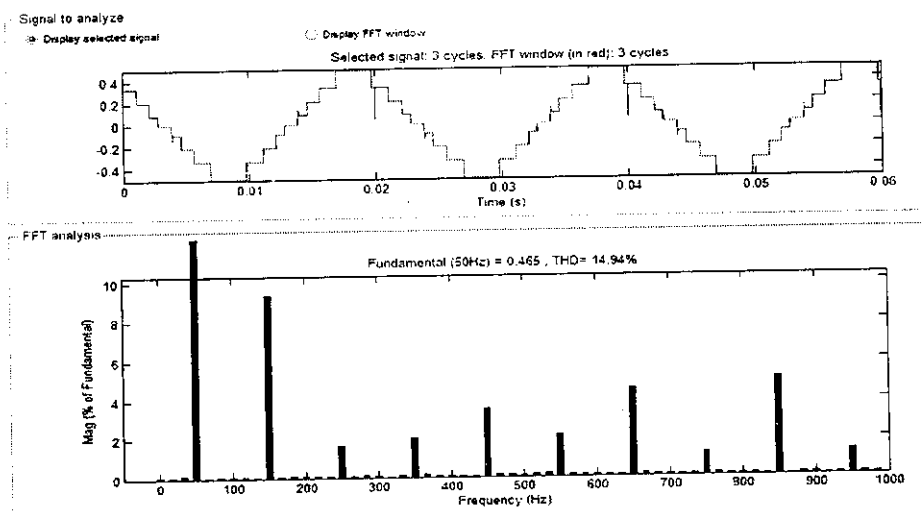
NINE LEVEL INVERTER -R PHASE CURRENT FFT



THD=14.87%

Fig 3.46. FFT-R Phase Current

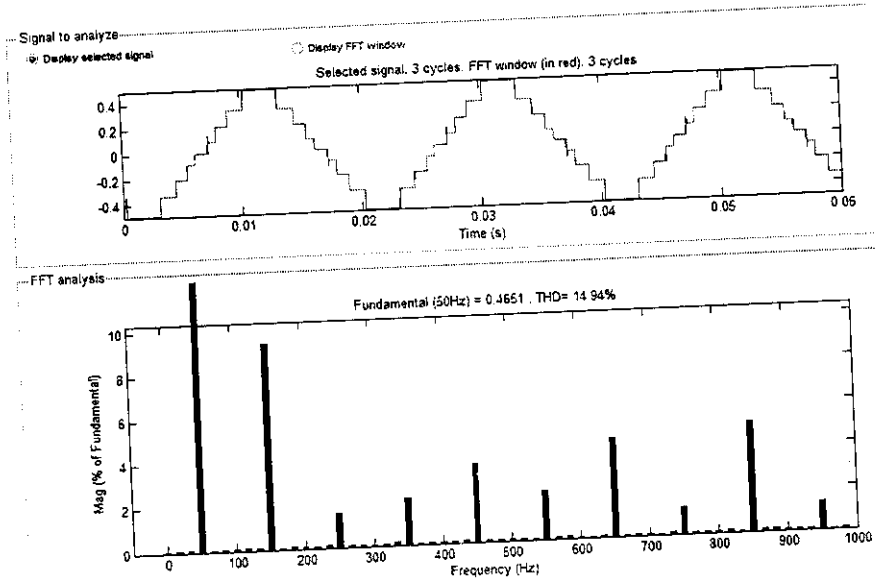
NINE LEVEL INVERTER -Y PHASE CURRENT FFT



THD=14.94%

Fig 3.47. FFT-Y Phase Current

NINE LEVEL INVERTER -B PHASE CURRENT FFT



THD=14.94%

Fig 3.48. FFT-B Phase Current

3.5 CONCLUSION

From the simulation results obtained, we have formulated the table which compares the THD values of phase and line voltages for 5-level, 7- level, 9- level and conventional inverter. And also the number of switches used for different levels are also tabulated. Here the simulation results for this topology are obtained by using optimized harmonic stepped waveform technique. This further reduces the harmonics in the system. Hence we come to the conclusion that the harmonics are considerably reduced when compared with the conventional inverter. Thus reduced THD is obtained using the least number of switching semiconductor devices.

Inverter	Phase voltage THD (%)	Line voltage THD (%)	Number of switches
5-level inverter	21.14	15.54	15
7-level inverter	14.36	9.10	18
9-level inverter	11.58	8.82	21
Conventional three phase inverter	27.51	28.03	-

CHAPTER

CHAPTER 4

HARDWARE DESCRIPTION

4.1 INTRODUCTION

The hardware for the proposed topology requires a separate MOSFET driver circuit there by increasing the overall cost. So hardware implementation is done only for single phase because of this problem. Here for single phase operation of the inverter hardware, harmonics is analyzed using a THD analyzer and the results are shown.

4.2 OVERALL BLOCK DIAGRAM

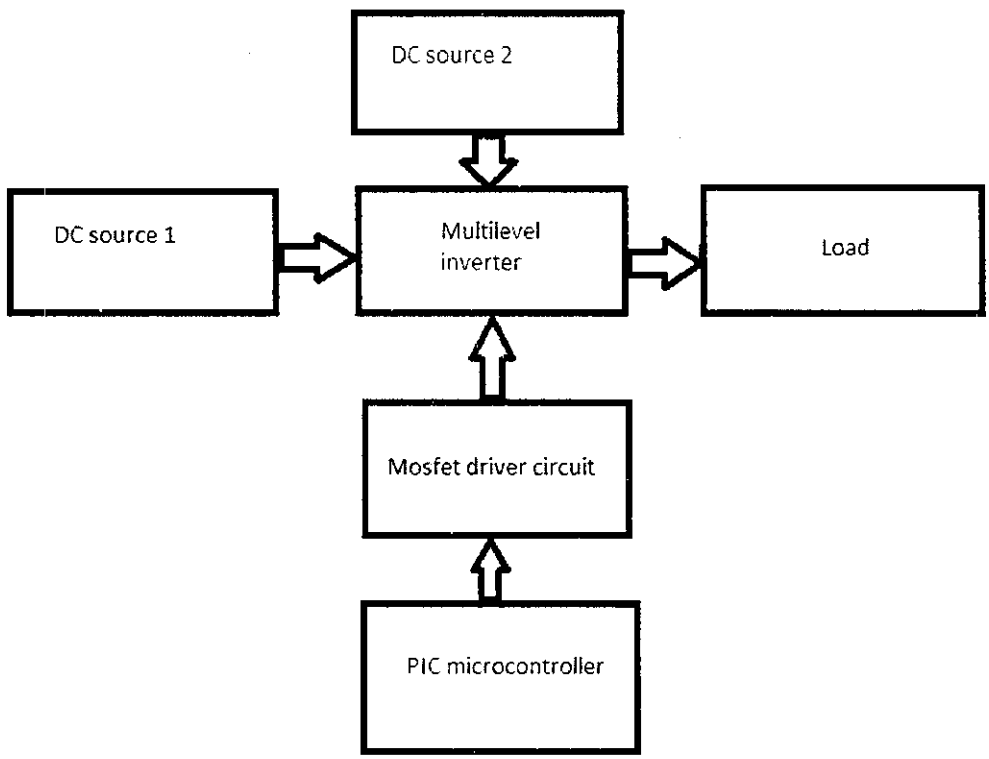


Fig 4.1. Overall block diagram

The circuit consists of the following blocks

- Power supply circuit
- H-bridge inverter circuit
- Bi-directional switching circuit
- Mosfet driver circuits
- Optoisolator circuits
- PIC microcontroller

4.3 POWER SUPPLY CIRCUIT

The ac voltage, typically 220V rms, is connected to a transformer, which steps that ac voltage down to the level of the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation.

A regulator circuit removes the ripples and also remains the same dc value even if the input dc voltage varies, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of the popular voltage regulator IC units.

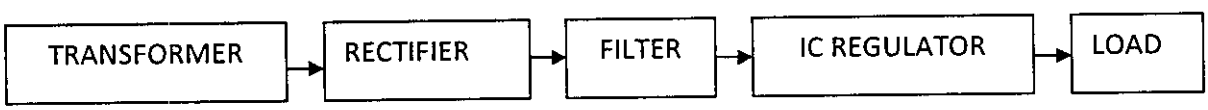


Fig 4.2. Block diagram (Power supply)

4.3.1 TRANSFORMER

The potential transformer will step down the power supply voltage (0-230V) to (0-6V) level. Then the secondary of the potential transformer will be connected to the precision rectifier, which is constructed with the help of op–amp. The advantages of using precision rectifier are it will give peak voltage output as DC, rest of the circuits will give only RMS output.

4.3.2 BRIDGE RECTIFIER

When four diodes are connected as shown in figure, the circuit is called as bridge rectifier. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners.

Let us assume that the transformer is working properly and there is a positive potential, at point A and a negative potential at point B. the positive potential at point A will forward bias D3 and reverse bias D4.

The negative potential at point B will forward bias D1 and reverse D2. At this time D3 and D1 are forward biased and will allow current flow to pass through them; D4 and D2 are reverse biased and will block current flow.

The path for current flow is from point B through D1, up through RL, through D3, through the secondary of the transformer back to point B. this path is indicated by the solid arrows. Waveforms (1) and (2) can be observed across D1 and D3.

One-half cycle later the polarity across the secondary of the transformer reverse, forward biasing D2 and D4 and reverse biasing D1 and D3. Current flow will now be from point A through D4, up through RL, through D2, through the secondary of T1, and back to point A. This path is indicated by the broken arrows. Waveforms (3) and (4) can be observed across D2 and D4. The current flow through RL is always in the same direction. In flowing through RL this current develops a voltage corresponding to that shown waveform (5). Since current flows through the load (RL) during both half cycles of the applied voltage, this bridge rectifier is a full-wave rectifier.

One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit.

This may be shown by assigning values to some of the components shown in views A and B. assume that the same transformer is used in both circuits. The peak voltage developed between points X and y is 1000 volts in both circuits. In the conventional full-wave circuit shown—in view A, the peak voltage from the center tap to either X or Y is 500 volts. Since only one diode can conduct at any instant, the maximum voltage that can be rectified at any instant is 500 volts.

The maximum voltage that appears across the load resistor is nearly-but never exceeds-500 v0lts, as result of the small voltage drop across the diode. In the bridge rectifier shown in view B, the maximum voltage that can be rectified is the full secondary voltage, which is 1000 volts. Therefore, the peak output voltage across the load resistor is nearly 1000 volts. With both circuits using the same transformer, the bridge rectifier circuit produces a higher output voltage than the conventional full-wave rectifier circuit.

4.3.3 IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milli watts to tens of watts.

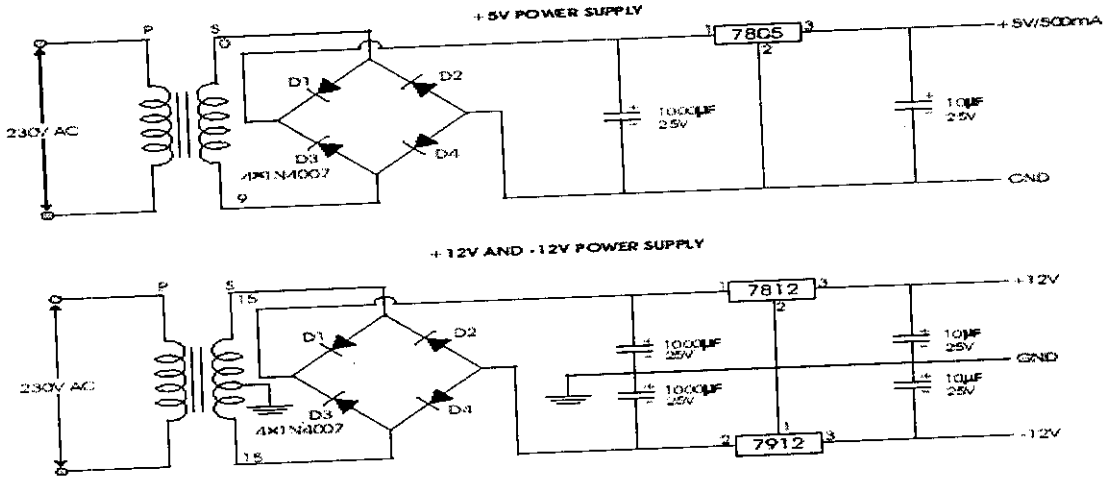


Fig 4.3. Circuit diagram (Power supply)

A fixed three-terminal voltage regulator has an unregulated dc input voltage, Vi, applied to one input terminal, a regulated dc output voltage, Vo, from a second terminal, with the third terminal connected to ground.

The series 78 regulators provide fixed positive regulated voltages from 5 to 24 volts. Similarly, the series 79 regulators provide fixed negative regulated voltages from 5 to 24 volts.

- For ICs, microcontroller, LCD --------- 5 volts
- For alarm circuit, op-amp, relay circuits ---------- 12 volts

4.4. H-BRIDGE INVERTER CIRCUIT

The circuit involves a single phase inverter that consists of four MOSFETS as switching devices. They are named as Q1, Q2, Q3, and Q4. The snubber circuit has resistors and capacitors for protecting the bridge from overvoltage and overcurrent. The load used here involves an

inductor. During the positive half cycle, MOSFETs Q1 and Q4 will conduct and Q2 and Q3 conduct during the negative half cycle.

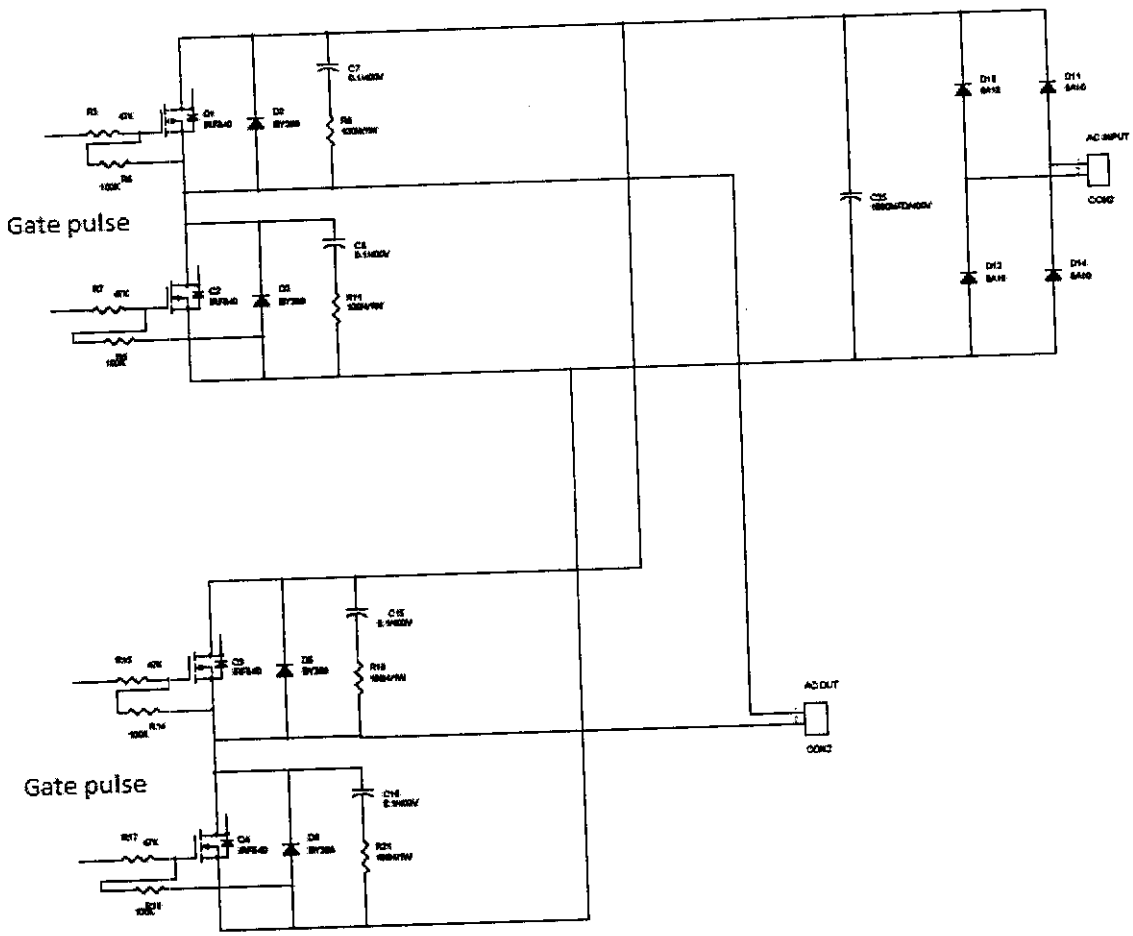


Fig 4.4. H-bridge circuit diagram

The driver circuit forms the most important part of the hardware unit because it gives the triggering pulses to the switches in proper sequence. It is used to provide 9 to 20 to switch the MOSFETs of the inverter. Driver amplifies the voltage from microcontroller which is 5 Volts.

4.5. BI-DIRECTIONAL SWITCHING CIRCUIT

There are five levels in the topology for single phase. (i.e. Vrms, Vrms/2, zero, -Vrms/2, -Vrms).And for three phase Y-phase is generated with 120 degree phase shift and B-phase with 240 degree phase shift. This is the bi-directional switching circuit generally consists of four diodes and one Mosfet which is used to generate the Vrms/2 & -Vrms/2 level of five levels.

During positive half cycle to generate +Vrms/2 level diode D7, Q12, D12 will be conducting and at negative half cycle -Vrms/2 level will be generated by the conduction of D9, Q12, D8.

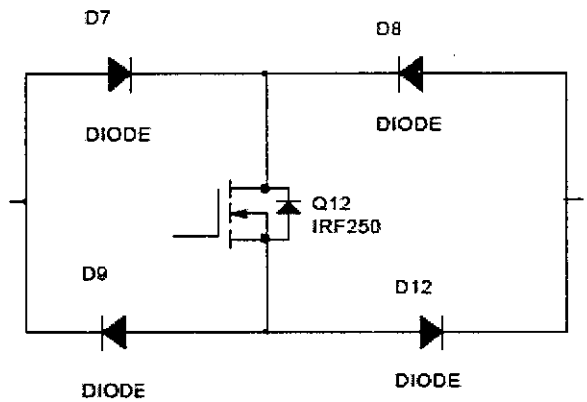


Fig 4.5. Bi-directional switching circuit

This bi-directional switching circuit is also controlled by the driver circuit which was provided signal from micro controller.

4.6. MOSFET DRIVERS

To turn a power MOSFET on, the gate terminal must be set to a voltage at least 10 volts greater than the source terminal (about 4 volts for logic level MOSFETs). This is comfortably above the Vgs(th) parameter.

One feature of power MOSFETs is that they have a large stray capacitance between the gate and the other terminals, Ciss. The effect of this is that when the pulse to the gate terminal arrives, it must first charge this capacitance up before the gate voltage can reach the 10 volts required.

The gate terminal then effectively does take current. Therefore the circuit that drives the gate terminal should be capable of supplying a reasonable current so the stray capacitance can be charged up as quickly as possible. The best way to do this is to use a dedicated MOSFET driver chip. The driver circuit used is ICL7667 and IR2110

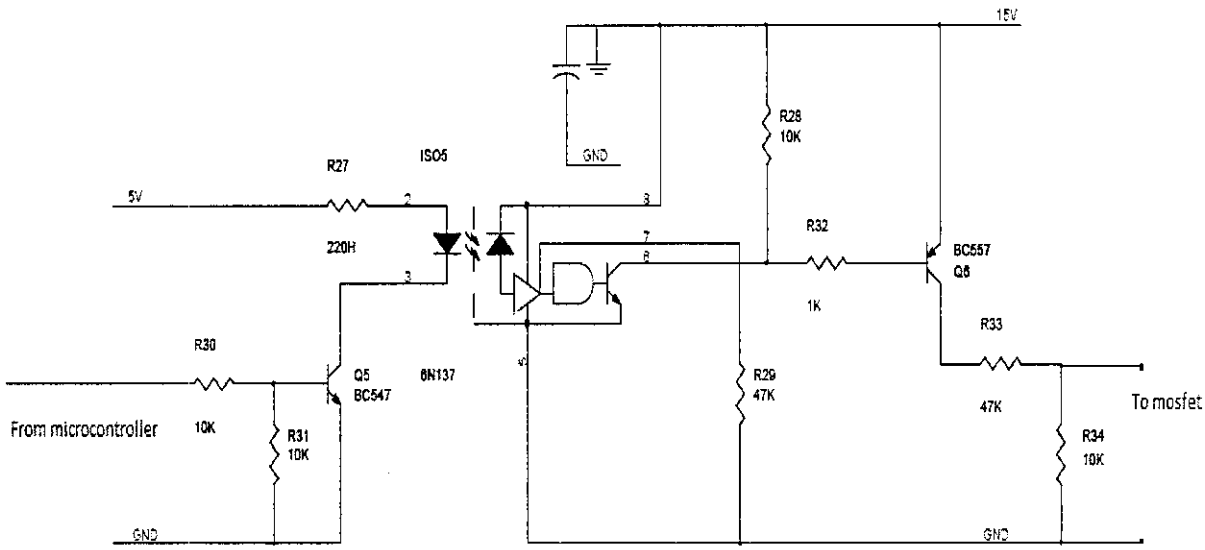


Fig 4.6. Mosfet driver circuit

4.7. OPTOISOLATOR

In electronics, an opto-isolator, also called an optocoupler, photocoupler, or optical isolator is an electronic device designed to transfer electrical signals by utilizing light waves to provide coupling with electrical isolation between its input and output. The main purpose of an

opto-isolator is "to prevent high voltages or rapidly changing voltages on one side of the circuit from damaging components or distorting transmissions on the other side." Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/μs.

Opto-isolator contains a source of light, almost always a near infrared light-emitting diode (LED), that converts electrical input signal into light, a closed optical channel (also called dielectrical channel) and a photo sensor, which detects incoming light and either generates electric energy directly, or modulates electric current flowing from an external power supply. The sensor can be a photo resistor, a photodiode, a phototransistor, a silicon-controlled rectifier (SCR) or a triac. Because LEDs can sense light in addition to emitting it, construction of symmetrical, bidirectional opto-isolators is possible. An optocoupled solid state relay contains a photodiode opto-isolator which drives a power switch, usually a complementary pair of MOSFET transistors. A slotted optical switch contains a source of light and a sensor, but its optical channel is open, allowing modulation of light by external objects obstructing the path of light or reflecting light into the sensor. The optocoupler used is 6N137 and FOD817.

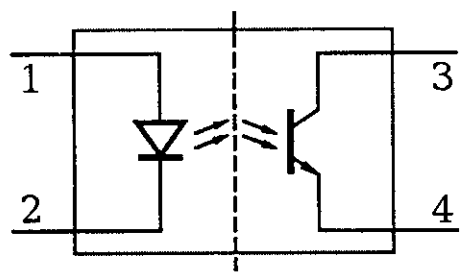


Fig 4.7. optoisolator

4.8 PIC MICROCONTROLLER

PIC 16F877 BASED CONTROL CIRCUIT

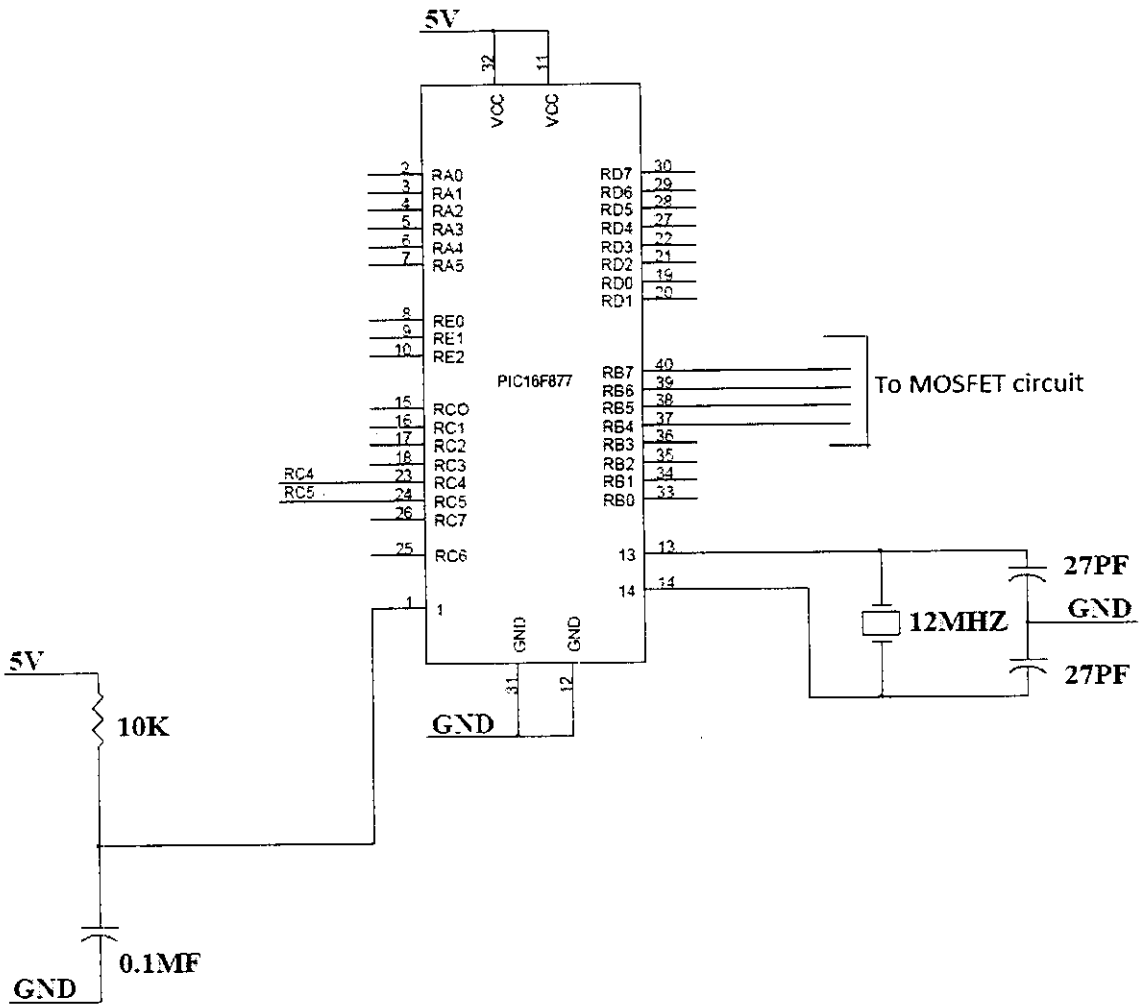


Fig 4.8. Microcontroller based control circuit

In this circuit the PIC microcontroller PIC16F877 is used. Here out of the four ports the port B is used for giving data to the MOSFET switches. In the port B pins 40, 39, 38 and 37 are used. The 5V supply to the microcontroller is given by means of the power supply

circuit. And the microcontroller input clock is given by means of external clock circuit of frequency 12MHZ to the pins 13 and 14. We also have a reset circuit of giving the external reset pulse in case of refreshing the whole control circuit. The 5V supply for the reset circuit is also provided by means of the power circuit. The data sheet of this PIC microcontroller and the microcontroller coding are provided in the appendix.

4.9 HARWARE RESULTS

4.9.1 HARDWARE PROTOTYPE

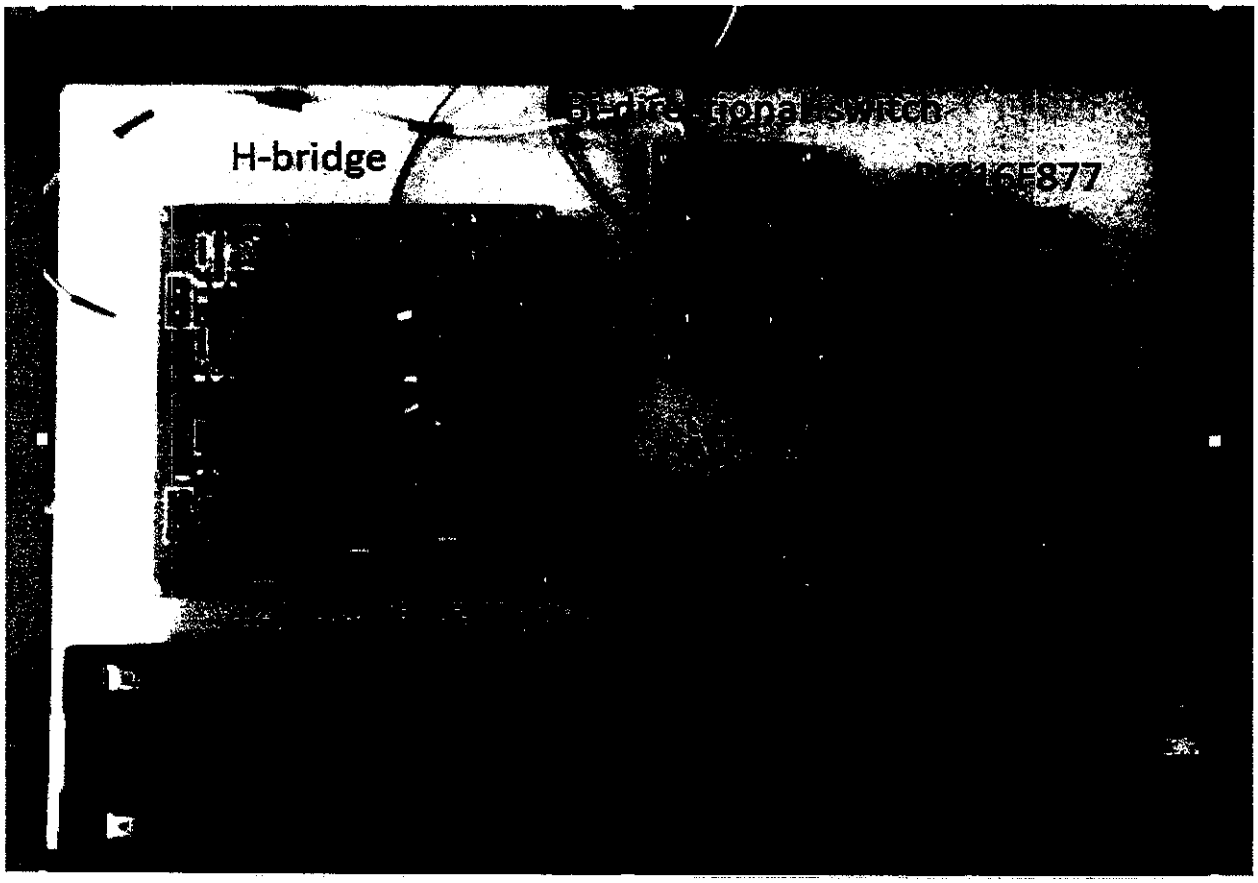


Fig 4.9. Hardware Prototype

4.9.2 OUTPUT WAVEFORM

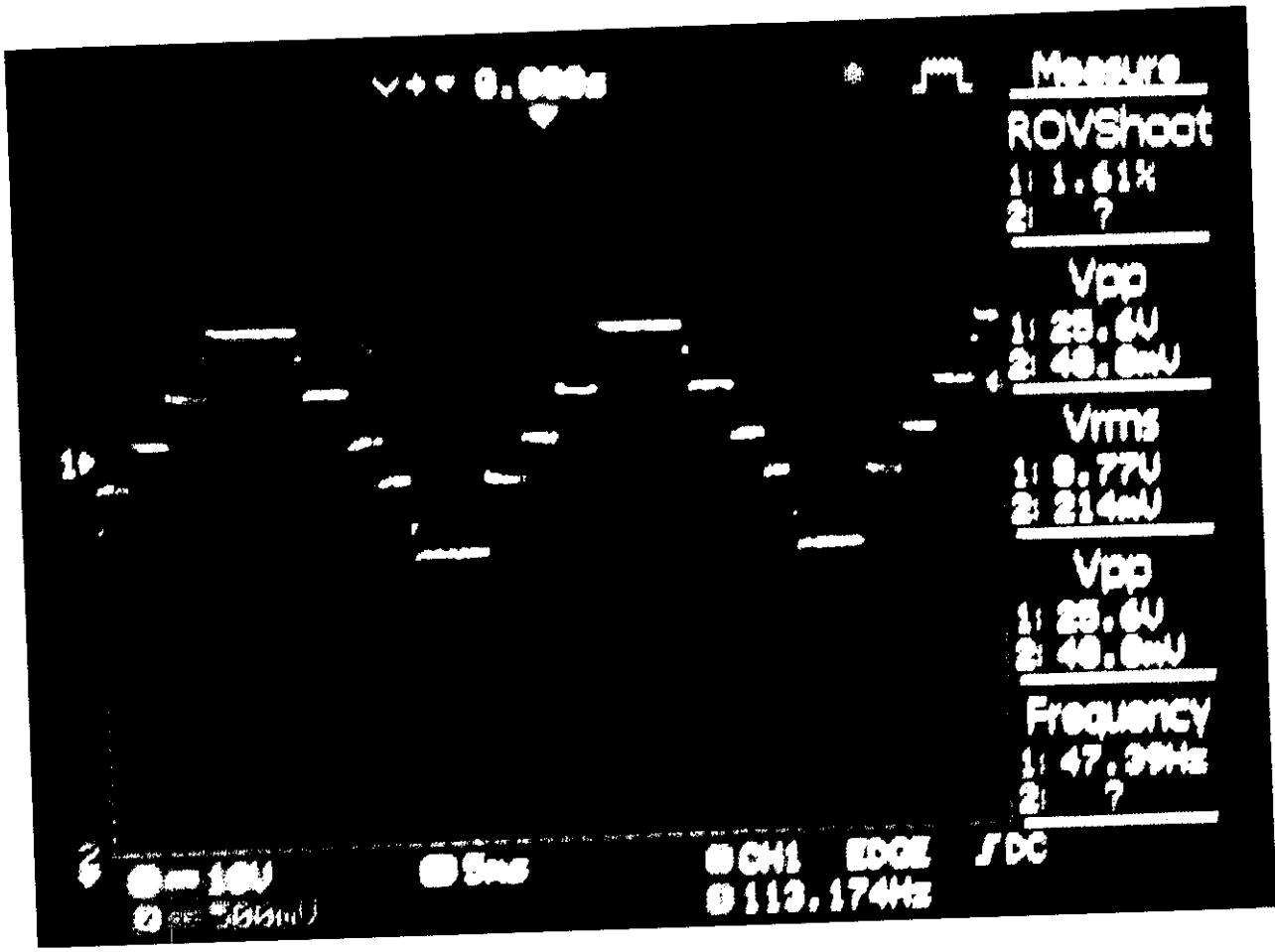


Fig 4.10. Hardware output waveform

INPUT VOLTAGE = +12V (DC voltage)

OUTPUT VOLTAGE = 24V (peak to peak voltage)

4.9.3 TOTAL HARMONIC DISTORTION ANALYSIS

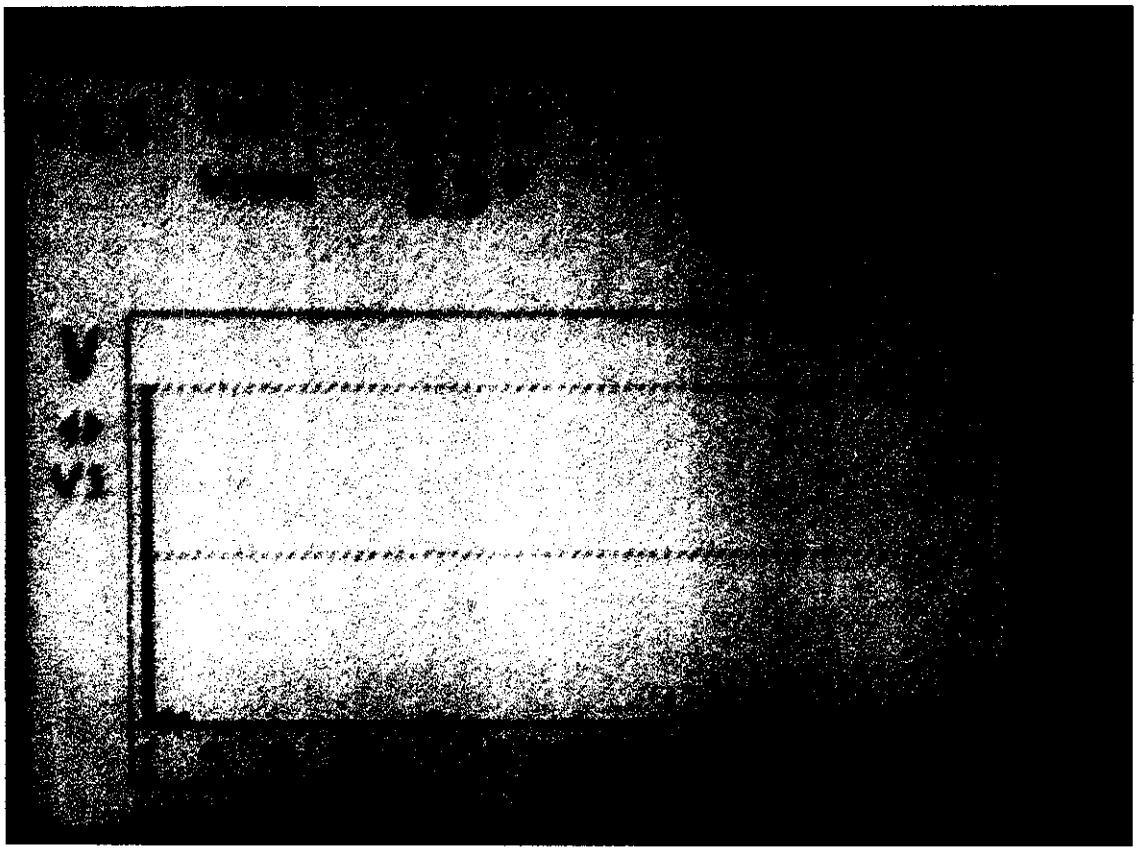


Fig 4.11. Total Harmonic Distortion Output

The output waveform from the hardware is analyzed using THD analyzer and the value of THD thus obtained is 6.3%.

CHAPTER

CHAPTER 5

CONCLUSION

5.1. CONCLUSION

Here we have obtained output for single phase multilevel inverter in the hardware. We also did THD analysis using THD analyser. Here we obtained optimized output waveform. This inverter configuration may be applied to large drive systems, UPS systems, static VAR compensation schemes, and distributed power generation involving fuel cells and photovoltaic cells. This can also be implemented using PWM and the harmonics in the system can be further reduced.

5.2. FUTURE SCOPE

This multilevel inverter configuration can be widely employed in power electronic drives because of its simple construction and minimum output distortion. Because of recent development the cost of the power electronic devices are being reduced rapidly. This can also be used in the field of renewable energy source. So this further shows the compatibility of this topology in the future.

REFERENCES

1. J. Lai and F. Peng, "Multilevel converters—a new breed of power converters," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 509-517, 1996.

2. J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverter: a survey of topologies, controls, and applications," IEEE Trans. Power Electron., vol. 49, no. 4, pp. 724–738, 2000.

3. K. Corzine, and Y. Familiant, "A new cascaded multilevel H0bridge drive," IEEE Trans. Power Electron., vol. 17, no. 1, pp. 125–131, 2002.

4. T. Abdelhamid, and N. Abbasy, "A new topology of three-phase five level inverter applied to static var generation schemes," International Review of Electrical Engineering Journal, vol. 2, no. 3, pp. 359-368, 2006.

5. G. Su, "Multilevel DC-link inverter," IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 848–854, 2005.

6. D. Soto-Sanchez and T. Green, "Voltage balance and control in a multi-level unified power flow controller," IEEE Trans. Power Delivery, vol. 16, no. 4, pp. 732–738, 2001.

7. Z. Du, L. Tolbert, and J. Chiasson, "Harmonic elimination for multilevel converter with programmed PWM method," Proc. of the IEEE Industry Applications Annual Meeting Conference, 2004, pp. 2210–2215.

APPENDIX A

APPENDIX A

PIC MICROCONTROLLER

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complementary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

PIN DIAGRAM OF PIC 16F877

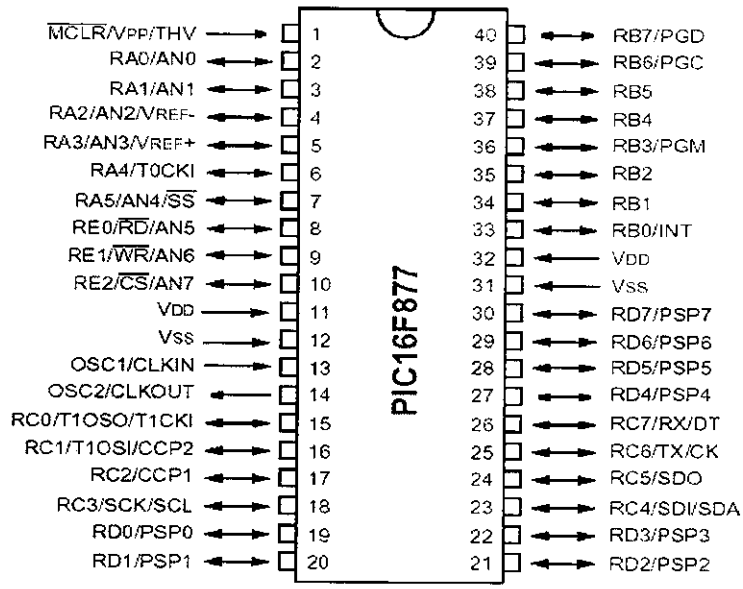


TABLE SPECIFICATIONS

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn

- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input

  DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,

  Up to 368 x 8 bytes of Data Memory (RAM)

  Up to 256 x 8 bytes of EEPROM data memory
- Pin out compatible to the PIC16C73/74/76/77
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins

• Processor read/write access to program memory

• Wide operating voltage range: 2.5V to 5.5V

• High Sink/Source Current: 25 mA

• Commercial and Industrial temperature ranges

• Low-power consumption:

< 2mA typical @ 5V, 4 MHz

20mA typical @ 3V, 32 kHz

< 1mA typical standby current

PERIPHERAL FEATURES:

• Timer0: 8-bit timer/counter with 8-bit prescaler

• Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep

Via external crystal/clock

• Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler

• Two Capture, Compare, PWM modules

Capture is 16-bit, max resolution is 12.5 ns,

Compare is 16-bit, max resolution is 200 ns,

PWM max. Resolution is 10-bit

• 10-bit multi-channel Analog-to-Digital converter

• Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)

• Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with

9- Bit addresses detection.

- Brown-out detection circuitry for Brown-out Reset (BOR).

APPENDIX

```
TMR1ON=1;count=0;


RC0=0;RC1=1;
while(1)
{
//      PORTB=0x00;
//      while(!count);count=0;
        PORTB=0x01;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x02;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x03;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x04;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x05;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x06;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x07;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x06;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x05;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x04;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
        PORTB=0x03;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;
```

```
        PORTB=0x02;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC3=~RC3;RC4=~RC4;

        PORTB=0x01;TMR1H=0X0f;TMR1L=0Xaf;count=0;TMR1ON=1;while(!count);TMR1
ON=0;RC0=~RC0;RC1=~RC1;

}

}
```

Dual Power MOSFET Driver

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

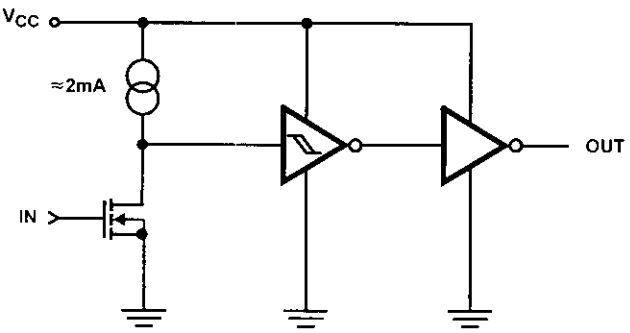
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7667CBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7667CPA	0 to 70	8 Ld PDIP	E8.3
ICL7667CJA	0 to 70	8 Ld CERDIP	F8.3A
ICL7667CTV	0 to 70	8 Pin Metal Can	T8.C
ICL7667MTV (Note 1)	-55 to 125	8 Pin Metal Can	T8.C
ICL7667MJA (Note 1)	-55 to 125	8 Ld CERDIP	F8.3A

NOTE:

1. Add /883B to Part Number for 883B Processing

Functional Diagram



Features

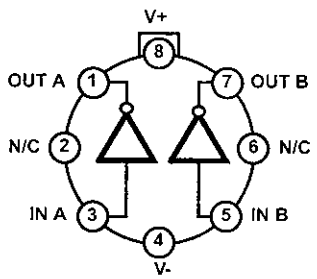
- Fast Rise and Fall Times
  - 30ns with 1000pF Load
- Wide Supply Voltage Range
  - V_{CC} = 4.5V to 15V
- Low Power Consumption
  - 4mW with Inputs Low
  - 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - R_{OUT} = 7Ω Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426

Applications

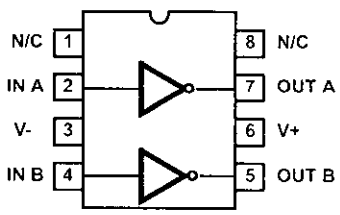
- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Pinouts

ICL7667 (CAN)
TOP VIEW



ICL7667 (PDIP, SOIC, CERDIP)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage V+ to V- 15V
Input Voltage . . . . . V- -0.3V to V+ +0.3V
Package Dissipation, T_A 25°C 500mW

Operating Temperature Range

ICL7667C . . . . . 0°C to 70°C
ICL7667M . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC}(°
PDIP Package	150	N
SOIC Package	170	N
Metal Can Package	156	6
CERDIP Package	115	3

Maximum Storage Temperature Range . . . . . -65°C to
Maximum Lead Temperature (Soldering 10s) 3
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

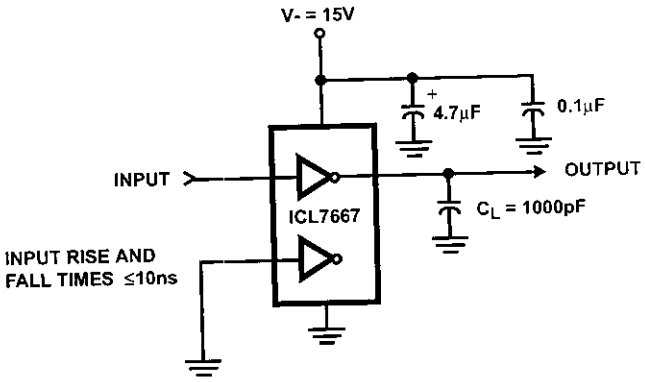
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

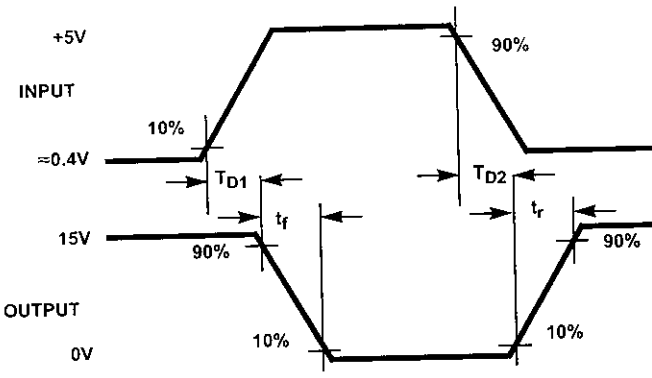
Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = 25°C			ICL7667M -55°C ≤ T_A ≤ 125°C			UN
			MIN	TYP	MAX	MIN	TYP	MAX	
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V_{CC} = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V_{CC} = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µ
Output Voltage High	V_{OH}	V_{CC} = 4.5V and 15V	V_{CC} -0.05	V_{CC}	-	V_{CC} -0.1	V_{CC}	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V_{CC} = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V_{CC} = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	m
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µ
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	Figure 3	-	35	50	-	-	60	n
Rise Time	T_R	Figure 3	-	20	30	-	-	40	n
Fall Time	T_F	Figure 3	-	20	30	-	-	40	n
Delay Time	T_{D1}	Figure 3	-	20	30	-	-	40	n

NOTE: All typical values have been characterized but are not tested.

Test Circuits





Typical Performance Curves

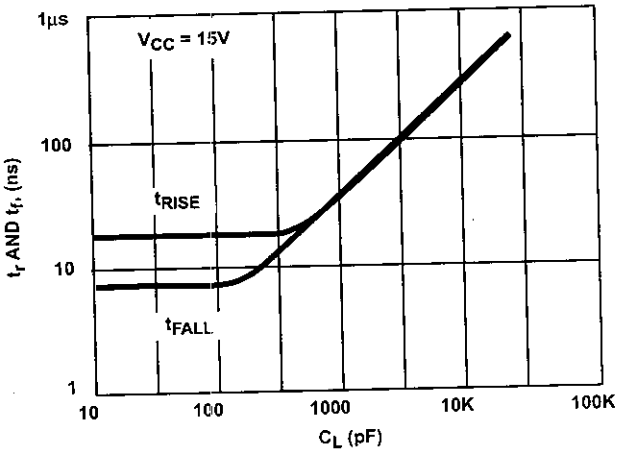


FIGURE 1. RISE AND FALL TIMES vs C_L

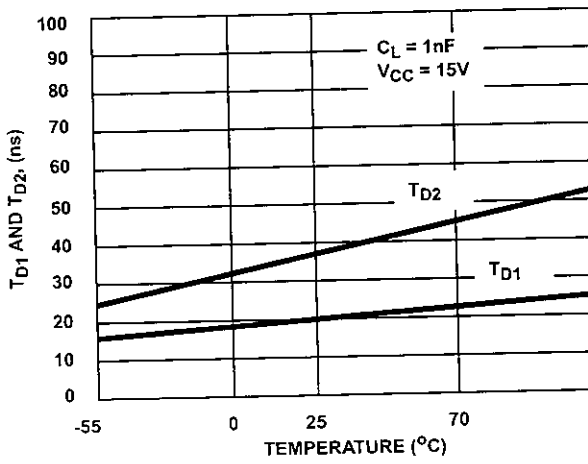


FIGURE 2. T_{D1}, T_{D2} vs TEMPERATURE

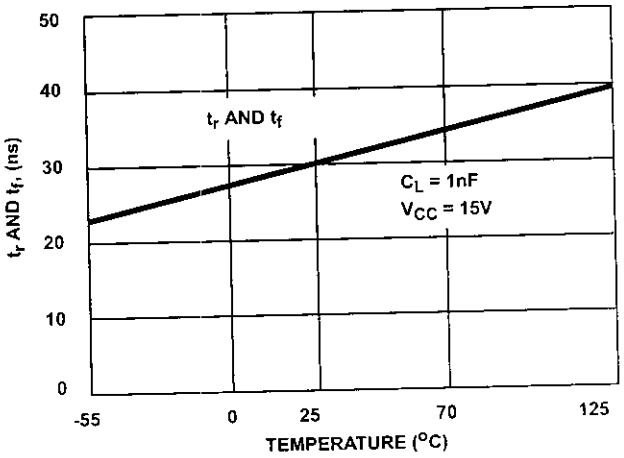


FIGURE 3. t_r, t_f vs TEMPERATURE

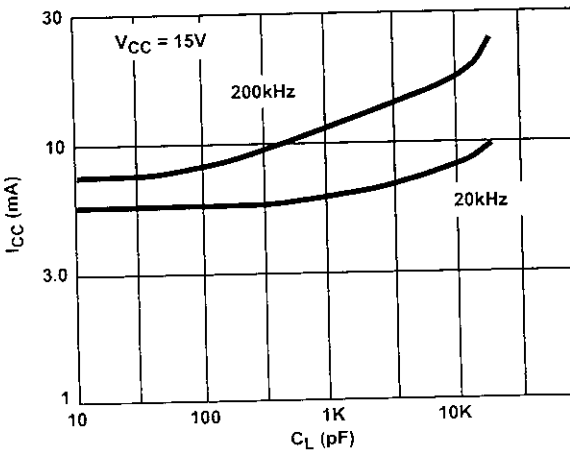


FIGURE 4. I_{CC} vs C_L

Typical Performance Curves (Continued)

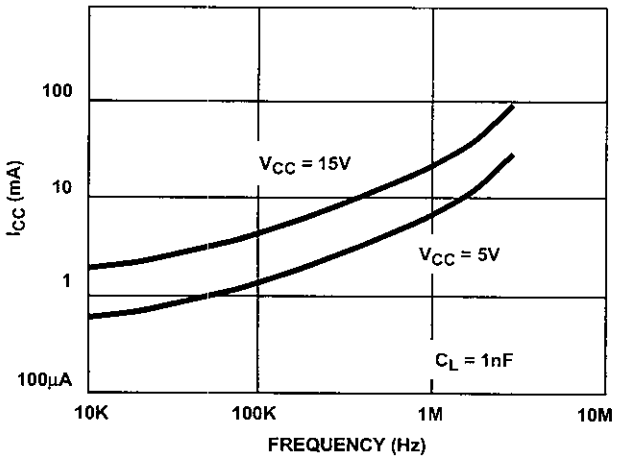


FIGURE 5. I_{CC} vs FREQUENCY

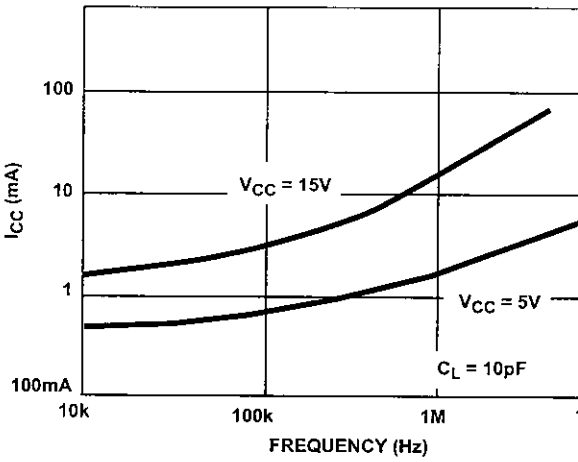


FIGURE 6. NO LOAD I_{CC} vs FREQUENCY

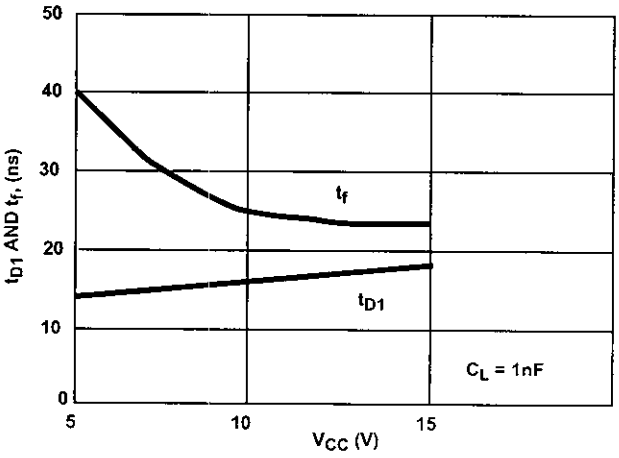


FIGURE 7. DELAY AND FALL TIMES vs V_{CC}

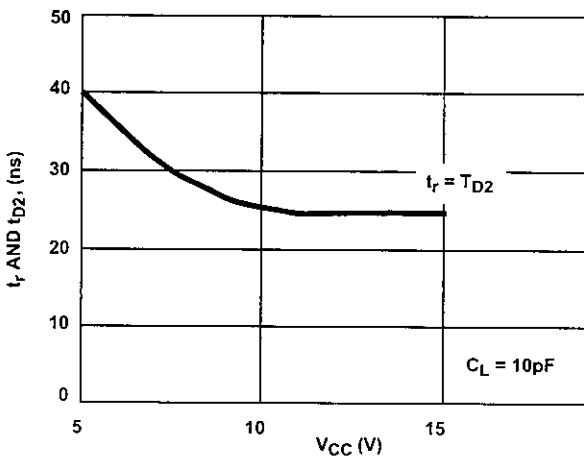


FIGURE 8. RISE TIME vs V_{CC}

Detailed Description

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at V_{CC} = 15V, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a large N-Channel FET with a P-char constant-current source. This circuit has a threshold of al 1.5V, relatively independent of the VCC voltage. This me that the inputs will be directly compatible with TTL over t entire 4.5V - 15V V_{CC} range. Being CMOS, the inputs d less than 1µA of current over the entire input voltage ran of ground to V_{CC}. The quiescent current or no load supp current of the ICL7667 is affected by the input voltage, g to nearly zero when the inputs are at the 0 logic level an rising to 7mA maximum when both inputs are at the 1 lo level. A small amount of hysteresis, about 50mV to 100m the input, is generated by positive feedback around the second stage.

Output Stage

The ICL7667 output is a high-power CMOS inverter, swinging between ground and VCC. At V_{CC} = 15V, the output impedance of the inverter is typically 7Ω. The hig

eak current capability of the ICL7667 enables it to drive a 000pF load with a rise time of only 40ns. Because the utput stage impedance is very low, up to 300mA will flow rough the series N-Channel and P-channel output devices from V_{CC} to ground) during output transitions. This crossover urrent is responsible for a significant portion of the internal ower dissipation of the ICL7667 at high frequencies. It can be inimized by keeping the rise and fall times of the input to the CL7667 below 1µs.

Application Notes

Although the ICL7667 is simply a dual level-shifting inverter, here are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize and common impedance in the ground return. Since the CL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close o the ICL7667 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use a 10Ω to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
4. Use good bypassing techniques to prevent supply voltage ringing.

Power Dissipation

The power dissipation of the ICL7667 has three main components:

5. Input inverter current loss
6. Output stage crossover current loss
7. Output stage I^2R power loss

The sum of the above must stay within the specified limits f reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.1mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N-Channel and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should nev be allowed to remain between V_{IL} and V_{IH} since this coul leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drive is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply curre drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more th the product of the output current times the voltage drop across the output device. In addition to the current drawn any resistive load, there will be an output current due to th charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipati is approximately

$$P_{AC} = CV_{CC}^2f$$

where C = Load Capacitance, f = Frequency

In cases where the load is a power MOSFET and the gat drive requirement are described in terms of gate charge, t ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

where Q_G = Charge required to switch the gate, in Coulombs, f = Frequency.

Power MOS Driver Circuits

Power MOS Driver Requirements

Because it has a very high peak current output, the ICL76 the at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 9 is a typical curve of charge vs gate voltage for a power MOSF The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs whil the power MOSFET is in the linear region and is dissipati significant amounts of power. The very high current outpu the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off

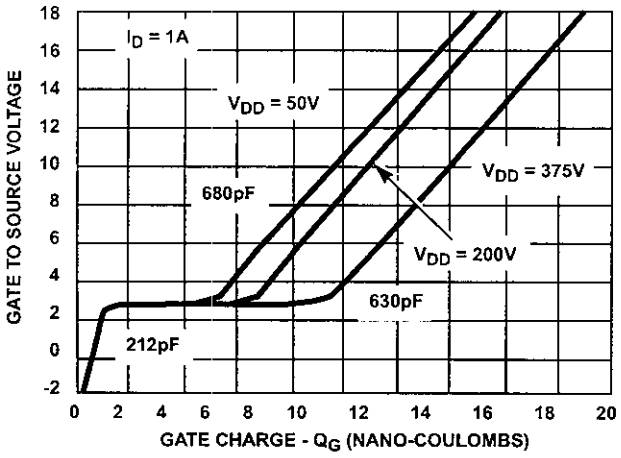


FIGURE 9. MOSFET GATE DYNAMIC CHARACTERISTICS

Direct Drive of MOSFETs

Figure 11 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The SG1527 IC is the same as the SG1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

Transformer Coupled Drive of MOSFETs

Transformers are often used for isolation between the lo and control section and the power section of a switching regulator. The high output drive capability of the ICL766 enables it to directly drive such transformers. Figure 11 shows a typical transformer coupled drive circuit. PWM with either active high or active low output can be used this circuit, since any inversion required can be obtained reversing the windings on the secondaries.

Buffered Drivers for Multiple MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very l and it can be difficult to charge and discharge quickly. Fig 13 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, C held in conduction by the lower half of the ICL7667 and C clamped off by Q_1. When the input goes positive, Q_1 is tu off and a current pulse is applied to the gate of Q_2 by the upper half of the ICL7667 through the transformer, T_1. Af about 20ns, T_1 saturates and Q_2 is held on by its own C_G and the bootstrap circuit of C_1, D_1 and R_1. This bootstrap circuit may not be needed at frequencies greater than 10 since the input capacitance of Q_2 discharges slowly.

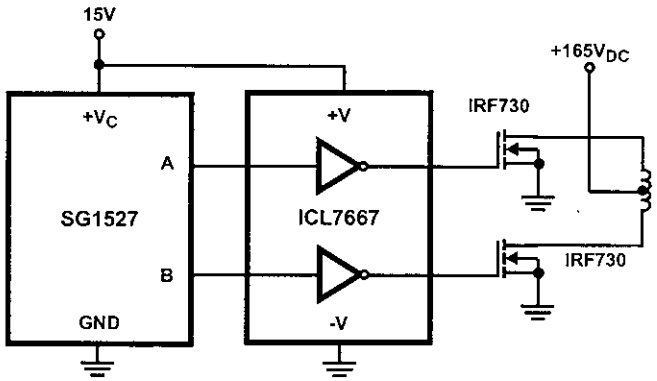


FIGURE 10A.

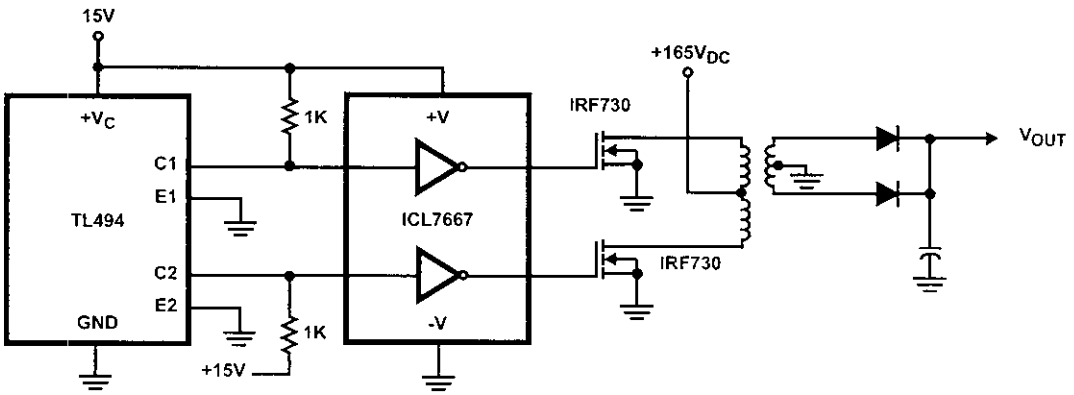


FIGURE 10B.

FIGURE 10. DIRECT DRIVE OF MOSFET GATES

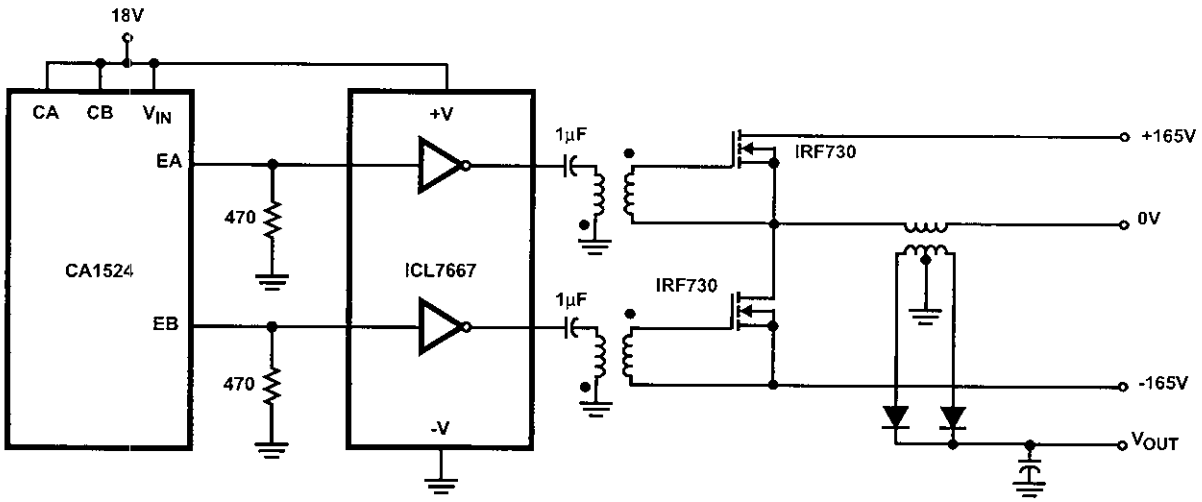


FIGURE 11. TRANSFORMER COUPLED DRIVE CIRCUIT

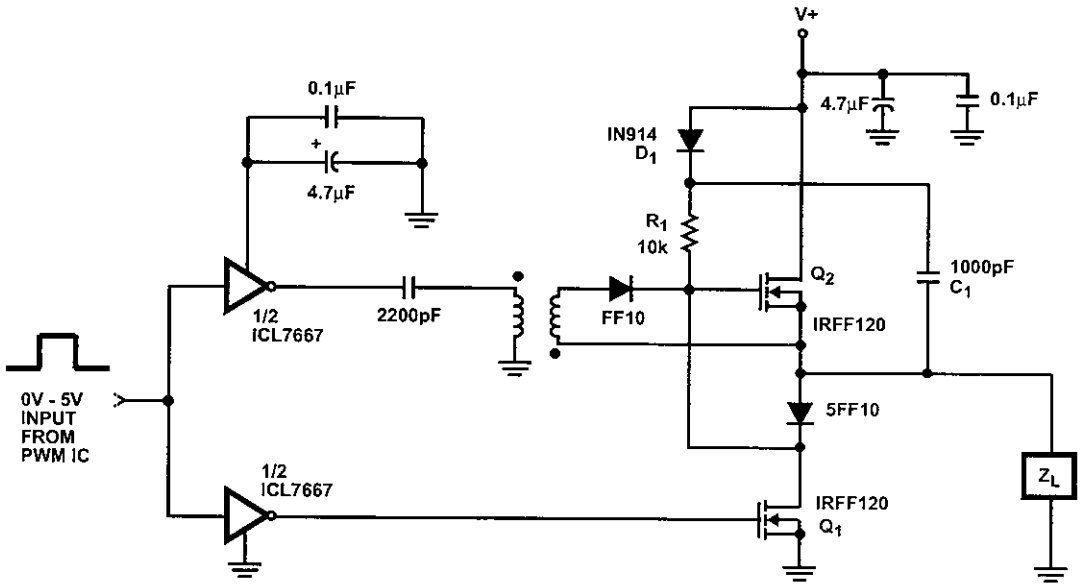


FIGURE 12. VERY HIGH SPEED DRIVER

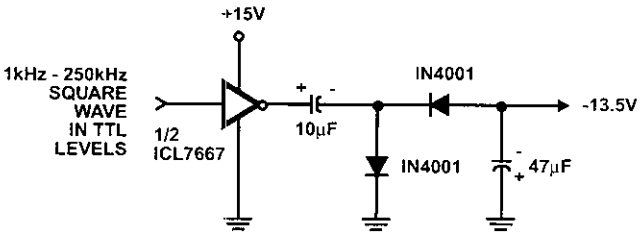


FIGURE 13A.

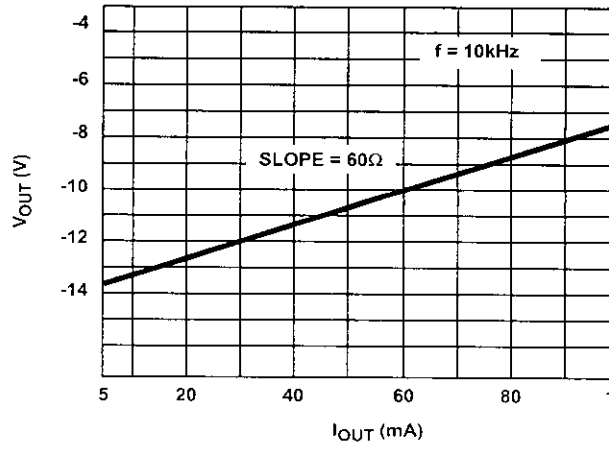


FIGURE 13B. OUTPUT CURRENT vs OUTPUT VOLTAGE

FIGURE 13. VOLTAGE INVERTER

Other Applications

Relay and Lamp Drivers

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

Charge Pump or Voltage Inverters and Doublers

The low output impedance and wide VCC range of the ICL7667 make it well suited for charge pump circuits. Figure 13A shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 14, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 13 would be to supply the higher voltage needed for EEPROM or EPROM programming.

Clock Driver

Some microprocessors (such as the CDP68HC05 famili use a clock signal to control the various LSI peripherals the family. The ICL7667s combination of low propagatio delay, high current drive capability and wide voltage swi make it attractive for this application. Although the ICL7 is primarily intended for driving power MOSFET gates a 15V, the ICL7667 also works well as a 5V high-speed bu Unlike standard 4000 series CMOS, the ICL7667 uses s channel length FETs and the ICL7667 is only slightly slo at 5V than at 15V.

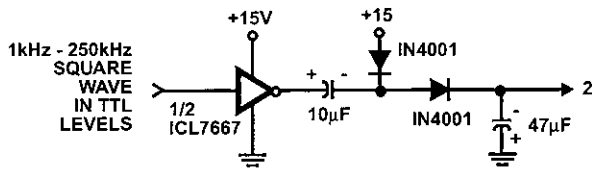


FIGURE 14. VOLTAGE DOUBLER

International
IOR Rectifier

Data Sheet No. PD60147 Rev.T

IR2110(S)/IR2113(S) & (PbF)

HIGH AND LOW SIDE DRIVER

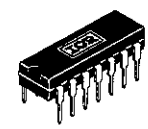
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Also available LEAD-FREE

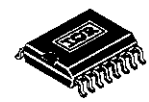
Product Summary

V_{OFFSET}	(IR2110)	500V max.
	(IR2113)	600V max.
I_O+/-		2A / 2A
V_{OUT}		10 - 20V
$t_{on/off}$ (typ.)		120 & 94 ns
Delay Matching	(IR2110)	10 ns max.
	(IR2113)	20ns max.

Packages



14-Lead PDIP
IR2110/IR2113

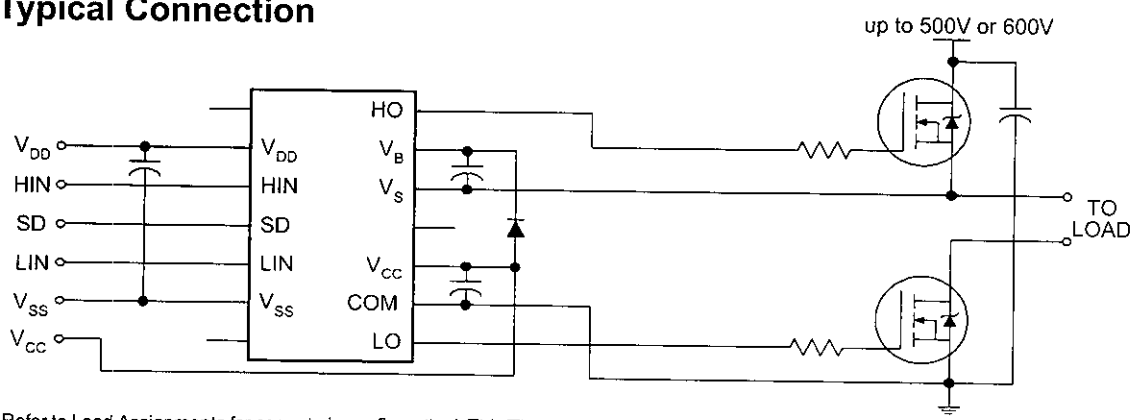


16-Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage	(IR2110)	-0.3	525	V
		(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply absolute voltage		V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	(IR2110)	Note 1	500	
		(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side fixed supply voltage		10	20	
V_{LO}	Low side output voltage		0	VCC	
V_{DD}	Logic supply voltage		V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage		-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS}	V_{DD}	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When V_{DD} < 5V, the minimum V_{SS} offset is limited to -V_{DD}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

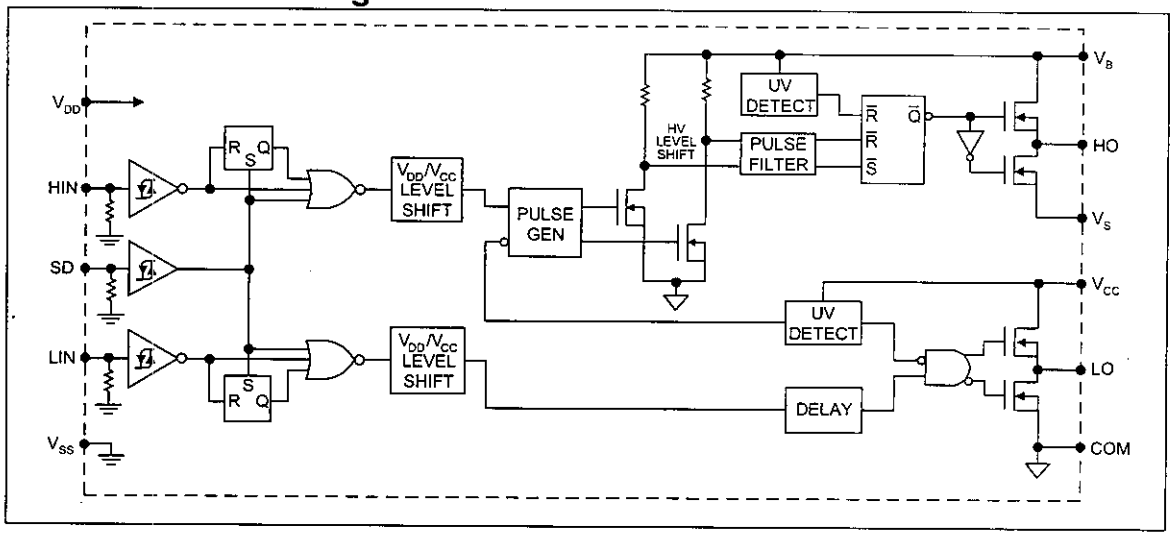
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-off propagation delay	8	—	94	125		V_S = 500V/600V
t_{sd}	Shutdown propagation delay	9	—	110	140		V_S = 500V/600V
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off (IR2110)	—	—	—	10		
	Delay matching, HS & LS turn-on/off (IR2113)	—	—	—	20		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	16	—	—	50	µA	V_B=V_S = 500V/600V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

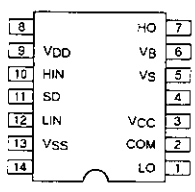
Functional Block Diagram



Lead Definitions

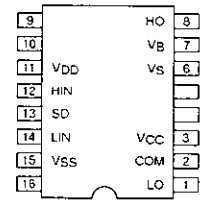
Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14 Lead PDIP

IR2110/IR2113



16 Lead SOIC (Wide Body)

IR2110S/IR2113S

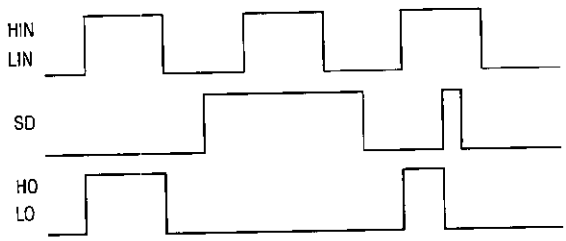


Figure 1. Input/Output Timing Diagram

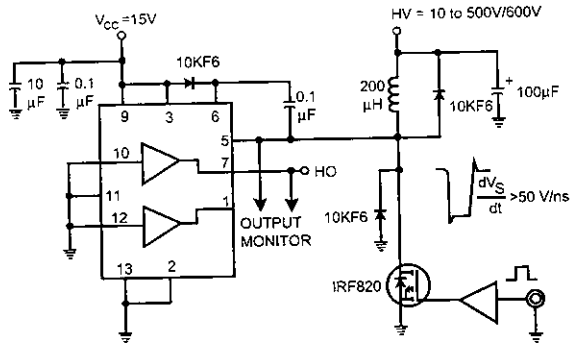


Figure 2. Floating Supply Voltage Transient Test Circuit

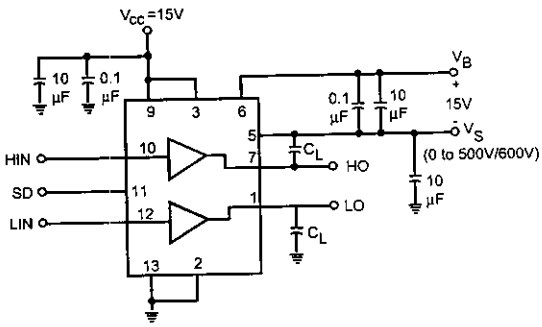


Figure 3. Switching Time Test Circuit

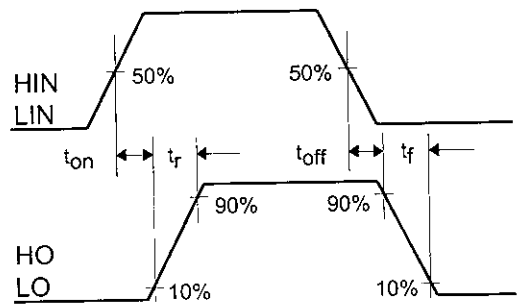


Figure 4. Switching Time Waveform Definition

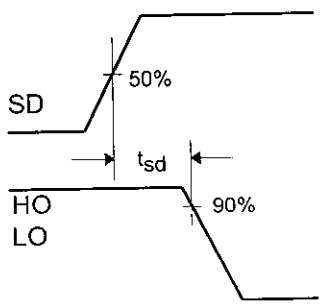


Figure 5. Shutdown Waveform Definitions

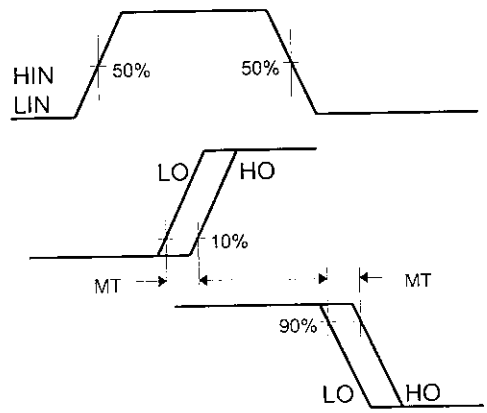


Figure 6. Delay Matching Waveform Definitions

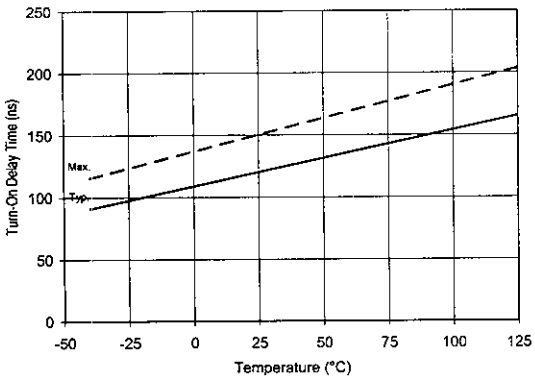


Figure 7A. Turn-On Time vs. Temperature

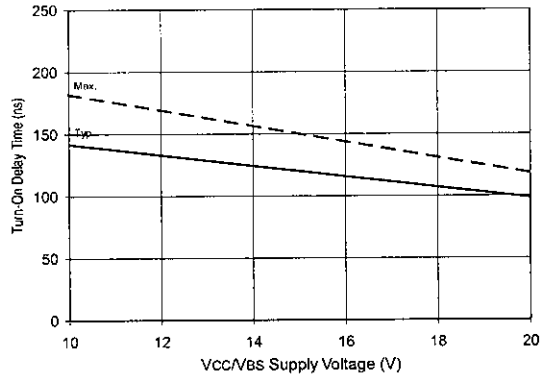


Figure 7B. Turn-On Time vs. Vcc/VBS Supply Voltage

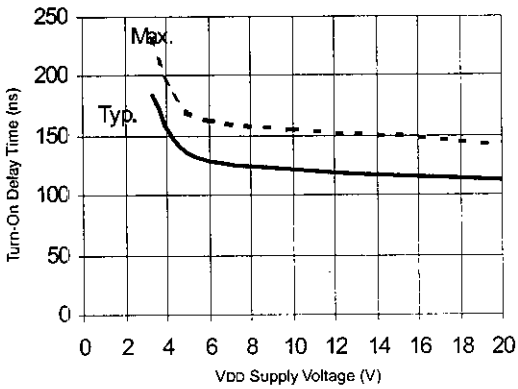


Figure 7C. Turn-On Time vs. VDD Supply Voltage

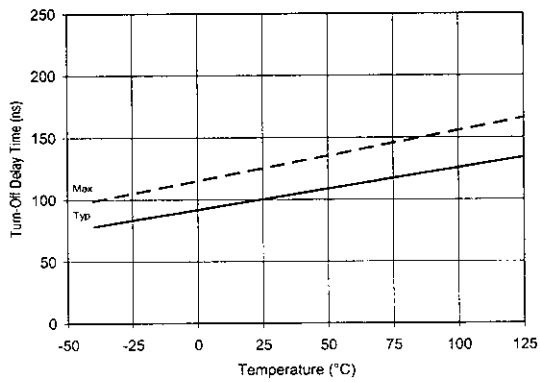


Figure 8A. Turn-Off Time vs. Temperature

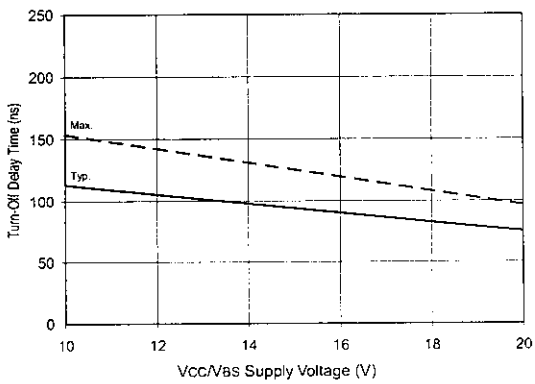


Figure 8B. Turn-Off Time vs. Vcc/VBS Supply Voltage

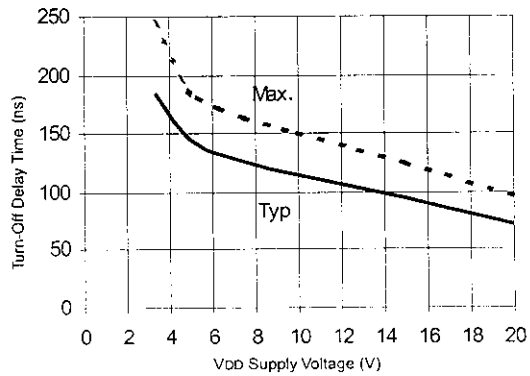


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

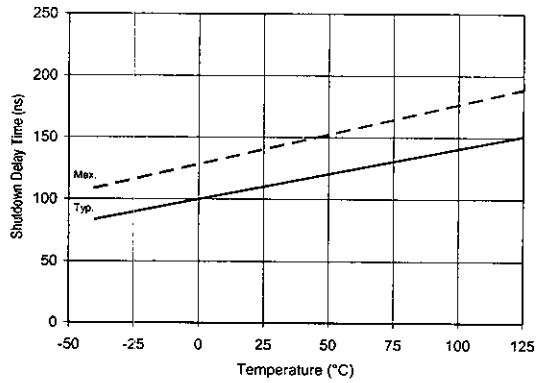


Figure 9A. Shutdown Time vs. Temperature

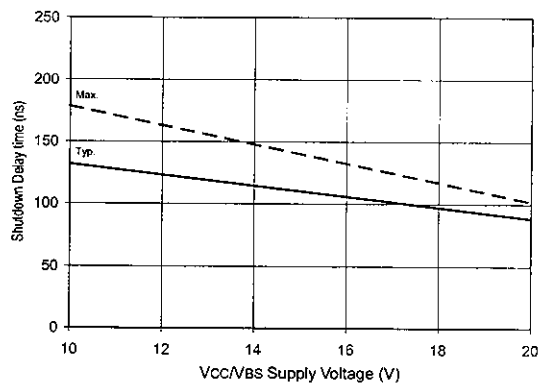


Figure 9B. Shutdown Time vs. V_{CC}/V_{BS} Supply Voltage

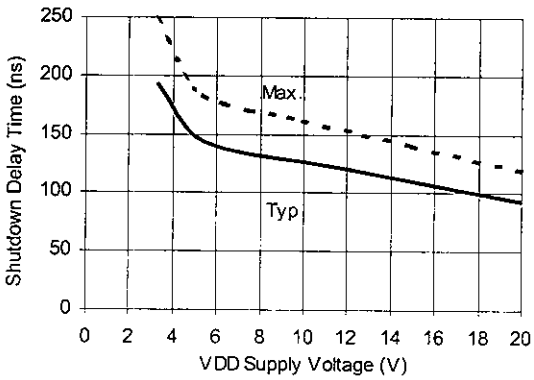


Figure 9C. Shutdown Time vs. V_{DD} Supply Voltage

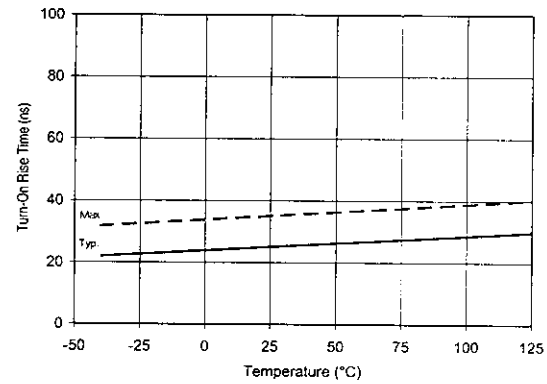


Figure 10A. Turn-On Rise Time vs. Temperature

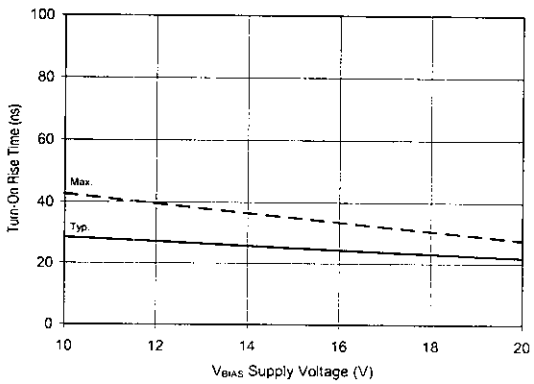


Figure 10B. Turn-On Rise Time vs. Voltage

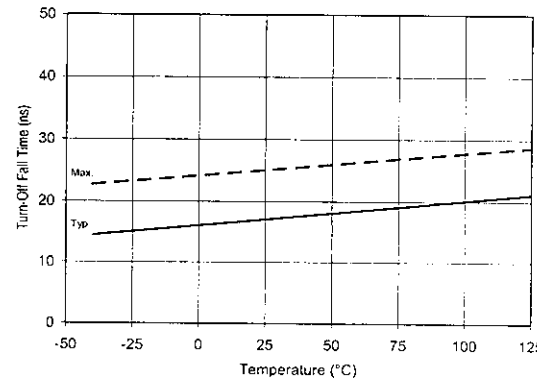


Figure 11A. Turn-Off Fall Time vs. Temperature

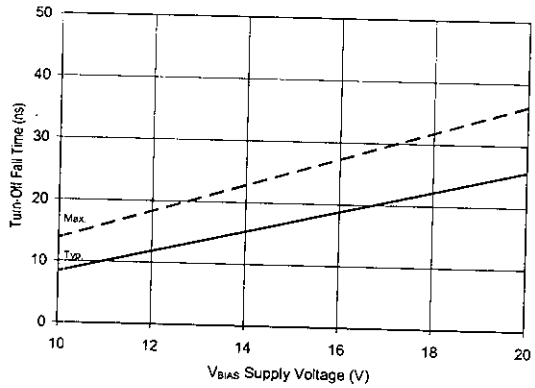


Figure 11B. Turn-Off Fall Time vs. Voltage

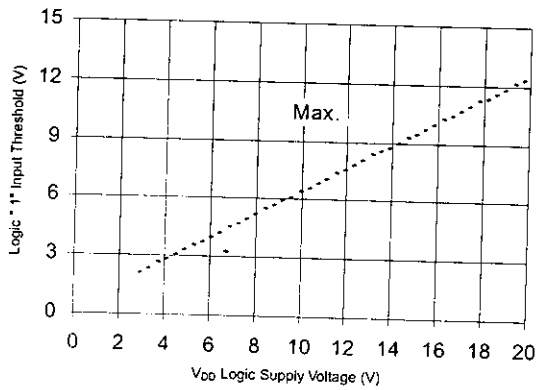


Figure 12B. Logic "1" Input Threshold vs. Voltage

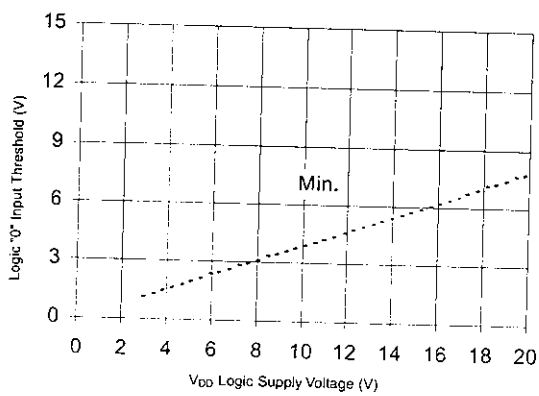


Figure 13B. Logic "0" Input Threshold vs. Voltage

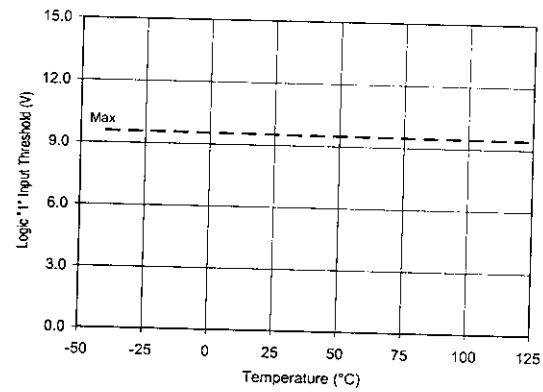


Figure 12A. Logic "1" Input Threshold vs. Temperature

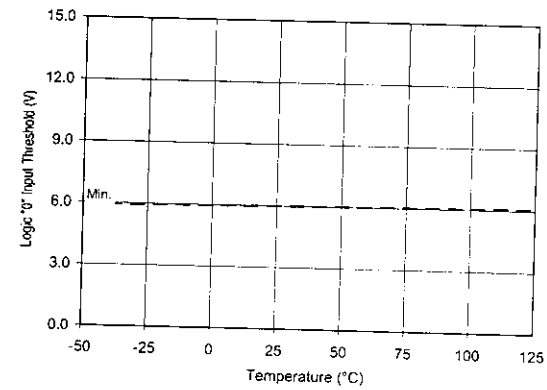


Figure 13A. Logic "0" Input Threshold vs. Temperature

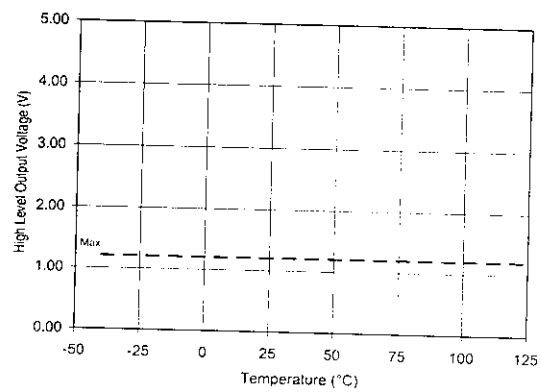


Figure 14A. High Level Output vs. Temperature

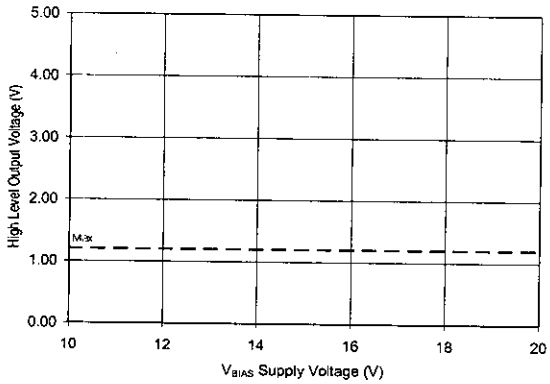


Figure 14B. High Level Output vs. Voltage

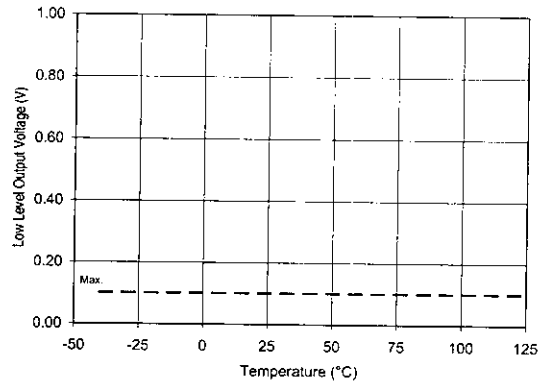


Figure 15A. Low Level Output vs. Temperature

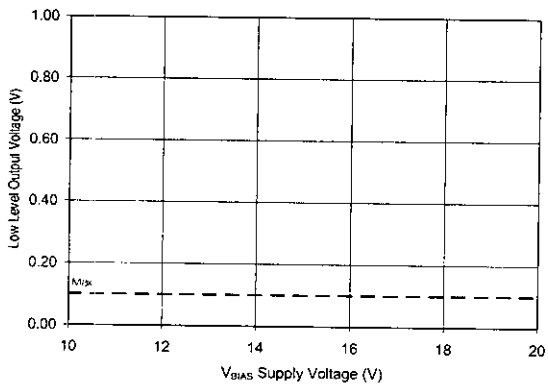


Figure 15B. Low Level Output vs. Voltage

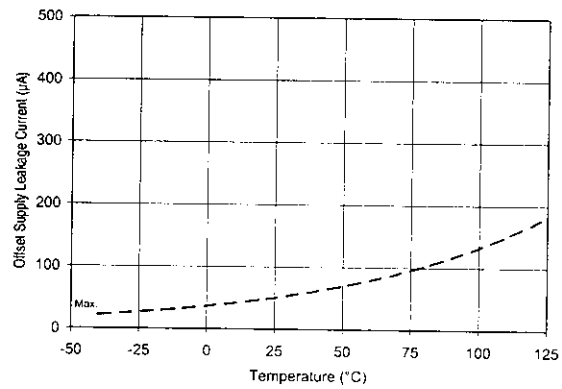


Figure 16A. Offset Supply Current vs. Temperature

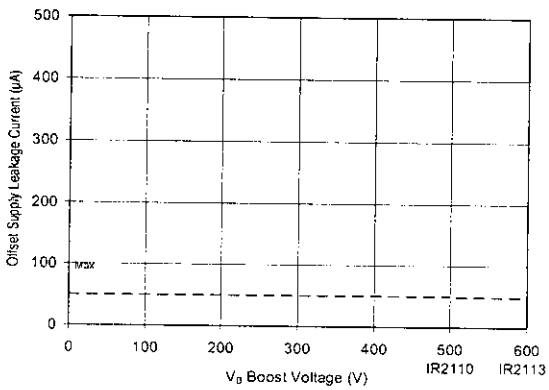


Figure 16B. Offset Supply Current vs. Voltage

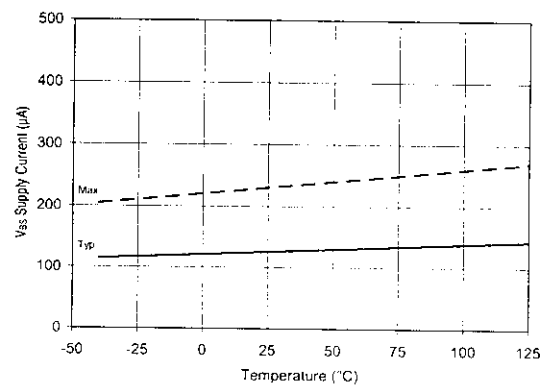


Figure 17A. V_{BS} Supply Current vs. Temperature

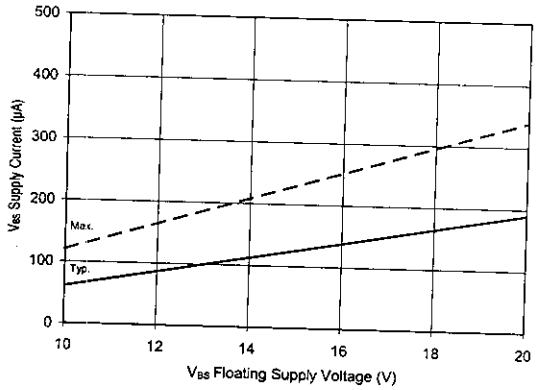


Figure 17B. V_{BS} Supply Current vs. Voltage

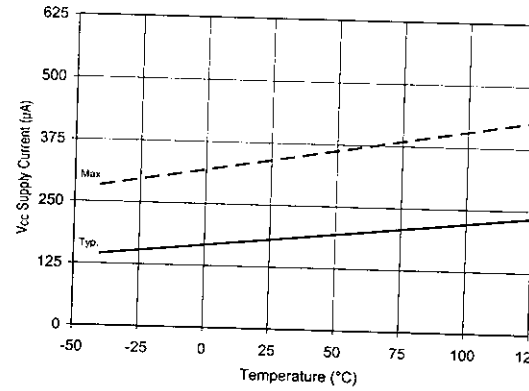


Figure 18A. V_{CC} Supply Current vs. Temperature

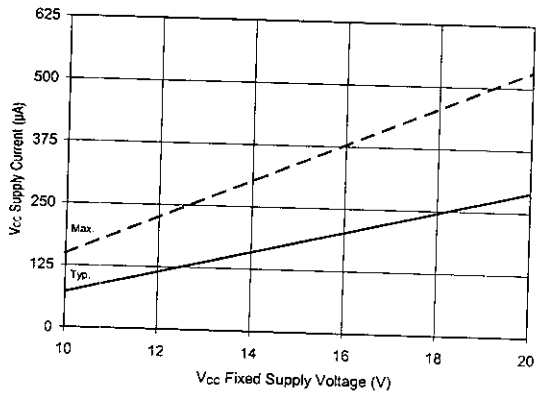


Figure 18B. V_{CC} Supply Current vs. Voltage

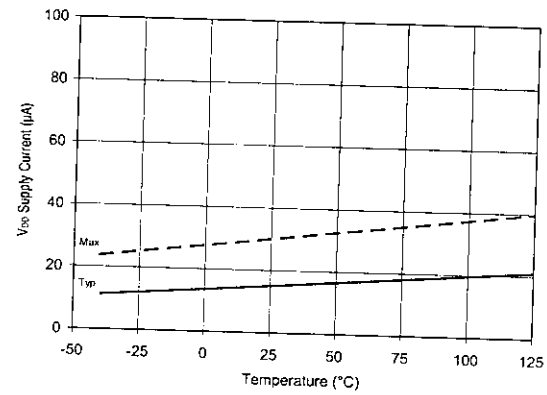


Figure 19A. V_{DD} Supply Current vs. Temperature

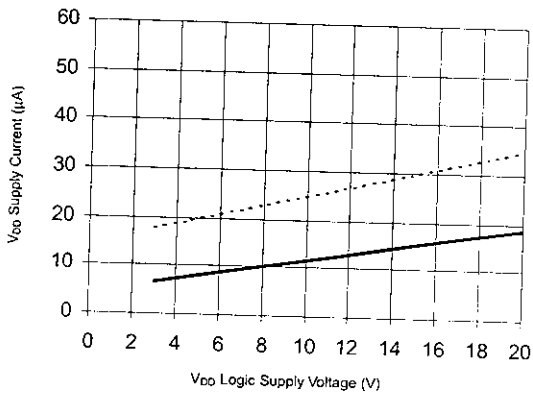


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

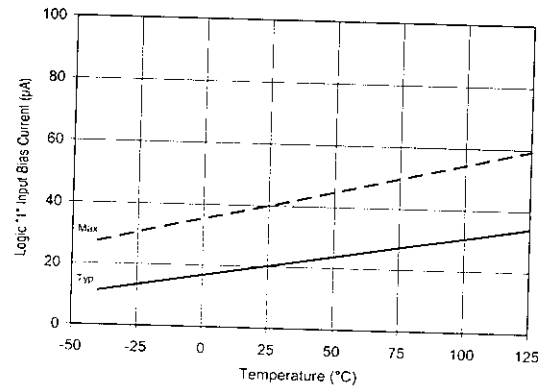


Figure 20A. Logic "1" Input Current vs. Temperature

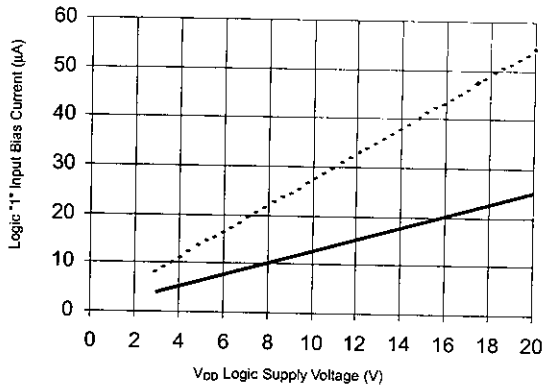


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

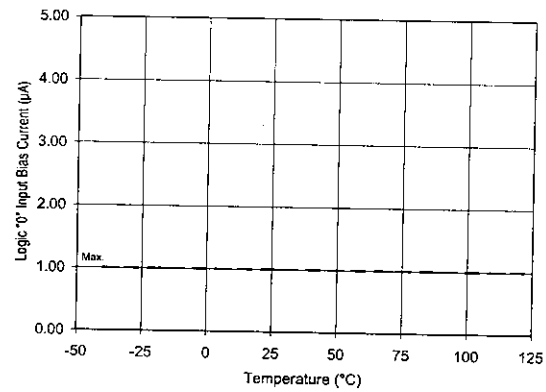


Figure 21A. Logic "0" Input Current vs. Temperature

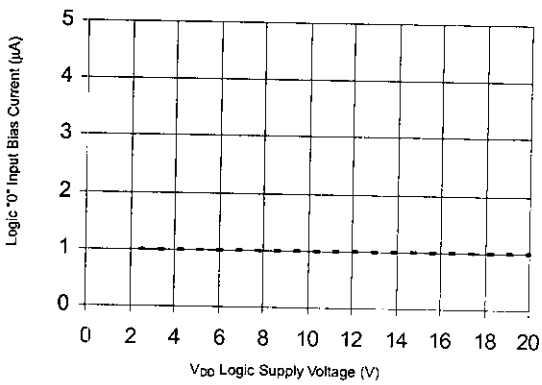


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

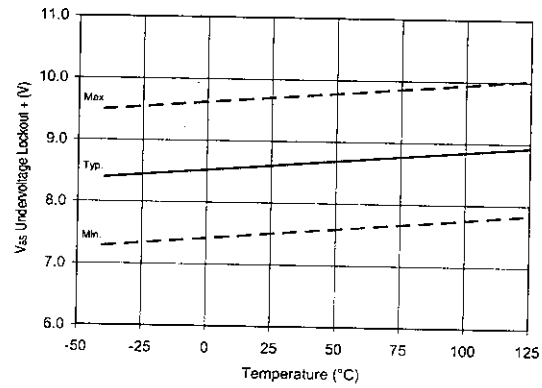


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

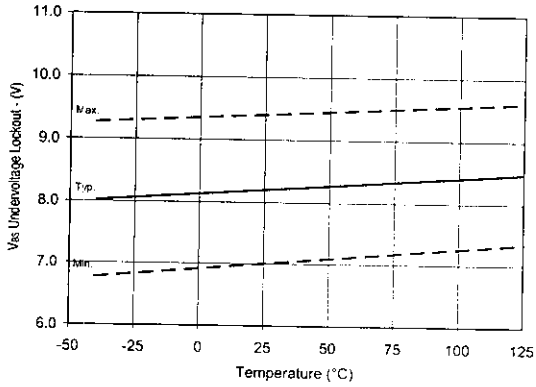


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

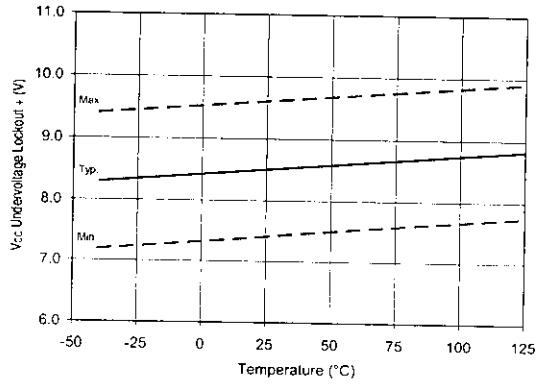


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

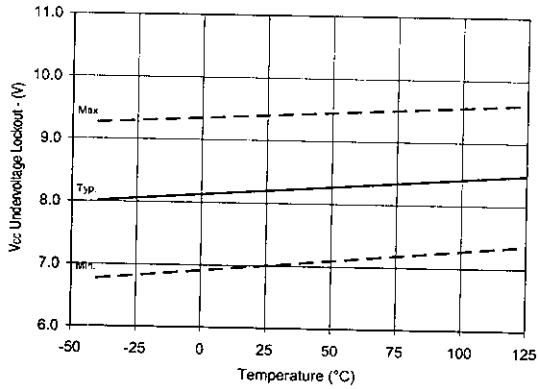


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

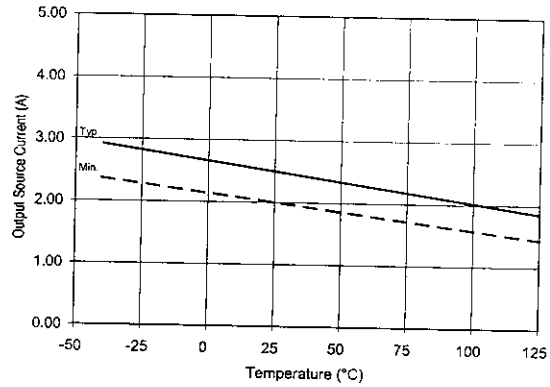


Figure 26A. Output Source Current vs. Temperature

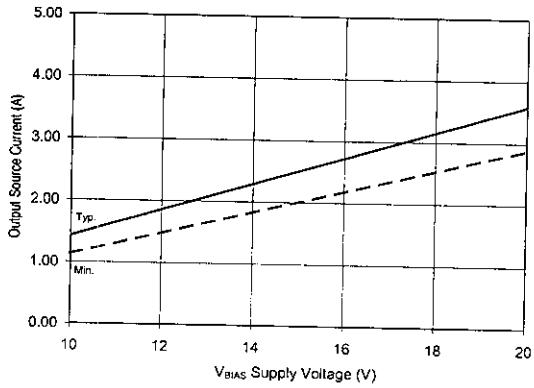


Figure 26B. Output Source Current vs. Voltage

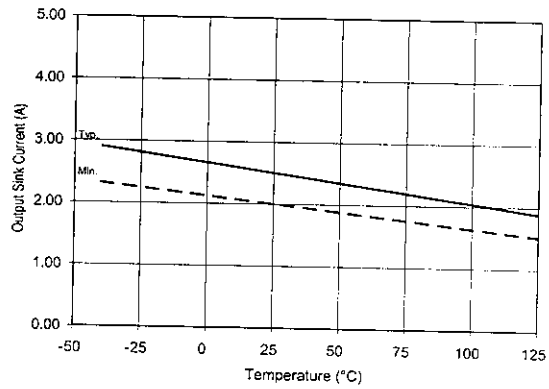


Figure 27A. Output Sink Current vs. Temperature

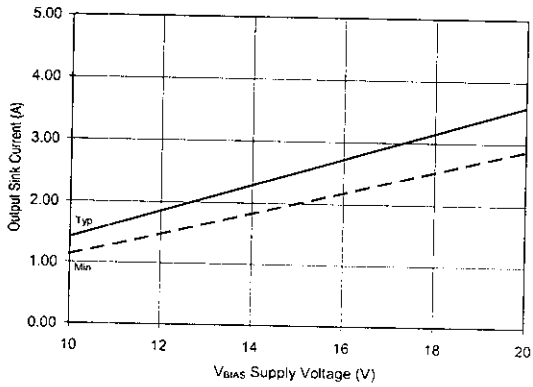


Figure 27B. Output Sink Current vs. Voltage

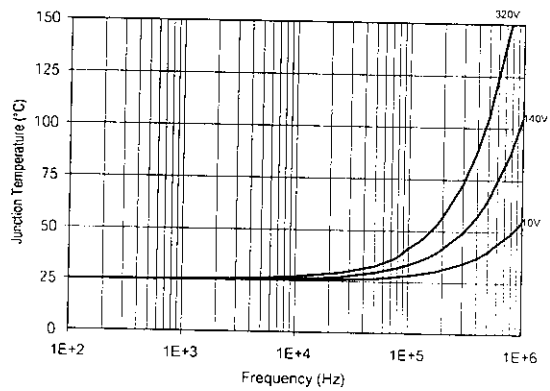


Figure 28. IR2110/IR2113 T_J vs. Frequency
(IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

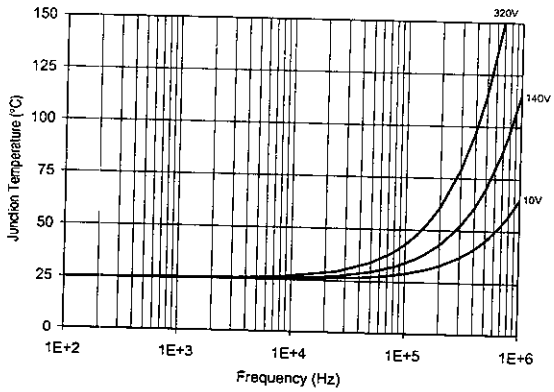


Figure 29. IR2110/IT2113 T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

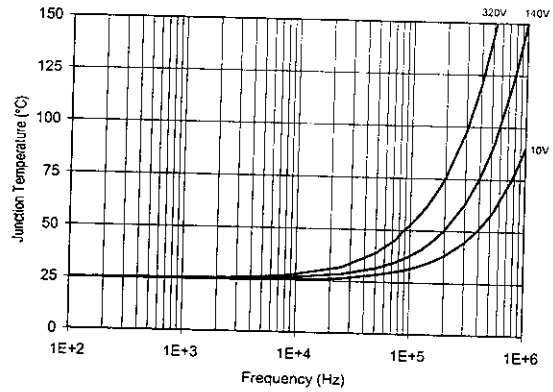


Figure 30. IR2110/IR2113 T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

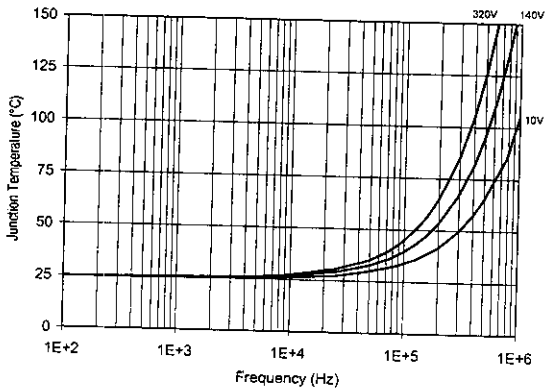


Figure 31. IR2110/IR2113 T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

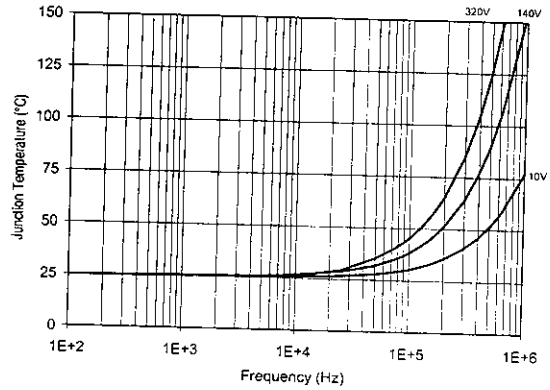


Figure 32. IR2110S/IR2113S T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

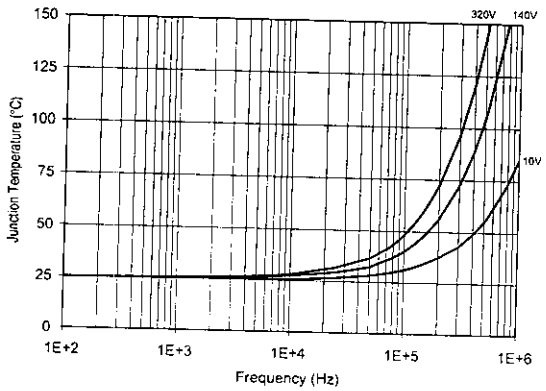


Figure 33. IR2110S/IR2113S T_J vs. Frequency (IRFBC30) R_{GATE} = 22Ω, V_{CC} = 15V

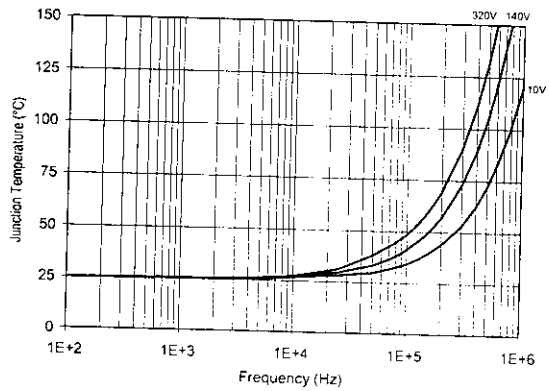


Figure 34. IR2110S/IR2113S T_J vs. Frequency (IRFBC40) R_{GATE} = 15Ω, V_{CC} = 15V

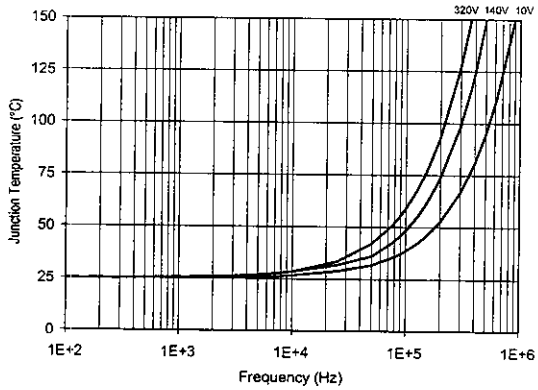


Figure 35. IR2110S/IR2113S T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

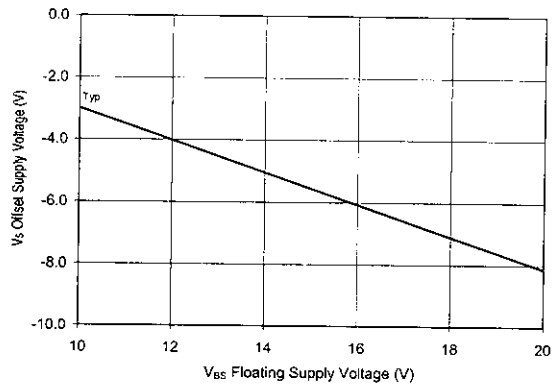


Figure 36. Maximum V_S Negative Offset vs.
V_{BS} Supply Voltage

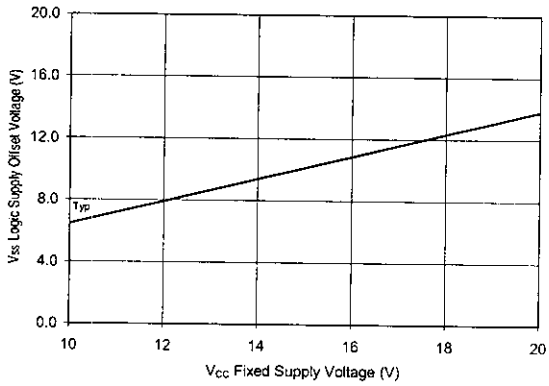
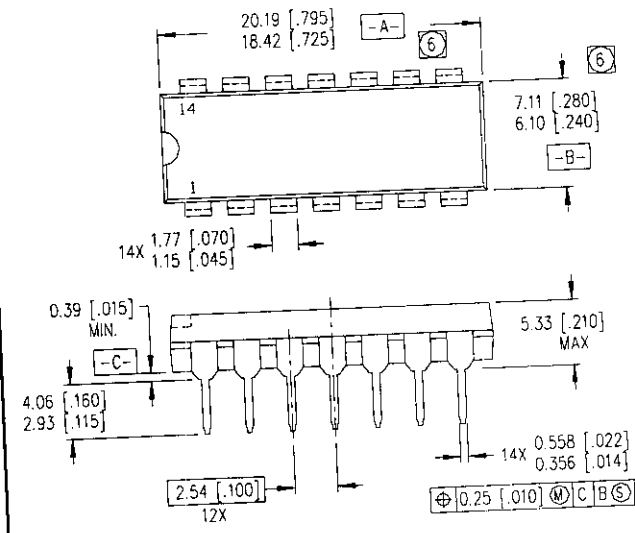
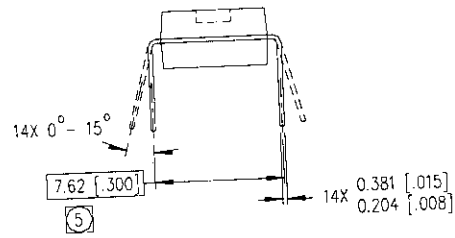


Figure 37. Maximum V_{SS} Positive Offset vs.
V_{CC} Supply Voltage

Case Outlines

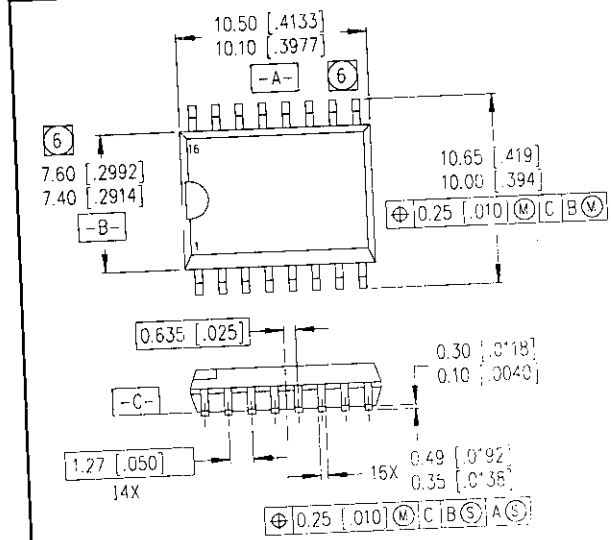


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

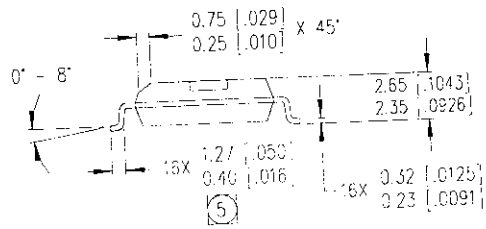


01-6010
01-3002 03 (MS-001AC)

14-Lead PDIP



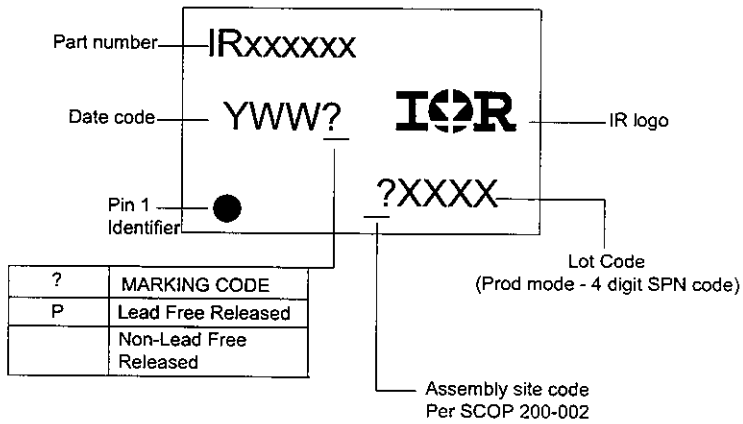
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



01 6015
01-3014 03 (MS-013AA)

16-Lead SOIC (wide body)

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)
14-Lead IR2110 order IR2110
14-Lead IR2113 order IR2113
16-Lead IR2110S order IR2110S
16-Lead IR2113S order IR2113S

Leadfree Part
14-Lead IR2110 order IR2110PbF
14-Lead IR2113 order IR2113PbF
16-Lead IR2110S order IR2110SPbF
16-Lead IR2113S order IR2113SPbF

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105