DESIGN AND IMPLEMENTATION OF MULTISTANDARD DIGITAL FILTER USING FPGA

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BONAFIDE CERTIFICATE

Certified that this project report entitled "**DESIGN AND IMPLEMENTATION OF MULTISTANDARD DIGITAL FILTER USING FPGA**" is the bonafide work of **Ms.A.Bhanu [Reg. No. 0920106004]** who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ABSTRACT

Recent efforts in the design of wireless RF transceivers focus on high integration and multi-standard operation. At the back of a wide-dynamic range sigma-delta modulator, a decimation filter can select a desired channel in the presence of both strong adjacent channel interferers and quantization noise from the digitization process. The decimation filters are important block in devices, which want to establish communication using different standards.

There are multiple ways to implement a decimator filter. This project addresses usage of Cascaded Integrated Comb Filter (CIC) and Half Band Filter (HB) as the decimation filter to reduce the implementation step to realize this design in hardware. Low power approach for CIC filter and HB filter will be discussed. Unlike the existing decimation filters, the filter architecture is designed using Canonical Signed Digit representation (CSD) and Minimum Signed Digit representation (MSD) in this project work. It is suitable for common sub expression elimination, and it significantly reduces the number of adders required for the filter synthesis.The proposed architecture fulfils the requirements of two standards: Wi-MAX and GSM.

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LIST OF ABBREVIATIONS

AAF	----	Analog Antialias Filter
ADC	----	Analog to Digital Converter
ASIC	----	Application Specific Integrated Circuits
BER	----	Bit Error Rate
CIC	----	Cascaded Integrator Comb
CSD	----	Canonic Signed Digits
CNR	----	Carrier to Noise Ratio
DDC	----	Digital Down Converter
DDR	----	Digital Drop Receiver
FPGA	----	Field-Programmable Gate Arrays
GSM	----	Global System for Mobile Communications
IF	----	Intermediate Frequency
LO	----	Local Oscillator
MATLAB	----	MATrix LABoratory
MSD	----	Minimum Signed Digits
NCO	----	Numerically Controlled Oscillator
OSR	----	Over Sampling Ratio
RF	----	Radio Frequency
SNR	----	Signal to Noise Ratio
SOC	----	System-On-Chip
WiMAX	----	Worldwide Interoperability for Microwave Access

CHAPTER 1
INTRODUCTION

1.1 MOTIVATION

Current research on radio frequency (RF) communication transceivers emphasizes both higher integration, to meet consumer demand for low-cost, low-power, small-form factor personal communication devices, and the ability to adapt to multiple communication standards. This trend stimulates the development of a single chip receiver capable of adapting to the various communication standards. Nowadays, the evolving wireless standards include GSM/GPRS/EDGE, WCDMA, CDMA2000, IEEE 802.15.4 (ZigBee), Bluetooth 1.2/ Bluetooth EDRIEEE 802.15.1, 1a, IEEE 802.15.3a Proposals, 802.11a/b/g/h/j/n, IEEE 802.16-2004 and 802.16e (WiMAX). Along with the development of fabrication, it is possible to integrate various separate systems in one chip; however, from the power consumption and cost point of view, increasing research activities concentrate on the hardware sharing in the receiver architectures.

Wireless telecommunication standards currently used throughout the world have channel bandwidths ranging from 6.25 kHz to 1.728 MHz. A multi-standard receiver that performs base band channel select filtering in the digital domain must have an Analog-to-Digital Converter (ADC) with a wide dynamic range that can accommodate undesired channels as well as the desired. Nowadays, a lot of analog to digital conversion techniques are being used. Sigma-Delta conversion is a worldwide technique that provides better channel selection. Besides, it is well adapted to the technology used in VLSI circuits' realizations. Nevertheless, Sigma-Delta modulation needs a post-conversion processing. Indeed, within the framework of Sigma-Delta A/D conversion, the decimation chain has to reduce any signal that may fold up to the effectivechannel by avoiding the quantization noise and the out-of-band signals. Then, it has to bring down the sampling frequency to the Nyquist rate.Following the sigma-delta modulator, a low pass digital decimation filter can select a desired channel in the presence of both strong adjacent channel interferers and quantization noise from the digitalization process.

1.2 PROJECT GOALS

The focus of this project is to design a power and area optimized decimation filter that can perform digital channel selection for the Wimax and GSM communication standards.

- To design a decimation filter that meets the Wimax and GSM specifications without significantly degrading the receiver noise figure.
- To design a decimation filter using canonic signed digit representation and minimum signed digit representation which reduces number of adders.
- To develop a power saving technique for a fixed multi-standard implementation, where filter blocks can be powered down, using multimode design which is able to handle mutually different exclusive filters with efficient resource sharing.

1.3 SOFTWARES USED

- MATLAB 7.3
- ModelSim XE III 6.2g
- Xilinx ISE 9.2i

1.4 ORGANISATION OF THE REPORT

- Chapter 2 discusses about the concepts of digital receiver
- Chapter 3 gives concept of analog to digital conversion
- Chapter 4 deals with concept of decimation process
- Chapter 5 explains the implementation of decimation filter
- Chapter 6 discusses different number representations used for filter design
- Chapter 7 discusses simulation results
- Chapter 8 shows conclusion and future scope of the project

CHAPTER 2
DIGITAL RECIEVER

Digital receivers have revolutionized electronic systems for a variety of applications including communications, data acquisition, and signal processing. This series shows how digital receivers, the fundamental building block for software radio, can replace conventional analog receiver designs, offering significant benefits in performance, density and cost.

The digital receiver block diagram is shown in Figure 2.1. Right after RF amplifier and an optional RF translator stage, an A/D (Analog-to-Digital) converter is used to digitize the RF input into digital samples for the subsequent mixing, filtering and demodulation that are performed using digital signal processing elements. The fundamental theorem to sample data which lays the foundation for the A/D converter requirements is Nyquist's Theorem: "Any signal can be represented by discrete samples, if the sampling rate is at least twice the bandwidth of the signal."For example, if an A/D converter is used with the sampling rate of 70 MHz, then the bandwidth of the analog input must be less than 35 MHz.

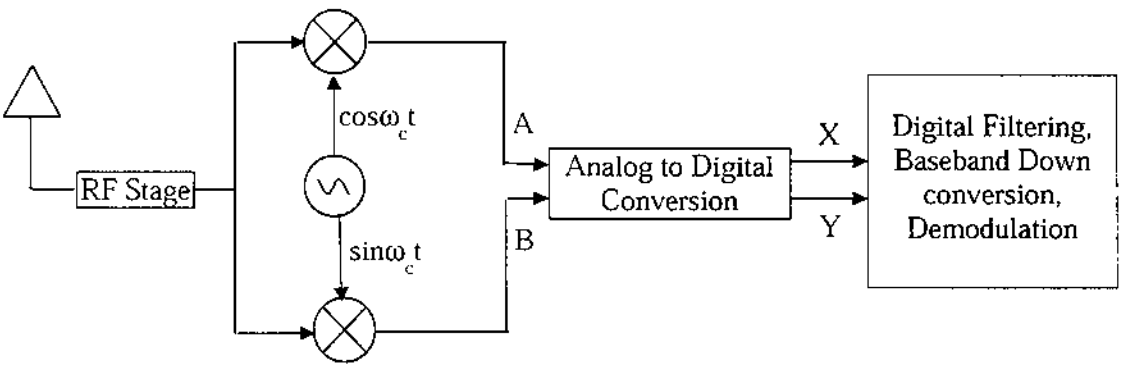

Figure 2.1 Digital Receiver Block Diagram

2.1 ALIASING

There occurs aliasing effect, if the Nyquist's criterion is ignored. Figure 2.2 shows a frequency display of a system being sampled at frequency f_s. For all input signals below $f_s/2$, such as the one at f_o, fully meets the Nyquist criterion. In fact, any number of signals can be present in the shaded region and all will be correctly represented in the sampled data.

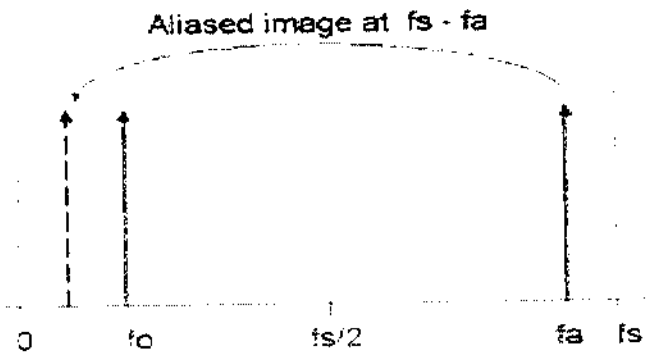

Figure 2.2 Frequency Display of a System being sampled at Frequency f_s

Consider a signal present at, f_a, which is above $f_s/2$, the sampling process will generate an aliased image which will appear in the sampled data at f_s-f_a. This image cannot be distinguished from a true signal which might have been present at that same frequency. The point is this: once an aliased image is created in the sampling process, no amount of further processing can distinguish between a true signal and an aliased signal. Therefore, it is imperative to prevent aliasing before it occurs.

The most straightforward way to prevent aliasing is to use a low pass filter before the A/D converter, which removes all signals above fs/2. This filter is called an Anti-Aliasing Filter. The Anti-Aliasing Filter response is shown in Figure 2.3. Now the signal at f_a is blocked, so the

A/D converter never sees it. Anti-aliasing filters are often included on the same board as the A/D converter as a convenience to the user.

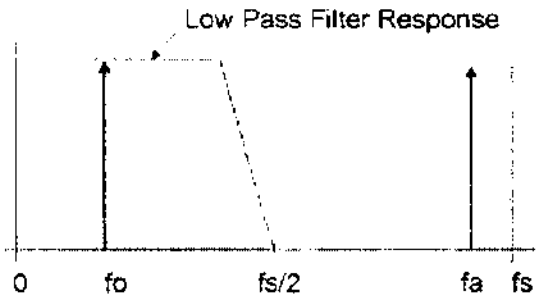

Figure 2.3 Anti-Aliasing Filter Frequency Response

As a side note, Nyquist's criterion can also be met by limiting the bandwidth of the sampled signal using other types of filters. For example, suppose it is interested to receive signals between $f_s/2$ and f_s in the above diagram. This can be achieved by using bandpass filter with a passband from $f_s/2$ to f_s, which satisfies the Nyquist criterion, because the bandwidth is equal to one half the sampling rates.

Once the sampling is done, the band of signals from $f_s/2$ to f_s is "Folded" into the frequency band from DC to $f_s/2$. This half-sampling frequency is often called the "Folding Frequency." This technique is sometimes called "Undersampling" and while this works well in theory, care must be taken in actual practice to ensure that the A/D converter supports the higher input frequencies it must handle.

2.2 DIGITAL RECIEVER CHIP

The digital samples coming out of the A/D converter are being fed to the next stage, which is the digital receiver chip. The digital receiver chip is typically contained on a single monolithic chip which forms the heart of the digital receiver system. It is also sometimes referred to as a Digital Down Converter (DDC) or a Digital Drop Receiver (DDR). Inside the digital receiver chip there are three major sections:

- Local Oscillator
- Mixer
- Decimating Low Pass Filter

2.3 LOCAL OSCILLATOR

It's a direct Digital Frequency Synthesizer (DFS) sometimes called a Numerically Controlled Oscillator (NCO). This device is implemented entirely with digital circuitry. The oscillator generates digital samples of two sine waves precisely offset by 90 degrees in phase, creating sine and cosine signals. It uses a digital phase accumulator and sine/cosine lookup tables. Note that the A/D clock is fed into the local oscillator. The digital samples out of the local oscillator are generated at a sampling frequency exactly equal to the A/D sample clock frequency, fs.

It is important to understand that the output sampling rate is always fixed at fs, regardless of the frequency setting. The sine/cosine output frequency is changed by programming the amount of phase advance per sample. A small phase advance per sample corresponds to a low frequency and a large advance to a high frequency. The phase advance per sample is directly proportional to the output frequency and is programmable from DC to fs/2 with up to 32-bit of resolution.

Using a 70-MHz sampling clock, the frequency range is from DC to 35 MHz and the resolution is well below 1Hz. The Local Oscillator has very impressive frequency switching characteristics as shown in Figure 2.4. When switching between two frequencies, the digital accumulator precisely maintains the phase of the sine and cosine outputs for phase-continuous switching.

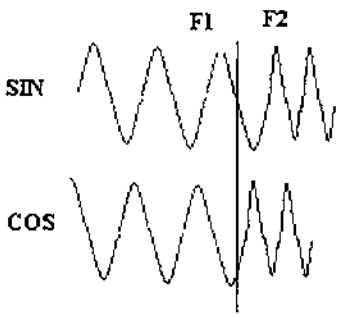

Figure 2.4 Frequency Switching Characteristics of Local Oscillator

When the frequency is changed, what actually changes is the amount of phase advance per sample. This allows the local oscillator to perform Frequency Shift Keying (FSK) and very finely resolved sweeps. Transients and settling normally associated with other types of local oscillators, such as phase-locked loop synthesizers, are eliminated.

The time it takes to retune the local oscillator is simply the time it takes to load a new digital frequency word (32-bit binary number) into a register, usually well below one microsecond. Some digital receiver chips employ a local oscillator with a built-in "Chirp" function. This is a fast, programmable and precise frequency sweep, which is very useful in radar systems.

2.4 DIGITAL MIXER

The next major component of the digital receiver chip is the mixer. The mixer actually consists of two digital multipliers. Digital input samples from the Analog/Digital (A/D) converter are mathematically multiplied by the digital sine and cosine samples from the Local Oscillator (LO).

Note that the input A/D data samples and the sine and cosine samples from the LO are being generated at the same rate, namely, once every A/D sample clock. Since the data rates into both inputs of the mixers are the A/D sampling rate f_s, the multipliers also operate at that same rate and produce multiplied output product samples at *fs*.

The sine and cosine inputs from the LO create in-phase (I) and quadrature (Q) outputs that are important for maintaining phase information contained in the input signal. From a signal standpoint, the mixing produces a single-sideband complex translation of the real input. Unlike analog mixers, which also generate many unwanted mixer products, the digital mixer is nearly ideal and produces only two outputs: the sum and difference frequency signals.

There is the "difference" mixer product in the frequency domain as shown in Figure 2.5. At the output of the mixer, the high frequency wideband signals in the A/D input have been translated down to DC with a shift or offset equal to the LO frequency.

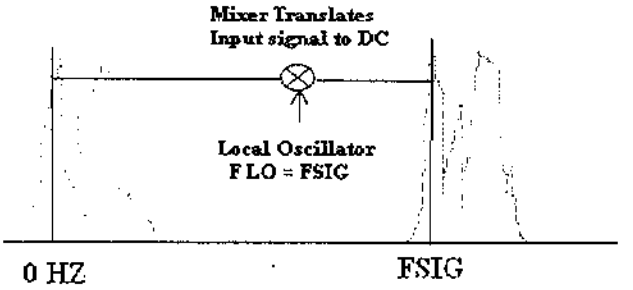

Figure 2.5 Digital Receiver Mixer Translation

This is similar to the analog receiver mixer except that the analog receiver mixes the RF input down to an intermediate frequency (IF). In the digital receiver, the precision afforded by the digital signal processing allows us to mix right down to baseband (or 0 Hz). Overlapping mixer images, difficult to reduce with analog mixers, are strongly rejected by the accuracy of the sine and cosine LO samples and the mathematical precision of the multipliers in the digital mixer.

By tuning the local oscillator over its frequency range, any portion of the RF input signal can be translated down to DC. In effect, the wideband RF signal spectrum can be shifted around 0 Hz, left and right, simply by changing the LO frequency. The objective is to tune the LO to center the signal of interest around 0 Hz, so that the low-pass filter that follows can pass only the signal of interest.

2.5 DECIMATING LOW PASS FILTER

Once the RF signal has been translated, it is now ready for filtering. The decimating low-pass filter accepts input samples from the mixer output at the full A/D sampling frequency *fs*. It utilizes digital signal processing to implement a Finite Impulse Response (FIR) filter transfer function. The filter passes all signals from 0 Hz up to a programmable cutoff frequency or bandwidth, and rejects all signals above that cutoff frequency. This digital filter is a complex filter which processes both I and Q signals from the mixer. At the output, it is possible to select either I and Q (complex) values or just real values, depending on the system requirements.

Figure 2.6 shows a representation of the action of the decimation filter in the frequency domain. The filter passes only signals from 0 Hz up to the filter bandwidth. All higher frequencies have been removed. Remember, the wideband input signal was translated down to DC by the mixer and positioned around 0 Hz by the tuning frequency of the LO.

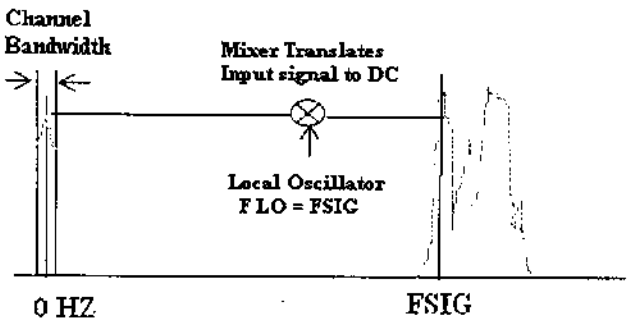

Figure 2.6 Decimating Filter Band limiting

Now, at the filter output a narrow slice of the RF input signal is effectively selected and translated it to DC. Note that, all other signals above and below the band of interest have blocked. The band limiting action of the filter is analogous to the action of the IF stage in the analog receiver, except that the decimating low-pass filter operates around DC instead of being centered at an IF.

In order to set the bandwidth of the filter, it is needed to program a parameter called the decimation factor. Since the output bandwidth and the output sampling rate are directly related in the DDC, the decimation factor also sets the output sampling rate. The decimation factor, N, determines the ratio between input and output sampling rates and also the ratio between input and output bandwidths.

Digital receivers can be divided into two classes, narrowband and wideband, distinguished by the programmable range of decimation factors. Narrowband receivers typically have a range of decimation factors from 32 or 64 to 65,536 or 131,072, depending on the chip manufacturer. Wideband receivers typically have a range of decimation factors from 2 to 64.

CHAPTER 3
ANALOG-TO-DIGITAL CONVERTER

An Analog-to-Digital Converter (abbreviated ADC, A/D or A to D) is a device which converts a continuous quantity to a discrete timedigital representation. An ADC may also provide an isolated measurement. Typically, an ADC is an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. The digital output may use different coding schemes. Typically the digital output will be a two's complement binary number that is proportional to the input, but there are other possibilities.

3.1 RESOLUTION

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is usually a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is called the *LSB* (least significant bit, since this is the voltage represented by a change in the LSB). The resolution Q of the ADC is equal to the *LSB* voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete voltage intervals as indicated in equation 3.1.

$$Q = E_{FSR}/N \tag{3.1}$$

Where N is the number of voltage intervals and E_{FSR} is the full scale voltage range. E_{FSR} is given by equation 3.2.

$$E_{FSR} = V_{RefHi} - V_{RefLow} \tag{3.2}$$

Where V_{RefHi} and V_{RefLow} are the upper and lower extremes, respectively, of the voltages that can be coded.Normally, the number of voltage intervals is given by equation 3.3.

$$N = 2^M, \tag{3.3}$$

where M is the ADC's resolution in bits.

3.2 SAMPLING RATE

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the sampling rate or sampling frequency of the converter.

A continuously varying bandlimited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be exactly reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the conversion time). An input circuit called a sample and hold performs this task—in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

3.3 OVERSAMPLING ADC

Usually, signals are sampled at the minimum rate required, for economy, with the result that the quantization noise introduced is white noise spread over the whole pass band of the converter. If a signal is sampled at a rate much higher than the Nyquist frequency and then digitally filtered to limit it to the signal bandwidth there are the following advantages:

- Digital Filters can have better properties (sharper rolloff, phase) than analogue filters, so a sharper anti-aliasing filter can be realised and then the signal can be downsampled giving a better result
- A 20-bit ADC can be made to act as a 24-bit ADC with 256× oversampling.
- The Signal-to-Noise Ratio (SNR) due to quantization noise will be higher than if the whole available band had been used. With this technique, it is possible to obtain an effective resolution larger than that provided by the converter alone
- The improvement in SNR is 3 dB (equivalent to 0.5 bits) per octave of oversampling which is not sufficient for many applications. Therefore, oversampling is usually coupled with noise shaping (Refer Sigma-Delta Modulators). With noise shaping, the improvement is 6L+3 dB per octave, where L is the order of loop filter used for noise shaping. e.g. a 2nd order loop filter will provide an improvement of 15 dB/octave.

3.4 ACCURACY

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity are intrinsic to any Analog-to-Digital Conversion. There is also a so-called aperture error, which is due to a clock jitter and is revealed, when digitizing a time-variant signal (not a constant value).

These errors are measured in a unit called the LSB, which is an abbreviation for Least Significant Bit. In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

3.5 ANALOG ANTIALIAS FILTER (AAF)

The ADC converts the signal from continuous to discrete domain. Since sampling introduces aliasing, an antialias filter needs to attenuate all out of band signals prior to the ADC. A Nyquist rate ADC is one that works at a sample rate close to the Nyquist sampling frequency of the signal i.e. the ADC sample rate will be slightly higher than twice the bandwidth of the signal. For such an ADC the AAF needs to attenuate all signals present outside the band $-f_N/2$ and $f_N/2$. Hence the AAF needs to have a sharp transition band as shown in the figure 3.1. An

oversampled ADC, on the other hand, works at a sample rate which is several times higher than the Nyquist sampling frequency. For such an ADC, the AAF can have a relaxed transition band stretching from the signal band edge to half the ADC sampling frequency.

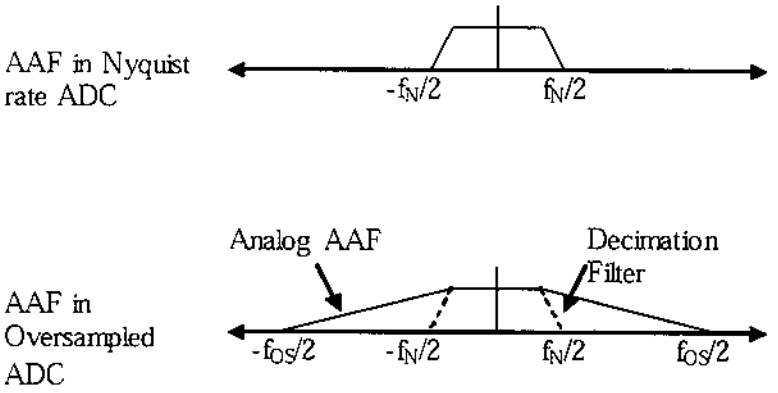

Figure 3.1 Effects on Analog Antialias Filter (AAF)

A digital filter placed after the ADC, filters the out of band signals and reduces the sampling frequency to the Nyquist rate or any other desired rate. These filters are called decimation filters. Thus, the use of an oversampled ADC enables the use of a much less stringent AAF at the cost of the decimation digital filters. Shifting design complexity from the analog to the digital domain is always a desirable feature as it enables more and more of integration in a single chip.

3.6 QUANTIZATION NOISE

The quantization noise that results as an effect of the Analog to Digital Conversion process is another important specification for the receiver system. Assuming that the quantization noise is white and uniformly distributed across the quantization intervalΔ, the total noise in an ADC is a function of the quantization interval Δ ($\Delta^2/12$). This noise is uniformly distributed from $-f_N/2$ to $f_N/2$, where f_N is the Nyquist frequency. In an oversampled ADC, which works at a frequency f_{os}, the total noise gets uniformly distributed over the frequency range, $-f_{os}/2$ to $f_{os}/2$ and hence the noise PSD at individual frequencies is smaller compared to the first

case. Thus, in an oversampled converter, the high sample rate yields low quantization noise at the cost of increased circuit complexity. There is a special class of ADCs called the Sigma Delta ADC. These ADCs have a special property: their quantization noise is not uniform over the frequency range.

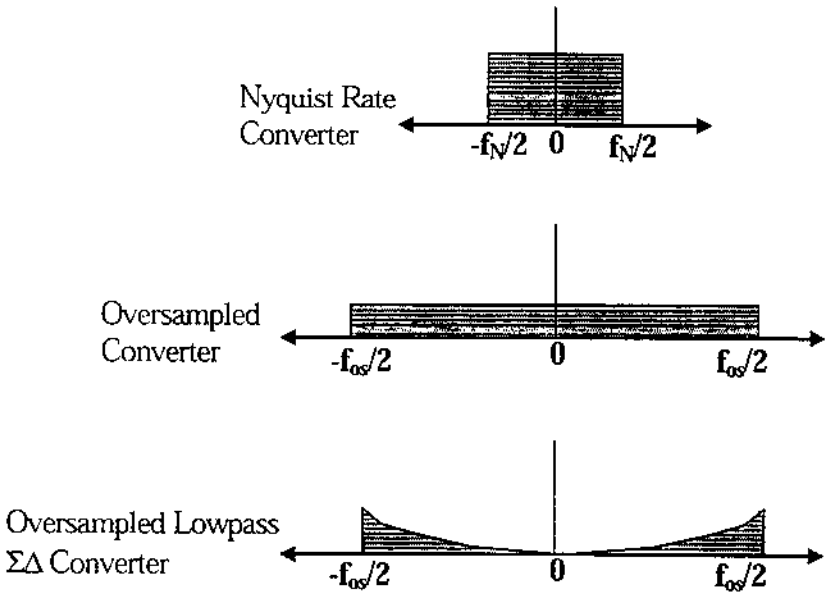

Figure 3.2 ADC Quantization Noise

The figure 3.2 shows the quantization noise for a low pass ΣΔ ADC. Here, the noise is low in the low frequency band, but increases in higher frequencies. Thus the Signal to Noise Ratio is very high for a system that uses signals in the low frequency range. This allows the use of a low resolution quantizer; significantly lower than that which would be required for an ADC with flat quantization noise for the same Signal to Noise Ratio requirement. Hence, in spite of it being an oversampled system, the use of a low resolution quantizer reduces the circuit complexity. Usually a single bit or dual bit quantizer is sufficient for providing high resolution ADCs employing ΣΔ modulation. It is this fact that allows the use of the ΣΔ modulator in high speed applications.

CHAPTER 4

DECIMATION PROCESS

"Decimation" is the process of reducing the sampling rate. In practice, this usually implies lowpass-filtering a signal, then removing some of its samples."Downsampling" is a more specific term, which refers to just the process of removing of samples, without the lowpass filtering operation. "Decimation" is loosely, sometimes known as "downsampling".

4.1 DECIMATION FACTOR

The decimation factor is simply the ratio of the input rate to the output rate. It is usually symbolized by "M", so

Input rate / Output rate = M.

4.2 NEED FOR DECIMATION

The most immediate reason to decimate is simply to reduce the sampling rate at the output of one system, so a system operating at a lower sampling rate can input the signal. But a much more common motivation for decimation is to reduce the cost of processing: the calculation and/or memory required to implement a DSP system generally is proportional to the sampling rate, so the use of a lower sampling rate usually results in a cheaper implementation.

Almost anything does with the signal can be done with fewer operations at a lower sample rate, and the workload is almost always reduced by more than a factor of M. For example, doubling the sample rate, an equivalent filter will require four times as many operations to implement. This is because both amount of data (per second) and the length of the filter increase by two, so convolution goes up by four. Thus, if sample rate is halved, the work load can be decreased by a factor of four. If the sample rate is reduced by M, the workload for a filter goes down to $(1/M)^2$. A signal can be downsampled whenever it is "oversampled", that is when a sampling rate used is greater than the Nyquist criteria required.

Specifically, the signal's highest frequency must be less than half the post-decimation sampling rate. Decimation involves removing of samples, so decimation can be done only by integer factors; decimation cannot be done by fractional factors.

In most cases, though, low pass-filtering is needed to the signal prior to down sampling, in order to enforce the Nyquist criteria at the post-decimation rate. For example, suppose the signal is sampled at a rate of 30 kHz, whose highest frequency component is 10 kHz (which is less than the Nyquist frequency of 15 kHz). If the sampling rate is to be reduced by a factor of three to 10 kHz, it is necessary to ensure that the signal must not have components greater than 5 kHz, which is the Nyquist frequency for the reduced rate. However, since the original signal has components up to 10 kHz, the signal have to be filtered by low pass filter prior to downsampling to remove all components above 5 kHz, so that no aliasing will occur when downsampling.This combined operation of filtering and downsampling is called Decimation.

4.3 MULTISTAGE STRUCTURE

As the Sigma-Delta Modulators are over sampled, the transition band is small relative to sampling frequency leading to excessively large filter orders. The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes much power. This can be overcome by multistage approach. Implementing decimation filter in several stages reduces the total number of filter coefficients. The filters operating at higher sampling rates have larger transition bands, and the filters with lower transition bands operate at reduced sampling frequencies. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will lead to low power consumption. However, here are a couple of rules of thumb which may help narrow down the choices of multistage structure:

- Using two or three stages is usually optimal or near-optimal.
- Decimate in order from the largest to smallest factor. In other words, use the largest factor at the highest sampling rate. For example, when decimating by a factor of 60 in three stages, decimate by 5, then by 4, then by 3.

4.4 IMPLEMENTATION

Decimation consists of the processes of lowpass filtering, followed by downsampling. To implement the filtering part, either FIR or IIR filters are used. To implement the downsampling part (by a downsampling factor of "M") simply keep every Mth sample, and throw away the M-1 samples in between. For example, to decimate by 4, keep every fourth sample, and throw three out of every four samples away.

In the case of FIR filters, any output is a function only of the past inputs (because there is no feedback). Therefore, it is necessary to calculate outputs which will be used.

For IIR filters, it is required to do part or all of the filter calculation for each input, even when the corresponding output won't be used. (Depending on the filter topology used, certain feed-forward parts of the calculation can be omitted.).The reason is that required outputs are affected by the feedback from the outputs that are not required.

Since we compute only one of every M outputs, M-1 operations per outputs are saved, or an overall "savings" of (M-1)/M. Therefore, the larger the decimation factor is, the larger the savings, percentage-wise.

A decimating FIR is actually the same as a regular FIR, except that M samples are shifted into the delay line for each output calculated. More specifically

- Store M samples in the delay line.
- Calculate the decimated output as the sum-of-products of the delay line values and the filter coefficients.
- Shift the delay line by M places to make room for the inputs of the next decimation.

Also, just as with ordinary FIRs, circular buffers can be used to eliminate the requirement to literally shift the data in the delay line.

CHAPTER 5
DECIMATION FILTER DESIGN

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Also, just as with ordinary FIRs, circular buffers can be used to eliminate the requirement to literally shift the data in the delay line.

5.1 CIC Filter

Cascaded Integrator-Comb (CIC), also called Hogenauer filters, are multi-rate filters that are used for realizing large sample rate conversions in digital systems. The main advantage of this filter is it does not use multipliers, and consists of only adders, subtractors and registers. They are typically employed in applications that have a large excess sample rate. That is the system sample rate is much larger than the bandwidth occupied by the signal. CIC filters find application in

- Digital Up-Converters and Digital Down-Converters.
- Channelization functions in a digital radio or MODEM.
- For ultra-tight integration of GPS/INS/PL sensors.
- Any filter structure that is required to efficiently effect a large sample rate change.

The characteristics of CIC filters are

- Linear phase response.
- Utilize only delay and sum block (no multiplication).
- The integrator and comb structure are independent of rate changes (there is no need to reproject the filter on decimation/interpolation rate change).

The basic structure of the CIC decimation filter is very simple. It consists of an integrator section operating at the high sampling rate and a comb section operating at the lowsampling rate and then is named Cascaded Integrator Comb (CIC).

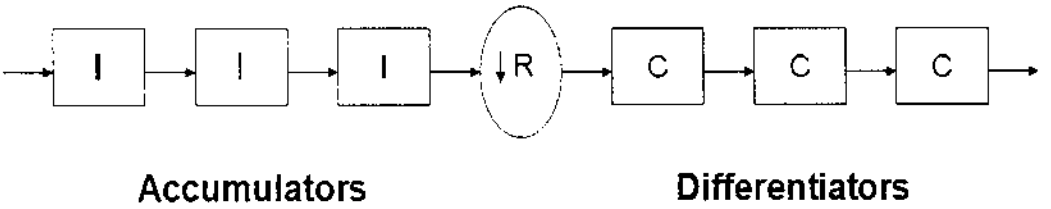

Figure 5.1 CIC Filter Architecture

In figure 5.1, the first integrator section comprises of N integrators which is the length of CIC filter and as the same amount as the comb section. That means, to discuss how many sections the CIC filters have, the number should be either the amount of the integrator section or the comb section, and in other words, totally, the length is 2N sections.

There is a switch downsampling the signal to fs/M after the integrator part. Operating in the low sampling rate, the comb filter consists of N comb blocks each of which has a differential delay of D samples. The transfer function of CIC is shown in equation 5.1.

$$H(z) = \left(\frac{1}{Mc} \cdot \frac{1-z^{-Mc}}{1-z^{-1}}\right)^{k} \tag{5.1}$$

According to thepower response, notches exist at multiples of $f = 1/D$. Thus, we are able to adjust the places of notches by selecting certain value of D. In sum, the frequency response of CICfilter exclusively depends on the three parameters, N, D and M.

CIC filter is a lowpass filter; however its scheme is different from other FIR filters. In general, the noise located at the frequency higher than stopband frequency is going to be eliminated after the FIR filter in order to satisfy the aliasing requirement. In contrast, CIC filter only attenuates the noise that can alias into the band of interest. For instance, the channel space is 200 kHz in GSM and it is assumed to set stopband at 800 kHz in the first decimation stage. Compared to FIR filter, which filter all the noises higher than 800 kHz, CIC filter only takes away the noises which are perhaps going to alias into 200 kHz after the down sampling and resolves other noises with very limited attenuations.

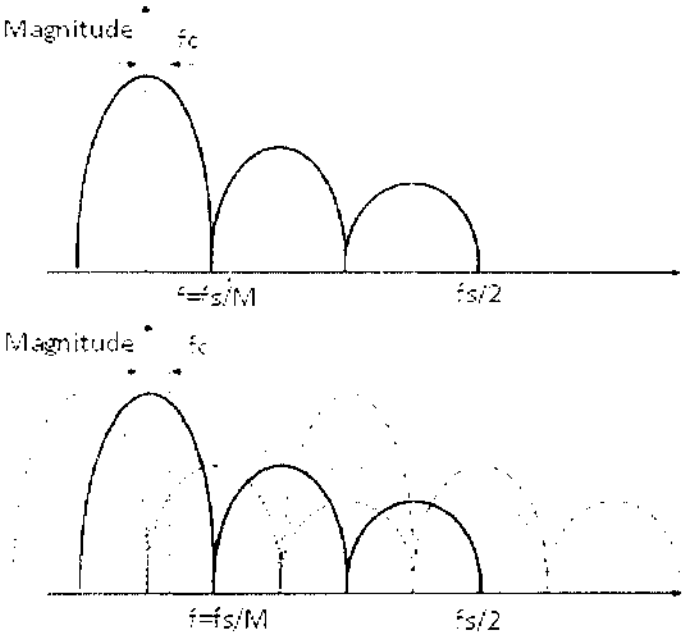

Figure 5.2 CIC Downsampling

CIC filter makes the most of essential function of decimation to down convert the sampling frequency and to keep the passband aliasing or imaging error within prescribed bounds. Figure 5.2 illustrates this mechanism clearly, in which M equals 3. Relative to high sampling frequency, there are notches in the multiples of f_s. Once the sampling rate is reduced to f_s/M, the spectrum repeats according to multiples of f_s. It is true there are still lots of noises left beyond f_s, however, aliasing noises into the f_c are quite limited due to the existence of notches. It is pretty appreciated that down conversion is succeeded without damaging the information in the signal channel. CIC structure is very popular in the first stage design of the multi-stage decimation filter design since it has lot of appreciated characteristics, especially in the high sample frequency field. It is apparent to find it economical because CIC filter has not multipliers and storage for filter coefficient. As the price, it results in undesired passband gain leading to too large passband ripple, which has bad effect on the signal demodulation. Therefore, a compensation filter is needed to resolve this loss.

Figure 5.3 shows the basic accumulator (Integrator) in z transforms and its digital circuit representation.

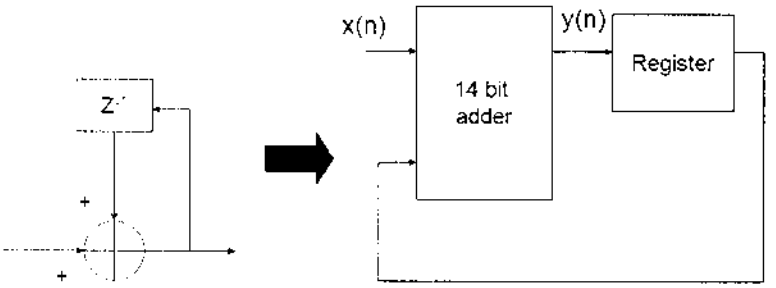

Figure 5.3 Accumulators in Z-transform and Digital Circuit Implementation

Figure5.4 shows the basic differentiator (Comb) in z-transforms and its digital circuit representation. M in the figure, is the differential delay which is 1 in this design.

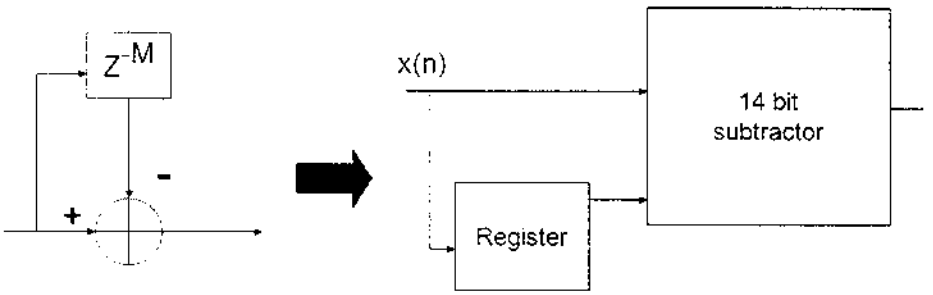

Figure 5.4 Differentiator in Z-transform and Digital Circuit Implementation

5.2 HALF-BAND FILTER

Figure 5.5 shows the tolerance specifications of the ideal lowpass filter, where Dpass and Dstop mean passband ripple and stopband ripple from the ideal response respectively. ω pass and ω stop stand by normalized passband frequency and stopband frequency respectively. Let us consider a special case, when

$$Dpass = Dstop$$

$$\omega\ pass + \omega\ stop = \pi.$$

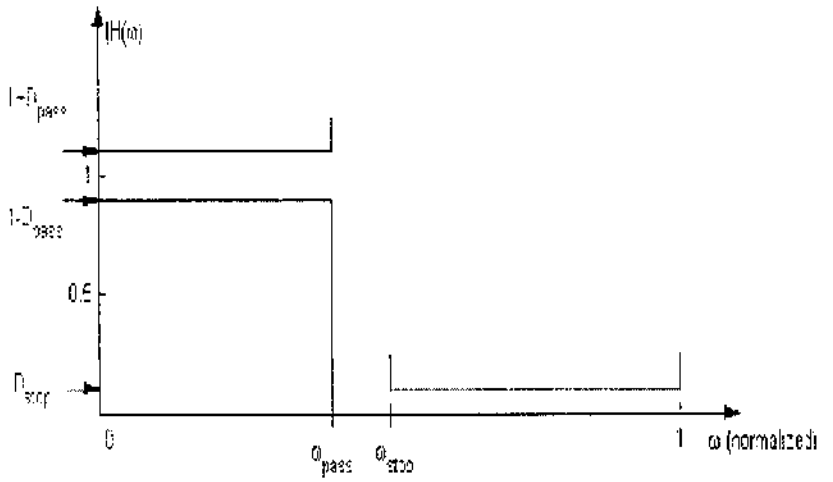

Figure 5.5 Lowpass Filter Specifications

Given this condition, the filter structure is called as half-band filter, which has been intensively studied in many literatures. The half-band filter has its cutoff frequency symmetrical around $\pi/2$which is in the middle of useful band. It leads to a simpler implementation structure compared to ordinary FIR implementation since its characteristics result in odd symmetry around $\pi/2$ and its impulse responses h(n) have zero values for all even values of n except n=0. In other words, half-band filter comprises of half multiplication blocks of common FIR filter, which further decreases the power consumption. However, this optimal architecture also has its constraints from flexibility point of view. Since the cutoff frequency must be set around $\pi/2$, the decimation ratio, in fact has been settled down at 2.

While using half-band decimation filters, it is required to confront the small available decimation rate which results in long cascaded half-band filters. The half-band filters are economical to decimator, where decimation ratios of 2 happen in each stage in the higher sampling rate.

Half-band filter is a kind of special FIR filter. Its frequency response is on the symmetry of $f_s/4$.Another, the coefficients of HB are symmetrical, to apply such trait, the number of coefficients can be reduced half again. So to achieve the half band filter by adopting "Folding FIR filter" .Using different encoding techniques can also substantially reduce the design computing operation. Therefore, CSD and MSD coding technique are employed to reduce computing operation. The structure of half band filter is shown in figure 5.6

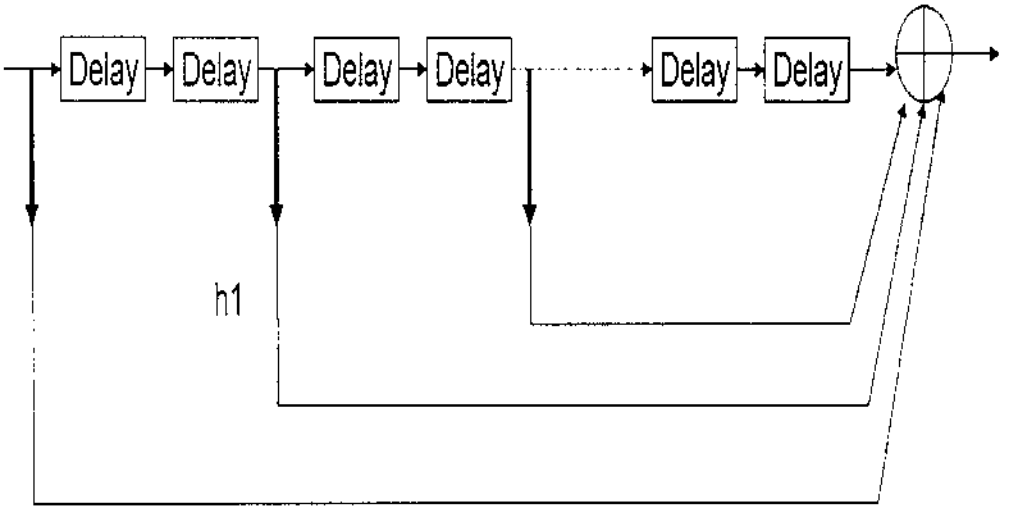

Figure 5.6 Structure of Half Band Filter

5.3 FIR FILTER

The last stage of decimation filter chain needs a compensation for the pass band droop caused by the CIC decimation that has a sinc-like response. This compensation filter keeps the passband smooth which is very important for the demodulation following up. In fact there is a demo in MATLAB about the digital down conversion, where it uses inverse sinc to compensate the CIC filter and then another FIR filter handles the further compression in the stopband. In this work, only one FIR filter is used to realize dual functions of the compensation and further compression.

Instead of inverse sinc function, FIR2 function that designs frequency sampling-based digital FIR filters with arbitrarily shaped frequency response is used. By the way of an example, figure 5.7 illustrates the frequency responses of front-end filters and compensation filters and the combinational decimation filters. It is apparent that the passband ripple stays in the limited ripple with effective compensation.

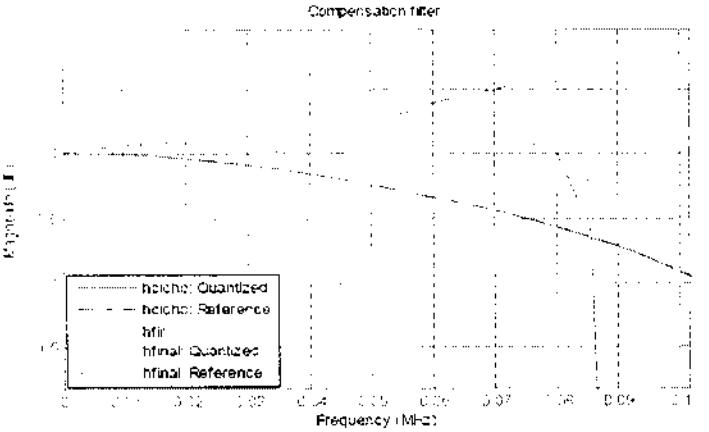

Figure 5.7 Compensation Filter

5.4 STANDARD SPECIFICATIONS

5.4.1 OVERVIEW

The target standards are described as table 5.1. This receiver profile determines the whole receiver architecture selection and design. For 802.11b, the channel width, in fact, is 25 and 30, in US and Europe respectively. Moreover, the 802.16 also has three standard channel widths as 20 or 25 in US and 30 in Europe.

Table 5.1 Multi-standard Receiver Profiles

Standards	GSM	WiMAX
Frequency range (GHz)	DL 0.935-0.96 UL 0.89-0.915	10-66
Channel spacing [MHz]	0.2	20
Sub carriers	1	256(192 data)
Symbol rate /chip rate	270.833 Ksymbol/s	16.704 Msymbol/s
Maximum User Data rate [Mbps]	0.0096	134
Modulation	0.3 GMSK	BPSK, QPSK, 16QAM, 64QAM, 256QAM

5.4.2 PARAMETERS FOR DECIMATION FILTER DESIGN

5.4.2.1 Dynamic Range

Dynamic Range (DR) is typically expressed in dB. The DR of an ADC is the range of signal amplitudes the ADC can solve. This factor plays a very important role in the communication applications where the signal swings quite dramatically. If the signal is too large, it will over-range the ADC input. Otherwise if the signal is too small, the signal will not be recognized due to the noise. In this project, it is assumed there are some variable gain controllers who can adjust signal strength before the signal goes into ADC. The values given in table 5.2 are only for draw the interference profile and filter mask in the consequent content. In the automatic gain controller, the practical DR is smaller than the differential between the sensitivity and max signal. In addition, sensitivity is the minimum signal level that the system can detect with acceptable signal to noise ratio. In the real test, we always give a little higher value in order to set up a certain margin.

Table 5.2 Dynamic Range

Standards	GSM	WiMAX
Sensitivity [dBm]	-102	-91
Max signal [dBm]	-15	-30

5.4.2.2 Blocking and Interference Profile

The interference blocks the signal of interest, so it is interpreted as the same items as interference or blocking. Interference is the major limiting factor in the performance of radio system. The interference results from another mobile in the same cell and the mobile in the neighboring cell. There are two kinds of interference in practice. One is co-channel and the other is adjacent channel interference. The interference comes from those which have the same set of frequency in a given area. This problem can only be solved by separating the co-channel base stations physically by a sufficient distance. Compared to coherence interference, the adjacent

interference, the neighboring signal, has more relation with filter design since it can be minimized through careful filtering and channel assignments. In sum, each standard has its own requirement on this issue, the communication only occurs properly when the interference limited in a certain range.According to the target standards, we can see the interference description is shown as table 5.3 and the figure 5.8.

Table 5.3 Interference Profile

Standards	GSM	WiMAX
Interference [MHz][dBm] (Frequency means offset from the central frequency)	0.2: -90 0.4: -58 0.6: -46 0.6-1.6: -43 1.6-3: -33 >3: -23	20: -68 40: -49

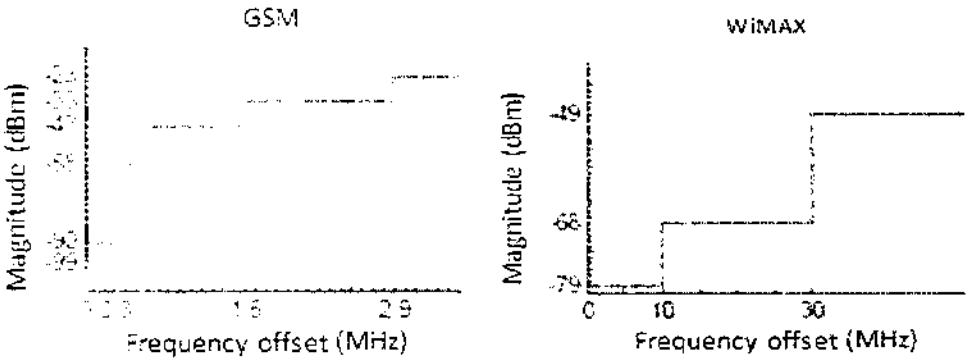

Figure 5.8 Blocking and Interference Profile

5.4.2.3 Carrier to Noise Ratio (CNR)

In the former parts, the input blocking profiles that are used to draw the filter masks are discussed and another important parameter Carrier to Noise Ratio (CNR), carriers to noise ratio, is going to be focused on this coming part. CNR states the output interference and blocking profile of the decimation filter in order to realize the correct demodulation and then to decide how much attenuation should decimation filters provide. It is not possible to gain the CNR from

the standards directly, so it is proposed to the other fundamental element E_b/N_o that is classically defined as the ratio of Energy per Bit (E_b) to the Spectral Noise Density (N_o).Then the relation between CNR and E_b/N_o is CNR = (E_b/N_o)*B, where B stands by how many bits per symbol, for instance, B=2 in QPSK. When we discuss bit error rates, which is regulated by the standards, or modulation methods, E_b/N_o explains the lowest signal to noise ratio in order to obtain a certain level of fidelity dependents on the target modulation. Different forms of modulations have different requirements on E_b/N_o. Too large noise that crosses the margin permitted in different modulations leads to signal crash. To gain the desired decimation filters, the crucial values has to be identified according to different standards in order to attain the ideal demodulation and draw filter masks as well. It is easy to calculate the desired CNR for each standard. For instance, WiMAX uses QPSK modulation where CNR is as twice large as E_b/N_o. The calculation goes as follows. Consider Bit Error Rate (BER)=10^{-3} and it is expressed by equation 5.2.

$$Q\left[\sqrt{\frac{2E_b}{N_o}}\right] = 10^{-3} \tag{5.2}$$

With the help of function *erfcinv* in MATLAB, CNR is arrived with 9.7998dB. However the popular value in literatures is 7.2dB. In addition, the same situation is identified in GSM that there is a differential between the value calculated and that used in previous research. It is possible that the coding rate in each standard relaxes the BER and thus results to a lower value than the theoretical value. For WiMAX, based on 16 QAM modulations which have a description about E_b/N_o of 14.5 with ¾ coding rate.

Table 5.4 Carrier to Noise Ratio of Different Standards

Standards	GSM	WiMAX
CN [dB]	9	21

The CNR for two standards is shown in table 5.4. Then the table 5.3 can be revised in order to draw the filter mask, which expresses the requirement for the cascade filters.

5.4.2.4 Passband and Ripple

Passband and passband ripple are another two elements to be considered when the filters are designed. In this work, it is observed that 80% of the bandwidth as the passband. For GSM, the values of passband ripples is 0.1 dB as shown in table 5.5; however in WiMAX, it is remarked to be assumptions.

Table 5.5 Passband and Ripple

Standards	GSM	WiMAX
passband [MHz]	0.08	8
Passband ripple [dB]	**0.1**	**0.5***

5.4.3 FILTER MASK DRAWING

Concerning the requirement in digital filter design, CNR is used for set up the level of stop band attenuation. That is, after the filter, the energy of passband signal must be as higher as CNR than the noise energy in stop band. Combining the permitted blocking signal energy and CNR, the filter masks can be derived. Regarding interferences, blockers and CNR, the last element before figuring out the filter mask is assumptions for the anti-aliasing filters. It is anti-aliasing filter that cooperates with decimation filter to remove the out of band noise, leaving an accurate digital replica of the original analog input. Figure 5.9 shows the channel selection filter. In this work, the largest signals after the anti-aliasing filters are 65dBand 39dB in GSM and WiMAX respectively. Figure 5.10 illustrates it more clearly and now we have got parameters prepared for the filter design.

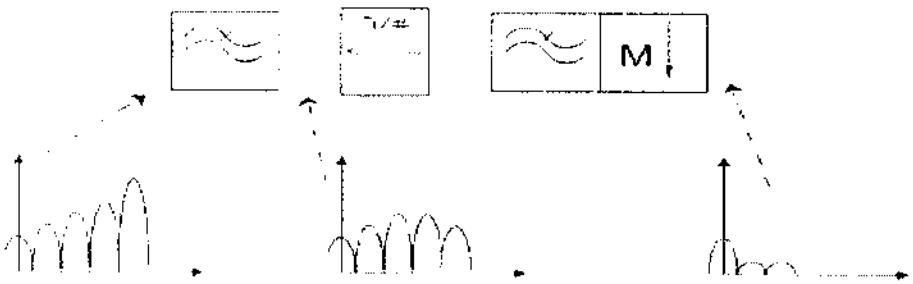

Figure 5.9 ChannelSelection Filter

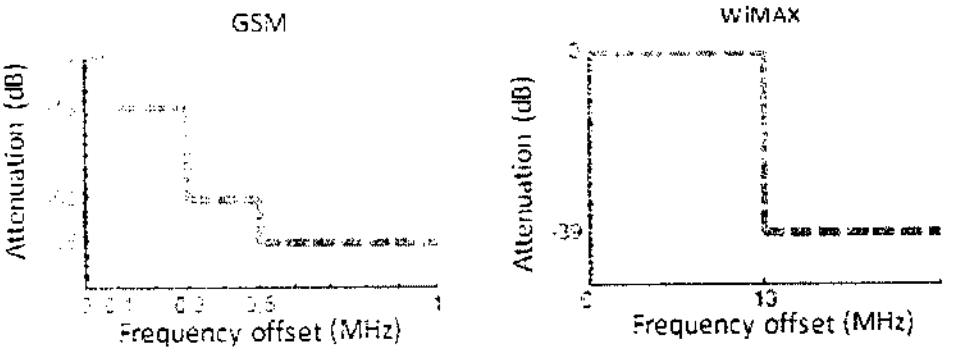

Figure 5.10 Decimation Filter Mask

5.4.4 SAMPLING FREQUENCY CALCULATIONS

Table 5.6 shows the various design parameters of the proposed strategies. To make the two methods comparable, the same OSR, filter structure and number of stages are considered for the design. Since the OSR is fixed, multibit modulators are used for WiMAX in order to satisfy requirements on the resolution. It is apparent that it is necessary to use both decimation and interpolation in the resampling block in order to realize the fractional conversion rate, which leads to bigger chip area than the second method, which only has integer decimation rate. In addition, it is recommended to keep the output sampling frequency higher than that of certain bandwidth concerning the anti-aliasing.

Table 5.6 Sampling Frequency

Standards			**GSM**	**WiMAX**
Quantization bits of modulators			1	4
OSR			250	5
M 1 Fixed Fs	Fs in decimation filters [MHz]	Input	100	100
		Output	0.4	20
	Fractional resampling rate as following ups		1.4769	1.1973
M 2 Variable Fs	**Fs in decimation filters [MHz]**	**Input**	**135.415**	**167.04**
		Output	0.541	33.4080
	Decimation rate as following ups		2	2
Symbol rate			270.833 Ksymbol/s	16.704 Msymbol/s
Passband [MHz]			**0.08**	**8**

5.5 PROPOSED MULTISTANDARD ARCHITECTURE

The aim of this work is to propose an architecture that uses the minimum multiplication operations and used for multiple standards. The decimation filter is a block that reduces the data rate from IF to baseband domain. Different communication standards require large factor of decimation resulting in large orders of filters. Multistage decimation reduces the overall complexity of system, by decomposing the decimation factor in several subfactors. Thus, each stage requires lower order filters. However, the use of several stages will increase control hardware complexity. Moreover, after four to five stages the filter complexity is not further reduced. Therefore a trade off between number of stages and complexity must be achieved. The figure 5.11 is the decimation filter architecture which supports two standards Wimax and GSM.

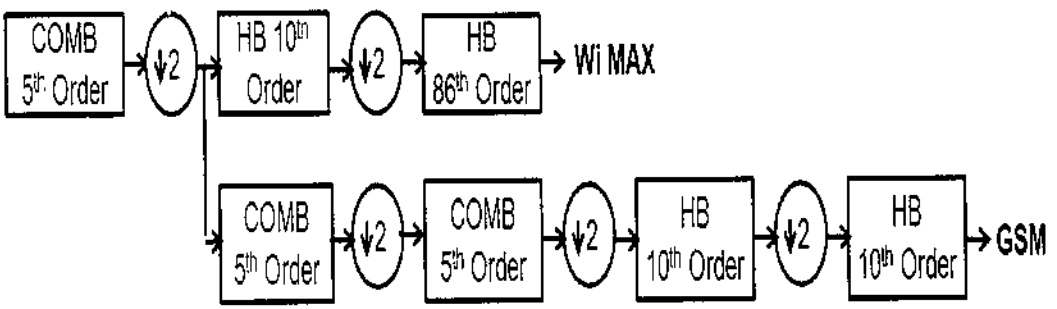

Figure 5.11 Architecture – Cascaded Decimation Chain

Furthermore, in order to have a multi-standard architecture with a unique cascade of filters for the three standards, the filter is realized by an architecture that exploits the similarities between the halfband filters. It is illustrated in figure 5.12. This process produces a multimode design, able to handle mutually different exclusive filters with efficient resource sharing. The design timing properties are not modified, glue logic as multiplexers are added to improve the hardware operators and registers sharing. In fact, using this method the halfband filters of the two standards are unified to keep only two filters instead of six. The first one has an order equal

to 10, which is the highest order between the orders of the second and the fourth filter of the standards WiMAX and GSM, respectively. As regards to the second halfband filter, it has an order equal to86. The most severe and the highest constraint between the last filters of the chains Wi-max and GSM, where the orders are respectively 86and26.

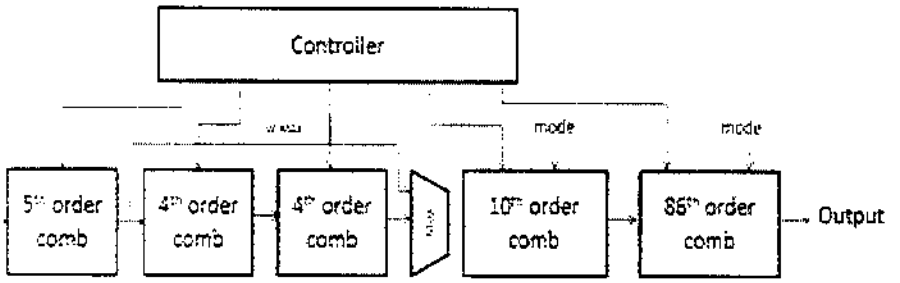

Figure 5.12 Decimation Chain with Unified Filters

Referring to figure 5.11 the halfband filters have a new input which corresponds to the selected decoding mode encoded into two bits. Depending on its value, the filter is able to download the coefficients, which correspond to the chosen standard. The multiplexer is placed before the two halfband filters. Depending on the mode, it selects the appropriate signal to finish its processing. This architecture allows to filter, in real time, one of the two standards (Wi-MAX or GSM) using a unique cascade of filters. Thus, the reconfigurability of the designed architecture is guaranteed. In addition, it may reduce the power consumption and the area of the receiver. The number of multiplications varies according to the selected mode too, as it is the case for the second architecture. It is respectively equal to 27or 12 when a Wi-max or GSM signal is being treated.

CHAPTER 6

NUMBER REPRESENTATION

In the previous section, all examples use the binary representation for the numerical values, where a number is decomposed as a sum of powers of two. Although, this is the numerical representation of choice for computer arithmetic, alternative representations can offer advantages, when implementing multiplications with known constants based on shift-adds. The representation of numbers using a sign digit system makes the use of positive and negative digits. The binary sign digit representation decomposes a number in a set of additions and subtractions of powers of two. Thus, an integer $C_i2^i=k$ represented in the binary sign digit system can be written as in equation 6.1.

$$k = \sum_{i=0}^{N-1} C_i 2_i \tag{6.1}$$

where c_i belongs to {1, 0,−1} and N is the number of digits used to represent k.

6.1 CANONICAL SIGNED DIGIT REPRESENTATION

The Canonical Signed Digit (CSD) representation is a signed digit system that has a unique representation for each value and verifies two main properties:

- The number of non-zero digits is minimal.
- Two non-zero digits are not adjacent.

This representation is widely used in multiplier less implementations, because it reduces the hardware requirements due to the minimum number of non-zero digits. Any N digit number in CSD format has at most (N+1)/2 non-zero digits, thus requires only that number of operators (adders/subtracters). On average the number of non-zero digits is reduced by 33%, when compared with the binary representation.

To obtain the CSD representation of a number, one could start processing its binary representation from the least significant digit to the most significant digit and replace repeatedly all the sequences found as 01...1 by the sequence10...01 with the same number of digits. This procedure is implemented by the pseudo-code presented in Figure 6.1, which uses a conversion table and a state variable to detect the ones sequences and generate the CSD output.

Inputs			Outputs	
State	b i+1	bi	ci	next_state
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	-1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	-1	1
1	0	1	0	1

```
CSD(b, N) {
    state = 0;
    bN = 0;
    bN+1 = 0;
    for i = 0 to N {
        ci = get out val from table(state, bi+1, bi);
        state = get next state from table(state, bi+1, bi);
        }
return c;
}
```

Figure 6.1 Pseudo-Code to Compute CSD using Conversion Table

6.2 MINIMUM SIGNED DIGIT REPRESENTATION

The Minimum Signed Digit (MSD) representation is obtained by dropping the second property of the CSD representation. Thus, a constant can haveseveral representations under MSD, but all with a minimum number of non-zerodigits. For example, consider the constant 23 defined in six bits. The representation of 23 in binary, 010111, includes 4 non-zero digits. The constant is represented as 101001 in CSD and both 101001 and 011001 denote 23 in MSD with 3 non-zero digits.

The MSD representations of a number can be computed from its CSD representation by replacing all possible combinations of the sequences 101 and 101 by the sequences 011 and 01 1, respectively. For each replacement, a MSD representation is obtained, since the number of non-zero digits does not increase. Figure 6.2 presents the pseudo-code of an algorithm that computes the MSD representations of a number from its CSD representation using the described replacement technique. Note that there are other optimized and alternative algorithms that compute the CSD and MSD representations of a number.

```
MSD (c, N) {
 MSD set= {c};
 working set= {c};
 while (working set6= 0){
  one rep = getelement(working set);
  for i = 0 to N - 2{
   if (matching(one repi, '101')) {
    new rep = replace three matching digits(one repi, '011');
    working set= working set? {new rep};
    MSD set= MSD set? {new rep};
   }
   if (matching(one repi, '101')) {
    new rep = replace three matching digits(one repi, '01 1');
    working set= working set? {new rep};
    MSD set= MSD set? {new rep};
   }
  }
 }
 return MSD set;
 }
```

Figure 6.2 Pseudo-code to Compute MSD from CSD Representation

The advantage of using the MSD representation for a coefficient results from increasing the possibilities of sharing partial terms between coefficients. This results from the fact that, in general, there exist several alternatives to represent a given coefficient in MSD. Consequently, there are more ways to decompose the coefficient with different partial terms that can be shared with other coefficients. Figure 6.3 shows all possible implementations that obtain 23x using CSD and MSDrepresentations of the constant 23.

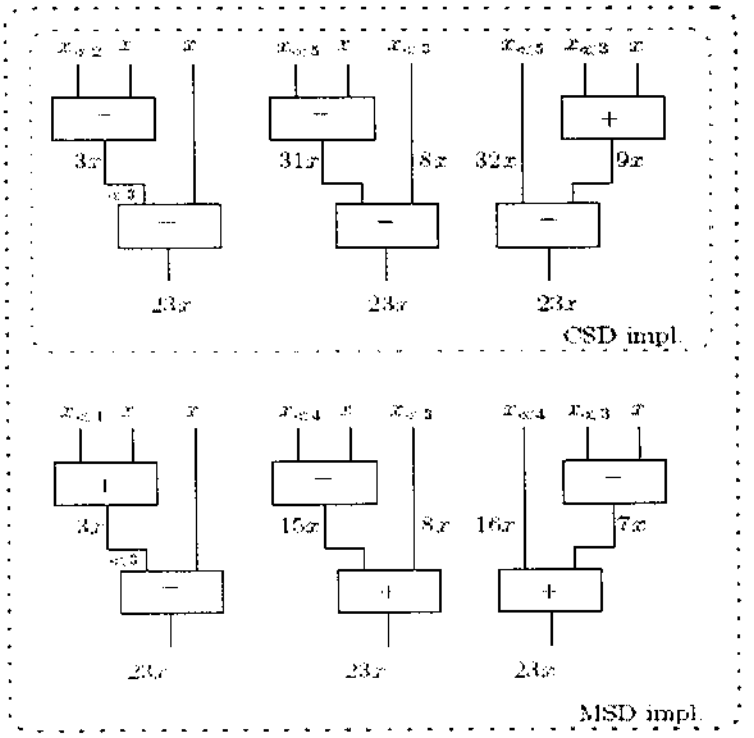

Figure 6.3 Representation of Numbers using CSD andMSD Implementation

6.3 COMPARISON

To minimize the chip size, the Signed Power-of-Two (SPT) method is adopted to implement the FIR filter without multipliers. Unfortunately, the SPT method can not guarantee the least numbers of adders and shifts, because of its various expressions. For example, the value of 23 can be expressed as three types, 010111, 01100-1, and 10-100-1. In order to overcome this fault, a Canonic Signed-Digit (CSD) representation can be employed to implement the basic shift-and-add algorithm. The algorithm of CSD is expressed as {11→10-1; 1-1→01;- 11→0-1;-1-1→-101}. Then a value of 27 can be expressed with the following steps: 11011→1110-1→10-110-1→100-10-1.

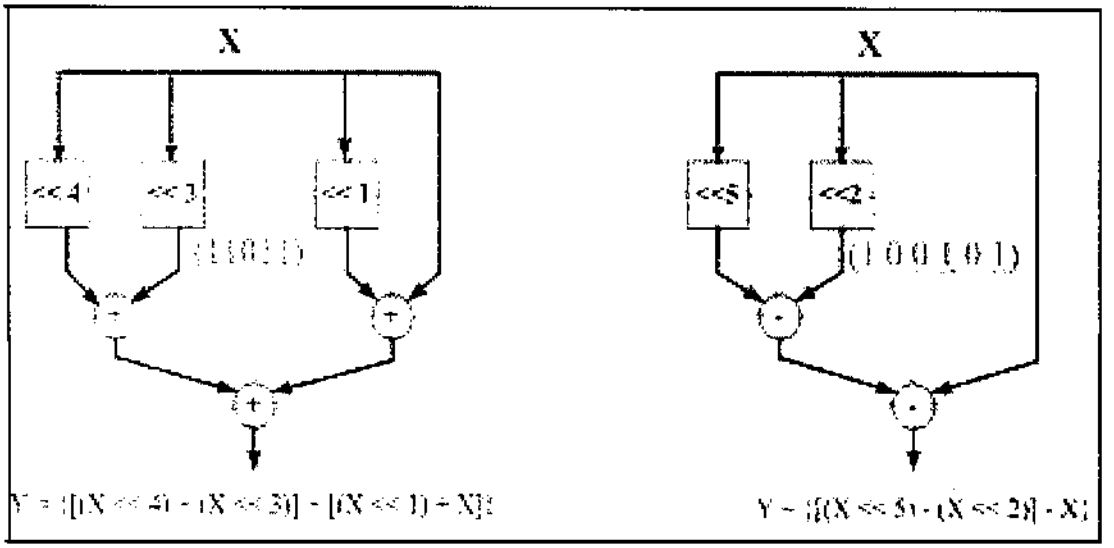

Figure 6.4 Comparison of Shift-And-Add Numbers between SPT and CSD

Figure 6.4 shows a comparison of shift-and-add numbers between SPT and CSD. The CSD obviously operates with lower adders and shifters.

CHAPTER 7
RESULTS AND DISCUSSION

The simulation of this project has been done using MATLAB 7.3, MODELSIMPE 5.4e and XILINX ISE 7.1i.

MATLAB (meaning "**MAT**rix **LAB**oratory") was invented in the late 1970s by Cleve Moler, then chairman of the computer science department at the University of New Mexico. MATLAB was first adopted by control design engineers, Little's specialty, but quickly spread to many other domains. It is now also used in education, in particular the teaching of linear algebra and numerical analysis, and is popular amongst scientists involved with image processing. It provides many convenient ways for creating vectors, matrices, and multi-dimensional arrays.

Modelsim is a simulation tool for programming {VLSI} {ASIC}s, {FPGA}s, {CPLD}s, and {SoC}s. Modelsim provides a comprehensive simulation and debug environment for complex ASIC and FPGA designs. Support is provided for multiple languages including Verilog, SystemVerilog, VHDL and SystemC.

Xilinx was founded in 1984 by two semiconductor engineers, Ross Freeman and Bernard Vonderschmitt, who were both working for integrated circuit and solid-state device manufacturer Zilog Corp. The Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6 FPGA families are particularly focused on system-on-chip (SOC) designers because they include up to two embedded IBM PowerPC cores. The ISE Design Suite is the central electronic design automation (EDA) product family sold by Xilinx. The ISE Design Suite features include design entry and synthesis supporting Verilog or VHDL, place-and-route (PAR), completed verification and debug using Chip Scope Pro tools, and creation of the bit files that are used to configure the chip.

7.1 COMB FILTER

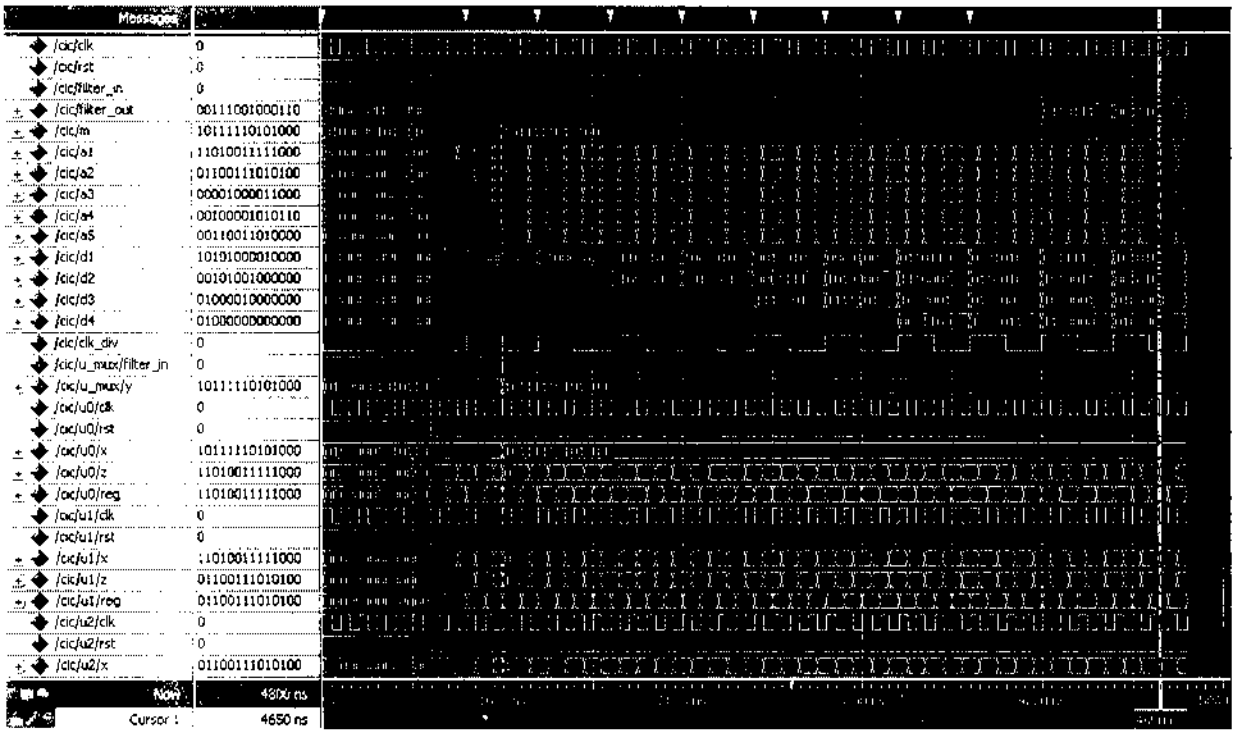

Figure 7.1 Simulation Result of Five Stage Comb Filter Output

Input frequency = 5 MHZ

Input bit value = 1 bit

Output frequency = 2.5 MHZ

Output bit value = 13 bits

7.2 DECIMATION FILTER COEFFICIENTS

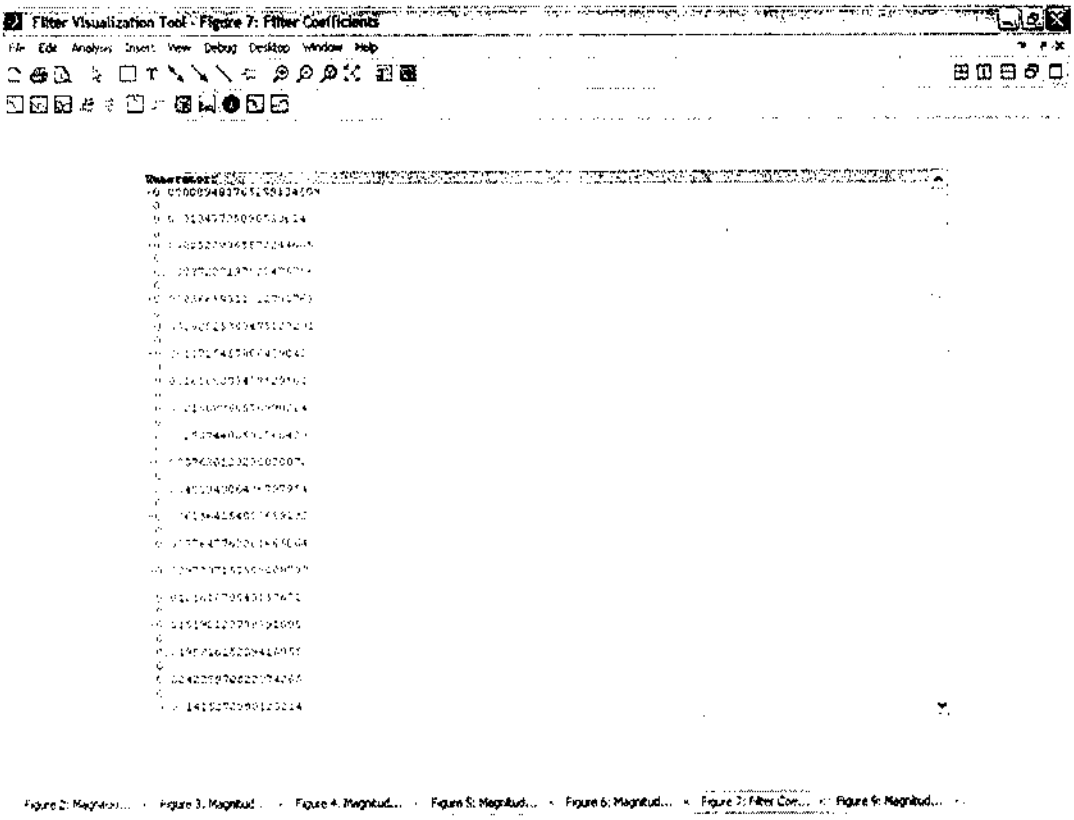

Figure 7.2 Filter Coefficients of Three Stage Decimation Filter

7.3 HALFBAND FILTER USING CSD REPRESENTATION

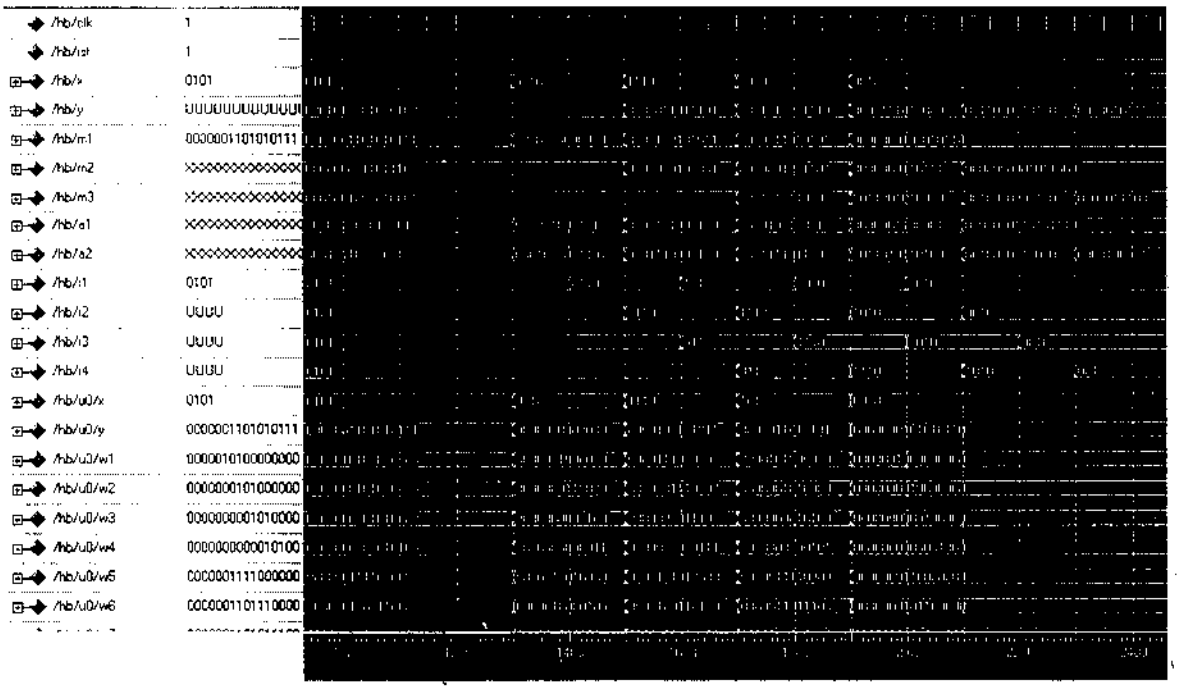

Figure 7.3 Simulation Result of Halfband Filter using CSD Representation

Input frequency = 2.5 MHZ

Input bit value = 13 bit

Output frequency = 1.25 MHZ

Output bit value = 16 bits

7.4 HALFBAND FILTER USING MSD REPRESENTATION

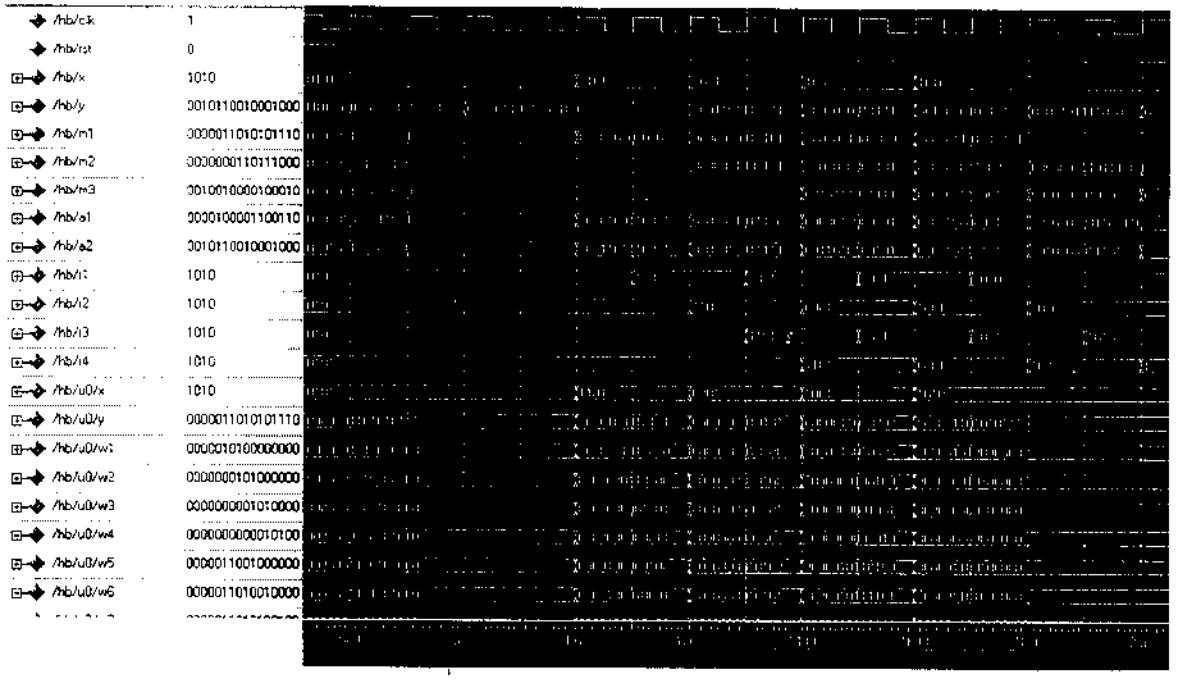

Figure 7.4 Simulation Result of Halfband Filter using MSD Representation

Input frequency = 2.5 MHZ

Input bit value = 13 bit

Output frequency = 1.25 MHZ

Output bit value = 16 bits

7.5 DECIMATION FILTER FOR GSM STANDARD

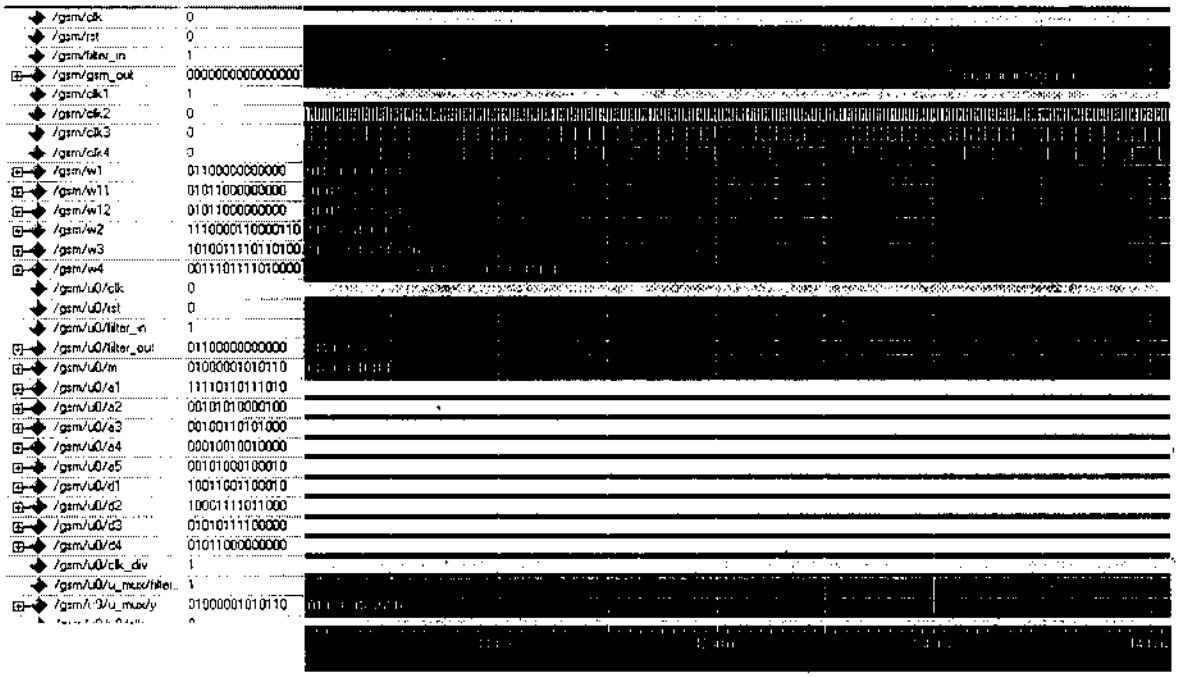

Figure 7.5 Simulation Result of Decimation Filter for GSM Standard

Decimation Factor : 2 at each stage

Input bit value = 1 bit

Output bit value = 16 bits

7.6 DECIMATION FILTER FOR WIMAX STANDARD

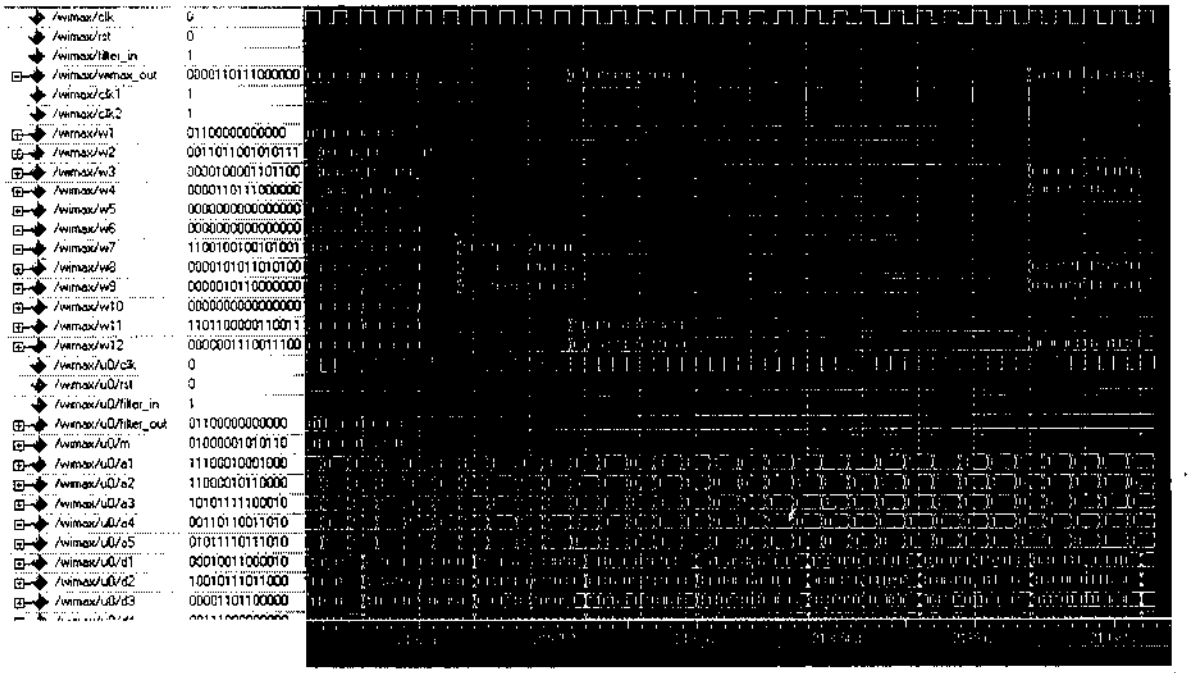

Figure 7.6 Simulation Result of Decimation Filter for WiMAX Standard

Decimation Factor	:	2 at each stage
Input bit value	=	1 bit
Output bit value	=	16 bits

7.7 DECIMATION FILTER USING UNIFIED FILTERS

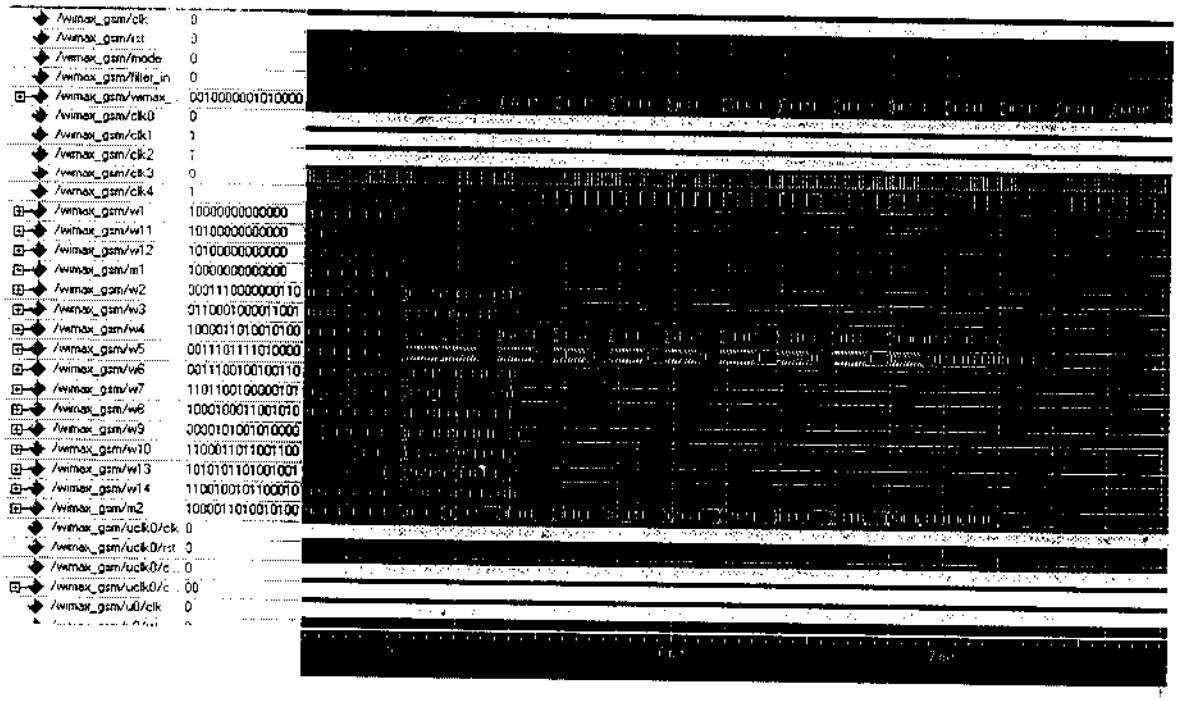

Figure 7.7 Simulation Result of Decimation Filter using unified filters

Mode 0 : GSM standard

Mode 1 : WiMAX standard

7.8 USING CONVENTIONAL MULTIPLIER:

7.8.1 MAP REPORT

Design Summary

Logic Utilization:

Number of Slice Flip Flops:	333 out of 13,824	3%
Number of 4 input LUTs :	348 out of 13,824	3%

Logic Distribution:

Number of occupied Slices	:	421 out of 6,912		3%
Number of Slices containing only related logic	:	235 out of 235		100%
Number of Slices containing unrelated logic	:	0 out of 235		0%

*See NOTES below for an explanation of the effects of unrelated logic

Total Number 4 input LUTs	:	425 out of 13,824		4%
Number used as logic	:	278		
Number used as a route-thru	:	17		
Number of bonded IOBs	:	24 out of	510	5%
Number of GCLKs	:	3 out of	4	75%
Number of GCLKIOBs	:	1 out of	4	25%

Total equivalent gate count for design: 3,182

7.8.2 POWER REPORT

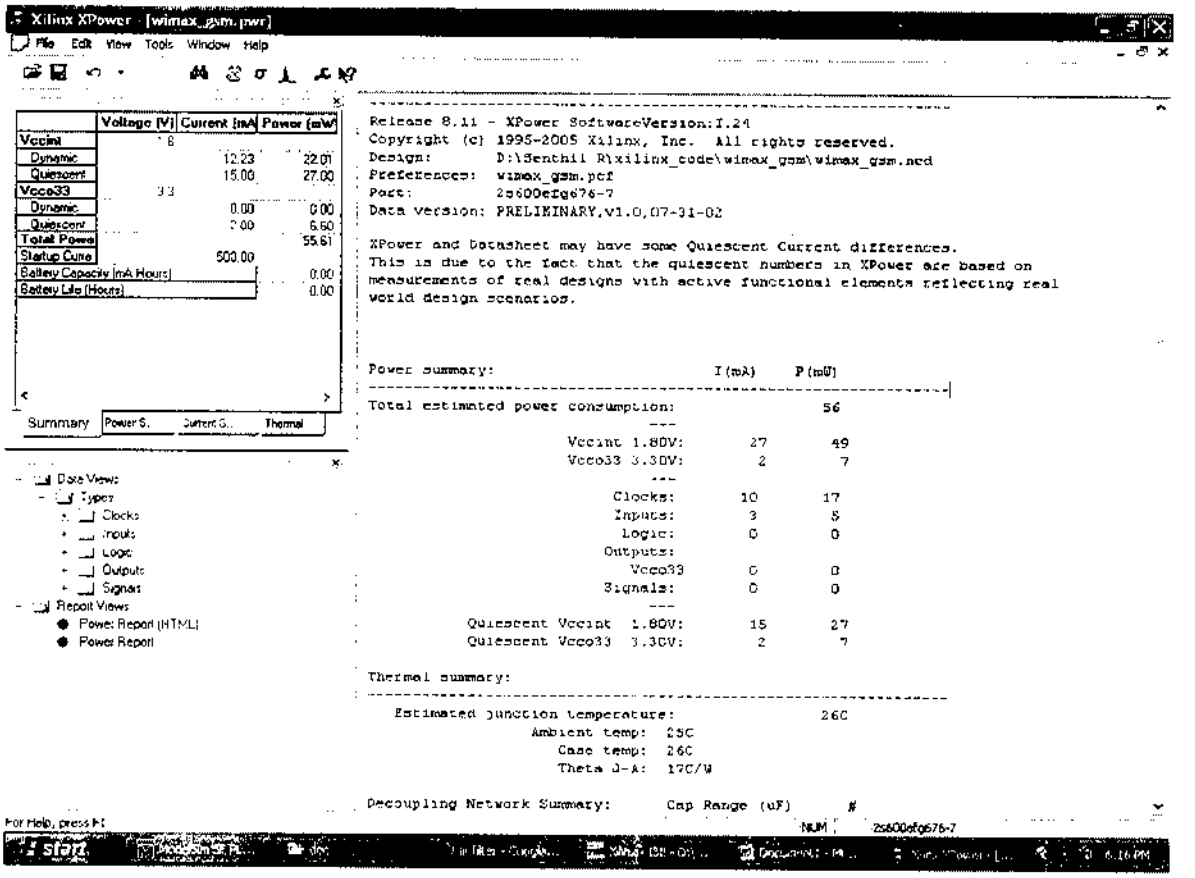

Figure 7.8 Power Report using Conventional Multiplier

7.9 USING CSD REPRESENTATION

7.9.1 MAP REPORT

Design Summary

Logic Utilization:

Number of Slice Flip Flops:	183 out of 13,824	2%
Number of 4 input LUTs :	238 out of 13,824	2%

Logic Distribution:

Number of occupied Slices	:	235 out of	6,912	2%
Number of Slices containing only related logic	:	235 out of	235	100%
Number of Slices containing unrelated logic	:	0 out of	235	0%

*See NOTES below for an explanation of the effects of unrelated logic

Total Number 4 input LUTs	:	325 out of	13,824	4%
Number used as logic	:	278		
Number used as a route-thru	:	17		
Number of bonded IOBs	:	24 out of	510	5%
Number of GCLKs	:	3 out of	4	75%
Number of GCLKIOBs	:	1 out of	4	25%

Total equivalent gate count for design: 2,762

7.9.2 POWER REPORT

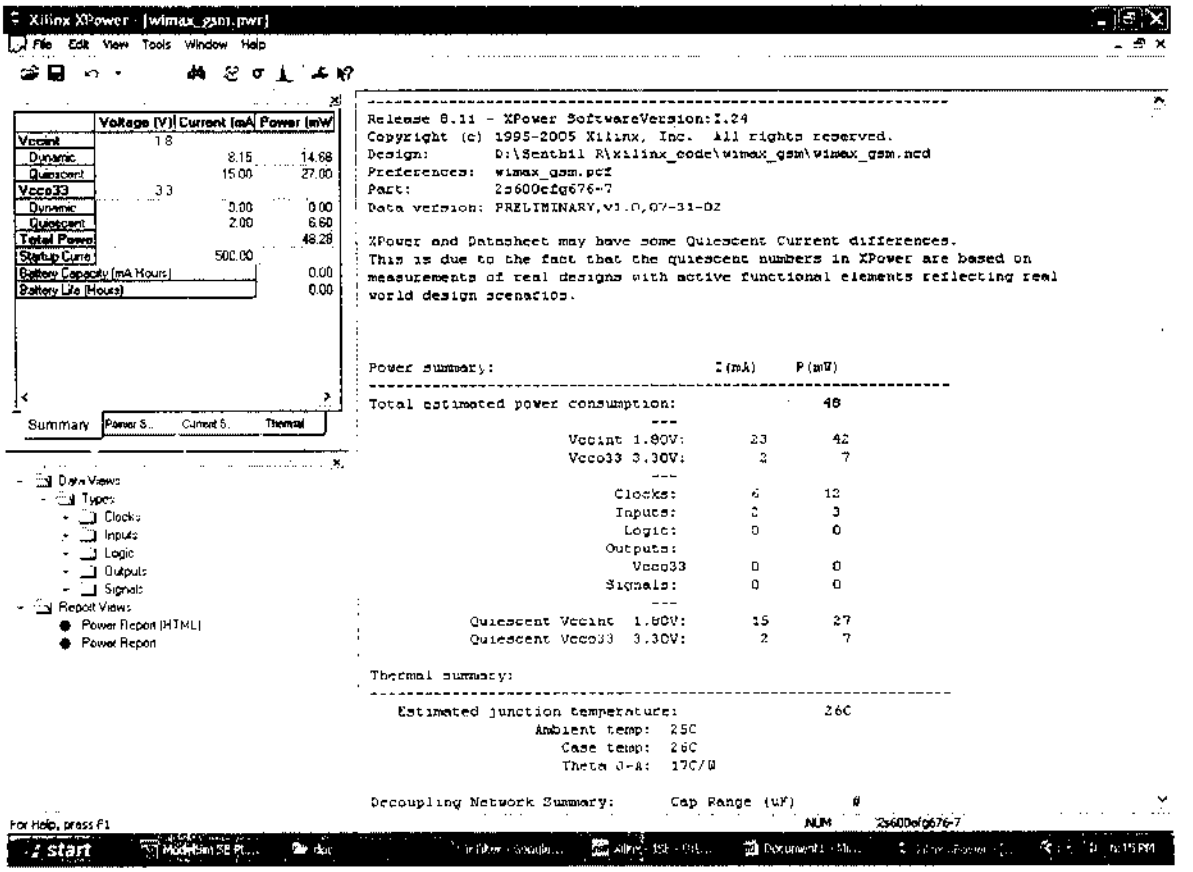

Figure 7.9 Power Report using CSD Representation

7.10 USING MSD REPRESENTATION

7.10.1 MAP REPORT

Design Summary

Logic Utilization:

Number of Slice Flip Flops:	77	out of 13,824	1%
Number of 4 input LUTs :	138	out of 13,824	1%

Logic Distribution:

Number of occupied Slices	:	135	out of	6,912	3%
Number of Slices containing only related logic	:	135	out of	235	100%
Number of Slices containing unrelated logic	:	0	out of	235	0%

*See NOTES below for an explanation of the effects of unrelated logic

Total Number 4 input LUTs	:	155	out of 13,824	4%
Number used as logic	:	138		
Number used as a route-thru	:	17		
Number of bonded IOBs	:	19	out of 510	3%
Number of GCLKs	:	3	out of 4	75%
Number of GCLKIOBs	:	1	out of 4	25%

Total equivalent gate count for design: 2,230

7.10.2 POWER REPORT

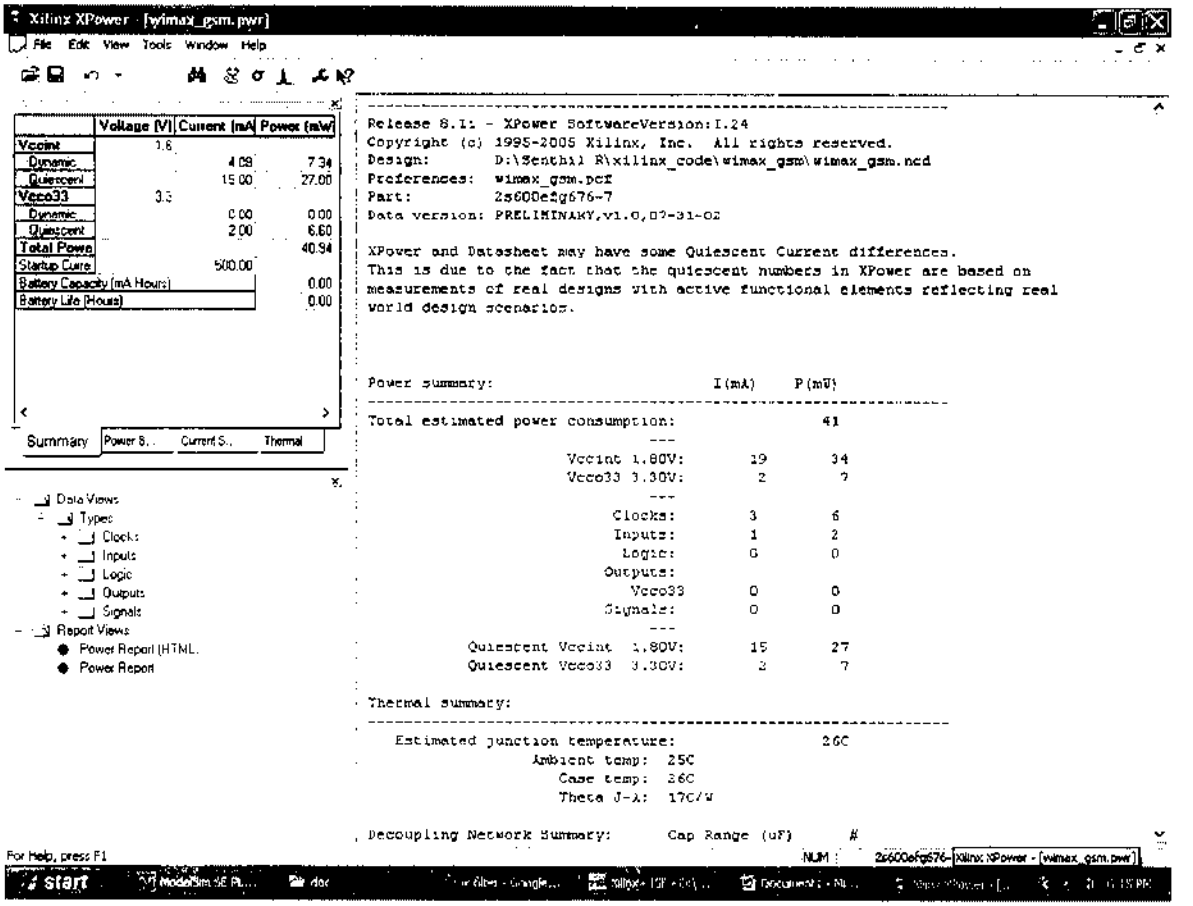

Figure 7.10 Power Report using MSD Representation

Table 7.1 Comparison of Decimation Filter Architecture

Number representation	Cascaded Decimation chain		Decimation chain with Unified Filters	
	Total Gate Count	Power	Total Gate Count	Power
Conventional	4279	57.45	3182	55.61
CSD	3968	50.11	2762	48.28
MSD	3172	42.77	2230	40.94

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

This project discusses the design and implementation of a decimation filter for use in the Sigma-Delta Analog to Digital-converter (SD-A/D). The decimation filter down-samples the data at the rate of 128:1, with 4 KHz cut-off frequency. The architecture designed is based on a CIC filter connected to 2-stage half-band filters. The coefficients of half band filter are implemented using CSD and MSD representations. The power consumption of decimation filter using MSD representation is better than that of the CSD representation. The proposed architecture is designed for multistandard applications.It fulfils the requirements of two standards: Wi-max and GSM.

The proposed decimation filter architecture requires less hardware and contributes to a hardware saving of 88%, compared tothe conventional architecture.The advantage of the proposed filter in comparison to the existing is that a considerable reduction in hardware due to reduction in number of adders. The power consumption of the decimation filter using CSD, MSD representations and for unified filters are identified to be 56mw, 48mw and 41mw respectively.

FUTURE SCOPE

The future scope of this project is to explore and implement the proposed digital filter hardware architecture using cyclotomic polynomials and modified comb filter structures for optimization of design issues.

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