A SPURIOUS POWER SUPPRESSION TECHNIQUE FOR H.264 CODEC AND VERSATILE MULTIMEDIA FUNCTIONAL UNIT

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A PROJECT REPORT

Submitted to the

FACULTY OF ELECTRONICS AND COMMUNICATION ENGINEERING

In partial fulfillment of the requirements for the award of the degree

of

MASTER OF ENGINEERING

IN

APPLIED ELECTRONICS

APRIL 2011

BONAFIDE CERTIFICATE

Certified that this project report titled "**A SPURIOUS POWER SUPPRESSION TECHNIQUE FOR H.264 CODEC AND VERSATILE MULTIMEDIA FUNCTIONAL UNIT**" is the bonafide work of **Ms. V.MANIMEKALAI (0920106009)** who carried out the project work under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project report of dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ACKNOWLEDGEMENT

A project of this nature needs co-operation and support from many for successful completion. In this regards, we are fortunate to express our heartfelt thanks to **Padmabushan Arutselvar Dr.N.Mahalingam B.Sc.,F.I.E.,Chairman and Co-Chairman Dr.B.K.Krishnaraj Vanavarayar B.com.,B.L.,** for providing necessary facilities throughtout the course.

I would like to express my thanks and appreciation to many people who have contributed to the successful completion of this project. First I thank **Dr.J.Shanmugam Ph.D.,Director,** for providing us an opportunity to carry out this project.

I wish to acknowledge my sincere gratitude and thanks to our beloved Principal **Dr.S.Ramachandran Ph.D.,** for having given me the adequate support and opportunity for completing this project work successfully.

I express my sincere thanks to **Dr.Rajeswari Mariappan Ph.D.,** the ever active, Head of the Department of Electronics and Communication Engineering, who rendering me all the time by helps throughout this project.

In particular, I wish to thank and everlasting gratitude to the project coordinator **Ms.R.Latha M.E.,** Asso.Professor, Department of Electronics and Communication Engineering for her expert counseling and guidance to make this project to a great deal of success with her careful supervision and ensured me in the attaining perfection of work.

I extend my heartfelt thanks to my internal guide **Ms.M.Shanthi M.S.,** Asso.Professor, Department of Electronics and Communication Engineering for her ideas and suggestion, which have been very helpful for the completion of this project work.

Last, but not the least, I would like to express my gratitude to my family members, friends and to all my staff members of Electronics and Communication Engineering department for their encouragement and support throughout the course of this project.

ABSTRACT

The development of the wireless infrastructure and the personal electronic devices like video mobile phones, mobile TV sets PDAs, etc., multimedia and DSP applications have been adopted in wireless environments. However, advanced multimedia/DSP applications such as H.264 CODECs induce much more algorithmic complexity, which increases the power consumption in real-time operation besides the cost in implementation. Therefore, dedicated low-power techniques are important for multimedia/DSP VLSI implementation. This project presents the design exploration and applications of a spurious-power suppression technique (SPST) which can dramatically reduce the power dissipation of combinational VLSI designs for multimedia/DSP purposes.

The proposed SPST separates the target designs into two parts, i.e., the most significant part and least significant part (MSP and LSP), and turns off the MSP when it does not affect the computation results to save power. Two multimedia/DSP design examples, i.e., a multi transform design for H.264 and a versatile multimedia functional unit (VMFU, is adopted to evaluate the proposed SPST. The design is implemented in VHDL (Very high speed integrated circuits Hardware Description Language) and logic simulation is done using Modelsim XE III 6.2g and synthesis is done using Xilinx ISE 9.2i. The VMFU and ETD are implemented with SPST based arithmetic circuits and also with conventional arithmetic units. Power comparison is made and it is found that SPST based design resulted in less power consumption. The multi transform design implemented with SPST saves power of about 41.6% and SPST equipped VMFU saves power of about 52.6%.

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LIST OF ABBREVIATIONS

ABEL	-------	Advanced Boolean Equation Language
CMOS	-------	Complementary Metal Oxide Semiconductor
CPLD	-------	Programmable Logic Devices
DRD	-------	Dynamic Range Detection
DSP	-------	Digital Signal Processing
ETD	-------	Efficient Transform Design
HDL	-------	Hardware Descriptive Language
LSP	-------	Least Significant Part
MPEG	-------	Moving Pictures Expert Group
MSP	-------	Most Significant Part
PGC	-------	Partial Guarded Computation
PS	--------	Pseudo Summations
SAD	-------	Sum of Absolute Difference
SE	-------	Sign Extension
VCEG	--------	Video Coding Experts Group
VMFU	--------	Versatile Multimedia Functional Unit
VHDL	-------	Very high speed integrated circuits Hardware Description Language
VLSI	-------	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

There are different entities that one would like to optimize when designing a VLSI circuit. These entities can often not be optimized simultaneously, and it is possible to improve only one entity at the expense of one or more others. The design of an efficient integrated circuit in terms of power, area, and speed simultaneously, has become a very challenging problem. Power dissipation is recognized as a critical parameter in modern VLSI design field. In Very Large Scale Integration, Low power VLSI design is necessary to meet MOORE'S law and to produce consumer electronics with more back up and less weight.

There are two major sources of power dissipation in digital CMOS circuits: dynamic power and static power. Dynamic power is related to circuit switching activities or the changing events of logic states, including power dissipation due to capacitance charging and discharging, and dissipation due to short circuit current. Dynamic power dissipation, which is major part of power dissipation, is due to charging and discharging capacitance in the circuit. The static power is primarily determined by fabrication technology considerations, which are usually several orders of magnitude smaller than dynamic power. In order to save significant power consumption, it is a good direction to reduce dynamic power, which is the major part of power consumption.

Owing to the vigorous development of the wireless infrastructure and the personal electronic devices like video mobile phones, mobile TV sets, PDAs, etc., multimedia and DSP applications have been adopted in wireless environments. H.264 becomes popular in wireless environments due to the significant compression ratio improvement and the network friendly design, as compared to previous MPEG standards [1]. However, H.264 CODEC system also induces much more algorithmic complexity [2], which increases the cost in real-time implementing the H.264 video coding systems. Besides, lowering down the power consumption of the circuit designs is undoubtedly one of the design challenges when H.264 is applied on portable electronics. Therefore, dedicated low power VLSI designs become good choices in the H.264 implementation considering both the real-time processing and the low-power requirements.

1.1 LITERATURE SURVEY

Various techniques have been developed for reducing the power consumption of VLSI designs, including voltage scaling, switched-capacitance reduction, clock gating, power-down techniques, threshold-voltage controlling, multiple supply voltages, and dynamic voltage frequency scaling [3]–[6]. These low-power techniques have been proven to be efficient at certain expense and are applicable to multimedia/DSP designs. Among these low-power techniques, a promising direction for significantly reducing power consumption is reducing the dynamic power which dominates total power dissipation. Consequently, this project work develops a new low-power technique which can reduce dynamic power. The proposed low power technique can be used with some of the aforementioned techniques without conflicts to further reduce the power consumption of the multimedia/DSP designs. The existing works that reduce the dynamic power consumption by minimizing the switched capacitance include the designs in [7]–[12]. The design in [7] proposes a concept called partially guarded computation (PGC), which divides the arithmetic units, e.g., adders and multipliers, into two parts and turns off the unused part to minimize the power consumption. The reported results show that the PGC can reduce power consumption by 10%–44% in an array multiplier with 30%–36% area overheads in speech-related applications. However, the PGC technique cannot gain any power reduction when applied on adders because of the overhead- augmented circuitry. The design in [8] proposes a 32-bit 2's complement adder equipping a two-stage (master and slave stages) flip-flop at each of the two inputs, a dynamic-range determination (DRD) unit and a sign-extension (SE) unit, which tends to reduce the power dissipation of conventional adders for multimedia applications. Additionally, the design in [9] presents a multiplier using the DRD unit to select the input operand with a smaller effective dynamic range to yield the Booth codes. However, the DRD unit induces additional delay and area overheads. Besides, the input data flows are also frequently switched if the input operands with a smaller effective dynamic range often change between operands A and B, and vice versa. In such cases, the power dissipation of the designs in [8] and [9] is increased rather than decreased. The design in [10] incorporates a technique for glitching power minimization by replacing some existing gates with functionally equivalent ones that can be frozen by asserting a control signal. This technique can be applied to replace layout-level descriptions and guarantees predictable results. However, it can only achieve savings of

6.3% in total power dissipation, since it operates in the layout-level environment which is tightly restricted. The design in [11] proposes a double-switch circuit-block switch scheme capable of reducing power dissipation during downtime by shortening the settling time after reactivation. The drawbacks of the scheme are the necessity for two independent virtual power rails and the requirement for two additional transistors for switching each cell. At last, the design in [12] presents a DCT core exploiting an adaptive bandwidth approach and a method which trades off power consumption and arithmetic precision.

1.2 OBJECTIVE

To implement a low power VLSI technique called Spurious Power Suppression Technique (SPST) and its application for Efficient Multitransform Coding design (ETD) for H.264 and a versatile multimedia functional unit (VMFU). The proposed SPST technique separates the design of 16 bit adder/subtractor used in these two applications into two parts namely most significant part (MSP) and least significant part (LSP). The MSP is turned off whenever it does not affect the computation result. Turning off MSP avoids unnecessary signal transitions and helps to save power. Thus dynamic power dissipated due to unwanted computations is reduced.

1.3 METHODOLOGY

- SPST based 16 bit adder/subtractor unit is designed by exploring the five possible cases of 16- bit additions.
- SPST is applied on the ETD and power analysis is done with SPST and without SPST.
- The VMFU is implemented with SPST circuits as well as with conventional arithmetic circuits. Power analysis is done for both the cases and the results are tabulated.

The modules are implemented using Xilinx and the power dissipation results are compared

1.4 ORGANISATION OF THE REPORT

The design of low power adder/subtractor adopting SPST and the application of proposed SPST on the ETD for H.264 as well as for VMFU is explored. The ETD can compute three transforms, i.e., the forward, inverse, and Hadamard transform, adopted in H.264 video encoding inverse, and Hadamard transform, adopted in H.264 video encoding.

The report is arranged as follows:

- Chapter 2 deals with the fundamentals of Spurious Power Suppression Technique.
- Chapter 3 deals with the design of SPST based Adder/ Subtractor unit.
- Chapter 4 deals with the design examples of SPST namely (1) Efficient Multitransform Design (ETD) for H.264 and (2) Versatile Multimedia Functional unit (VMFU).
- Chapter 5 discusses the implementation of the proposed SPST technique.
- Chapter 6 deals with simulation results and discussions.
- Chapter 7 deals with conclusion and future work.

CHAPTER 2

SPURIOUS POWER SUPPRESSION TECHNIQUE FUNDAMENTALS

2.1 SPURIOUS POWER SUPPRESSION TECHNIQUE

Spurious power suppression technique is a low power VLSI technique to reduce unwanted power. Spurious signal is an unwanted signal flowing through the circuit. Hence this technique is used to suppress the unwanted power required by the circuit for its performance and operation. The SPST uses a detection logic circuit to detect the effective data range of arithmetic units namely adders and multipliers. When a portion of data does not affect the final computing results, the data controlling circuits of the SPST latch this portion to avoid useless data transitions occurring inside the arithmetic units. Besides there is a data asserting control realized by using registers to further filter out the useless spurious signals of the arithmetic unit every time when the latched portion is turned on. The proposed SPST separates the target design into two parts, i.e., the most significant part (MSP) and the least significant part (LSP), and turns off the MSP when it does not affect the computation results to save power.

2.2 APPLICATIONS OF SPST

The SPST can dramatically reduce the power dissipation of combinational VLSI designs for multimedia/DSP applications. The two main applications of SPST for multimedia/DSP purposes are (1) Efficient Multi Transform (ETD) Design for H.264 and (2) Versatile Multimedia Functional Unit (VMFU). H.264/AVC is the current video standardization project of the ITU-T Video Coding Experts Group (VCEG) and the ISO/IEC Moving Picture Experts Group (MPEG). The H.264 multitransform requires more than two times higher data processing performance than the individual transform. The ETD can compute three transforms, i.e., the forward, inverse, and Hadamard transform, adopted in H.264 video encoding. The ETD can achieve the real-time performance requirements of HD720, HD1080, and digital cinema of the H.264 encoding system when operated at 22, 50, and 100 MHz, respectively. The VMFU can compute six commonly used arithmetic operations in multimedia/DSP processing, i.e., addition, subtraction, multiplication, MAC, interpolation, and Sum-of-Absolute-Difference (SAD). When applying the SPST to these two designs, the realization issues highly differ from each other due

to the large hardware-conFigureuration differences. However, with an elaborate design optimization, the proposed SPST reduces power dissipation by an average of 41.6% and 52.6% for the ETD and the VMFU with 1.8-V supply voltage, respectively. Encapsulating the VMFUs, as shown in Figure. 2.1, designers can increase the flexibility and scalability of multimedia/ DSP processors.

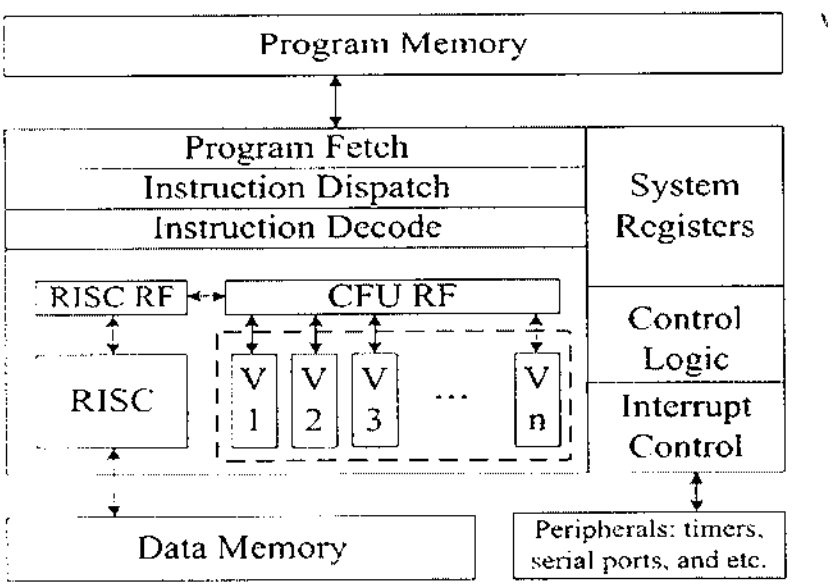

Figure.2.1 Multimedia/DSP processor encapsulating VMFUs

2.3 ANALYSIS OF INPUT DATA FOR H.264 FORWARD TRANSFORM

The data of multimedia/DSP computations, such as transform coding tend to fluctuate within a small range of bit width due to temporal and spatial redundancies existing in video signals. However, the corresponding hardware design still needs to provide the maximum data bit width to avoid data accuracy loss. Figure.2.2 shows the input data pattern (i.e., X00 and X30) of adder/subractor in MPEG-I-0 when executing the H.264 forward transform, as shown in Figure.4.1. From Figure.2.2 it is clear that the data values fall in the range between $+2^6$ and -2^6. This implies that the higher order byte data rarely affect the computational results. This creates an opportunity to minimize the extra power dissipating due to unwanted computations using SPST.

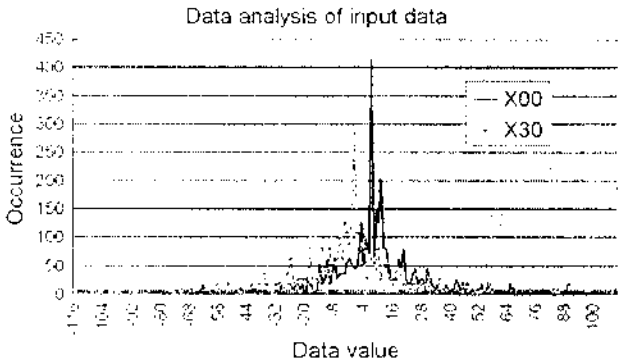

Figure.2.2 Input Data of Efficient Transform Design.

The adders/subtractors in the transform coding design are separated into two parts, i.e., the Most Significant Part (MSP) and the Least Significant Part (LSP), and the input data of the MSP circuits are latched whenever they do not influence the computation results. Besides, detection-logic and SE units are introduced in the proposed SPST to determine the effective ranges of the operands and compensate for the sign signals of the MSP, respectively. Although this concept is similar to the PGC [3], efficiently implementing the concept and manifesting its effects on power saving in real circuits remains challenging. The basic reasons for the occurrence of spurious power are studied and a thorough analysis is made for efficiently implementing SPST adders/subtractors.

CHAPTER 3

DESIGN OF LOW POWER ADDER/SUBTRACTOR USING SPST

3.1 THEORITICAL ANALYSIS AND LOGIC DERIVATION

A 16-bit value is added or subtracted from another 16-bit number. There are chances for the occurrence of unwanted spurious signals. The main objective is to avoid unnecessary transitions to save power. The SPST technique adopts the design concept of separating the arithmetic units into Most Significant Part (MSP) and Least Significant Part (LSP), and then freezing the MSP whenever this part of circuits does not affect the computation result. To illustrate the influence of the spurious signal transitions, five cases of a 16-bit addition are explored as shown in Figure.3.1. The cases of exchanging the operands A and B in additions lead to the same spurious transitions.

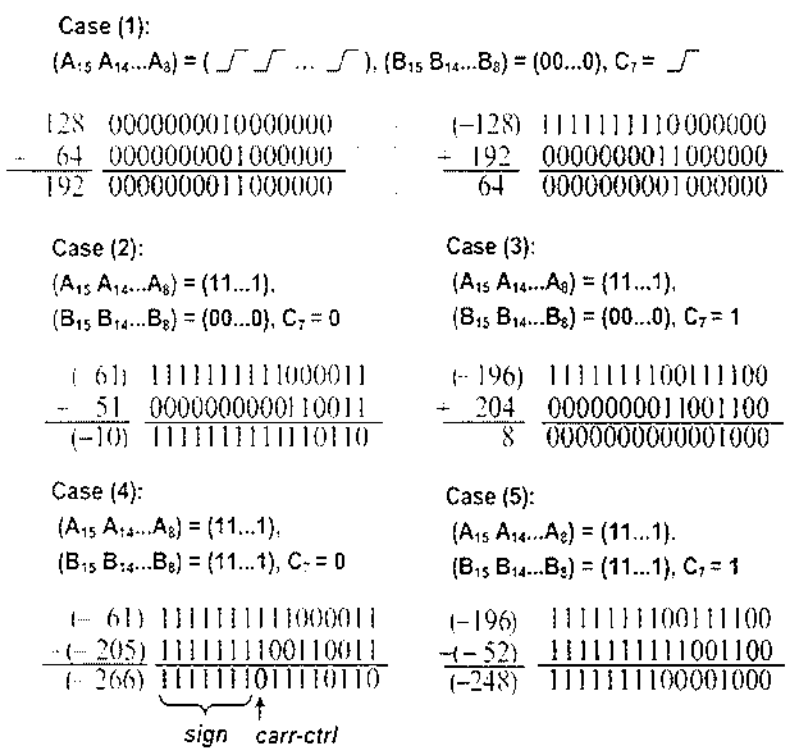

Figure 3.1 Spurious transitions in Multimedia/DSP computations.

The 1st case illustrates a transient state in which the spurious transitions of carry signals occur in the MSP though the final result of the MSP are unchanged. Hence, there is probably no other case beyond these five based on this design. The first case illustrates a transient state in which spurious transitions of carry signals occur in the MSP, although the final result of the MSP is unchanged. Meanwhile, the second and third cases describe situations involving one negative operand adding another positive operand without and with carry-in from the LSP, respectively. Moreover, the fourth and fifth cases demonstrate the addition of two negative operands without and with carry-in from the LSP, respectively. In those cases, the results of MSP are predictable; therefore, the computations in MSP are useless and can be neglected. Eliminating those spurious computations not only can save the power consumption inside the adder/subtractor in the current stage but also can decrease the glitching noises which cause power wastage inside the arithmetic circuits in the next stage. The SPST separates the adder/subtractor into two parts and then latches the input data of the MSP whenever they do not affect the computation results. Therefore the MSP of the original adder/subtractor is modified to include detection logic circuit, data controlling circuits (The data controlling circuits mainly consists of latch A and latch B), sign extension circuit (SE). The SPST can be expanded to be a fine-grain scheme in which the adder/subtractor is divided into more than two parts. However, the hardware complexity of the augmented circuits such as the detection-logic unit, the data latches, and the SE unit increases dramatically. The Boolean logical equations showed as follows express the behavioral principles of the detection-logic unit:

$$A_{MSP} = A[15:8] \quad B_{MSP} = B[15:8] \tag{3.1}$$

$$A_{and} = A[15] \times A[14] \times \cdots \times A[8] \tag{3.2}$$

$$B_{and} = B[15] \times B[14] \times \cdots \times B[8] \tag{3.3}$$

$$A_{nor} = \overline{A[15] + A[14] + \cdots + A[8]} \tag{3.4}$$

$$B_{nor} = \overline{B[15] + B[14] + \cdots + B[8]} \tag{3.5}$$

$$close = \overline{(A_{and} + A_{nor}) \times (B_{and} + B_{nor})} \tag{3.6}$$

Where A[m] and B[n], respectively, denote the m^{th} bit of the operand A and the n^{th} bit of the operand B. A_{MSP} and B_{MSP}, respectively, denote the MSP parts, i.e., the 9th bit to the 16th bit, of the operands A and B in the examples shown in Figure. 3.1. When the bits in A_{MSP} and/or

B_{MSP} are all ones, the value of A_{and} and/or that of B_{and} , respectively, become one, while when the bits in A_{MSP} and/or B_{MSP} are all zeros, the value of A_{nor} and/or that of B_{nor}, respectively, turn into one. Being one of the three outputs of the detection-logic unit, close denotes whether the MSP circuits can be neglected or not. When the two input operands is classified into one of the five cases shown in Figure. 3.1, the value of close becomes zero, which indicates that the MSP circuits can be closed to save power dissipation. This design intends to close the MSP circuits by feeding zero inputs into them, which may freeze the switching activities in the MSP circuits to avoid dynamic power consumption. Accordingly, we derive the Karnaugh maps shown in Figure.3.2 which lead to the Boolean logical equations (3.7) and (3.8). From these equations the necessary circuits for SPST adder/subtractor are designed and implemented.

carr-ctrl		$C_{MSP}, A_{and}, A_{nor}$							
		000	001	011	010	100	101	111	110
B_{and}, B_{nor}	00	0	0	0	0	0	0	0	0
	01	0	0	0	1	0	1	0	0
	11	0	0	0	0	0	0	0	0
	10	0	1	0	0	0	0	0	1

(a)

sign		$C_{MSP}, A_{and}, A_{nor}$							
		000	001	011	010	100	101	111	110
B_{and}, B_{nor}	00	0	0	0	0	0	0	0	0
	01	0	0	0	1	0	0	0	0
	11	0	0	0	0	0	0	0	0
	10	0	1	0	1	0	0	0	1

Figure 3.2 Representation of (a) carr-ctrl signal and (b) sign signal in terms of KARNAUGH maps

3.2 DETECTION LOGIC UNIT

The detection logic unit produces three outputs as close, sign and carr-ctrl, which are given to the asserting circuits to assert the output in the required manner. It makes use of the karnaugh map in order to determine whether the input data should be latched or not. The output signals of the detection logic are obtained by deriving necessary equations from the karnaugh maps. The block diagram of detection logic unit is shown in Figure 3.3.

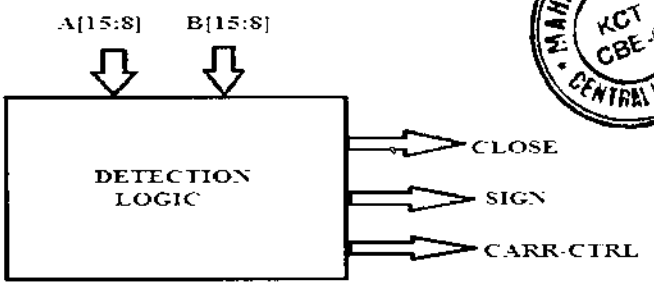

Figure 3.3 Block diagram of detection logic unit

The Boolean logic equations governing the detection logic circuit is derived as follows.

$$\begin{aligned} carr-ctrl &= \overline{C_{LSP}} \times \overline{A_{n[4]}} \times A_{3or} \times B_{n[4]} \times \overline{B_{3or}} \\ &\quad - \overline{C_{LSP}} \times A_{n[4]} \times \overline{A_{3or}} \times \overline{B_{n[4]}} \times B_{3or} \\ &\quad - C_{LSP} \times \overline{A_{n[4]}} \times A_{3or} \times \overline{B_{n[4]}} \times B_{3or} \\ &\quad - C_{LSP} \times A_{n[4]} \times \overline{A_{3or}} \times B_{n[4]} \times \overline{B_{3or}} \\ &= \overline{C_{LSP}} \times (\overline{A_{n[4]}} \times B_{n[4]} - A_{n[4]} \times \overline{B_{n[4]}}) \\ &\quad \times (A_{n[4]} \times B_{n[4]} - A_{n[4]} \times B_{3or} - A_{3or} \times B_{n[4]} \\ &\quad - A_{3or} \times B_{3or}) - C_{LSP} \\ &\quad \times (A_{n[4]} \times B_{n[4]} - \overline{A_{n[4]}} \times \overline{B_{n[4]}}) \\ &\quad \times (A_{n[4]} \times B_{n[4]} - A_{n[4]} \times B_{3or} - A_{3or} \times B_{n[4]} \\ &\quad - A_{3or} \times B_{3or}) (C_{LSP} - A_{n[4]} \oplus B_{n[4]}) \end{aligned} \tag{3.7}$$

$$\begin{aligned} sign &= \overline{C_{LSP}} \times (\overline{A_{n[4]}} \times A_{3or} \times B_{n[4]} \times \overline{B_{3or}} - A_{n[4]} \\ &\quad \times \overline{A_{3or}} \times \overline{B_{n[4]}} \times B_{3or} - A_{n[4]} \times \overline{A_{3or}} \\ &\quad \times B_{n[4]} \times \overline{B_{3or}}) \\ &\quad - C_{LSP} \times A_{n[4]} \times \overline{A_{3or}} \times B_{n[4]} \times \overline{B_{3or}} \\ &= \overline{C_{LSP}} \times (\overline{A_{n[4]}} \times B_{n[4]} - A_{n[4]}) \\ &\quad - C_{LSP} \times A_{n[4]} \times B_{n[4]} \\ &= \overline{C_{LSP}} \times (A_{n[4]} - B_{n[4]}) - C_{LSP} \times A_{n[4]} \times B_{n[4]} \end{aligned} \tag{3.8}$$

3.3 SIGN EXTENSION UNIT

Sign- extension circuits (denoted by SE) shown in Figure.3.4 can be intuitively implemented by multiplexers to compensate the sign signals of the MSP using OR gates. The input data of the sign-extension circuits are pseudo summations (PS) from the MSP adder/subtractors. The SE

circuits can also be implemented with simple OR gates as shown in Figure 3.5 or using complementary pass transistor logics.

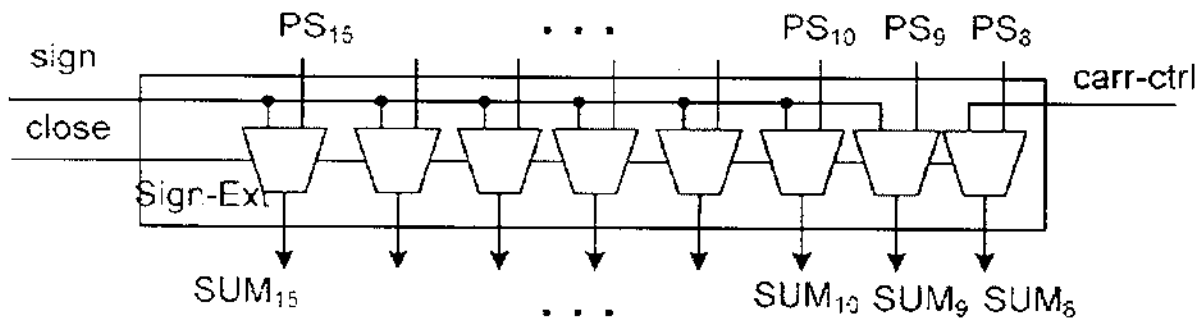

Figure.3.4 Sign Extension circuit using multiplexers.

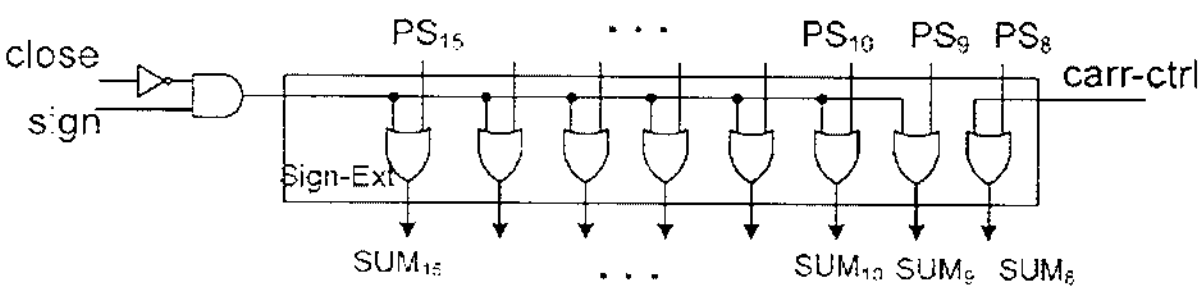

Figure 3.5 Sign extension circuit using simple OR gates.

3.4 DATA LATCH CIRCUIT

Latches implemented with simple AND gates are used to control the input data of the MSP. The detection logic unit of the MSP decides whether the input data of the MSP should be latched or not. Being one of the three outputs of the detection-logic unit, close denotes whether the MSP circuits should be fed or not. When the two input operands belongs to one of the five cases shown in Figure. 3.1, the value of close becomes zero, which indicates that the MSP circuits can be closed to save power dissipation. This design intends to close the MSP circuits by feeding zero inputs into them, which may freeze the switching activities in the MSP circuits to avoid dynamic power consumption.

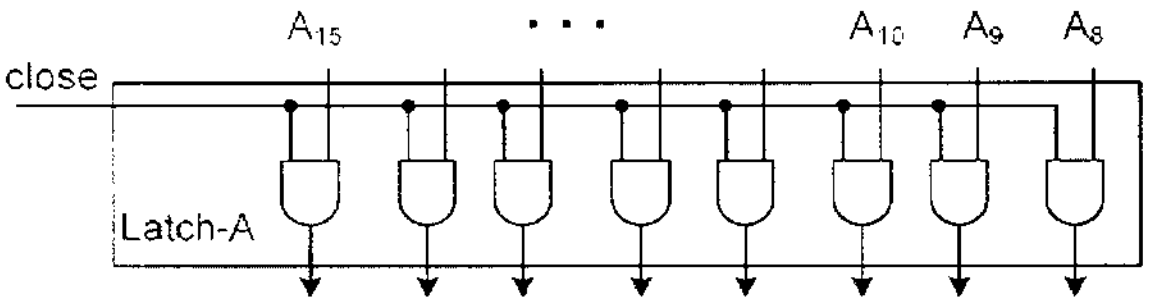

Figure 3.6 Data latch circuit

3.5 REALIZATION ISSUES OF THE PRROPOSED SPST

1) When the detection-logic unit turns off the MSP: At this moment, the outputs of the MSP are directly compensated by the SE unit; therefore, the time saved from skipping the computations in the MSP circuits shall cancel out the delay caused by the detection-logic unit.

2) When the detection-logic unit turns on the MSP: The MSP circuits must wait for the notification of the detection-logic unit to turn on the data latches to let the data in. Hence, the delay caused by the detection-logic unit will contribute to the delay of the whole combinational circuitry, i.e., the 16-bit adder/subtractor in this design example.

3) When the detection-logic unit remains its decision: No matter whether the last decision is turning on or turning off the MSP, the delay of the detection logic is negligible because the path of the combinational circuitry (i.e., the 16-bit adder/subtractor in this design example) remains the same.

3.6 SPST BASED LOW POWER ADDER/SUBTRACTOR

Figure. 3.8 shows a 16-bit adder/subtractor design example adopting the proposed SPST. In this example, the 16-bit adder/subtractor is divided into MSP and LSP between the eighth and the ninth bits. Latches implemented by simple AND gates are used to control the input data of the MSP. When the MSP is necessary, the input data of MSP remain unchanged. However, when the MSP is negligible, the input data of the MSP become zeros to avoid glitching power consumption. The two operands of the MSP enter the detection-logic unit, except the adder/subtractor, so that the detection-logic unit can decide whether to turn off the MSP or not.

Based on the derived Boolean equations (3.1) to (3.8), the detection-logic unit of SPST is shown in Figure. 3.7, which can determine whether the input data of MSP should be latched or not.

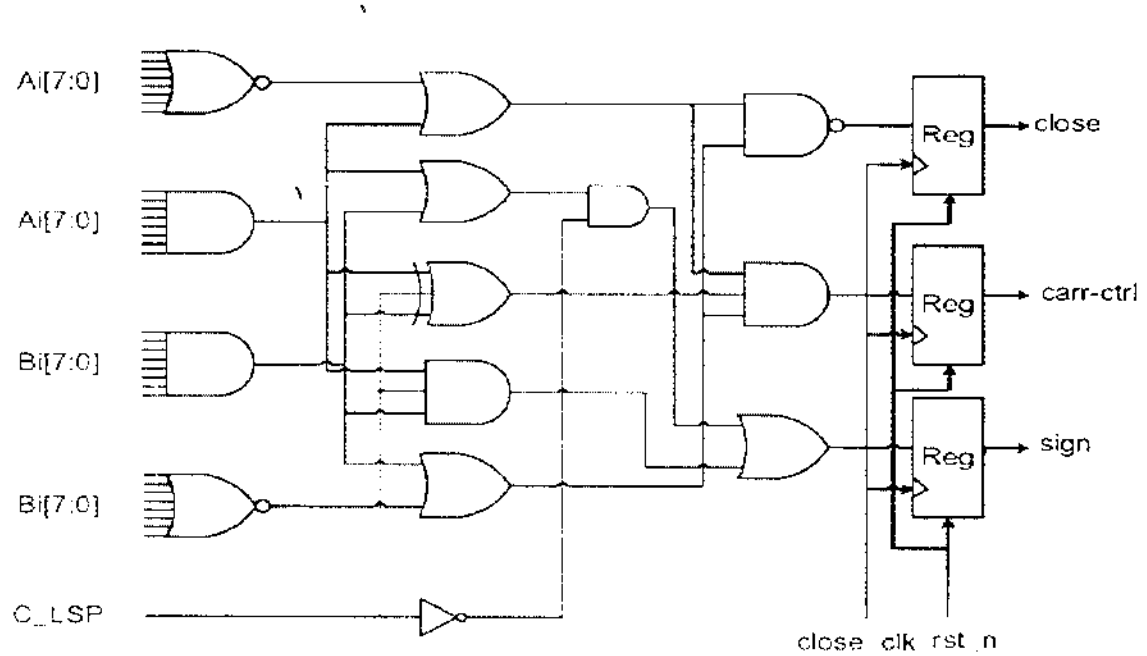

Figure 3.7 Circuit for detection logic unit

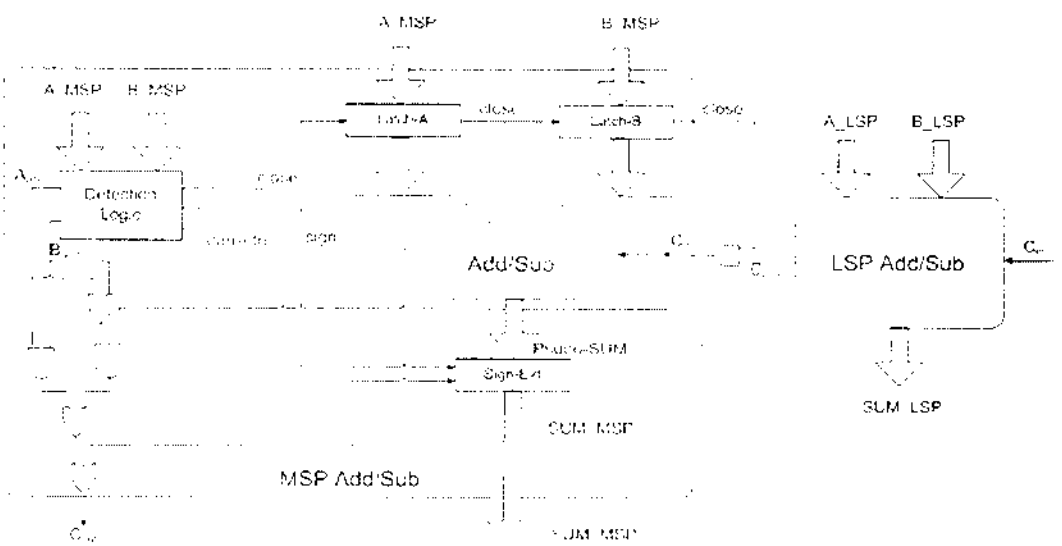

Figure 3.8 Low power adder/subtractor adopting SPST

CHAPTER 4

DESIGN EXAMPLES OF SPST

4.1 SPST BASED MULTI TRANSFOM DESIGN FOR H.264

The first design example using the proposed SPST is the ETD, which is shown in Figure. 4.1. The ETD possesses two types of PEs. From the algorithmic view point, the four PEs in the left-hand side of Figure.4.1, denoted by MPE-Is, are used for computing the 1-D transform. Meanwhile, the two PEs on the right-hand side of Figure.4.1,denoted by MPE-IIs, are used for computing the 2-D transform. The ETD possesses a throughput of eight pixels per cycle so that it can perform 720p HD, 1080i HD, and digital cinema video formats at 22, 50, and 100 MHz, respectively. Based on the previous data analysis, the 15-bit SPST arithmetic units of the MPE-Is is divide into 8-bit MSP and 7-bit LSP and the 17-bit SPST arithmetic units of the MPE-IIs is divided into 8-bit MSP and 9 bit LSP, respectively, as shown in the fraction values near the SPST arithmetic units in Figure. 4.1 where the SPST arithmetic units are marked with dotted shadows. The adder/subtractors located on the second and the fourth stages of the ETD are kept unchanged because most of the spurious signals existed in the data flowing out of the first and the third stages have been filtered out by the SPST. Therefore, it is useless to replace these adder/subtractors located on the second and the fourth stages with the SPST ones.

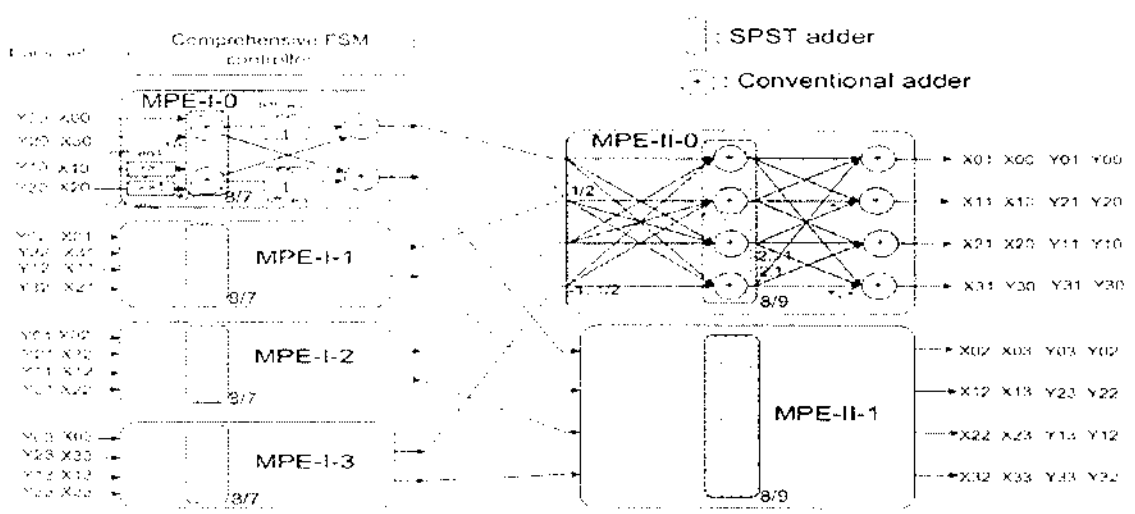

Figure 4.1 ETD for H.264 based on SPST

4.2 VERSATILE MULTIMEDIA FUNCTIONAL UNIT

The second design example using the proposed SPST is the VMFU, which is constructed on the basis of a modified Booth encoding multiplier. The proposed VMFU can compute six kinds of arithmetic operations, i.e., addition, subtraction, multiplication, MAC, interpolation, and SAD, which are frequently used in multimedia/DSP computations.

4.2.1 SUM OF ABSOLUTE DIFFERENCE

Sum of Absolute Differences (SAD) is a widely used, extremely simple video quality metric used for block-matching in motion estimation for video compression. It works by taking the absolute value of the difference between each pixel in the original block and the corresponding pixel in the block being used for comparison. These differences are summed to create a simple metric of block. The circuit implemented for SAD is shown in Figure 4.2.

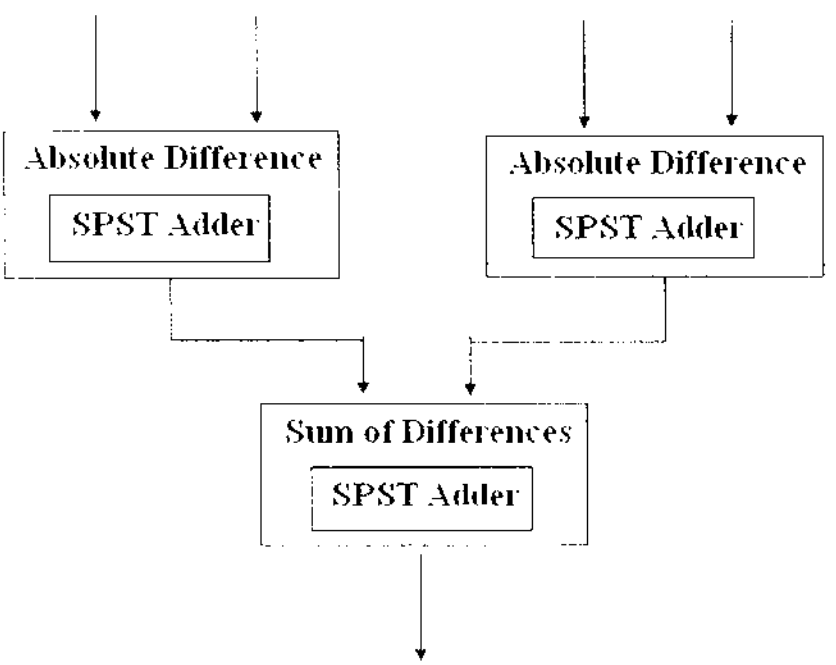

Figure 4.2 Block diagram for SAD circuit implemented in VMFU

4.2.2 MULTIPLY ACCUMULATE UNIT

Multiply-accumulate is a common operation that computes the product of two numbers and adds that product to an accumulator. A dedicated multiply-accumulate unit, or MAC unit,

consists of a multiplier implemented in combinational logic followed by an adder and an accumulator register which stores the result when clocked. Here SPST adder is used instead of conventional adder as shown in the Figure.4.3. The output of the register is fed back to one input of the adder, so that on each clock the output of the multiplier is added to the register. Combinational multipliers require a large amount of logic, but can compute a product much more quickly than the method of shifting and adding typical of earlier computers.

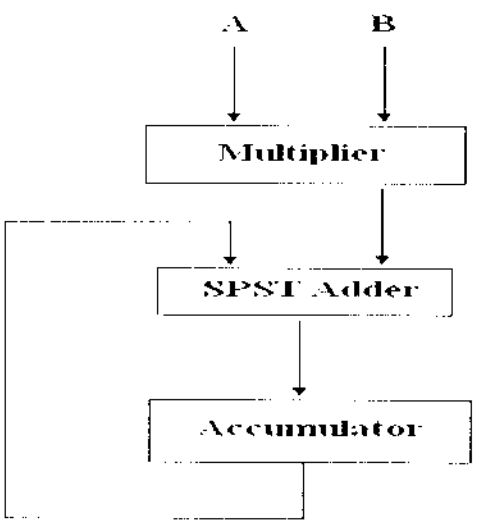

Figure 4.3 Block diagram of MAC using SPST

4.2.3 INTERPOLATION

The process of interpolation is one of the fundamental operations in image processing. The image quality highly depends on the used interpolation technique. Interpolation is the process of determining the values of a function at positions lying between its samples. It achieves this process by fitting a continuous function through the discrete input samples. This permits input values to be evaluated at arbitrary positions in the input, not just those defined at the sample points. While sampling generates an infinite bandwidth signal from one that is band limited, interpolation plays an opposite role: it reduces the bandwidth of signal by applying a low-pass filter to the discrete signal. That is, interpolation reconstructs the signal lost in the sampling process by smoothing the data samples with an interpolation function. The interpolation circuit implemented in VMFU is shown in Figure 4.4.

Common interpolation algorithms can be grouped into two categories: adaptive and non-adaptive. Adaptive methods change depending on what they are interpolating (sharp edges vs smooth texture), whereas non-adaptive methods treat all pixels equally.

The interpolation techniques can also be classified as deterministic and statistical interpolation techniques. The difference is that deterministic interpolation techniques assume certain variability between the sample points, such as linearity in case of linear interpolation. Statistical interpolation methods approximate the signal by minimizing the estimation error. This approximation process may result in original sample values not being replicated.

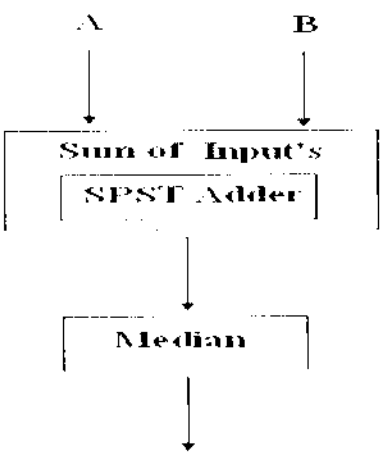

Figure 4.4 Block diagram for Interpolation circuit implemented in VMFU

4.3 LOW POWER SPST EQUIPPED VMFU

There are three distinguishing design considerations in designing the VMFU are listed.

```
2AC9      0010101011001001
006A x)   0000000001101010
          +0 +0 +0 +0 +2 -1 -1 -2
          1101010100110110    PP0
          1110101010011011    PP1
          1110101010011011    PP2
          0010101011001001    PP3
          0000000000000000    PP4
          0000000000000000    PP5
          0000000000000000    PP6
+)        0000000000000000    PP7
00000000000100011011011100111010(11B73A)
```

Figure 4.5 Illustration of multiplication using modified Booth encoding.

1) Applying the SPST to the Modified Booth Encoder: Figure. 4.5 shows a computation example of Booth multiplying two numbers "$2AC9_{hex}$" and "$006A_{hex}$," where the shadow denotes that the numbers in this part of Booth multiplication are all zeros so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals.

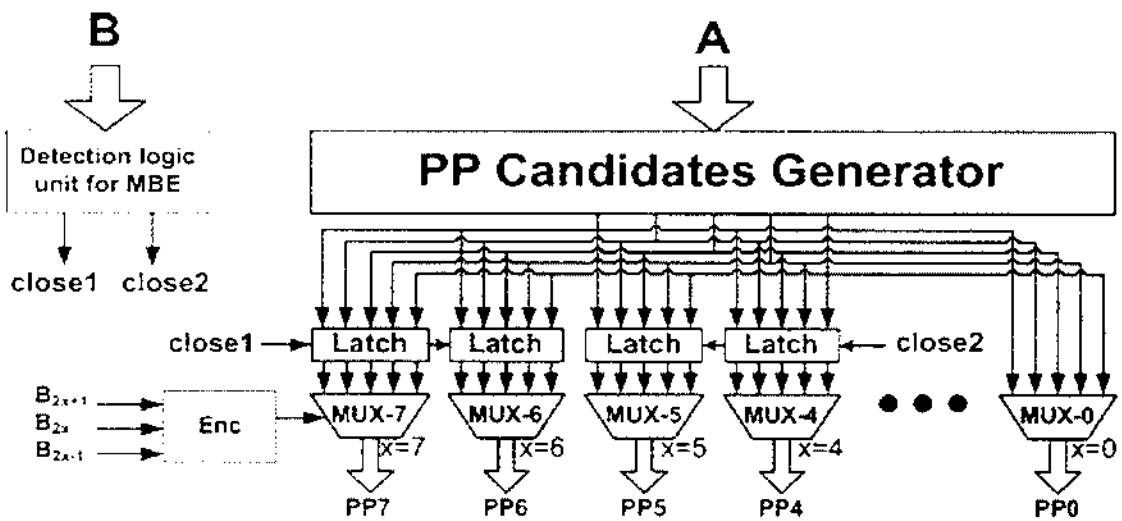

Figure 4.6 SPST modified Booth encoder.

According to the analysis of the multiplication shown in Figure. 4.5, the SPST modified Booth encoder is designed which includes a detection unit, as shown in Figure. 4.6. From one of the two operands, e.g., the operand A, the partial product (PP) candidate generator generates five candidates of the partial products, i.e., {-2A,-A, 0, A, 2A}, which are then selected according to the Booth encoding results of the other operand, i.e., the operand B. Meanwhile, the detection unit has the second one of the two operands, i.e., the operand B in this case, as its input to decide whether the Booth encoder includes redundant computations. As shown in Figure. 4.6, the latches can, respectively, freeze the inputs of MUX-4 to MUX-7 or only those of MUX-6 to MUX-7 when the PP4 to PP7 or only the PP6 to PP7 are zeros to reduce the transition power dissipation. Such cases occur frequently in wireless multimedia-data coding like texture coding, orthogonal frequency-division multiplexing, and filter designs.

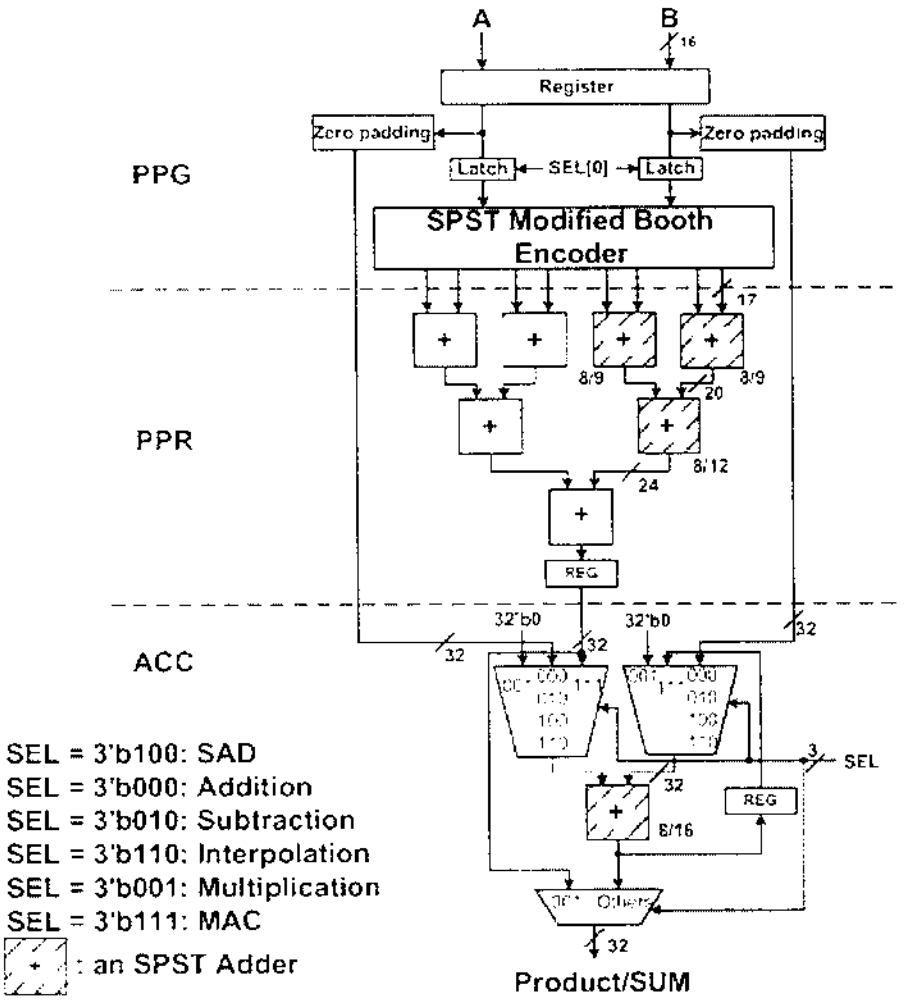

Figure 4.7 Proposed low-power SPST-equipped VMFU

2) Applying the SPST to the Compression Tree: Figure. 4.7 shows the architecture diagram for the proposed VMFU in which the SPST modified Booth encoder has been shown in Figure.4.6. The VMFU can be roughly decomposed into three sections, i.e., the Partial Product Generation, the Partial Product Reduction (PPR), and the Accumulation (ACC) sections. When the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree in the PPR section. According to the analysis of the addition shown in Figures. 3.1 and 4.5, some of the adders in the compression tree of the VMFU which add up the PP0

to PP3, with the SPST-equipped adders. Besides, the adder in the ACC section is also replaced with the SPST-equipped adder. This adder is used to accumulate the multiplication results in the MAC operation and compute the interpolation, SAD, addition, and subtraction. These adders are marked with oblique lines as shown in Figure. 4.7 with their bit widths of the MSP and LSP indicated, respectively, in the numerator and the denominator of the nearing fraction values.

3) Freezing the Switching Activities of the Unused Circuits: The data flows of the VMFU are controlled by the properly arranged multiplexers. By freezing the unused circuits in response to the selection of a certain kind of functionality, wasteful switching power dissipation can be avoided, as shown in Figure. 4.7. Besides, the circuits induced by the SPST can be frozen to turn off the SPST function of the VMFU. This option may be useful when the input data do not possess advantageous features like the multimedia data because the SPST may not contribute positive power saving when both the input data are random.

CHAPTER 5

IMPLEMENTATION AND SOFTWARE TOOLS

5.1 SOFTWARE TOOLS

In this chapter the software tools that have been used for implementing SPST based adder/subtractor, SPST based VMFU and SPST based ETD are discussed. The following software tools are used for implementing the project.

1. Modelsim 6.2c
2. Xilinx 9.1

5.1.1 MODELSIM 6.2C

Modelsim 6.2c provides a comprehensive simulation and debug environment for complex ASIC and FPGA designs. It supports multiple languages including Verilog, System Verilog, VHDL snd SystemC. Here the design is coded in VHDL usng Modelsim6.2c and each module is synthesized in Xilinx and the results are obtained.

5.1.2 XILINX 9.1

It is a synthesis tool that supports HDL languages, Xilinx 9.1 devices. It can be used to create, define, and compile your FPGA or CPLD design using the suite of ISE tools available from the project navigator. The codes simulated in modelsim6.2c are synthesized and implemented using this software.

5.2 LANGUAGE USED

VHDL is the main source or the language used to implement the project. In the mid-1980's the U.S. Department of Defense and the IEEE sponsored the development of this hardware description language with the goal to develop very high-speed integrated circuit. It has become now one of industry's standard languages used to describe digital systems.The other

widely used hardware description language is Verilog. Both are powerful languages that allow describing and simulating complex digital systems. A third HDL language is ABEL (Advanced Boolean Equation Language) which was specifically designed for Programmable Logic Devices (PLD). ABEL is less powerful than the other two languages and is less popular in industry. This proposed work deals with VHDL, as described by the IEEE standard.A HDL program mimics the behavior of a physical, usually digital, system. It also allows incorporation of timing specifications (gate delays) as well as to describe a system as an interconnection of different components.

VHDL allows one to describe a digital system at the structural or the behavioral level. The behavioral level can be further divided into two kinds of styles: Data flow and Algorithmic.

CHAPTER 6

RESULTS AND DISCUSSIONS

6.1 SIMULATION RESULT OF DETECTION LOGIC

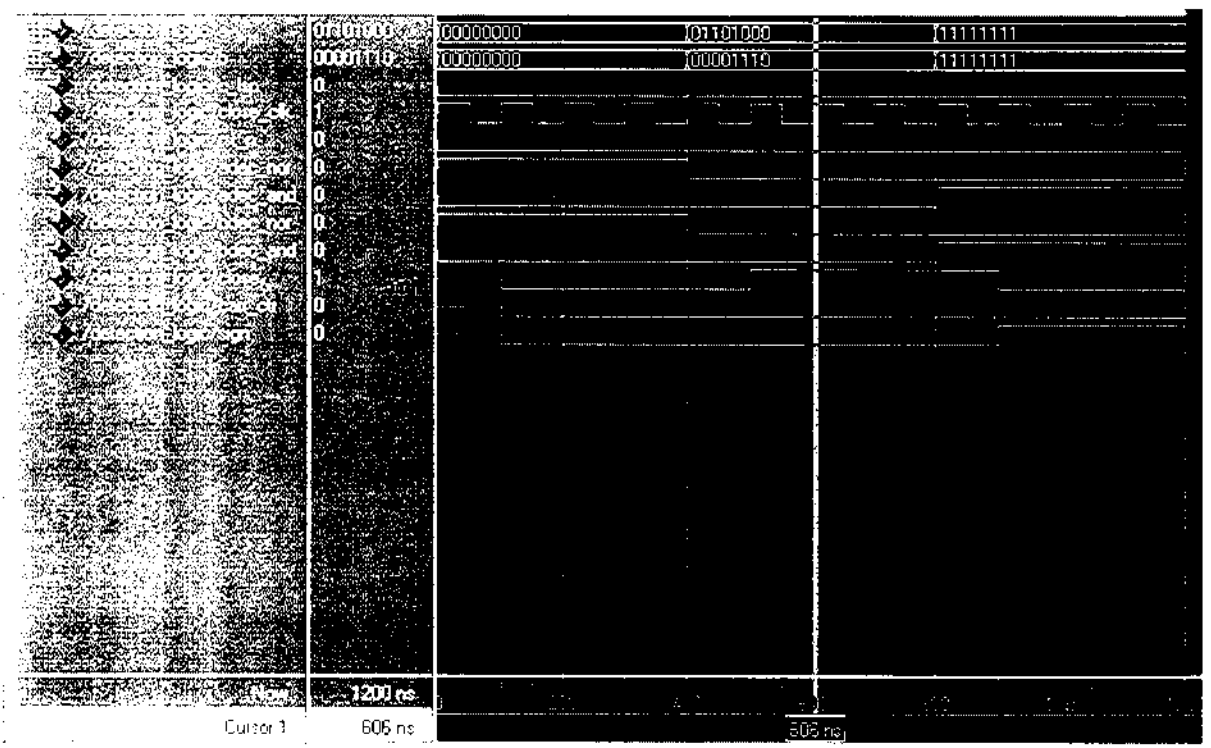

Figure 6.1 Simulated result of Detection logic

6.2 SIMULATION RESULT OF SPST BASED 16- BIT ADDER/SUBTRACTOR

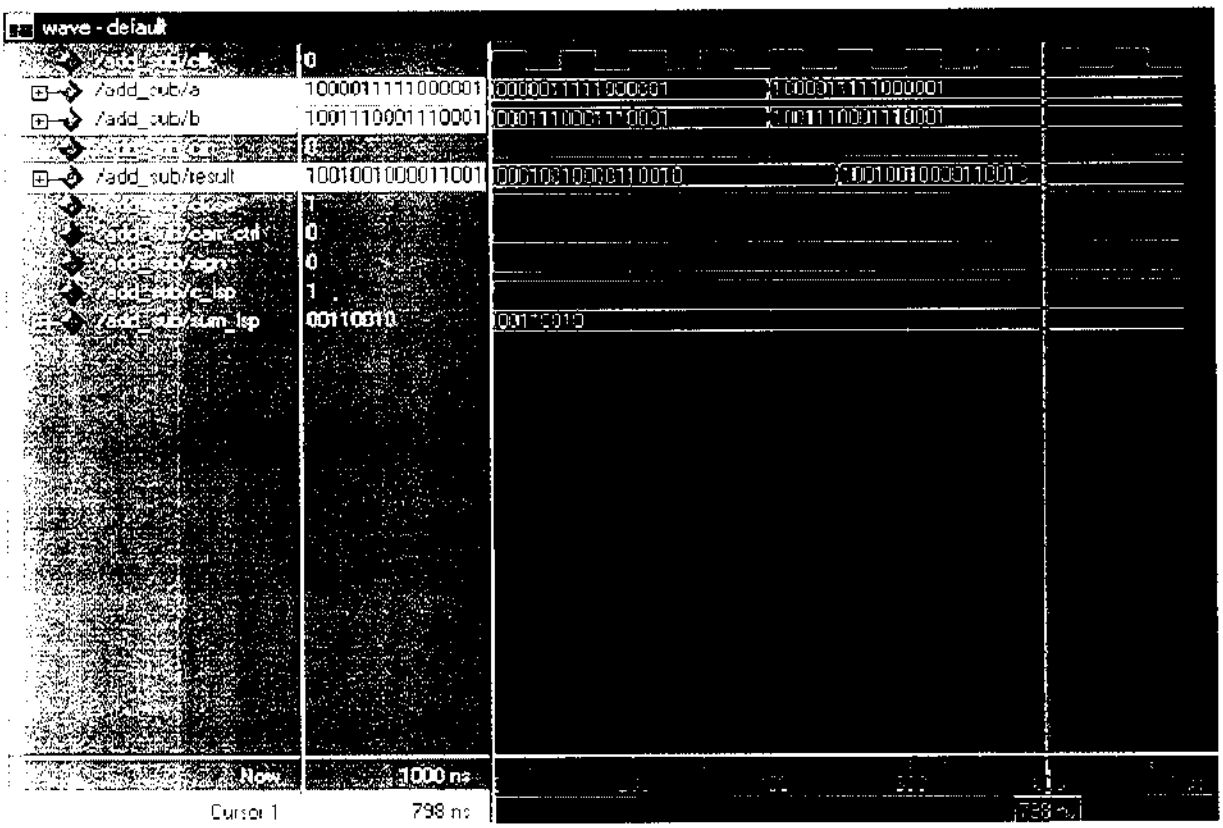

Figure 6.2 Simulated result of SPST adder/subtractor

6.3 POWER ANALYSIS REPORT OF CONVENTIONAL ADDER/SUBTRACTOR

Table.6.1 Power analysis report for conventional adder/subtractor

Power summary:	**I(mA)**	**P(mW)**
Total estimated power consumption:		**73**
Vccint 1.80V:	**19**	**34**
Vcco33 3.30V:	**2**	**7**
Inputs:	**1**	**2**
Logic:	**3**	**5**
Outputs:		
Vcco33	**0**	**0**
Signals:	**0**	**0**
Quiescent Vccint 1.80V:	**15**	**27**
Quiescent Vcco33 3.30V:	**2**	**7**

DEVICE UTILIZATION SUMMARY

Logic Utilization:

Number of Slice Flip Flops:	31 out of 13,824	1%
Number of 4 input LUTs:	64 out of 13,824	1%

Logic Distribution:

Number of occupied Slices:	32 out of 6,912	1%
Number of Slices containing only related logic:	32 out of 32	100%
Number of Slices containing unrelated logic:	0 out of 32	0%
Total Number of 4 input LUTs:	64 out of 13,824	1%
Number of bonded IOBs:	98 out of 510	19%

IOB Flip Flops:	33	
Number of GCLKs:	1 out of 4	25%
Number of GCLKIOBs:	1 out of 4	25%
Total equivalent gate count for design:	859	

6.4 POWER ANALYSIS REPORT OF SPST BASED ADDER AND SUBTRACTOR

Table.6.2 Power analysis report for SPST based adder/subtractor

Power summary:	**I(mA)**	**P(mW)**
Total estimated power consumption:		**41**
Vccint 1.80V:	**19**	**34**
Vcco33 3.30V:	**2**	**7**
Inputs:	**1**	**2**
Logic:	**3**	**5**
Outputs:		
Vcco33	**0**	**0**
Signals:	**0**	**0**
Quiescent Vccint 1.80V:	**15**	**27**
Quiescent Vcco33 3.30V:	**2**	**7**

DEVICE UTILISATION SUMMARY

Logic Utilization:		
Number of 4 input LUTs:	106 out of 13,824	1%
Logic Distribution:		
Number of occupied Slices:	62 out of 6,912	1%
Number of Slices containing only related logic:	62 out of 62	100%
Number of Slices containing unrelated logic:	0 out of 62	0%
Total Number of 4 input LUTs:	106 out of 13,824	1%

Number of bonded IOBs:	98 out of	510	19%
IOB Flip Flops:	33		
Number of GCLKs:	1 out of	4	25%
Number of GCLKIOBs:	1 out of	4	25%
Total equivalent gate count for design:	903		

From the power analysis report of SPST adder/ subtractor and conventional adder it is found that SPST based adder/subtractor unit saves 43% of power compared to conventional adder/subtractor unit with just an increase in area of about 5%.

6.5 SIMULATION RESULT OF ETD WITH SPST

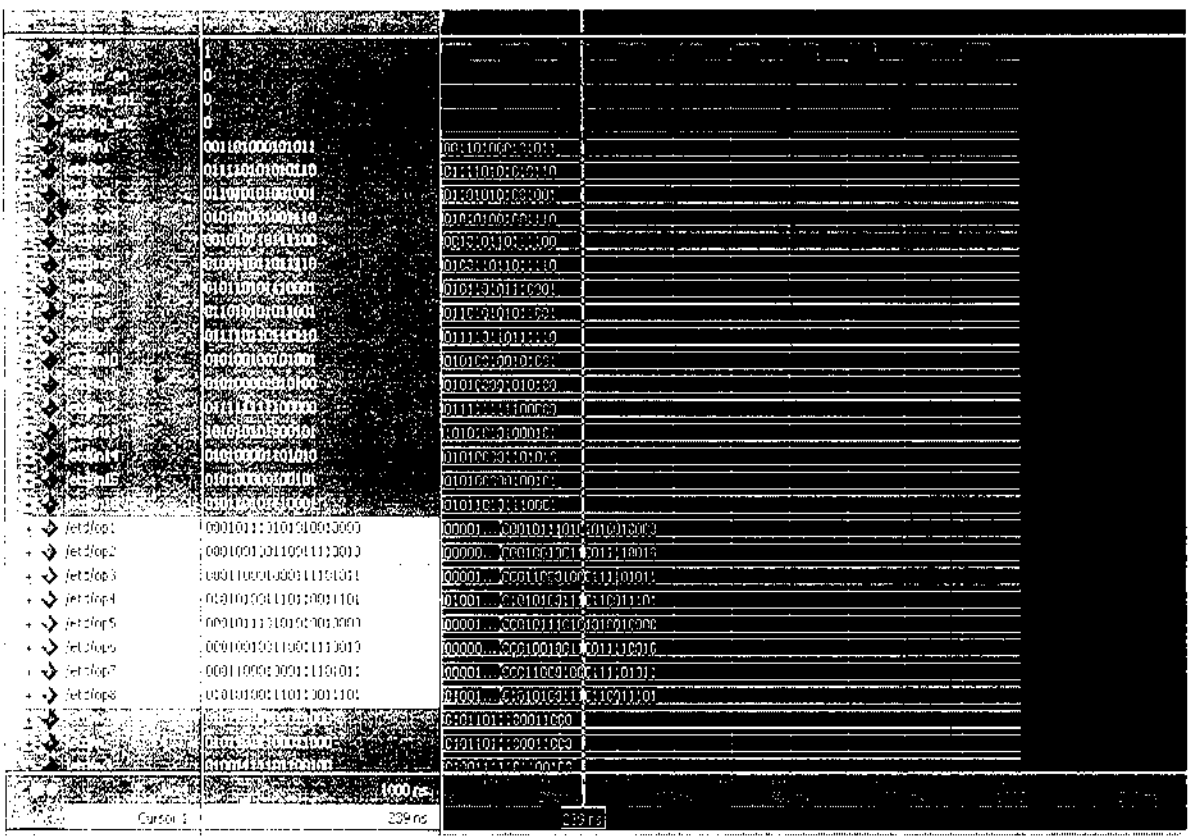

Figure 6.3 Simulated result of ETD without SPST.

6.6 POWER ANALYSIS REPORT OF ETD WITHOUT SPST

Table.6.3 Power Analysis report of ETD without SPST.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		**162**
Vccint 1.80V:	**86**	**155**
Vcco33 3.30V:	**2**	**7**
Clocks:	**71**	**127**
Inputs:	**1**	**2**
Logic:	**0**	**0**
Outputs:		
Vcco33	**0**	**0**
Signals:	**0**	**0**
Quiescent Vccint 1.80V:	**15**	**27**
Quiescent Vcco33 3.30V:	**2**	**7**

DEVICE UTILIZATION SUMMARY

Logic Utilization:		
Number of Slice Flip Flops:	146 out of 13,824	1%
Number of 4 input LUTs:	2,943 out of 13,824	21%
Logic Distribution:		
Number of occupied Slices:	1,528 out of 6,912	22%
Number of Slices containing only related logic:	1,528 out of 1,528	100%
Number of Slices containing unrelated logic:	0 out of 1,528	0%
Total Number 4 input LUTs:	2,979 out of 13,824	21%
Number used as logic:	2,943	

Number used as a route-thru:	36	
Number of bonded IOBs:	411 out of 510	80%
IOB Flip Flops:	16	
Number of GCLKs:	1 out of 4	25%
Number of GCLKIOBs:	1 out of 4	25%
Total equivalent gate count for design:	20758	

6.7 POWER ANALYSIS REPORT OF ETD WITH SPST

Table.6.4 Power Analysis report of ETD with SPST

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		**95**
Vccint 1.80V:	**31**	**55**
Vcco33 3.30V:	**2**	**7**
Clocks:	**15**	**27**
Inputs:	**1**	**2**
Logic:	**0**	**0**
Outputs:		
Vcco33	**0**	**0**
Signals:	**0**	**0**
Quiescent Vccint 1.80V:	**15**	**27**
Quiescent Vcco33 3.30V:	**2**	**7**

DEVICE UTILIZATION SUMMARY

Logic Utilization:		
Number of Slice Flip Flops:	1,234 out of 13,824	8%
Number of 4 input LUTs:	1,554 out of 13,824	11%
Logic Distribution:		
Number of occupied Slices:	784 out of 6,912	11%
Number of Slices containing only related logic:	784 out of 784	100%
Number of Slices containing unrelated logic:	0 out of 784	0%
Total Number of 4 input LUTs:	1,554 out of 13,824	11%
Number of bonded IOBs:	409 out of 510	80%
IOB Flip Flops:	168	

Number of GCLKs:	1 out of	4	25%
Number of GCLKIOBs:	1 out of	4	25%
Total equivalent gate count for design:	22540		

From the power analysis reports of Efficient Transform Design (ETD) it is found that SPST based ETD unit saves 41.6% of power compared to conventional ETD unit with just an increase in area of about 7.9%.

6.8 SIMULATION REPORT OF SPST EQUIPPED VMFU

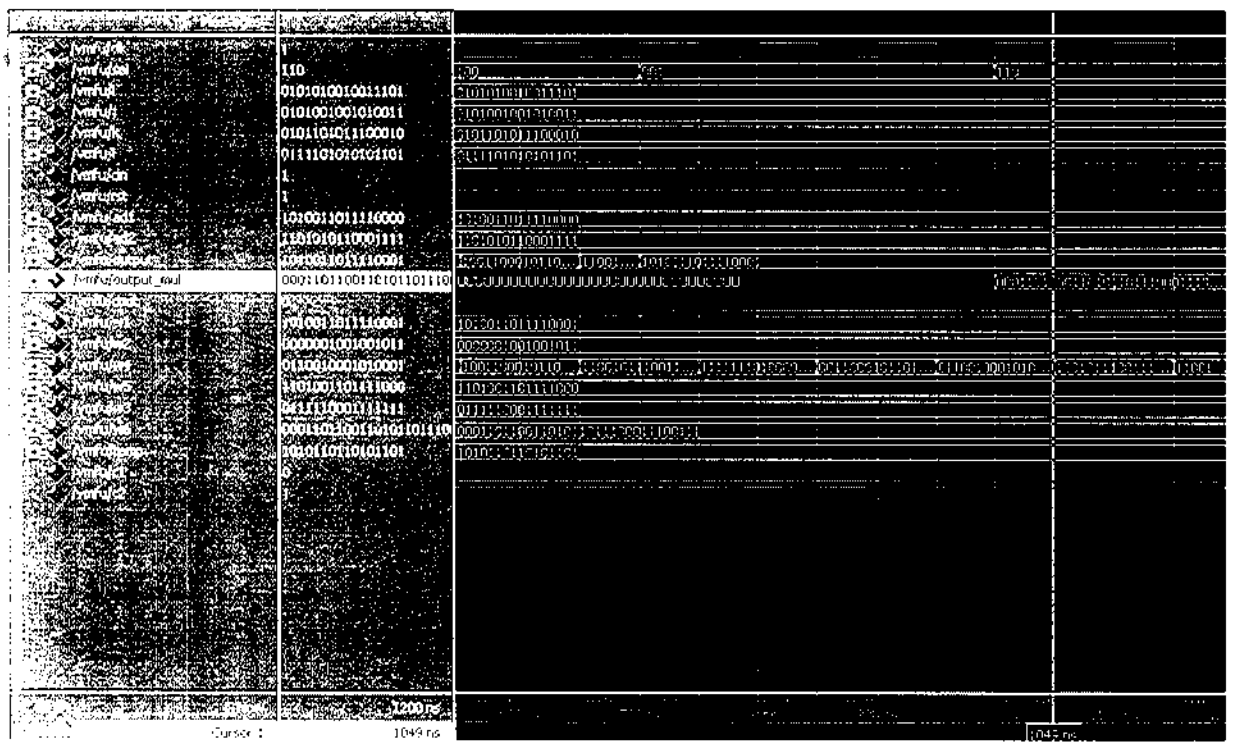

Figure 6.4 Simulation report of SPST equipped VMFU.

6.9 POWER ANALYSIS REPORT OF VMFU WITHOUT SPST

Table.6.5 Power analysis report of VMFU without SPST

Power summary:	**I(mA)**	**P(mW)**
Total estimated power consumption:		**112**
Vccint 1.80V:	**58**	**105**
Vcco33 3.30V:	**2**	**7**
Clocks:	**42**	**76**
Inputs:	**1**	**2**
Logic:	**0**	**0**
Outputs:		
Vcco33	**0**	**0**
Signals:	**0**	**0**
Quiescent Vccint 1.80V:	**15**	**27**
Quiescent Vcco33 3.30V:	**2**	**7**

DEVICE UTILIZATION SUMMARY

Logic Utilization:

Number of 4 input LUTs:	626 out of 13,824	4%

Logic Distribution:

Number of occupied Slices:	343 out of 6,912	4%
Number of Slices containing only related logic:	343 out of 343	100%
Number of Slices containing unrelated logic:	0 out of 343	0%
Total Number 4 input LUTs:	627 out of 13,824	4%
Number used as logic:	626	

Number used as a route-thru:	1		
Number of bonded IOBs:	64 out of	510	12%
IOB Flip Flops:	32		
Number of GCLKs:	1 out of	4	25%
Number of GCLKIOBs:	1 out of	4	25%
Total equivalent gate count for design:	9251		

6.10 POWER ANALYSIS REPORT OF VMFU WITH SPST

Table.6.6 Power analysis report of VMFU with SPST

Power summary:	**I(mA)**	**P(mW)**
Total estimated power consumption:		**53**
Vccint 1.80V:	**19**	**34**
Vcco33 3.30V:	**2**	**7**
Inputs:	**1**	**2**
Logic:	**3**	**5**
Outputs:		
Vcco33	**0**	**0**
Signals:	**0**	**0**
Quiescent Vccint 1.80V:	**15**	**27**
Quiescent Vcco33 3.30V:	**2**	**7**

DEVICE UTILIZATION SUMMARY

Logic Utilization:		
Number of Slice Flip Flops:	556 out of 13,824	4%
Number of 4 input LUTs:	841 out of 13,824	6%
Logic Distribution:		
Number of occupied Slices:	615 out of 6,912	8%
Number of Slices containing only related logic:	615 out of 615	100%
Number of Slices containing unrelated logic:	0 out of 615	0%
Total Number 4 input LUTs:	857 out of 13,824	6%
Number used as logic:	841	
Number used as a route-thru:	16	

Number of bonded IOBs:	64 out of 510	12%
IOB Flip Flops:	48	
Number of GCLKs:	1 out of 4	25%
Number of GCLKIOBs:	1 out of 4	25%
Total equivalent gate count for design:	10118	

From the power analysis reports of SPST equipped VMFU it is found that SPST based unit saves 52.6% of power compared to conventional VMFU unit with just an increase in area of about 8.4%.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

Thus an efficient Spurious Power Suppression Technique (SPST) and its applications on transform coding design for H.264 and Versatile Multimedia Functional Unit (VMFU) is implemented. Using the proposed SPST technique, the spurious power occurred in the H.264 transform coding got reduced. The simulations illustrate that the proposed SPST technique can save 47% power consumption on an average. The simulation results show that turning on the SPST function can save 41.6% power dissipations with a slight increase in area of about 8.4% when operated at 100MHz with 1.8V supply voltage. This indicates that the proposed SPST technique effectively reduces the power dissipation in the transform coding designs for H.264, which facilitates video coding applications on portable electrical devices. The SPST is further applied on the Versatile Multimedia Functional Unit (VMFU) which resulted in power reduction of about 52.6% with just a slight increase in area of about 8.4% when operated at 100MHz.

7.2 FUTURE SCOPE

The SPST can be expanded to a fine-grain scheme in which the adder/subtractor is divided into more than two parts. However, the hardware complexity of the augmented circuits such as the detection-logic unit, the data latches, and the SE unit may increase dramatically. Based on an adder/subtractor example, it is found that the area expense caused by the augmented circuits is very less than the power reduction in bipartitioned scheme. This may not be true in case of tripartitioned scheme. By thoroughly analyzing the tripartitioned scheme, it may also be possible to implement SPST in many other multimedia/DSP applications.

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APPENDIX

Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information

DS077-1 (v1.0) November 15, 2001

Preliminary Product Specification

Introduction

The Spartan™-IIE 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The five-member family offers densities ranging from 50,000 to 300,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Spartan-IIE devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (to 64K bits), distributed RAM (to 98,304 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 6,912 logic cells with up to 300,000 system gates
  - Streamlined features based on Virtex-E architecture
  - Unlimited in-system reprogrammability
  - Very low cost
- System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Low cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards, including LVDS and LVPECL
  - Up to 120 differential I/O pairs that can be input, output, or bidirectional
  - Zero hold time simplifies system timing
- Fully supported by powerful Xilinx ISE development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	84	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	263	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. The Xilinx XC17S00A PROM family is recommended for serial configuration of Spartan-IIE FPGAs. The XC18V00 reprogrammable PROM family is recommended for parallel or serial configuration.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. Spartan-IIE FPGAs offer the most cost-effective solution while maintaining leading edge performance. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with 100Ω external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

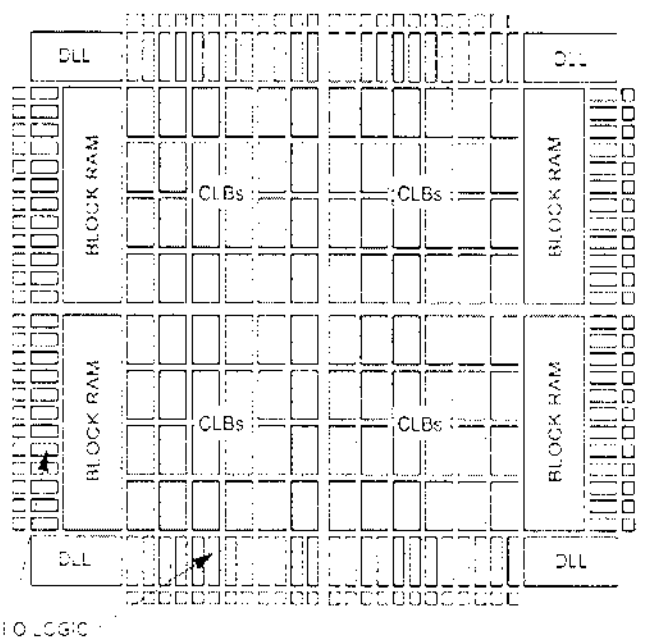


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

Spartan-IIE Product Availability

Table 2 shows the package and speed grades available for Spartan-IIE family devices. Table 3 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE Package and Speed Grade Availability**

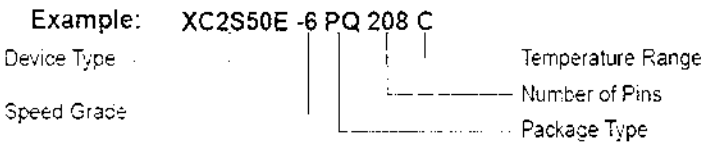
	Pins	144	208	256	456
	Type	Plastic TQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA
Device	Code	TQ144	PQ208	FT256	FG456
XC2S50E	-6	C, I	C, I	C, I	-
	-7	(C)	(C)	(C)	-
XC2S100E	-6	C, I	C, I	C, I	C, I
	-7	(C)	(C)	(C)	(C)
XC2S150E	-6	-	(C, I)	(C, I)	(C, I)
	-7	-	(C)	(C)	(C)
XC2S200E	-6	-	C, I	C, I	C, I
	-7	-	(C)	(C)	(C)
XC2S300E	-6	-	C, I	C, I	C, I
	-7	-	(C)	(C)	(C)

Notes:
1. C = Commercial, T_J = 0 to +85 C; I = Industrial, T_J = –40 C to +100 C
2. Parentheses indicate product not yet released. Contact sales for availability.

Table 3: **Spartan-IIE User I/O Chart**

		Available User I/O According to Package Type			
Device	Maximum User I/O	TQ144	PQ208	FT256	FG456
XC2S50E	182	102	146	182	-
XC2S100E	202	102	146	182	202
XC2S150E	263	-	146	182	263
XC2S200E	289	-	146	182	289
XC2S300E	329	-	146	182	329

Ordering Information



Device Ordering Options

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XC2S50E	-6	Standard Performance	TQ144	144-pin Plastic Thin QFP	C = Commercial	0°C to +85°C
XC2S100E	-7	Higher Performance	PQ208	208-pin Plastic QFP	I = Industrial	–40°C to +100°C
XC2S150E			FT256	256-ball Fine Pitch BGA		
XC2S200E			FG456	456-ball Fine Pitch BGA		
XC2S300E						

Revision History

Version No.	Date	Description
1.0	11/15/01	Initial Xilinx release

The Spartan-IIE Family Data Sheet

DS077-1 *Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information* (Module 1)

DS077-2 *Spartan-IIE 1.8V FPGA Family: Functional Description* (Module 2)

DS077-3 *Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics* (Module 3)

DS077-4 *Spartan-IIE 1.8V FPGA Family: Pinout Tables* (Module 4)