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PERFORMANCE ANALYSIS OF

HIGH PERFORMANCE FULL ADDER CELL

By

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BONAFIDE CERTIFICATE

Certified that this project report entitled "**PERFORMANCE ANALYSIS OF HIGH PERFORMANCE FULL ADDER CELL**" is the bonafide work of **Ms.K.P.Keerthana [Reg. no. 1020106010]** who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ABSTRACT

Full adder is an essential component for the design and development of all types of processors like digital signal processors (DSP), microprocessors etc. Adders are the core element of complex arithmetic operations like addition, multiplication, exponentiation, division etc. In most of these systems adder lies in the critical path that affects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is a significant goal. The present study analysis energy efficient full adder cell with least MOS transistor count that reduces the serious problem of threshold loss. The contribution of this project are 45% improvement in threshold loss problem, 40% improvement in power delay product over the other types of adders with comparable performance and considerably increases the speed and reduces the area. The simulation has been carried out on Microwind 3.1.using 90nm technology.

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LIST OF ABBREVIATIONS

VLSI	-------	Very Long Scale Integration
T	-------	Transistors
CMOS	-------	Complementary metal–oxide–semiconductor
XOR	-------	Exclusive OR Gate
XNOR	-------	Inverse of the Exclusive OR
MOSFET	-------	Metal-Oxide-Semiconductor Field-Effect Transistor
PMOS	-------	P-Channel MOSFET
PDP	-------	Power Delay Product
ASIC	-------	Application Specific Integrated Circuits
NMOS	-------	N-Channel MOSFET
V_{dd}	-------	The Label of an IC Power Supply Pin
SERF	-------	Static Energy-Recovery Full-Adder
NAND	-------	Not AND
NOR	-------	Not OR
RAM	-------	Random Access Memory

CHAPTER 1

INTRODUCTION

Ever since its inception, the design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement. It is being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed. The full adder performance would affect the system as a whole. Full adder transistor based model is one of the important components that are used in all kinds of processors. There are no of processors used in digital systems. To meet the growing demand, we propose a new high speed, energy efficient adder circuit using 8 transistors (least number of transistors) that yielded very encouraging results so to say, the best in speed, power, and power delay product. So a comparative study is made so as to conclude that the 8 transistor model is the superior than the previous model, when the design aspects are the above mentioned aspects. The process has been carried by the Microwind 3.1 using 90nm technology.

1.1 MOTIVATION

Full adders an essential component for the design of the all type of processors. So to design a full adder as a main component, a least count transistor is designed for the basic need of low area, power dissipation, delay and power delay product as a main design aspect ratio. Several other adders like 16T, 14T, 10T are compared and the superiority of 8T is proved.

1.2 PROJECT GOAL

A variety of full adders using static or dynamic logic styles have been reported in literature . To meet the growing demand, we propose the new high speed, energy efficient adder circuit using 8T (least number of transistors) that yielded very encouraging results so to say, the best in speed, power, threshold loss and power delay product in comparison to other adders using transistor count of 10, 14 and 16. The adder has been designed using 90nm and technology. The power-delay simulation of the adder has been carried out. Simulation results indicate that the analyzed 8T full adder cell has much less power-delay product than its peer designs.

1.3 OVERVIEW

The full adder circuit is a basic building block of all the digital VLSI circuits to have been undergoing a considerable improvement. The very wide spectrum availability of adder designs over the past decades. So in that way the full adder cell based on 16T model has been modeled. There are some of disadvantages in 16T model. To further minimize the number of transistors, pass transistor logic based XOR and XNOR circuits were used and as a result the fourteen transistor full adder circuit was designed. But it suffers with the threshold loss problem. The further designed 10T full adder uses 4T XOR gates in their design and shows the remarkable improvement in power-delay product and reduces the silicon area. The drawback of this circuit is that it also suffers from threshold loss problem approximately equal to 14T adder circuit. The design of proposed full adder is based on three transistor XOR gates. 8T model shows the better performance than the earlier designed full adder and acquires less silicon area as the aspect ratio of transistors is less compared to previous 8T full adder design. The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor. The design of eight transistor full adder (which has the least number of transistors) using three transistor XOR gates and the comparison is made to prove its superiority when the design aspects are the power, delay, PDP and the area.

1.4 SOFTWARE USED

- Microwind 3.1
- Technology used : 90nm

1.5 ORGANIZATION OF THE CHAPTERS

- **Chapter 2** Discusses the design aspects of the full adder cell using different transistor models.
- **Chapter 3** Discusses about the 16 T model full adder cell.
- **Chapter 4** Discusses about the 14 T model full adder cell.
- **Chapter 5** Discusses about the 10 T model full adder cell.
- **Chapter 6** Discusses the 8T model full adder cell.
- **Chapter7** Discusses the comparison of the 16T, 14T, 10T, 8T.
- **Chapter 8** Discuss the simulation and discussions of the performance of the full adder cell.
- **Chapter 9** Shows the conclusion and the future scope of the project.

CHAPTER 2

DESIGN ASPECTS OF FULL ADDER CELL

The main design aspects that are discussed in the project are the following

- Area
- Power dissipation
- Delay (propagation delay)
- PDP

2.1 AREA

An area is defined as a space allocated for a specific purpose. The main aspect in the modeling of full adder cell using transistor count is the area. As the number of transistors is reduced the area is also reduced.

2.2 POWER DISSIPATION (D_p)

CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). On a typical ASIC in a modern 90 nanometer process, switching the output might take 120 picoseconds, and happen once every ten nanoseconds. NMOS logic dissipates power whenever the output is low ("static power"), because there is a current path from V_{dd} to V_{ss} through the load resistor and the n-type network. There are two types of power dissipation available they are the

- Static power dissipation
- Dynamic power dissipation

2.2.1 STATIC DISSIPATION

Sub threshold condition when the transistors are off. Both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current through the device drops exponentially. CMOS designs operated at supply voltages much larger than their threshold voltages.

2.2.2 DYNAMIC DISSIPATION

Charging and discharging of load capacitances. CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from V_{dd} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge. Therefore in one complete charge/discharge cycle, a total is thus transferred from V_{dd} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device.

2.3 DELAY (P_t)

The propagation delay, or gate delay, is the length of time starting from when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. Often this refers to the time required for the output to reach from 10% to 90% of its final output level when the input changes. Reducing gate delays in digital circuits allows them to process data at a faster rate and improve overall performance.

2.4 PDP

The power–delay product is a figure of merit correlated with the energy efficiency of a process. Also known as switching energy, it is the product of power consumption (averaged over a switching event) times the input–output delay, or duration of the switching event. It has the dimension of energy, and measures the energy consumed per switching event. The PDP can be calculated by using $DP = D_p P_t$

CHAPTER 3

16T FULL ADDER MODEL

The spectrum availability of adder designs over the past few decades. The full adder models are designed here using the transistor model. And there are different types of full adder circuit are available. The 16 T model is one of the full adder cell model.

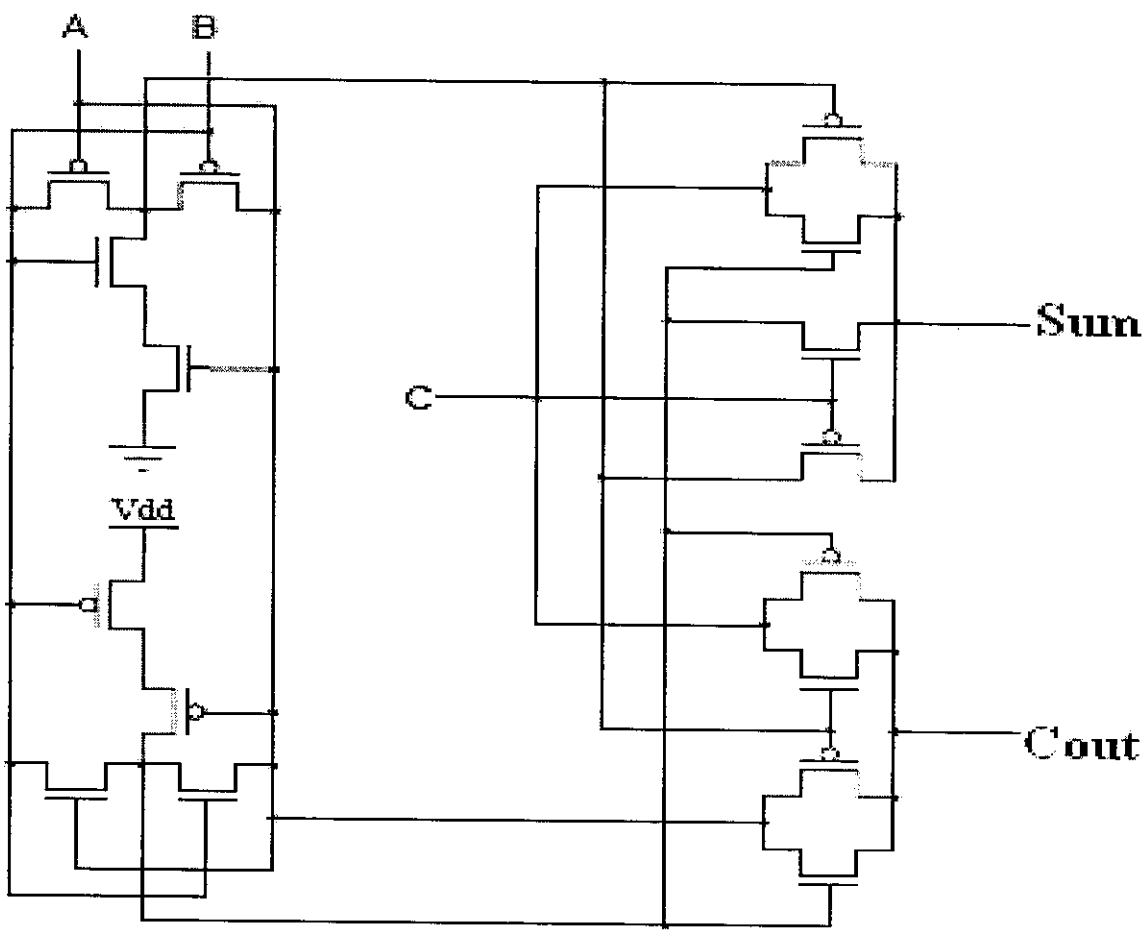

FIGURE 3.1 16T FULL ADDER CIRCUIT

3.1 WORKING OF 16T MODEL

The 16T model of the full adder circuit is working on the static cmos design. The full adder cell realization of the circuit using 16T is shown in the figure 3.1.This circuit can operate with full output voltage swing but consumes significant power and have more delay compared to other adders having less transistor count.

3.2 DRAW BACK OF 16T MODEL

As CMOS technology scaling continues into the nanoscale domain, static or leakage power consumption becomes a vital design parameter. This paper proposes methods for reducing leakage currents by controlling the input vector in nano-scale full adder cells operating in either active mode or standby mode. With proper input vector control, it is possible to obtain over 40% leakage power savings for most of the full adder circuits presented.

CHAPTER 4

14T FULL ADDER CELL

To overcome the drawbacks in the 16T full adder, and to further minimize the number of transistors, pass transistors logic based XOR and XNOR circuits were used and as a result 14T model has been designed. The special aspect of this 14T model is that, it shows the better results for delay and power and power as compared as compared to 16T full adder, but it suffers with the threshold loss problem. It works well in high performance multipliers with low power consumption.

4.1 PASS-TRANSISTOR LOGIC STYLES

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used However, the threshold voltage drop through the NMOS transistors while passing a logic "1" makes swing restoration at the gate outputs necessary in order to avoid static currents at the subsequent output inverters or logic gates. Adjusting the threshold voltages as a solution at the process technology level is usually not feasible for other reasons. Because the MOS networks are connected to variable gate inputs rather than constant power lines, only one signal path through each network must be active at a time in order to avoid shorts between inputs. Therefore, each pass-transistor network must realize a multiplexer structure, which limits the number of logic functions that can be implemented efficiently. In other words, transistor sizing is crucial for correct gate operation and therefore more difficult.

4.2 ADVANTAGE OF LOW TRANSISTOR COUNT

- Also, the required double inter-cell wiring increases wiring complexity and capacitance by a considerable amount.
- Layout of pass-transistor cells is not as straightforward and efficient due to rather irregular transistor arrangements and high wiring requirements.
- Finally, pass-transistor logic with swing restoration circuitry is sensitive to voltage scaling and transistor sizing with respect to circuit robustness (reduced noise margins), i.e., efficient or reliable operation of logic gates is not necessarily guaranteed at low voltages or small transistor sizes.

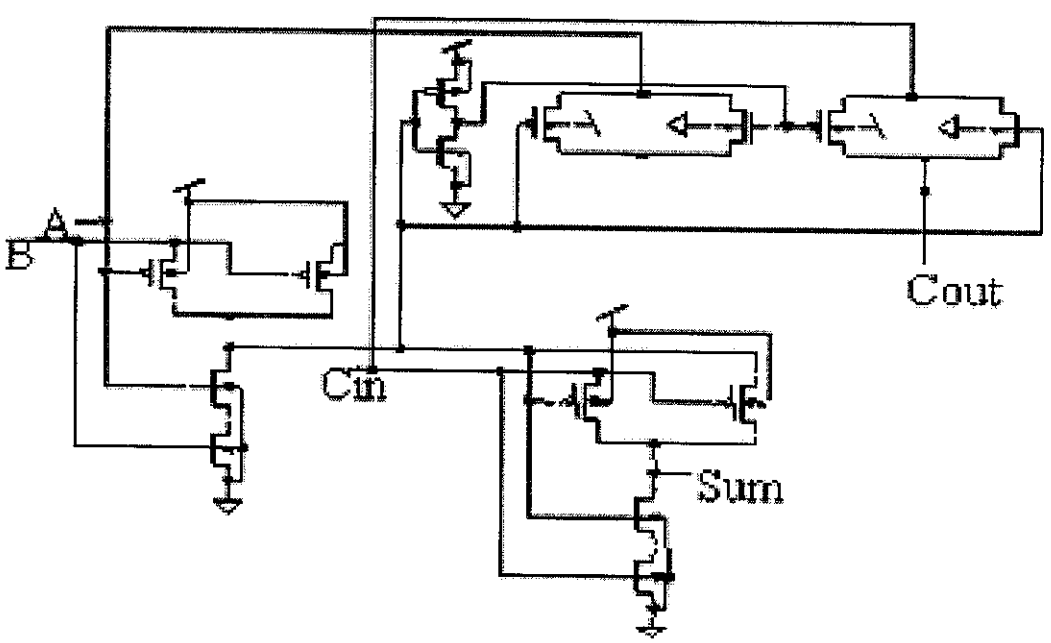

FIGURE 4.1 14T FULL ADDER CIRCUIT

4.3 WORKING OF THE 14T FULL ADDER

A MOS gate employing this method has experimentally exhibited of operating with lower delay. Injecting current may increase the static power consumption hut since the injecting current is small. In size its contribution to the total static power consumption is negligible shows applying the current bulk technique to the NMOS transistor which is suffering from body effect and located in the critical path of the analyzed adder. In fast digital circuit design, to maintain the operating speed as high as possible the threshold voltage of MOSFET must be reduced. This problem can be overcome in the circuit level by compensating the body effect, which directly affects the threshold voltage. The 14T full adder cell suffers from this effect.

4.4 ADVANTAGE OF USING 14T FULL ADDER CELL

- The delay is better.
- Power dissipation is also low when compared with the previous model (i.e., 16T).
- The area is minimized.
- Transistor counts are decreased to 14.

CHAPTER 5

10T FULL ADDER CELL

The 10T is the next main full adder cell that has to be considered. A new full adder called static energy-recovery full-adder (SERF) uses only 10 transistors, which has the least number of transistors and has reported to be the best in power consumption. Many low-power adders apply circuit level techniques using various pass transistors, such as the SERF. The circuit diagram of the 10T full adder cell is given below,

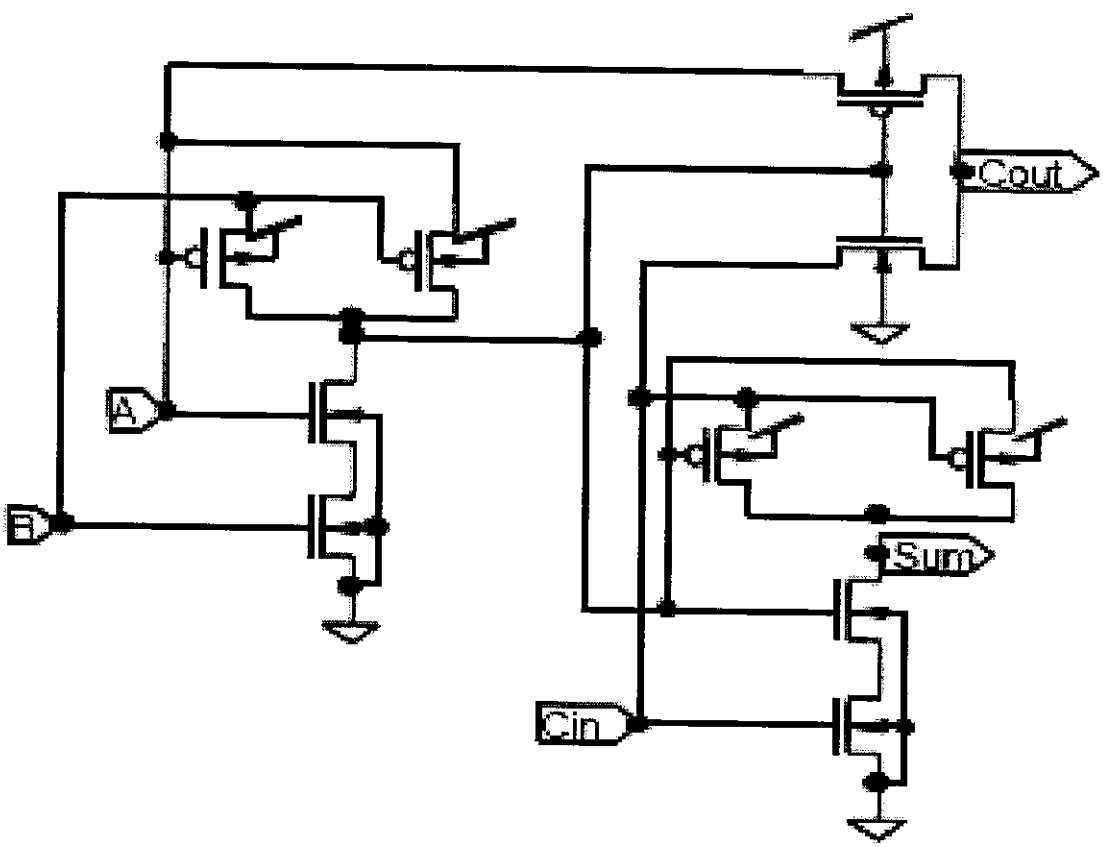

FIGURE 5.1 10T FULL ADDER CIRCUIT

5.1 WORKING OF 10T FULL ADDER CELL

The further designed 10T full adder uses 4T XOR gates in their design. The circuit uses the logic which helps in improving the performance are certainly useful in building up larger circuits such as multiple- bit input adders and multipliers. Where pass transistors are used to generate carry functions and all pass transistors suffer the threshold-loss problem, yet the final adder circuit functions correctly reported. We propose a systematic approach to designing many 10-transistor full adders. The new adders also have the threshold-loss problem; however, the adders are useful in larger circuits such as multipliers despite the threshold-loss problem.

5.2 XOR GATE LOGIC

If a specific type of gate is not available, it can be constructed from other available gates. An XOR gate can be trivially constructed from an XNOR gate followed by a NOT gate. If we consider the expression $A \cdot \overline{B} + \overline{A} \cdot B$, we can construct an XOR gate directly using AND, OR and NOT gates. However, this approach requires five gates of three different kinds. An XOR gate can be made from four NAND or five NOR gates in the configurations shown below. Any logical function can be constructed from either NAND logic or NOR logic alone.

5.3 ADVANTAGES OF 10T FULL ADDER CELL

- Remarkable improvement in the power delay product.
- It also reduces the silicon area.
- Shows better performance than the SERF 10T adder cell.

5.4 DRAWBACK OF THE 10T FULL ADDER CELL

- Suffers from threshold loss problem which is approximately equal to 14T adder circuit.

CHAPTER 6

8T FULL ADDER CELL

The design of proposed full adder is based on three transistor XOR gates. It shows the better performance than the earlier designed full adder and acquires less silicon area as the aspect ratio of transistors is less compared to previous 8T full adder design. The design of 3T XOR gate is shown Fig. .The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor

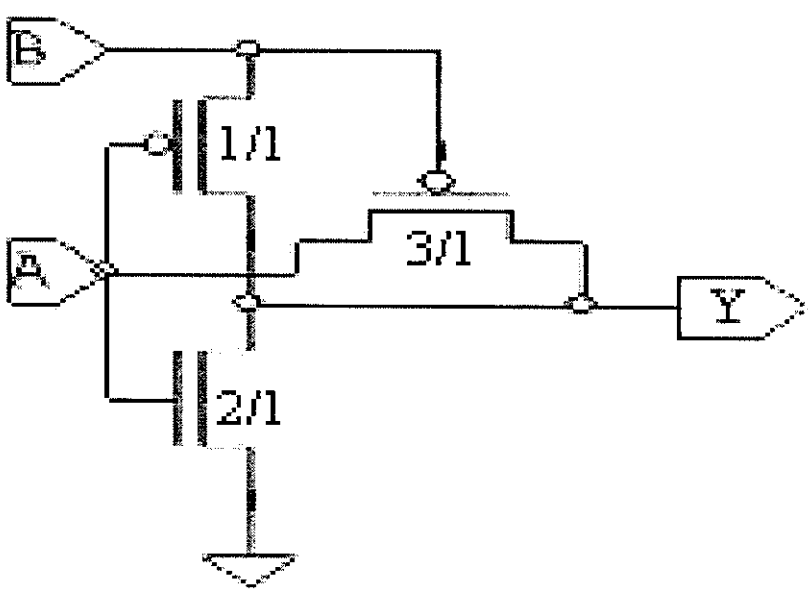

FIGURE 6.1 DESIGN OF 3T XOR GATE

6.1 ANALYSED 8T FULL ADDER

The design of eight transistor full adder (the least number of transistors) using the three XOR gates is shown in the figure 6.2.1. The paper proposes the novel design of a 3T XOR gate combining complementary CMOS with pass transistor logic. The design has been compared with earlier proposed 4T and 6T XOR gates and a significant improvement in silicon area and power-delay product has been obtained. An eight transistor full adder has been designed using the three-transistor XOR gate and its performance has been investigated. Compared to the earlier designed 10 transistor full adder, the proposed adder shows a significant improvement in silicon area and power delay product. The Boolean equations for the design of the eight transistor full adder are as follows:

$$\mathbf{Sum = A \oplus B \oplus Cin}$$

$$\mathbf{Cout = Cin\ (A \oplus B) + AB}$$

The 8Tadder cell is given below.

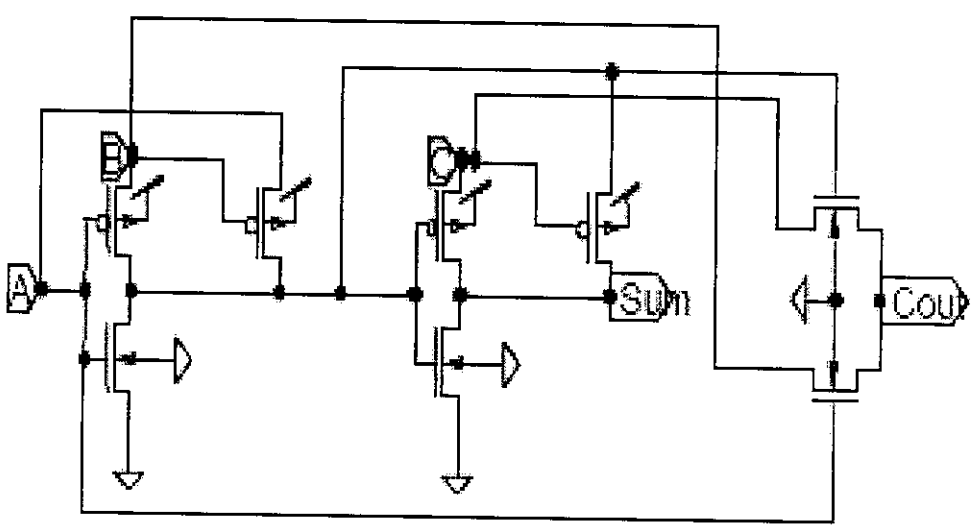

FIGURE 6.2 - ANALYZED 8T FULL ADDER

6.2 WORKING OF 8T FULL ADDER CELL

The working of the 8T full adder cell is based on the 3T XOR gate. The design of the 8T full adder is based on a modified version of the CMOS inverter and a PMOS pass transistor.

6.2.1 CMOS INVERTER AND ITS WORKING

A CMOS, or complementary metal-oxide-semiconductor, inverter is a device that is capable of producing logic functions and is the primary component of all integrated circuits. CMOS inverters are a type of field-effect transistor and are composed of a metal gate that lies on top of a semiconductor. CMOS inverters are found in most electronic devices and are responsible for producing data within small circuits. CMOS inverters work like most other types of field-effect transistors, but depend on a layer of oxygen to separate electrons in the gate and those found in the semiconductor. CMOS inverters are composed of a power supply, a voltage input terminal, a gate, a drain, a voltage output, and PMOS and NMOS that are connected to both the gate and the drain. As a low voltage is applied to the voltage input, the PMOS is turned on while the NMOS remains off, allowing electrons to flow through the gate and causing the voltage output to produce a high logic. Conversely, as a high voltage is applied to the voltage input, both the PMOS and NMOS is turned on, preventing as many electrons from reaching the voltage output and causing the voltage output to produce a low logic.

6.2.2 APPLICATIONS

CMOS inverters are used for a wide variety of applications and play a critical role in integrated circuits including microprocessors, microcontrollers, static RAM, image sensors, data converters, and some types of transceivers. CMOS inverters are found in digital cameras, mobile devices, home computers, network servers, routers, modems, cell phones, and virtually every other electronic device that requires logic functions.

6.2.3 ADVANTAGES

CMOS inverters have several important advantages. For example, CMOS inverters only use electricity when they are turned on and off, resulting in very little power consumption. Consequently, CMOS inverters also produce very little heat waste, making them highly efficient and able to be used in a wide variety of small, delicate electronic devices. Additionally, CMOS inverters have high noise immunity, allowing them block both incoming and outgoing frequency spikes, and are inexpensive to mass produce.

6.3 PASS TRANSISTOR LOGIC

Pass transistors require lower switching energy to charge up a node, due to the reduces voltage swing. The output node charges and the energy drawn from the power supply for charging the output of a pass transistor are given. While lower switching power is consumed, it may consume static power when output is high – the reduced voltage level may be insufficient to turn off the PMOS transistor of the subsequent CMOS inverter.

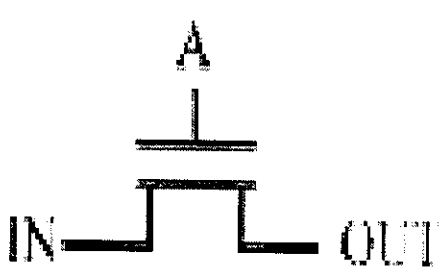

FIGURE 6.3 PASS TRANSISTOR LOGIC

CHAPTER 7

COMPARISON OF THE FULL ADDER CELLS

The comparisons between different adders are given below with a constant voltage of 1.2V.

FULL ADDER CELL	DELAY (P_t)	POWER DISSIPATION (D_p)	PDP (D_p P_t)
16T	0.055ns	44.331μW	2.438fJ
14T	0.097ns	0.229mW	22.213fJ
10T	0.051ns	0.648μW	0.0334fJ
8T	0.038ns	0.052μW	0.00198fJ

FIGURE 7.1 COMPARISONS OF DIFFERENT ADDERS

From the tabulation, the 16T model has delay of 0.055ns, power dissipation of 44.331μW and the PDP of 2.438fJ. And whereas the 14T model has 0.097ns the delay is more than that of 16T, this is due to threshold loss problem and D_P as 0.229mW, PDP as 22.313fJ, hence the delay s more. For 10T model delay of 0.051ns, power dissipation of 0.648μW and the PDP of 0.0334fJ. The parameters of 10T have the better performance than the previous model. 8T have the delay of 0.038ns, power dissipation of 0.052μW, PDP as 0.00198fJ. On comparing the all four types of full adder cell has better performance than the previous model. Hence the superiority of the 8T model is proved.

CHAPTER 8

SIMULATIONS AND DISCUSSIONS OF THE PERFORMANCE OF FULL ADDER

8.1 PERFORMANCE OF 16T FULL ADDER CELL

The simulation is carried out for the 16T and waveform for the power dissipation is obtained. And the power dissipation of 16T is = 46.932μW

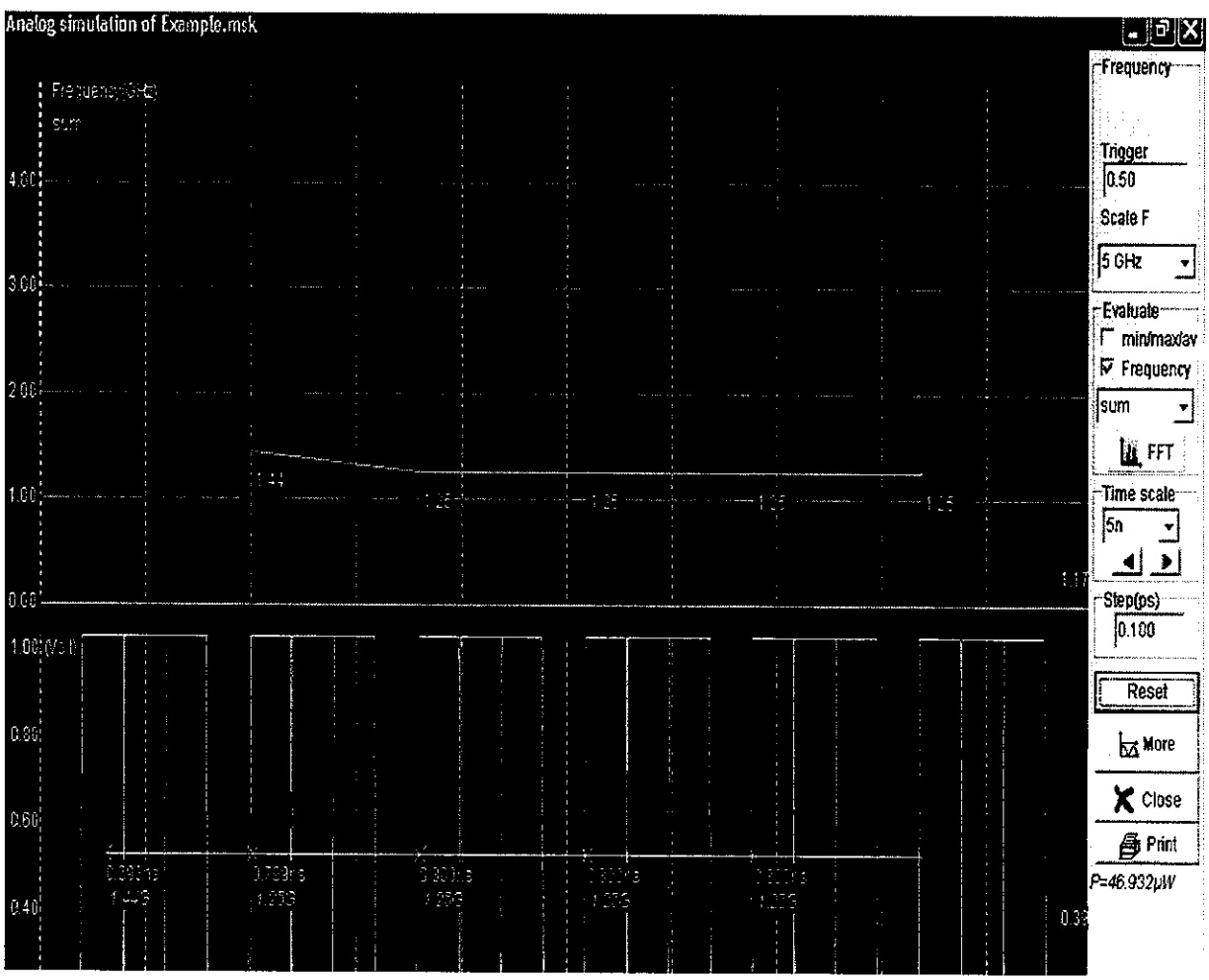

FIGURE 8.1 SIMULATION RESULT OF 16T POWER DISSIPATION

8.1.1 DELAY OF 16T

The delay of 16T full adder cell is carried out for 1.2V and the simulation result is given below in figure 8.2. The delay of 16T is 0.055ns

Verilog, Hierarchy and Netlist

Verilog | Hierarchy | Netlist | Critical path

Path n°	Symbol	Pin	Node	Delay (ns)
1	light(15)	carry(1)	6	0.055
2	pmos(5)	d(3)	6	0.055
3	pmos(5)	g(2)	4	0.040
4	pmos(1)	d(3)	4	0.040
5	pmos(2)	d(3)	4	0.040
6	nmos(3)	d(3)	4	0.050
7	nmos(3)	s(1)	5	0.010
8	nmos(4)	d(3)	5	0.010
9	nmos(8)	d(3)	6	0.055
10	nmos(8)	g(2)	4	0.040
11	pmos(1)	d(3)	4	0.040
12	pmos(2)	d(3)	4	0.040
13	nmos(3)	d(3)	4	0.050
14	nmos(3)	s(1)	5	0.010
15	nmos(4)	d(3)	5	0.010

FIGURE 8.2 SIMULATION RESULT OF 16T - DELAY

8.2 PERFORMANCE OF 14T FULL ADDER CELL

The simulation has been carried out for the 14T full adder cell and the waveform is shown below. Power dissipation of 14T is 0.229mW

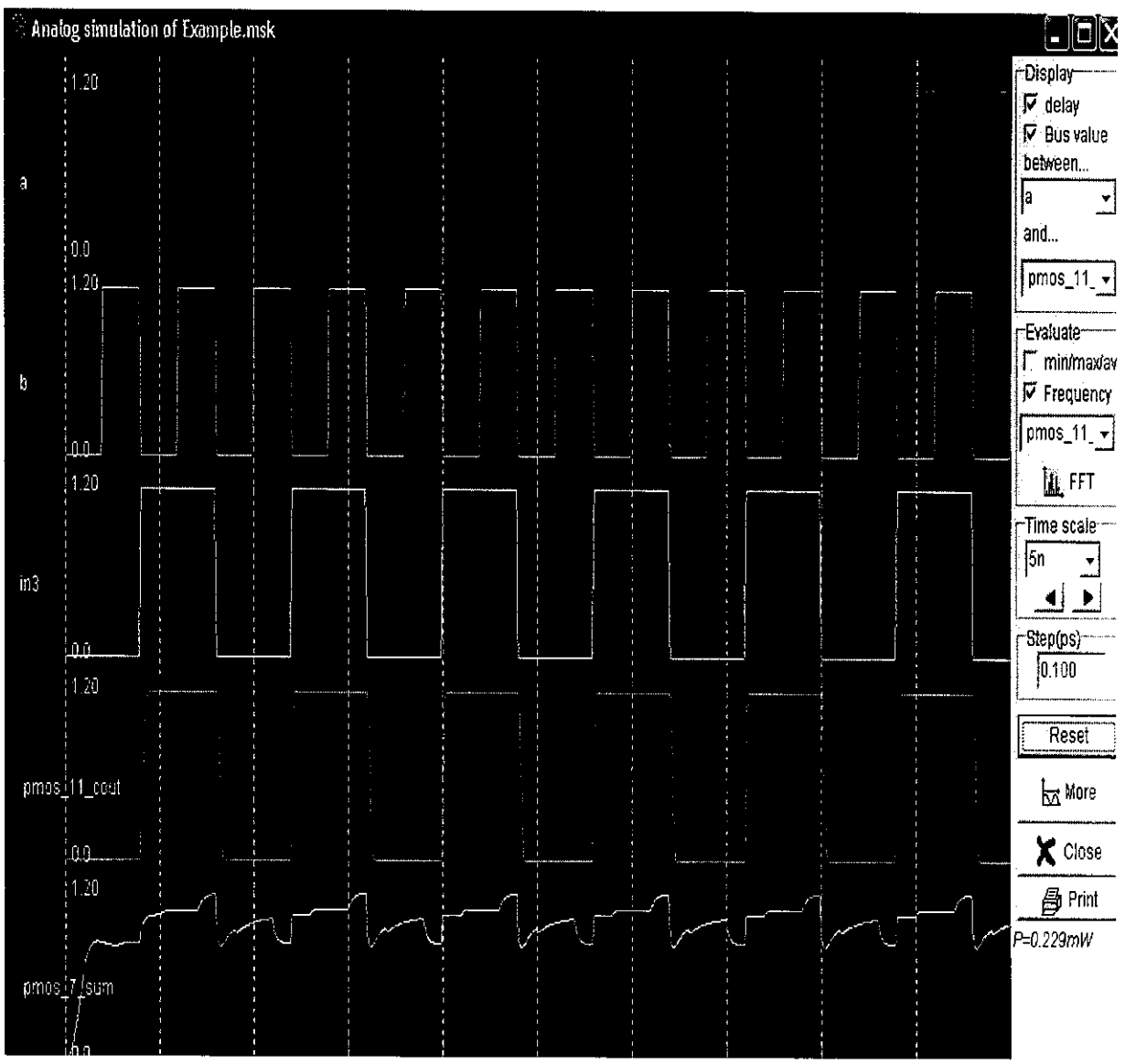

FIGURE 8.3 SIMULATION RESULT OF 14T-POWERDISSIPATION

8.2.1 DELAY OF 14T

The delay of 14T full adder cell is carried out for 1.2V and the simulation result is given below in the figure 8.4. The delay of 14T is 0.097ns

Verilog | Hierarchy | Netlist | Critical path

Path n°	Symbol	Pin	Node	Delay (ns)
1	light(14)	sum(1)	7	0.097
2	pmos(6)	d(3)	7	0.097
3	pmos(6)	s(1)	6	0.079
4	pmos(5)	d(3)	6	0.079
5	pmos(5)	g(2)	5	0.071
6	pmos(2)	d(3)	5	0.071
7	pmos(2)	s(1)	3	0.008
8	pmos(1)	d(3)	3	0.008
9	nmos(3)	d(3)	5	0.063
10	nmos(4)	d(3)	5	0.063
11	nmos(7)	d(3)	7	0.089
12	nmos(7)	s(1)	5	0.071
13	pmos(2)	d(3)	5	0.071
14	pmos(2)	s(1)	3	0.008
15	pmos(1)	d(3)	3	0.008
16	nmos(3)	d(3)	5	0.063
17	nmos(4)	d(3)	5	0.063
18	nmos(8)	d(3)	7	0.089
19	nmos(8)	s(1)	5	0.071
20	pmos(2)	d(3)	5	0.071
21	pmos(2)	s(1)	3	0.008
22	pmos(1)	d(3)	3	0.008

FIGURE 8.4 SIMULATION RESULT OF 14T- DELAY

8.3 PERFORMANCE OF 10T FULL ADDER CELL

The simulation has been carried out for the 10T full adder cell and the waveform is shown below in the figure 8.5. The power dissipation of 10T is 0.513μW

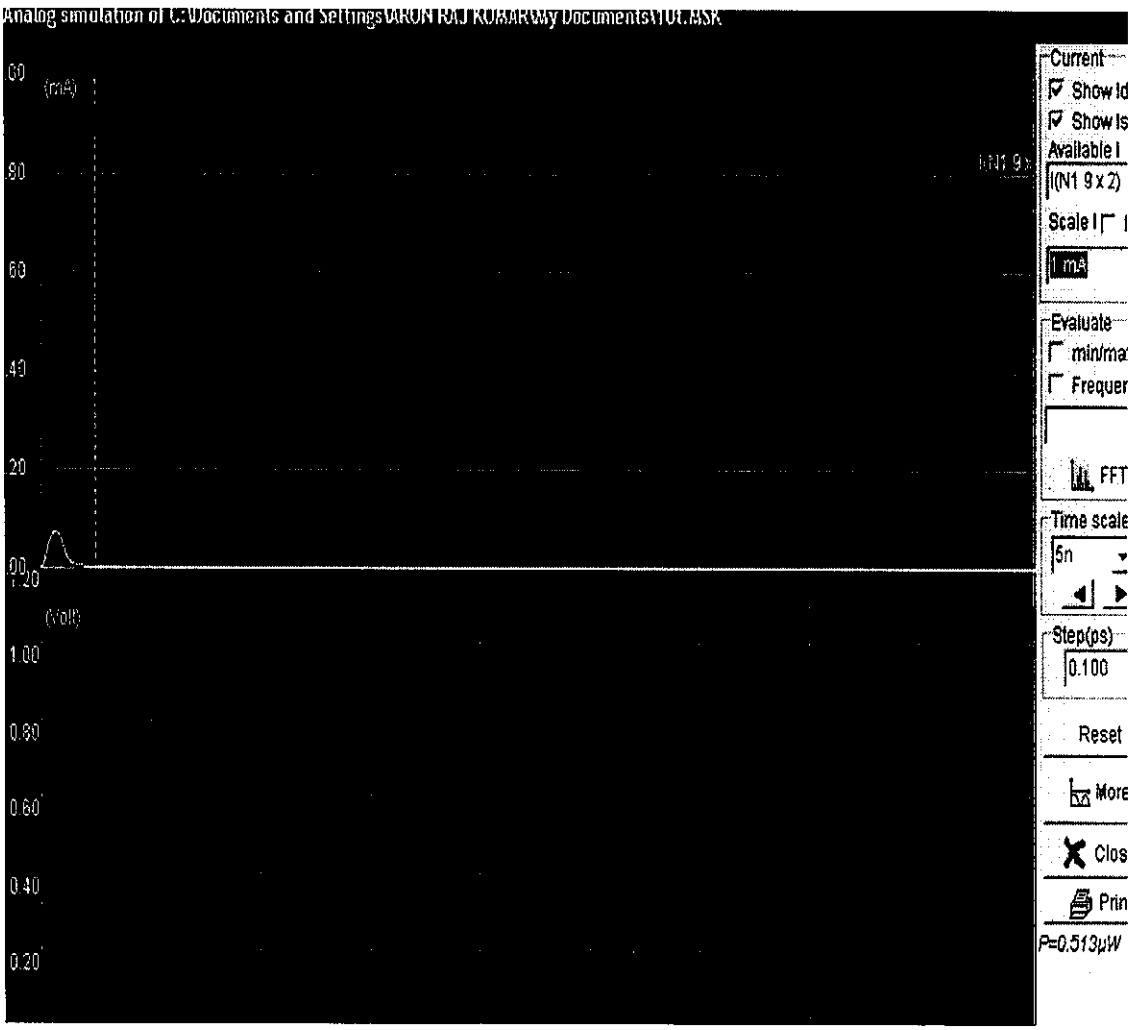

FIGURE 8.5 SIMULATION RESULT OF 10T -POWER DISSIPATION

8.3.1 DELAY OF 10T

The delay of 10T full adder cell is carried out for 1.2V and the simulation result is given below in the figure 8.6. The delay of the 10T is 0.051ns.

Verilog, Hierarchy and Netlist

Verilog | Hierarchy | Netlist | Critical path

Path n°	Symbol	Pin	Node	Delay (ns)
1	light(16)	COut(1)	6	0.051
2	pmos(8)	d(3)	6	0.051
3	pmos(8)	g(2)	4	0.038
4	pmos(1)	d(3)	4	0.038
5	pmos(2)	d(3)	4	0.038
6	nmos(3)	d(3)	4	0.046
7	nmos(3)	s(1)	5	0.008
8	nmos(4)	d(3)	5	0.008
9	nmos(9)	d(3)	6	0.051
10	nmos(9)	g(2)	4	0.038
11	pmos(1)	d(3)	4	0.038
12	pmos(2)	d(3)	4	0.038
13	nmos(3)	d(3)	4	0.046
14	nmos(3)	s(1)	5	0.008
15	nmos(4)	d(3)	5	0.008

FIGURE 8.6 SIMULATION RESULT OF 10T- DELAY

8.4 PERFORMANCE OF 8T FULL ADDER CELL

The simulation has been carried out for the 8T full adder cell and the waveform is shown below in the figure 8.4.the power dissipation of 8T is 0.052μW

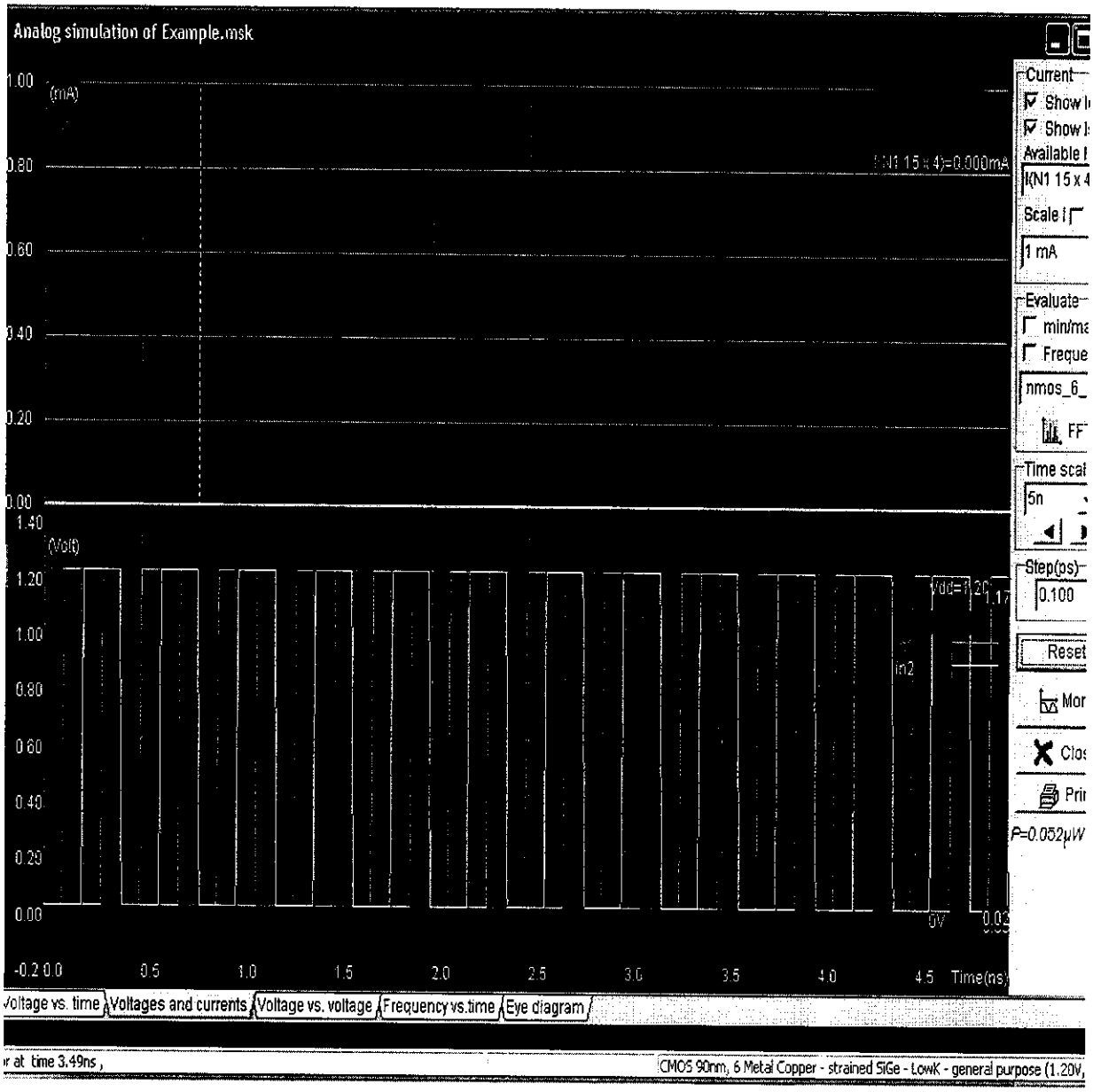

FIGURE 8.7 SIMULATION RESULT OF 8T - POWER DISSIPATION

8.4.1 DELAY OF 8T

The delay of 8T full adder cell is carried out for 1.2V and the simulation result is given below in the figure 8.8 .The delay of 8T is 0.038ns.

Verilog, Hierarchy and Netlist

Verilog | Hierarchy | Netlist | Critical path |

Path n°	Symbol	Pin	Node	Delay (ns)
1	light(17)	out1(1)	8	0.038
2	nmos(9)	d(3)	8	0.038
3	nmos(9)	g(2)	4	-0.036
4	nmos(1)	d(3)	4	0.036
5	nmos(1)	g(2)	3	0.030
6	nmos(11)	d(3)	3	0.029
7	nmos(12)	d(3)	3	0.021
8	nmos(7)	d(3)	4	0.020
9	nmos(7)	s(1)	7	0.029
10	nmos(6)	d(3)	7	0.016
11	nmos(14)	d(3)	8	0.021

FIGURE 8.8 SIMULATION RESULT OF 8T- DELAY

CHAPTER 9

CONCLUSION AND FUTURE SCOPE

9.1 CONCLUSION

The design of the improved full adder using 8T which acquires least area and has least power-delay product with the lowest transistor count. It also reduces the power loss problem compared to other circuits. With the help of this adder cell, we can design an efficient and high performance multiplier unit. The analyzed 8T adder has been designed and studied using 90nm technology which establishes the technology independence of the circuit.

So far the transistor modeling of full adder cells are of different count. The superiority of the least count transistor (8T) is proved as the best in power dissipation, delay, and power delay product. By giving out the proper and the constant voltage maintained at each level of the transistors is clearly given in figure 7.1. The conclusion of the project is that the 8T models of full adder cell have the better performance if the design aspects are the power, delay and power delay product.

9.2 FUTURE SCOPE

The analyzed 8T adder will be designed using various technologies, which establish the technology independence of the circuit. With the help of this adder cell, we can design efficient and high performance arithmetic units.

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