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IMPROVED CARRY SELECT ADDER WITH REDUCED AREA AND LOW POWER CONSUMPTION

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BONAFIDE CERTIFICATE

Certified that this project report entitled **"IMPROVED CARRY SELECT ADDER WITH REDUCED AREA AND LOW POWER CONSUMPTION"** is the bonafide work of **Ms.S.PRIYA** [Reg. No.1020106015] who carried out the mini project under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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External Examiner

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ABSTRACT

Power dissipation is one of the most important design objectives in integrated circuits, after speed. As adders are the most widely used components in such circuits, design of efficient adder is of much concern for researchers. Applications where these are used are multipliers, DSP to execute various algorithms like Fast Fourier Transform (FFR), Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Wherever concept of multiplication comes adders come in to the picture. This project presents performance analysis of different Fast Adders. The comparison is done on the basis of two performance parameters i.e. Area and Power consumption. In Carry Select Adder, two adders one for Cs1=1 and other for Cs1=0 are used to calculate the sum and carry whereas one adder is used in Modified Carry Select Adder in order to reduce the area and power consumption .Each of two additions is performed in one clock cycle. These are changes made in carry select adder to obtain clock select adder with sharing as modified carry select adder. In this project work ,the ripple carry adder ,carry skip adder ,carry select adder and clock select adder with sharing are compared with respect to two parameters and the results reflects that modified carry select adder with sharing provides better performance in terms of area and power consumption.

(**INDEX TERMS** - Adder, Carry Select Adder, Carry Skip Adder, Clock Select Adder with Sharing.)

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LIST OF ABBREVIATIONS

RCA	-------	Ripple Carry Adder
CSKA	-------	Carry Skip Adder
CSA	-------	Carry Select Adder
VBA	-------	Variable Block Adder
CSAS	-------	Clock Select Adder with Sharing
LUT's	-------	Look Up Tables

CHAPTER 1

INTRODUCTION

Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes, adders come in to the picture.

1.1. PROJECT GOAL

The performance analysis of different fast adders is done. The comparison is made on two parameters .i.e. Area and Power. The main goal of the project is to prove modified carry select designed in different stages are better in area and power consumption.

1.2 OVERVIEW

The Ripple carry adder is first implemented, which is slowest in speed and leads to high power consumption. A carry skip adder and variable carry skip adder is implemented, which occupies more area and high power consumption. The modified carry select is implemented and comparison is made between different adders. The modified carry select adder is provides better reduction in area and low power consumption.

1.3 SOFTWARE USED

- ModelSim XE 6.3 f
- Xilinx ISE 8.1 i

1.4 ORGANIZATION OF THE REPORT

- **Chapter 2** discusses about the Ripple Carry adder.
- **Chapter 3** discusses about the Carry Skip adder.
- **Chapter 4** discusses about the Carry Select adder.
- **Chapter.5** discusses about the Variable Stage Carry Select adder
- **Chapter 6**. discusses about the Clock Select adder with sharing
- **Chapter 7** discusses the simulation results
- **Chapter8** shows the conclusion of the project.

CHAPTER 2
RIPPLE CARRY ADDER

Concatenating the N full adders forms N bit Ripple carry adder .In this carry out of previous full adder becomes the input carry for the next full adder. It calculates sum and carry according to the following equations. As carry ripples from one full adder to the other, it traverses longest critical path and exhibits worst case delay. The sum and carry expressions are specified by equations 2.1 and 2.2.

Si = Ai xor Bi xor Ci   2.1

Ci+1 = Ai Bi + (Ai + Bi) Ci; where i = 0, 1… n-1   2.2

RCA is the slowest in all adders (O (n) time) but it is very compact in size (O (n) area). If the ripple carry adder is implemented by concatenating N full adders, the delay of such an adder is 2N gate delays from Cin to Cout. The delay of adder increases linearly with increase in number of bits. Block diagram of RCA is shown in figure 1.1.

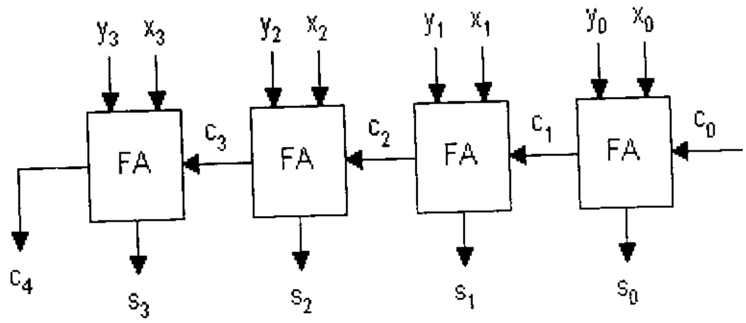


Figure1.1: Block Diagram of Ripple Carry Adder

CHAPTER 3

CARRY SKIP ADDER (CSKA)

A carry skip divides the words to be added in to groups of equal size of k-bits. Carry Propagate *pi* signals may be used within a group of bits to accelerate the carry propagation. If all the pi signals within the group are pi=1, carry bypasses the entire group as shown in figure 2.1.

In this way delay is reduced as compared to ripple carry adder. The worst-case carry propagation delay in a N-bit carry skip adder with fixed block width *b*, assuming that one stage of ripple has the same delay as one skip, can be derived by equation 3.1

$$TCSKA = (b - 1) + 0.5 + (N/b - 2) + (b - 1) = 2b + N/b - 3.5 \text{ Stage.} \qquad 3.1$$

Block width tremendously affects the latency of adder. Latency is directly proportional to block width. The idea behind Variable Block Adder (VBA) is to minimize the critical path delay in the carry chain of a carry skip adder, while allowing the groups to take different sizes. In case of carry skip adder, such condition will result in more number of skips between stages.

Such adder design is called variable block design, which is tremendously used to fasten the speed of adder The bit widths of groups are taken as; First block is of 4 bits, second is of 6 bits, third is 18 bit wide and the last group consist of most significant 4 bits

.

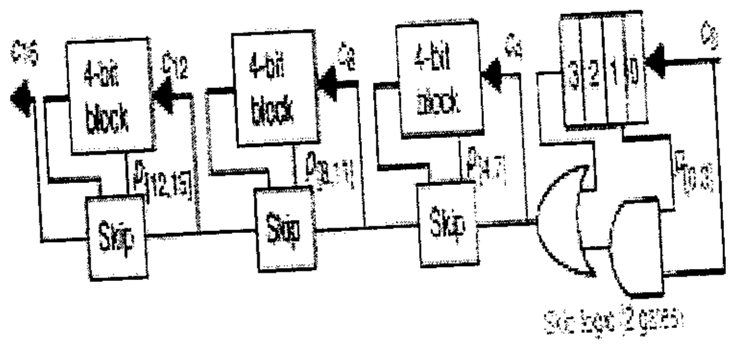


Figure 2.1: Carry Skip Adder

CHAPTER 4

The CARRY SELECT ADDER

The carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional carry select adder consists of k/2bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits (MSB's) two k/bit adders. In MSB adders one adder assumes carry input as one for performing addition and another assumes carry input as zero. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum. The selection is done by using a multiplexer. This technique of dividing adder in to stages increases the are a utilization but addition operation fastens. The block diagram of conventional k bit adder is shown in figure 3.1.

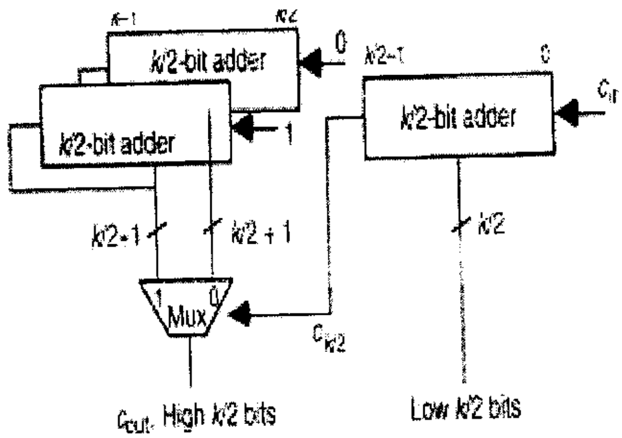


Figure 3.1: Block Diagram of k-bit Carry Select Adder

CHAPTER 5

VARIABLE STAGE CARRY SELECT ADDER

The idea of iterating the CSA will reduce the delay of the adder. The diagram of three-stage carry select adder is shown in figure 4.1. For constructing such a k-bit adder it is divided in to m groups where group i, contains Pi bits, such that bit width of the least significant part is P1 and bit width of the most significant part is Pm. In part Pm adders will be duplicated or there are two adders; one computing addition for carry input 1 and another for carry input 0. Where cs1 is the carry out of P1 bit adder. Cs2 is the carry propagated from the other part of adder. Cout is the final carry output of the adder. Similarly we can design for further 4 stage and 5 stage CSA adders to further reduce the delay. The main focus is on value of m. Some effort has been done to improve such adders.

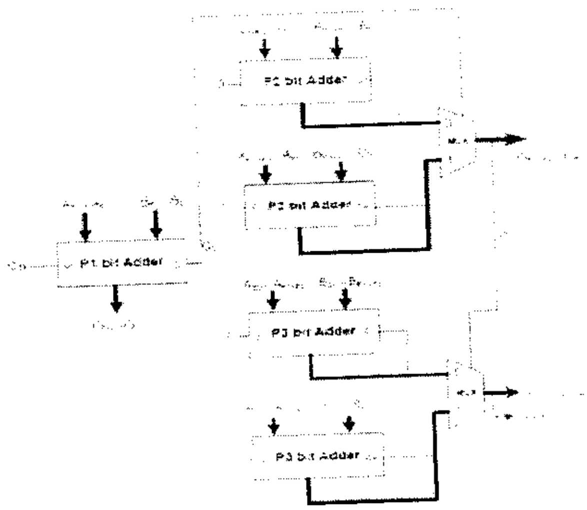


Figure 4.1: Three stage Carry Select Adder

CHAPTER 6

CLOCK SELECT ADDER WITH SHARING (CSAS)

Instead of using two separate adders in conventional CSA, one for the Cs1 =1 and another for theCs1=0 One adder is used to reduce the area and power consumption. Each of the two additions is performed in one clock cycle. The block diagram of CSAS is shown in figure 5.1. This is a32-bit adder in which least significant bit (LSB) adder is a ripple carry adder (RCA) adder, which is 22 bits wide. The upper half of the adder i.e. most significant part is 10 bits wide.

This part works according to clock. Whenever clock goes high addition for the carry input one is performed. And when clock goes low then carry input is assumed as zero and addition is stored in adder itself. As can be seen from the figure 5 latch is used to store the sum and carry for Cin=1. Carry out from the previous stage i.e. least significant bit adder is used as control signal for multiplexer to select the final output carry and sum of the adder. Cout is the output carry. Similarly, CSAS adders can be designed for more stages to reduce area and power consumption.

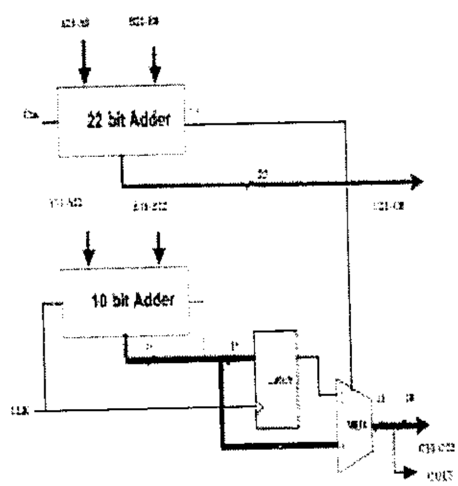


Figure5.1: The Architecture of Clock Select Adder with Sharing

CHAPTER 7
RESULTS AND DISCUSSION

The simulation of this project has been done using MODELSIM SE 6.3f and XILINX ISE 8.1 i.

ModelSim is a simulation tool for programming {VLSI} {ASIC}s, {FPGA}s, {CPLD}s, and {SoC}s. Modelsim provides a comprehensive simulation and debug environment for complex ASIC and FPGA designs. Support is provided for multiple languages including Verilog, SystemVerilog, VHDL and SystemC.

Xilinx was founded in 1984 by two semiconductor engineers, Ross Freeman and Bernard Vonderschmitt, who were both working for integrated circuit and solid-state device manufacturer Zilog Corp. The Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6 FPGA families are particularly focused on system-on-chip (SOC) designers because they include up to two embedded IBM PowerPC cores The ISE Design Suite is the central electronic design automation (EDA) product family sold by Xilinx. The ISE Design Suite features include design entry and synthesis supporting Verilog or VHDL, place-and-route (PAR), completed verification and debug using Chip Scope Pro tools, and creation of the bit files that are used to configure the chip.

The simulation results for Ripple Carry adder, Carry Skip adder, Variable Stage Carry Skip adder, Carry Select adder, 3 and 4 Stage Carry select adder, and Clock Select adder with sharing are attached here.

7.1 SIMULATION RESULT

7.1.1 RIPPLE CARRY ADDER

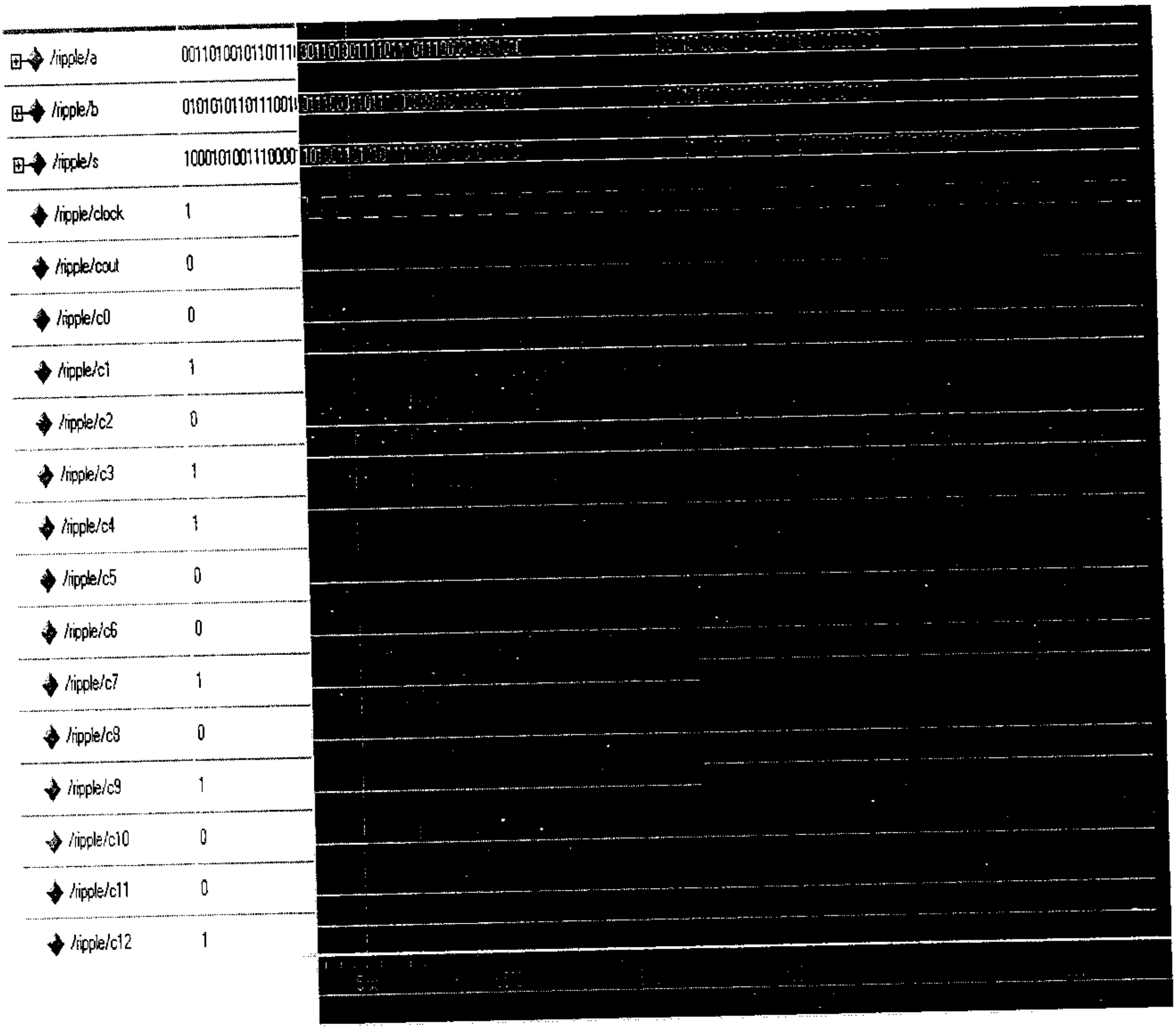


Figure 6.1 Simulation results of Ripple Carry Adder.

7.1.2 CARRY SKIP ADDER

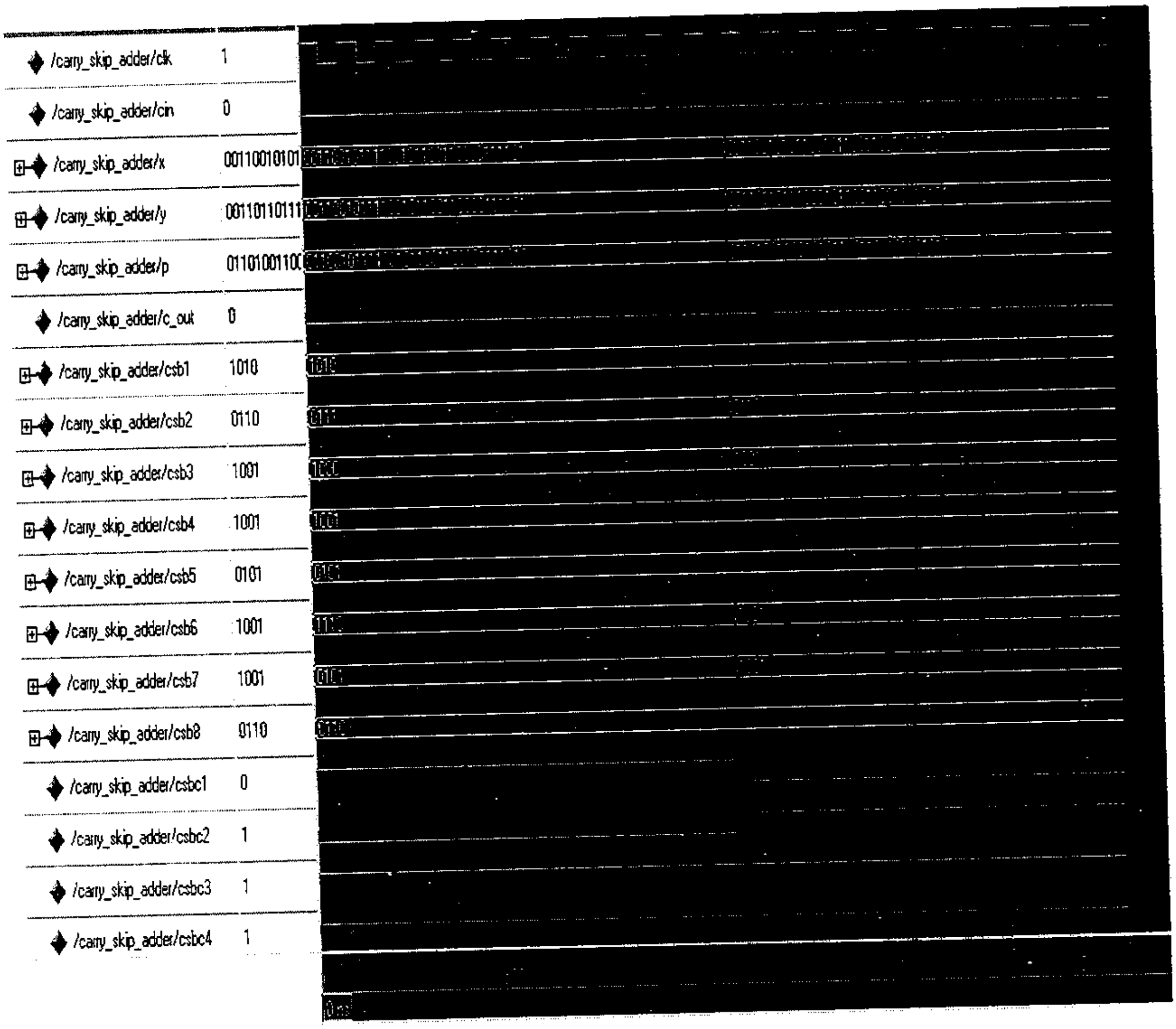


Figure6.2 Simulation result of Carry Skip Adder

7.1.3 VARIABLE CARRY SKIP ADDER

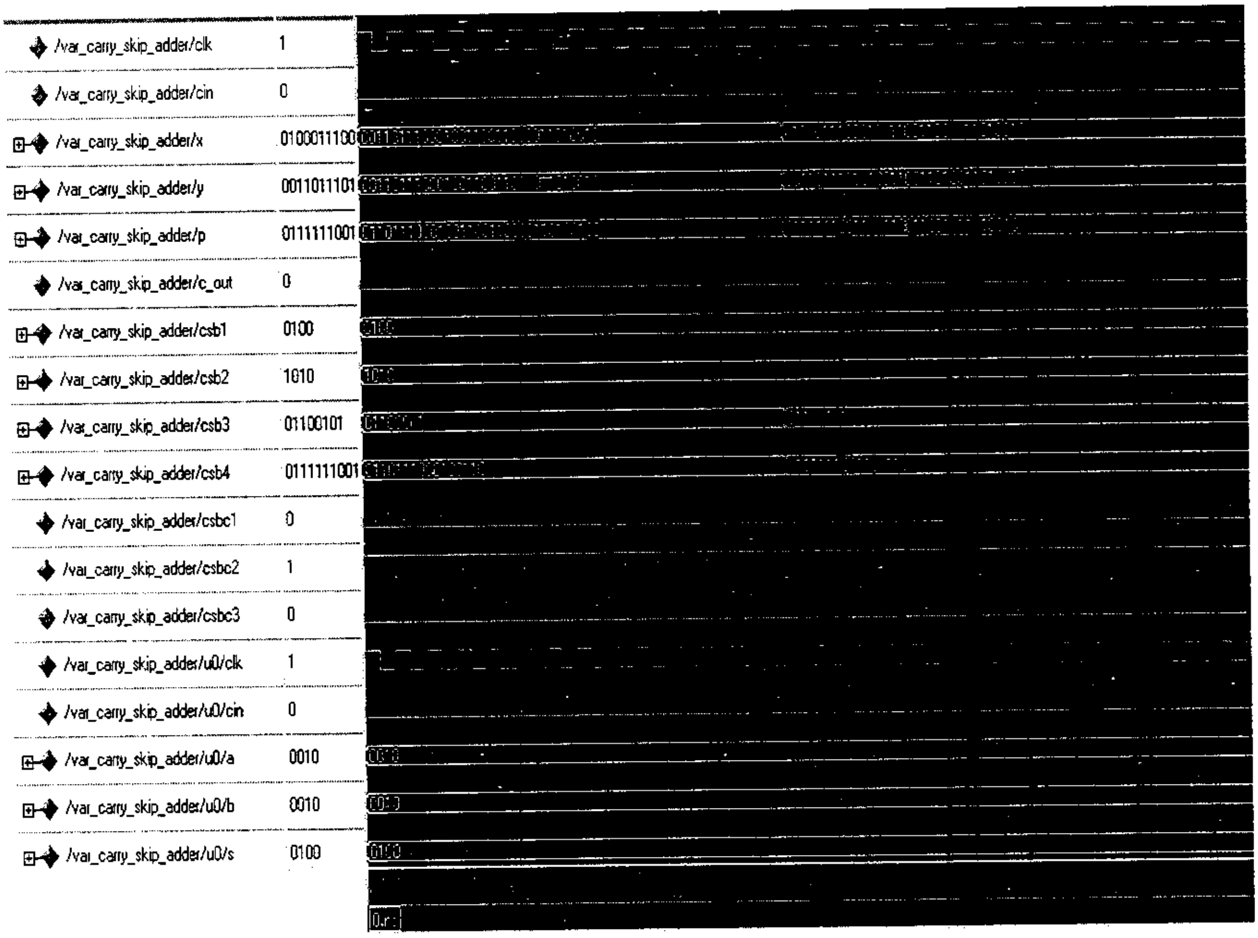


Figure 6.3 Simulation result of Variable Carry Skip Adder

7.1.4 CARRY SELECT ADDER

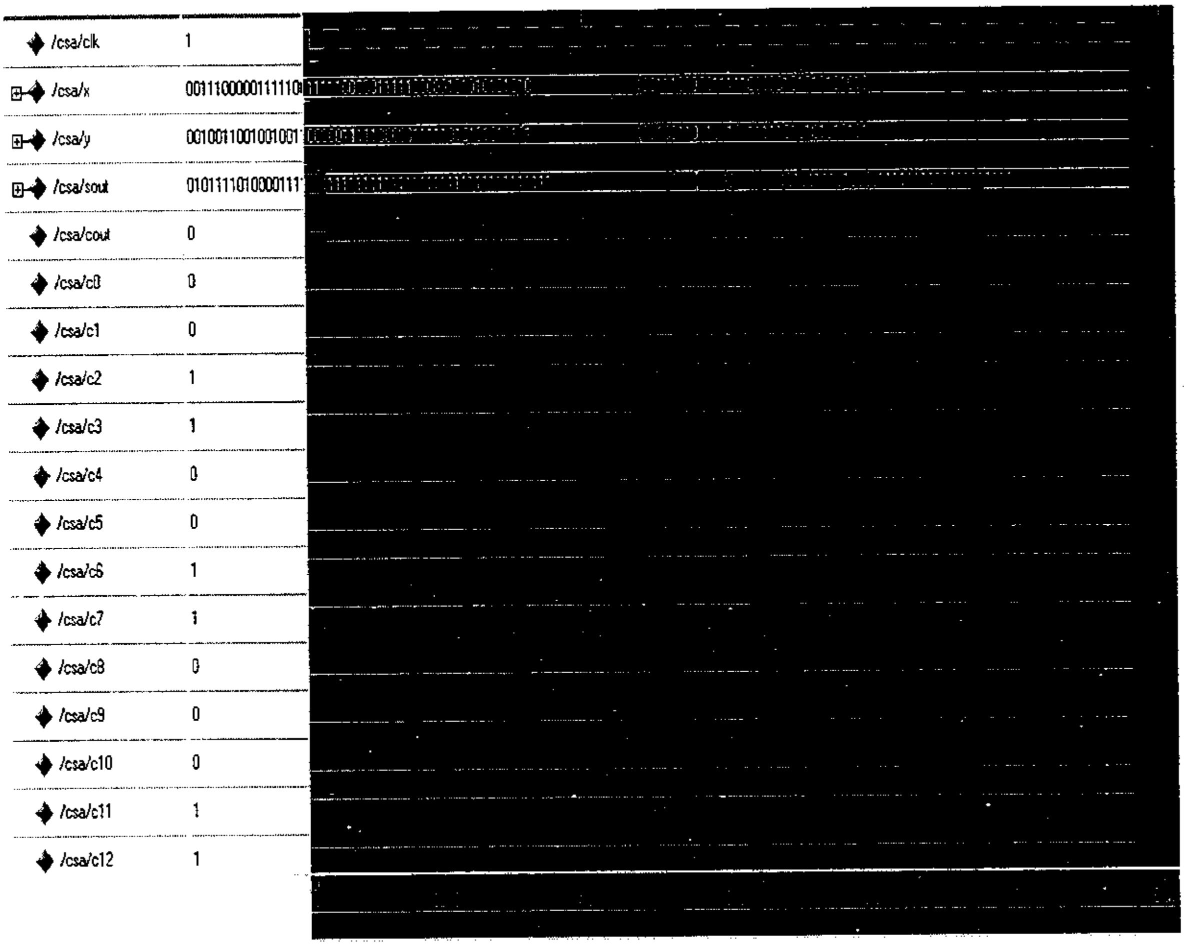


Figure 6.4 Simulation result of Carry Select Adder

7.1.5 3 Stage Carry Select adder

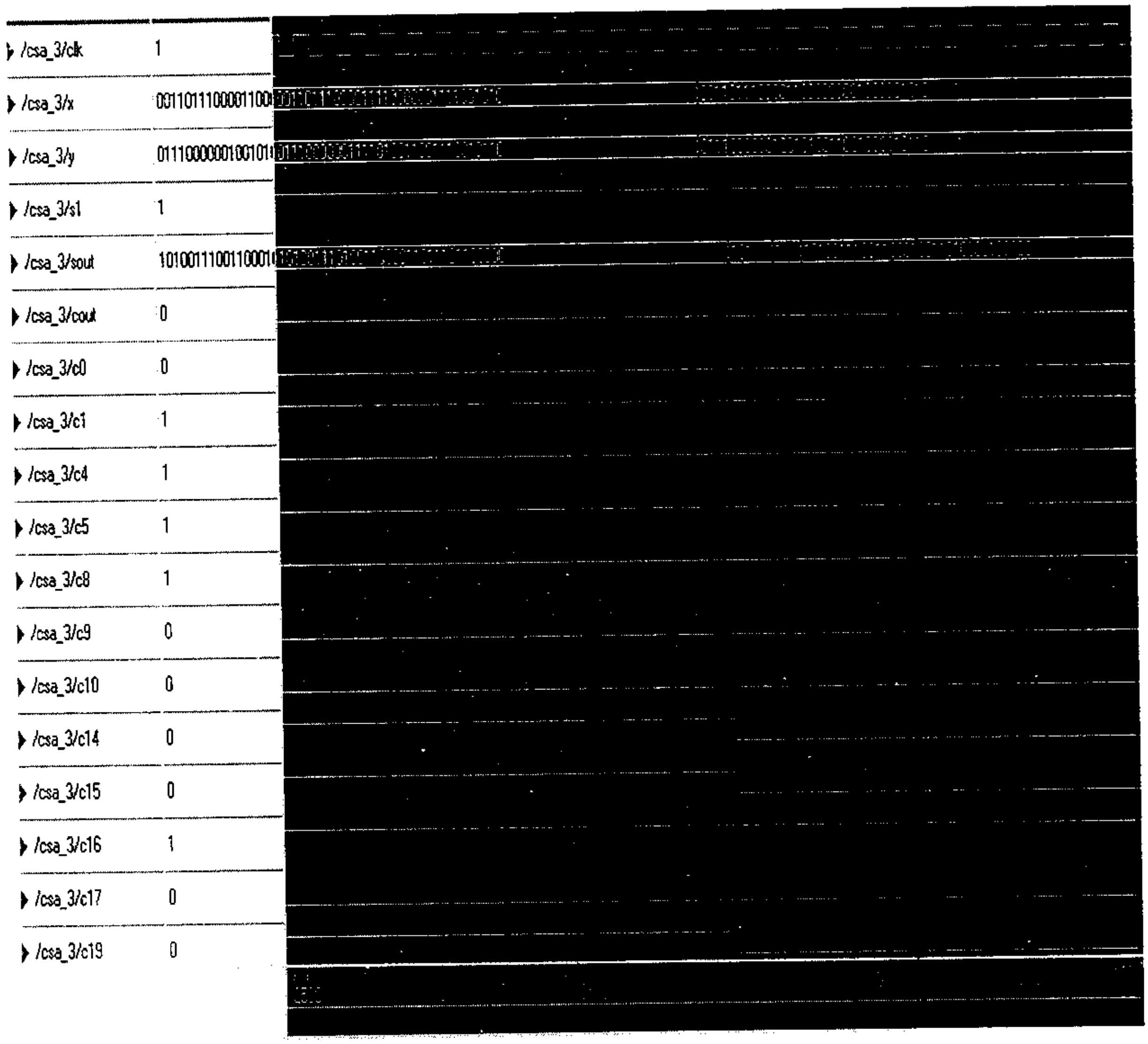


Figure 6.5 Simulation result of 3 Stage Carry Select Adder

7.1.6 4 STAGE CARRY SELECT ADDER

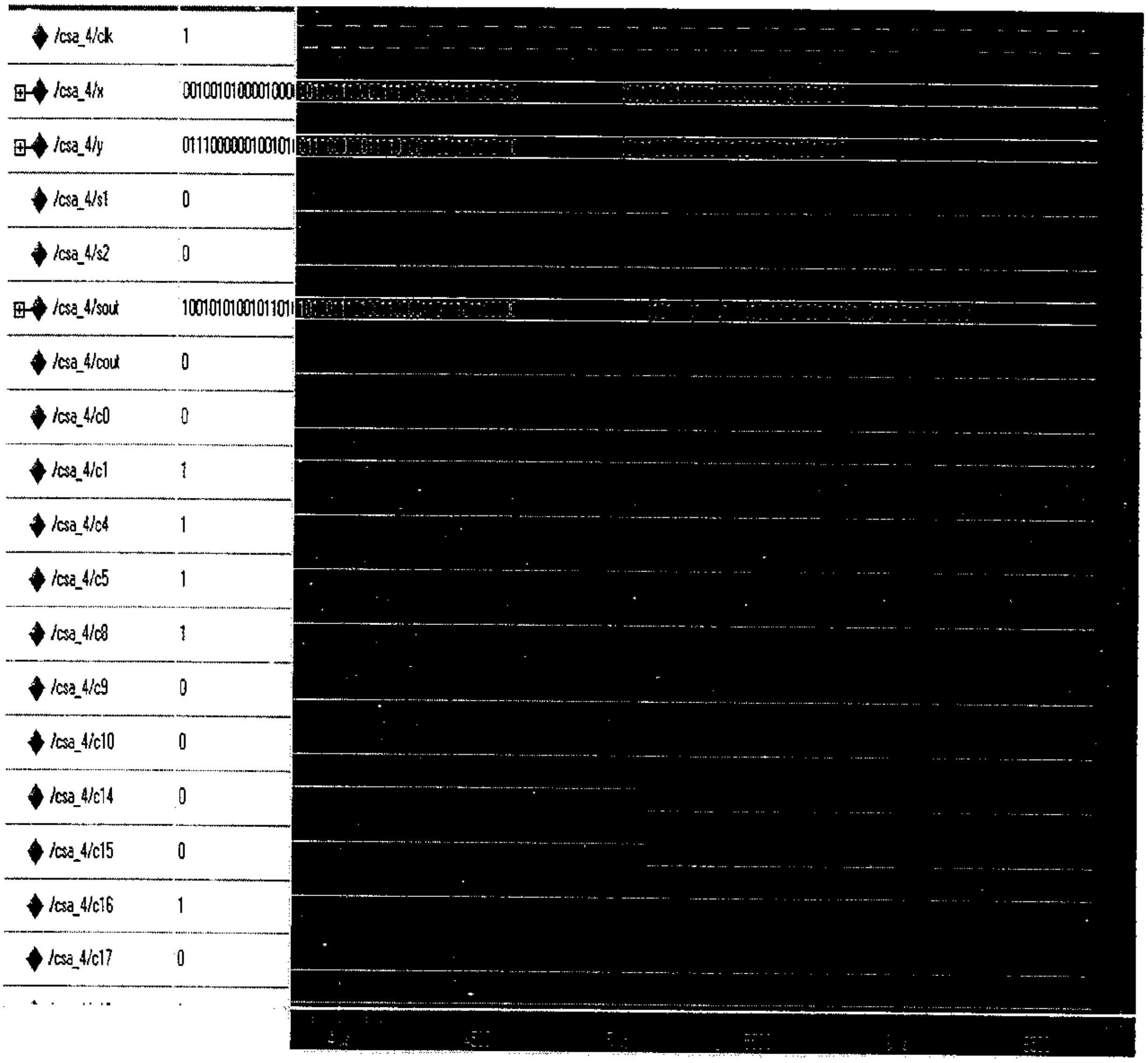


Figure 6.6 Simulation result of 4 Stage Carry Select Adder

7.1.7 CLOCK SELECT ADDER WITH SHARING

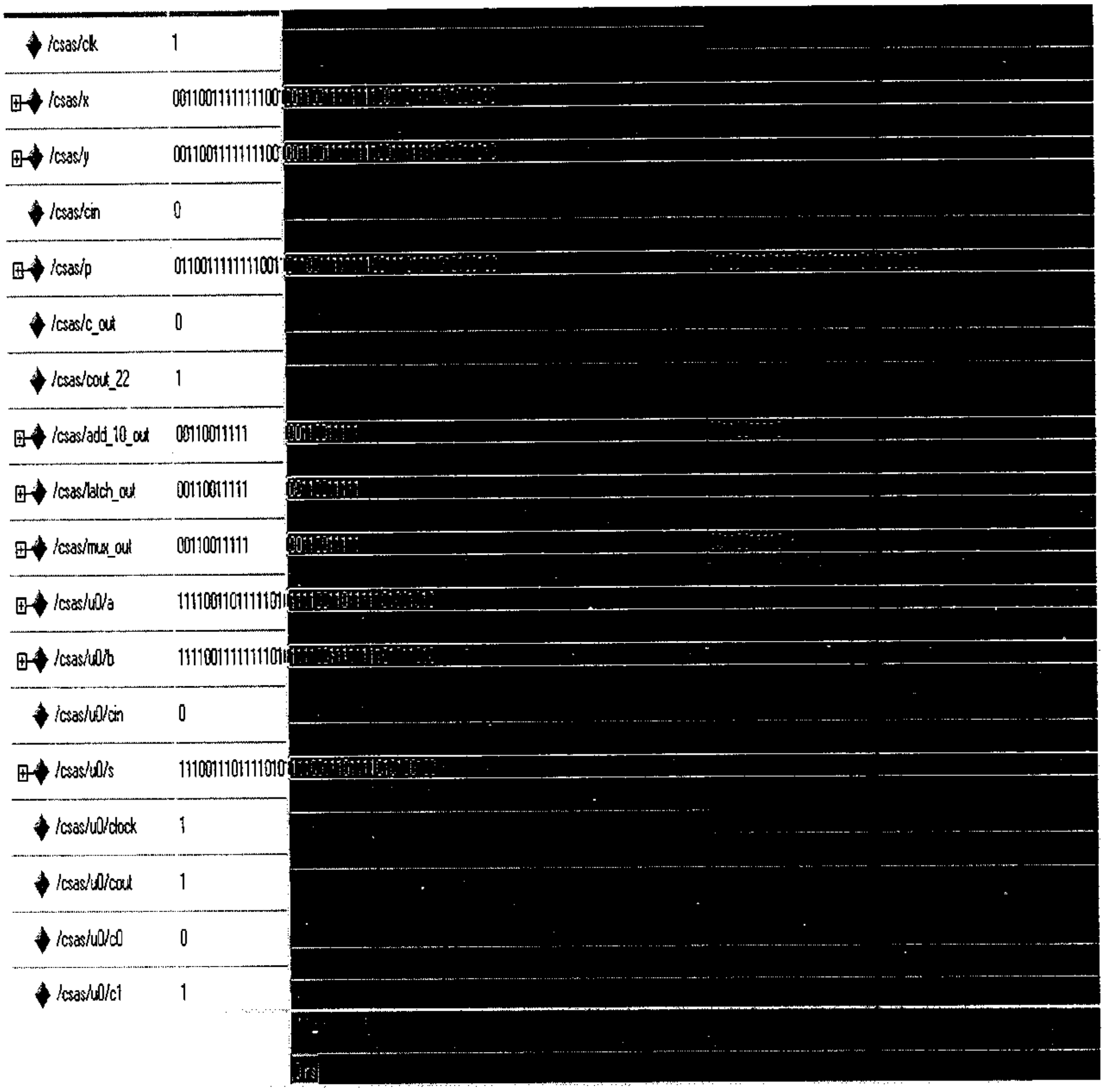
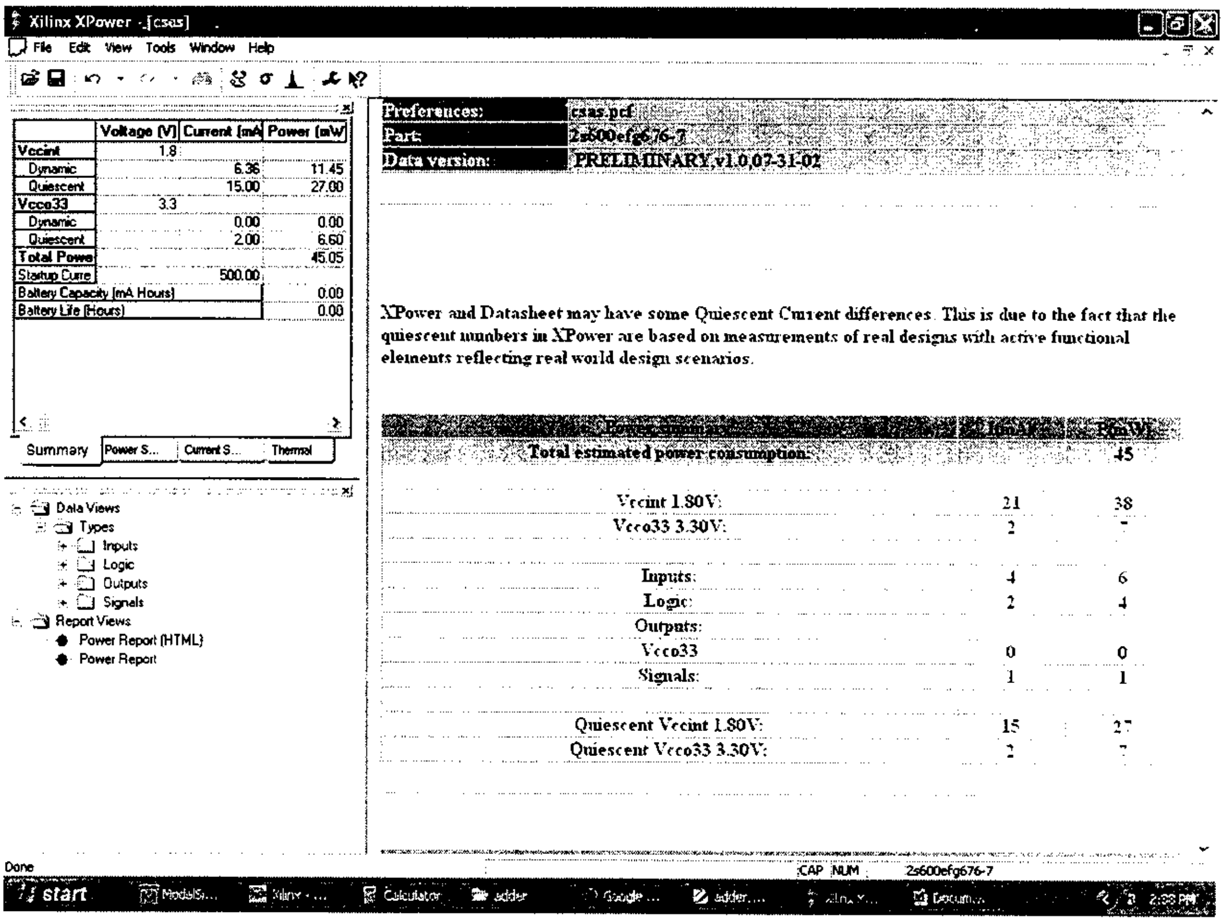


Figure 6.7 Simulation result of Clock Select Adder with Sharing.

7.2 SYNTHESIS REPORT:

7.2.1 CLOCK SELECT ADDER WITH SHARING:

POWER REPORT:

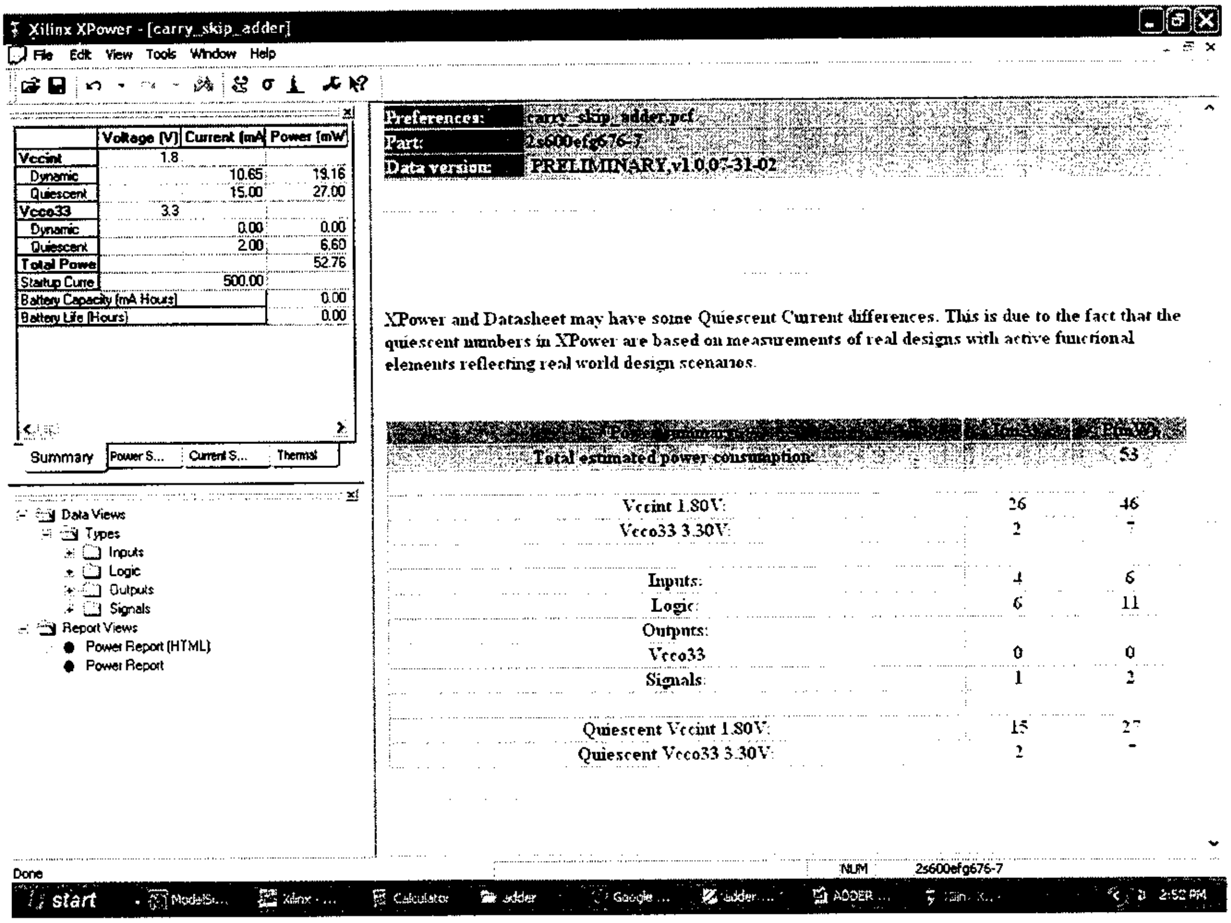


MAP REPORT:

Number of Slice Latches	:	1 out of 13,824 1%
Number of 4 input LUTs	:	42 out of 13,824 1%
Number of Slices containing unrelated logic	:	0 out of 25
Number of bonded IOBs	:	66 out of 510 12%
Total equivalent gate count for design	:	257

7.2.2CARRY SKIPADDER:

POWER REPORT:

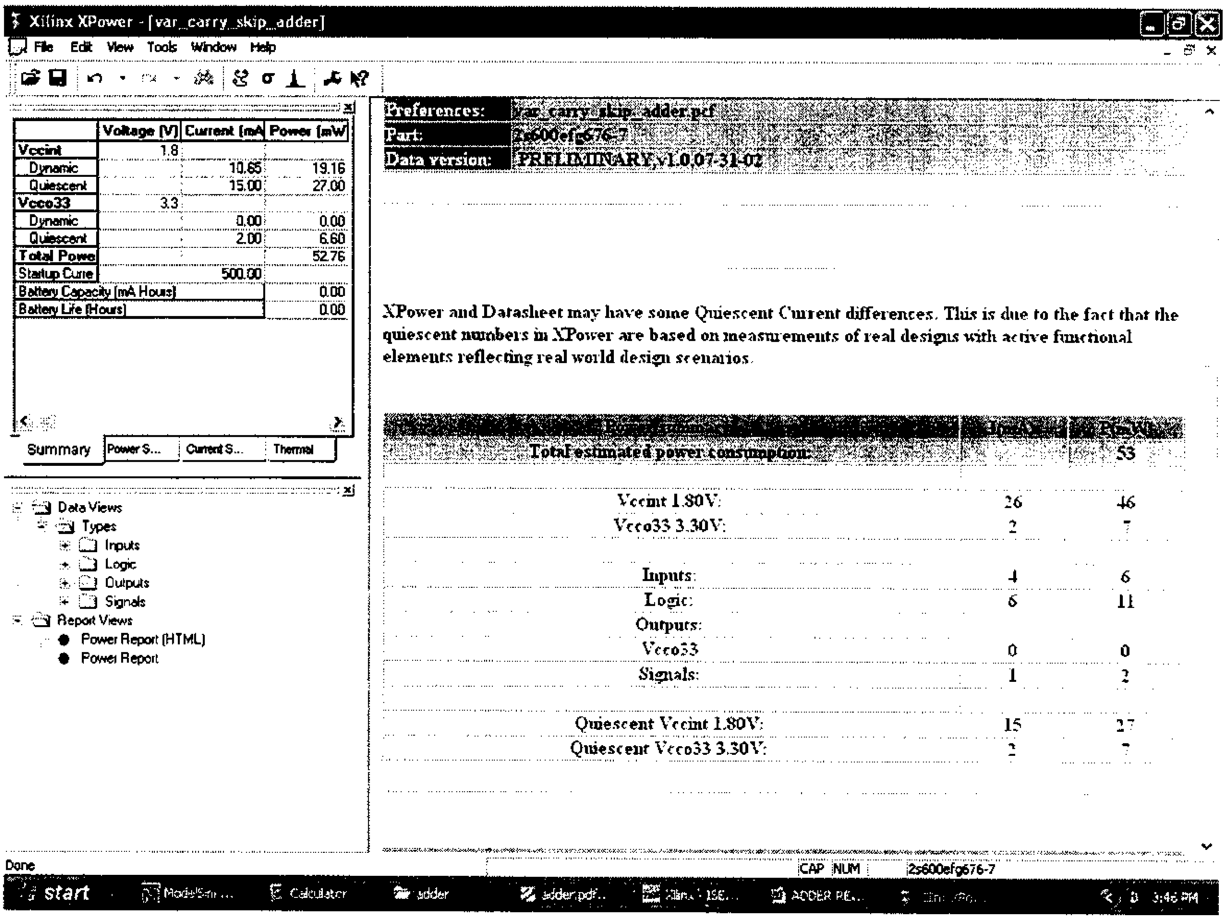


MAP REPORT:

Number of 4 input LUTs	:	65 out of 13,824 1%
Number of occupied Slices	:	48 out of6,912 1%
Number of Slices containing unrelated logic	:	0 out of 48 0%
Number of bonded IOBs	:	98 out of 510 19%
Total equivalent gate count for design	:	390

7.2.3 VARIABLE CARRY SKIP ADDER:

POWER REPORT:

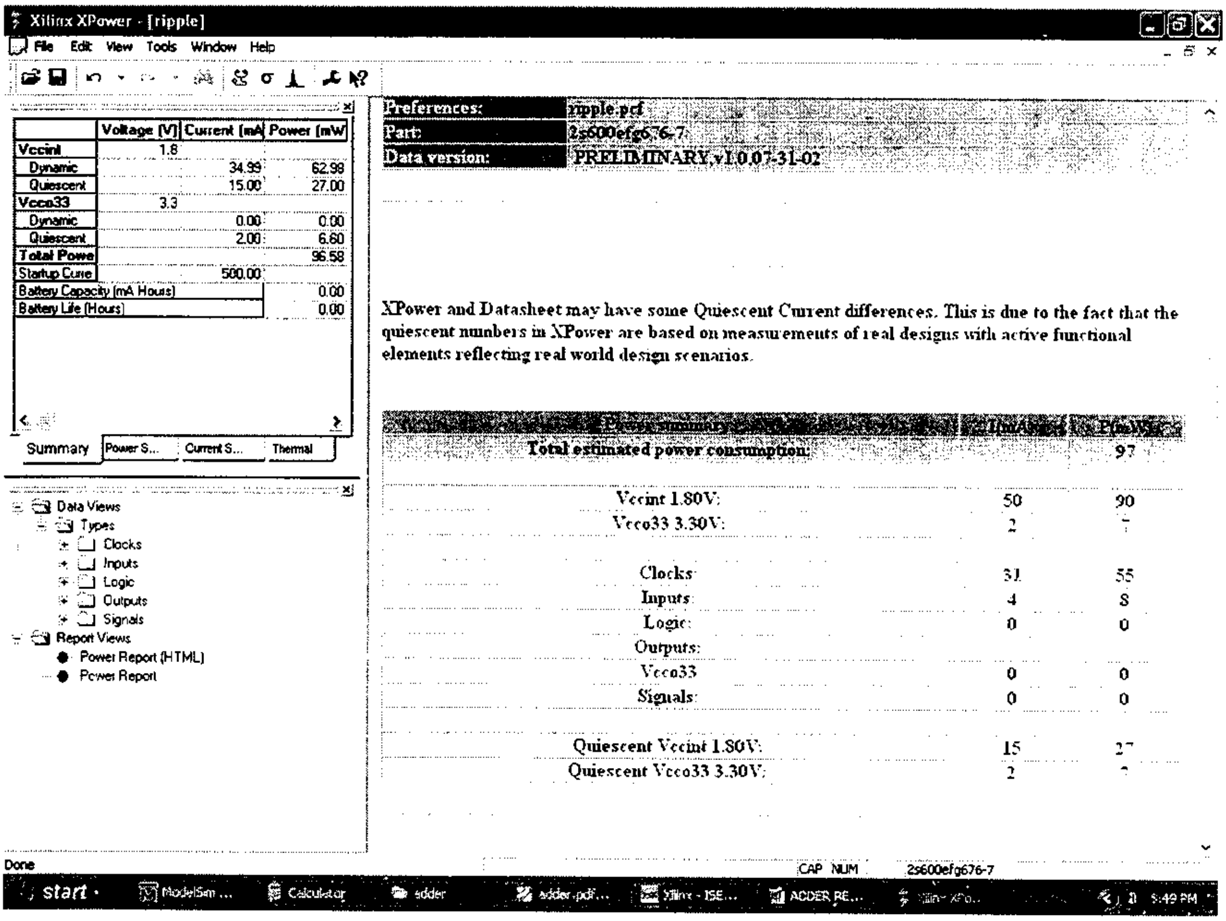


MAP REPORT:

Number of 4 input LUTs	:	65 out of 13,824 1%
Number of occupied Slices	:	48 out of 6,912 1%
Number of Slices containing unrelated logic	:	0 out of 48 0%
Number of bonded IOBs	:	98 out of 510 19%
Total equivalent gate count for design	:	390

7.2.4 RIPPLE CARRY ADDER:

POWER REPORT:

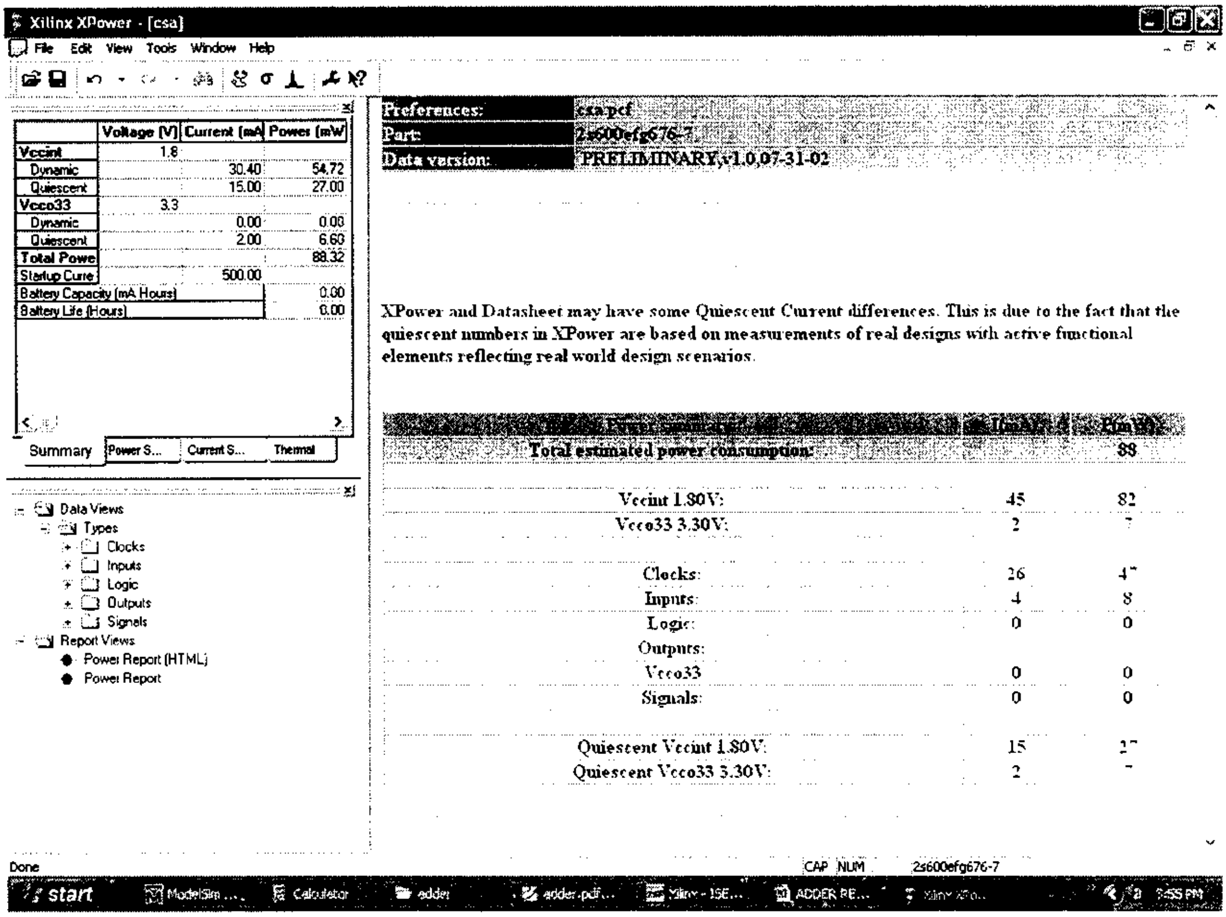


MAP REPORT:

Number of 4 input LUTs	:	64 out of 13,824 1%
Number of occupied Slices	:	32 out of 6,912 1%
Number of Slices containing unrelated logic	:	0 out of 32 0%
Number of bonded IOBs	:	97 out of 510 19%
Total equivalent gate count for design	:	896
Additional JTAG gate count for IOBs	:	4,704

7.2.5 CARRY SELECT ADDER:

POWER REPORT:

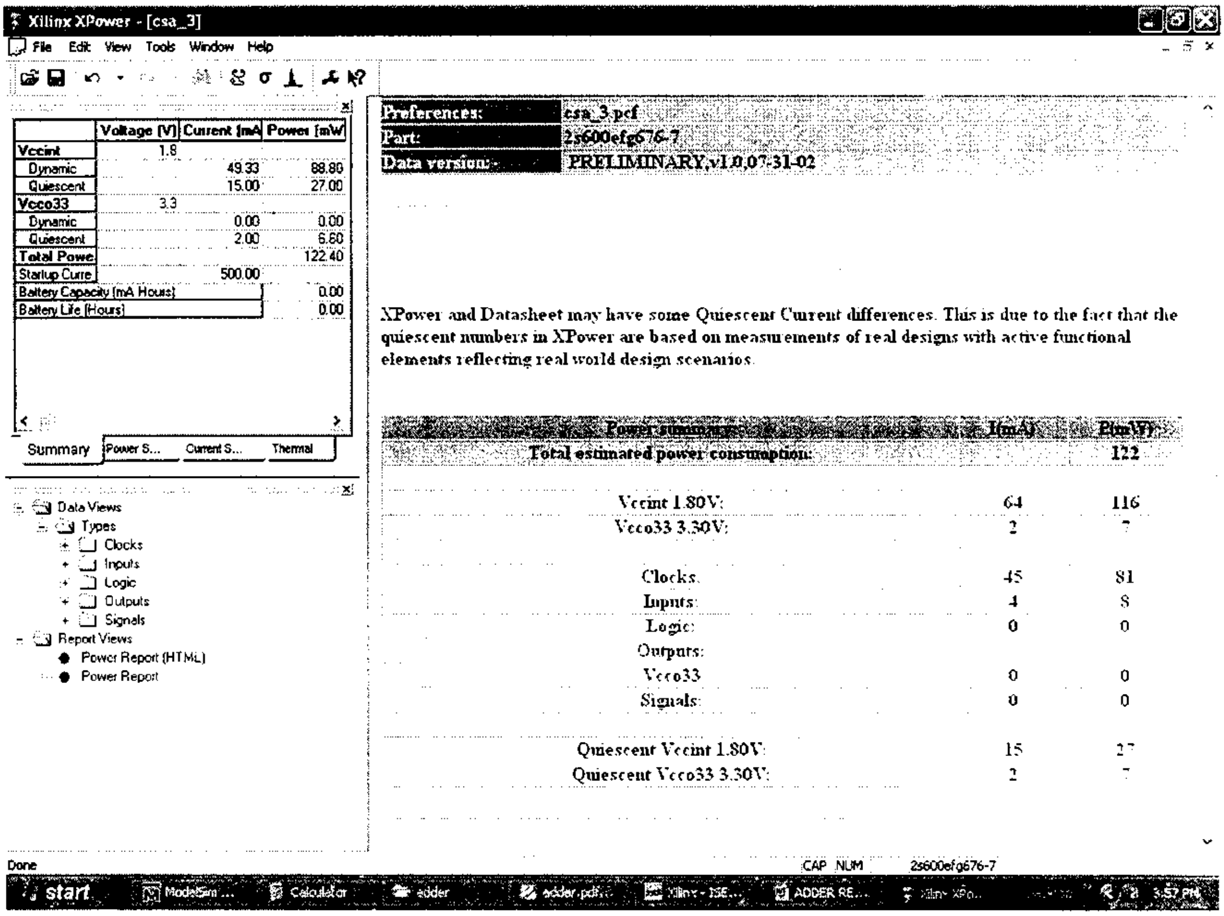


MAP REPORT:

Number of Slice Flip Flops	: 31 out of 13,824 1%
Number of 4 input LUTs	: 64 out of 13,824 1%
Number of occupied Slices	: 32 out of 6,912 1%
Number of bonded IOBs	: 97 out of 510 19%
IOB Flip Flops	: 33
Total equivalent gate count for design	: 896

7.2.6 3 STAGE CARRY SELECT ADDER:

POWER REPORT:

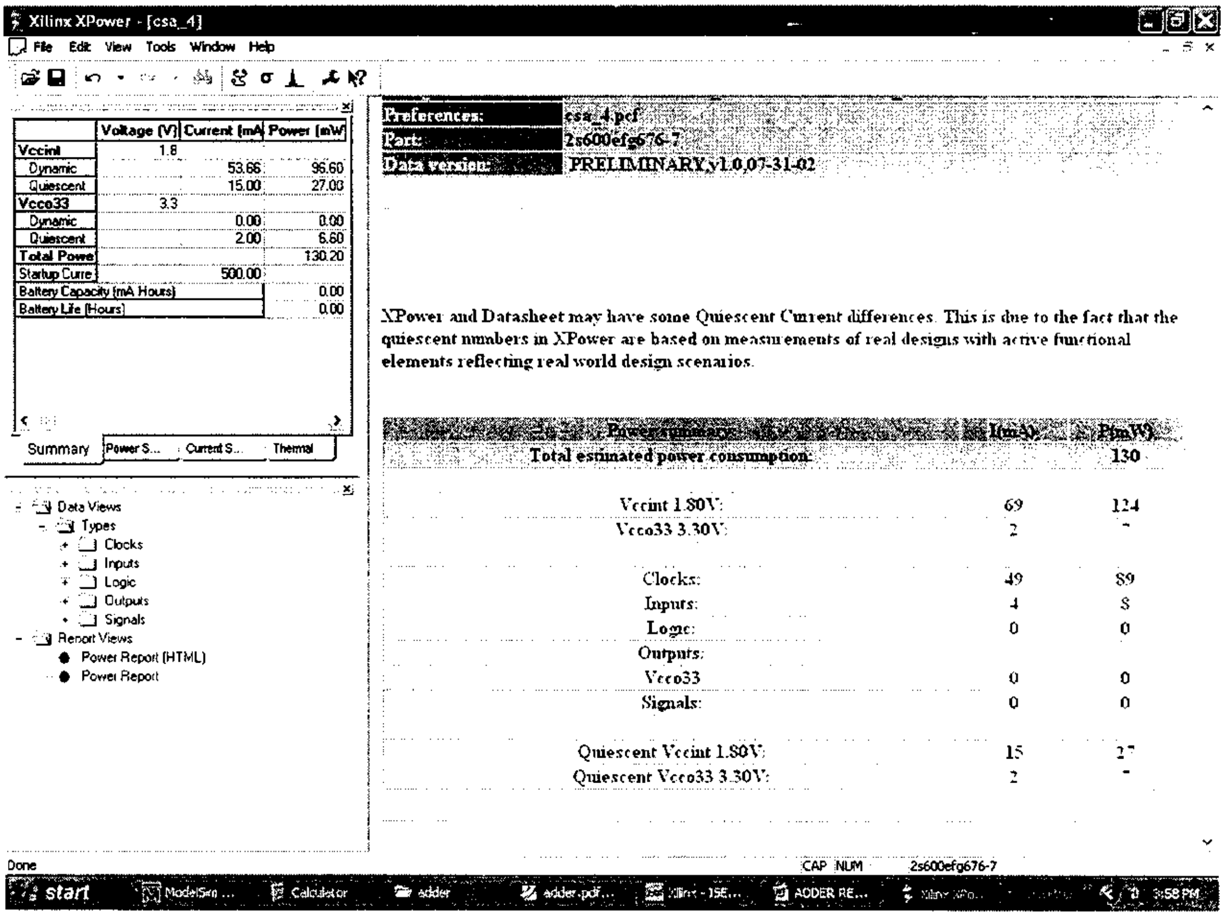


MAP REPORT:

Number of Slice Flip Flops	:	105 out of 13,824 1%
Number of 4 input LUTs	:	150 out of 13,824 1%
Number of occupied Slices	:	77 out of 6,912 1%
Number of Slices containing unrelated logic	:	0 out of 77 0%
Number of bonded IOBs	:	98 out of 510 19%
IOB Flip Flops	:	9
Total equivalent gate count for design	:	1,851

7.2.7 4 STAGE CARRY SELECT ADDER:

POWER REPORT:



MAP REPORT:

Number of Slice Flip Flops	:	103 out of 13,824 1%
Number of 4 input LUTs	:	146 out of 13,824 1%
Number of occupied Slices	:	74 out of 6,912 1%
Number of Slices containing unrelated logic	:	0 out of 74 0%
Number of bonded IOBs	:	99 out of 510 19%
IOB Flip Flops	:	9
Total equivalent gate count for design	:	1,796

7.3 COMPARISON BETWEEN ADDERS:

Parameters	Ripple carry adder	Carry Skip adder	Variable Carry skip adder	Carry Select adder	Clock Select adder with sharing
LUT'S	64/13824	65/13824	65/13824	64/13824	42/13824
Bonded IOB's	97/510	98/510	98/510	97/510	66/510
Gate count	896	390	390	896	257
Dynamic Power	97mW	53mW	53mW	88mW	45mW

Table 1.1 Comparison between adders

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

This project presents modified carry select adder is better in reduced area and low power consumption. These adders are faster than ripple carry adder but slower than the carry select adder. Whenever there is need of small area and low power consumption, while some delay can be tolerated, such design can be used. 28.68 percentage of area reduced in modified carry select adder when compared with ripple carry adder. 46.39 percentage of power reduced in modified carry select adder when compared with ripple carry adder

FUTURE SCOPE

For further to explore in this project, the adder can be designed in a way to reduce the delay along with power and area reduction.

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