DEVOLPMENT OF TEST STRATERGY FOR ANALOG CIRCUITS

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BONAFIDE CERTIFICATE

Certified that this project report entitled "**DEVOLPMENT OF TEST STRATERGY FOR ANALOG CIRCUITS**" is the bonafide work of Ms.P.M.Sneha Angeline [Reg. no. 1020106017] who carried out the mini project under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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ABSTRACT

The analog and mixed signal circuits are embedded system-on-chip.The integrated circuit (IC) fabrication involves several process .The imperfection in any of these fabrication process affects the performance of the mixed signal circuits, since these circuits are very sensitive.testing assures the product flawless and improves the quality of the product. the test methodolgies for digital circuits are well developed compared to the analog circuits. the test methods for analog circuits includes design for testability (dft),built in self test(bist),oscillation based built in self test(obist).

Dft adds testability feature to the circuit. It involves expensive test equipment which produce long test time thereby increase the test cost. test programmes are executed in automatic test equipment. bist makes the electrical testing of a chip easier, faster and more efficient. it reduces the dependence on external automated test equipment which produce less test cost and test time is reduced as more structures can be simulated in parallel .obist is a defect identifying technique which does not require stimulus generators and minimize the external test pins thereby enhancing the observability of the faults and controllability of the test procedure.

Through the ***DEVOLPMENT OF TEST STRATERGY FOR ANALOG CIRCUITS,*** it is planned to obtain an efficient fault coverage for the circuit under test(CUT).The CUT is converted into an oscillator and simulated to obtain a fault free test parameters. The faults are injected for the same CUT and simulated to obtain faulty test parameters. The fault is detected by comparing the two test parameters and the fault coverage is calculated. The circuit is simulated using TANNER software.

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LIST OF ABBREVIATIONS

IC	-----	Integrated Circuit
SOC	-----	System On Chip
CUT	-----	Circuit Under Test
DFT	-----	Design For Testability
BIST	-----	Built In Self Test
OBIST	-----	Oscillation Based Built In Self Test

CHAPTER 1

INTRODUCTION

With the growing use of analog circuits in commercial mixed-signal integrated circuits and system, testing of analog integrated circuits is considered as one of the most important problems in analog and mixed-signal integrated circuit design. Analog circuits have traditionally been tested for critical specifications. The performance of mixed signal ICs will be greatly degraded, since these circuits are very sensitive to even small imperfections in any step of the fabrication process. In the digital circuit domain, however, some of these faults may be rather unimportant, but in mixed-signal circuits, imperfection in the form of small capacitance between the traces can present a significant circuit-parameter variation, thereby changing the circuit behavior drastically. The testing improves the overall quality of the final product, although it has no effect on the ICs' manufacturing excellence. Furthermore, the testing assures the product flawlessness when implemented during the key phases of a product development.

The test methodologies for digital devices are already well developed compared to analog-test methods are still so underdeveloped due to the lack of accepted test principle such as standard fault model for analog components. Almost all the digital test techniques are based on single stuck-fault model, and the test generation algorithms are evaluated by their fault coverage. The main sources of test difficulties in digital and analog circuits are also different; for example, the size and complexity in digital circuits remain a measure of test difficulty, whereas in analog and mixed-signal circuits, the behaviors of circuit signals are much more important than circuit sizes. A major problem in the analog and mixed signal circuit testing is in defining the line of demarcation between a fault-free and faulty circuit, resulting in uncertainty of quantification of the product yield.

1.1 OVERVIEW OF THE PROJECT

The oscillation based built in self test is able to operate without a test stimulus generator .This test allows several parts of the chip to be tested in parallel, thereby reducing the required testing time. It enhances the observability of the faults and controllability of test procedure. This effective testing methodology is incorporated in this project the circuit is converted into oscillator and simulated for fault free condition .The faults such as stuck open and stuck short are injected in the circuit under test and simulated for faulty condition. The deviations in the test observables such as oscillation frequency and output voltage are used to calculate the fault coverage.

1.2 TESTING METHODOLOGY

The proposed test methodology shown in Fig. 1.1 consists of first partitioning the analog mixed-signal integrated circuit into functional building blocks such as amplifier, comparator, filter, and data converter and then converting each building block into an oscillating circuit by adding the proper circuitry in order to achieve sustained oscillation and the oscillation parameters are evaluated. The oscillation parameters can be the frequency, output voltage amplitude, distortion, or dc level of the output signal. The circuit's output is connected to its input via a passive and/or active analog circuit such that, the loop's overall gain and phase cause oscillation. The faulty circuit is detected from a deviation of its oscillation parameters with respect to the oscillation parameters under fault-free conditions if the oscillation frequency lies close to the nominal frequency range, the CUT is accepted to be fault-free.

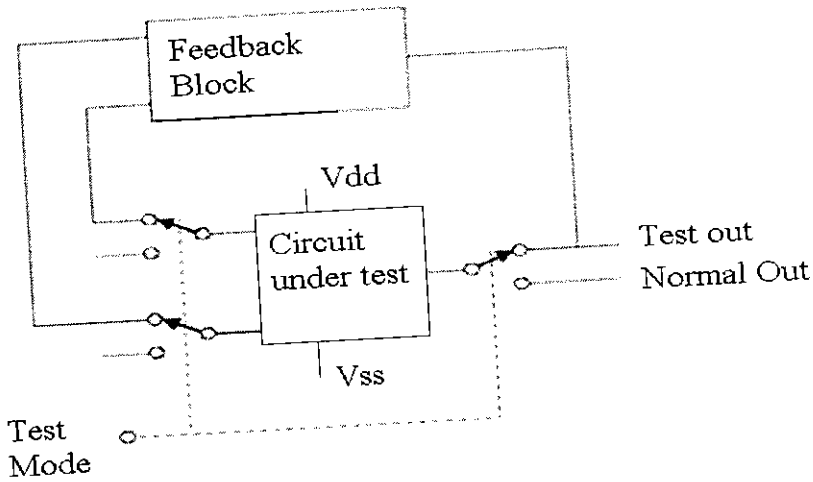


FIGURE 1.1 BLOCK DIAGRAM OF THE PROPOSED TEST STRATERGY

1.3 ADVANTAGES OF OBIST

The OBT is an analog and mixed-signal testing technique which can be used in conventional off-line testing or as the core of the so-called OSCILLATION BASED BUILT IN SELF TEST (OBIST).In high complexity analog and mixed-signal systems, where the accessibility to the system internal nodes is critically restricted and where there is a extremely limited number of test pins, the best option is to implement OBT by means of a BIST approach. Therefore, an OBIST would allow not only to minimize the number of external test pins, but also to enhance the observability of the faults and the controllability of the test procedure. The main objectives:

- An on-chip stimulus generation.
- An on-chip control of the test strategy (test circuitry, test configurations, test facilities, etc).

Many BIST structures need specific test stimulus generators. But, the implementation of an on chip stimulus generator normally requires a note worthy investment in hardware. It becomes very critical in some cases, not only because of the involved additional area which can increase significantly the production cost, but also

OBIST, test generation, test application and response verification are all accomplished through built-in hardware, which allows different parts of a chip to be tested in parallel, thereby reducing the required testing time, besides eliminating the necessity for external test equipment. This method does not require extensive modifications of the CUT for testing. It can be used at all levels of testing.

1.4 SOFTWARE USED

- Tanner Tool.
- Technology Used = 0.25μm

1.5 CHAPTER ORGANIZATION

In the following chapters, the methodology, circuit design in normal and oscillation mode is presented. Simulation results are discussed.

Chapter2 Explains the basic structure and operation of a CMOS inverter. It also explains the methodology for oscillation testing, converting the CUT into an oscillator and injecting the faults. The functionality test for a CMOS inverter is also presented.

Chapter 3 Explains the basic structure and operation of a MOS amplifier with series shunt feedback. The circuit is tested by obtaining the frequency response in fault free condition and by injecting faults the deviation in the response is studied.

The two stage op amp in normal mode is tested for the specification parameters.The voltage follower circuit is simulated for fault free condition and the stuck short fault is injected and the deviation in the parameters are observed.

Chapter 4 Provides a conclusion and future scope of the work presented.

Appendix Presents the MOS model parameters used for the design.

CHAPTER 2

DESIGN FOR TEST OF A CMOS INVERTER IN OSCILLATION MODE

2.1 CMOS INVERTER

CMOS inverter is a device that is capable of producing logic functions and is the primary component of all integrated circuits. CMOS inverters also produce very little heat dissipation, making them highly efficient and resulting in very little power consumption. Additionally, CMOS inverters have high noise immunity and block both incoming and outgoing frequency spikes, and are inexpensive to produce. The functionality of the CMOS inverter is tested. The CMOS inverter is designed in standard .25μm CMOS technology.

2.1.1 CMOS INVERTER IN OSCILLATION MODE

The n-channel MOS (NMOS) and p-channel MOS (PMOS) complementary transistors pair forms a CMOS inverter, with the transistor gates connected together as input and drains connected together as an output. To obtain the symmetric characteristics, it is necessary to make the PMOS device wider than NMOS such that the threshold voltage becomes Vcc/2. To oscillate the CMOS inverter circuit (Fig 2.1), CMOS astable-oscillator concepts are employed. The resistor $R1$ connects the output of the CMOS inverter (CUT, in this case) to its input and thus acts as dc negative feedback. The output of the CUT is connected to the input of another inverter U1 directly. The output of U1 is connected to the input of the CUT through a capacitor. This provides positive ac feedback. It is considered that the input of the CUT is zero; then, the output of the inverter U1 is low, and there is no charge stored in the capacitor. The capacitor begins to charge through the resistor $R1$, since the input impedance of the CMOS inverter is quite large. As soon as the capacitor voltage exceeds the threshold voltage of the CUT, Vth(Vth

The voltage across a capacitor is continuous; therefore, the voltage difference between the two sides of the capacitor must remain at Vcc/2. That means, when one side of the capacitor jumps to Vcc from zero, the other side must jump to 3Vcc/2. The voltage Vcc/2 appears on common node of $R1$ and $C1$, whereas the other node of $R1$ is zero so that the capacitor starts to discharge through $R1$. As soon as the voltage across $R1$ reaches the threshold voltage Vth, the output of the CUT transits to Vcc, and the output of the inverter U1goes to zero. The voltage at the common node of $R1$ and $C1$ is then pulled to $-V$cc/2. Thus, the capacitor $C1$ starts to charge toward Vcc.The cycle continues to produce a square-wave output. The oscillation frequency of the simulated circuit is obtained as $f$osc= 86.95Hz.

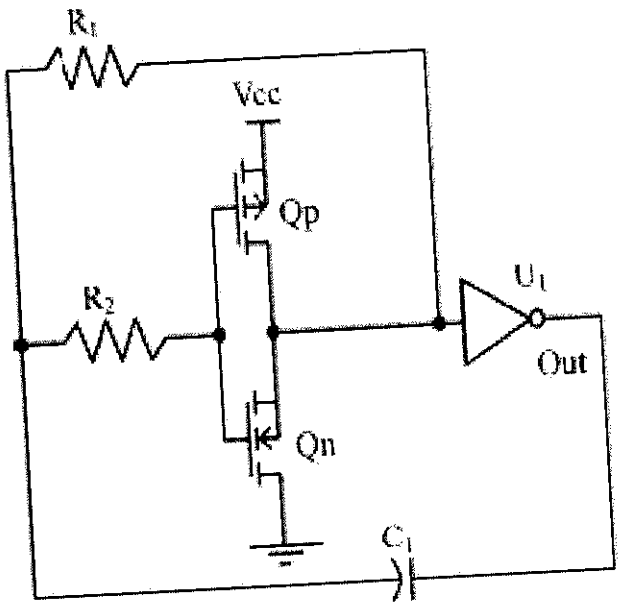


FIGURE 2.1 CMOS INVERTER IN OSCILLATION MODE.

2.1.2 FREQUENCY DETERMINATION

The frequency of oscillation can be determined as follows:

During the time interval t1, when the output is low, the voltage across the capacitor C1(vc) rises from –Vcc /2 to Vth. Substituting vc = Vth = Vcc/2 at t = t1 results in

Also, during the time interval t2 when the output is high, vc falls from 3Vcc/2 to Vth. The exponential fall of vc can be described by

$$vc = 3Vcc/2e^{-t2/R1C1}.$$

Substituting vc = Vth = Vcc/2 at t = t2 results in

$$T2 = R1C1 \ln 3.$$

The period of output T can be achieved by summing t1 and t2 as

$$T = t1 + t2$$

$$T = 2R1C1 \ln 3 = 2.2R1C1.$$

The frequency of the oscillation is given by

$$fosc = 1/2.2R1C1.$$

By choosing R1 = 500 kΩ, C1 = 10 nF, and R2 = 5 MΩ, the oscillation frequency is calculated as

fosc = 90.9 Hz.

2.1.3 FAULT MODELS

Faults occurring in analog circuits can be categorized in two types: hard faults and soft faults. Hard faults or catastrophic faults are those faults that cause the circuit performance to differ catastrophically from normal conditions. Catastrophic fault model is the same as stuck-fault model used in the digital test domain where every component can be either stuck-open or stuck-short. Stuck-open fault results when the terminal of an analog circuit component is not connected to the rest of the circuit, while stuck-short fault occurs when a short is created between the terminals of a component. On the other hand, soft or parametric faults refer to changes in a circuit that do not affect its connectivity, resulting in circuit functions out of specifications. The parametric faults can be modeled as variations of component parameters that are beyond their tolerance limits. The catastrophic faults are considered for the CMOS inverter. The standard fault models for capacitors, resistors, and MOS field-effect transistors (MOSFETs), are shown in the fig 2.2 where the parallel resistor *Rp* is 10 Ω that emulates stuck-short fault and that of the series resistor *Rs* is 100 MΩ that emulates stuck-open fault.

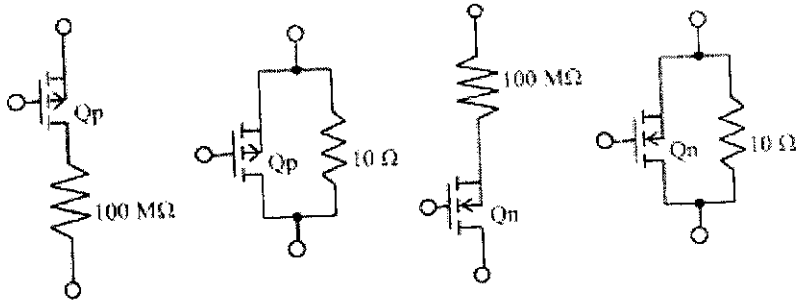
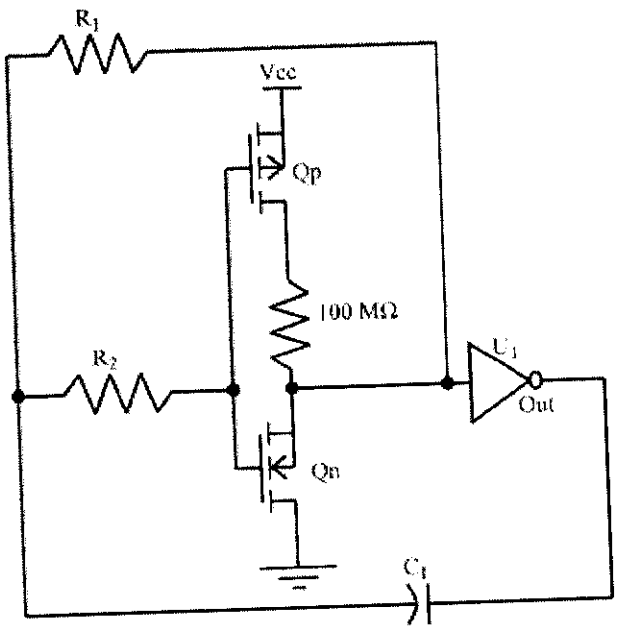


FIGURE 2.2 FAULT MODELS FOR PMOS AND NMOS TRANSISTORS OF INVERTER

2.1.4 STUCK OPEN FAULT

The circuit for testing stuck open fault of PMOS transistor Qp and NMOS transistor Qn is shown in the Fig 2.3 and Fig 2.4. The series resistor *Rs* of 100 MΩ is connected in series with Qp and Qn. Assuming that the input of U1 is +5 V, its output will be zero. First the capacitor *C*1 will start to charge through *R*1 until the gate voltage of Qn becomes more than *V*th (threshold voltage of Qn), or *V*gs ≥*V*th. Therefore, Qn will operate, and *V*ds of Qn will be zero from *V*ds = *V*gs − *V*th. Then, the output of *U*1 will turn high (+5 V) and stay high, since the drain of Qp has been disconnected and has no influence on the output of Qn. The similar operation is carried for stuck open Qn .



...TOR WITH STUCK-OPEN Qp

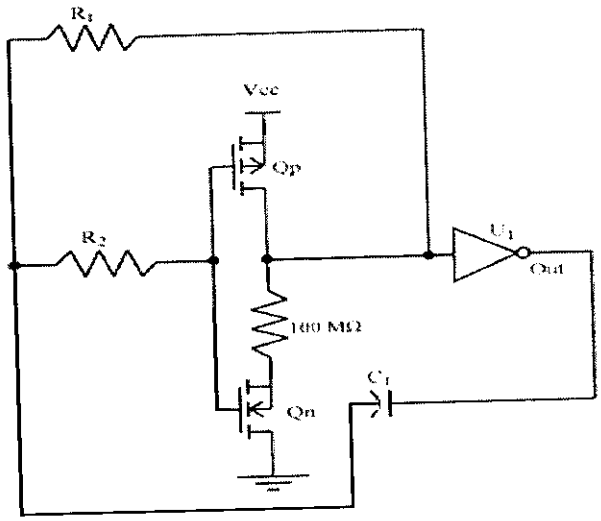


FIGURE 2.4 OSCILLATOR WITH STUCK-OPEN Q_N.

2.1.5 STUCK SHORT FAULT

The circuit for testing stuck short fault of PMOS transistor Qp is shown in the figure 2.13.1. The parallel resistor Rp of 10 is connected in parallel with Qp and Qn. This resistor causes a short between the drain of the PMOS and NMOS. Since the input of U1 is shorted to *V*cc, the output will always be zero.

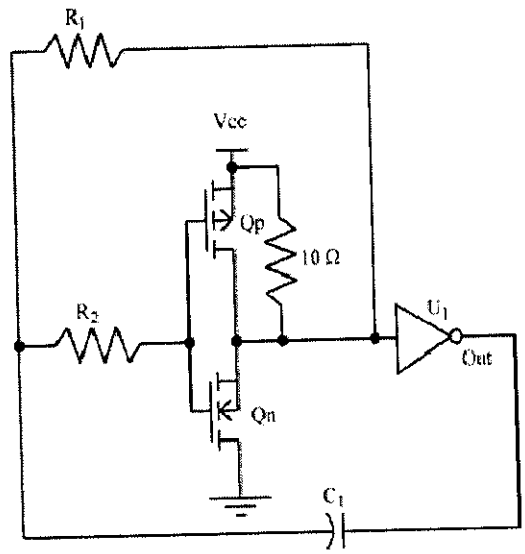


FIGURE 2.5 OSCILLATOR WITH STUCK-SHORT Q_P.

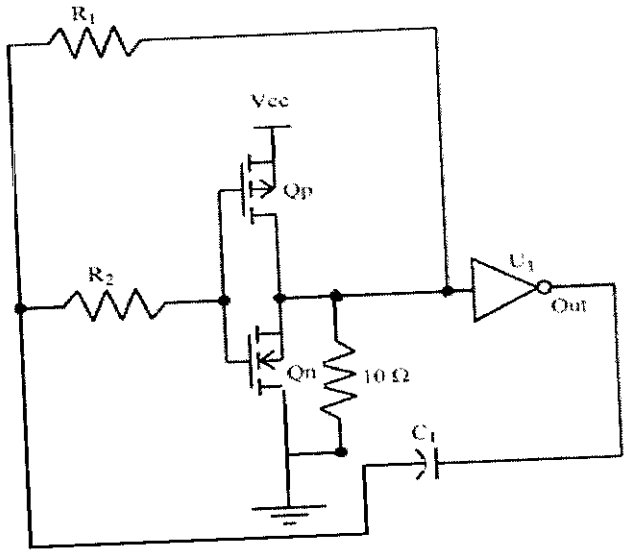


FIGURE 2.6 OSCILLATOR WITH STUCK-SHORT Q_N.

Fault Injected	**Output Voltage**
Stuck open Qp	5V
Stuck short Qp	0V
Stuck open Qn	0V
Stuck short Qn	5V

TABLE 2.1 OSCILLATION PARAMETERS OF THE FAULT MODELS

2.2 SIMULATION RESULTS

2.2.1 FUNCTIONALITY TEST FOR CMOS INVERTER

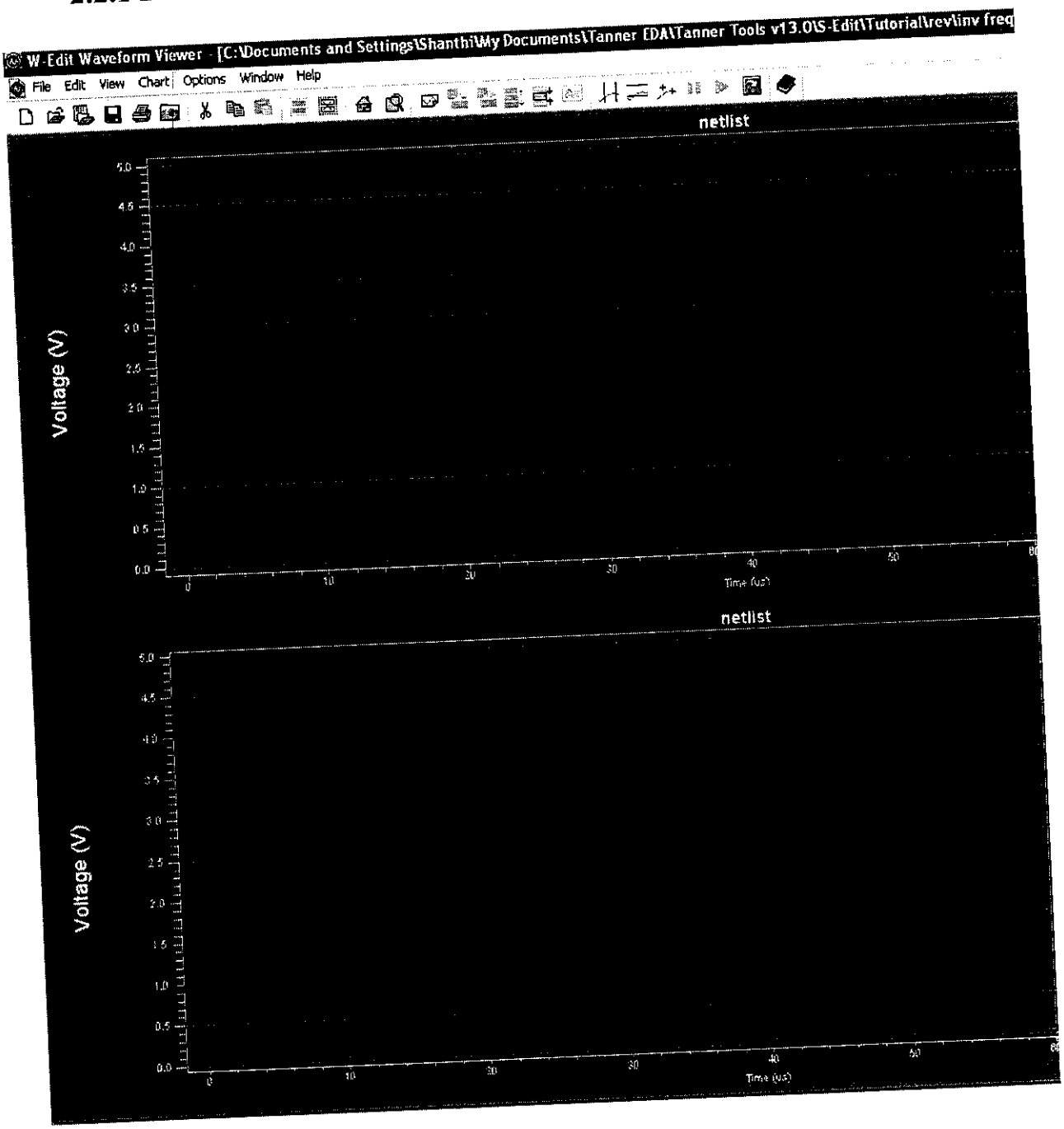


FIGURE 2.7 SIMULATION RESULT FUNCTIONALITY TEST FOR CMOS INVERTER

The input voltage of 5V is applied such that the output obtained is an inverted square pulse of 5V.

2.2.2 FAULT FREE CMOS INVERTER IN OSCILLATION MODE

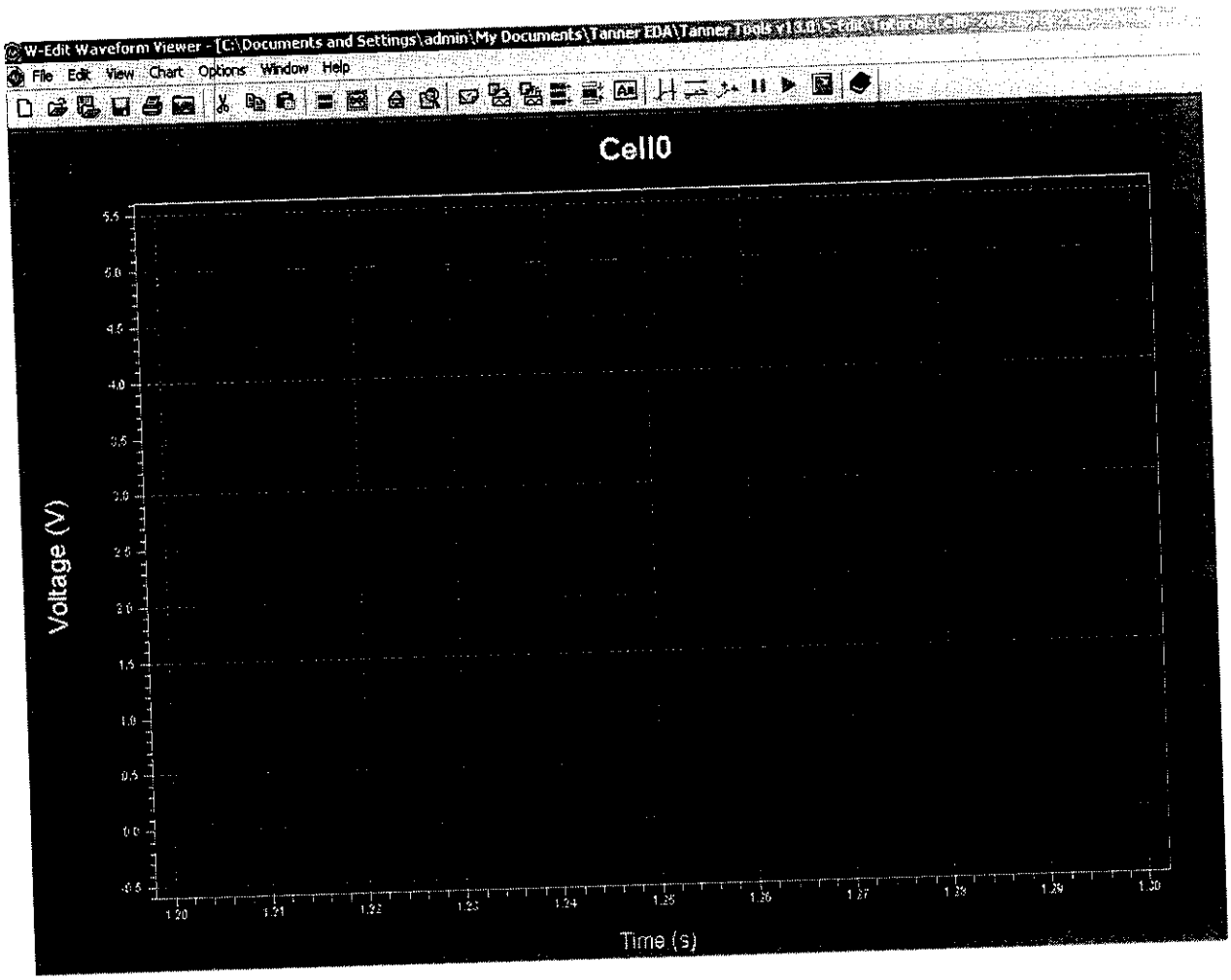


FIGURE 2.8 SIMULATION RESULT FOR FAULT FREE CMOS INVERTER

The fault free CMOS inveter produces a square wave output.The oscillation frequency of the simulated circuit is obatained as $f$osc = 100Hz which matches with the theoretical frequency of 90.9Hz.

2.2.3 STUCK OPEN FAULT IN Q_P

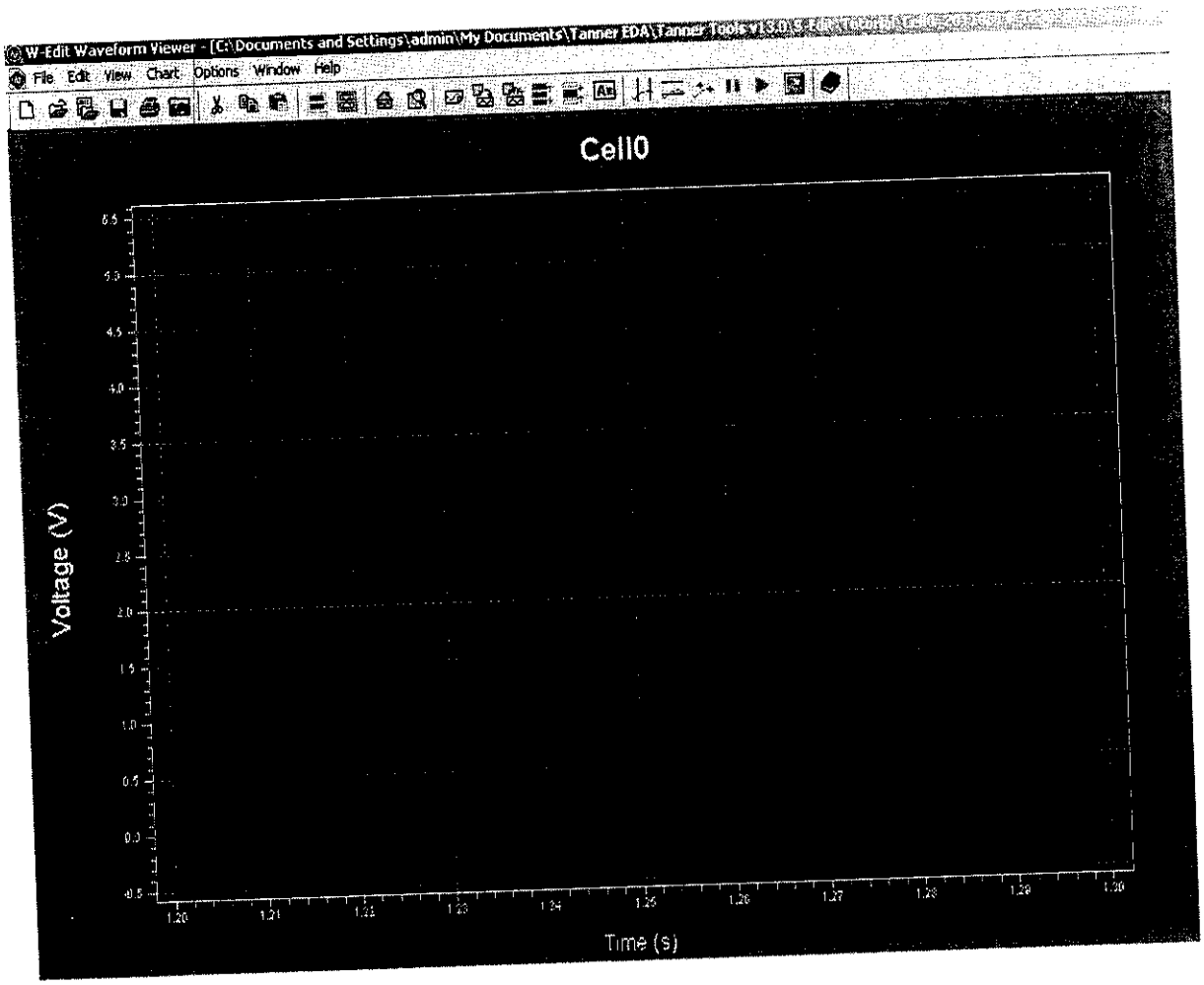


FIGURE 2.9 SIMULATION RESULT FOR STUCK OPEN FAULT Q_P

Stuck open fault in Qp transistor makes the output to stay always high.

2.2.4 STUCK SHORT FAULT IN Q_N

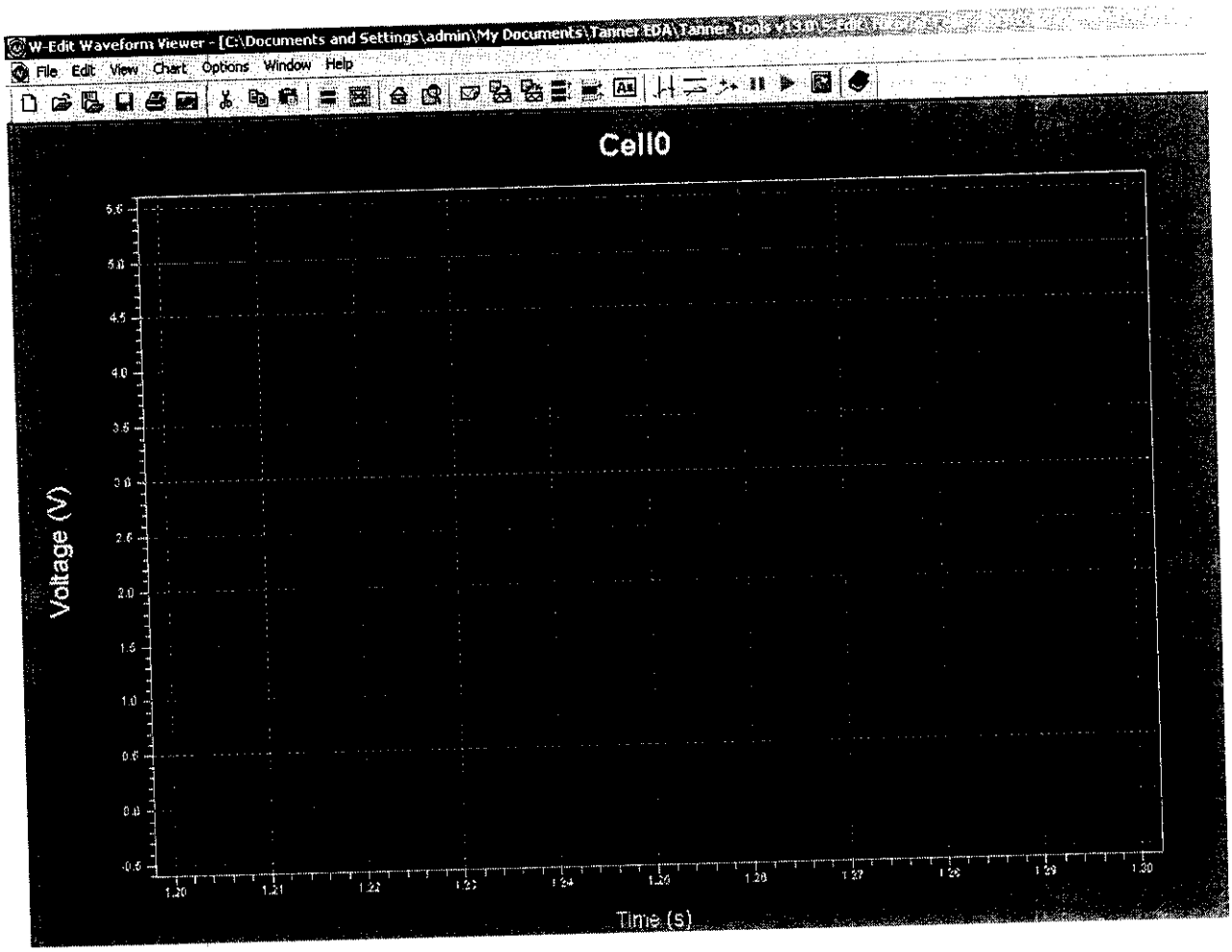


FIGURE 2.10 SIMULATION RESULT FOR STUCK SHORT FAULT Q_N

Stuck short fault in Qn transistor makes the output to stay always high.

In the similar manner stuck short fault in Qp and stuck open fault in Qn is tested and the output remains in zero volts.

CHAPTER 3

DESIGN FOR TEST FOR AN AMPLIFIER CIRCUIT

3.1 MOSFET SERIES SHUNT FEEDBACK AMPLIFIER

The series-shunt feedback means, the feedback signal is a voltage which is added in series with the input voltage and it is derived in parallel to the load impedance.The series feedback is used to improve the input return loss of low noise amplifiers and in parallel feedback path is introduced between the output and the input,parallel to the signal.The feedback signal must have a high-pass characteristic, because the DC potential at the gate and drain terminals of a FET are never equal.

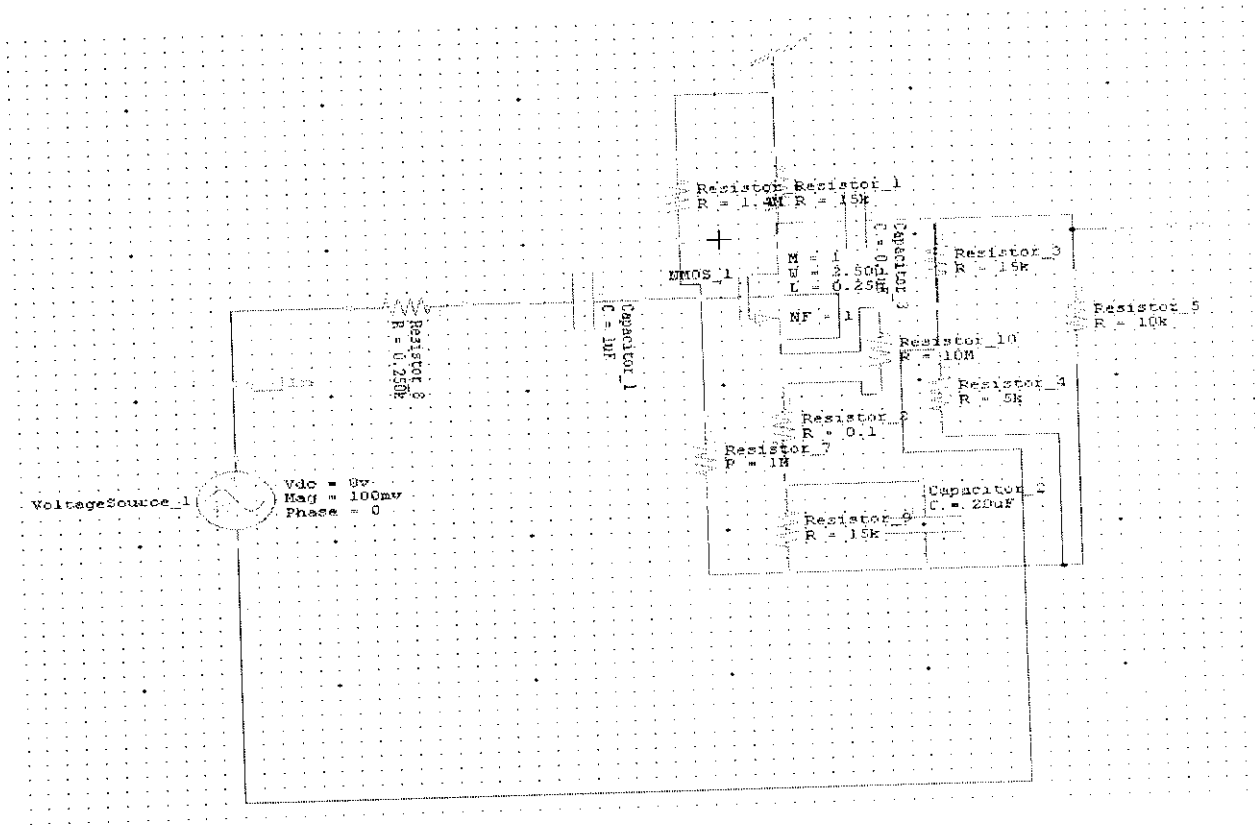


FIGURE 3.1 MOSFET SERIES SHUNT FEEDBACK AMPLIFIER

Frequency Response

The frequency response of any circuit is the plot of magnitude of the gain in decibels (dB) as a function of the frequency of the input signal. The voltage gain of an amplifier expressed in dB is 20 $\log_{10}|G|$, where $G = V_{out}/Vin$ for voltage gain. The modified frequency response after injecting stuck short fault for the MOSFET amplifier is shown in fig 3.3.

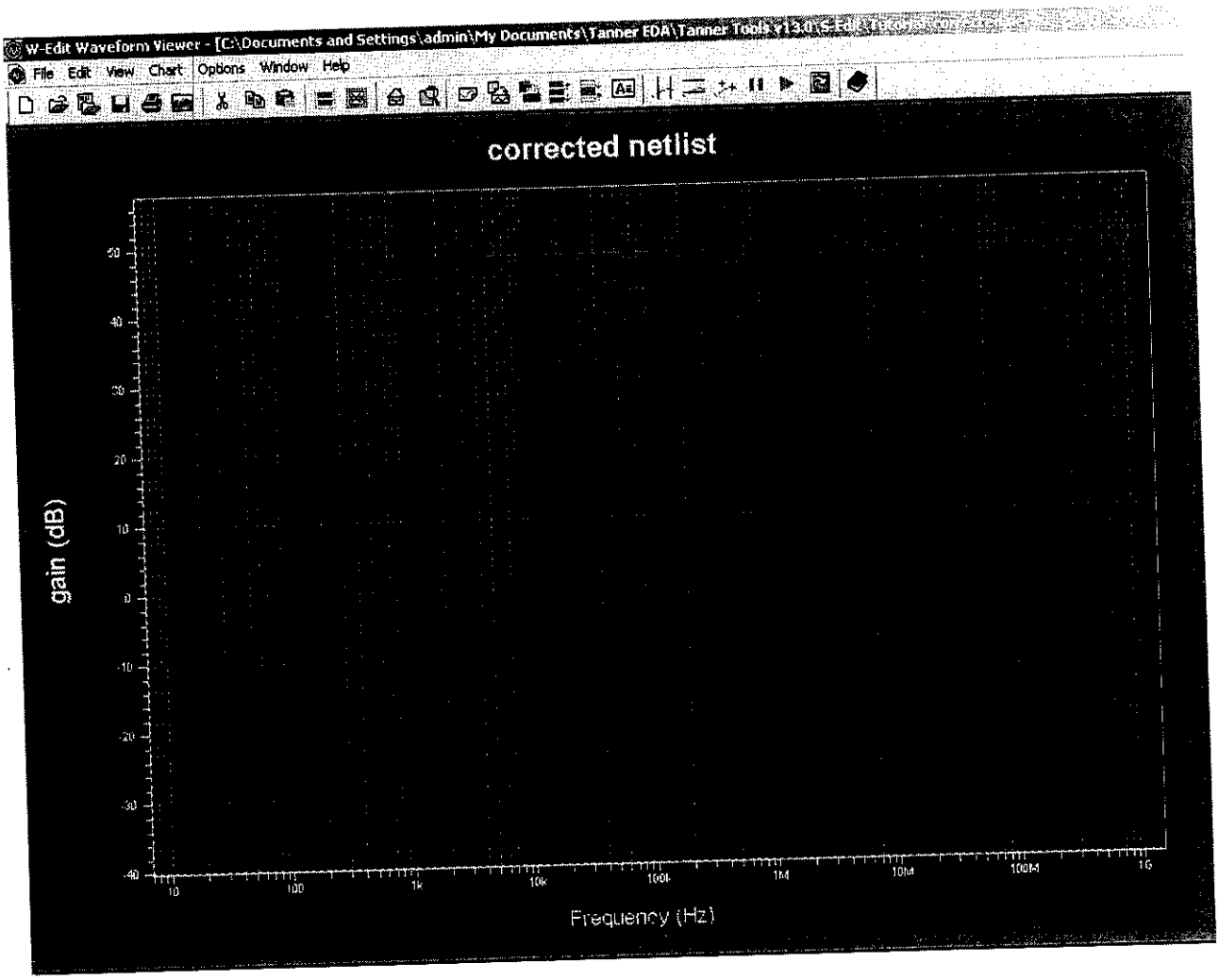


FIGURE 3.2 SIMULATION RESULT FOR FREQUENCY RESPONSE OF MOSFET AMPLIFIER

The fault free mosfet amplifier is simulated and the gain is obtained as 49db.

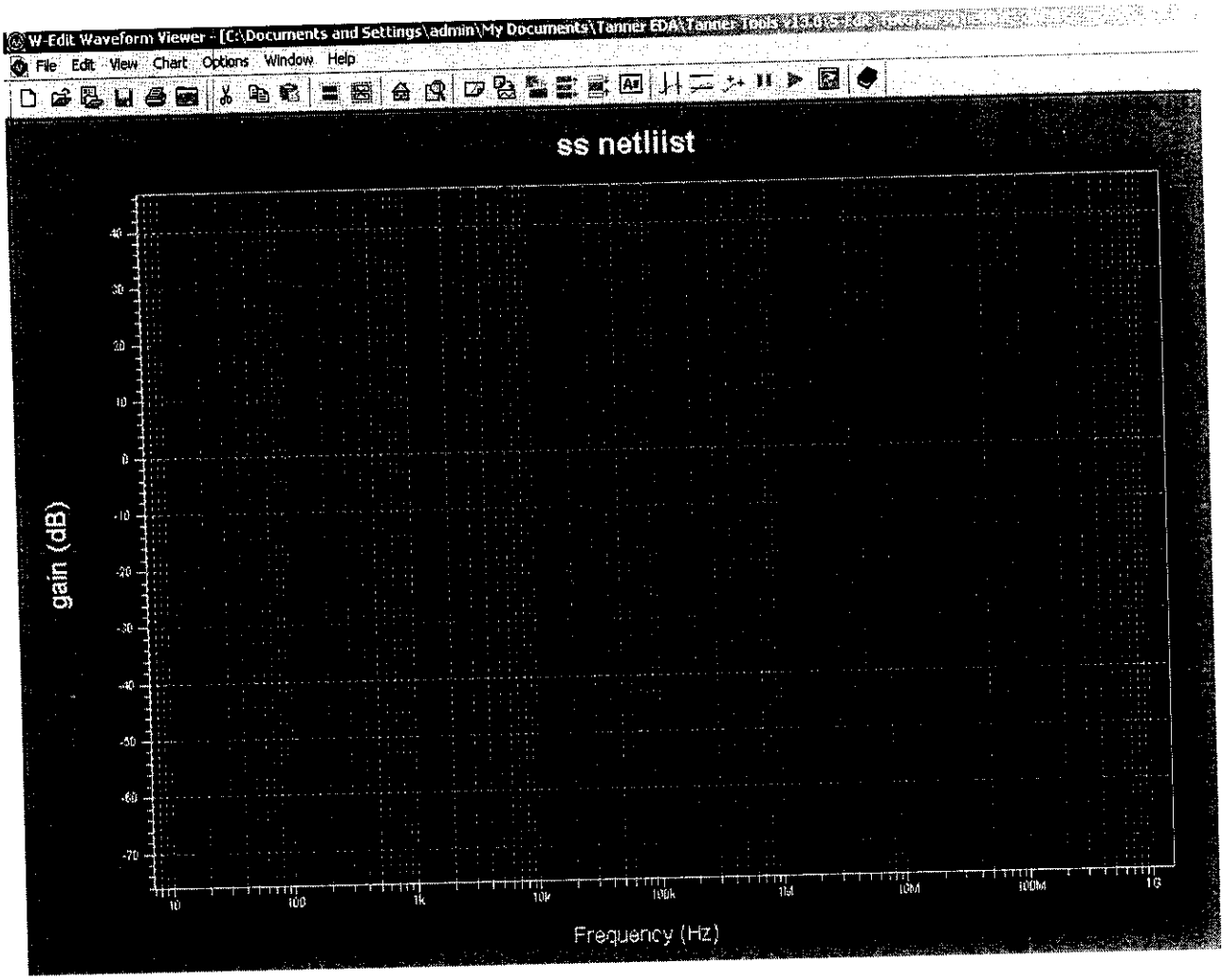


FIGURE 3.3 SIMULATION RESULT FOR FREQUENCY RESPONSE OF STUCK SHORT FAULT

The struck short fault is injected in the mosfet amplifier such that there is a drop in the gain.

3.2 CMOS OPERATIONAL AMPLIFIER

An ideal op-amp with a single-ended output has a differential input, infinite voltage gain, infinite input impedance and zero output impedance. Figure 2.3 shows the circuit diagram of a two-stage, internally compensated CMOS amplifier used for the testing. The circuit provides good voltage gain, a good common-mode range and good output swing. Before the analysis of the op-amp is done, some of the basic principles behind the working of MOS transistors are reviewed. The first stage in Fig. 2.3 consists of a p-channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M5.The second stage consists of an n-channel common-source amplifier M6 with a p-channel current-source load M7. The high output resistances of these two transistors equate to a relatively large gain for this stage and an overall moderate gain for the complete amplifier. Because the op-amp inputs are connected to the gates of MOS transistors, the input resistance is essentially infinite when the amplifier is used in internal applications. The compensation capacitance and resistor are added to provide a better gain. The specification test is performed determining the gain, unity gain frequency and slew rate for op amp through simulation and the obtain results are tabulated. The voltage follower operation is also tested with and without fault and the results shown in fig 3.5 and 3.6.

Parameter	Theoretical value	Simulated value
Gain in dB	80 dB	75 dB
Unity gain frequency in MHz	20 MHz	6 MHz
Slew rate in V/μ sec	10 V/μ sec	9.6 V/μ sec

TABLE 3.1 SPECIFICATION TEST PARAMETERS FOR CMOS OP AMP

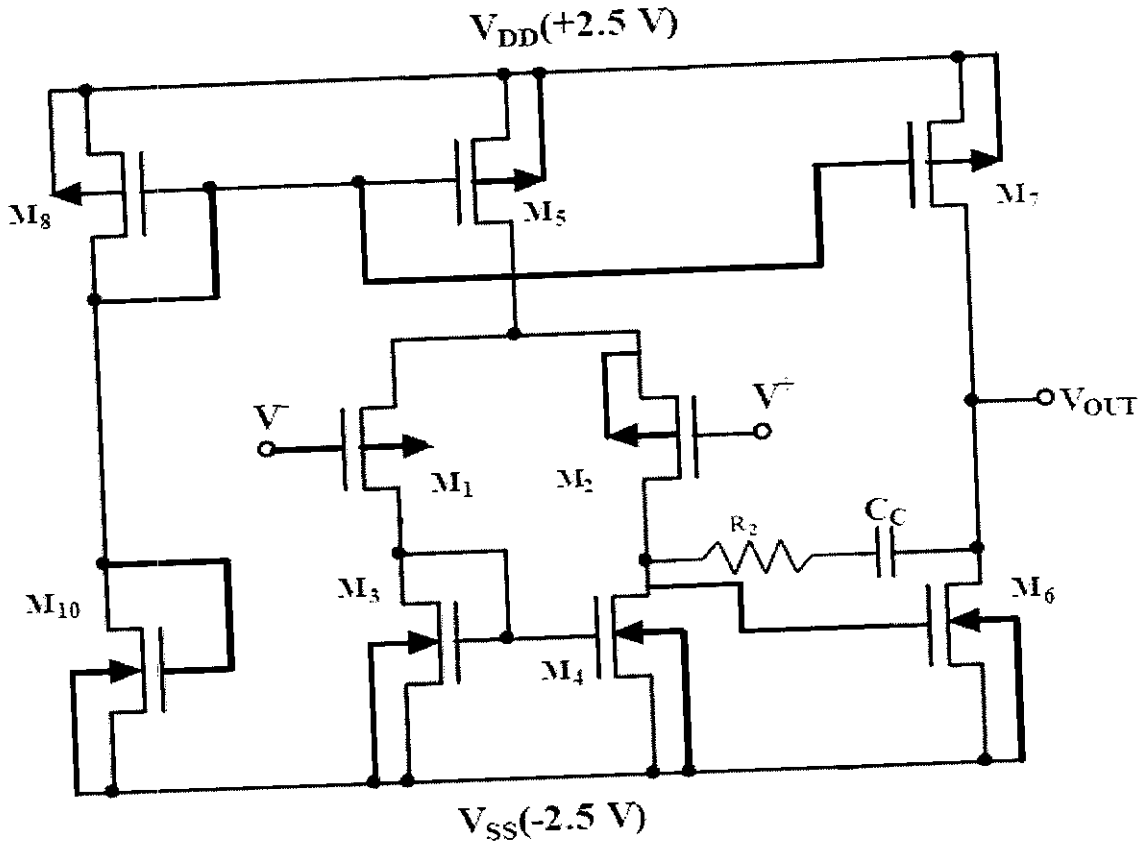


FIGURE 3.4 TWO-STAGE CMOS OPERATIONAL AMPLIFIER

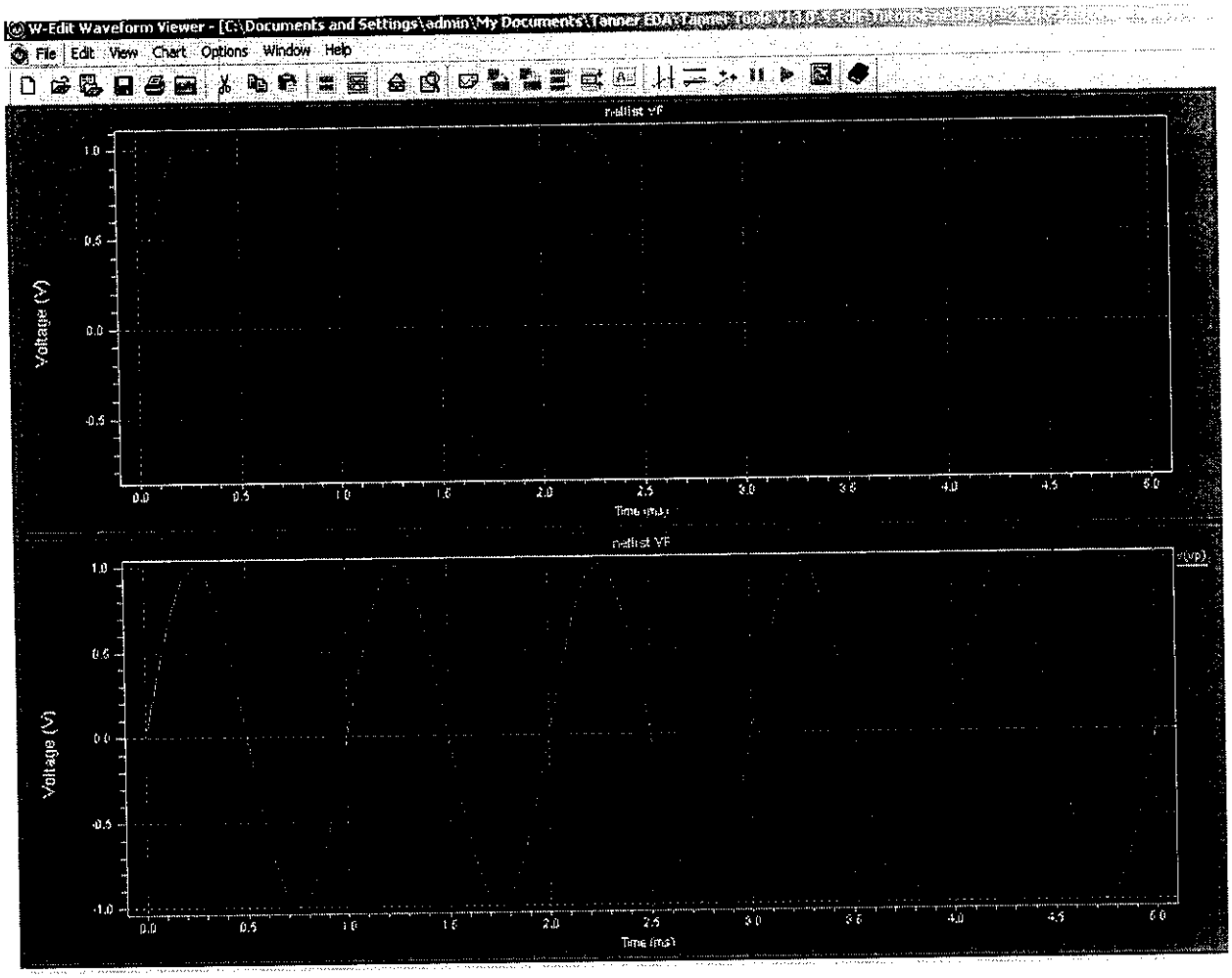


FIGURE 3.5 SIMULATION RESULT FOR FAULT FREE VOLTAGE FOLLOWER

The fault free voltage follower produces a output of 1V which is similar to the input voltage.

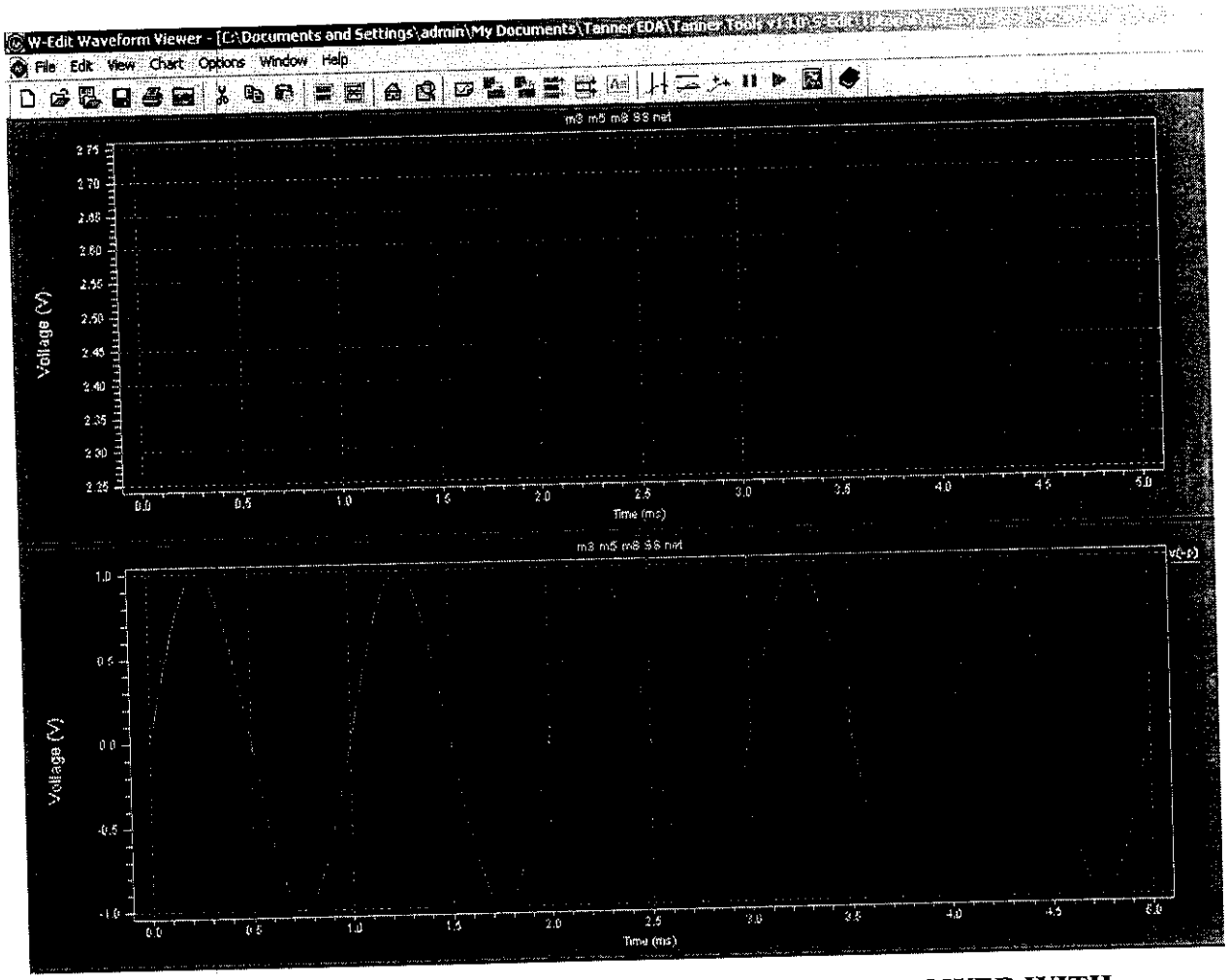


FIGURE 3.6 SIMULATION RESULT FOR VOLTAGE FOLLOWER WITH STUCK SHORT

The stuck short fault is injected in the circuit which causes the output voltage drop to a constant value of .25V

CHAPTER 4

CONCLUSION AND FUTURE SCOPE

This project presents a testing methodology for analog and mixed signal circuits.The oscillation based built in self test is implemented for a CMOS inverter.The circuit is simulated for fault free and faulty condition.The parameters such as oscillation frequency and output voltage are observedfor both fault and free condition.

The similar work is carried out for a mosfet amplifier in which the frequency response is performed in normal mode. The stuck short fault is injected and the deviation in the frequency response is observed.

The specification test is performed in the two stage CMOS opamp and the parameters such as frequncy response,unity gain,gain in dB and slew rate are calculated.The fault free voltage follower is simulated and the stuck short faults are injected and the deviaions are observed.

Future scope

Oscillation based built in testing is to be carried out for the two stage CMOS operational amplifier. The faults such as stuck open and stuck short can be injected into the circuit and simulated for faulty condition. The deviations in the parameters such as oscillation frequency and output voltage are to be determined. Fault coverage can be estimated as the ratio of fault identified to the total number of faults injected.

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APPENDIX

.MODEL NMOS NMOS (LEVEL = 49

+VERSION	= 3.1	TNOM	= 27	TOX	= 5.7E-9
+XJ	= 1E-7	NCH	= 2.3549E17	VTH0	= 0.43
+K1	= 0.4737692	K2	= 4.116E-5	K3	= 1E-3
+K3B	= 1.7999035	W0	= 1E-7	NLX	= 1.740604E-7
+DVT0W	= 0	DVT1W	= 0	DVT2W	= 0
+DVT0	= 0.4350667	DVT1	= 0.5819313	DVT2	= -0.5
+U0	= 282.63827	UA	= -1.459113	UB	= 2.666853E-18
+UC	= 3.876176E	VSAT	= 1.369009E5	A0	= 1.7826131
+AGS	= 0.3272708	B0	= -7.702255	B1	= -1E-7
+KETA	= -8.593406E	A1	= 1.899746	A2	= 0.4721967
+RDSW	= 200	PRWG	= 0.2843144	PRWB	= -0.2
+WR	= 1	WINT	= 0	LINT	= 1.584238E-9
+XL	= 0	XW	= -4E-8	DWG	= -7.786168E-9
+DWB	= 6.299903	VOFF	= -0.0967223	NFACTOR	= 1.429191
+CIT	= 0	CDSC	= 2.4E-4	CDSCD	= 0
+CDSCB	= 0	ETA0	= 2.584237	ETAB	= 1.060555E-4
+DSUB	= 0.0117695	PCLM	= 2.1515753	PDIBLC1	= 1
+PDIBLC2	= 2.145825	PDIBLCB	= 0.0471159	DROUT	= 1
+PSCBE1	= 2.386732E8	PSCBE2	= 7.052974	PVAG	= 4.599408E-3
+DELTA	= 0.01	RSH	= 4	MOBMOD	= 1
+PRT	= 0	UTE	= -1.5	KT1	= -0.11
+KT1L	= 0	KT2	= 0.022	UA1	= 4.31E-9
+UB1	= -7.61E-18	UC1	= -5.6E-11	AT	= 3.3E4
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	XPART	= 0.5
+CGDO	= 5.83E-10	CGSO	= 5.83E-10	CGBO	= 1E-12
+CJ	= 1.761007	PB	= 0.99	MJ	= 0.4688965

+CJSWG	= 3.29E-10	PBSWG	= 0.99	MJSWG	= 0.3271876
+CF	= 0	PVTH0	= -6.465496	PRDSW	= -10
+PK2	= 3.1412E-3	WKETA	= 6.591068	LKETA	= 3.835101E-3)

MODEL PMOS PMOS (LEVEL = 49

+VERSION	= 3.1	TNOM	= 27	TOX	= 5.7E-9
+XJ	= 1E-7	NCH	= 4.1589E17	VTH0	= 0.4
+K1	= 0.6419605	K2	= -7.282E-4	K3	= 0
+K3B	= 7.915875	W0	= 1E-6	NLX	= 2.685026E-8
+DVT0W	= 0	DVT1W	= 0	DVT2	= 0
+DVT0	= 3.1945843	DVT1	= 1	DVT2	= -0.1117614
+U0	= 101.30736	UA	= 1.041625E-9	UB	= 1E-21
+UC	= -1E-10	VSAT	= 1.425879E5	A0	= 1.1063182
+AGS	= 0.2045858	B0	= 1.017974E-6	B1	= 5E-6
+KETA	= 0.0111427	A1	= 0.0109159	A2	= 0.3
+RDSW	= 2.014607E3	PRWG	= -0.03098	PRWB	= -0.0309254
+WR	= 1	WINT	= 0	LINT	= 4.068013E-8
+XL	= 0	XW	= -4E-8	DWG	= -2.666714E-8
+DWB	= 3.702655	VOFF	= -0.1370541	NFACTOR	=1.243528
+CIT	= 0	CDSC	= 2.4E-4	CDSCD	= 0
+CDSCB	= 0	ETA0	= 0.2653362	ETAB	= -0.0830656
+DSUB	= 1.2359917	PCLM	= 1.3932016	PDIBLC1	=4.033555
+PDIBLC2	= -4.055943	PDIBLCB	= -1E-3	DROUT	= 0.0602572
+PSCBE1	= 2.392979	PSCBE2	= 2.163848E-9	PVAG	= 0.0141131
+DELTA	= 0.01	RSH	= 3	MOBMOD	= 1
+PRT	= 0	UTE	= -1.5	KT1	= -0.11
+KT1L	= 0	KT2	= 0.022	UA1	= 4.31E-9
+UB1	= -7.61E-18	UC1	= -5.6E-11	AT	= 3.3E4
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	XPART	= 0.5

+CJ	= 1.893734	PB	= 0.9889579	MJ	= 0.4705132
+CJSW	= 3.124347	PBSW	= 0.8	MJSW	= 0.2786992
+CJSWG	= 2.5E-10	PBSWG	= 0.8	MJSWG	= 0.2786992
+CF	= 0	PVTH0	= 4.821637E-3	PRDSW	= -2.2211772
+PK2	= 2.088108	WKETA	= 0.0199978	LKETA	= -5.605069E-3)