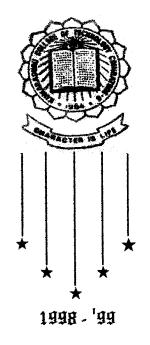
Microcontroller based Cyclic Timer

P-349

Praject Repart



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in partial fulfilment of the requirements
for the award of the Degree of
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in Electrical and Electronics Engineering
of the Bharathiar University

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Certificate

This is to certify that the report entitled

Microcontroller Based Tyclic Timer
has been submitted by

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Date: 18-03.99	PROFESSOR & HEAD Dept, of Electrical & Electronics Engg Kumaraguru College of Tech., Coimbatara
Certified that the candidate with 担:	nibersity Registration No
was examined in project work biba	– boce on
Internal Examiner	External Examiner

DEDICATED TO OUR BELOVED PARENTS TEACHERS AND FRIENDS

CERTIFICATE

PREMIER INSTRUMENTS & CONTROLS LIMITED

+ pricol +

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PROJECT CERTIFICATE

This is to certify that the following final year BE (EEE) students of Kumaraguru College of Technology, Coimbatore have undergone project work in our organisation:-

- 1. Mr M Rajesh
- 2. Ms G Premalatha
- 3. Ms M Kavitha
- 4. Mr J Antony Vijai Joshua

Title of the Project : MICROCONTROLLER BASED CYCLIC TIMER

Period of the Project: November 1998 to March 1999

Department : Product Engineering (Electronics)

During this period their attendance and conduct were found to be good.

We wish them the very best for a bright future.

ANTHONY THIAGARAJAN ASST. MANAGER - HRD



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SYNOPSIS

SYNOPSIS

In order to achieve good popularity in the market, any product must have good reliability. The main objective of our project is to test the reliability of a product. In short, the microcontroller based cyclic timer is a reliability testing kit used for ISO certification.

In this project, the microcontroller Z86E30 is used. It belongs to the Z8 family of microcontrollers from ZILOG Inc.

The principle behind the cyclic timer is " TO ON & TO OFF the device to be tested for a preset number of counts using a relay, so as to test the device."

There are two LEDs to indicate whether the device is in ON or OFF state. There is an impulse counter to indicate the number of cycles completed.

The ON & OFF durations for testing are loaded using BCD thumb-wheel switches. A relay is used for switching ON & OFF the device to be tested or that using for testing purpose. The function of the impulse counter is to increment by one, after each ON & OFF state is completed. This equipment is far more advantageous compared to manual detection. Skilled labour is not required and time of detection is less and so on. A detailed description of the circuit and its operations are dealt in the later

chapters. **ZILOG** processor is used to control the operations of the device. **Emulator** is used as an interface between the hardware and the software for testing the software.

ZILOG is preferred because of its user-friendliness and low cost.

The other important features include the provision of two timers, sufficient memory capacity and compact size.

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I INTRODUCTION

INTRODUCTION

We are going the period of micro-electronic revolution. For a common person, the role electronics is limited to audio-visual gadgets like radio and television. But the truth is that the growth of any industry like computers, communication, control or instrumentation is dependent on electronics.

PRICOL is a highly reputed and well-established company in the field of electronics and instrumentation. This project is sponsored by M/s. PRICOL. The company was established in the year 1974 and is one of the leading corporate bodies in India with a huge reputation behind it. Today it maintains high quality levels that matches the best in the industry and is well entrenched in catering to the needs of industries which include Textiles, Process industry, Defense, Electronics and small machine tools.

The objective of our project is to test the reliability of a device using the cyclic timer.

The ON / OFF time can be set manually using BCD thumb-wheel switches. The set time will be displayed in the switch panel, for the ON and OFF times separately. During operation, the set ON / OFF time is loaded into the counting circuit. When the device is operating, the ON

time is first displayed at first and counting begins. The counting is also displayed by decrements in the displayed value. When this value (ON time) reaches zero, the OFF time is displayed and counting begins, in a similar fashion. When this value (OFF time) reaches zero, one cycle is completed. This is recorded separately recorded on an impulse counter provide for this purpose. This operation for ON and OFF times is repeated as per the required number of cycles.

II BLOCK DIAGRAM

BLOCK DIAGRAM

2.1 **General Description**

Microcontrollers are digital computers designed to supervise, manage, and control various processes in industry, business, defense, aerospace and other areas of application, with the advent of **VLSI** technology. Microcontrollers are essentially single-chip micro-computers. The CPU, cache, main memory, I/O interface, DMA, interrupt handlers, timers and other sub-systems necessary to implement an efficient microcontroller are incorporated in the same chip.

INPUT DEVICES:-

- Min / Sec select switch (2 inputs)
- BCD switch (4 inputs)

OUTPUT DEVICES:-

- LEDs (2 outputs)
- Relays
- Impulse counter
- Demodulator (3 outputs)
- Display unit (8 outputs)

Figure (2.1) shows the block diagram of the cyclic timer.

The Z86E30 architecture is characterised by ZILOG's 8-bit microcontroller core with an expanded register file to allow easy access to the register mapped peripheral and I / O circuits. The CCP offers a flexible I / O scheme, an efficient register and address space structure and a number of auxillary features that are useful in many consumer, automotive, peripheral and industrial applications.

For applications demanding powerful I / O capabilities, the Z86E30 provides 24 pins dedicated to input and output purposes. These lines are grouped into three ports, eight lines per port. These three ports are configurable under software control to provide timings, status signals and parallel I / O with or without hand-shake.

There are three basic address spaces available to support this wide range of configurations, program memory register file and expanded register file. The register file comprises of 236 bytes of general purpose registers, three I / O port registers and the control and status registers. The expanded register file consists of three control registers.

The Min / Sec switches are selected according to the users wish.

The BCD switches are fed with input ranging from a limit of 0.1seconds to 999.9minutes.

The ON time and OFF time of the relays are loaded in the counter.

The corresponding minute or second is selected. Now as the ON switch is closed the corresponding LED glows and the relay connects the timer with the equipment to be tested.

Now the values are displayed on the display unit and it is decremented. As soon as it reaches zero the ON time LED gets switched-off and the OFF time LED starts glowing. The value loaded in the OFF time switch is now displayed on the display unit. As soon as the value reaches zero the impulse counter registers one complete cycle. Now the same process is repeated in a cyclic manner and hence the name cyclic timer.

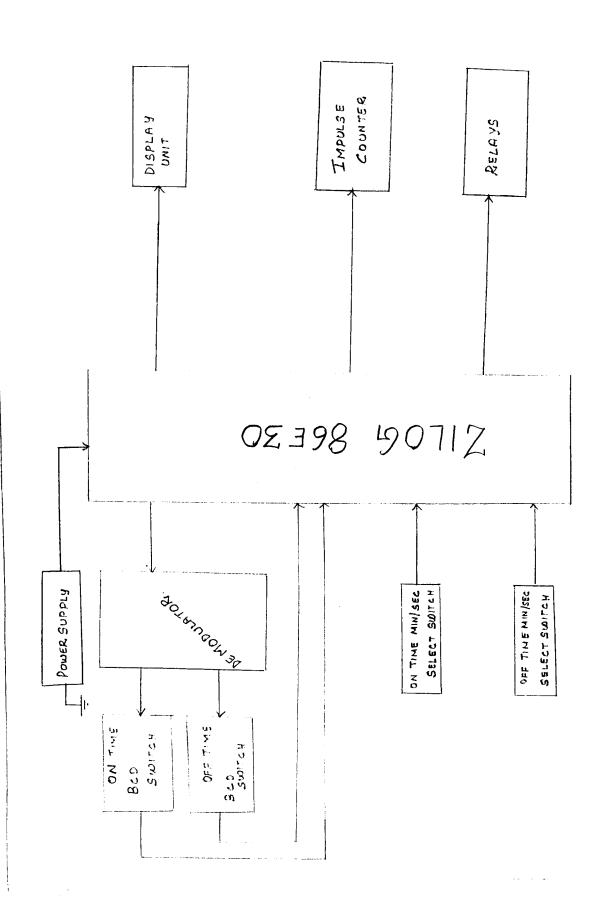
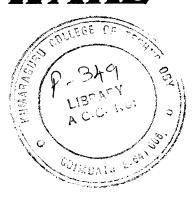


FIG 2:1 BLOCK DIAGRAM

III DESIGN OF HARDWARE



The microcontroller chip which is used in this project is **Z86E30** which belongs to the **Zilog** family. The reason for using Zilog microcontroller is that it has various advantages when compared to the other families of microcontrollers which are listed below:

- User friendly Emulator is present
- Powerful instruction set
- Less cost when compared to other microcontrollers
- Easily available
- Bit programmable

3.1 GENERAL DESCRIPTION OF MICROCONTROLLER:

The Z86E30 CCP (Consumer Controller Processor) is a member of the Z8 single chip microcontroller family with 4K bytes of EPROM and 236 bytes of RAM. The device is packaged in a 28-pin DIP and manufactured using CMOS technology. The Z86E30 offers two on-chip counters / timers with a huge number of user selectable modes and two on-board comparators to process analog signals with a common reference voltage.

The Z86E30 has the following general characteristics:

- 8 bit CMOS Microcontroller
- 28-pin DIP package
- Low cost
- 4.5 V to 5.5 V operating range
- Software programmable low EMI mode
- Pull up active / open drain programmable on port 0 and 2
- EPROM protect option
- RAM protect programmable
- RC Oscillator programmable
- Low power consumption 60 mW

- Two stand-by modes (STOP and HALT)
- 24 input / output lines (3 with comparator inputs)
- 17 digital inputs with CMOS levels, Schmitt triggered
- 3 digital inputs with CMOS levels only
- 3 expanded register file control registers
- 2 programmable 8-bit counter / timer each with a 6-bit programmable prescaler
- 6 vectored, priority interrupts from six different sources
- Clock speeds upto 12 MHz
- Watch-dog timer
- Auto power ON reset
- 2 comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC,
 RC or external clock drive.

3.2 Thumbwheel BCD Switches:-

Single or multiple pole, decimal or binary coded switches are used in computer or measuring instruments. Thumbwheel adjustments with 10 positions is available. This switch consists of a glass epoxy stator with tin plated copper tracks for ways. The pole is spring loaded brass contact. The operating level and assembly is plastic coated.

The 1000, 1100 and 1200 series switches are the smallest panel mounted switches. Each series is available in one or more of the following actuation methods, viz., thumb-set, push-set, pen-set and lock-set. The following codes are available in all the three series – (0 position decimal, Binary coded decimal and BCD with diode provision). The 1000 series is a rear panel mount, while the 1100 and 1200 series are front mount. The switches snap together, allowing custom assemblies and eliminating the need for extra hardware. All switches feature dust-proof construction and come with a one-year warranty.

3.2.1 Specifications:-

Number of positions - 10

• Life - 300 000 operations (min)

• Actuation force - 105 oz. (300 g) - all models

- Operating temperature
- -20 0 C to +60 0 C
- Storage temperature range
- -40 0 C to +80 0 C

- Electrical ratings
 - Non switching load
- 0.5 A, 50 VAC or 28 VDC

Switching load

- 1 A, 50 VAC or 28 VDC

• Contact resistance

- 0 to 200 ohms (max initial)
- Dielectric withstanding
- 500 VDC (1 minute)

voltage

- Insulation resistance
- 10 mega-ohms (min)

• Vibration .

- 50 m/sec (5-55 Hz, max)

Shock

- $100 \text{ m/sec} (10 \mu\text{A}, \text{max})$

• Seal

- dust proof

Weight

- 0.11 oz. (3 grams)

• Standard colour

- Black matte

• Thumbwheel

- Black white character

- Materials
 - Plastic

- poly acetal resin

Contact interface

- phosphorous, bronze, gold
 - over nickel

- Printed circuit board
- Glass epoxy, gold over nickel

In this project eight BCD ie., 8421 switches are used in the circuit. The first four BCD switches are used for loading the ON time of the relay and the remaining four switches for loading the OFF time of relay. Eight outputs are given from the microcontroller chip to the BCD switches. There are four inputs from the switches to the chip. Four diodes are connected along with each switch. They are placed upside-down with reference to the input. There are four individual switches in each BCD switch. A low is given as input to any one of the port pin and when any of the switch is pressed that corresponding diode alone gets forward biased. Thus a high is received at the output of the chip.

There are four pull-down resistors of 100 k each, connected to the four inputs from the switches. Pull-up resistors can also be used, but the advantage here is that the chip acts as a source by giving 5 volts.

3.3 Crystal:

Certain rock crystals are used in conjunction with oscillators to provide a highly stable source of electrical signals. The basic crystal material used is natural or synthetic quartz. A piece of crystalline quartz is cut, ground, polished and lapped with atleast one set of parallel surfaces. Electrodes are applied or plated to the set of parallel edges and connected to the oscillator circuit. The crystal vibrates mechanically

when a voltage is applied. Physically it has the quality called 'Piezo-electric' such that it accompanies the mechanical vibrations and corresponding electrical vibrations. Thus the crystal can oscillate both mechanically and electrically.

It could be seen from figure (3.1) that an equivalent LC tank circuit is provided for the crystal. This is a series – parallel circuit with a very low resistance, that is Q is very high, indicating that there is a very low loss in the crystal LC tank. Since there are both series and parallel capacitances in this circuit the crystal actually has two resonant frequencies close together. The frequency to be used is dependent upon the oscillator circuit.

3.3.1 <u>Accuracy</u>:-

The long term accuracy of a crystal is much better than that of the sample LC or RC oscillators. Long term frequency stability depends upon the care with which the crystal is cut and polished, the type of crystal cut, the maintenance of constant temperature and supply voltage and also the final circuit adjustment. Unless a crystal is operated in a constant temperature oven, a temperature change can cause a frequency change. When first operated a crystal may get aged or changes its frequency slightly. Typically the accuracy may be 0.01 or 0.001 percent of the

claimed frequency for the crystal. In use the crystal may have to be frequency adjusted very slightly or trimmed by the means of a small shunt and adjustable capacitor. The short-term frequency stability of the crystal is very good.

In this circuit, a crystal of frequency 8 mega hertz is connected between pins 9 and 10.

3.4 Switches:-

A switch is used to make or break the electric circuit. It should operate in such a way that it should make the circuit firm and under some abnormal condition it must retain its rigidity and keep its alignment between switch-blades and contacts correct to a fraction of a centimetre. At the instant of breaking the switch it should break the current so that there is no formation of an arc between the switch-blades and contact terminals. The disadvantage of formation of arc is avoided usually by means of providing a spring to a movable blade so as to have a quick action. Further the switch used must have a base mechanically strong capable of holding the parts together and must have a high insulation resistance.

The characteristics of switches are:

1. Maximum operating voltage

- 2. Current rating
- 3. Type of load
- 4. Capacitance
- 5. Insulation resistance
- 6. Change-over time

3.5 **POWER SUPPLY**:-

The main requirement of any circuit is a power supply. A regulated power supply is essential for sensitive devices like microcontrollers, microprocessors, etc. This project work is built around a microcontroller Z86E30, which is a sensitive device. This chip requires a power supply in the range 4.5 - 5.5 volts. So a circuit to obtain the regulated supply of 5 volt is designed and used in this project.

The power supply circuit incorporates a step-down transformer that is 230 / 0-24, 0-9 volts. An unregulated power supply is obtained at 24 volts DC using bridge rectifier and filter capacitors. This is used for the relay circuit.

Form the 9 volt secondary winding a regulated power supply at 5 volts DC is obtained using a regulator IC 7805 and the associated circuitry.

3.6 Circuit Operation :-

The V_{CC} (+5 volts) from the power supply is given to the pin number 8 of the Zilog chip. A capacitor of 0.1 μF is placed in series with the supply, which is used to reduce the inductance effects due to long distribution leads. A crystal of 8 MHz is used to provide a highly stable source of electrical signals. The main function of our project is to test the given component. For this purpose we load the BCD switches with the ON / OFF time values.

A toggle switch is used to select between the minutes and seconds. The time values are set manually using the BCD thumb-wheel switches. The two LEDs connected in circuit glow correspondingly to indicate which time state (ON / OFF) is being currently maintained.

When the ON time is being maintained the relay closes the circuit to be tested. The value of the set time is decremented successively until it reaches zero. On reaching zero the relay disconnects the circuit and the OFF time is maintained. The corresponding LED glows. At the end of the OFF time the impulse counter registers one count, thereby indicating the completion of one cyclic state. This process is repeated cyclically and on completion of the requisite number of cycles, the timer is switched off

manually. All the above operations are performed by the microcontroller as per the software which is loaded in its memory location.

3.7 ADVANTAGES:-

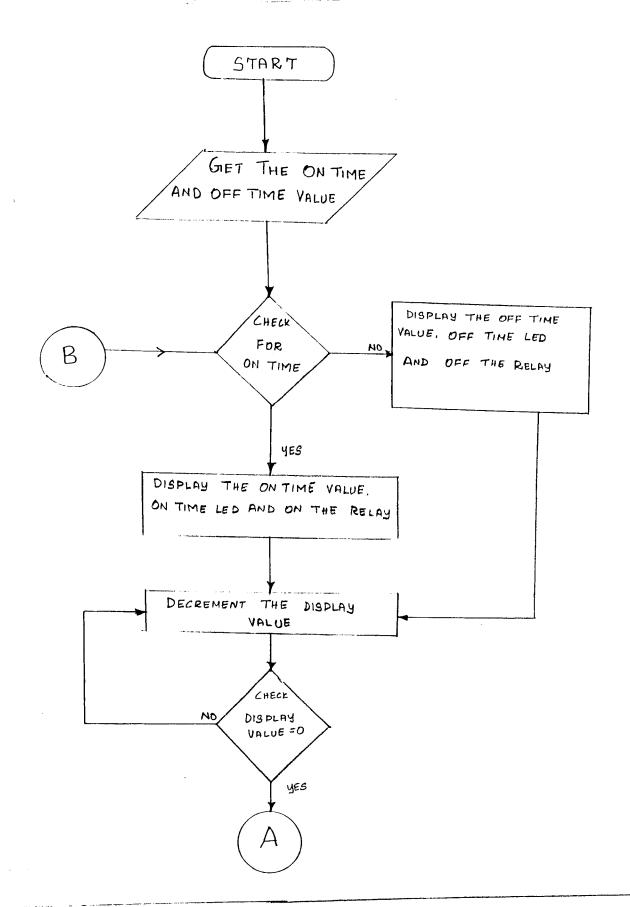
- In testing the reliability of any electrical components like lamps, relays, etc., the cyclic timer can be used. In the present type of testing equipments contactors are used, which are unreliable for long-time operations. The cyclic timer has a long-time reliability.
- **Eliminates** wastage of man-power.
- More number of cycles can be completed in a given duration due to faster time delay calculations due to absence of accumulator.

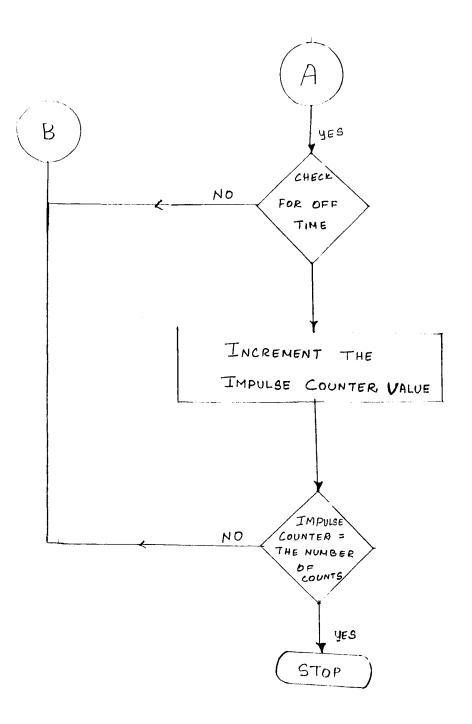
3.8 APPLICATIONS:-

- Used in component checking.
- Used to check reliability of products.
- Used in process control in chemical industry.

IV SOFTWARE

FLOWCHART





4.3 Structure of Software:

Software for Cyclic Timer

Controller 86E30

Crystal

CPU "Z8.tb1"

HOF "int8"

; Standard Control Registers:

P0:	EQU	H00
P2:	EQU	02H
P3:	EQU	03H
TMR:	EQU	0F1H
T1:	EQU	0F2H
PRE1:	EQU	0F3H
T0:	EQU	0F4H
PRE0:	EQU	0F5H
P2M:	EQU	0F6H
P3M:	EQU	0F7H
POIM:	EQU	0F8H
IPR:	EQU	0F9H
IRQ:	EQU	0FAH
IMR:	EQU	0FBH
FLAGS:	EQU	0FCH
RP:	EQU	0FDH
SPL:	EQU	0FFH
•		

; General Purpose Register Equates:

sw_ctr:	equ	27
ctr:	equ	28
bcd_on:	equ	31
bed value:	eau	32

bcd temp:	equ	33
bcd_on_temp:	equ	35
bcd on time:	equ	38
bcd off time:	equ	41
index rotate:	equ	44
bcd_on_temp_1:	equ	46
counter_1:	equ	4
counter_2:	equ	5
product_5:	equ	6
product_4:	equ	7
product h:	equ	8
product m:	equ	9
product_1:	equ	10
multiplicand_h:	equ	11
multiplicand_m:	equ	12
multiplicand_l:	equ	13
multiplier_h:	equ	14
multiplier_l:	equ	15
quotient_1:	equ	16
quotient_h:	equ	17
dividend 1:	equ	18
dividend m:	equ	19
dividend h:	equ	20
dividend_3:	equ	21
dividend_4:	equ	22
dividend_5:	equ	23
overflow_l:	equ	24
overflow_m:	equ	25
overflow_h:	equ	26
bcd_temp_1:	equ	48
disp_buff_3:	equ	50
disp_buff_2:	equ	51
disp_buff_1:	equ	52
disp_buff_0:	equ	53
disp_main_4:	equ	54
disp_main_3:	equ	55
disp_main_2:	equ	56
disp_main_1:	equ	57
disp_main_0:	equ	58
data_temp:	equ	59
data_temp1:	equ	60

ctr1:

equ

61

;Equate Interrupt Vectors

ORG 0

;IRQ0

DWM start

ORG 2

;IRQ1

DWM start

ORG 4

;IRQ2

DWM start

ORG 6

;IRQ3

DWM start

ORG 8

;IRQ4(T0)

DWM timer_int

ORG 10

;IRQ5(T1)

DWM start

ORG 12

start:		
	NOP	
	NOP	
	NOP	
	di	
	ld spl, #6FH	
	ld P3m, #00000001b	;P3 input digital, push-pull
	ld P2m, #00001111b	;lo-output hi-input
	or P0, #80H	;relay on (P0.4)
	or P2, #04H	;relay on (P2.2)
	ld P01m, #00000101b	;P0 output
	ld rp, #00000000b	
	di	
	wdt	
clr_ra	am:	
init_ı	ram:	
	ldr counter 1, #50	

ldr counter_2, #0

```
loop_20:
      wdt
      ld 4(rcounter_1), rcounter_2
      djnzr counter_1, loop_20
ctr_read:
      clr sw_ctr
      ld ctr + 2, #E8H
      ld ctr + 1, #03H
      ld ctr , #00H
      clr bcd on temp
BCD READ:
BCD_ON_READ:
      ld P0, sw_ctr
       ld bcd on, P3
       and bcd value #0FH
       ld bcd temp + 1, bcd value
       ld bcd temp, #00H
       ld multiplicand_l, ctr + 2
       ld multiplicand_m, ctr + 1
       ld multiplicand h, ctr
```

```
ld multiplier_l, bcd_temp + 1
ld multiplier_h, bcd_temp
```

CALL MULTIPLY:

add bcd_on_temp + 2, product_4
adc bcd_on_temp + 1, product_5
ld dividend_h, ctr
ld dividend_m, ctr + 1
ld dividend_l, ctr + 2
ld overflow_l, #10
ld overflow_m, #0
ld overflow_h, #0

CALL DIVIDE:

ld ctr + 2, quotient_l
ld ctr + 1, quotient_h
inc sw_ctr
cp sw_ctr, #4
jr nz, bcd on read

STORE:

```
TM bit, #1
    jr NZ, load_off
     ld bcd_on_time + 2, bcd_on_temp + 2
     ld bcd_on_time + 1, bcd_on_temp + 1
     ld bcd_on_time, bcd_on_temp
     or bit, #1
     jr, ctr READ
STORE LOAD OFF:
     ld bcd_off_time + 2, bcd_on_temp + 2
     ld bcd_off_time + 1, bcd_on_temp + 1
      ld bcd off time, bcd_on_temp
MULTIPLY:
      clr product_5
      clr product_4
      clr product_h
      clr product_m
      clr product_l
      ldr counter 1, #25
       rcf
```

```
MULT 1:
      wdt
      rrc product_5
      rrc product_4
      rrc product_h
      rrc product_m
      rrc product 1
      rrc multiplicand_h
      rrc multiplicand_m
      rrc multiplicand_1
      jn NC, ON ADD IT
ADD IT:
      add product_4, multiplier_1
      add product_5, multiplier_h
ON ADD IT:
      djnzr counter_1, mult 1
      ret
DIVIDE:
      ldr counter_2, #25
```

```
clr dividend_4
     clr dividend_5
     clr dividend_3
     clr quotient_l
      clr quotient_h
DIV 1:
      wdt
      sub dividend_3, overflow_l
      sub dividend_4, overflow_m
      sub dividend_5, overflow_h
      ccf
      ir c, DIV 2 ; complement logic
      add dividend_3, overflow_l
       adc dividend_4, overflow_m
       adc dividend_5, overflow_h
       rcf
 DIV 2:
       ldr counter_1, #8
       ld index rotate, #quotient_1
```

DIV 3:

wdt
rlc @ index_rotate
djnzr counter_1, DIV 3
djnzr counter_2, DIV 1
ret

DISPLAY UNIT

da bcd_on_time + 2

da bcd_on_time + 1

da bcd_on_time

ld bcd_temp_1, bcd_on_time + 2

and bcd_temp_1, #0FH

ld disp_buff_3, bcd_temp_1

ld bcd_temp_1, bcd_on_time + 2

and bcd_temp_1, #F0H

swap bcd_temp_1

ld disp_buff_2, bcd_temp_1

ld bcd_temp_1, bcd_on_time + 1

and bcd_temp_1, #0FH

ld disp_buff_1, bcd_temp_1

ld bcd_temp_1, bcd_on_time + 1
and bcd_temp_1, #F0H
swap bcd_temp_1
ld disp_buff_0, bcd_temp_1

get 7 seq: ld table reg, # ROM table +D ld disp_main_4, @ table_reg ld table reg, # ROM table add table_reg, disp_buff_3 ld disp main 3, @ table_reg ld table reg, # ROM table ld table reg, disp buff 2 ld disp main_2, @ table_reg ld table reg, # ROM table add table reg, disp buff 1 ld disp main 1, @ table reg ld table reg, ROM table add table reg, disp buff 0 ld disp main 0, @ table reg ld data pointer, # disp main ld common byte, # 11111011b

```
disp_timer:
```

ld data_temp, @ data_pointer ld data_temp_1, data_temp and data_temp, #0FH and data_temp_1, #F0H ld P0, data_temp ld P3, data temp_1 rl common_byte ld P2, common_byte inc data_pointer cp common byte, #7FH jr NZ, disp_timer_ret add common byte, #7CH ld data_pointer, #disp_main disp timer_ret: iret timer: ldr spl 240, #64H

ldr P3m_240, #00000001b

ldr P2m 240, #11101110b

and P2, #11101111b

ldr P01m_240, #00000101b

ldr tmr_240, #2CH

ldr t1_240, #25 ;timer_1_register 25

ldr Pre1_240, #01010011b ;prescalar_1 50

ldr ipr_240, #00001100b

ldr imr_240, #10100001b

ldr irg_240, #00000000b

or P2, #1

slp #0

clear:

clr counter

clr count_secs

ei

wt_loop:

jr wt_loop

timer_int:

inc counter

cp counter, #100



```
jr nz, timer_int_ret
      clr counter
      inc count_secs
      cp count_secs, #5
      jr nz, timer_int_ret
      clr count_secs
      xor P2, #1
      NOP
timer_int_ret:
      iret
timer:
      1d ctr + 2, #01
      ld ctr + 1, #00
      ld ctr1, #00
      tm bit_ctr, #1
      jr nz, off_time
on_time:
       incw bcd_on_time
       ld bcd_temp + 2, bcd_on_time + 2
```

```
ld bcd_temp + 1, bcd_on_time + 1
    ld bcd_temp, bcd_on_time
     sub bcd_temp + 2, ctr_1 + 2
     sbc bcd_temp + 1, ctr_1 + 1
     sbc bcd_temp, ctr_1
     cp bcd_on_temp, #00
     jr nz, on_time
     or bit ctr, #1
     jr exit
off time:
      incw bcd_off_time
      ld bcd_off_temp + 2, bcd_off_time + 2
      ld bcd_off_temp + 1, bcd_off_time + 1
      ld bcd_off_temp, bcd_off_time
      sub bcd_temp + 2, ctr_1 + 2
      sbc bcd_temp + 1, ctr_1 + 1
       sbc bcd temp, ctr_1
       cp bcd off_temp, #00
       jr nz,off_time
       or bit_ctr, #1
       jr exit
```

exit:

iret

ROM table:

dfb EB, 88, 6D, CD, 8E, C7, E7, 89, EF, 8F, 00, 10, 01, 40

V TEST & RESULTS

TESTS AND RESULT:

After completion of any product, it must be tested to observe its performance characteristics. Testing is also necessary to compare the actual output of the device with a predetermined result. Modifications will be necessary if there are any deviations between the actual performance and desired performance.

The cyclic timer is also tested in the following ON / OFF time settings.

ON / OFF time

- ❖ 5 sec / 15 sec
- ❖ 5 min / 15 min
- ❖ 75 min / 60 min
- ❖ 10 hours / 15 hours

RESULTS:-

The following results are observed.

ON / OFF time

- ❖ 5 sec / 15 sec
- ❖ 5 min / 15 min
- ❖ 75 min / 60 min
- ❖ 10 hours / 15 hours

VI CONCLUSION

CONCLUSION:-

A cyclic timer using microcontroller Z86E30 is designed, developed and tested fir testing the reliability of electrical products. A software program is written and is loaded into the memory of the microcontroller using the emulator.

The cyclic timer can also be used in component checking operations and chemical processing industries.

This project eliminates the deficiencies in the existing models like contactor type and other timers which use INTEL microcontrollers. The test results show that the desired performance characteristics are obtained.

SUGGESTIONS:-

- Introducing a provision for automatic switching off of the cyclic timer after completing the preset number of cycles.
- An LCD panel with back-lighting can be used for the display unit instead of the 7 segment LED display panel.

VII REFERENCES

- 1. Z8 MICROCONTROLLER, ZILOG Inc., Technical Manual, 1995.
- 2. Z8 MICROCONTROLER, ZILOG Inc., User Handbook, 1991.
- 3. High Speed CMOS Logic, Texas Instruments, Data Book.
- 4. Voltage Regulators, Linear IC Data Book, National Semiconductors.
- 5. The Z8 Application Note Handbook, ZILOG Inc., 1996.

APPENDIX

FUNCTIONAL BLOCK DIAGRAM:-

The Z8 chip incorporates special functions to enhance the Z8's applications in Industrial, Scientific, Research and advanced technologies.

RESET:-

The device is reset in one of the following conditions

- Power ON reset
- Watch Dog timer
- Stop Mode Recovery Source.

Having the Auto Power ON Reset circuitry built in, the Z86E30 does not need to be connected to an external power – on reset circuit. The reset time is 5ms plus 8 clock cycles. The Z86E30 does not re-initialise WDTMR, SMR, P2M and P3M registers to their reset values on a stopmode recovery operation.

PROGRAM MEMORY:-

The Z86E30 can address upto 4K bytes of internal program memory. The first 12 bytes of program memory are reserved for the

interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts.

Address 12 (000CH) to Address 4095 (0FFFH) are reserved for the user program. After reset, the program counter points at the address 000CH which is the starting address of the user program.

EPROM PROTECT:-

The 4 KB program memory is a one time PROM. An EPROM protect feature prevents "dumping" of the ROM contents by inhibiting and executing of LDC and LDCI instructions to program memory in all modes. In EPROM protect mode, the instructions of LDC and LDCI are disabled globally. ROM look-up tables cannot be used with this option.

EXPANDED REGISTER FILE:-

The Register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and I / O ports into Register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group. These register groups are known as the expanded register file. The low nibble (D3 – D0) of the register pointer selects the active ERF group and the high nibble

(D7 – D4) of the register RP selects the working register group. Three system configuration registers reside in the Expanded Register file at bank FH:PCON, SMR and WDTMR. The reset of the expanded register is not physically implemented and is removed for future expansion.

REGISTER FILE:-

The register file consists of three I/O port registers, 236 general purpose registers, 15 control and status registers in the expanded register group. The instruction can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register pointer. In the 4-bit mode the register file is divided into 16 working register groups, each occupying 16 continuous locations. The register pointer addresses the starting location of the active working register group.

RAM PROTECT:-

The upper portion of the RAM's address spaces 007F to 00EF (excluding the control registers) can be protected from reading and writing. The RAM protect bit option is EPROM programmable. After the EPROM option is selected, the user can activate from the internal ROM

code to turn OFF / ON the RAM protect bit by loading a bit D6 in the IMR register either a 0 or 1 respectively.

GPR:-

The register R254 is a general purpose register.

STACK:-

The Z86E30 has 236 general purpose registers. A 8-bit stack pointer for the internal stack that resides within the general purpose registers.

COUNTER / TIMER:-

There are two 8-bit programmable counter / timer each driven by its own 8-bit programmable prescalar. The T1 prescalar can be driven by an internal or external clock source. However the T0 prescalar is driven by the internal clock only.

The 6-bit prescalars can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescalar drives the counter, which decrements the value that has been loaded into the

counter. When the counter reaches the end of count, a timer interrupt request IRQ5 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue or restart from the initial value. The counters can also be programmed to stop upon reaching zero or to automatically reload the initial value and continue counting.

The counters but not the prescalars can be read at any time without disturbing their value or count mode. The clock source for T1 is user defineable and can be either the internal microprocessor clock divided by four or an external signal input through port 3. The timer mode register configures the external time input as an external clock, a trigger input that can be retriggerable or not retriggerable or as a gate input for the internal clock. Port-3 line P36 serves as a timer output through which T0, T1 or the internal clock is output.

INTERRUPTS:

The Z86E30 has six different interrupts from six different sources. The interrupts are maskable and prioritised. The six sources are divided as follows, four are claimed by port 3 line and 2 in counter / timers. The interrupt mask register globally or individually enables or disables the six interrupt requests.

CLOCK:-

The Z86E30 on-chip oscillator has a high gain, parallel resonant amplifier for connection to a crystal RC oscillator, ceramic resonator or any suitable external clock source. The crystal should be AT cut, 10 kHz to 12 MHz maximum, with a series resistance ($R_{\rm S}$) less than or equal to 100 ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitors from each pin directly to device pin 22. This is to reduce the injection of system ground noise.

POWER ON RESET:

A timer circuit clocked by a dedicated on-board RC oscillator is used for the power on reset timer function. The POR timer allows $V_{\rm CC}$ and the oscillator circuit to stabilise before instruction and execution begins.

The POR timer circuit is a one-shot timer triggered by one of the three conditions listed below.

Power - bad to Power - ok status.

Stop – mode recovery.

WDT time - out.

The POR time is normally 5ms. Bit 5 of the stop-mode register determines whether the POR timer is by-passed after the stop-mode recovery (typical for external clock and RC / LC oscillators with fast start-up time).

HALT:-

The halt-mode turns off the internal CPU clock, but not the XTAL oscillation. The counter / timer and external interrupts IRQ0, IRQ1 and IRQ2 remain active. The device is recovered by interrupts, either internally or externally generated. An interrupt request must be executed to exit halt-mode. After the interrupt service routine, the program continues from the instruction of HALT.

STOP:-

The STOP instruction turns off the internal clock and the external crystal oscillation and reduces the standby current to 10 µA or less. STOP is terminated by one of the following resets, viz., WDT time out, POR or stop-mode recovery source which is defined by SMR register. This causes the processor to restart the application program at address 000CH. In order to enter stop-mode, it is necessary to first flush the instruction pipelined to avoid suspending execution in mid-instruction. To do this,

the user must execute a NOP instruction immediately before the appropriate STOP instruction.

PIN DESCRIPTION:

Z86E30 STANDARD MODES

Pin#	Symbol	Function	Direction
1 – 3	$P_{25} - P_{27}$	Port2, pin 5, 6	Input / output
4 – 7	$P_{04} - P_{07}$	Port0, pin 4, 5, 6, 7	Input / output
8	$V_{\rm cc}$	Power supply	
9	XTAL2	Crystal oscillator	Output
10	XTALI	Crystal oscillator	Input
11 – 13	$P_{31} - P_{33}$	Port3, pin 1, 2, 3	Input
14 – 15	$P_{34} - P_{35}$	Port3, pin 4, 5	Output
16	P ₃₇	Port3, pin 7	Output
17	P ₃₆	Port3, pin 6	Output
18	P ₃₀	Port3, pin 0	Input
19 – 21	$P_{00} - P_{02}$	Port0, pin 0, 1, 2	Input / output
22	V_{SS}	Ground	
23	P ₀₃	Port0, pin 3	Input / output
24 – 28	$P_{20} - P_{24}$	Port2, pin 0, 1, 2, 3, 4	Input / output

TABLE: 1

PIN FUNCTIONS:-

• XTAL1 Crystal 1 (time based input):-

This pin connects a parallel resonant crystal, ceramic resonator, LC / RC network or external single phase clock to the on-chip oscillator input.

• XTAL2 Crystal 2 (time based input):-

This pin connects a parallel resonant crystal, ceramic resonator, LC / RC network to the on-chip oscillator output.

• Port 0 ($P_{07} - P_{00}$):-

Port 0 is a 8-bit bidirectional CMOS compatible input / output port. These eight I / O lines can be nibble programmed as $P_{03} - P_{00}$ input / output and $P_{07} - P_{04}$ input / output separately. The input buffers are Schmitt triggered and nibble programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can also be used as a hand-shake I / O port.

In hand-shake mode, port 3 lines P_{32} and P_{34} are used as hand-shake control lines. The hand-shake direction is determined by the

configuration assigned to port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

• Port 2 $(P_{27} - P_{20})$:-

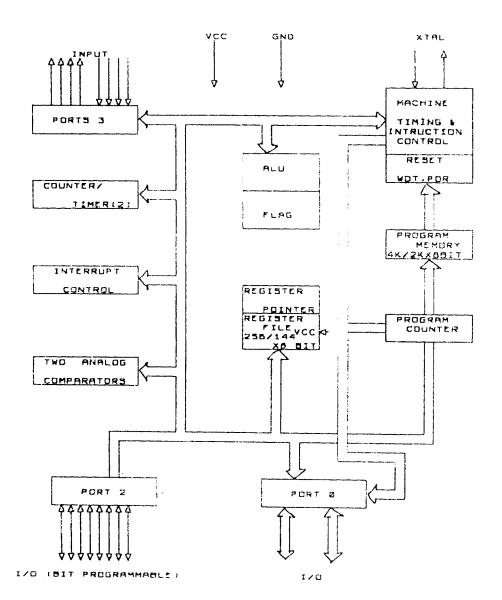
Port 2 is an 8-bit, bidirectional CMOS compatible I / O port. These eight I / O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I / O port, port can be placed under the handshake control. In the hand-shake mode, port 3 lines $P_{31} - P_{36}$ are used as hand-shake control lines. The hand-shake direction is determined by the controller assigned to bit 7 of port 2.

• Port 3 $(P_{37} - P_{30})$:-

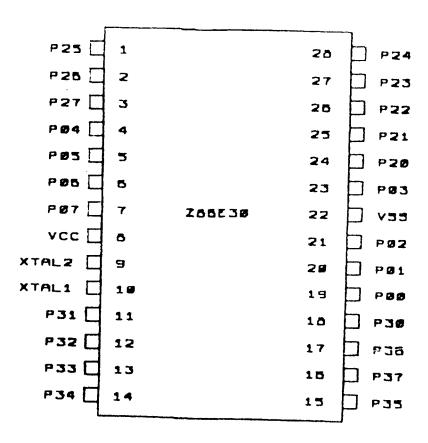
Port 3 is an 8-bit, CMOS compatible port bit four fixed inputs and four fixed outputs. Port 3 consists of four fixed inputs ($P_{37} - P_{34}$) and four fixed outputs ($P_{33} - P_{30}$) and can be configured under software for interrupt and hand-shake control functions. Port 3, pin 0 is Schmitt triggered. Pin P, P_{32} , P_{31} , P_{33} and P_{34} are standard CMOS inputs and pin P,

 P_{35} , P_{36} and P_{37} are push-pull output lines. Low EMI output buffers can be globally programmed by software. Two on-bound comparators can process analog signals on P_{31} and P_{32} with reference to the voltage on P_{33} . The comparator output can be outputted from P_{34} and P_{37} respectively by setting P register bit 0 to 1.

The analog function is enabled by setting the D1 of port 3 mode register. For the interrupt function P_{30} and P_{33} are falling edge triggered interrupt inputs P_{31} and P_{32} can be programmed as falling, rising or both edge triggered interrupt inputs.



FUNCTIONAL BLOCK DIAGRAM



PIN DIAGRAM

PROGRAM MEMORY

4095/2047

LOCATION OF FIRST BYTE ON-CHIP OF INSTRUCTION EXECUTED 12 ROM AFTER RESET 11 IROS 18 IRRE IRQ4 8 IRQ4 IRDJ IRGS INTERRUPT VECTOR (LOWER BYTE) IR92 INTERRUPT VECTOR (UPPER BYTE) 1683 IRB1 IRD1 IRDO IRDØ