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MULTISTAGE DECIMATION FILTER DESIGN BASED ON RESIDUE NUMBER SYSTEM

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BONAFIDE CERTIFICATE

Certified that this project report entitled **"MULTI STAGE DECIMATION FILTER DESIGN BASED ON RESIDUE NUMBER SYSTEM"** is the bonafide work of **Mr.R.Venkata Krishnan [Reg. No. 0920107025]** who carried out the research under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

Project Guide

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Head of the Department

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The candidate with university Register No. 0920107025 is examined by us in the project viva-voce examination held on 21-04-2011.....

Internal Examiner

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ABSTRACT

In recent days, the use of efficient digital filter in wireless application is increasing because of the speed of conversion, fast performance, less hardware and less power consumption. The decimation filter provides all the above objectives. This paper presents a multistage, programmable decimation filter based on Residue Number System (RNS) that is adaptable for GSM standard. Multi-stage decimation filter implementation offers low computational complexity and power dissipation. The FIR filters of the multi-stage decimator operating in RNS domain offers an integer system appropriate for implementing fast digital signal processors. It also offers high data rate because of carry free operations on smaller residues in parallel channels. Finally, the computational complexity comparisons are performed based on the results from simulation of the proposed RNS based decimation filter with traditional binary one. It is observed that computational complexity is reduced by 30% in RNS based multi stage decimation filter compared with traditional implementation.

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LIST OF ABBREVIATIONS

RNS	-------	**Residue Number System**
FIR	-------	**Finite Impulse Response**
MATLAB	-------	**MATrix LABoratory**
SNR	-------	**Signal to Noise Ratio**
OSR	-------	**Over Sampling Ratio**
ADC	-------	**Analog to Digital Converter**
CIC	-------	**Cascaded Integrator Comb**

CHAPTER 1
INTRODUCTION

Nowadays in wireless and audio application the use of efficient digital filter is increasing because of the speed of conversion, fast performance. So the filters are designed to match the requirements. While going for multi stage decimation filter design it is possible to speed of conversion, fast performance, less hardware, and less power consuming. The demand for higher system capacities and data rates led to the rapid development of wireless communication systems that allow coexistence of multiple standards. Reduction in cost and power in the implementation of multi-standard wireless transceivers is drawing market and research interest.

1.1 MOTIVATION

The digital receiver should perform efficiently to match with the modern technology trends. The sampling frequency of over sampling A/D converters is much higher than Nyquist rate. It also provides the desired value for the decimation filter. The Multi stage decimation filter will reduce the number of coefficient. Then the coefficients were converted into residues and it is used to reduce number of adders and multipliers for the filter synthesis. If number of adders and multipliers are reduced, then hardware requirement and power consumption is also less.

1.2 PROJECT GOAL

The goal of this project is to design and implementation of a multi-stage decimation filter based on Residue Number System (RNS) for a GSM standard. Firstly, this technique addresses the problem of multi-standard decimation filtering. Secondly, and more importantly, since the implementation is multi-rate, the subsequent filters operate at lower sampling rates. The filter specifications of individual filters are relaxed to reduce the filter order while the multi-stage structure meets the overall decimator specifications. Thus it reduces power consumption and computations with compared to a single stage implementation.

1.3 OVERVIEW

The basic steps for designing multi stage decimation filter and RNS Algorithm have been shown in the Figure 1.1

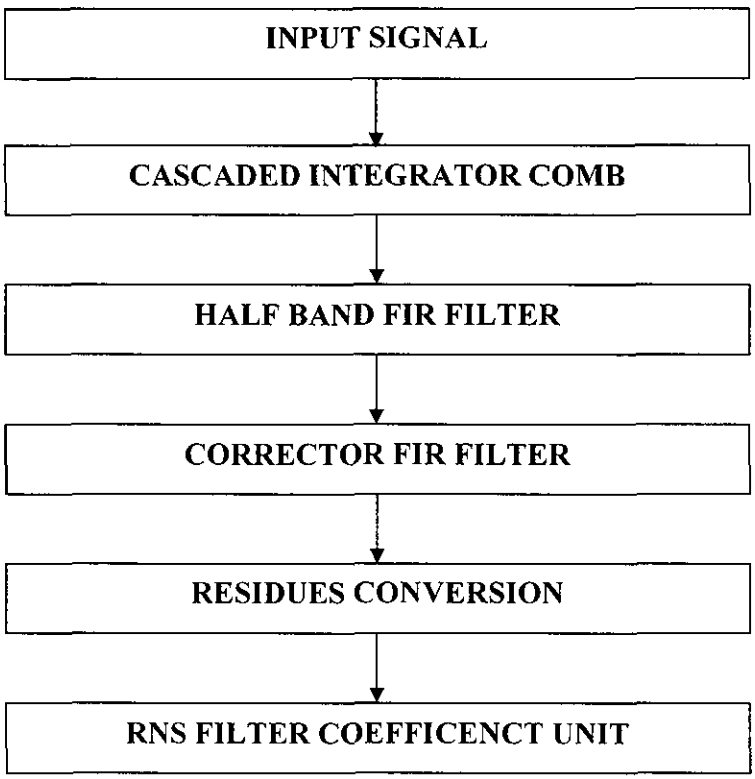

Figure 1.1 Overview of the Design Steps of the Project

1.4 SOFTWARES USED

- Matlab 7.3

1.5 ORGANIZATION OF THE REPORT

- **Chapter 2** discusses about the digital receiver and its operation
- **Chapter 3** deals about the Decimation Filter Fundamentals and Over-Sampling Analog to Digital Converter characteristics
- **Chapter 4** explains the Residue Number System and its conversion
- **Chapter 5** gives the digital filter architecture and implementation steps of the project
- **Chapter 6** discusses the simulation results
- **Chapter 7** shows the Conclusion of the project.

CHAPTER 2
DIGITAL RECEIVER

The digital receiver block diagram is shown in Figure 2.1. A quick overview of a digital receiver will readily confirm that its main task is to take a signal sampled at a high rate, down convert it, low-pass filter it, decimate it and format it into one or more of several forms. After demodulation, this signal is converted to analog form and apply it to a power amplifier and loudspeaker.

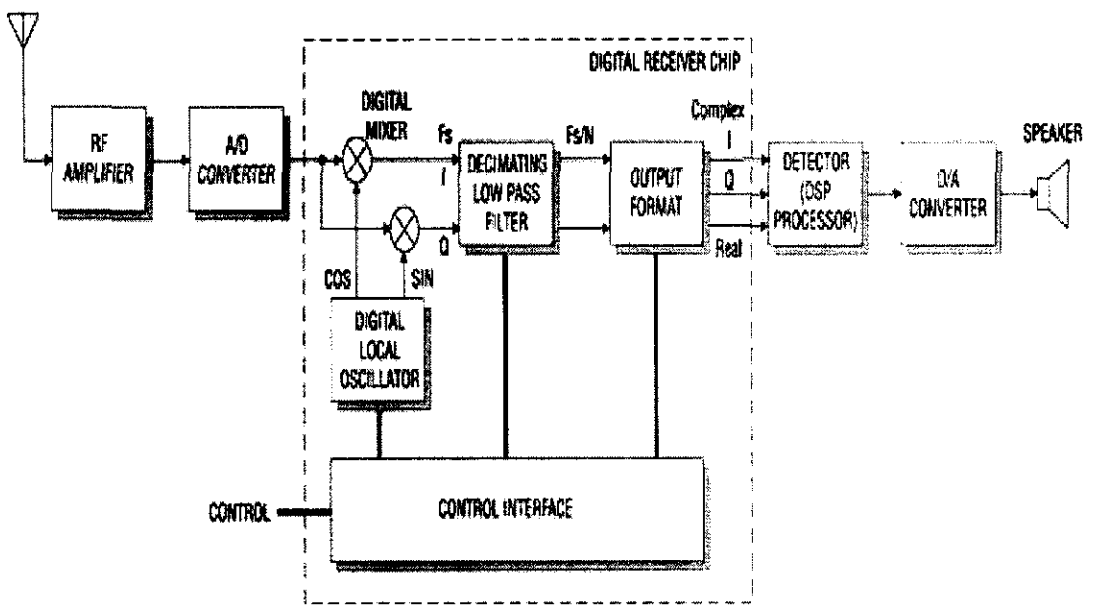

Figure 2.1 Digital Receiver Block Diagram

The input analog signal is converted to digital form with the aid of the A/D converter. Next, this signal of ones and zeros is applied to a digital Mixer, just as in the analog receiver. Only at this time the signal is applied to two Mixers, driven by digital In-phase (I) and Quadrature (Q) components of a Local Oscillator signal, which in turn is provided by a digital Frequency Synthesizer. In essence, the input signal is multiplied