FUZZY LOGIC CONTROLLER FOR DC MOTOR

Project Report

Submitted by

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Under the Guidance of

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SYNOPSIS

Speed control/regulation of the motor is an essential criteria, almost in all industries. For many applications, they prefer DC motors, for its advantages over the A.C. motors. Hence, in this project we have designed the system for controlling the speed of a DC motor which is used in the paper industries that plays a vital role to have uniform thickness and continuity of the sheet. Even though there us a fluctuation in the raw materials.

At present, there are many methods available for the speed control of DC motor. Here the speed is varied by varying the armature voltage of the DC motor by applying Fuzzy Logic program and power transistor as controller. A fuzzy logic controller has higher accuracy and reliability.

A proximity sensor generates a pulse signal of frequency proportional to the speed of the motor shaft. The generated frequency is then converted into voltage in the range of 0 to 5 volts.

This analog voltage is converted to digital values by using suitable A/D converter and fed to the personal computer. In the computer, we have designed a FLC, that will working three steps ,

a) Fuzzification, where crisp input is translated into fuzzy value.

b) Rule Evaluation, where the fuzzy output values are computed.

c) Defuzzification, where the fuzzy output translated to crisp value (or) actual value.

This value is nothing but the value that determine the speed of the motor to be adjusted or not. This value is given to the input of DAC converter and the fed to the motor to control the speed.

CONTENTS

CHAPTER I

INTRODUCTION

Speed control is one of the many foremost and essential one in many process industries such as tyre manufacturing, paper industries etc., Though the conventional PID controllers have simple structure, they cannot always effectively control the systems with changing parameters and may need frequent online retuning. So we opt for fuzzy logic controllers that are considered as non-linear PID controllers where the parameters can be determined on line, based on the error signal and their time derivative of difference.

1.1 SPEED SENSING

For speed sensing there are many methods available in the market. In this model we are sensing the speed of the motor by using proximity sensor which generates frequency proportional to the speed. We are converting the frequency to equivalent voltage by the process of signal conditioning.

1.2 CONTROLLER

This analog voltage is converted to digital value by using A/D converter chip. The controller works in the following three steps to achieve the desired control action.

1) Input stage
2) Processing stage
3) Output stage

1.2.1 Input stage

The input stage maps sensor of other inputs to the appropriate membership functions and truth values. The most common shape of membership function is triangular, although trapezoidal and bell curves are also used, but the shape is generally less important than the number of curves and placement. From 3 to 7 curves are generally appropriate to cover the entire range of an input value.

1.2.2 PROCESSING STAGE

The processing stage invokes each appropriate rule and generates a result for each then combines the results of the rules. The processing stage is a collection of logic rules in the form of IF- THEN statement, where the IF part is called 'antecedent' and the THEN part is called the 'consequent'. This rule uses the truth value of input to generate a result in the fuzzy rule set for the output. This result is used with the results of other rules to finally generate crisp composite output. In practice fuzzy rules sets usually have several antecedents that are combined using fuzzy operations, such as AND, OR and NOT. Results can be solved in parallel with hardware and sequentially in software.

1.2.3 OUTPUT STAGE

The outputs stage converts the combined result back into a specific control value. The results of all the rules that have fired are defuzzified by one of several methods, there are dozens in theory each with various advantages and drawbacks. The centroid methods favour O/P or greatest area while height method favour greatest O/P value.

1.3 DC DRIVE

The control signal from the FLC is given to the Digital to Analog converter, to get a analog control signal. This control signal is given to the DC drive. The main aim of this project is to maintain a consistency in speed of motor at any condition for which we are in need of the control circuit. The control circuit produces gate control to the SCR.

According to the gate control to the SCR the average voltage to the armature is varied, which proportionately vary the speed of the motor. The armature is fed by supply form full wave half controlled bridge, while the field circuit is supplied from a bridge rectifier.

1.4 GENERAL BLOCK DIAGRAM

The general block diagram of our model is shown in the figure (1.1).

The block starts from the proximity sensor that the generators a signal proportional to the speed of the motor. Its output signal is conditioned and given to analog to digital converter. The output of ADC is fed to the personal computer.

The output from the PC is then given to the digital to analog converter. This analog signal is given to the DC motor driver that drives the motor at desired speed. The speed of the DC motor which is to be controlled is measured using sensor. The measured speed is in the form of pulses whose frequency is proportional to the speed of the motor.

The frequency signal is converted into voltage signal using signal conditioner. The obtained analog value is converted to digital value to be fed to the compiler using Analog to Digital converter. The fed value is proceeded by the controlled and the digital value seat out is again converted to analog value using digital to analog converter. The obtained will be in the range of 0 –10 volts

According to the volts obtained the DC motor drive changes the armature voltage of the motor and hence speed of motor is varied and controlled.

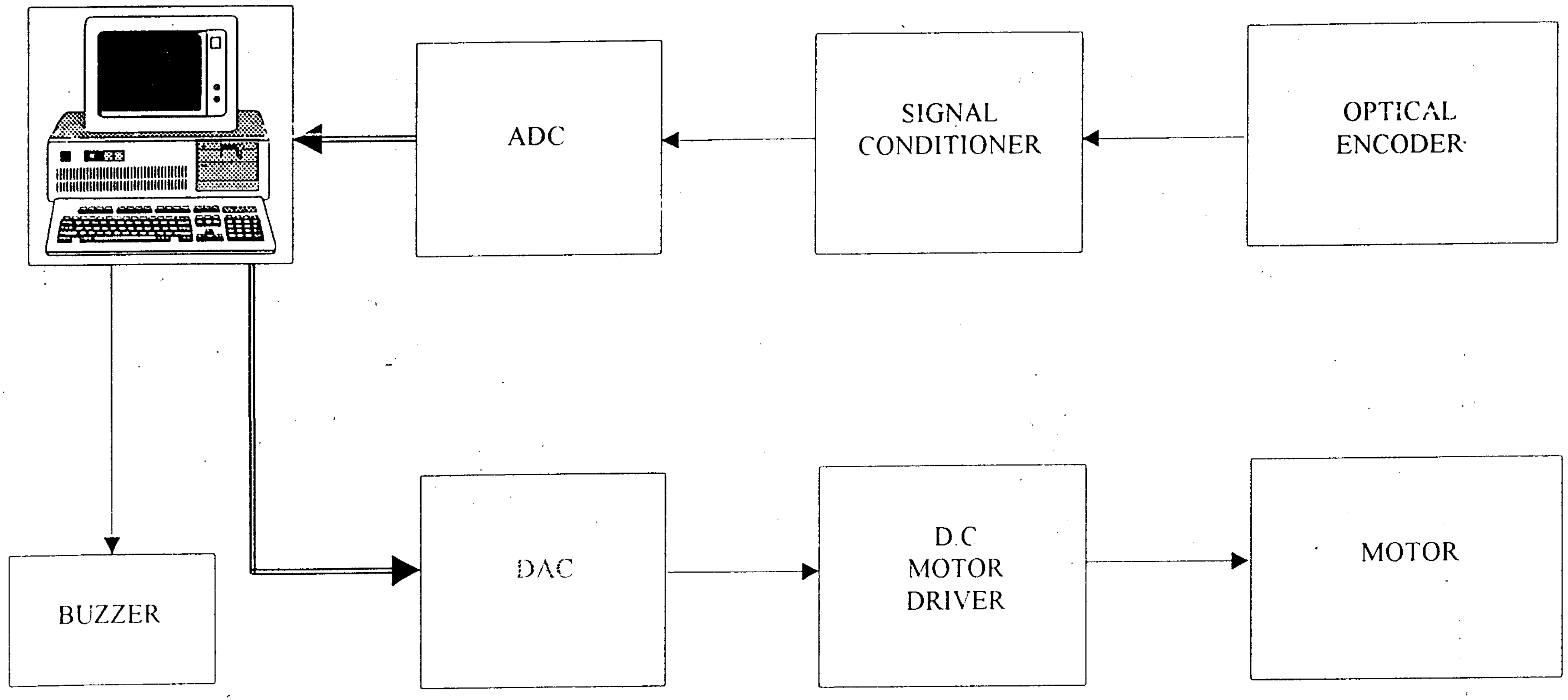


FIG 1.1 **GENERAL BLOCK DIAGRAM**

CHAPTER II

SPEED SENSING UNIT

2.1 PROXIMITY SENSOR

The proximity sensor is used in our project to sense the speed of the motor. Fig.2.1 shows the internal configuration of the proximity sensor. The proximity sensor consists of a core, which is energised by giving supply to it. Whenever this core comes across a metal, it will induce some current, which flow through this core. According to the frequency of this current signal, the oscillator to which this current signal is connected, will produce a signal of corresponding frequency.

This signal is given to the rectifier, whose output is given to the comparator. The comoparator output will be of signal, whose frequency is proportional to the speed of the motor.

2.2 SIGNAL CONDITIONING

The pulse output form the proximity sensor is fed to the base of the transistor. The output of the transistor is in the inverted form of actual input. This signal is differentiated by a RC network and the negative going edge at pin 6 causes the input comparator to trigger the timer circuit. The current at the output terminal can be changed by varying the resistance at pin 2. The output current at pin 1 is given by

$$i = (1.1\ RC)\ .\ f \qquad \text{----------------------2.4}$$

where, f = frequency of the supply at pin 6

R,C = resistance and capacitor value at pin 8 and pin 6 respectively.

By changing the values of Rt and Ct the current through the capacitor can be varied. The filtering action is done by R1 = 100K and C = 1 f. The output voltage is fed through an inverting amplifier with unity gain which results in negative value of the actual input, to the inverting amplifier.

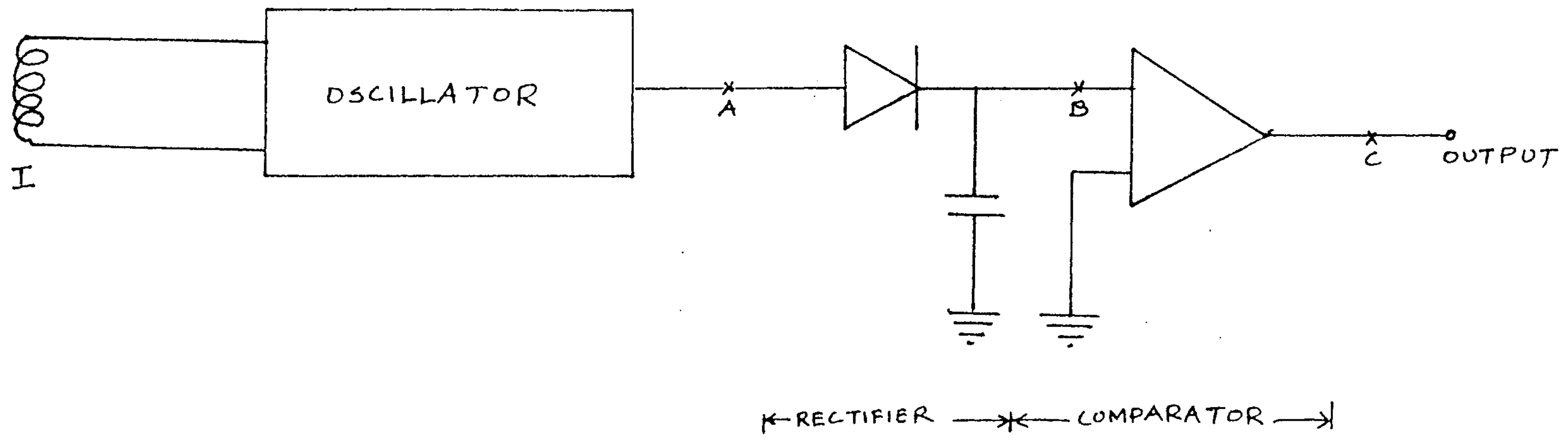


FIG 2.1 INTERNAL CONFIGURATION OF PROXIMITY SENSOR

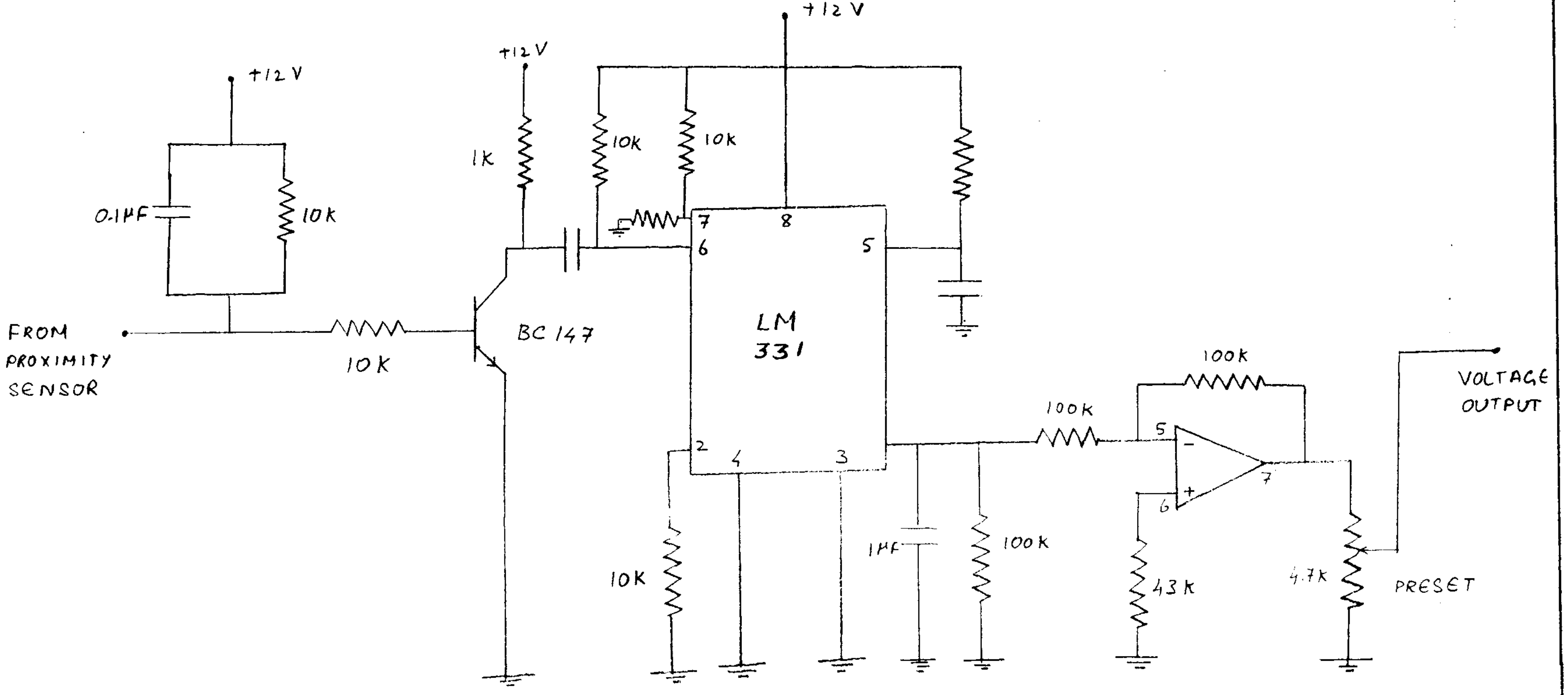


FIG: 2.2 SIGNAL CONDITIONING

CHAPTER III

INTERFACING HARDWARE

3.1 FUNCTIONAL BLOCK DIAGRAM:

The functional block daigram of the ADD-ON Card is shown in the fig.3.1. Here IC 74LS245 is the transceiver which is nothing but a buffer that transfers the data between the Personal Computer and the chips in the ADD-ON Card. IC 74LS273 is nothing but the latch that holds the data for the processing. IC 74LS688 is a 8 bit comparator used for designing the address of ADD-ON card.

The chip selector IC 74LS138 which is a Demultiplexer is used to select particular chip by sending enable signal, for the proper working sequence of the card. For selecting the input, we are using 8-1 multiplexer IC 4051. The output of multiplexer is given to ADC 574 which is 12 bit digital converter, whose output is latched using IC 74LS373 and finally read by the computer through transceiver.

The digital value from the computer is given to the DAC 7541 through the latch IC 74LS273, which convert the digital value to anlog value which will be available at the connectors pin.

3.2 WORKING OF ADD-ON CARD

The basic function of this card is to convert analog input to digital value and the digital value form the computer to analog output with the help of the ADC and DAC chips. To perform this transformation, apart from the main converter many other functional blocks are required. These are amplifier, multiplexer and other signal conditioning circuits. The choice of these various blocks and their specifications have to be properly matched to get the optimum performance.

For determining the base address of the Add-on card, we are using a comparator that compares the address we set on the Add-on card and the address in to address bus of the personal computer. Here we are using 74LS688 IC as comparator, which is a 8-bit comparator. For the purpose of setting the address of the Add-on card, there is a DIP switch provided in the card. The output of the comparator is given to the chip selector IC, which is used to select the chips in the card for the purpose of transformation of datas. The IC used as chip selector is 74LS138, which is basically a three to eight line decoder/demultiplexer. With respect to the input control signal, it will select the appropriate chip for proper conversion.

There is a transceiver present in the Add-on card that will transmit or receive the data between the computer and Add-on card. IC 74LS245 that can handle 8-bit data serves as a transceiver in this Add-on card. To hold the data for processing, to the transceiver, a 74LS273 flip-flop IC is connected. The control signal from the personal computer is fed to the chip selector IC by means of a buffer 74LS244 IC.

The function of the Add-on card can be divided into three parts as follows:

1. Analog to Digital Conversion
2. Digital to Analog Conversion
3. Programmable Peripheral Interfacing

3.2.1 ANALOG TO DIGITAL CONVERSION:

"Analog to Digital Converter" choice is one of the very important considerations. To suit wide ranging applications, different A/D conversion techniques are used. Flash converter, successive approximation, integrating, tracking and floating point are some of the commonly used techniques.

IC ADC574 is used here for the purpose of converting the Analog input to Digital value. IC ADC574 does the conversion by means of successive approximation method.

The successive approximation method uses a very efficient method of conversion. The fig. 3.1 shows an 8-bit converter. The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error method.

At the beginning, start command is initiated and SAR sets the MSB d_1 = 0 and all other bits to zero so that the trial code is 1000000. The output of DAC, V_d is now compared with Va. If Va> V_d ,then 10000000 is less than correct digital representation. MSB is left '1' and next LSB is made '1' and tested. Suppose if Va< V_d, then 1000000 is greater than correct digital representation, so reset MSB to '0' and go to next LSB. This procedure is repeated for all bit positions.

IC ADC574 has an in-built sample and hold circuit. So when we give the input analog single to the ADC through the 4051 multiplexer, the input is sampled and hold for few microseconds for the process of successive approximation. During this time IC 7400 will give a ' busy ' signal so that there will not be any disturbance form the input signal. The output form the ADC is then latched by using two flip-flops as shown in the circuit and finally it will read by the personal computer.

Base I/O ADDRESS Selection:

Base address selection logic details are tabulated below. All the combinations of the switches swc1 -swc4 are supported by the card.

SWITCH ON = 1 : OFF = 0

ADDR.SEL	SWC1	SWC2	SWC3	SWC4
FROM	(A8)	(A9)	(A10)	A(11)
1300H*	1	1	0	0
1600H	0	1	1	0

* --------------- PRESENT SETTING

3.2.2 DIGITAL TO ANALOG CONVERSION:

The digital to Analog conversion is done by using R-2R ladder network as shown in the fig.3.2. The IC used for this purpose is DAC7541, which is a 12-bit chip. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp, which is also at a virtual ground. Since both the terminal of switches di are at ground potential, current flowing in the resistance is constant and independent of switch position i.e., independent of input binary word. When switch di is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch di is at logical '1' i.e., to the right , the current through 2R sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or the left of any nodes is exactly 2R. the equal division of current in successive nodes remains the same in the inverted 'R-2R ladder ' irrespective of the input binary word. Thus the current remains equal in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltage remain constant at $VR/2^0$, $VR/2^1$, $VR/2^2$,........ $VR/2^n$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode of inverted ladder is that since the ladder node voltage remains constant even with changing input binary words , the stray capacitance are not able to produce slow down effects on the performance of the circuit.

According to bit di, the corresponding switch get connected either to ground for di = 0 or to positive for di = 1. The current flows into the inverting input terminal from $+V_R$ for di = 1 and from $+V_R$ for di = 0, regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant. However the current through the feedback resistor R is the summing current depending upon the input binary word. The DAC is a voltage driven one.

3.2.3 PROGRAMMABLE PERIPHERAL INTERFACE:

For peripheral interfacing of devices we use a interfacing chip. The chip used is 8255. The 8255 is a general purpose programmable input/output device. It is a 40 pin IC in Dual-In line Package. It has 24 input/output pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

In first mode (MODE 0) each group of 12 input/output pins may be programmed in sets of 4 to be input or output. In MODE 1, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for hand shaking and interrupt control signals. MODE 2 is a bi-directional bus mode which uses 8 lines for a bi-directional bus, and 5 lines borrowing one from the other group fo5r hand shaking. The 8255 contains three 8 bit ports (A,B and C). All can be configured or "personality" further enhance the power and flexibility of the 8255.

Port A: one 8 bit data output latch/buffer and one 8 bit data input latch.

Port B: one 8 bit data input/output latch/buffer and one 8 bit data input latch.

Port C: one 8 bit data output latch/buffer and one 8 bit data input buffer (no latch for input). This port can be divided into two 4 bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

The functional configuration of each port is programmed by the system's software. In essence, the CPU 'outputs' a control word to the 8255. The control work contains information such as "mode" , " bit set" , " bit reset " etc., that initialise the functional configuration of 8255. Each of the control blocks (Group A group B) accepts command from the Read/Write control logic, receives " control words" from the internal data bus and issue the proper commends to its associated ports. No read operation of control word register is allowed.

A high on the reset input pin clears the control register and all ports (A,B,C) are set to the input mode. A low CS on this pin enables the communication between 8255 and the CPU. A 'low' on RD enables the 8255 to send the data of status information to the CPU to read from the 8255A. A 'low' on this WR pin enables the CPU to write the data or control words into the 8255 A.

A0 and A1 are the port select pin. These input signals in conjunction with the RD and WR inputs control the selection of one of the three ports, to the control work registers. They are normally connected to the least significant bits of the address bus.

CHAPTER IV

DC DRIVE

4.1 DC SHUNT MOTOR:

Characteristics of shunt motors:

4.1.1 Ta/Ia CHARACTERISTICS:

Assuming flux to be practically constant (though at heavy loads, flux decreases somewhat due to increased armature reaction) we find that Ta directly proportional to flux.

Hence, the electrical characteristic as shown in fig. 4.1 is practically a straight line through the origin. Shaft torque is shown dotted. Since a heavy starting current shunt motor should never be started on (heavy) load.

4.1.2 N/Ia CHARACTERISTICS:

If flux is assumed constant, then N is directly proportional to Eb. As Eb is also practically constant, speed for most purpose , is constant.

But strictly speaking both Eb and flux decrease with increasing load. However, Eb decreases slightly drooping as shown by the dotted line in fig. 4.2. But for all practical purposes, shunt motor is taken as a constant speed motor.

Because there is no appreciable change in the speed of a shunt motor from no load to full load, it may be connected to loads which are totally and suddenly thrown off without and fear of excessive speed resulting. Due to the constancy of their speed, shunt motors are suitable for driving, shafting, machine tools, lathes wood-working machines and for all other purposes where an approximately constant speed is required.

4.1.3 N/Ta CHARACTERISTICS:

It can be deduced from Ta/Ia and N/Ia characteristics above and shown in fig.4.3

4.2 <u>SPEED CONTROL TECHNIQUES :</u>

There are three methods by which speed of a DC shunt motor can be controlled. Out of this there are two common methods and less common method in use. The common ways in which the speed of a shunt dc machine can be controlled are by:

1) Adjusting the field resistance Rf.
2) Adjusting the terminal voltage applied to armature.
3) Inserting a resistor in series with the armature circuit.

These methods are discussed in detail as below.

4.2.1 CHANGING THE FIELD RESISTANCE:

When the field resistor of DC motor is changed, assume that field resistor increases and observe the response. If the field resistance increases, then the field current decreases, and as the field current decreases, the flux decreases with it. A decrease in flux causes an Ea which causes a large increase in the machine's armature current, since

Ia = (Vt – Ea)/Ra --------------------------------4.1

The induced torque in a motor is given by

T ind = K_0 Ia --------------------------------4.2

The increase in current predominates over the decrease in flux and the induced torque rises.

Since T ind >T load, motor speeds up.

However as the motor speeds up, the internally generated voltage Ea rises, causing Ia to fall. As Ia falls the induced torque T ind falls too and finally T ind again equals T load at a higher steady state speed than originally.

To summarize the cause and effect behavior involved in this method of speed control:

(a) Increasing Rf causes If to decrease.

(b) Decreasing If decreases 0.

(c) Decreasing 0 lowers Ea.

(d) Decreasing Ea increases Ia.

(e) Increasing Ia increased T ind, with the change in Ia dominant over the change in flux.

(f) Increasing T ind makes T ind > T load, and the speed W increases.

(g) Increasing Ea decreases Ia.

(h) Decreasing Ia decreases T ind until T ind = T load at a higher speed W.

The effect of increasing in the field resistance on the output characteristics of a shunt motor is shown in figure. Notice that as the flux in the machine decreases the no load of the motor increases, while the slope of the torque-speed curve becomes steeper. Naturally, decreasing Rf would reverse the whole process and the speed of the motor would drop.

Fig. 4.4 shows the terminal characteristics of the motor over the range from no load to full load conditions. Over this range an increase in field resistance increases the motor's speed as said above.

Fig. 4.5 shows the terminal characteristics of the motor over the full range from no load to stall conditions. It is apparent from the fig. 4.6 that at very slow speeds an increase in field resistance will actually decrease the speed of the motor. This effect occurs because at very low speeds, the increase in armature current caused by the decrease in Ea is no longer large enough to compensate for the decrease in the flux in the induced torque equation. With the flux decrease, actually larger than the armature current increases the induced torque, decreases and the motor slows down.

4.2.2 CHANGING THE ARMATURE VOLTAGE:

The second form of speed control involves changing the voltage applied to the armature of the motor without changing the voltage applied to the field. A connection similar to that in fig. 1.6 is necessary for this type of control. In effect, the motor must be separately excited to use armature voltage control.

If the voltage Va is increased, then the armature current in the motor must rise. As Ia increase, the induced torque T ind increases, making T ind > T load and the speed W of the motor increases.

But as the speed W increases, the internally generated voltage Ea increases, causing the armature current to decrease. This decrease in Ia decreases the induced torque causing T ind to equal T load at a higher rotational speed W.

To summarize the cause and effects behavior in this method of speed control.

1. An increase in Va increases Ia.
2. Increasing Ia increases T ind.
3. Increasing T ind makes T ind > T load, increasing W
4. Increasing W increase Ea
5. Increasing Ea decreases Ia
6. Decreasing Ia decrease T ind until T ind = T load at higher W

The effect of an increase in Va on t 789he torque – speed characteristics of a separately excited motor is shown in fig. 4.7. Notice that the no-load speed of the motor is shifted by this method of speed control but the slope of the curve remains constant.

4.2.3 INSERTING A RESISTOR IN SERIES WITH THE ARMATURE CIRCUIT:

If a resistor is inserted in series with the armature circuit, the effect is to drastically increase the slope of the motor's torque-speed characteristics, making it to operate slowly if loaded as more slowly if loaded as shown if fig. 4.8. The insertion of a resistor is a very wasteful method of speed control, since the losses in the inserted resistor are very large. For this reason it is rarely used. It will be found only in applications in which the motors spends almost all its time operating at full speed of in applications too inexpensive to justify a better form of speed control.

4.2.4 FULL WAVE HALF CONTROLLED BRIDGE RECTIFIER:

A variable DC voltage is required to vary the speed of the DC motor. This is obtained by controlling the firing angle of SCR. The circuit used for controlling the firing angle is called as controlled rectifier or converters.

Fig. 4.9 shows a half controlled bridge circuit. The main difference between a fully-controlled circuit and a half-controlled circuit is that the former can operate as an inverter when the firing angle is between 90 and 180, and the latter can operate only in the rectifying mode as the firing angle changes from zero to 180.

Since the cathodes of the two SCRs are at the same potential, their gates can be connected and a single gate pulse can be used for triggering either SCR. The SCR which has the forward bias at the instant of firing will turn on.

In the fig. 4.10 the free wheeling action will take place through 1 and 1' or 2 and 2' when the input voltage polarity is reversed. Therefore, SCR 1 will not be turned off even though the input current iL and the output voltage Eo go to zero. The output voltage and current waveforms are as shown in fig. 4.11. In the circuit discussed above, the input power factor is poor when the DC power output voltage and power, it is necessary to devise a method by which the phase angle of the line current iL with respect to the input voltage can be kept reasonably small as the firing angle of the SCRs is varied. This is achieved by connecting a fully controlled bridge in series with an uncontrolled bridge.

4.3. <u>HARDWARE DESCRIPTION:</u>

The circuitry can be broadly sub-divided into three portions for the purpose of simplicity. The sub-divisions are as follows:

1) Power circuit
2) Control circuit

4.3.1. POWER CIRCUIT:

The power circuit acts as the heart of the hardware. It is implemented for the purpose of the supplying power toe various ICs. It consists of a centre tapped transformer, a rectifying unit (Bridge Rectifier) and a regulator unit.

The centre tapped transformer steps down the 230V,50 Hz source to 12-0-12V, 50Hz supply. This alternating supply is fed to the bridge rectifier whose output is a pulsating DC. The pulsating DC is fed to a 3 pin IC regulator 7805 whose output is a regulated +5V DC. We also make use of 7812 and 7912, 3 pin IC regulators for providing +12V and –12V DC, which is needed for LM324.

4.3.2 CONTROL CIRCUIT:

The main aim of the project is to maintain a constancy in speed of motor at any condition for which we are in need of the control circuit. The control circuit is used to produce gate control to the SCR. Now we shall have an outlook of various ICs which plays a major role.

We have used a proximity switch to get the feed back signal. An LM331 IC is used whose main function is conversion of frequency in to voltage. LM324 used in the hardware is an integrated circuit, consisting of 4 operational amplifiers. Each one can be used as a comparator, an adder, a zero crossing detector, a buffer and an inverting amplifier. We have designed an integrated circuit comprising of a transistor, resistor, capacitor which converts a pulse input at the base of transistor into a ramp output at the collector terminal. A 555 timer in monostable mode is used as a wave shaper. A Darlington pair is used to drive the pulse transformer.

In the above paragraph we have given a general idea of the ICs used . The following section deals with the principle of operation.

4.3.3 OPERATIONAL AMPLIFIER:

An operational amplifier is a direct – coupled high gain amplifier usually consisting of one or more differential amplifier. The operational amplifier is a versatile device that can be used to amplify DC, AC input signals and also it can be used for computing such mathematical functions as addition, subtraction, multiplication and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to OP – AMP.

Here we use the op-amp as inverting amplifier, comparator, adder and zero crossing detector.

4.3.4 INVERTING AMPLIFIER:

Here, the output voltage is fed back to the inverting input terminal through feedback resistor. Input signals applied to the inverting input terminal and non-inverting input terminal of op-amp is grounded.

The closed loop gain, Acl = Vo / Vi = - Rf / R1

The negative sign indicates a phase shift of 180 between input and output voltages. Fig 4.12 shows an inverting amplifier.

4.3.5 COMPARATOR:

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp.

There are basically two types of comparators

1) Non-inverting comparator
2) Inverting comparator

Fig. 4.13 and 4.14 show ideal and practical non-inverting comparator respectively.

Fig. 4.15 and 4.16 show input and output waveforms for positive and negative reference voltage respectively.

In noninverting comp0aarator, a fixed reference voltage V ref is applied to negative input and time varying signal Vi is applied to positive input. The output voltage is at –V sat for Vi <Vref and Vo goes into +V sat for Vi> Vref. Figure 2.6 shows an inverting comparator.

Figure 4.17 and 4.18 show input and output wave forms for positive and negative reference voltages respectively.

4.3.6 ZERO CROSSING DETECTOR:

The basic comparators can be used as a zero crossing detector provided that Vref is set to zero. An inverting zero crossing detector is shown in fig. 4.19 and the output wave form for a sinusoidal input signal also shown in fig 4.20.

4.3.7 ADDER:

The fig. 4.21 shows the inverting summing amplifier. Here, the number of inputs is two Va,Vb.

$$\left.\begin{aligned} \text{The closed loop gain, Acl} &= Vo / Vi \\ &= Vo / (Va + Vb) \\ &= -Rf / R \end{aligned}\right] \quad \text{---------------4.1}$$

where,

R = Ra = Rb.

If Ra # Rb then,

$$\text{Output voltage } Vo = -[Va(Rf/Ra) + Vb(Rf/Rv)] \quad \text{---------------4.2}$$

Thus the output voltage is the sum of individual gain of the respective loop.

4.3.8 VOLTAGE FOLLOWER:

The lowest gain that can be obtained from a noninverting amplifier with feedback is 1. When the noninverting amplifier is configured for unity gain, it is called a voltage follower because the output voltage is equal to and in phase with the input. In other words, in the voltage follower the output follows the input.

Although it is similar to the discrete emitter follower, the voltage follower is preferred because it has much higher input resistance, and the output amplitude is exactly equal to the input.

The voltage follower circuit is as shown in the fig. 4.22. In this figure all the output voltage is fed back into the inverting terminal of the op-amp; consequently the gain of the feedback circuit is 1 (B = Af = 1).

Since the voltage follower is a special case of the non-inverting amplifier, all the formulae developed from the later are indeed applicable to the former except that the gain of the feedback circuit is 1 (B = 1). The formulae are:

Af = 1
Rif = AR I
Rof = Ro / A
Ff = Afo
Vout = + Vsat /A, since (1+A) = A

Where,

Af is closed loop voltage gain
Rif is input resistance with feedback
Rof is output resistance with feedback
Ri, Ro are input aand output resistances without feedback

A is open loop voltage gain

Fo is breaking frequency of op-amp

Ff is baandwidth with feedback

Vout is total output offset voltage with feedback

Vsat is saturation voltage.

The voltage follower is also called a NON – INVERTING BUFFER because when placed between two networks it removes the loading on first network.

4.3.9 Monostable Multivibrator:

The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays of oscillation. It operates in one of the two modes: either as a monostable (one shot) or as an astable (free running)..

A monostable multivibrator is a pulse generating circuit in which the duration of pulse is determined by the Rc network connected externally to the 555 timer. In a stable of stand by state the o/p of the circuit is approximately zero of at logic low level, when an external trigger pulse is applied, the output is forced to go high. The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state(output low), hence the name monostable. Normally, the output of the monostable multivibrator is low.

Fig. 4.23 shows input and output wave forms of 555 monostable multivibrator.

The time during which the output remains high is given by

$$t = 1.1\,R\,C \quad \text{(seconds)} \qquad \text{------------------------}4.3$$

where,

R is in Ohms

C is in farads

4.4 FUNCTIONAL DESCRIPTION:

In the preceding section, the need and functions of various ICs have been listed out. Now in this section we will deal with the working principle of the hardware in detail.

The block diagram of the hardware is shown in fig. 4.24.

AC supply of 12V, 50Hz is fed to the full wave rectifying unit which produces a pulsating DC output. This is fed to the inverting pin of zero crossing detector. From a resistor divider network a fraction of voltage is fed to the non-inverting input of zero crossing points of the pulsating DC.

A ramp generator is designed using a transistor, a resistor and a capacitor. When the output of the zero crossing detector is low, the transistor is in cut-off state, which results in charging of the capacitor. The transistor will be in the active region when the output of the zero crossing detector goes high. The capacitor discharges suddenly through the transistor, when the transistor is properly biased. The consequence of this action is generation of a ramp signal. An op-amp in buffer mode is used for impedance matching. Now the ramp signal form the buffer is fed to the inverting pin of comparator.

A 1K pot is used for the purpose of setting the speed at a particular value. The inverted output of f/v converted is added with the reference voltage in the adder circuit constructed using op-amp. The 4.7 K at the non-inverting pin is used for the purpose of thermal stability. Initially when there is no output from the adder, the potential at the non-inverting input is about 6V. As the voltage at the adder output terminal is sensed, potential at the non-inverting pin reduces gradually. The peak value of the ramp input at the non-inverting pin of the comparator is about 5V. The comparator compares the ramp input and the potential at non-inverting input and its output is in the form of a pulse. The width of the pulse is proportional to the speed of the motor. The pulse output is differentiated through a RC network.

A 555 timer in monostable mode is used to detect the transients from low to high and vice versa. By this gate dissipation can be minimized. This pulse signal is fed to the base of the BC 147, common emitter transistor whose output is in the inverted form of the input. This negative going pulse biases the transistor BC 157 and the positive going pulse is produced at the collected output to which the pulse transformer primary is connected. The pulse transformer drives the gate of the SCR1 and SCR2. The major advantage of BC 157 and BC 147 is that the pulse within the former can be minimum so that the gate dissipation is kept at a minimum.

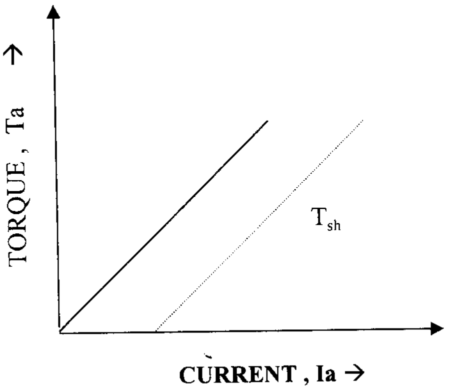


FIG. 4.1 Ta/Ia CHARACTERISTIC

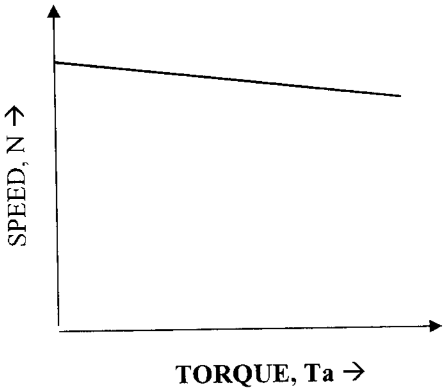


FIG.4.2 N/Ia CHARACTERISTIC

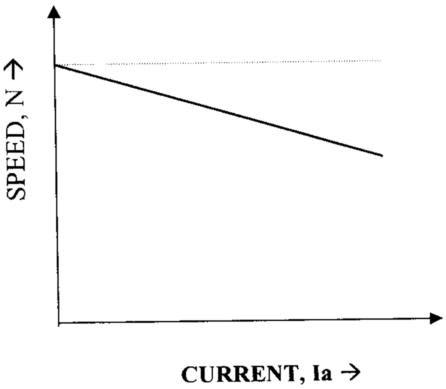


FIG 4.3 N/Ia CHARACTERISTIC

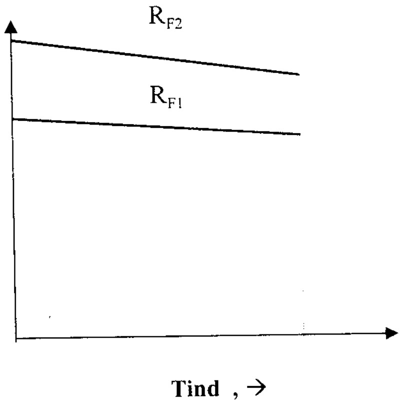


FIG 4.4 NORMAL OPERATING RANGE OF MOTOR

$R_{F2} > R_{F1}$

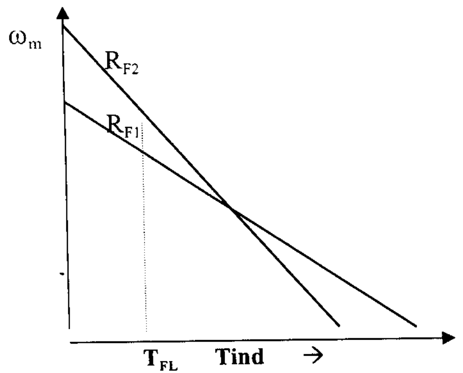


FIG. 4.5 THE ENTIRE RANGE OF OPERATOIN, FROM NO LOAD TO STALL CONDITION

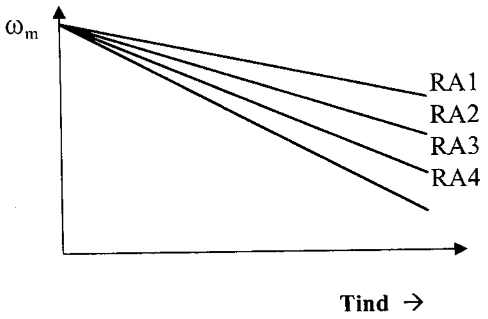


FIG. 4.6 THE EFFECT OF ARMATURE RESISTANCE SPEED CONTROL ON A SHUNT MOTOR'S TORQUE-SPEED CHARACTERISTICS
RA1<RA2<RA3<RA4

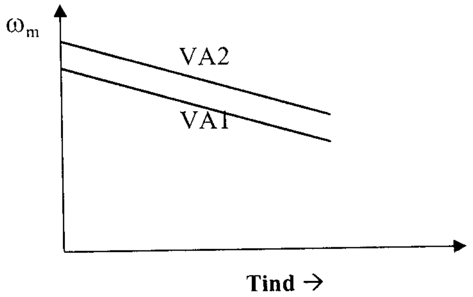


FIG. 4.7 THE EFFECT OF ARMATURE SPEED CONTROL ON A SHUNT MOTOR'S TORQUE-SPEED CHARACTERISTICS
VA2>VA1

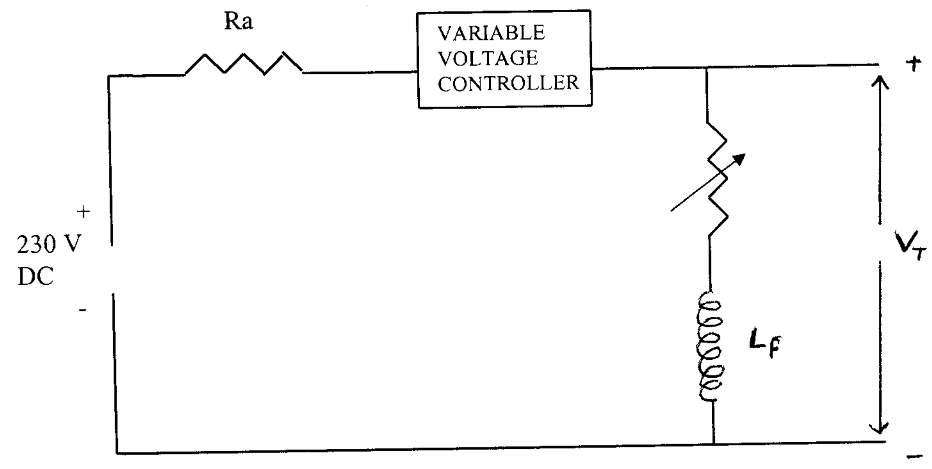


FIG. 4.8 ARMATURE CONTROL OF DC SHUNT MOTOR

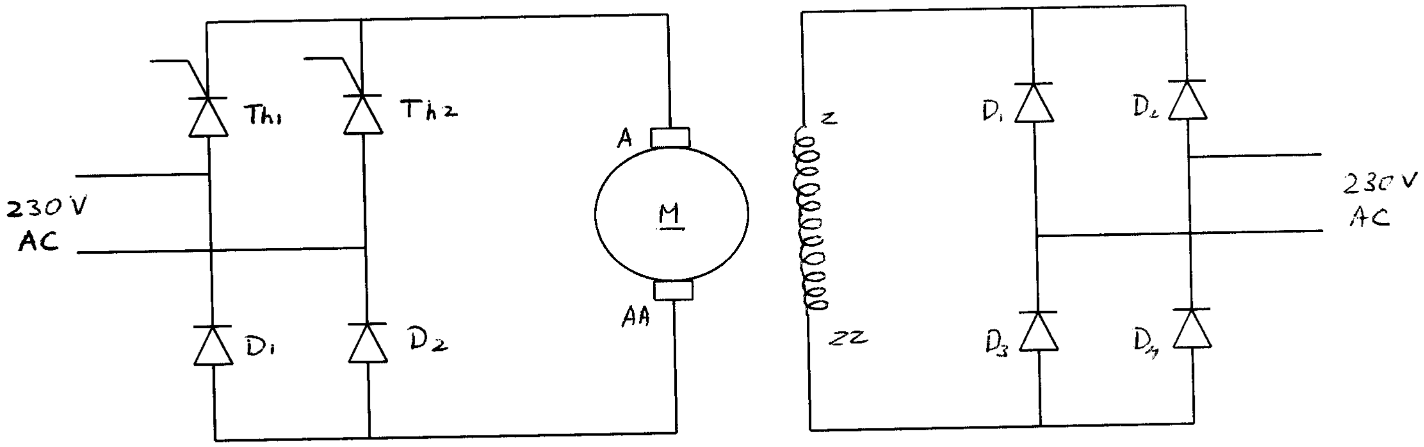


FIG 4.9 SCHEMATIC DIAGRAM OF DC DRIVE

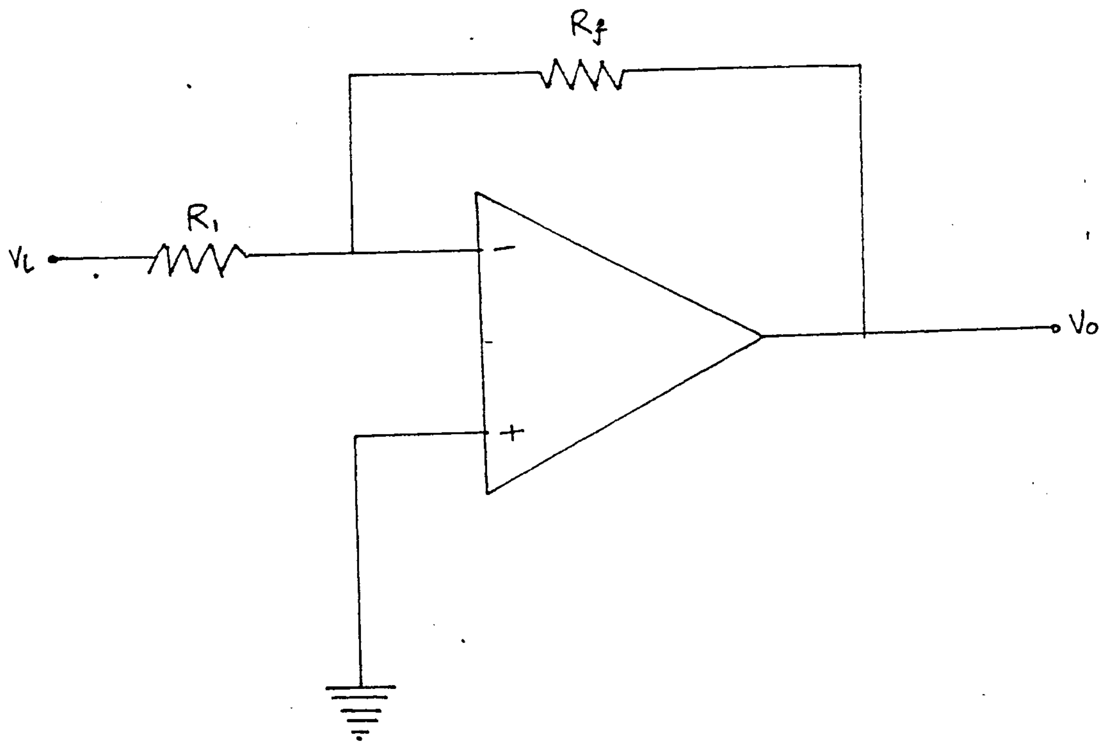


FIG. 4.10 INVERTING AMPLIFIER

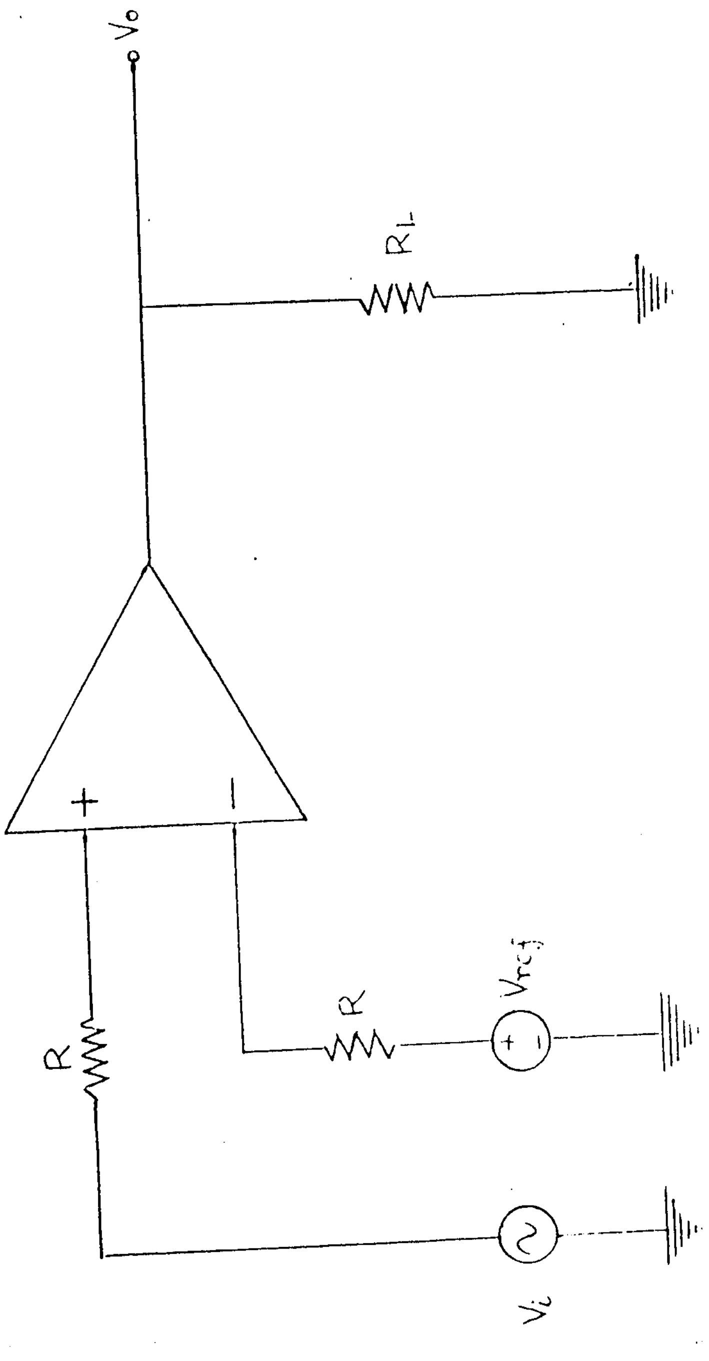


FIG. 4.1 NONINVERTING COMPARATOR

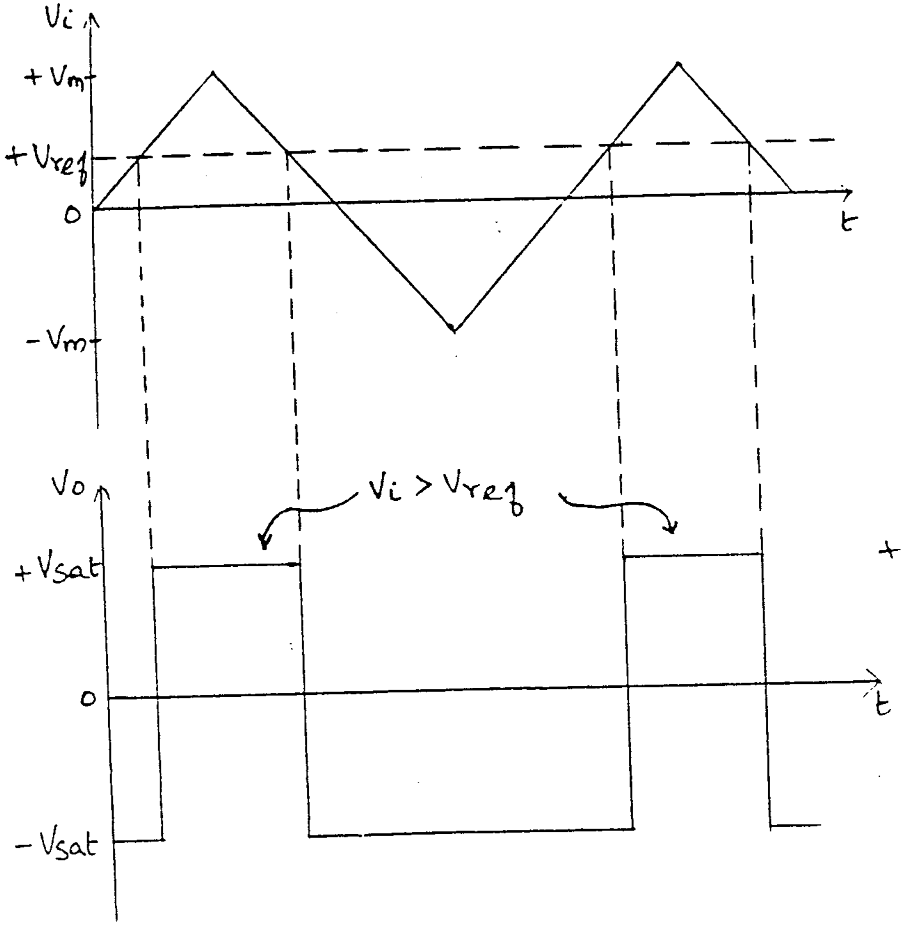


FIG. 4.12 I/O WAVEFORMS
FOR V ref Positive

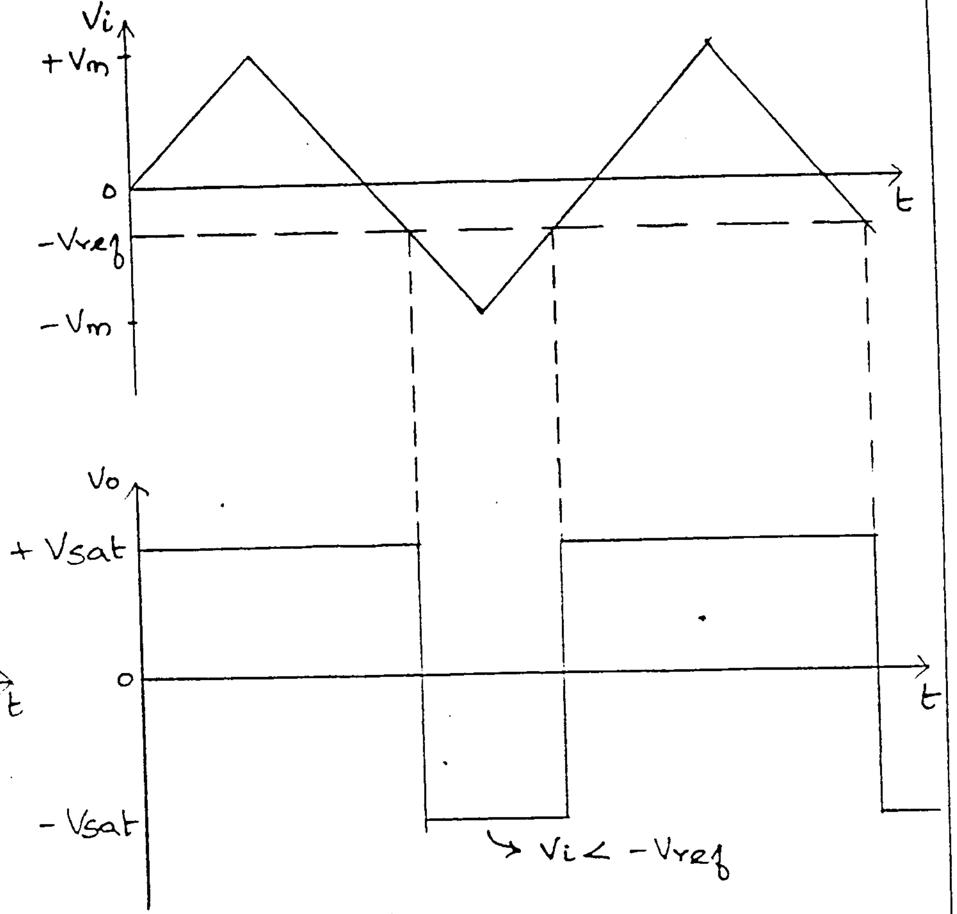


FIG. 4.13 I/O WAVEFORMS FOR
V ref Negative

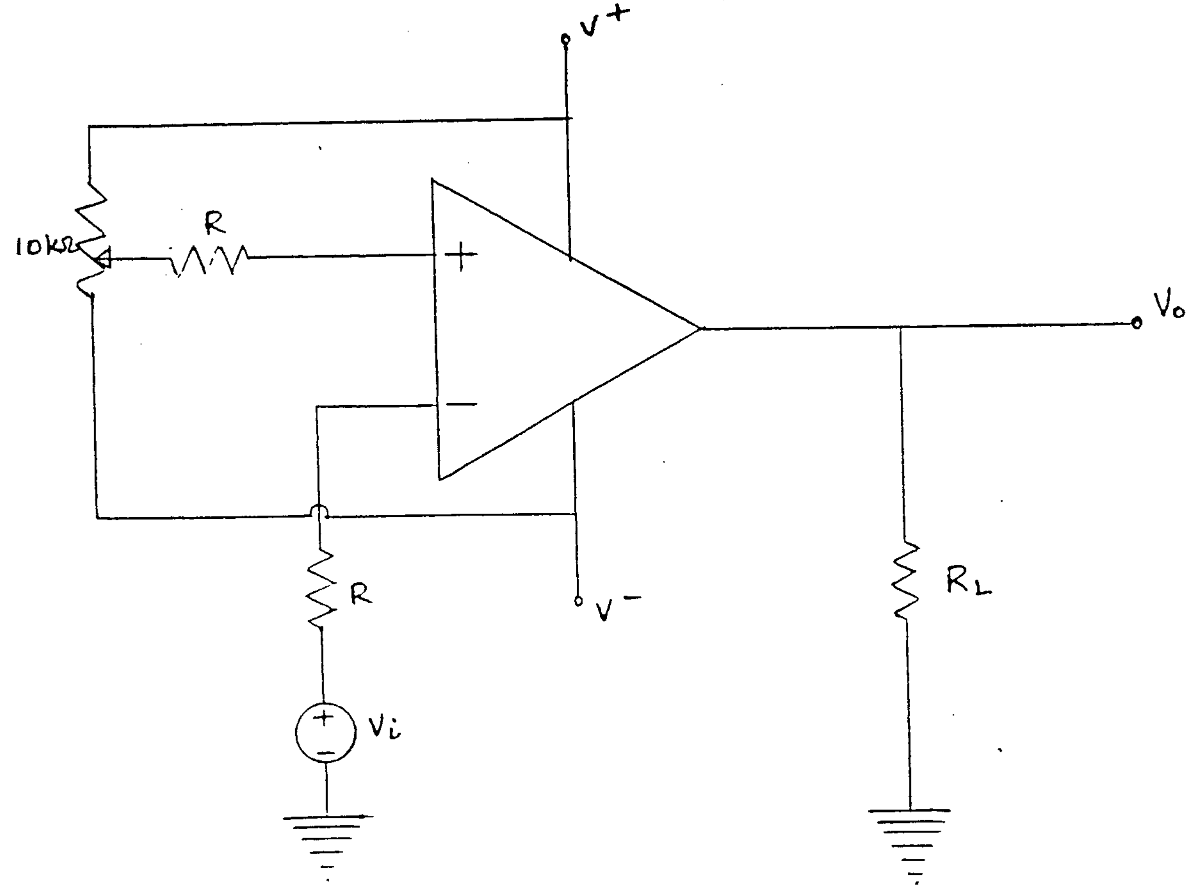


FIG. 4.14 INVERTING COMPARATOR

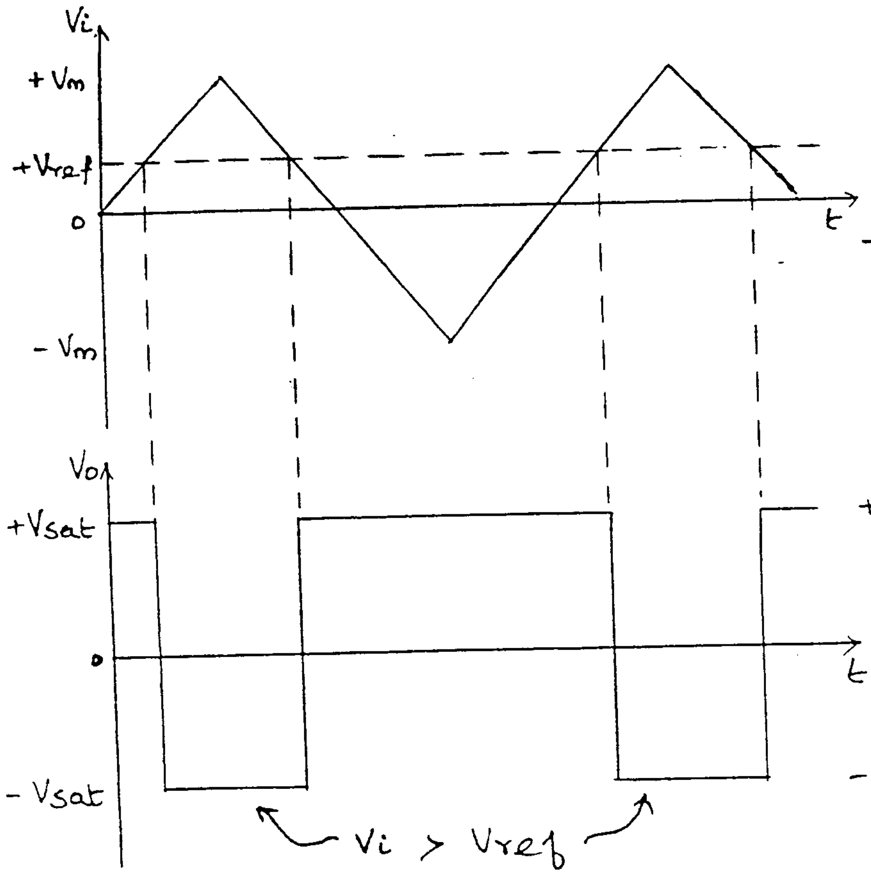


FIG.4.15 I/O WAVEFORMS FOR
V ref POSITIVE

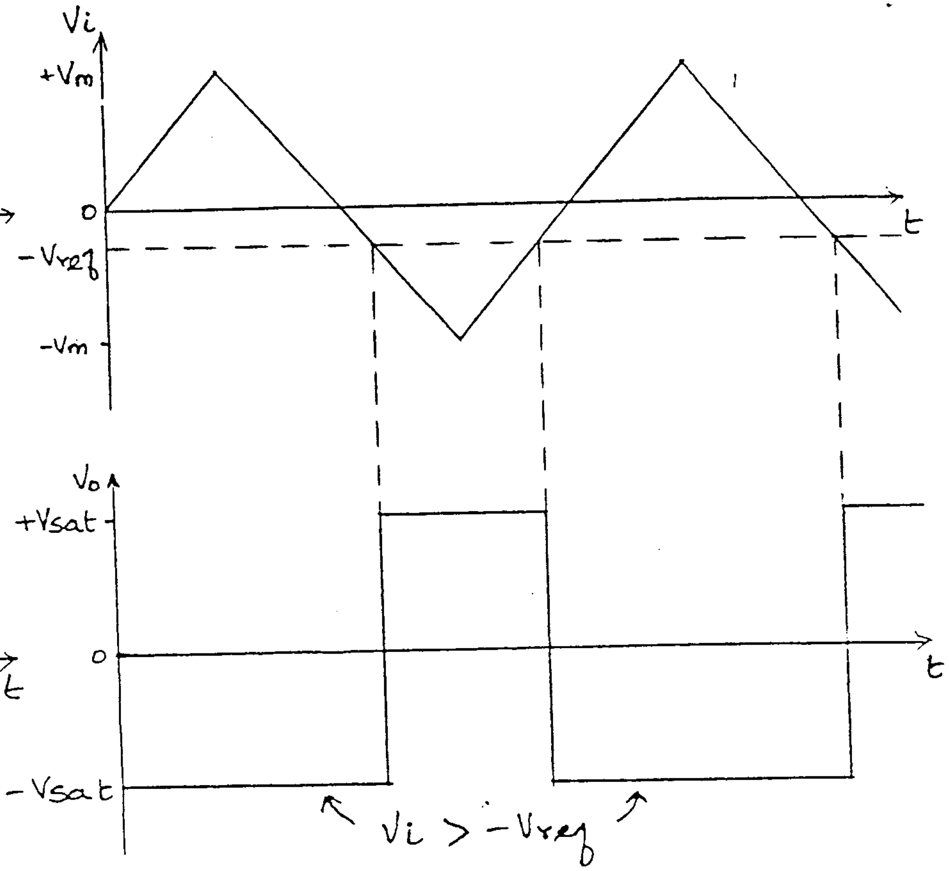


FIG.4.16 I/O WAVEFORMS FOR
V ref NEGATIVE

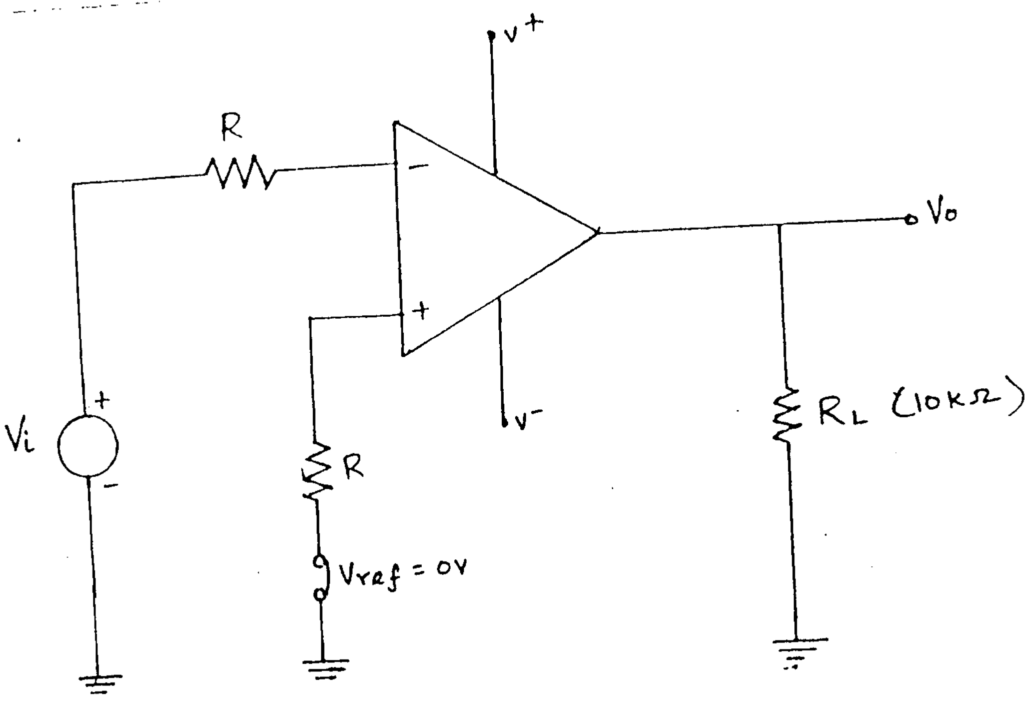


FIG. 4.17 ZERO CROSSING DETECTOR

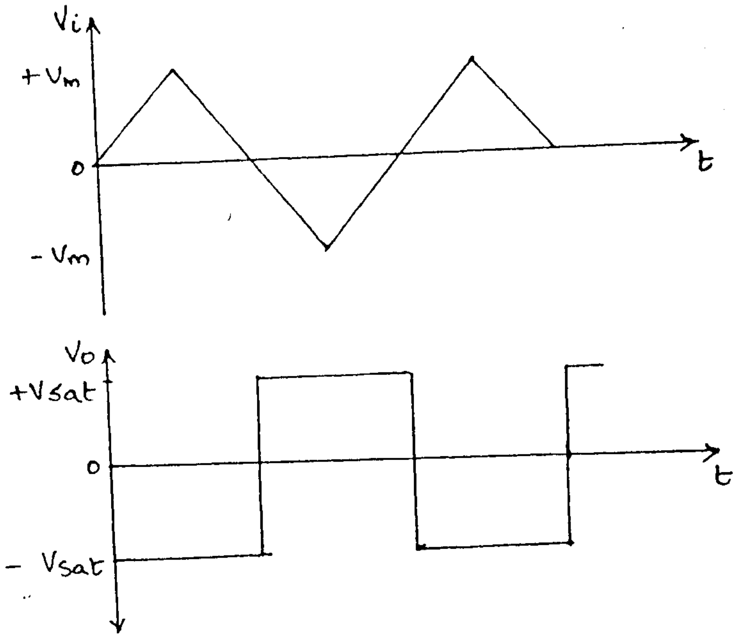


FIG. 4.18 I/O WAVEFORMS

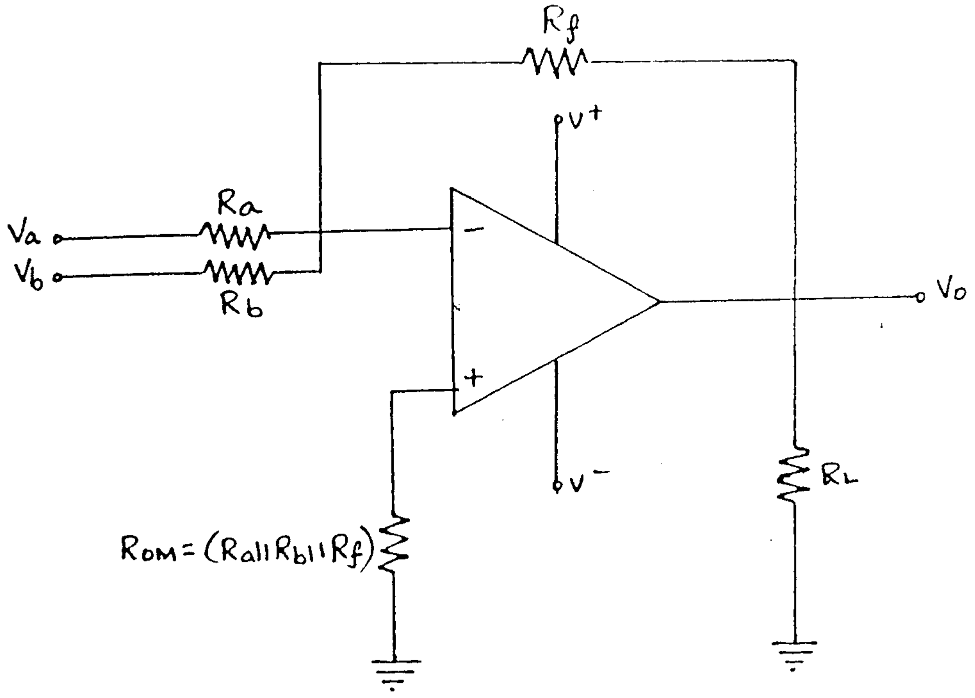


FIG. 4.19 INVERTING SUMMING AMPLIFIER

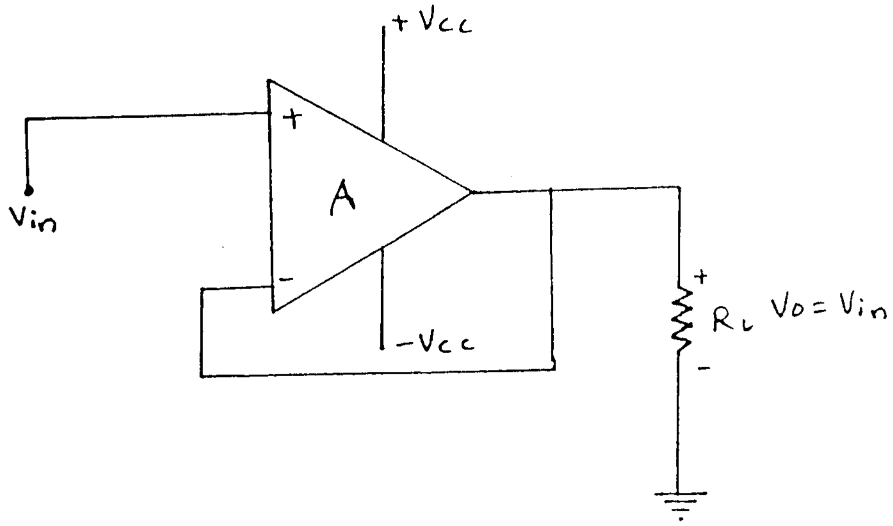


FIG. 4.20 VOLTAGE FOLLOWER

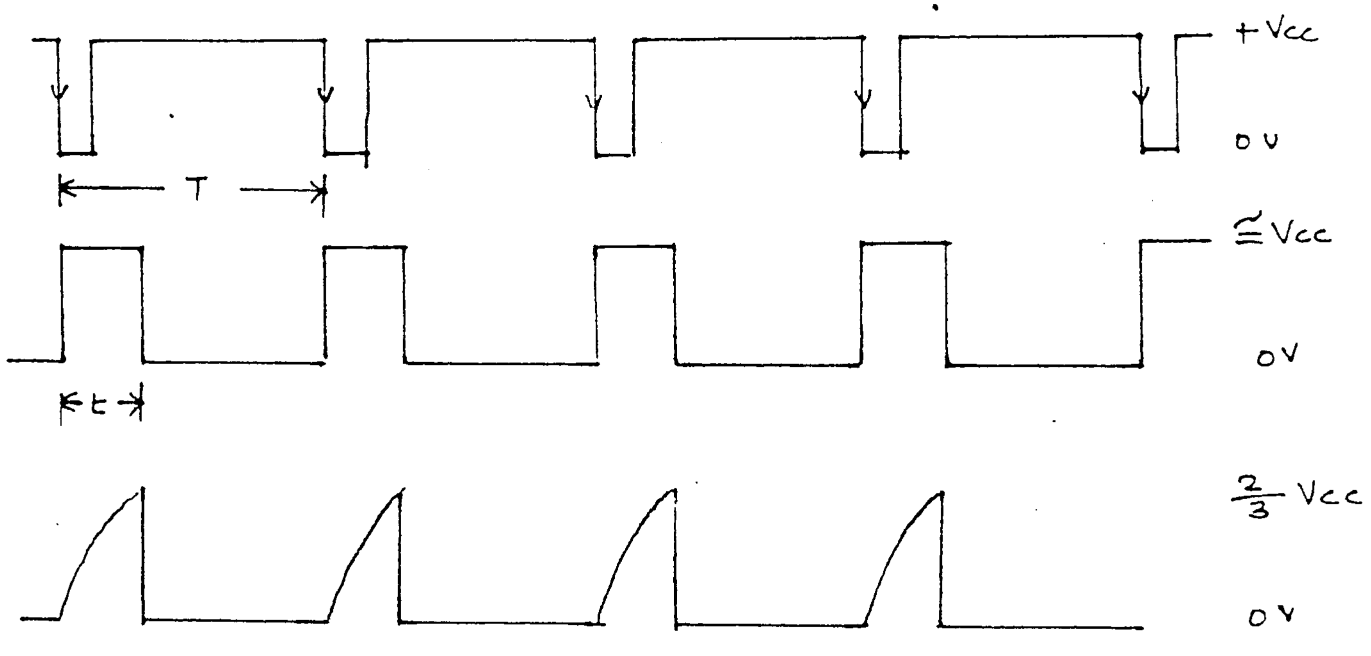


FIG.4.21 I/O WAVEFORMS OF 555 MONOSTABLE MULTIVIBRATOR

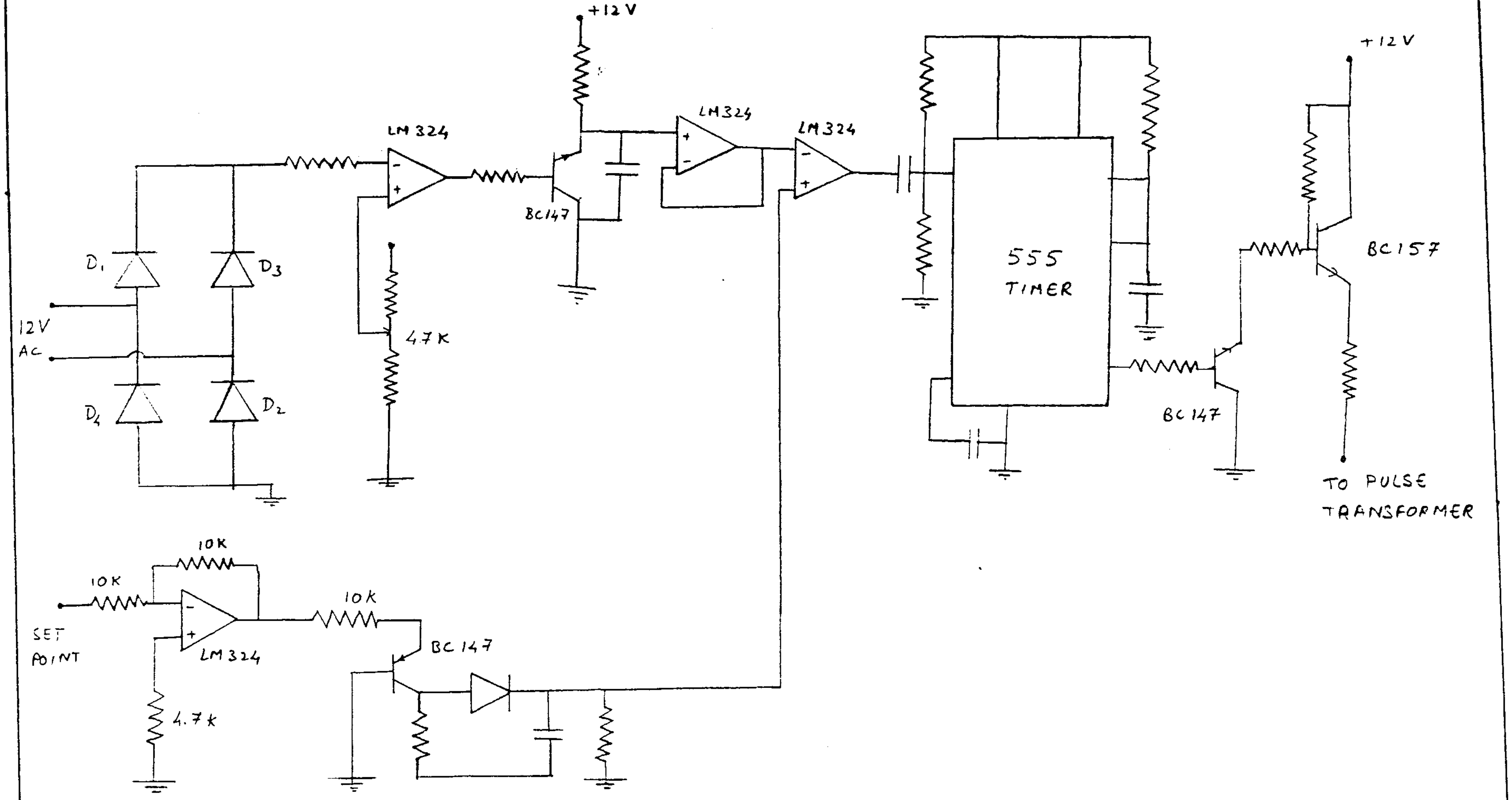


FIG.4.22 CIRCUIT DIAGRAM OF DC DRIVE

CHAPTER V

SOFTWARE

5.1 INTRODUCTION TO FUZZY LOGIC:

Fuzzy logic is a logic system which is much closer in spirit to human thinking and natural language than traditional logic system.

Ordinary logic deals with true or false, while fuzzy logic deals with proportion that can be fuse to a certain degree- somewhere from 0 to 1. Therefore proportion truth value indicates the degree of certainty about which the proportions is true. The degree of certainty sounds like probability. But it is not quite toe same. Probabilities for mutually exclusive events cannot add up to more than 1, but their fuzzy values may. Fuzzy values need not add up to 1. There is no restriction on what there values must add up to.

5.1.1 FUZZY LOGIC CONTROLLER:

A control system is a close-loop system that typically controls a machine to achieve a particular desired response, given a number of environmental inputs. A fuzzy control system is also a closed loop system that uses the process of fuzzification, to generate fuzzy input to an inference engine, which is a knowledge base of actions to take. The inverse process called defuzzification is also used in a fuzzy control system to create crisp, real values to apply to the machine of process under control.

The principal components of a FLC are:

a) Fuzzification interface (Fuzzifier).

b) A Knowledge Base .

c) Decision making logic.

d) Defuzzification interface (Defuzzifier).

a) The fuzzifier involves the following functions

- ❖ Measure the values of input variables.
- ❖ Performs a scale mapping that transforms the range of values of input variables into corresponding universe of discourse.
- ❖ Performs the function of fuzzification that converts the input data into a suitable linguistic value which may be viewed as labels of fuzzy sets.

b) The knowledge base comprises a knowledge of the application domain and the attendant control goals. It consists of a 'data base' and a 'Linguistic fuzzy control rule base'.

- ❖ The data base provides necessary definition which are used to define linguistic control rules and fuzzy data manipulation in a FLC.
- ❖ The rule base characterizes the control goals and control policy of the domain experts by means of linguistic control rules.

c) The decision making logic is the kernel of an FLC, it has the capability of simulating human decision making based on fuzzy concepts and of interring fuzzy control action employing fuzzy implication and the rules of inference in fuzzy logic .

d) The defuzzifier performs the following functions:

- ❖ A scale mapping which converts the range of output variables into corresponding universe of discourse.
- ❖ Defuzzification, which yields a non-fuzzy control activities from an inferred fuzzy control action.

5.1.2 IMPACT OF FLC OVER CONTROL:

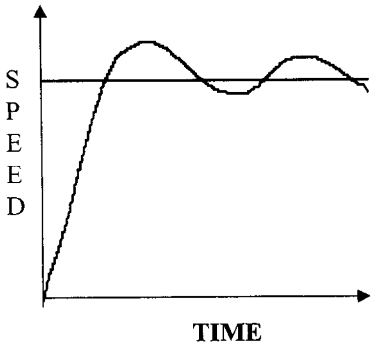
The conventional PID controller is governed by the characteristic equation given below.

$$U(t) = Kp\ e(t) + Ki \int e(t)\ dt\ + kd\ de(t)/dt$$

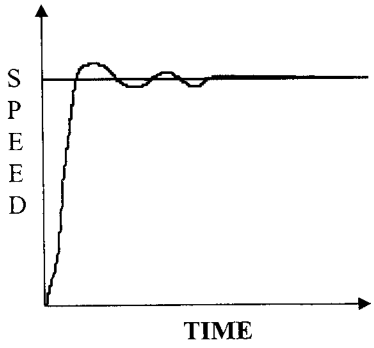
Here, U(t) is the control signal, e(t) is the error signal between the reference and the process output and Kp,Ki and Kd are proportional, integral and derivative gains respectively. The entire system performance depends only on these system parameters. So the performance can't be improved to a greater extend.

Where as in case of fuzzy logic controller (FLC), it is not governed by any characteristic equations as in case of conventional PID controller. Here the crisp values are converted to linguistic variables say zero, small, medium, large, very large and these values are processed by English like rule and finally value is converted back to crisp value.

The advantage of the FLC over the PID controller can be well understand, if we analysis the step input response of both the system.



PID CONTROLLER



FLC

It is seen from the graph that the transient time is greater for PID controller than that of FLC. It should be noted that the accuracy and the response is higher in the case of FLC, but not so in case of PID controller. Sometimes, in PID controller, the desire speed will not be achieved.

5.2 WORKING OF A FLC:

The FLC works in three steps. They are

1) Fuzzification
2) Rule Evaluation
3) Defuzzification.

5.2.1 FUZZIFICATION:

Fuzzification is related to the vagueness and imprecision in a natural language. It is a subjective valuation which transforms a measurement into a valuation of a subjective value and hence it could be deigned as a mapping from an universe of discourse. Fuzzification plays an important role in dealing with uncertain information which may be objective of subjective in nature.

`For fuzzy control application the observed date are usually crisp. Since the data manipulation in the FLC is based on fuzzy set theory, fuzzification is necessary during an earlier stage.

A fuzzification operator conceptually converts a crisp value into a fuzzy singleton with a certain universe of discourse. Basically a fuzzy singleton is a precise value and hence no fuzziness is introduced in this case. This strategy had been widely used in fuzzy control applications since it is natural and easy to implement.

Observed data are disturbed by random noise. In this case a fuzzification operator should convert the probabilistic data into a fuzzy number i.e., fuzzy data. In this way, computational efficiency is enhanced since fussy number are much easier to manipulate then random variables. An isosceles triangle was chosen to be the fuzzification function. The vertex of this triangle corresponds to the mean value of a data set, while the base is twice the standard derivation of the data set.

In a large scale systems and other applications, some observations relating to the behavior of such system are precise, while others are measurable only in a statistical sense, and some referred to as 'Hybrids', require both probabilistic and possibilistic modes of characterization. The strategy of fuzzification in this case is to use the concept of hybrid numbers, which involves both uncertainty and randomness.

5.2.2 RULE EVALUATION:

A fuzzy sysstem is characteerized by a set of linguistic statements based on expert knowledge. The expert knowledge is usually in the form of "IF- THEN " rules, which are easily implemented by fuzzy conditional statements in fuzzy logic . the collection of fuzzy control rules but aare expressed as fuzzy conditional statements forms the rules base or the rule set of an FLC.

The inference mechanisms employed in an FLC are generally much simpler then those used in expert system, since in an FLC, the consequent of a rule is applied to the antecdent of another. In other words, in FLC we do not employ the chaining inference mechenism, since the control actions are based on one forward data-driven inference.

The rule base of an FLC is usually derived from expert knowledge. Let us consider the general form of MISO fuzzy control rules in case of two input and one output fuzzy system.

INPUT: x is A' , y is B'

R1 :if x is A1 and y is B1 then z is C1

also R2 : if x is A2 and y is B2 then z is C2

"

"

"

also Rn : if x is An and y is Bn then z is Cn

output : z is C'

where,

x,y and z are linguistic variable representing process state variables and the control variable respectively.

Ai, Bi, and Ci are linguistic values of the linguistic variables x, y, and z in the universe of discourse u,v and v respectively with I = 1,2,....n.

'and' and 'also' used are connectives.

In the processing stage each appropriate rules will be provoked and the results of each rule will be combined to finally generate a crisp composite output. Results can be solved in parallel with hardware and sequentially in software.

5.2.3 DEFUZZIFICATION:

Defuzzification is a mapping from a space of fuzzy control actions defined over an output universe of discourse into a space of non-fuzzy control actions. It is employed because in many practical application a crisp control action is required.

A defuzzification strategy is aimed at producing non-fuzzy control action that best represents the possibility distribution of an inferred fuzzy control action. Unfortunately there is no systematic procedure for choosing a fuzzification strategy. The commonly used defuzzication strategies may be described as:

- The max - criterion
- The mean of maximum
- The center of area.

Max – criterion Method:

The max-criterion produces the point at which the possibility distribution of the control action reaches a maximum value.

Mean of Maximum Method(MOM):

The MOM strategy generates a control action which represents the mean value of all local control actions where membership functions reach the maximum.

Center of Area Method:

The widely used COA strategy generates the center of gravity of the possibility distribution of a control action.

COMPARSON OF DIFFERENT DEFUZZIFICATION STARTEGY:

From the analysis of different strategy concluded that COA strategy yields a superior results. However the MOM strategy yields better transient performance, while COA yields a better steady state performance. When the MOM strategy is used, the performance of an FLC is similar to that of a multilevel relay system. While COA strategy yields result which are similar to those obtainable with a conventional pi controller. An FLC based on the a COA generally yields a lower mean square error than that based on MOM. Further more MOM strategy yields a better performance than Max-criterion strategy.

DESIGN PARAMETER OF THE FLC:

The principal design parameters for an FLC are the following:

1. Fuzzification strategies and interpretation of a fuzzification operator(fuzzifier).

2. Data base:

   - Discretization / normalization of Universes of discourse.
   - Fuzzy partition of input and output spaces.
   - Completeness
   - Choice at membership function of a primary fuzzy set.

3. Rule base:
   - Choice of process state (input) variables and control (output) variables of fuzzy control rules.
   - Source and derivation of fuzzy control rules.
   - Type of fuzzy control rules.

4. Decision – making logic:

   - Definition of a fuzzy implication
   - Interpretation of the sentence connective
   - Interpretation of the sentence connection also
   - Definitions of a compositional operator
   - Inference mechanism.

5. Defuzzifiacation strategies and the interpretation of a defuzzifacation operator (defuzzification)

ALGORITHM FOLLOWED IN DESIGN OF AN FLC:

Suppose we are given a set of desired input - output data pairs:

$$(X_1^{(1)} ,X_2^{(1)}, Y^{(1)}) , (X_1^{(2)} , X_2^{(2)},Y^{(2)}),\ldots\ldots\ldots\ldots\ldots\ldots$$

where X1 and X2 are inputs and y is the output. The task here is to generate a set of fuzzy rules from the desired input - output pairs of (n) and are these fuzzy rules to determine a mapping

$$f: (X1, X2) \quad \rightarrow Y$$

our approach consists of the following five steps:-

STEP-1: divide the input and output spaces into fuzzy regions:

- assume that the domain intervals of X1, X2 and Y are [X1-,X1+], [X1-,X1+] and [Y-,Y_] respectively, where 'domain interval' of a variable means that most probably this variable will lie in this intervel (the value of a variable are allowed to lie outside this intervel).
- divide each domain interval into 2N+ 1 region (Ncan be different for diggerent variable and the leangth of thesee regions can be equal or unequal, denoted by SN(Small N).......S1 (Small 1) , CE (Center), B1(Big1)........ BN(Big N).
- assgin each region a fuzzy membership function. The shape of membership functionmay be triangular, trapezoidal or bell shaped. The shape of FLC

curve does not have any influence, but the number of curves determine the accuracy of the output.

STEP - 2: Generate fuzzy rules from the given data pairs:

- First determine the degree of given $X_1^{(i)}$,$X_2^{(i)}$ and $Y^{(i)}$ in different regions. Consider an example shown in figure 4.1. $X_1^{(1)}$ has degree of 0.8 in B1, degree 0.2 in B2, zero degree in all other regions. Similarly $X_2^{(1)}$ has degree 1 in CE and zero degrees in other regions.
- Second assign a given $X_1^{(i)}$,$X_2^{(i)}$ or $Y^{(i)}$ to the region with maximum degree.

For example : $X_1^{(1)}$ is considered to be in S.

$X_2^{(1)}$ is considered to be in CE.

- Finally obtain one rule from one pair of desired input - output data, example :-

($X_1^{(1)}$,$X_2^{(1)}$, $Y^{(1)}$) ➔ [$X_1^{(1)}$ (0.8 in B1 maximum) . $X_2^{(1)}$ (0.75 in S1 maximum) ; $Y^{(1)}$ (0.9 in CE maximum)] ➔ Rule 1:

IF X1 is B1 and X2 is S1 THEN Y is CE:

($X_1^{(2)}$,$X_2^{(2)}$, $Y^{(2)}$) ➔ [$X_1^{(2)}$ (0.6 in B1 maximum) . $X_2^{(2)}$ (1 in CE maximum) ; $Y^{(2)}$ (0.7 in B1 maximum)] ➔ Rule 2:

If rules generated in this way are “and” rules, i.e., rules in which the conditions of the IF part must be met simulteneously inorder for the result of the THEN part to occur.

STEP-3: Assign a degree to each rule:

Since there are usually lots of data pairs, and each data pair generates one rule, it is highly probable that there will be some conflicting rules i.e., rules that have the same IF part but a different THEN part.

One way to resolve this conflict is to assign a degree to each rule generated from data pairs, and accept only the rule from a conflict grout that have maximum degree. In this way not only the conflict problem resolved, but also the number of rules is greatly reduced.

We use the following product by D(Rule) is defined as

$$D(Rule) = Ma(X1)\ Mb(X2)\ Mc(Y).$$

As example, Rule 1 has degree

$$\begin{aligned} D(Rule\ 1\ ) &= M_{B1}(X_1)\ M_{S1}(X_2)\ M_{CE}(Y). \\ &= 0.8 * 0.7 * 0.9 \\ &= 0.504 \end{aligned}$$

and Rule 2 has degree

$$\begin{aligned} D(Rule\ 2\ ) &= M_{B1}(X_1)\ M_{CE}(X_2)\ M_{B1}(Y). \\ &= 0.6 * 1.0 * 0.7 \\ &= 0.424 \end{aligned}$$

In practice, we often have some a prior information about the data pairs. The expert may suggest that some are very useful and crucial, but others are very unlikely and may be caused just by measurement errors. We can therefore assign a degree to each data pair that represents out belief of its usefulness. In this sense, the data pairs contribute a fuzzy set, i.e., the fuzzy set is defined as the useful measurements a data pair belongs to this set to a degree assigned by a human expert.

Suppose the data pair ($X_1^{(1)}$,$X_2^{(1)}$, $Y^{(1)}$) has a degree M(1), then we redefine the degree of Rule 1 as

D(Rule 1) $= M_{B1}(X_1)\, M_{S1}(X_2)\, M_{CE}M(1)$.

i.e., the degree of a rule is defined as the product of the degree of its components and the degree of data pair that generate this rule.

This is important in practical applications, because real numerical data have different reliabilities. Example some real data can be very dad. For good data we aim higher degrees, and for dad data we assign lower degrees. In this way, human experience about the data in cued in a common base as other information. If one employing objectivity and does not want a human to judge the numerical data, out strategy still works by setting all the degrees of the data pairs equal to unity.

STEP-4: Create a combined fuzzy Rule base:

The form of a fuzzy rule base is illustrated in figure 4.3. We fill the boxes of the base with fuzzy rules according to the following strategy a combined fuzzy rule base is assigned rules from either those generated from numerical of linguistic rules from either those generated from numerical data of linguistic rules (we assume that a linguistic rule also has degree that is assigned by the human expert and reflects the expert's belief of the importance of the rule). If there is more than one rule in one box of the fuzzy rule base, use the rule that has maximum degree.

In this way, both numerical and linguistic information are verified into a common framework. The combined fuzzy rule base. If a linguistic rule is an "and " rule , it fills only one box of the fuzzy rule base; but , if a linguistic rule is an "or" rule (i.e., a rule for which the THEN part follows if any condition of the IF part is satisfied), it fills all the boxes in the rows of columns corresponding to the regions of the IF part.

For example, suppose we have the linguistic rule , If X1 is S1 or X2 is CE , THEN Y is B2

STEP-5 : Determine a mapping based on the combined fuzzy rule base:

We use the defuzzification strategy to determine the output control Y for given inputs (X1, X2) .

```
        /* F U Z Z Y  L O G I C FOR CONTROL SYSTEM */
#include<stdio.h>
#include<conio.h>
   float pb(float x);
   float pm(float x);
   float ps(float x);
   float ze(float x);
   float ns(float x);
   float nm(float x);
   float nb(float x);
   float ps1(float x);
   float ze1(float x);
void main()
{
   int i,j;
   float w[20],sp,t=5.0,m[500],e[500],ce[500];
   float se,sce,tmp1,tmp2,suc,r[25],c[500];
   FILE *fp1,*fp2;
   clrscr();
   fp1=fopen("m.d","w");
   fp2=fopen("c.d","w");
   c[-1]=10.0,e[-1]=0.0;

 scanf("%f",&sp);
 for(i=0;i<=500;i++)
 {

 e[i]=sp-c[i-1];
 ce[i]=e[i]-e[i-1];
 se=(6.0*e[i])/sp;
 sce=(10.6*ce[i]-0.667)/sp;



        /*F U Z Z Y  R U L E S */

    r[1]=(ns(se)<ps1(sce))?ns(se):ps1(sce);
    r[2]=(nm(se)<=ps1(sce))?nm(se):ps1(sce);
    r[3]=(nm(se)<ps1(sce))?nm(se):ps1(sce);
    r[4]=(nb(se)<=ps1(sce))?nb(se):ps1(sce);
    r[5]=(pb(se)<pb(sce))?pb(se):pb(sce);
    r[6]=(pm(se)<ps1(sce))?pm(se):ps1(sce);
    r[7]=(ns(se)<ns(sce))?ns(se):ns(sce);
    r[8]=(pb(se)<ns(sce))?pb(se):ns(sce);
    r[9]=(pm(se)<nb(sce))?pm(se):nb(sce);
    r[10]=(pm(se)<ns(sce))?pm(se):ns(sce);
    r[11]=(ps(se)<ns(sce))?ps(se):ns(sce);
   r[12]=(ze(se)<ns(sce))?ze(se):ns(sce);
   r[13]=(ze(se)<=ze1(sce))?ze(se):ze1(sce);
   r[14]=(ze(se)<ps1(sce))?ze(se):ps1(sce);

       /* D E F U Z Z Y I F I C A T I O N */


   w[1]=-1.50;w[2]=-3.5;w[4]=-7.0;w[5]=8.0;w[6]=4.0;w[7]=-3.5;
   w[8]=8.0;w[9]=4.0;w[10]=4;w[11]=2.5;w[12]=-
1.5;w[13]=0.08;w[14]=3.50;
   tmp1=0.0;tmp2=0.0;
     for(j=1;j<=14;j++)
     {
     tmp1+=r[j]*w[j];
     tmp2+=r[j];
     }
     suc=tmp1/tmp2;
     m[i-6]=1.6*suc*sp;
     if(m[i-6]>=10.0) m[i-6]=10.0;else if(m[i-6]<-10.0) m[i-6]=-
10.0;


      /*TRANSFER FUNCTION*/
     c[i]=0.990*c[i-1]+0.00896*(m[i-6]+1.11607*sp/t);


     fprintf(fp1,"%f           %f\n",c[i],m[i-6]);
     fprintf(fp2,"%f           %f\n",c[i],sp);
     printf("%f          %f\n",c[i],sp);

     }

     fcloseall();
     getch();
     }


      /*FUNCTION SUBROTINE */

    float pb(float x)
    {float y;
    if((4.50<x)&&(x<=6)) y=x-4.5;
    else if(x>=6.0) y=1.0;else y=0;
    return(y);
    }

    float pm(float x)
```

```
{ float y;
if((2.5<x)&&(x<=4.5)) y=(x-4.50)/2.0;
else if((4.5<x)&&(x<=6.0)) y=(6-x)/1.5; else y=0;
return(y);
}

float ps(float x)
{float y;
if((0.0<x)&&(x<=2.5)) y=(x-0.0)/2.5;
else if((2.5<x)&&(x<=4.50)) y=(4.5-x)/2.0; else y=0;
return(y);
}

float ze(float x)
{ float y;
if((0.0<x)&&(x<=2.0)) y=(2.0-x)/2.0;
else if((-2.0<x)&&(x<=0.0)) y=(2.0+x)/2.0; else y=0;
return(y);
}
float ze1(float x)
{ float y;
if((0.0<x)&&(x<=1.0)) y=(1.0-x)/1.0;
else if((-1.0<x)&&(x<=0.0)) y=(1.0+x)/1.0; else y=0;
return(y);
}
float ns(float x)
{ float y;
if((-2.5<x)&&(x<=0.0)) y=(x+0.0)/2.5;
else if((-4.0<x)&&(x<=-2.5)) y=(x+4)/1.5; else y=0;
return(y);
}
float nm(float x)
{
float y;
if((-4.5<x)&&(x<=-3.0)) y=(x+3.0)/1.5;
else if((-6.0<x)&&(x<=-4.5)) y=(x+6.0)/1.5; else y=0;
return(y);
}
float nb(float x)
{
float y;
if((-6.0<x)&&(x<=-5.0)) y=-(x+5.0);
else if(x<=-6.0) y=1.0; else y=0;
return(y);
}
float ps1(float x)
{
```

```
float y;
if((0.0<x)&&(x<=1)) y=x;
else if(x>=1.0)y=1.0; else y=0;
return(y);
}
```

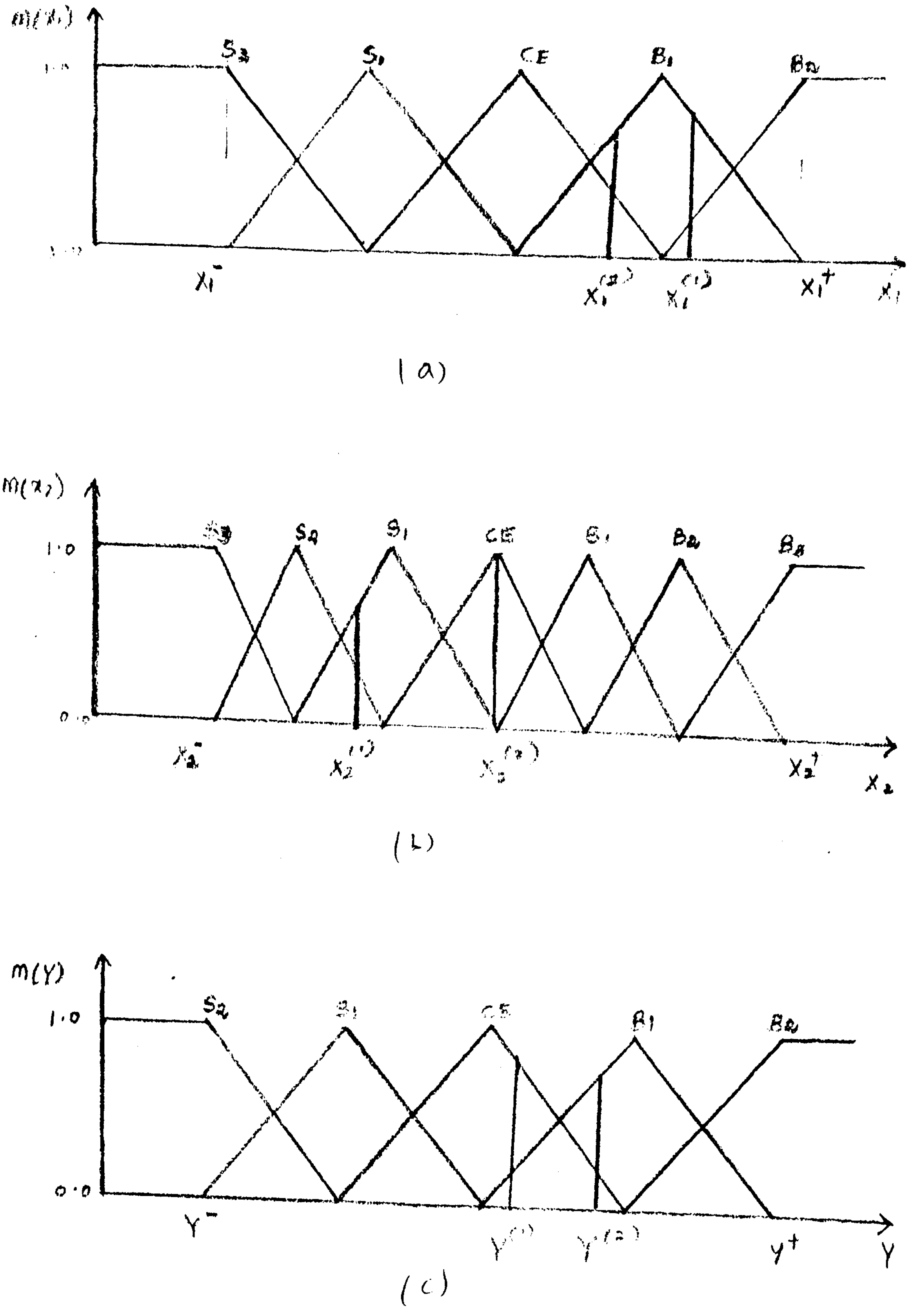


FIG. 5.1 FUZZIFICATION

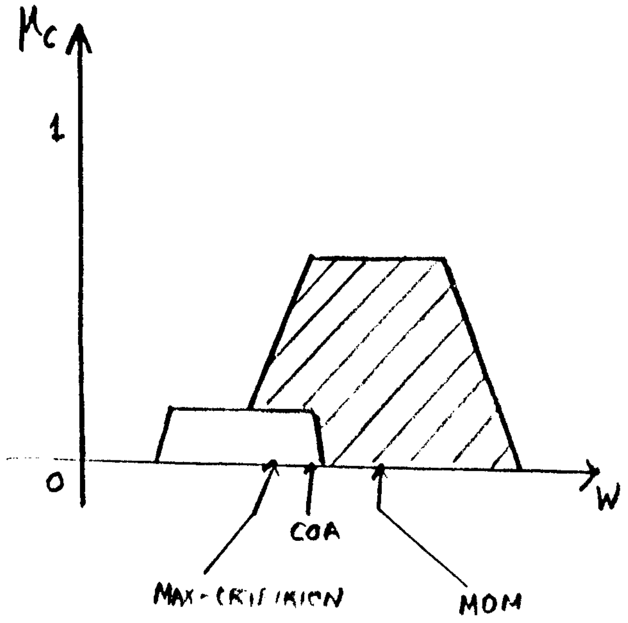


FIG. 5.2

DIAGRAMMATIC REPRESENTATION OF VARIOUS DEFFUZZIFICATION STARTERGIES

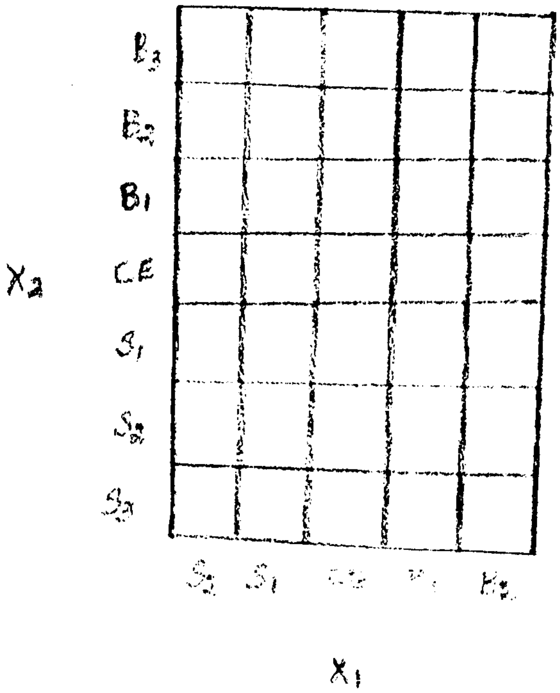


FIG. 5.3

FUZZY RULE BASE

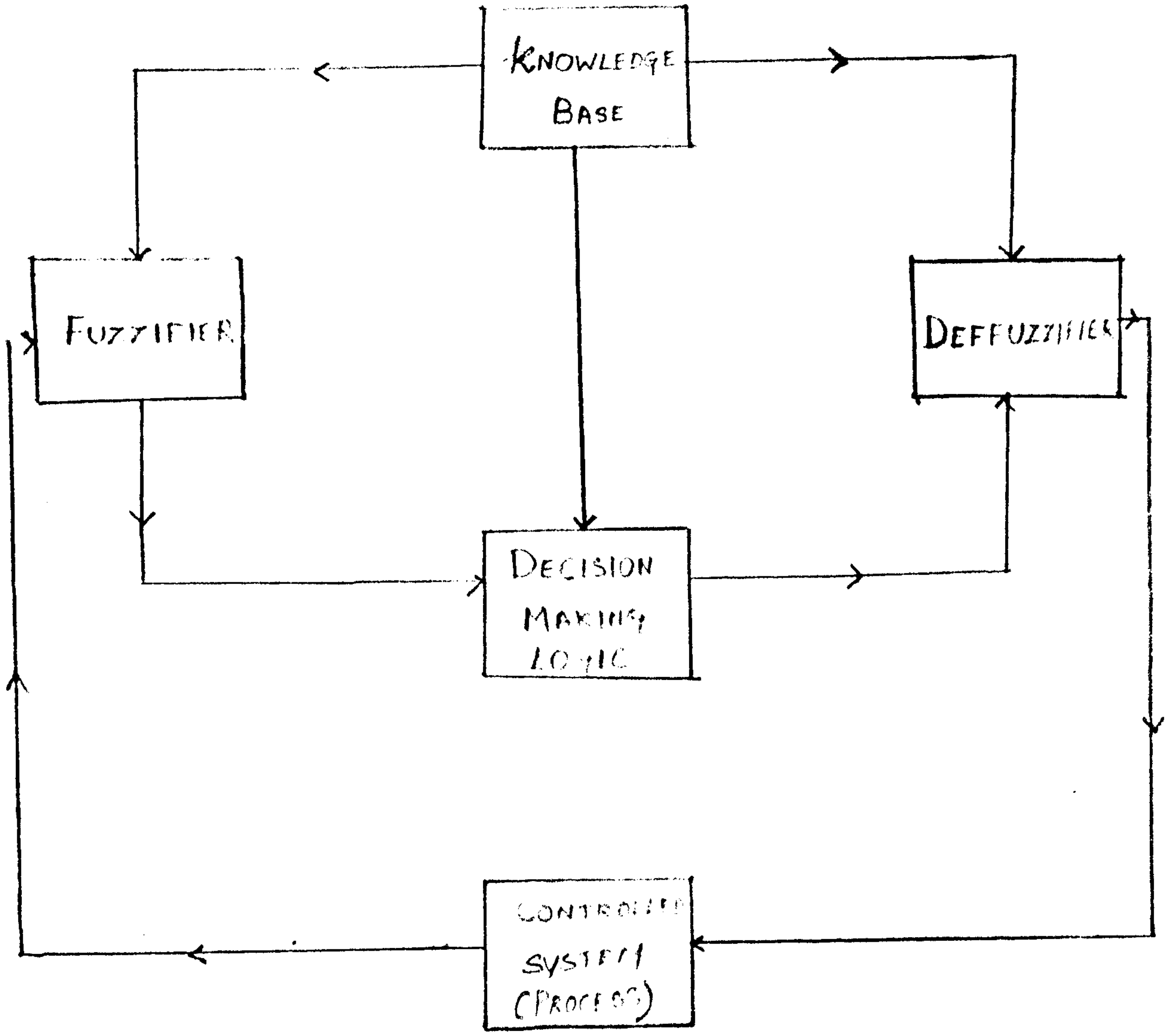


FIG. 5.4

BASIC CONFIGURATION OF FUZZY LOGIC CONTROLLER

CHAPTER VI

TEST REPORTS

This project consists of four modules and they are :

1) Speed sensing unit
2) Interfacing hardware
3) Fuzzy Logic Controller
4) DC drive unit

The test report of each module is presented in this chapter.

6.1 SPEED SENSING UNIT

We have designed and mounted a metal disc on the motor shaft, such that the proximity sensor will generates one pulse for one revolution. The number of pulses are counted for one second and multiplied with 60 so that we get number of revolutions per minute.

6.2 INTERFACING HARDWARE

It is nothing but Analog to Digital converter and Digital to Anolog converter. The digital output, for the analog input given to ADC and the Analog output, for the Digital input given to DAC are given in the Table 6.1 and Table 6.2 respectively.

TABLE 6.1 ADC OUTPUT

ANALOG I/P O/P	DIGITAL
0	689
1	85f
2	a87
3	b9c
4	d7a

TABLE 6.2 DAC OUTPUT

DIGITAL I/P O/P	ANALOG
fff	5.02
dbf	4.35
b91	3.70
303	1.07
14e	0.64

6.3 FUZZY LOGIC CONTROLLER

In the software program, the Anolog voltage value is scaled and the respective RPM is given in the Table 6.3

TABLE 6.3 EQUIVALENT RPM

DIGITAL VALUE	RPM
689	0
85f	398
a87	866
b9c	1011
d7a	1566
f0f	1850

6.4 DC DRIVE UNIT

The speed of the motor for different control signal voltage from the computer is tested and shown in Table 6.4

TABLE 6.4 SPEED CORESPONDING TO CONTROL SIGNAL

CONTROL SIGNAL VOLTAGE	SPEED IN RPM
0.45	0
0.50	150
0.60	450
0.75	900
0.90	1350
1.0	1650
1.05	1850

CHAPTER VII

CONCLUSION

A PC based fuzzy logic controller to control the speed of a DC motor has been designed. The speed of the motor is measured using a proximity sensor. ADC and DAC card has been fabricated and used for inputting the speed to the PC and outputting control signal to the DC drive, which is designed and constructed using Full wave Half controlled bridge rectifier. A software in C-language has been developed for Fuzzification, Rule base evoluation and Defuzzification. This system has been successfully tested on a DC motor.

This system finds application in process industries like paper mills and tyre manufacturing industries. This method gives more accurate speed control which ensures the quality of the product. Any modification in the operation of the system can be achieved by simple changes in the software.

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<u>**PRODUCT SPECIFICATION:**</u>

1) Octal transceiver

- Octal bi-directional bus interface.
- 3 - state buffer output
- PNP inputs for reduced loading
- Hystersis on all data inputs
- Type 74LS245
- Typical propagation delay: 8ns
- Typical supply current : 58mA

2) 8-bit Magnitude Comparator:

- Typical propagation delay 20ns
- Wide poser supply range 2-6V
- Low quiescent current, 80μA
- Large output current, 4mA
- Equality detector
- Comparison of words greater than 8 bits
- Drives 10 low power loads

3) Programmable Peripheral Interface:

- 24 programmable input pins
- completely TTL compatible
- Improved timing characteristics
- Fully compatible with Intel μP families
- Reduces system package card
- Improved DC driving capability
- 40 pin DIP package
- 3 modes of operation
- 3 8-bit ports

4) Flip - Flops:

- Typical f_{max} i.e., 40MHz
- Typical supply current i.e., 176mA
- Eight edge triggered D-flip-flops
- Buffered common clock
- Buffered asynchronous master reset
- Cermaic DIP packages
- Slim 20-pin plastic

5) Analog to Digital Converter:

- It is 12 bit converter
- Single +5V supply operation
- Low power 100mW max
- Package options - 0.6” and 0.3” DIPs, SOIC.
- Guaranteed AC and DC performance
- Fast acquisition and conversion - 25 μs max
- Replaces ADC574 for new designs
- Eliminates external sample/hold in most applications

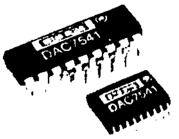
6) Chip Selector:

- Typical propagation delay 20ns
- Typical supply current 6.3mA
- Demultiplexing capabilities
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

7) Digital to Analog Converter:

- Four quadrant multiplication
- 12-bit end point linearity
- Differential linearity
- TTL/ CMOS compatible
- Single +5V to +15V supply
- Latch - up resistant
- Plastic DIP , plastic SOIC
- Low cost
- Monotoxicity guaranteed over temperature

BURR-BROWN®



DAC7541

www.burr-brown.com/databook/DAC7541.html

DAC7541 3 DIGITAL-TO-ANALOG CONVERTERS

Low Cost 12-Bit CMOS Four-Quadrant Multiplying DIGITAL-TO-ANALOG CONVERTER

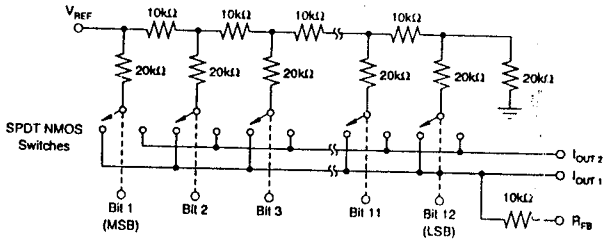
FEATURES

- FULL FOUR-QUADRANT MULTIPLICATION
- 12-BIT END-POINT LINEARITY
- DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- TTL-/CMOS COMPATIBLE
- SINGLE +5V TO +15V SUPPLY
- LATCH-UP RESISTANT
- 7521/7541/7541A REPLACEMENT
- PACKAGES: Plastic DIP, Plastic SOIC
- LOW COST

DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature range.

DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to a standard 18-pin plastic package, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.



Digital Inputs (DTL-/TTL-/CMOS-compatible)

Logic: A switch is closed to $I_{OUT\,1}$ for its digital input in a "HIGH" state.

Switches shown for digital inputs "HIGH".

ABSOLUTE MAXIMUM RATINGS[1]

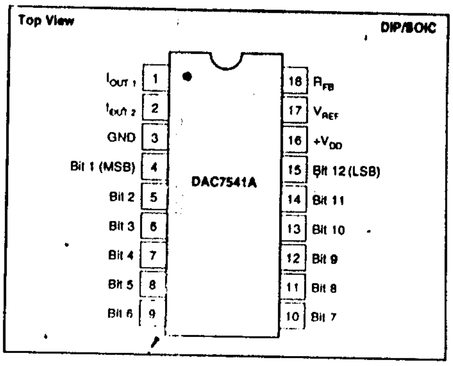
V_{DD} (Pin 16) to Ground	+17V
V_{REF} (Pin 17) to Ground	±25V
V_{RFB} (Pin 18) to Ground	±25V
Digital Input Voltage (pins 4-15) to Ground	–0.4V, V_{DD}
$V_{PIN\,1}$, $V_{PIN\,2}$ to Ground	–0.4V, V_{DD}
Power Dissipation (any Package):	
To +75°C	450mW
Derates above +75°C	–6mW/°C
Lead Temperature (soldering, 10s)	+300°C
Storage Temperature: Plastic Package	+125°C

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONNECTIONS



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7541JP	Plastic DIP	218
DAC7541KP	Plastic DIP	218
DAC7541JU	Plastic SOIC	219
DAC7541KU	Plastic SOIC	219
DAC7541JP-BI	Plastic DIP	218
DAC7541KP-BI	Plastic DIP	218

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

BURR-BROWN®

ADS574

www.burr-brown.com/databook/ADS574.html

Microprocessor-Compatible Sampling CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- REPLACES ADC574 FOR NEW DESIGNS
- COMPLETE SAMPLING A/D WITH REFERENCE, CLOCK AND MICROPROCESSOR INTERFACE
- FAST ACQUISITION AND CONVERSION: 25µs max
- ELIMINATES EXTERNAL SAMPLE/HOLD IN MOST APPLICATIONS
- GUARANTEED AC AND DC PERFORMANCE
- SINGLE +5V SUPPLY OPERATION
- LOW POWER: 100mW max
- PACKAGE OPTIONS: 0.6" and 0.3" DIPs, SOIC

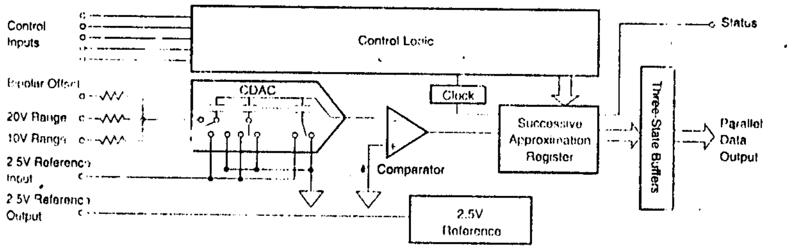
DESCRIPTION

The ADS574 is a 12-bit successive approximation analog-to-digital converter using an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This is a drop-in replacement for ADC574 models in most applications, with internal sampling, much lower power consumption, and capability to operate from a single +5V supply.

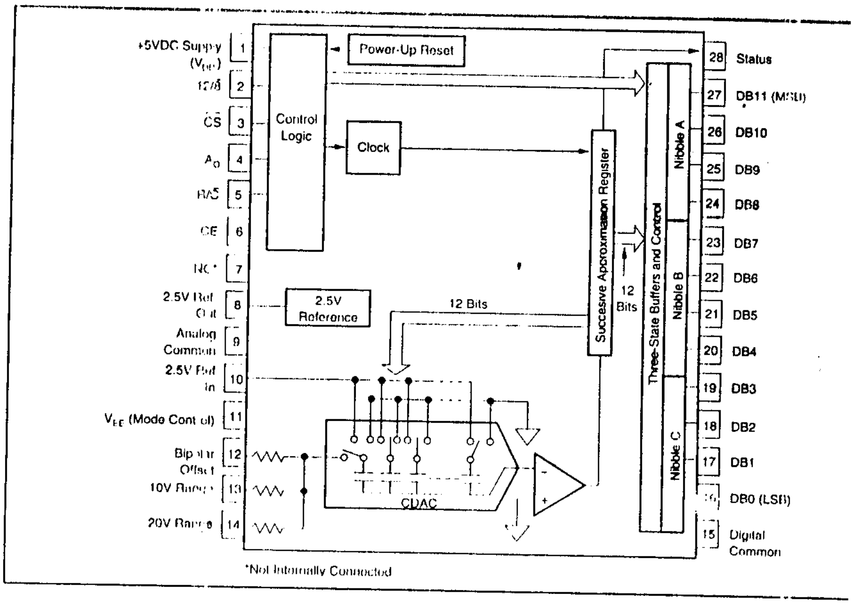
The ADS574 is complete with internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time for 12-bit conversions is 25µs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS574 requires +5V, with -12V or -15V optional, depending on usage. No +15V supply is required. Available packages include 0.3" or 0.6" wide 28-pin plastic DIPs and 28-lead SOICs.



CONNECTION DIAGRAM


+5VDC Supply (V_LOGIC) 1
12/8 2
CS 3
A0 4
R/C 5
CE 6
NC* 7
2.5V Ref Out 8
Analog Common 9
2.5V Ref In 10
V_EE (Mode Control) 11
Bipolar Offset 12
10V Range 13
20V Range 14
Power-Up Reset
Control Logic
Clock
2.5V Reference
12 Bits
CDAC
Successive Approximation Register
12 Bits
Three-State Buffers and Control
Nibble A
Nibble B
Nibble C
28 Status
27 DB11 (MSB)
26 DB10
25 DB9
24 DB8
23 DB7
22 DB6
21 DB5
20 DB4
19 DB3
18 DB2
17 DB1
16 DB0 (LSB)
15 Digital Common
*Not Internally Connected