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Design and Development of Hybrid Power Filter for Single Phase Power Converter

A Project Report

Submitted by

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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

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BONAFIDE CERTIFICATE

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Certificate

This is to certify that Mr/Mrs/Ms. D. Banumathi, KC1, Coimbatore has participated and presented a paper titled Design of Hybrid Power Filter For Single Phase Power Converter in Fourth National Conference on Electrical and Instrumentation Systems 2011, held on 17th March 2011 at Government College of Technology, Coimbatore.

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CONTENTS

ABSTRACT

The quality of the electrical current becomes a major concern. Power electronic equipments draw non-sinusoidal currents from the utility, causing interference with adjacent sensitive loads and limit the utilization of the available electrical supply. A single-phase hybrid power filter for harmonics and reactive power compensation for a diode rectifier load is presented in this thesis. A combination of passive and active filters is proposed for reducing the rating of active filter. In the proposed technique passive filter is tuned to compensate 3^{rd} and 5^{th} order harmonics and active power filter compensates all remaining harmonic components which are not compensated by passive filter. A half bridge inverter with DC bus capacitor is used as active filter. The active power filter control is based on DC side voltage control. With the use of hybrid filter in parallel to load the source current is exactly in phase with the source voltage and approximately in sinusoidal waveform after reactive power and harmonic compensation. The effectiveness of the proposed algorithm is demonstrated by its simulation in PSIM software. The proposed controller is implemented in hardware and tested. Micro controller PIC16F877A is used to generate the pulses for the switching devices in active filter.

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

DC	Direct Current
AC	Alternating Current
PWM	Pulse Width Modulation
APF	Active Power Filter
PF	Passive Filter
HPF	Hybrid Power Filter
THD	Total Harmonic Distortion
TDD	Total Demand Distortion
ASD	Adjustable Speed Drive
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electro technical Commission
VSI	Voltage Source Inverter
CSI	Current Source Inverter
C	Capacitor
L	Inductor
LV	Low Voltage
MV	Medium Voltage
HV	High Voltage
EHV	Extra High Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

IGBT	Insulated Gate Bipolar Transistor
PIC	Peripheral Interface Controller

LIST OF SYMBOLS

S1, S2	Power MOSFETs
i_L	Inductor Current
i_C	Capacitor Current
i_{Lf}	Fundamental Load Current
i_{Lh}	Harmonic Load Current
V_s	Supply Voltage
I_{load}	Load Current
I_{comp}	Compensation Current
I_{sc}	Short Circuit Current
V_{dc}	Voltage across dc side capacitor of Active Filter
h	Order of Harmonic

CHAPTER 1

CHAPTER 1

INTRODUCTION TO HYBRID POWER FILTER

1.1 INTRODUCTION

The widespread use of nonlinear loads is leading to a variety of undesirable phenomena in the operation of power systems. The harmonic components in current and voltage waveforms are the most important among these. Harmonic pollution in electricity distribution systems is becoming so serious nowadays that the quality of the public supply is barely acceptable. In spite of poor quality of power supply, industry is increasingly connecting nonlinear loads to the system. In some weak network areas, the voltage and current distortions are so large that, it is essential to use filters to avoid damage or malfunctioning in sensitive electric equipments. Further, low frequency harmonics (2nd ~ 13th harmonics) should be suppressed because they can excite resonance in the electric network and cause problems such as over voltage, protection failure, mechanical stress and additional heating. The requirements of power quality at the input of the ac mains, several standards have been developed and imposed on the consumers. The realization of these standards and guidelines such as IEEE-519-1992/ IEC 61000 has attracted the attention of both utility and consumer to share their responsibilities, to keep the harmonics contamination within acceptable limits. Therefore, the harmonic percents of the single phase systems should also obey the standards. Harmonics problem are usually resolved by the use of conventional passive and active filters. Passive filters introduce resonance in the power system and tend to be bulky. Though active filters can be used for wide range of compensation they are costly. To overcome the disadvantages of active and passive filter, a hybrid filter which combines the advantages of both active and passive filter, with simple control strategy has been proposed to suppress harmonic current.

1.2 OBJECTIVE OF THE PROJECT

To design a hybrid power filter with a simple control strategy for a single phase system with a diode rectifier load in order to achieve the following

1. To minimize harmonics in source current.
2. To improve supply power factor.
3. For reactive power compensation.

1.3 ORGANISATION OF THE THESIS

CHAPTER 1

It deals with the introduction and objectives of the project.

CHAPTER 2

It deals with power quality, sources and effects of harmonics, IEEE standard for harmonic limit and harmonic mitigation techniques.

CHAPTER 3

It deals with the types of filter and their advantages and disadvantages.

CHAPTER 4

It deals with the proposed hybrid filter topology, active filter compensation and passive filter design.

CHAPTER 5

It deals with the control method used for hybrid power filter and the algorithm for the control method.

CHAPTER 6

It deals with simulation of hybrid power filter and also provides the simulation results and discussion on the results.

CHAPTER 7

It deals with hardware description and schematic of the components and output waveforms.

CHAPTER 8

Gives the conclusion and recommendations for the future work.

CHAPTER 2

CHAPTER 2

POWER QUALITY PROBLEMS AND ITS COMPENSATION

2.1 INTRODUCTION

The ubiquitous applications of power electronic equipments resulted in power quality problems, such as voltage distortion due to harmonics generated in supply currents of various order energy efficient electronic equipments and non linear loads on voltage and current waveforms. The power quality is of increasing concern of electric utilities, since the ill effects of harmonics causes the deterioration of various sensitive electronic and electric equipment designed to operate on pure sinusoidal waveform of a.c. supply at rated voltage and frequency. Harmonic distortion and subsequent equipment damage is one of the most serious power quality problems now a days.

Harmonic Voltages and Currents are the integral multiples of the fundamental frequency. In India, for 50Hz frequency of second harmonic is 100Hz, third harmonic is 150Hz. and so on. Though the applied voltage is sinusoidal because of the nonlinear characteristics of the load, the current drawn by them is non sinusoidal. This non sinusoidal current after passing through the low impedance of power system causes distortion in sinusoidal voltage which can be split up as sinusoids of different frequencies, which when added together results in original distorted waves. Advancements in power electronics caused the use of such equipment in power system at LV,MV,HV and EHV levels increasing at a faster rate, harmonics is negative by product of this development. Utility of nonlinear loads resulted in large harmonics in supply currents causing distortion of the voltage waveform resulting in deterioration of power quality. Deviation from sinusoidal shape is generally expressed in terms of harmonic components. All the harmonic current deteriorates the performance and impose various problems.

2.2 SOURCES OF HARMONICS

The different sources of harmonics namely from three main areas as listed below.

- From the fast switching associated with power electronic devices
- From the conventional sources such as electrical rotating machines and

- From modern electronic equipments

The different sources of harmonics in power distribution system is shown in fig 2.1.

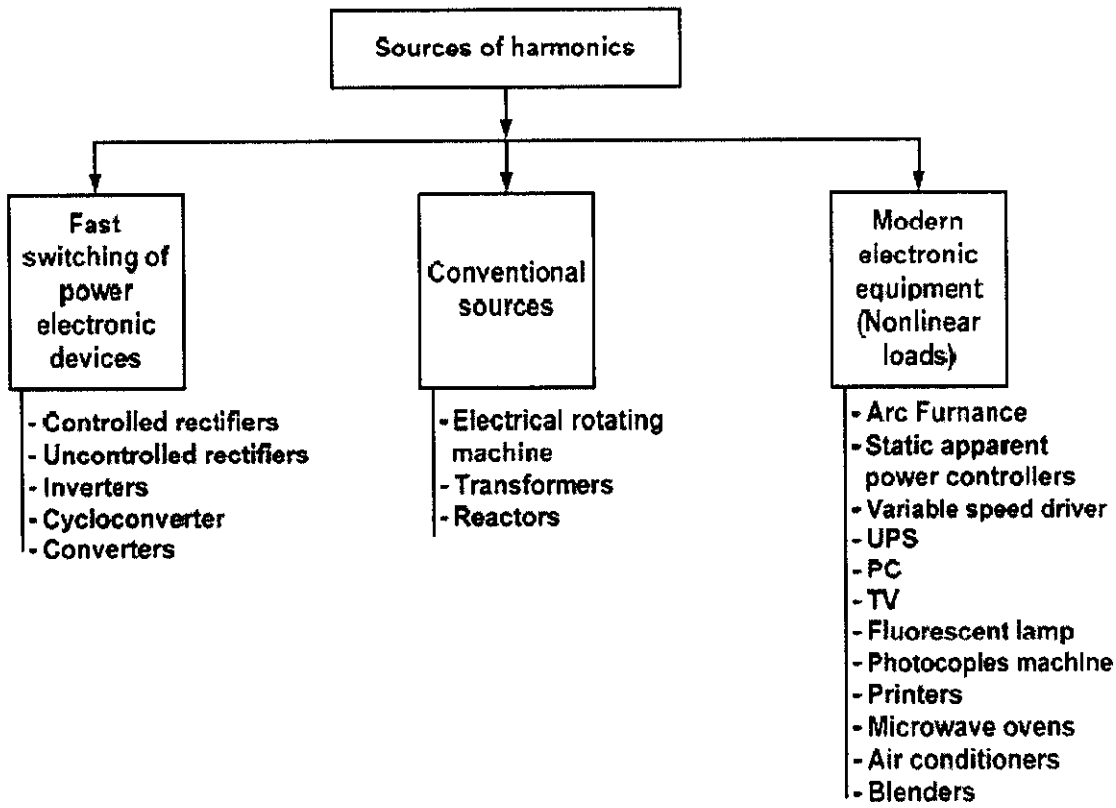

Fig 2.1 The sources of harmonics in power distribution system

2.3 EFFECTS OF HARMONICS:

Most power systems can accommodate a certain level of harmonic currents but will experience problems when harmonics become a significant component of the overall load. As these higher frequency harmonic currents flow through the power system, they can cause communication errors, overheating and hardware damage, such as:

- Overheating of electrical distribution equipment, cables, transformers, standby generators, etc.
- High voltages and circulating currents caused by harmonic resonance
- Equipment malfunctions due to excessive voltage distortion

- Increased internal energy losses in connected equipment, causing component failure and shortened life span
- False tripping of branch circuit breakers
- Metering errors
- Fires in wiring and distribution systems
- Generator failures
- Crest factors and related problems
- Lower system power factor, resulting in penalties on monthly utility bills
- Deterioration or failure of power factor correction capacitors.

2.4 IEEE STANDARD FOR HARMONIC LIMITS

IEEE Standard 519-1992 suggests limits on the harmonic currents that a user can induce back into the utility power system and also specifies the voltage quality that the utility should furnish the user. IEEE Standard 519-1992 recommended harmonic current limits, shown in Table 2.1, is expressed in terms of current TDD, rather than current THD.

Table 2.1 North American IEEE 519 (1992) Recommendations (120V – 69kV)

Maximum Harmonic Current Distortion in percent of I_L						
Individual Harmonic Order(Odd Harmonic)						
I_{sc}/I_L	< 11	11≤ h <17	23≤ h <35	<35	35≤h	TDD
<20	4%	2%	1.5%	0.6%	0.3%	5%
20<50	7%	3.5%	2.5%	1%	0.5%	8%
50<100	10%	4.5%	4%	1.5%	0.7%	12%
100<1000	12%	5.5%	5%	2%	1%	15%
>1000	15%	7%	6%	2.5%	1.4%	20%

I_{SC} = Short circuit current at point of common coupling (PCC). The PCC can be considered as the connection point between linear and non-linear (harmonic producing) loads.
I_L = Maximum demand load current (fundamental) at PCC.
TDD = 'Total demand distortion' of current (expressed as measured total harmonic current distortion, per unit of load current. For example, a 30% total current distortion measured against a 50% load would result in a TDD of 15%).

The IEEE Standard 519-1992 recommended harmonic voltage limits, shown in Table 2.2, are given for the maximum harmonic components and for the voltage THD.

Table 2.2 Voltage Distortion Limits

Bus Voltage at PCC	Maximum Individual Harmonic Component %	Maximum THD%
69kV and Below	3.0	5.0
69.001kV through 161kV	1.5	2.5
161.001kV and above	1.0	1.5

2.5 HARMONIC MITIGATION TECHNIQUES:

Various harmonic reduction techniques have been developed to meet the requirements imposed by the current harmonic standards. In general these techniques can be classified into three broad categories:

1. Phase multiplication systems (12-pulse, 18-pulse rectifier systems)
2. PWM rectifiers
3. Filters

2.5.1 PHASE MULTIPLICATION SYSTEM

Harmonic can be reduced by phase multiplication. Phase multiplication technique is based on increasing the pulse number for the converter. If m six-pulse rectifier sections;

- Have the same transformer ratios.
- Have transformers with identical impedances.
- Are phase shifted exactly 60/m degrees from each other.
- Are control at exactly the same delay angle, and
- Share the dc load current equally.

Then the only harmonics present will be of the following order;

$$h = kq \pm 1 \qquad (2.1)$$

where

h is the harmonic order

q is now 6m

m is the number of six-pulse rectifiers

2.5.2 PWM RECTIFIERS

For PWM- Voltage Source Rectifiers (PWM-VSR) benefits like power regeneration, low harmonic distortion, unity power factor, and controlled DC link can be obtained. They are often used in applications where substantial regenerative operating mode occurs. PWMVSR operation principle is based on direct sinusoidal current generation with minimum harmonic content.

2.5.3 FILTERS:

Filters are used to eliminate components of current and voltage whose frequencies are integral multiples of power system frequencies. Used to minimize distortion in waveforms caused by harmonics injected by non linear loads.

CHAPTER 3

CHAPTER 3
TYPES OF FILTER

3.1 PASSIVE FILTER

These are widely used to control harmonics, especially the 3^{rd} , 5^{th} and 7^{th} harmonics. Passive harmonic filters are made of inductive, capacitive and resistive elements. In passive filters, the flow of the undesired harmonic currents into the power system can be prevented by the usage of a high series impedance to block them or by diverting them to a low impedance shunt path.

3.1.1 SERIES PASSIVE FILTER

When passive filters are connected in series with the power line, they are designed to have a large impedance at a certain harmonic. This will isolate the harmonics produced by the loads from reaching the supply system. Series passive filters can be purely inductive type or LC tuned type. AC line reactor filter and DC link inductor filter are the two purely inductive type filters. The tuned series passive filter is connected in series with the load. The filter consists of parallel inductance and capacitance that are tuned to provide high impedance at a selected harmonic frequency. The high impedance then blocks the flow of harmonic current at the tuned frequency only. At fundamental frequency, the filter is designed to yield low impedance, thereby allowing the fundamental current to flow. For blocking multiple harmonics, multiple series filters are needed. They must be designed to carry a full rated load current as they are connected in series to full line voltage. Therefore, they can create significant losses at the fundamental frequency.

3.1.2 SHUNT PASSIVE FILTER

When passive filters are connected in parallel with the power line, they provide a low impedance path for selected harmonic currents to pass to ground, thus preventing them from entering the supply system. In contrast to series passive filters, shunt passive filters carry only a fraction of the current that a series filter must carry. Given the higher cost of a series filter, and the fact that shunt filters may supply reactive power at the fundamental frequency, the most practical approach usually is the use of shunt filters. A shunt filter offers very low impedance path at the frequency to which it is tuned and it shunts most of the harmonic current at that frequency. Most Common shunt filter types are the single tuned and high-pass filters. These two filters are the relatively simple to design and implement among the other

shunt types. The layout of common shunt filter types is shown in Fig 3.1.The most common design of shunt filter is a single-tuned filter.

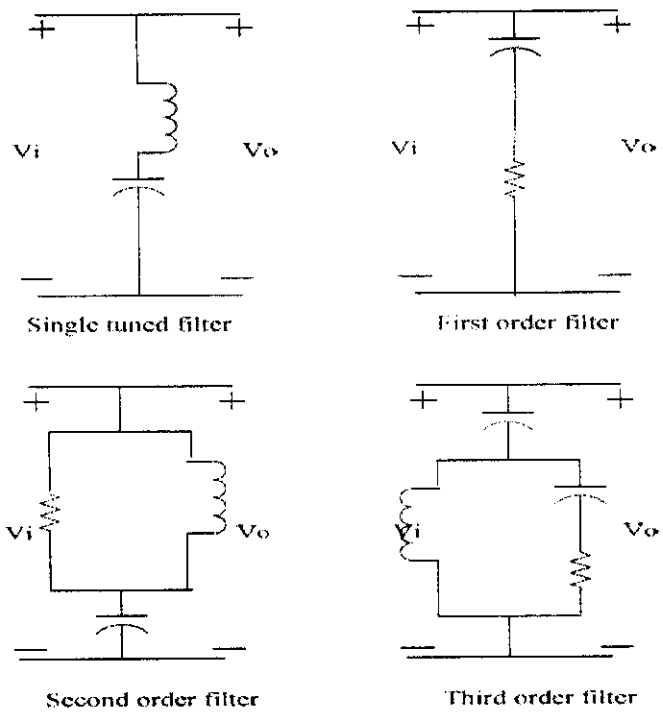

Fig 3.1 Types of shunt passive filter

3.1.3 ADVANTAGES AND DISADVANTAGES OF PASSIVE FILTER

ADVANTAGES

- Simple in construction, less costly and efficient
- Serves dual purpose harmonic filtration and power factor correction of load.

DISADVANTAGES

- Cannot function under saturated condition.
- Number of passive filters installed must be equal to the number of harmonic levels to be compensated.
- Connection of passive filters necessities a specific analysis of each installation.
- Non adaptability to system variations.
- Bulky in size.
- Tendency to resonate with the other load.

3.2 ACTIVE POWER FILTER

Active harmonic compensation (filtering) method is relatively a new method for eliminating current harmonics from the line. Active filters give good system performance and

current harmonics reduction. In active filters the basic idea is to inject to the line equal magnitudes of the current/voltage harmonics generated by the nonlinear load and with 180 degrees phase angle difference so they cancel each other.

Active filters can be classified based on converter type, topology, and number of phases. The converter type can be either Current Source Inverters (CSI) or VSI. CSI based active filters employ an inductor as the energy storage device. VSI-based active filters used a capacitor as the energy storage device. The topology can be shunt or series. The third classification is based on the number of phases, such as two-wire (single-phase) and three- or four-wire (three phase) systems. Three phase active filters are used for high power nonlinear loads such as ASD and AC/DC converters.

3.2.1 SERIES ACTIVE FILTER

These are connected in series with network and non-linear load. It introduces a suitable voltage through a matching transformer, voltage introduce by series filter is in such a way that the supply sees a very high impedance for harmonic and low impedance for fundamental. The series active power filter is shown in fig 3.2.

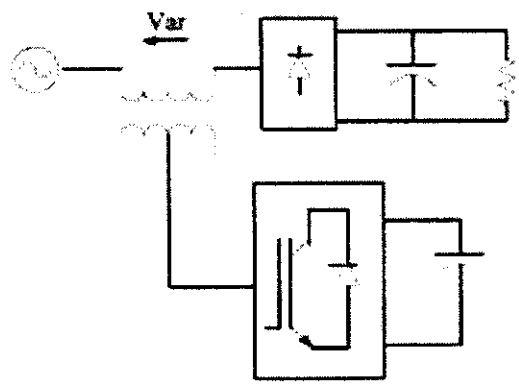

Fig 3.2 Series active filter

3.2.2 SHUNT ACTIVE FILTER

These devices are designed to constantly monitor the harmonics in the load current and same harmonic equal in magnitude and opposite in phase are thus injected to cancel the original harmonics. These are connected in parallel with harmonic generating non-linear load.

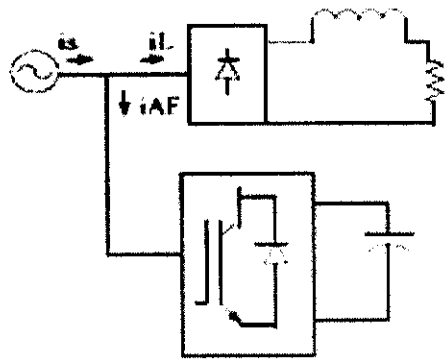

Figure 3.3 Shunt Active Filter

Of all various configurations of active filter, the parallel active filter using the voltage source inverter topology accompanied by high performance current regulation methods is the most frequently employed type. The shunt active filter is shown in fig 3.3.

3.2.3 ADVANTAGES AND DISADVANTAGES OF ACTIVE FILTER:

ADVANTAGES

- Used for wide range of compensation

DISADVANTAGES

- However, they are based on sophisticated power electronics components and thus they are much more expensive than passive filters.

3.3 HYBRID POWER FILTER

Hybrid filters, combine active and passive filters in various configurations. The main purpose of hybrid active filters is to reduce initial costs and to improve efficiency. They are also used to improve the compensation characteristics of passive filters and alleviate any series or parallel resonance due to supply or load respectively Practically, more viable and cost effective hybrid filter topologies have been developed than stand-alone active filters. They enable the use of significantly small rating active filters that is less than 5% of the load KVA compared to stand-alone parallel (25-30%) or series active filter solutions. Usually, with shunt passive filter combinations, the passive filter is tuned up to a specific frequency to suppress the corresponding harmonic and decrease the power rating of the active filter. Another typical combination is of a series active filter and a series passive filter. The common configurations of hybrid filter are shown in fig 3.4.

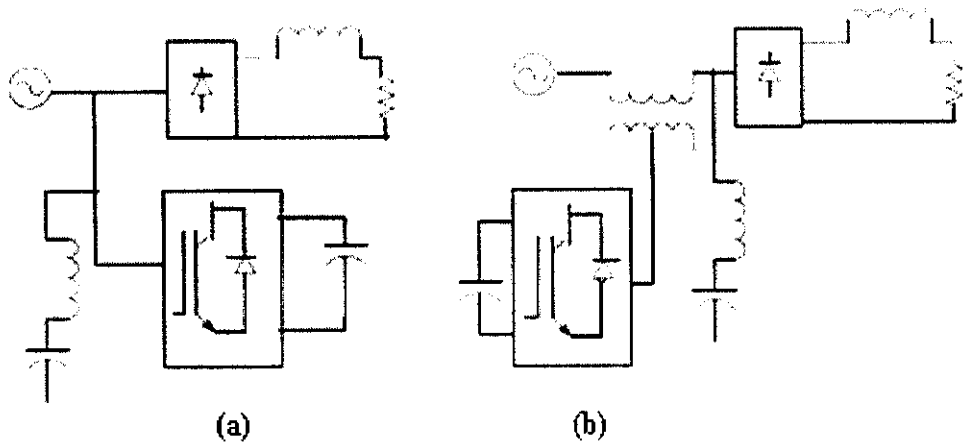

Fig.3.4 Hybrid filters common configurations;
(a) Shunt active filter and shunt passive filter,
(b) Series active filter and shunt passive filter

CHAPTER 4

CHAPTER 4

PROPOSED HYBRID POWER FILTER TOPOLOGY

4.1 SYSTEM CONFIGURATION

A schematic diagram of a single-phase HPF which consists of an active power filter in parallel with two single tuned passive filters is shown in Fig.4.1. A single-phase voltage source supplying power to nonlinear load which is connected in parallel with a current controlled APF and two single-tuned passive filter. A single-phase full bridge uncontrolled rectifier with R-L load on its dc-side is used as a nonlinear load. The APF consists of an inductor and a half bridge single phase current controlled voltage source inverter (CC-VSI) with a self-charging capacitor. Random PWM technique is used to obtain the PWM pulses to control the switches used in CC-VSI circuit. The single-tuned passive filters consist of fixed value inductors and capacitors are tuned to compensate 3rd and 5th order harmonics.

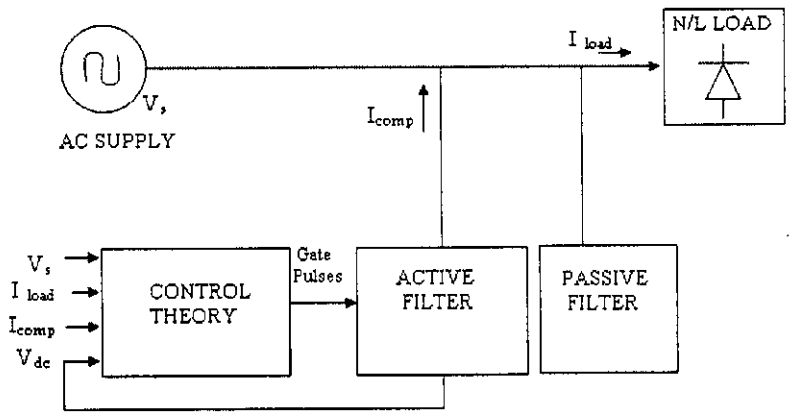

Fig 4.1 Block Diagram of Single Phase Hybrid Power Filter

4.2 ACTIVE POWER FILTER COMPENSATION

Generally, an active power filter generates a harmonic spectrum that is opposite in phase to the distorted harmonic current it measures. Harmonics are thus cancelled and the result is a non-distorted sinusoidal current. The single leg topology of active power filter across voltage source and rectifier load is shown in Fig. 4.2. To avoid flowing of the fundamental current of the voltage source to the active power filter, a passive shunt LC filter is used.

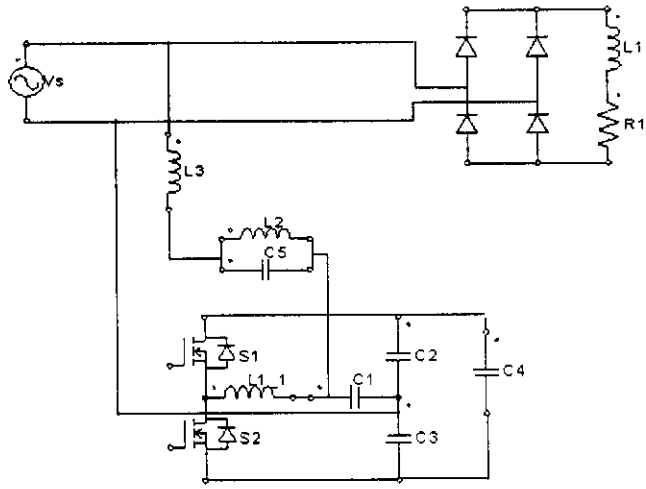

Fig 4.2 One leg active power filter across voltage source and load

4.3 MODES OF OPERATION:

4.3.1 MODE 1

In this mode switch S1 is on and S2 is off. In this case capacitor C4 is discharging. The single phase equivalent circuit of the system when the S1 is on and the S2 is off is shown in Fig. 4.3. From Fig. 4.3, we have the following equations:

$$i_{C4} = i_{C2} + i_{L1} \quad (4.1)$$

$$i_{L1} = i_{C1} + i_{L3} \quad (4.2)$$

$$i_L = i_S + i_{L3} \quad (4.3)$$

$$i_L = i_{Lf} + i_{Lh} \quad (4.4)$$

If $i_{L3} = i_{Lh}$, thus from equations (4.3),(4.4) we have

$$i_S = i_{Lf} \quad (4.5)$$

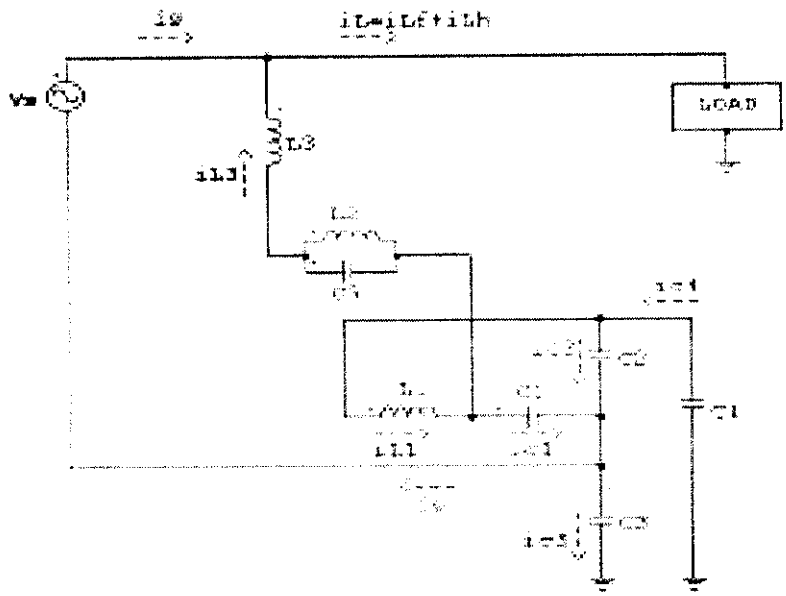

Fig 4.3 Equivalent circuit of the system in Fig.4.2 in the case of S1=on and S2=off.

4.3.2 MODE 2

In this mode switch S1 is off and S2 is on. In this case capacitor C4 is charging. The single phase equivalent circuit of the system when the S1 is off and the S2 is on is shown in Fig. 4.4.

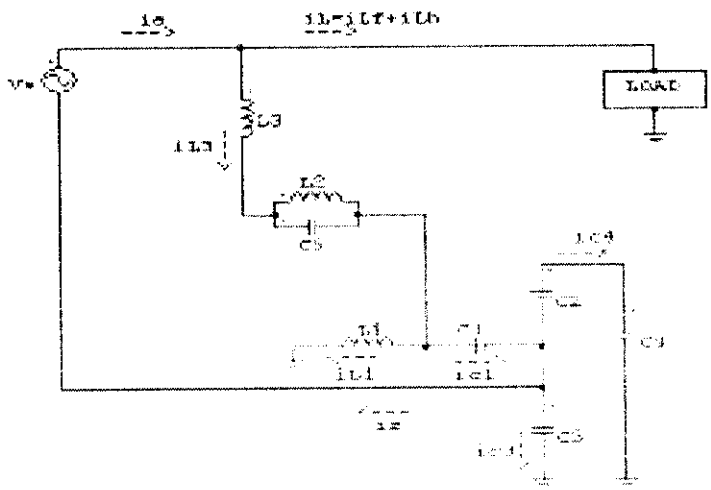

Fig 4.4 Equivalent circuit of the system in Fig. 4.2 in the case of S1=off and S2=on.

From Fig. 4.4, we have the following equations:

$$i_S = i_{L3} + i_L \qquad (4.6)$$

Thus if $i_{L3} = -i_{Lh}$, we have:

$$i_s = i_{Lf} \qquad (4.7)$$

Thus in both cases harmonics are cancelled by APF making the source current sinusoidal.

4.4 PASSIVE FILTER DESIGN

Two single tuned passive filter is used to eliminate the 3rd order and 5th order harmonics. The selection of inductance and capacitance has many criteria that should be considered simultaneously. The PF should have an impendence as low as possible at the major harmonics, such as the 3rd and 5th to achieve good filtering characteristics and low power rating of APF. So the capacitance value C_F should be as large as possible whereas the inductance value of L_F should be as small as possible. However, a large capacitance value of C_F will introduce a large amount of capacitive reactive current flowing into the LC filter. Moreover, a low inductance value of L_F would make the LC filter have no capability to suppress the switching ripples caused by the APF. On the other hand, in order to obtain good dynamic characteristics the value of the inductance should be as small as possible. The design result should be a compromise among all the above-mentioned criteria.

To suppress 3rd and 5th order harmonic the L and C are tuned at 150Hz and 250Hz. For this PF is tuned at hth harmonic that is:

$$h\omega_1 L_F = \frac{1}{h\omega_1 C_F} \qquad (4.8)$$

CHAPTER 5

CHAPTER 5

CONTROL STRATEGY OF HYBRID POWER FILTER

5.1 CONTROL BY DC SIDE VOLTAGE

The active power filter is controlled by means of DC side voltage control algorithm. This theory is based on the voltage value at the capacitors in the DC side of the power inverter. The control system maintains the average voltage across the capacitor constant against variations in line and filtering load on the APF. Inverter is gated in such a way that the filter compensation current follows a reference current waveform set by the concerned control system. The voltage required at the terminals of inverter output will be automatically made suitable for maintaining the required compensation current i.e. the inverter is controlled in the 'current regulated' mode. The current delivered by the source is desired to be a pure sinusoidal wave even when the load draws a highly distorted current wave. This is accomplished by making the compensation current equal to the harmonic current required by the load. Under a loss free situation, the inverter does not need to draw any active power. However, there will be losses in the resistances of inductor, switches, etc. and switching losses when the inverter is generating current. Unless these losses are compensated, the capacitor voltage will come down steadily. Hence the control of capacitor voltage involves drawing an in phase sinusoidal component of current from the source along with the required harmonic currents. Fig. 4 shows a block diagram that represents the algorithm used to control an Active Power Filter based on the regulation of the DC side voltage.

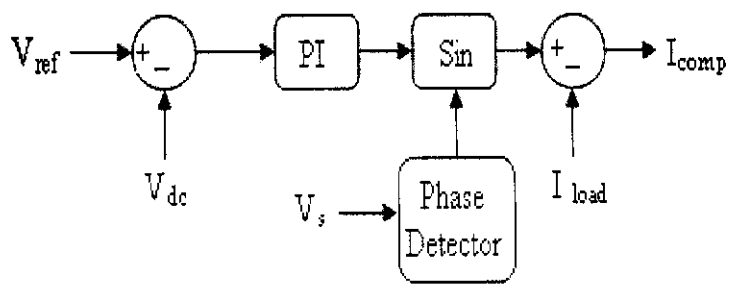

Fig 5.1 Block Diagram for DC side control algorithm

According to the DC side voltage, the control, estimates the ideal source current. This calculation uses a proportional integral controller (PI).The adjustment of the PI parameters is crucial on this theory, since the behavior of the Active Power Filter is hardly dependent of this controller. So the PI response must be fast, enabling the Active Power Filter to quickly respond to load changes, and also must be stable. Oscillations on the response of the PI controller will cause variations in the current amplitude. The value obtained by the PI controller is used to generate a sinusoidal signal that is equivalent to the ideal current at source, necessary to supply the load. To compensate the power factor, the generated sinusoid must be synchronized with the system voltage. This synchronization can be done through a PLL algorithm. After, the load current waveform will be subtracted to the obtained sinusoid to get the compensation current.

This reference compensation current is compared with the actual compensation current produced by the filter and according to that gate pulses are given to the switches of APF in order to get pure sinusoidal source current. The pulses are generated by means of PIC micro controller.

5.2 ALGORITHM FOR THE CONTROL METHOD

1. Set the reference voltage for the DC side capacitor voltage of the active filter.
2. Compare the actual voltage across the DC side capacitor with the reference voltage.
3. The error signal is given to the PI controller.
4. Generate a sinusoidal waveform according to the value obtained from the PI controller. This waveform should be equivalent to the ideal source waveform.
5. Make that sinusoidal waveform to be in phase with the supply voltage in order to compensate power factor.
6. Compare that current with load current in order to obtain the compensation current required to cancel the harmonic.

7. Compare the obtained compensation current with actual compensation current injected by the filter.

8. According to that error generate pulses to the switches of active filter in order to make the source current sinusoidal by cancelling harmonics.

CHAPTER 6

CHAPTER 6

SIMULATION OF HYBRID POWER FILTER

6.1 PSIM SOFTWARE

PSIM is a simulation software specifically designed for power electronics and motor control. With fast simulation and friendly user interface, PSIM provides a powerful simulation environment to address your simulation needs. The PSIM package consists of three parts: PSIM schematic program, PSIM Simulator, and waveform display program Simview. PSIM provides an intuitive and easy-to-use graphic user interface for schematic editing. A circuit can be easily created and edited. Extensive on-line help is available for each component. To handle large systems, PSIM provides the subcircuit function which allows part of a circuit to be represented by a subcircuit block.

PSIM simulator is the engine of the simulation environment. It uses efficient algorithms to overcome the convergence problem and long simulation time existing in many other simulation software. The fast simulation allows repetitive simulation runs and significantly shortens the design cycle. Simulation results are displayed and evaluated in Simview. Various waveform processing functions, such as multiple screens and line styles, are provided. Post-processing functions such as addition/subtraction and average/rms value calculation are also provided.

With its unique features in simulation speed, capability of handling power converter circuits of any size, and simulation of control circuits, PSIM is ideal for circuit-level and system-level simulation, control loop design, motor drive systems, and other dynamic system simulation.

6.2 KEY FEATURES OF PSIM

- **Easy to use**: PSIM is so easy to use that one hardly needs the User Manual to use the software. Even without prior experience with CAD software, one could start building a circuit and obtaining results in minutes.

- **Fast Simulation**: PSIM is one of the fastest simulators for power electronics simulation. It achieves fast simulation while retaining excellent simulation accuracy. This makes it particularly efficient in simulating converter systems of any size, and performing multiple-cycle simulation.
- **Flexible Control Representation**: PSIM can simulate control circuit in various forms: in analog circuit, s-domain transfer function block diagram, z-domain transfer function block diagram, custom C code, or in Matlab/Simulink. PSIM's control library provides a comprehensive list of components and function blocks, and makes it possible to build virtually any control schemes quickly and conveniently.
- **Frequency Response Analysis (ac sweep)**: While almost all the simulation software require that a switchmode circuit be represented by an average model first before performing ac analysis, PSIM can perform ac analysis even if the circuit is in switchmode. This feature greatly reduces the time required to obtain frequency response.
- **Co-simulation with Matlab/Simulink**: PSIM can perform co-simulation with Matlab/Simulink. This feature allows users to make full use of PSIM and Matlab/Simulink in a complementary way.
- **Comprehensive Motor Drive Library**: PSIM provides a comprehensive library for motor drive system studies. Commonly used electric machine models and mechanical load models are available. With the Motor Drive Module, PSIM provides an easy and effective way of modeling and simulating motor drive systems.
- **Digital Control System Simulation**: PSIM can simulate control systems in z-domain. It can be used to simulate the performance of digital control loops, study digital filters, and evaluate various effects in digital control, such as truncation errors, sampling/hold delay, and computational delay.
- **Dynamic Link to Finite Element Analysis Software**: PSIM can link to the finite element analysis software JMAG through the MagCoupler Module. JMAG is a finite element analysis software for electromagnetic field analysis. With this link, the power converter and control part of a system can be implemented and simulated in PSIM, and electric machines and other magnetic devices can be implemented and simulated in JMAG.
- **Custom C/C++ Code**: PSIM supports DLL (dynamic link library) blocks which

flexibility and capability. One can, for example, use PSIM to represent the power stage, write the control scheme in C, and interact control with the power stage via DLL. This allows one to test the performance of a control scheme for microprocessors/DSP implementation with the minimum effort.

- **Built-in Power and Control Blocks**: To facilitate the circuit setup, commonly used blocks such as three-phase converter bridges, transformers, abc-dqo transformation blocks, filters, etc. are provided in PSIM. This not only speeds up the circuit creation/editing, but also simplifies the control circuitry.

6.3 SIMULATION USING PSIM SOFTWARE

The simulation of hybrid power filter with a shut active and passive filter is done using the PSIM software. The supply voltage amplitude is considered to be 110 V with the frequency of 50 Hz. The source impedance is a series R-L impedance with the values of R = 2Ω and L = 20μH. The value of reference voltage is chosen as 50V.The values of series L and C in the power converter are selected 100 μH and 3.3 mF respectively. The values of the shunt L, C are chosen 1mH, 4.3mF and the value of series L is selected 1mH. The value of dc capacitor is chosen 4.7 mF and the values of split capacitors are selected as 560μF. The load connected to the dc side of diode rectifier is series R-L with the values of R = 2 Ω, L =10mH The passive filter values for 3^{rd} order harmonic are L=11.26 mH, C=100 μF and for 5^{th} order harmonics L=8.11 mH, C=50 μF. The simulation diagram of the hybrid power filter, is shown in Fig. 6.1.

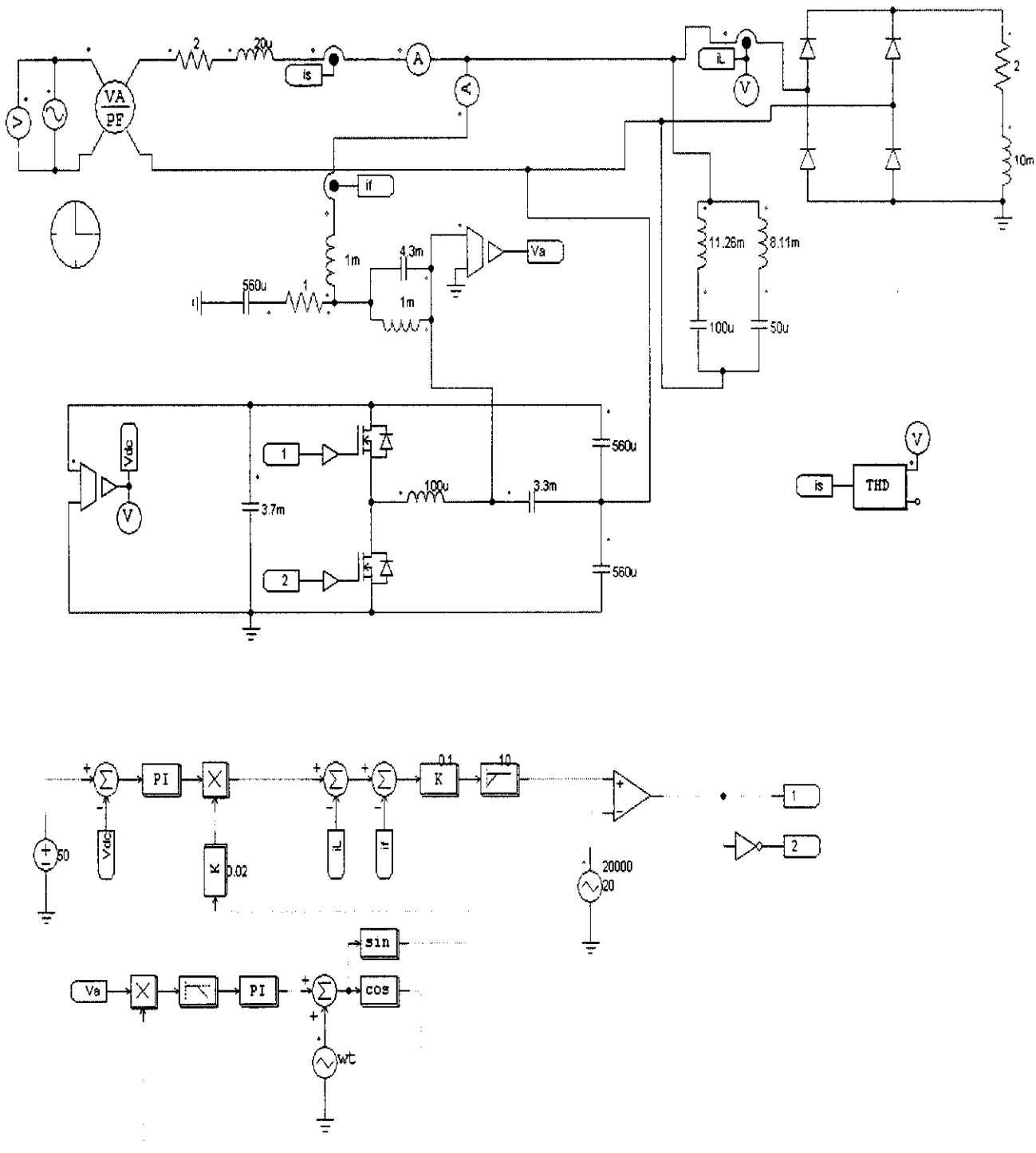

Fig 6.1 Simulation diagram of hybrid power filter

6.4 SIMULATION RESULTS

6.4.1 WITHOUT FILTER

The source current and the THD of the system when filter is not connected to it is shown in Fig 6.2. The source current drawn by the nonlinear load is distorted due to the presence of harmonics. The THD of source current is 26.8%.

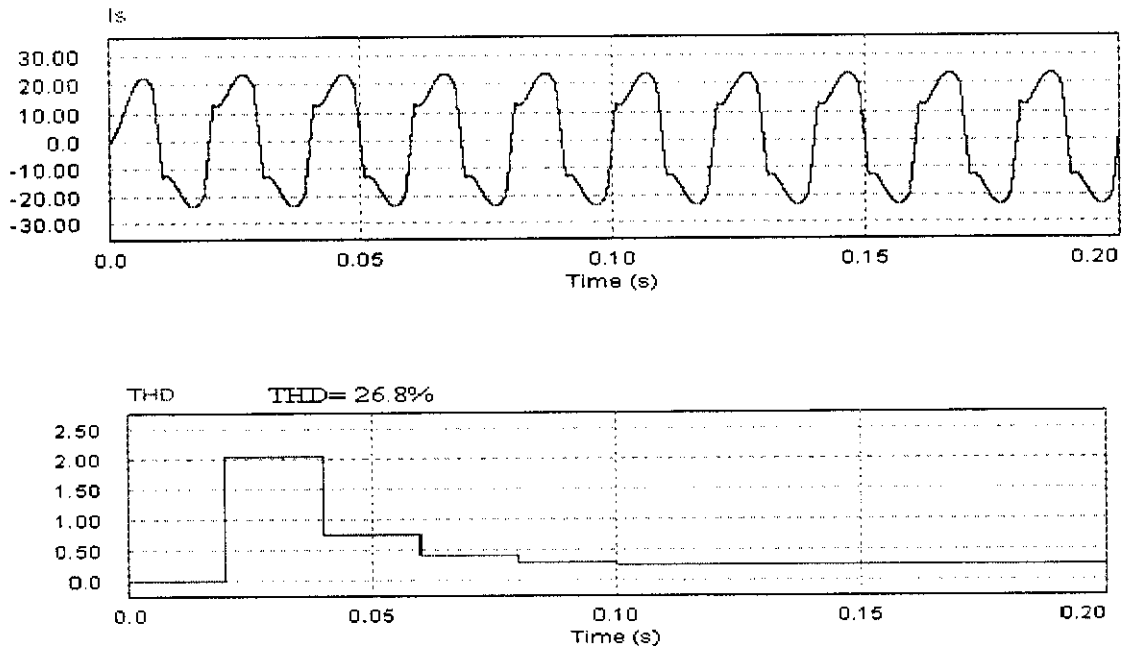

Fig 6.2 Source current, THD of the system without Filter

6.4.2 WITH PASSIVE FILTER ALONE

The source current and the THD of the system when passive filter alone is connected to it is shown in Fig 6.3. The distortions in source current are minimized due to the elimination of 3^{rd} and 5^{th} harmonic components by the passive filter. The THD of source current is reduced to 12.4%.

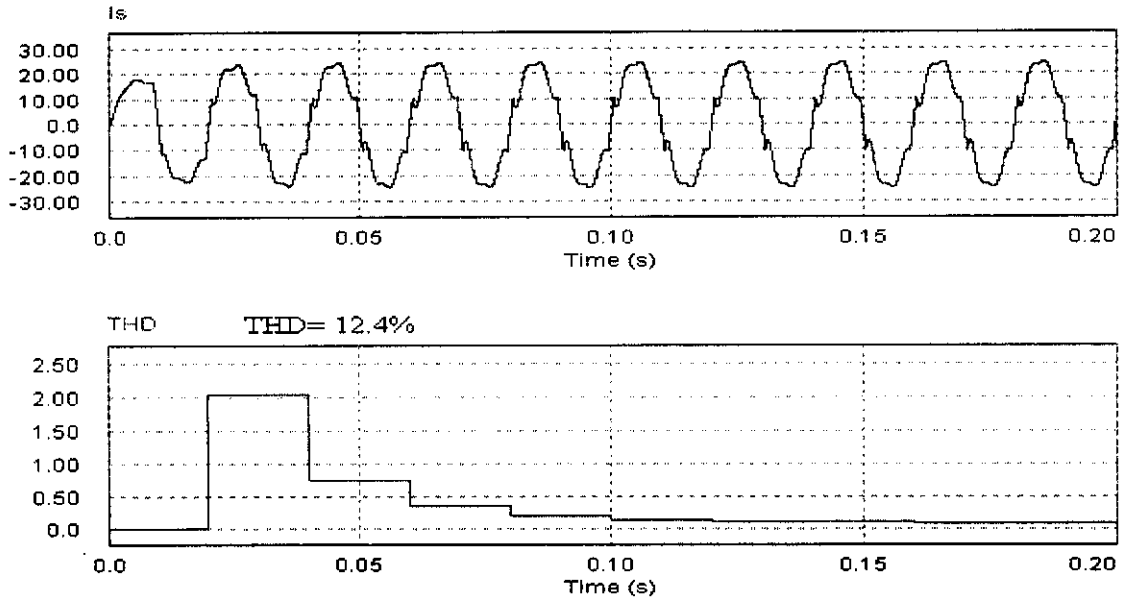

Fig 6.3 Source current, THD of the system with passive filter alone

6.4.3 WITH ACTIVE FILTER ALONE

The source current and the THD of the system when active filter alone is connected to it is shown in Fig 6.4. The distortions in source current are further minimized due to the elimination of all harmonic components by the active filter. The THD of source current is reduced to 5.7%.

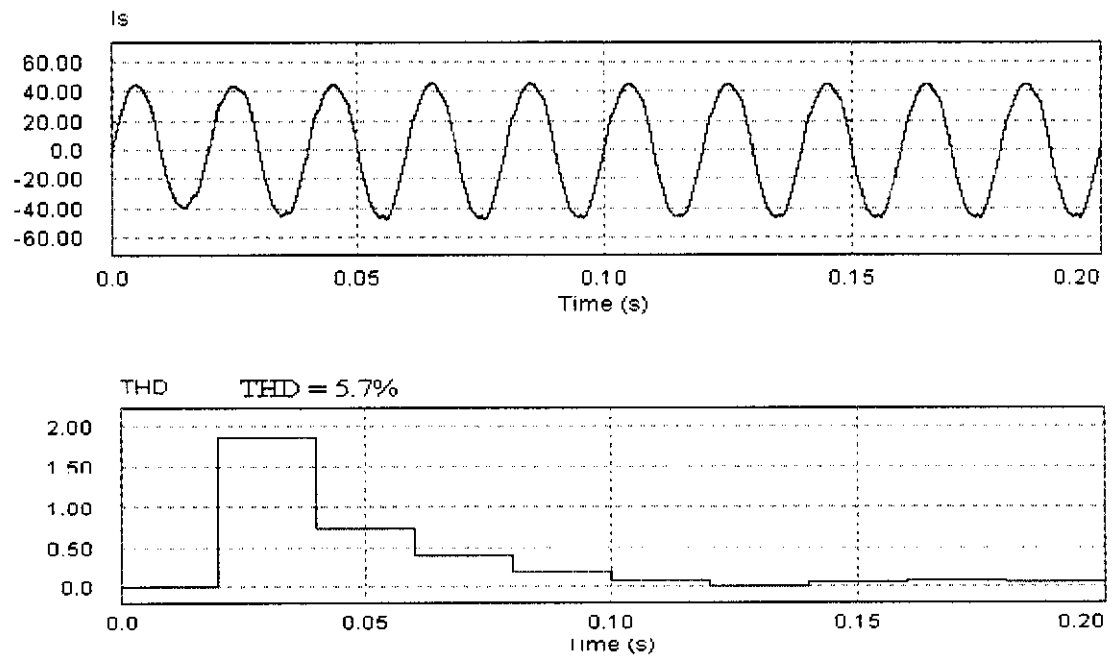

Fig 6.4 Source current, THD of the system with active filter alone

6.4.4 WITH HYBRID FILTER

The source current and the THD of the system when hybrid filter is connected to it is shown in Fig 6.5. The distortions in source current are further minimized due to the elimination of all harmonic components by the hybrid filter. The THD of source current is reduced to 5.1%. The improvement in THD for the connection of active filter alone and that of hybrid filter is very small but the addition of passive filter in parallel to active filter reduces the rating and thereby the cost of active filter.

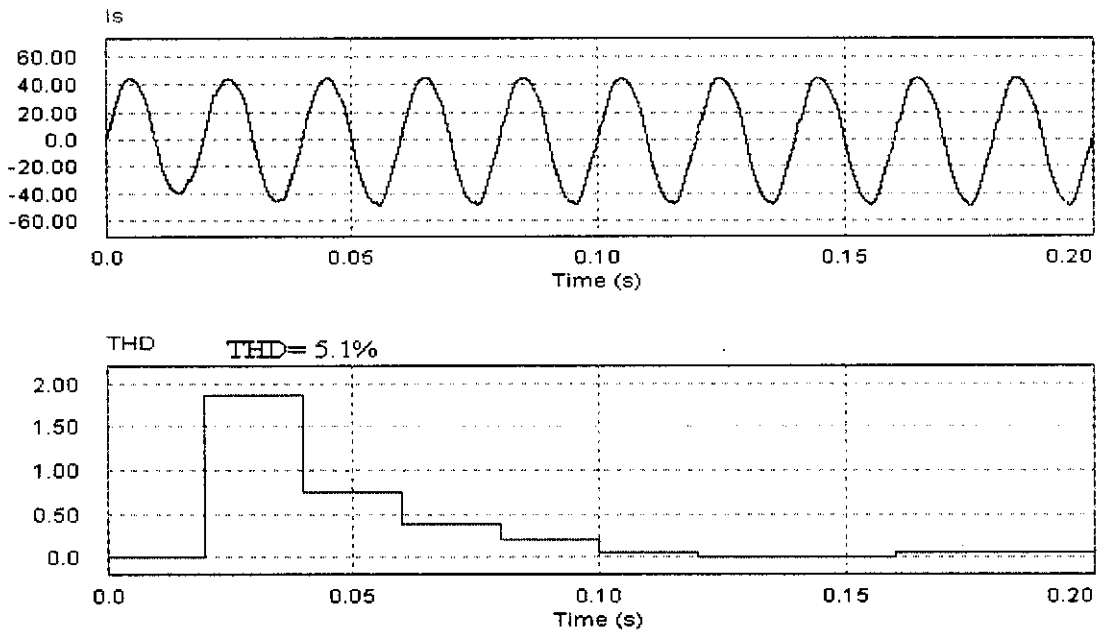

Fig 6.5 Source current, THD of the system with hybrid filter

Supply voltage and supply current, DC capacitor voltage of active filter, power factor of the system with hybrid filter is shown in fig 6.6. Due to power factor compensation the supply voltage and supply current are in phase and also the power factor is maintained at 0.99. The DC capacitor voltage is maintained nearly constant at 50V.

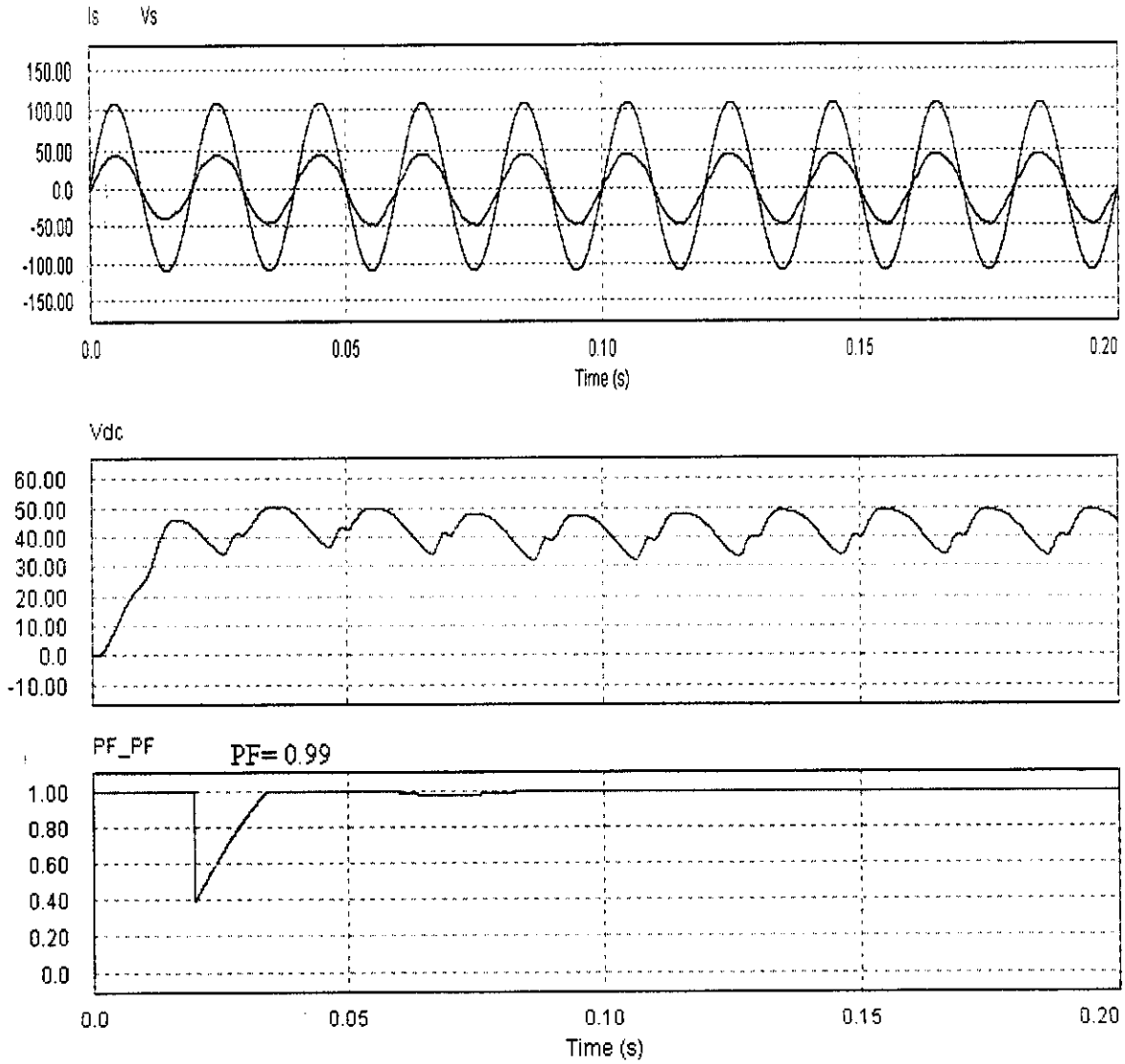

Fig 6.6 Supply voltage & supply current, DC capacitor voltage of active filter, power factor of the system with hybrid filter

The active filter current and passive filter current are shown in fig 6.7. These are the currents delivered by the filters in order to cancel harmonic current and to make the source current sinusoidal.

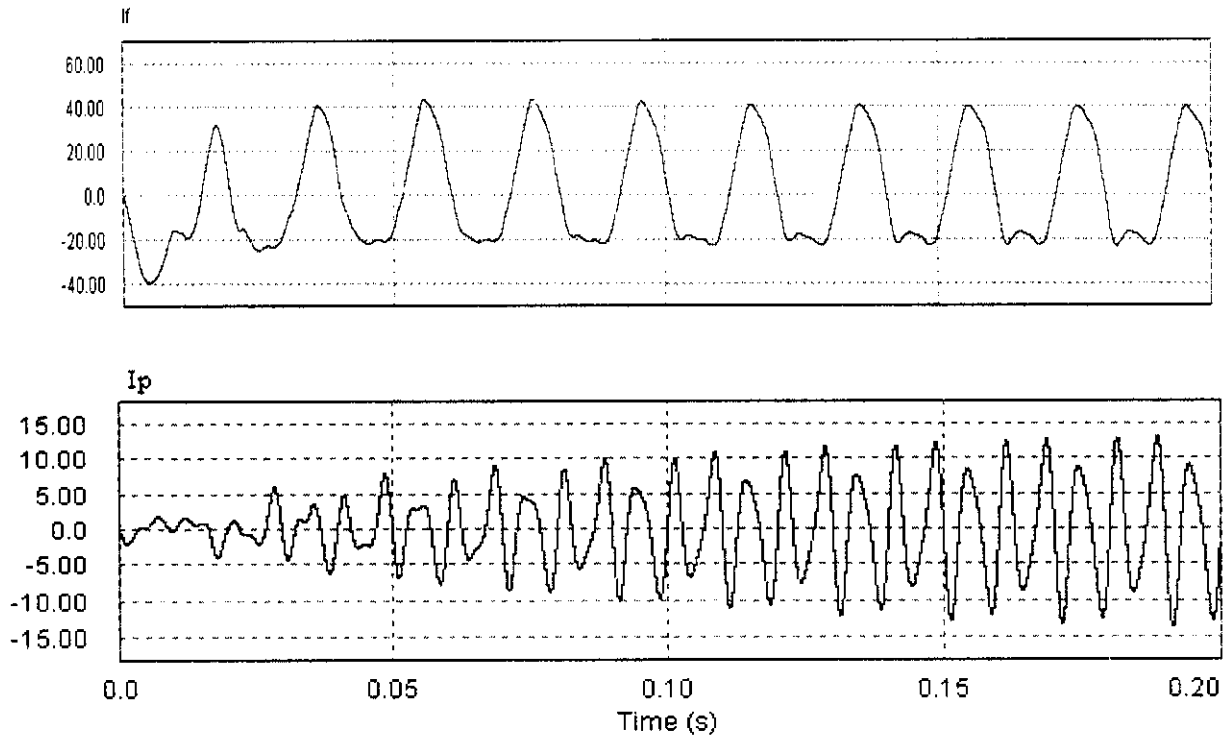

Fig 6.7 Active and passive filter current

The comparison of THD of source current and input power factor of the system without filter, with active filter alone, with passive filter alone and with hybrid filter is made and it is shown in Table 6.1.

Table 6.1 Comparison of results

Case	THD of source current	Input power factor
Without filter	26.8%	0.93
With passive filter alone	12.4%	0.99
With active filter alone	5.7%	0.99
With both Active and Passive filter	5.1%	0.99

CHAPTER 7

CHAPTER 7

HARDWARE IMPLEMENTATION OF HYBRID POWER FILTER

7.1 BLOCK DIAGRAM OF HYBRID POWER FILTER

This chapter explains the block diagram and components used for the hardware prototype of the proposed system. It includes the photographs of the fabricated model and output waveform. The voltage of the system is reduced to 24V. The schematic is done in AutoCAD.

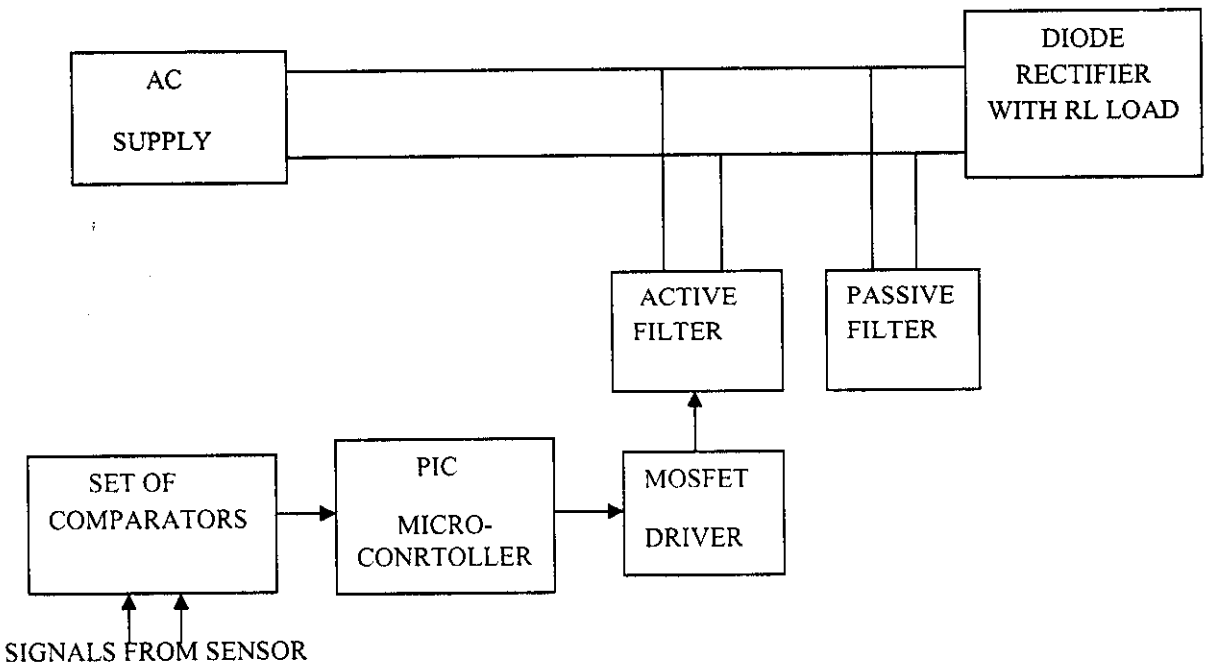

Fig 7.1 Hardware Block Diagram

The prototype of the proposed system consists of active filter, passive filter, set of comparators, micro controller (PIC16F877A) with 5V power supply unit. These parts are explained with schematic diagram in following sections.

7.1.1 ACTIVE FILTER

Active filter is a voltage source inverter. It consists of half bridge inverter with a DC side capacitor. The inverter consists of two MOSFET switches. These power switches are driven by the gate pulse generated by micro controller (PIC16F877A). This circuit bridge is isolated from the gating circuit by the opto-coupler. The active filter connected across the load is shown in the fig.7.2.

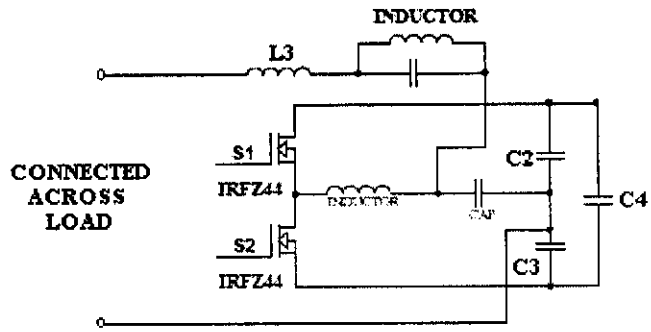

Fig 7.2 Schematic of active filter

ADVANTAGES OF MOSFET

- MOSFET provides much better system reliability.
- Driver circuitry is simpler and cheaper.
- MOSFET's fast switching speed permit much higher switching frequencies and thereby the efficiency are increased.
- Overload and peak current handling capacity is high
- MOSFETs have better temperature stability
- MOSFET's leakage current is low
- Drain-source conduction threshold voltage is absent which eliminates electrical noise.
- MOSFETs are able to operate in hazardous radiation environments.

Here N-Channel Power MOSFETs IRFZ44 are used with the common emitter configuration. The details of IRFZ44 are given in APPENDIX I

7.1.2 SET OF COMPARATORS

The set of comparators are used for generating the compensation current required to cancel the harmonic current produced by load. For this purpose OP-AMP LM358 is used. The details of the LM358 is given in APPENDIX I

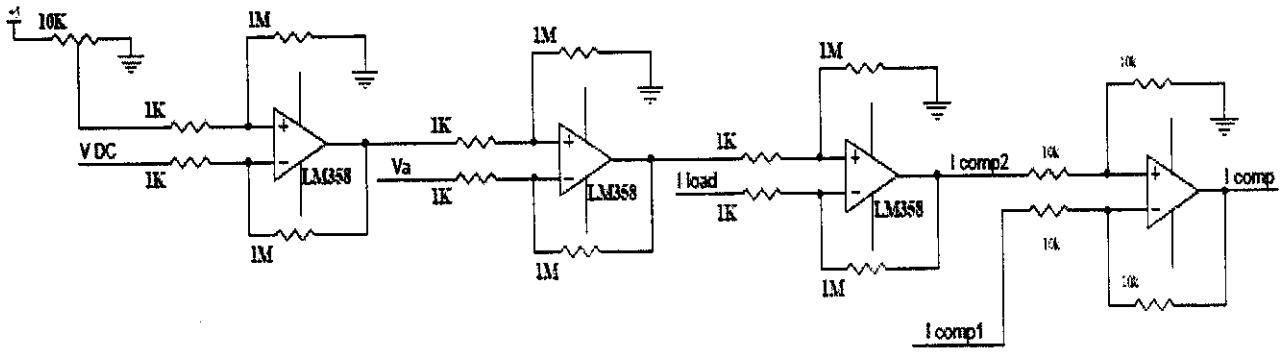

Fig 7.3 Schematic of the set of comparators

7.1.3 MICROCONTROLLER FOR PULSE GENERATION

The gate pulse for the active filter switches is generated by PIC16F877A controller. This micro controller circuit works in 5V power supply. The details about PIC16F877A is given in APPENDIX II. This controller is isolated from the main circuits by means of opto-coupler. The schematic of micro controller circuit is shown in fig.7.4.

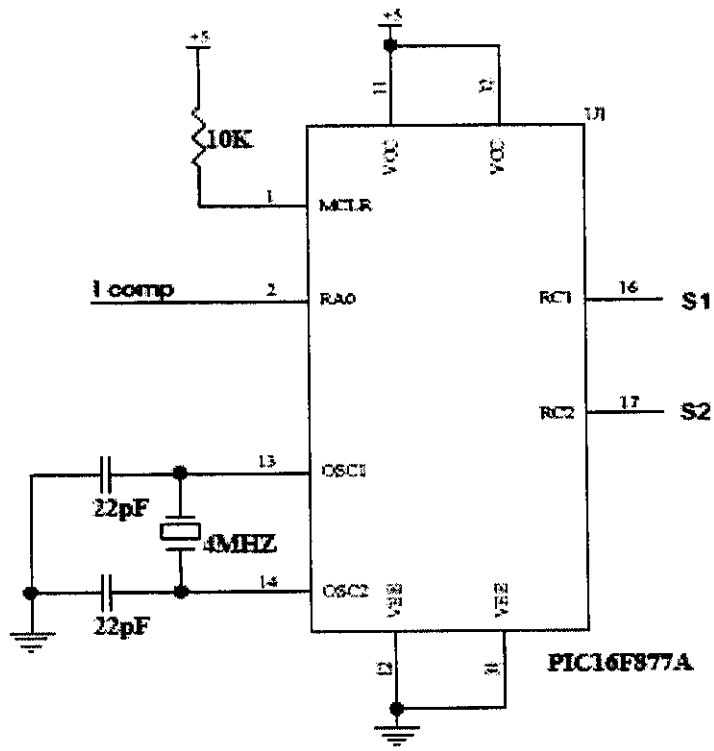

Fig7.4 Schematic of micro controller circuit

7.1.4 POWER SUPPLY

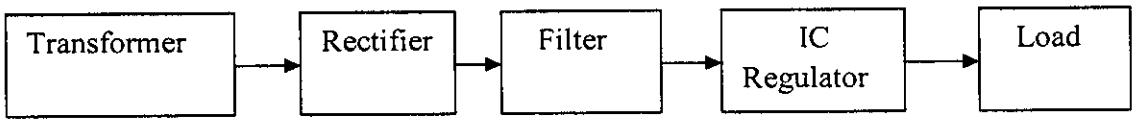

Figure 7.5 Block diagram of power supply

The Ac voltage, typically 220V rms, is connected to a transformer, which steps that ac voltage down to the level of the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation.

A regulator circuit removes the ripples and also remains the same dc value even if the input dc voltage varies, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of the popular voltage regulator IC units. The power circuit diagram is shown in figure 7.6

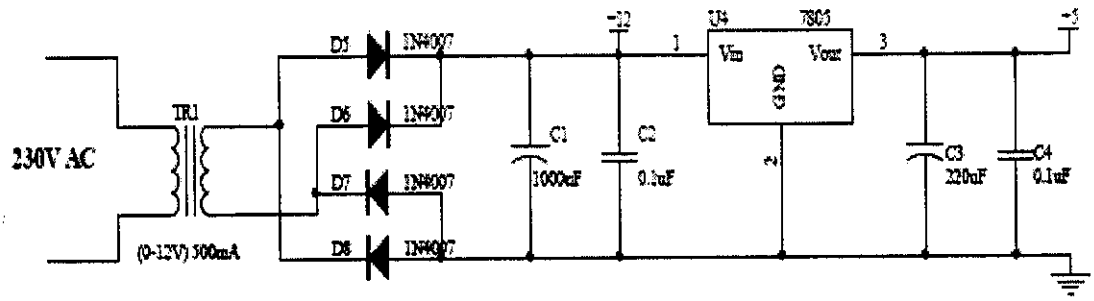

Figure 7.6 Power circuit diagram

7.2 HARDWARE PROTOTYPE AND RESULTS

The fabricated hardware model is as shown in fig.7.7. The waveforms of the source current of the system without filter and that with filter and pulses to the switches of active filter are shown in the figures 7.8, 7.9 and 7.10.

Fig 7.7 Hardware prototype

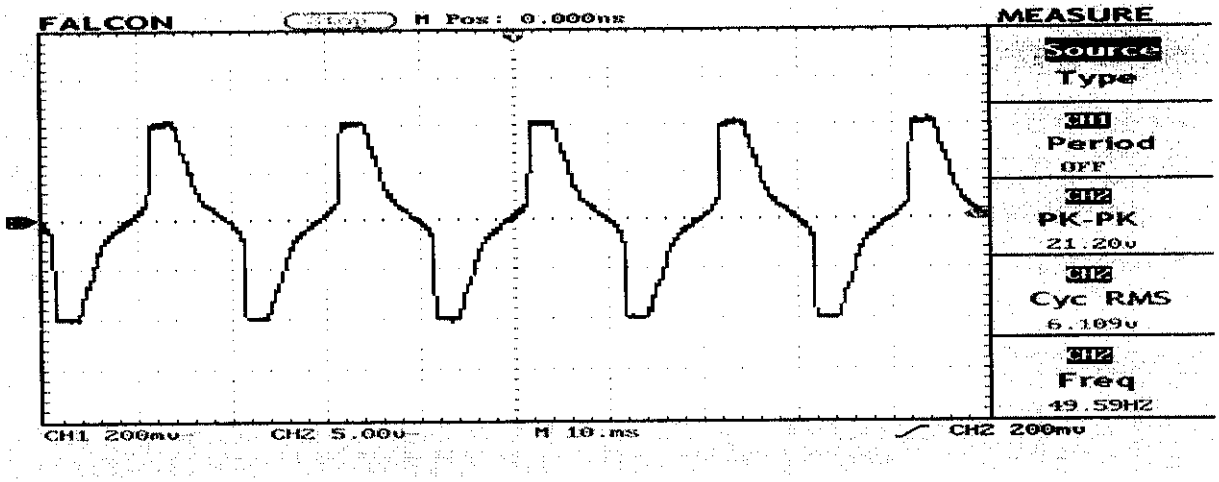

Fig 7.8 Source current waveform of the system without filter

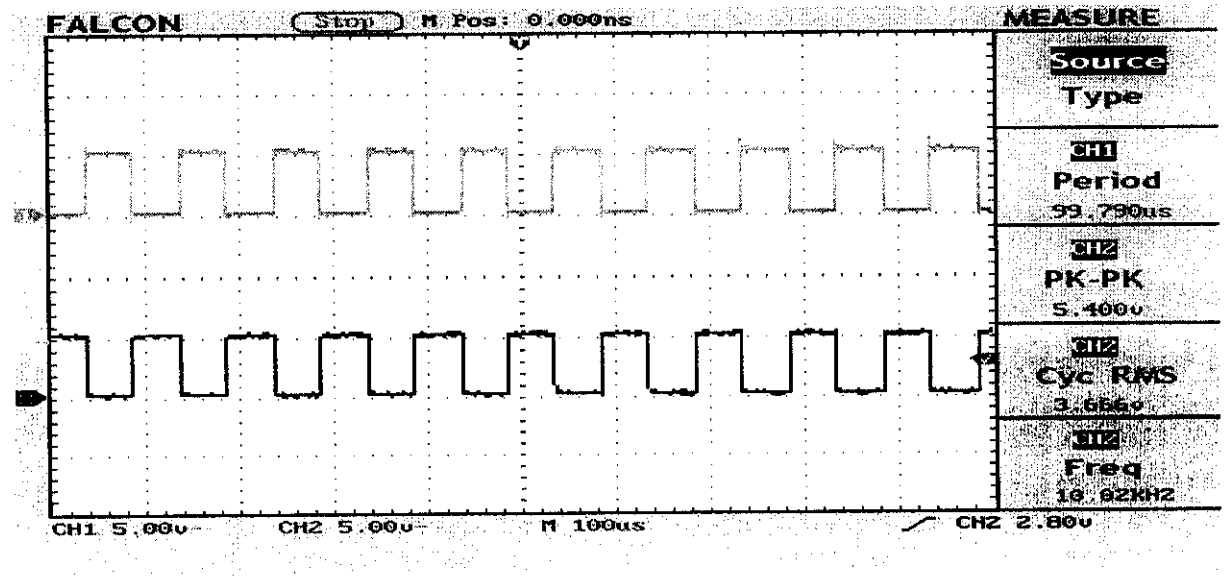

Fig 7.9 Pulses to the switches of active filter

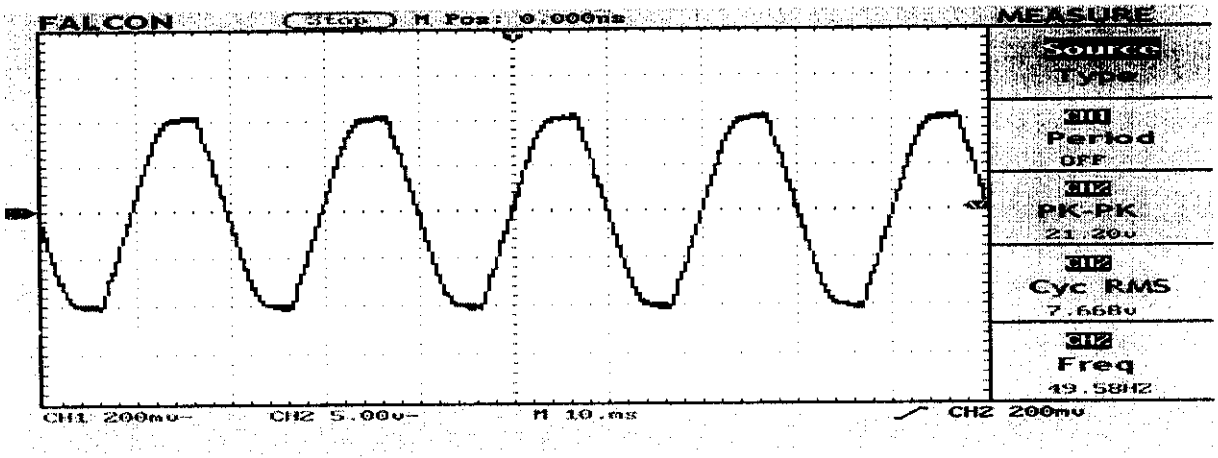

Fig 7.10 Source current waveform of the system with hybrid filter

CHAPTER 8

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION

In order to reduce the rating of active power filter, hybrid power filter which combines the advantages of both passive and active filter for nonlinear load compensation is presented in this paper. A simple control scheme of the single phase shunt active power filter is proposed which requires sensing of one voltage and two currents only. The proposed HPF reduces THD of supply current nearly to the prescribed permitted limits specified by IEEE519. The THD of source current is reduced from 26.8% to 5.1%. The quality of the supply is improved so as to meet the requirement of neighboring sensitive loads. The reactive power compensation provides the improved power factor and also reduces the losses in the electrical devices connected with the system.

8.2 FUTURE SCOPE

In the future scope of the work, the proposed hybrid filter topology can be extended for three phase non-linear loads with MOSFET switches of active filter replaced by IGBT switches to reduce THD of source current. The efficiency of hybrid filter can be improved further by using fuzzy logic controller and adaptive neural network control and implementing those techniques in Digital Signal Processor (DSP).

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APPENDIX I

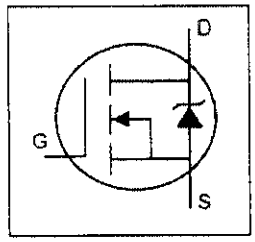
International
IOR Rectifier

PD - 94053

IRFZ44N

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

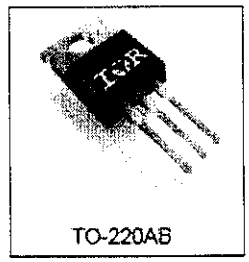
$R_{DS(on)}$ = 17.5mΩ

I_D = 49A

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	49	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	35	
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_C = 25°C	Power Dissipation	94	W
	Linear Derating Factor	0.63	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	25	A
E_{AR}	Repetitive Avalanche Energy①	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	17.5	mΩ	V_{GS} = 10V, I_D = 25A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	19	—	—	S	V_{DS} = 25V, I_D = 25A④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	63	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	—	—	14		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 28V
t_r	Rise Time	—	60	—		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		R_G = 12Ω
t_f	Fall Time	—	45	—		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1470	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	360	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	88	—		f = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	530②	150②	mJ	I_{AS} = 25A, L = 0.47mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	49	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	63	95	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse Recovery Charge	—	170	260	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.48mH R_G = 25Ω, I_{AS} = 25A. (See Figure 12)

③ I_{SD} ≤ 25A, di/dt ≤ 230A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

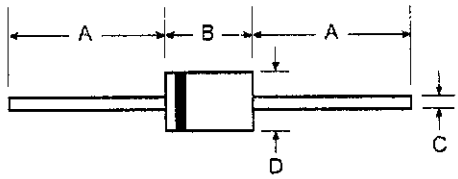
⑥ This is a calculated value limited to T_J = 175°C .

1N4001/L - 1N4007/L

1.0A RECTIFIER

Features

- Diffused Junction
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 30A Peak
- Low Reverse Leakage Current
- Plastic Material: UL Flammability Classification Rating 94V-0



	DO-41 Plastic		A-405	
Dim	Min	Max	Min	Max
A	25.40	----	25.40	----
B	4.06	5.21	4.10	5.20
C	0.71	0.864	0.53	0.64
D	2.00	2.72	2.00	2.70
All Dimensions in mm				

"L" Suffix Designates A-405 Package
No Suffix Designates DO-41 Package

Mechanical Data

- Case: Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Weight: DO-41 0.30 grams (approx)
  A-405 0.20 grams (approx)
- Mounting Position: Any
- Marking: Type Number

Maximum Ratings and Electrical Characteristics @ T_A = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

Characteristic	Symbol	1N 4001/L	1N 4002/L	1N 4003/L	1N 4004/L	1N 4005/L	1N 4006/L	1N 4007/L	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	V
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	V
Average Rectified Output Current (Note 1) @ T_A = 75°C	I_O	1.0							A
Non-Repetitive Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	30							A
Forward Voltage @ I_F = 1.0A	V_{FM}	1.0							V
Peak Reverse Current @ T_A = 25°C at Rated DC Blocking Voltage @ T_A = 100°C	I_{RM}	5.0 50							μA
Typical Junction Capacitance (Note 2)	C_j	15				8			pF
Typical Thermal Resistance Junction to Ambient	$R_{\theta JA}$	100							K/W
Maximum DC Blocking Voltage Temperature	T_A	+150							°C
Operating and Storage Temperature Range (Note 3)	T_j, T_{STG}	-65 to +175							°C

Notes: 1. Leads maintained at ambient temperature at a distance of 9.5mm from the case.
2. Measured at 1. MHz and applied reverse voltage of 4.0V DC.
3. JEDEC Value.

Order this document by LM358/D

MOTOROLA

LM358, LM258, LM2904, LM2904V

Dual Low Power Operational Amplifiers

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) single supply or split supply operation and 4) pinouts compatible with the popular MC1558 dual operational amplifier. The LM158 series is equivalent to one–half of an LM124.

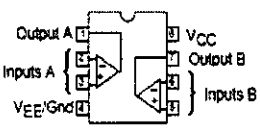
These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation

N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM258 LM358	LM2904 LM2904V	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (Note 2)	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range LM258 LM358 LM2904 LM2904V	T_A	 –25 to +85 0 to +70 – –	 – – –40 to +105 –40 to +125	°C

NOTES: 1. Split Power Supplies.
2. For Supply Voltages less than 32 V for the LM258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2904D	T_A = –40° to +105°C	SO–8
LM2904N		Plastic DIP
LM2904VD	T_A = –40° to +125°C	SO–8
LM2904VN		Plastic DIP
LM258D	T_A = –25° to +85°C	SO–8
LM258N		Plastic DIP
LM358D	T_A = 0° to +70°C	SO–8
LM358N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

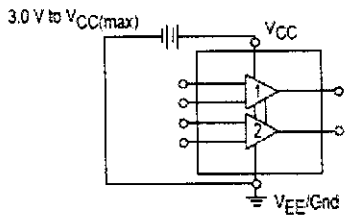
Characteristic	Symbol	LM258			LM358			LM2904			LM2904V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904, V), V_{IC} = 0 V to V_{CC} −1.7 V, V_O ≈ 1.4 V, R_S = 0 Ω	V_{IO}													mV
T_A = 25°C		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	–	–	–	
T_A = T_{high} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	–	–	13	
T_A = T_{low} (Note 1)		–	–	9.0	–	–	9.0	–	–	10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	–	45	200	
Input Bias Current	I_{IB}	–	−45	−150	–	−45	−250	–	−45	−250	–	−45	−250	
T_A = T_{high} to T_{low} (Note 1)		–	−50	−300	–	−50	−500	–	−50	−500	–	−50	−500	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	–	10	–	pA/°C
Input Common Mode Voltage Range (Note 2), V_{CC} = 30 V (26 V for LM2904, V)	V_{ICR}	0	–	28.3	0	–	28.3	0	–	24.3	0	–	24.3	V
V_{CC} = 30 V (26 V for LM2904, V), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	24	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,	A_{VOL}	50	100	–	25	100	–	25	100	–	25	100	–	V/mV
T_A = T_{high} to T_{low} (Note 1)		25	–	–	15	–	–	15	–	–	15	–	–	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	−120	–	–	−120	–	–	−120	–	–	−120	–	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	50	100	–	50	100	–	dB
Output Voltage–High Limit (T_A = T_{high} to T_{low}) (Note 1)	V_{OH}													V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
V_{CC} = 30 V (26 V for LM2904, V), R_L = 2.0 kΩ		26	–	–	26	–	–	22	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2904, V), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	23	24	–	
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	20	40	–	20	40	–	20	40	–	mA
Output Sink Current	I_{O-}													
V_{ID} = −1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	10	20	–	10	20	–	mA
V_{ID} = −1.0 V, V_O = 200 mV		12	50	–	12	50	–	–	–	–	–	–	–	μA
Output Short Circuit to Ground (Note 3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low}) (Note 1)	I_{CC}													mA
V_{CC} = 30 V (26 V for LM2904, V), V_O = 0 V, R_L = ∞		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

NOTES: 1. T_{low} = −40°C for LM2904
= −40°C for LM2904V
= −25°C for LM258
= 0°C for LM358
T_{high} = +105°C for LM2904
= +125°C for LM2904V
= +85°C for LM258
= +70°C for LM358

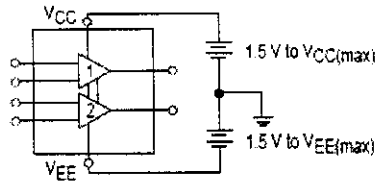
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} −1.7 V.

3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Single Supply

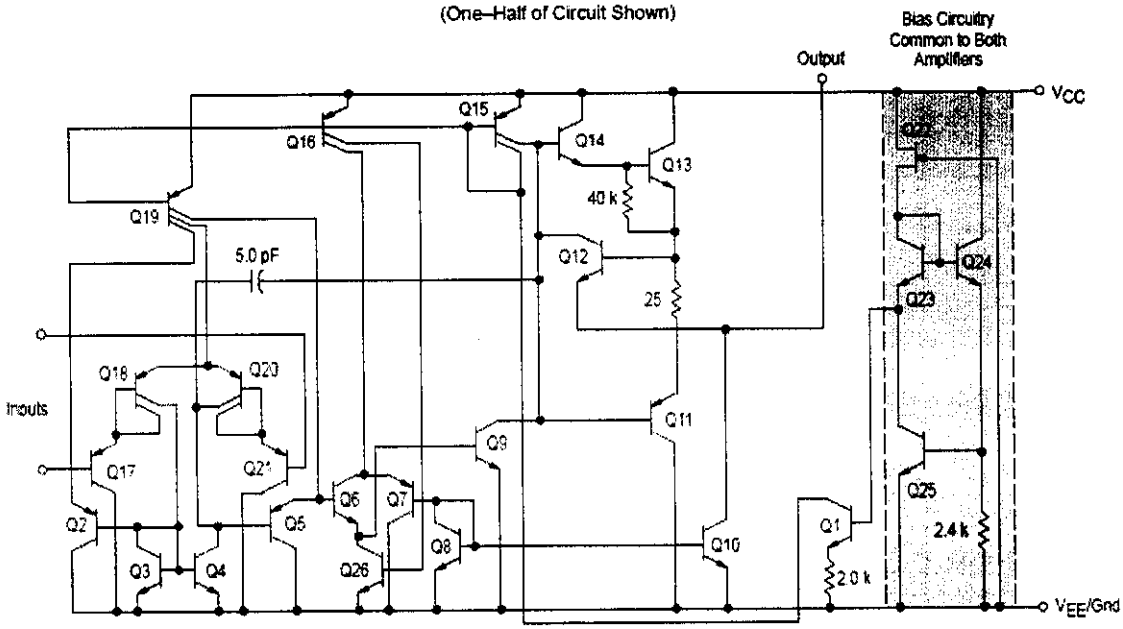


Split Supplies



Representative Schematic Diagram

(One–Half of Circuit Shown)

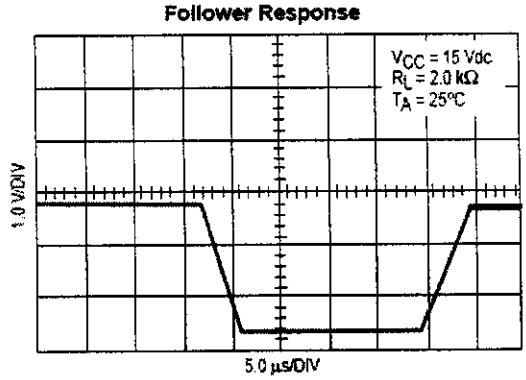


CIRCUIT DESCRIPTION

The LM258 series is made using two internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal–voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Large Signal Voltage Follower Response



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MC78XX/LM78XX/MC78XXA

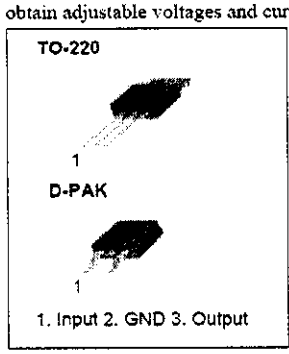
3-Terminal 1A Positive Voltage Regulator

Features

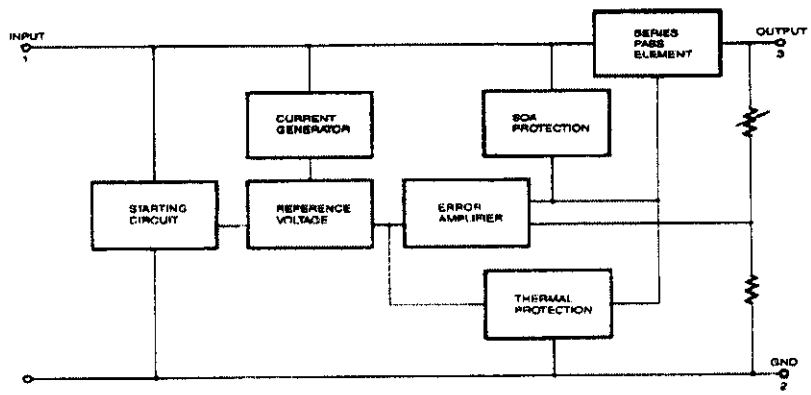
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Digram



Rev. 1.0.1

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V		4.75	5.0	5.25	
Line Regulation (Note1)	Regline	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation (Note1)	Regload	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	μV/Vo
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

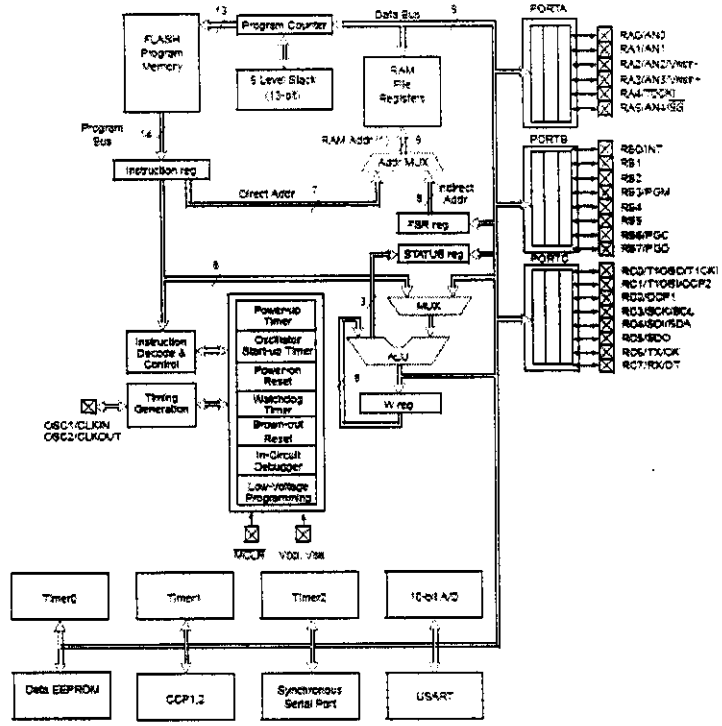
Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

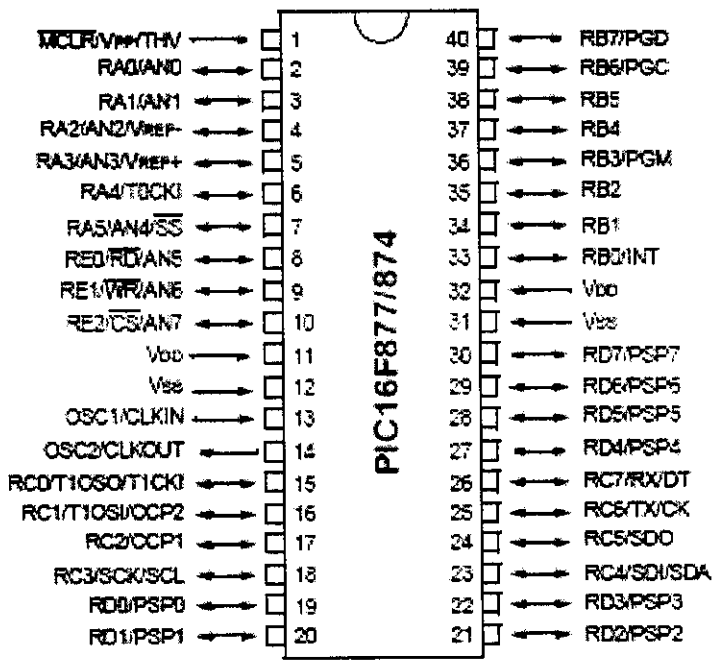
APPENDIX II

ARCHITECTURE OF PIC 16F877A

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F873	4K	192 Bytes	128 Bytes
PIC16F876	8K	368 Bytes	256 Bytes



Pin Configuration of PIC16F877A



TIMER 0 CONTROL REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7: **RBPU**

bit 6: **INTEDG**

bit 5: **T0CS**: TMR0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

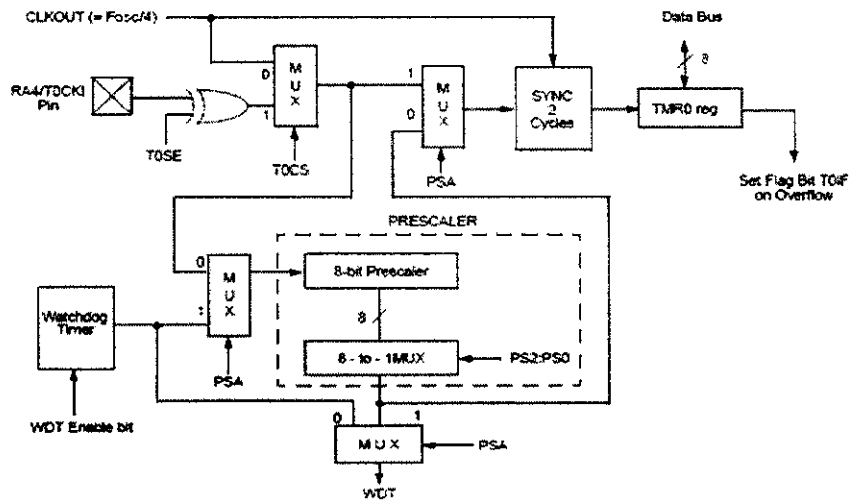
bit 3: **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

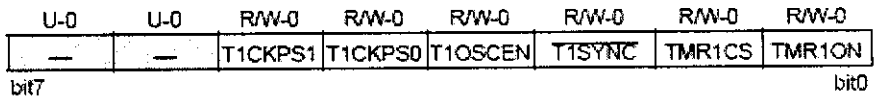
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2 PS1 PS0**: Prescaler Rate Select bits

TIMER 0 BLOCK DIAGRAM:



TIMER 1 CONTROL REGISTER:



U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled

0 = Oscillator is shut off (The oscillator inverter is turned off to eliminate power drain)

bit 2: **T1SYNC**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1

1 = Do not synchronize external clock input

0 = Synchronize external clock input

TMR1CS = 0

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)

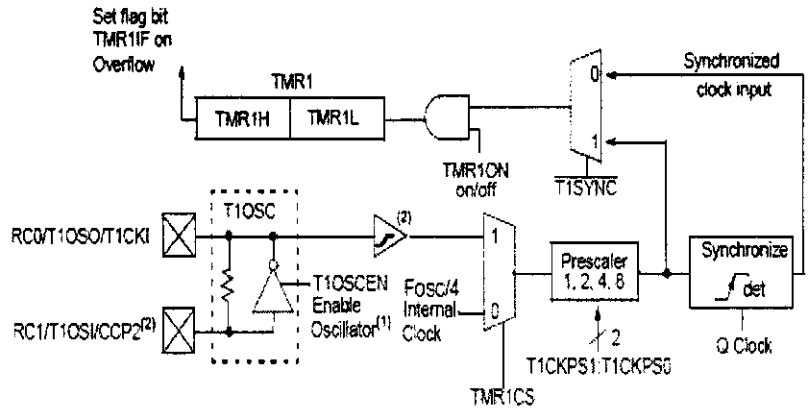
0 = Internal clock (FOSC/4)

bit 0: **TMR1ON**: Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

TIMER 1 BLOCK DIAGRAM:



TIMER 2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale

0001 = 1:2 Postscale

0010 = 1:3 Postscale

1111 = 1:16 Postscale

bit 2: **TMR2ON**: Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

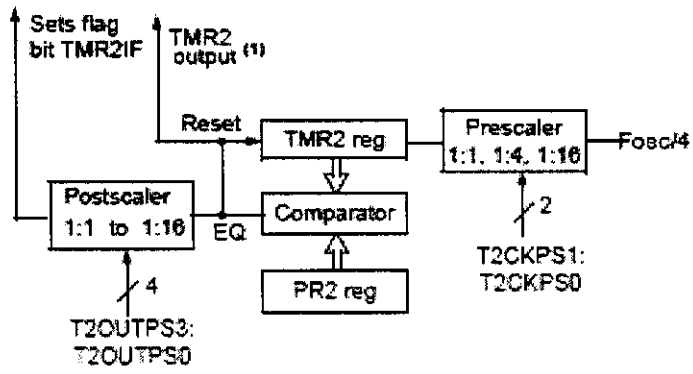
bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

TIMER2 BLOCK DIAGRAM:



CCP1CON REGISTER/CCP2CON REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX :CCPxY**: PWM Least Significant bits

Capture Mode: Unused

Compare Mode: Unused

PWM Mode: These bits are the two LSB s of the PWM duty cycle. The eight MSB s are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets CCPx module)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (CCPxIF bit is set)

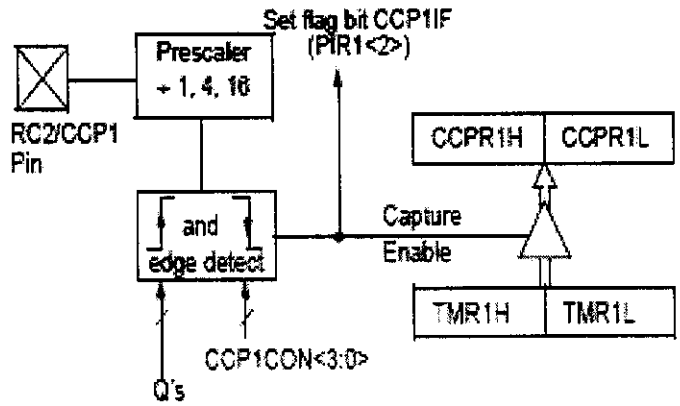
1001 = Compare mode, clear output on match (CCPxIF bit is set)

1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)

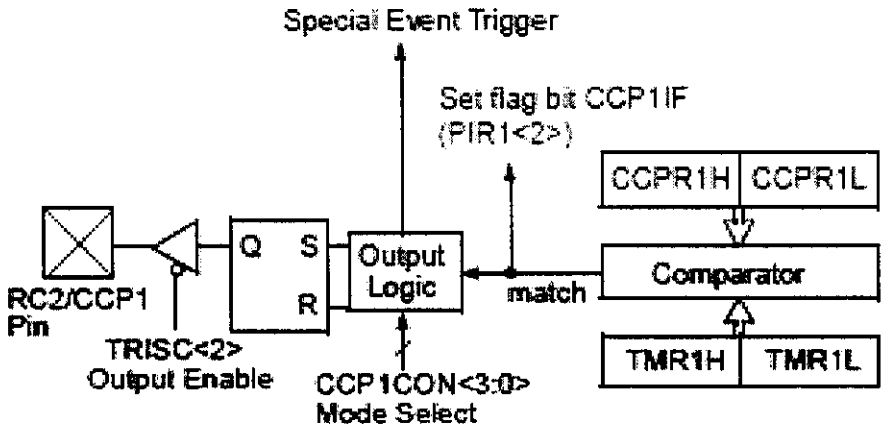
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)

11xx = PWM mode

CAPTURE MODE OPERATION BLOCK DIAGRAM:



COMPARE MODE OPERATION BLOCK DIAGRAM:



APPENDIX III

PiC PROGRAMMING

```
#include<pic.h>
__CONFIG(0X20E4);
__CONFIG(0X3FFF);
unsigned int REFF1,INPUT1,REFF2,INPUT2;
unsigned char count;
delay(void);
delay1(void);
void main()
{
        TRISC=0;
        PORTC=0;
        TRISA=0XFF;
        ANSEL=0X0F;
        ANSELH=0;
        ADCON1=0X80;
        PR2=99;
        T2CON=0X04;
        CCP1CON=0X0F;
        CCPR1L=25;
        CCP2CON=0X0C;
        CCPR2L=75;
        while(1)
        {
/****************** ADC SCAN ****************/
                ADCON0=0X81;       // adc AN0
                delay();
```

```
                GODONE=1;
                while(GODONE);
                REFF1=(ADRESH*256)+ADRESL;
/****************** ADC SCAN END ********************/
/******************  PWM LIMIT  ********************/
                if(CCPR1L<30)
                CCPR1L=30;
                if(CCPR1L>85)
                CCPR1L=85;
/************** OUTPUT REGULATION*****************/
                delay1();
                if(REFF1>600)
                CCPR1L--;
                delay();
                if(REFF1<600)
                CCPR1L++;
                delay1();
        }
}
delay()
{
        unsigned int i;
        for(i=0;i<100;i++);
}
delay1()
{
        unsigned int j;
        for(j=0;j<10000;j++);
```