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Impedance Source Inverter for Wind Turbine Driven Permanent Magnet Synchronous Generator

A Project Report

Submitted by

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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

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BONAFIDE CERTIFICATE

Certified that this project report entitled **"Impedance Source Inverter for Wind Turbine Driven Permanent Magnet Synchronous Generator"** is the bonafide work of

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It is hereby certified that T. MUTHUKUMAR

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has participated in the First National Conference on **"RECENT ADVANCES IN POWER ELECTRONICS AND INDUSTRIAL DRIVES"** (PEID) 2011 and presented a paper titled IMPEDANCE SOURCE INVERTER FOR WIND TURBINE DRIVEN PERMANENT MAGNET SYNCHRONOUS GENERATOR on March 04/05,2011

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ABSTRACT

The main thrust in Wind Energy Conversion System (WECS) is to maintain a constant voltage at the output in spite of variations in wind velocity. The Impedance Source Inverter (ZSI) has been identified to exhibit in steady-state, both voltage buck-and boost-capabilities. It employs a unique impedance network included between the DC power source and converter circuit. The Impedance Source Inverter system employs a unique *LC* network in the dc link and a small capacitor on the ac side of the diode front end. By controlling the shoot-through duty cycle, the Impedance source can produce any desired output AC voltage, even greater than the line voltage. All the traditional pulse width modulation (PWM) schemes can be used to control the Impedance Source inverter. When the DC voltage is high enough to generate the desired AC output voltage, normal PWM is used. While the DC voltage is not enough to directly generate a desired output voltage, a modified PWM with shoot-through zero states is employed to boost the voltage. The proposed Impedance Source inverter with Permanent Magnet Synchronous Generator (PMSG) and wind turbine are modeled and simulated using MATLAB/SIMULINK.

ACKNOWLEDGEMENT

At this delightful moment of having accomplished, I extend my sincere thanks to the management of Kumaraguru College of Technology.

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ABREVIATIONS

WECS	-	Wind Energy Conversion System
PMSG	-	Permanent Magnet Synchronous Generator
ZSI	-	Impedance Source Inverter
VSI	-	Voltage Source Inverter
CSI	-	Current Source Inverter
DC	-	Direct Current
AC	-	Alternating Current
EMI	-	Electro Magnetic Interference
PWM	-	Pulse Width Modulation

LIST OF SYMBOLS

SYMBOL		DESCRIPTION
B	-	Boost Factor
B_b	-	Buck-Boost Factor
C	-	Capacitance
d_s	-	Duty cycle of the shoot –through state
E_s	-	Voltage Source of ZSI
I_c	-	Capacitor current of ZSI
I_i	-	Current at the output terminal connected to the VSI
I_L	-	Inductance current of ZSI
I_s	-	Input Current at the terminals of the impedance network connected to the source
I_{1fA}	-	Final value of current in Active- 1 state
I_{1fS}	-	Final value of current in Shoot-Through- 1 State
I_{liA}	-	Initial value of current in Active- 1 state
I_{liS}	-	Initial value of current in Shoot-Through- 1 state
ΔI_c	-	Peak value of the capacitor current ripples
K	-	Ratio of peak ripples to their average values

T	-	Shoot-Through-1 state
t_A	-	Active-1 state
T	-	Total time period
T_s	-	Period of the switching cycle of VSI
T_1	-	Non-Shoot -Through period
v_a	-	Phase A inverter output voltage
V_{ac}	-	Output line voltage of Z-source inverter
v_b	-	Phase B inverter output voltage
v_c	-	Phase C inverter output voltage
V_c	-	Capacitor Voltage
V_{ciA}	-	Initial capacitor voltage in active state
V_{cfS}	-	Final capacitor voltage in active state
V_{cmin}	-	Minimum capacitor voltage
V_{dc}	-	DC voltage
V_i	-	Voltage at the output terminal connected to the VSI
ΔV_c	-	Peak value of the capacitor voltage ripples
$\overline{Vc}$	-	Average capacitor voltage
λ	-	Ratio of average capacitor voltage to source volt

CHAPTER 1

CHAPTER 1

INTRODUCTION

As energy demands around the world increase, the need for renewable energy source that will not harm the environment has been also increased. Some projections indicate that the global energy demand will almost triple by 2050. Oil can only supply the world for up to 150 years. Using wind energy is one way to meet the future need. So, it can be said that the wind energy is the fuel of the future. Utilities have the flexibility to accept a contribution of about 20% or more from wind energy systems and more than 50% fuel savings from wind-diesel systems.

Nowadays, wind power is the most rapidly growing technology for renewable power generation and it could supply 12 percent of world's electrical demand by 2020. The capital cost of small wind turbine driven electrical power generation system (of rating less then 15kW) is very competitive compared to that of other known non-polluting and renewable energy sources. This project addresses the issues related to the implementation of permanent magnet generators for the stages of power conversion of wind energy. Permanent magnet generators are preferred over induction generators, in view of this improved efficiency and non drawal reactive excitation current.

1.1 NEED FOR THE PROJECT

Power generation using wind-driven windmills (turbines) is usable in areas that have good wind resources and that can benefit from the addition of wind-generated power into a constant load or local power transmission system. However, wind turbines are relatively unstable power sources that fluctuate with wind conditions and must be properly interfaced to avoid carrying over instabilities into a constant load or grid. A wind farm connected to a constant load or to a weakly supported transmission line or to a relatively small transmission system (such as for an isolated region or island) can inject instabilities in both voltage and frequency of the backbone transmission system because of the gusty and turbulent nature of the wind source. Even on a more robust, interconnected transmission system, such instabilities can create disturbances that propagate through the system.

The change in energy output of the wind farm is reflected by changes in both frequency and voltage in the load to which the wind farm is connected. In extreme cases, these fluctuations may become large enough that it is necessary to disconnect the wind farm from the transmission system and simply waste the wind energy. Such conditions have a strong economic impact on a wind farm, which recovers costs only when electricity is being generated. Under less extreme conditions, the shifting winds create energy surges that are reflected in lower-level voltage and frequency disturbances on the transmission system-over a period of 1-2 minutes.

1.1.1 EXISTING METHODOLOGY

The basic components of a wind electric system considered in this project are shown in figure 1.1 Wind Turbine converts wind energy in to rotary mechanical energy. A mechanical interface consists of step up gear and a suitable coupling transmitter, which is connected between wind turbine and Permanent Magnet Synchronous Generator (PMSG). The electric power from generator is connected to local load through power converters, where output with constant voltage and constant frequency can be obtained.

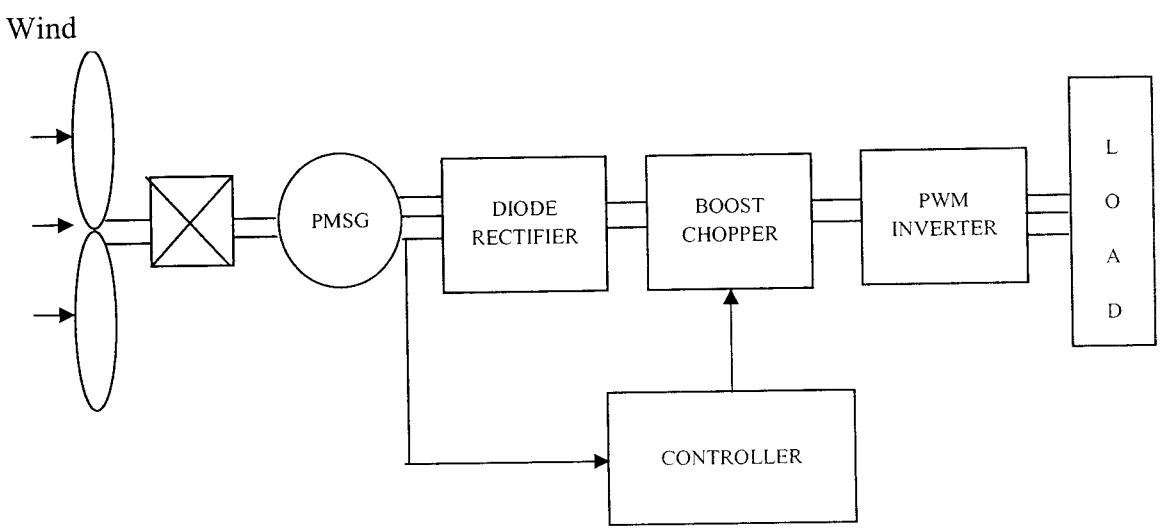


Figure 1.1 Block Diagram of the Existing System

The wind turbine converts the kinetic energy of the wind into mechanical energy, which drives the permanent magnet synchronous generator through a gear box. Since the wind is an intermittent source of energy, the output voltage and frequency from generator will vary according to the wind velocities. The variable AC power from the generator is first rectified into DC using diode bridge rectifier. The voltage across the rectifier terminal is regulated for constant voltage by controlling the duty ratio. The constant DC output is inverted and, fed to the load at the required level of voltage and frequency employing a PWM inverter.

1.1.2 DRAWBACKS

The traditional wind energy conversion system employs a Diode Rectifier, a Boost Chopper and a PWM inverter. The boost chopper can boost up the voltage to a certain extent only. If the wind speed is very less this system fails to work properly.

1.1.3 PROPOSED METHODOLOGY

The proposed micro controller based control for the Z-Source inverter is expected to exhibit both buck and boost capabilities, for which a unique LC impedance network is introduced between the dc power source and inverter circuit. The Z-Source Inverter has the advantage of both the Voltage Source Inverter and Current Source Inverter. It can be used as both the buck and boost inverter. So the required output voltage is obtained in spite of the variation in the wind speed. Thus the overall efficiency of the system is improved.

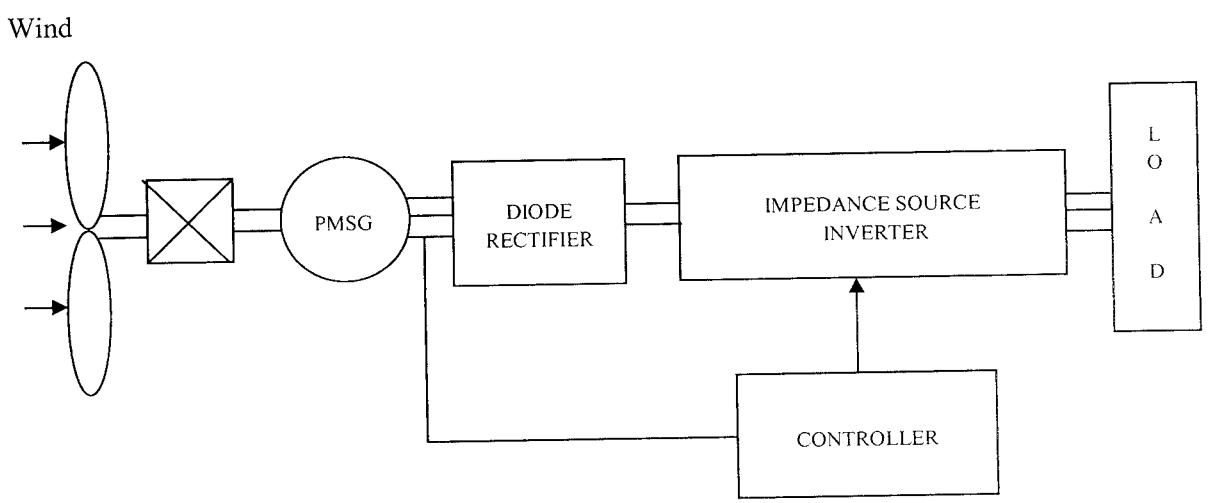


Figure 1.2 Block Diagram of the proposed System

1.2 OBJECTIVE OF THE PROJECT

Objectives of the project are as follows:

- To maintain constant output voltage in spite of the variation in the wind speed.
- To prevent the voltage instabilities caused due to variable wind speed.
- It can also improve the overall system stability.

1.3 ORGANIZATION OF THESIS

This gives an overall outline of the Project report.

CHAPTER 1

It describes the general Introduction, Objective and Need for the Project

CHAPTER 2

It describes the Basic Consideration of Wind Energy Conversion System with ZSI

CHAPTER 3

It describes about the Impedance Source Inverter

CHAPTER 4

In this chapter describes the Design of Z-Source Inverter

CHAPTER 5

It includes the introduction of MATLAB (simulink), simulation details of individual block and simulation results of the system.

CHAPTER 6

It includes the proposed system model and description of all hardware components. It shows the schematic diagram of the hardware and output waveforms and test results.

CHAPTER 7

Gives the Conclusion and Recommendations for the future work.

CHAPTER 2

CHAPTER 2

BASIC CONSIDERATION OF WECS WITH ZSI

2.1 WIND TURBINE MODEL

There are two types of wind turbines namely vertical axis and horizontal axis types. Horizontal axis wind turbines are preferred due to the advantages of ease in design and lesser cost particularly for higher power ratings.

The power captured by the wind turbine is obtained as

$$P = \frac{1}{2}\pi\rho R^2 V^2 C_p \qquad (1)$$

where the power coefficient Cp is a nonlinear function of wind velocity and blade pitch angle and is highly dependent on the constructive features and characteristics of the turbine. It is represented as a function of the tip speed ratio given by

$$\lambda = \frac{R\omega_t}{V} \qquad (2)$$

It is important to note that the aerodynamic efficiency is maximum at the optimum tip speed ratio. The torque value obtained by dividing the turbine power by turbine speed is formed obtained as follows:

$$T_t(V, \omega_t) = \frac{1}{2}\pi\rho R^2 C_t(\lambda) V^2 \qquad (3)$$

Where

$C_t(\lambda)$ is the torque co-efficient of the turbine, given by

$$C_t(\lambda) = \frac{C_p(\lambda)}{(\lambda)} \qquad (4)$$

The power coefficient Cp is given by

$$C_p(\lambda) = \left(\frac{116}{\lambda 1} - (0.4 * \beta) - 5\right) 0.5 e^{\frac{-165}{\lambda}} \qquad (5)$$

Where

$$\lambda 1 = \frac{1}{\left(\frac{1}{(\lambda + 0.089\beta)} - \frac{0.035}{(\beta^2 + 1)}\right)} \qquad (6)$$

Generated emf/phase,

$$E = V_t + I_a(R_a + jX_s) = V_t + I_a Z_s \qquad (7)$$

where

$$Z_s = \sqrt{R_a{}^2 + X_s{}^2}$$

2.2 PERMANENT MAGNET GENERATOR MODEL

Permanent Magnet Generator provides an optimal solution for varying-speed wind turbines, of gearless or single-stage gear configuration. This eliminates the need for separate base frames, gearboxes, couplings, shaft lines, and preassembly of the nacelle. The output of the generator can be fed to the power grid directly. A high level of overall efficiency can be achieved, while keeping the mechanical structure of the turbine simple.

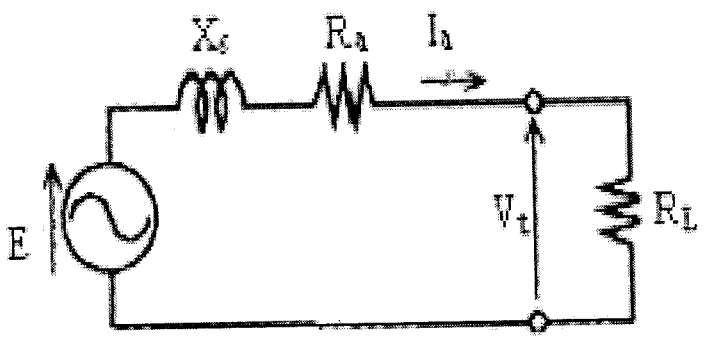


Figure 2.1 Per phase equivalent circuit of PMG.

The rotor reference frames of the voltages are obtained as the rotor reference frames of the voltages are

$$V_q = -(R_s + L_q p)I_q - \omega_r L_d I_d + \omega_r \lambda_m \qquad (8)$$

$$V_d = -(R_s + L_d p)I_d + \omega_r L_q I_q \qquad (9)$$

The expression for the electromagnetic (EM) torque in the rotor is given by

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P_n}{2}\right)[(L_d - L_q)I_q I_d - \lambda_m I_q] \qquad (10)$$

The relationship between the angular frequency of the stator voltage (ω_r) and the mechanical angular velocity of the rotor (ω_m) is obtained as follows:

$$\omega_r = \frac{P_n}{2}\omega_m G \qquad (11)$$

$$p\omega_r = \frac{P_n}{2J_g}(T_m - T_e) \qquad (12)$$

$$p\theta = \omega_r \qquad (13)$$

Torque developed by the turbine Tt released to the input to the generator Tm is expressed as

$$T_m = \frac{T_t}{G} \qquad (14)$$

2.3 TRADITIONAL INVERTERS

Traditionally, power inverters can be broadly classified as either the Voltage Source Inverter (VSI) or Current Source Inverter (CSI) type. For a VSI the inverter is fed from a dc voltage source usually with a relatively large capacitor connected in parallel. It is well known that the maximum ac voltage output of a VSI is limited to 1.15 times half the dc source voltage (using modulation strategies with offsets added) before being over-modulated.

The VSI can therefore only be used for buck (step-down) dc-ac power conversion or boost (step-up) ac-ac power rectification assuming that no additional dc-dc inverter is used to buck/boost the dc link voltage. On the other hand, a CSI is fed from a dc current source, which is usually implemented by connecting a dc source in series with a relatively large inductor and its ac voltage output is always greater than the dc source voltage that feeds the dc-side inductor. The CSI is therefore only suitable for boost dc-ac power conversion or buck ac-dc power rectification.

2.3.1 VOLTAGE SOURCE INVERTER:

Fig. 2.2 shows the traditional VSI structure. A dc voltage source supported by a relatively large capacitor feeds the main inverter circuit, a three-phase bridge. The dc voltage-source can be a battery, fuel-cell stack, diode rectifier and/or capacitor. Six switches are used in the main circuit; each is traditionally composed of a power transistor and an anti-parallel (or freewheeling) diode to provide bidirectional current flow and unidirectional voltages blocking capability.

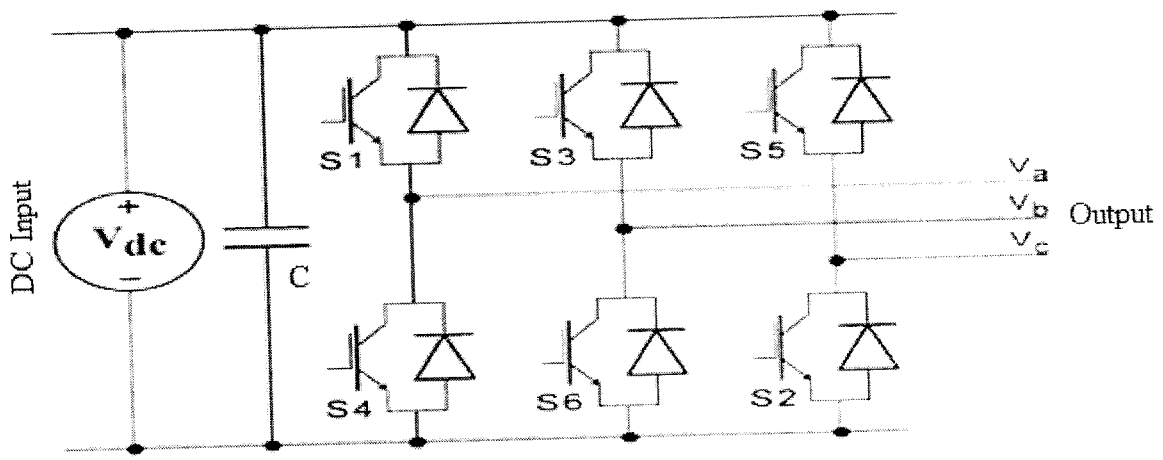


Figure 2.2 Traditional Voltage Source Inverter

2.3.2 CURRENT SOURCE INVERTER:

Fig. 2.3 shows the traditional three-phase CSI structure. A dc current source feeds the main inverter circuit, a three-phase bridge. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel cell stack, diode rectifier, or thyristor inverter.

Six switches are used in the main circuit; each is traditionally composed of a semiconductor switching device with reverse blocking capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking.

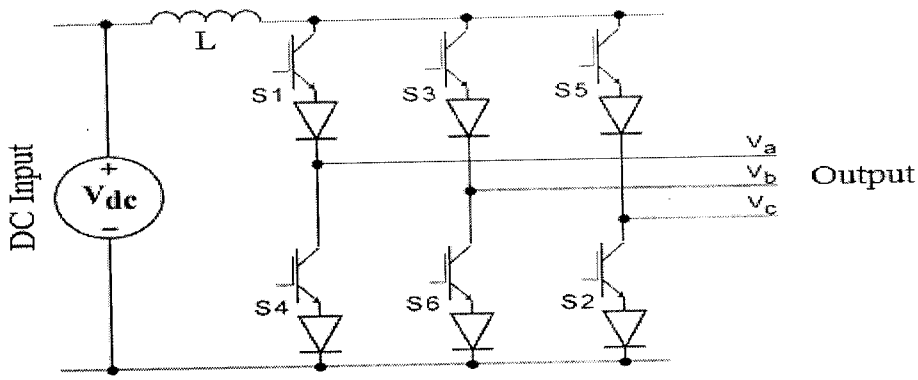


Figure 2.3 Traditional Current Source Inverter

2.3.4 DRAWBACKS:

The VSI has the following conceptual and theoretical barriers and limitations.

1. The ac output voltage is limited below and cannot exceed the dc-rail voltage or the dc-rail voltage has to be greater than the ac input voltage. Therefore, the VSI is a buck (step-down) inverter for dc-to-ac power conversion and the VSI is a boost (step-up) rectifier (or boost converter) for ac-to-dc power conversion. For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost inverter is needed to obtain a desired ac output. The additional power inverter stage increases system cost and lowers efficiency.

2. The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a Shoot-Through would occur and destroy the devices. The shoot-Through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the converter's reliability. Dead time to block both upper and lower devices has to be provided in the VSI, which causes waveform distortion.

3. An output LC filter is needed for providing a sinusoidal voltage compared with the CSI, which causes additional power loss and control complexity.

The CSI has the following conceptual and theoretical barriers and limitations,

1. The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. Therefore the CSI is a boost inverter for dc-dc power conversion and the CSI is a buck rectifier for ac-ac power conversion. For applications where a over drive is desirable, an additional dc-dc buck (or boost) converter is needed. The additional power conversion stage increases system cost and lowers efficiency.

2. At least one of the upper devices and one of the lower devices have to be gated on and maintained on any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open circuit problem by EMI noise's misgating-off is a major concern of the inverter's reliability. Overlap time for safe current communication is needed in the CSI, which also causes waveform distortion.

3. The main switches of the CSI have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high-performance IGBT modules.

In addition both the both the VSI and the CSI have the following common problems,

1. They are either a boost or a buck converter and cannot be a buck-boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage.
2. Their main circuits cannot be interchangeable. In other words, neither the VSI main circuit can be used for the CSI or vice versa.
3. They are vulnerable to EMI noise in terms of reliability.

2.4 IMPEDANCE SOURCE INVERTER:

To overcome the above problems of the traditional VSI and CSI, an impedance-source (or impedance-fed) power inverter and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion is proposed. Fig. 2.4 shows the general ZSI structure proposed. It employs a unique impedance network to couple the inverter main circuit to the power source, load, or another inverter, for providing unique features that cannot be observed in the traditional VSI and CSI where a capacitor and inductor are used, respectively.

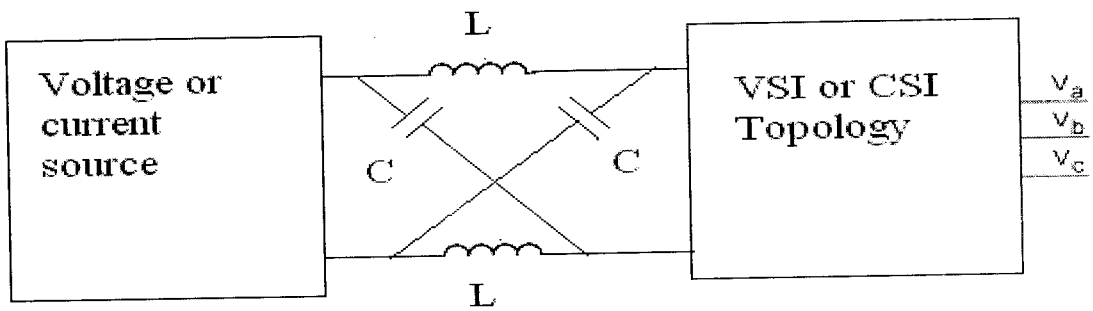


Fig. 2.4 Z-Source Inverter

2.4.1 ADVANTAGES AND COMPARISON OF ZSI WITH TRADITIONAL INVERTERS

The ZSI overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional VSI and CSI provides a novel power conversion concept.

Current Source Inverter	Voltage Source Inverter	Impedance Source Inverter
1. As inductor is used in the d.c link, the source impedance is high; a constant current source is realized.	As capacitor is used in the d.c link, it acts as a low impedance voltage source.	As capacitor and inductor are used in the d.c link, it acts as a constant high impedance voltage source.
2.A current source inverter is capable of withstanding short circuit across any two of its output terminals hence momentary short circuit on load and mis-firing of switches are acceptable.	A VSI leads to more dangerous situation as the parallel capacitor could feed more power in to the fault.	In ZSI mis-firing of the switches may be acceptable.
3. Used in boost operation of the inverter.	Used in buck mode of operation of the inverter.	Used in both buck and boost operating modes of the inverter.
4.Affected by the EMI noise	Affected by the EMI noise	The Less affected by the EMI Noise. Impedance source acts as a filter.
5. Considerable amount of harmonic distortion.	Considerable amount of harmonic distortion.	Harmonic distortion is low.

Table 1 Comparison of ZSI with Traditional Inverters

CHAPTER 3

CHAPTER 3

IMPEDANCE SOURCE INVERTER

3.1 INTRODUCTION OF Z-SOURCE INVERTER

To overcome the problems of the traditional V-source and I-source converters, this project presents an impedance-source (or impedance-fed) power converter (abbreviated as Z-source converter) and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. Fig.3.1 shows the general Z-source converter structure. It employs a unique impedance network (or circuit) to couple the converter main circuit to the power source, load, or another converter, for providing unique features that cannot be observed in the traditional V and I-source converters where a capacitor and inductor are used respectively.

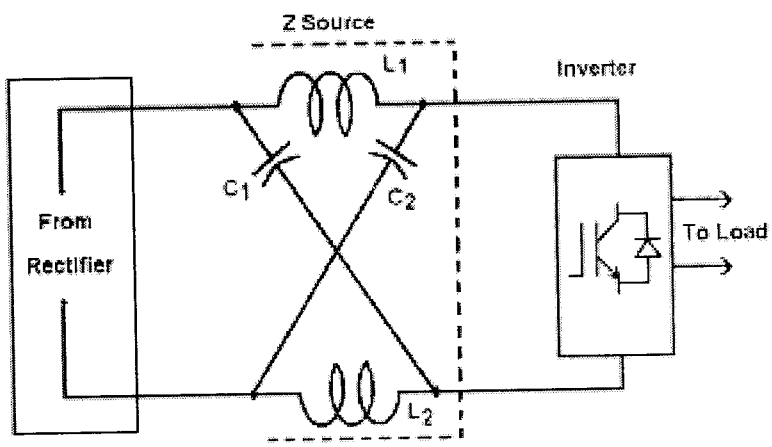


Figure 3.1 General Structure of the Z-source inverter.

The Z-source converter overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional V-source converter and I-source converter and provides a novel power conversion concept. In Fig.3.1, a two-port network that consists of a split inductor L1 and L2 and capacitors C1 and C2 connected in X shape is employed to provide an impedance source (Z-source) coupling the converter (or inverter) to the dc source, load, or another converter. The dc source or load can be either a voltage or a current source or load.

Therefore, the dc source can be a battery, diode rectifier, thyristor converter, fuel cell, an inductor, a capacitor, or a combination of those. Switches used in the converter can be a combination of switching devices and diodes such as the anti-parallel combination as shown in Fig. 3.1. The inductance L1 and L2 can be provided through a split inductor or two separate inductors.

3.2 OPERATING PRINCIPLE OF ZSI

To describe the operating principle and control of the Z source inverter in Fig. 3.2, let us briefly examine the Z-source inverter structure. In Fig. 3.2, the 3-phase Z-source inverter bridge has nine permissible switching states (vectors) unlike the traditional three-phase V-source inverter that has eight.

The traditional three-phase V-source inverter has six active vectors when the dc voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices, respectively. However, the 3-phase Z-source inverter bridge has one extra zero state (or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on), any two phase legs, or all three phase legs.

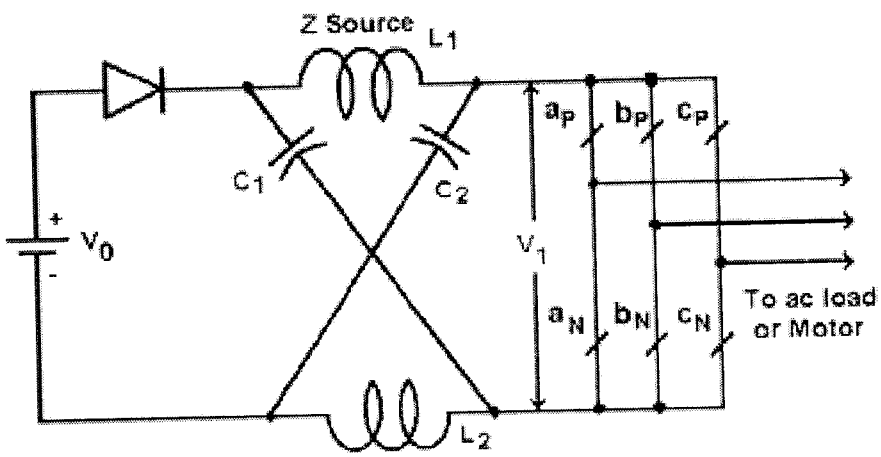


Figure 3.2 Z-source inverter.

This shoot-through zero state (or vector) is forbidden in the traditional V-source inverter, because it would cause a shoot-through. We call this third zero state (vector) the shoot-through zero state (or vector), which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs, and all three phase legs. The Z-source network makes the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter.

3.3 EQUIVALENT CIRCUIT OF ZSI

Fig.6 shows the equivalent circuit of the Z-source inverter shown in Fig 3.3 when viewed from the dc link. When viewed from the Z-source network, the inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state, as shown in Fig. 3.4, whereas the inverter bridge becomes an equivalent current source as shown in Fig 3.5 when in one of the six active states.

Note that the inverter bridge can be also represented by a current source with zero value (i.e., an open circuit) when it is in one of the two traditional zero states. Therefore, Fig. 3.5 shows the equivalent circuit of the Z source inverter viewed from the dc link when the inverter bridge is in one of the eight non shoot-through switching states

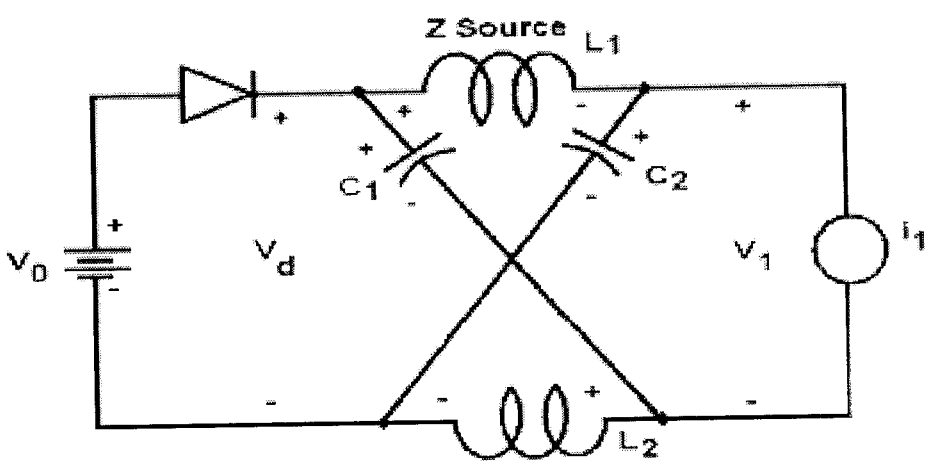


Figure 3.3 Equivalent circuit of the Z-source inverter viewed from the dc link.

In the peak dc-link voltage across the inverter bridge is expressed as

$$V_i = \frac{T}{T_1 - T_0} V_s \qquad 15$$

where

To is the shoot through time period in secs

T1 is the non shoot thro' time period or Active state

T is the Total time period in secs

$$V_i = BV_0 \qquad 16$$

where B is the Boost factor resulting from the shoot through zero state. The dc link voltage Vi is the equivalent dc link voltage of the inverter. On the other side the output peak phase voltage from the inverter can be expressed as

$$V_{ac} = M\frac{V_i}{2} \qquad (17)$$

where M is the Modulation Index.

Vac is the output line voltage of Impedance Source Inverter (ZSI) can be further expressed as

$$V_{ac} = M.B.\frac{V_0}{2} \qquad (18)$$

The output of ZSI mainly depends on the shoot thro' zero states of gating pulses

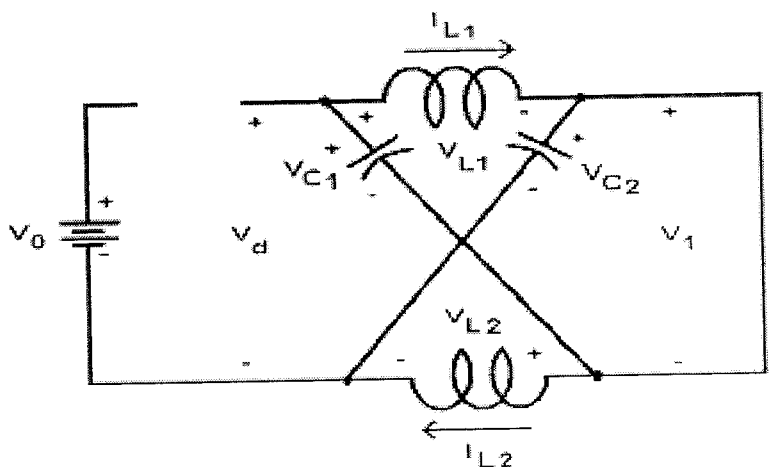


Figure 3.4 Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in the shoot-through zero state.

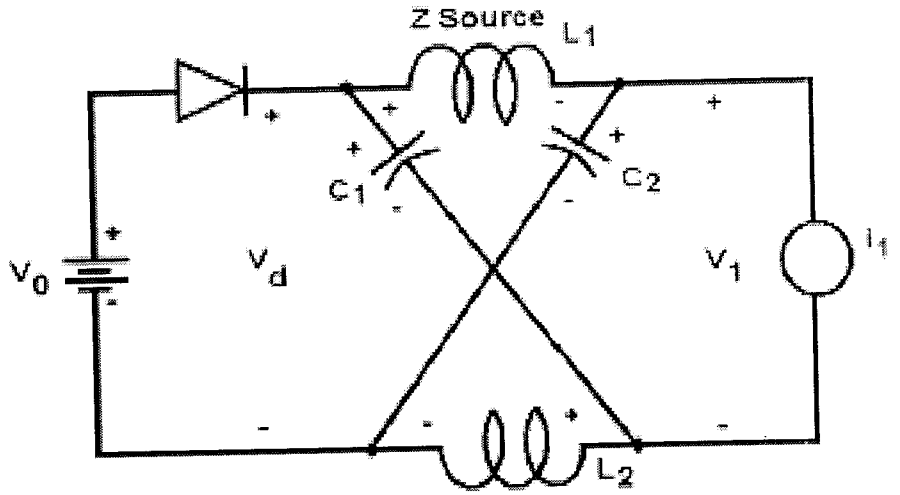


Fig 3.5 Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight non-shoot-through switching states.

3.4 OPERATING STATES OF THE IMPEDANCE NETWORK:

The operating states of the impedance network at the dc link is decided by the switching states of the semiconductor devices on its input and output terminals. As illustrated in Fig.3.6, the diode D_s on its input side has two switching states as 'On' and 'Off' and the VSI on its output side has three switching states as 1, 2& 3.

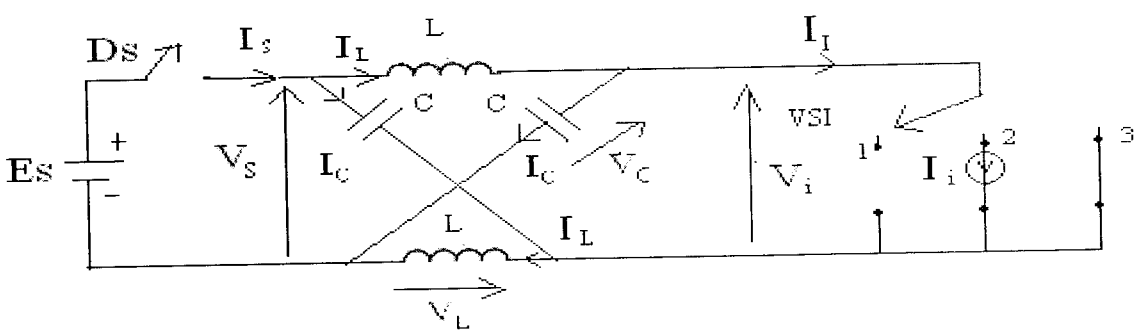


Fig.3.6 Switching equivalent of Z source Inverter

Thus, in general, the impedance network of the ZSI at a given time can operate in any one of the six possible states given in Table 2.

Table 2 Possible operating states of the Impedance Network

VSI Input State	Open		Active		Shoot-Through	
Diode Ds	On	Off	On	Off	On	Off
State of Impedance Network	Open-1	Open-2	Active-1	Active-2	Shoot-Through-1	Shoot-Through-2

A switching cycle of the ZSI may consist of any number of states ranging from two to six. However, as will be seen later in the following sections, the Open-1, Active-1, Shoot-Through-1 states are the desired states in practical applications.

The three states, Open-2, Active-2, Shoot-Through-2 are undesirable and are to be avoided by proper sizing of the inductors and capacitors of the impedance network. The impedance network in general can be written as,

$$V_l = L\left(\frac{dI_l}{dt}\right); \qquad I_c = C\left(\frac{dV_c}{dt}\right)$$

$$V_s = V_c + V_l, \qquad I_s = I_c + I_l \tag{19}$$

$$V_i = V_c - V_l, \qquad I_i = I_l - I_c \tag{20}$$

A. Open -1 state

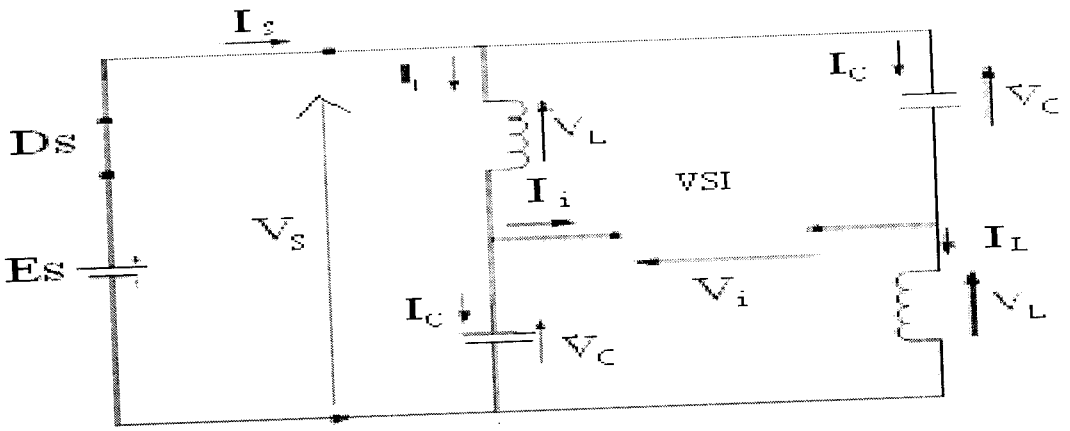


Figure 3.7 Equivalent circuit of ZSI during Open-1 state

The equations that define the open-1 state are given by,

$$V_s=E_s; \quad I_i=0; \tag{21}$$

The inductor voltage and output voltage in this state are given by,

$$V_l= E_s-V_c; \quad V_i= 2V_c-E_s; \tag{22}$$

B. Open-2 state

In the Open-2 state, the diode remains in the Off states and the VSI in the Open state. Therefore, the state defining equations can be written as,

$$I_s=0; \quad I_i=0;$$

In order to avoid this state, the necessary condition for the minimum value of inductor current (I_{lomin}) can be seen as,

$$I_{lomin}>0.$$

C. Active-1 state

As seen in the equivalent circuit given in the Fig.3.8, the only difference between Open-1 state is the presence of the constant current source Io across the input terminals of the VSI.

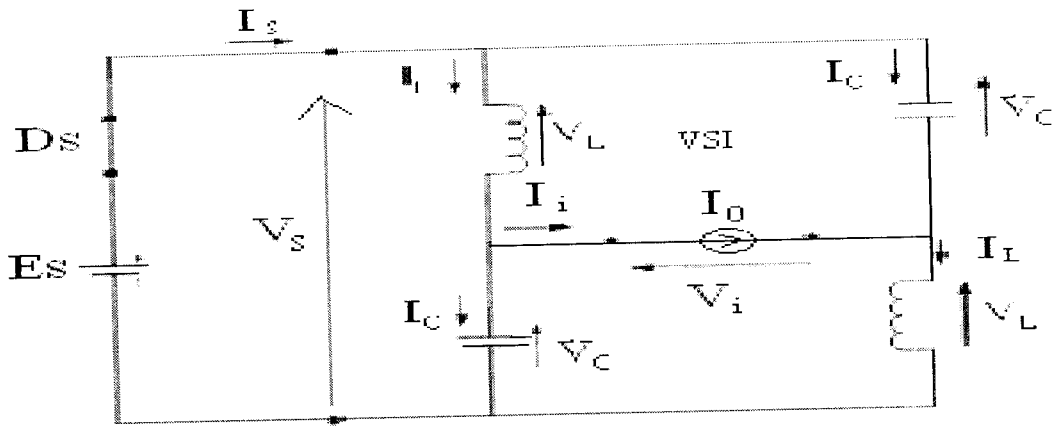


Figure 3.8 Equivalent circuit of ZSI during Active-1 state.

The state defining equations for Active-1 state are,

$$V_s = E_s; \quad I_i = I_o \tag{23}$$

It can be seen that the current through the diode, Is, will be zero and the diode will turn off when,

$$I_l = -I_c = \frac{I_o}{2} \tag{24}$$

This marks the end of Active-1 state and the beginning of Active-2 state.

D. Active-2 state

The state defining equations for Active-2 state are

$$I_i = I_o; \quad I_s = 0 \tag{25}$$

It can be seen that the currents remain constant at $I_l = -I_c = \frac{I_o}{2}$ and the capacitor discharges linearly with time at the rate of $\frac{I_o}{2C}$

In order to avoid Active-2 state in appearing during operation, the necessary condition for minimum inductor current in Active-1 period (I_{lAmin}) is

$$I_{lAmin} > \frac{I_o}{2} \tag{26}$$

E. Shoot-Through-1 state

As seen from Fig. 3.9, the state defining equations for Shoot-Through-1 state are,

$$I_s=0; \quad V_i = 0 \tag{27}$$

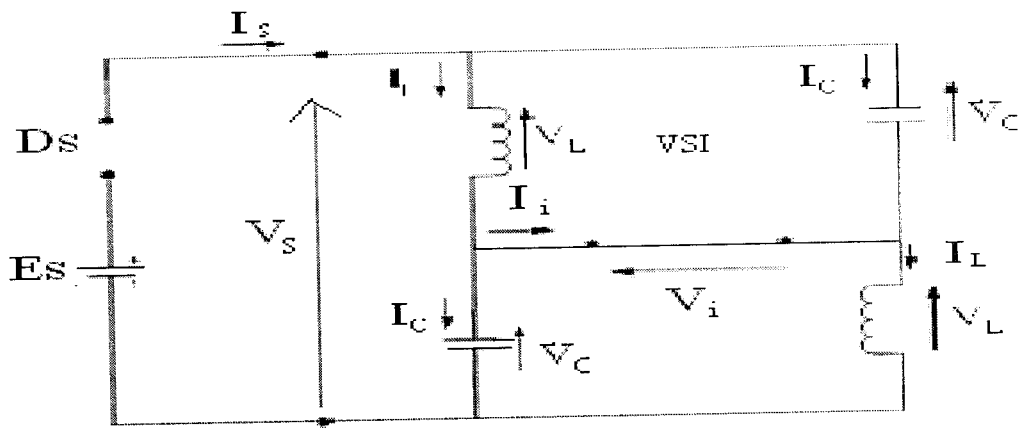


Figure 3.9 Equivalent circuit of ZSI during Shoot-Through-1 state

The energy stored in the capacitors during Open and Active state is transferred to inductors during Shoot-Through-1 state, thereby allowing the boosting of the voltage applied to the VSI.

F. Shoot-Through-2 state

The defining equations of Shoot-Through-2 state can be written as,

$$V_s=E_s; \qquad V_i=0 \tag{28}$$

In order to prevent appearing of Shoot-Through-2 state during operation the necessary condition for minimum capacitor voltage (V_{cmin}) is

$$V_{cmin} > \frac{E_s}{2} \tag{29}$$

From the preceding discussion it is clear that the Open-2, Active-2, Shoot-Through-2 states do not contribute to the power conversion process and should be avoided. Thus they are named as 'static states' .Practical inverters are operated only in two or three of the Open-1, Active-1, Shoot-Through-1 states. They are hereby named as 'dynamic states'.

Since the three static states appear only when the capacitor voltage and inductor current fluctuate in a wide leading to the violation of conditions given in the Open-2, Active-2, Shoot-Through-2 states, it is necessary to limit the ripples of the related voltage and current by increasing the sizes of the inductors and capacitors appropriately.

3.5 SHOOT-THROUGH TIME PERIOD, BOOST FACTOR, MODULATION INDEX:

3.5.1 SHOOT-THROUGH TIME PERIOD:

Shoot-Through time period is defined as the duration at which the two switches of the same-phase leg are gated on at the same time.

3.5.2 BOOST FACTOR:

$$V_i = \frac{T}{T_1 - T_0} V_s \qquad (30)$$

Where,

T0 is the Shoot-Through time period in seconds

T1 is the non Shoot-Through time period or Active state of ZSI

T is the Total time period in sec

V_s is the input source voltage

$V_i = B\ V_o$

Where B is the Boost factor resulting from the Shoot-Through zero state.

3.5.3 MODULATION INDEX:

On the other side the output peak phase voltage from the inverter can be expressed as,

$$V_{ac} = \frac{M.V_i}{2} \qquad (31)$$

Where

M is the Modulation Index.

V_{ac} is the output line voltage of ZSI.

Using equations (30), (31) can be further expressed as,

$$V_{ac} = \frac{M.B.V_o}{2} \tag{32}$$

$$V_{ac} = \frac{B_b.V_o}{2} \tag{33}$$

Where, B_b is the buck boost factor.

CHAPTER 4

CHAPTER 4

DESIGN OF Z-SOURCE INVERTER

4.1 ASSUMPTION:

1. Identical L and C.
2. Dynamic states are alone considered.

4.2 IMPEDANCE NETWORK FOR OPERATING WITH TWO DYNAMIC STATES:

Since Open -1 period is not essential for the conversion process and Open -2 and Active-1 state behave in a similar manner, the Open-1 period is considered as part of the Active-1 period. Thus, ZSI operates only in the Active-1 and Shoot-Through-1 state as depicted in Fig.3.6 since the final value of the variable in one state in the initial value of the same variable in the other state , the boundary conditions can be defined as,

$$V_{ciA} = V_{cfS} \; ; \quad V_{ciS} = V_{cfA} \; ; \tag{34}$$

$$I_{liA} = I_{lfS} \; ; \quad I_{liS} = I_{lfA} \; ; \tag{35}$$

Furthermore, since one switching cycle of VSI has only the Active-1 and Shoot-Through-1 periods,

$$t_A + t_s = T_s \; ; \tag{36}$$

Where T_s is the period of switching cycle of VSI, which is assumed to be known.

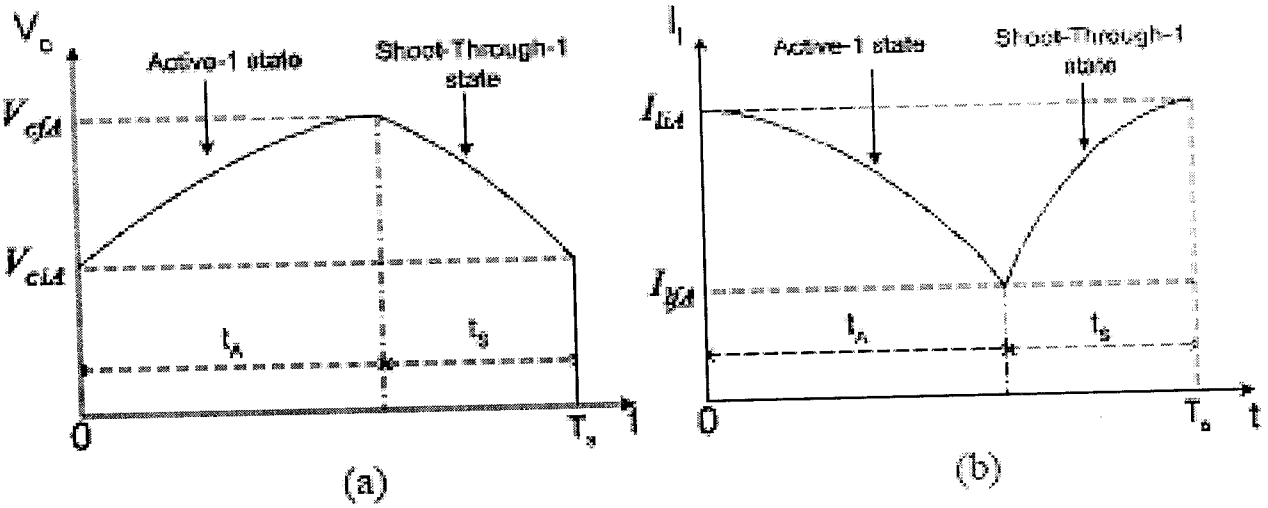


Figure 4.1 Steady state waveforms of (a) Capacitor Voltage (b) Inductor Current for the operation with two dynamic states.

The duty cycle of the shoot-Through state,

$$d_s = \frac{t_s}{T_s};$$

It is not a simple task to accurately design the impedance network even for the simplest case of operation with two dynamic states as it involves many equations. Hence a less accurate, yet a much simpler method is proposed in the next section for the sizing of the impedance network.

4.3 APPROXIMATE DESIGN WITH LINEARISED WAVEFORM:

A ripple in the capacitor voltage in turn appears as a ripple in the dc link voltage applied to the VSI. A large ripple in the dc link voltage degrades the waveform of the ac voltage by giving rise to unexpected harmonics in addition to increasing the voltage rating of VSI. As a consequence, the ripple of the capacitor voltage in practical converters is limited by these concerns and leads to a much smaller ripple than the one allowed. Similarly, the ripple of the inductor current in turn appears as a ripple in the current through the diode and the source.

In order to limit the current rating of the diode and the source, the ripple of the inductor current is constrained to a range which is much smaller ripples allowed by the condition .Due to the small ripples allowed, the changes in the capacitor voltage and the inductor current can be assumed as linear, instead of sinusoidal, for simpler analysis and designing of the ZSI.

Fig.4.2 illustrates the waveform of the capacitor voltage and inductor current under this condition. The average values of V_c and I_l respectively and the peak values of their ripples are given as ΔV_c and ΔI_l respectively.

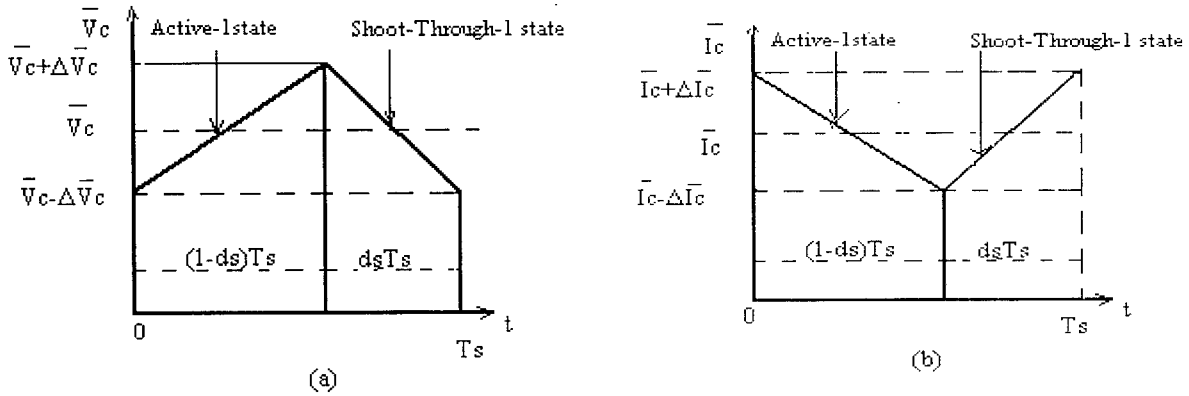


Fig.4.2 Linearised waveforms of (a) Capacitor Voltage (b) Inductor Current for small ripples.

With linear variations of waveform, from fig (4.2), the peak ripples ΔV_c and ΔI_l can be expressed as,

$$\Delta V_c = \frac{\bar{I}_c \Delta t}{C};$$
$$\Delta I_l = \frac{\bar{V}_l \Delta t}{C}; \qquad (37)$$

Considering the Shoot-Through-1 period,

$$C = \frac{I_c d_s T}{2\Delta V_c};$$
$$L = \frac{V_c d_s T}{2\Delta I_c}; \qquad (38)$$

Since the average inductor voltage and average capacitor current over a complete switching cycle in steady-state are zero,

$$\frac{\overline{V_c}}{E_s} = \frac{\overline{I_l}}{I_0} = \lambda; \tag{39}$$

By expressing the ratio of peak ripples to their average values as k, where k<<1 for linear waveforms,(38) and(39) can be combined as,

$$C = \frac{I_0 d_s T_s}{2kE_s};$$
$$L = \frac{E_s d_s T_s}{2kI_0}; \tag{40}$$

Thus, if the source voltage, load current, switching period and duty ratio of Shoot-Through state are known, C and L for any control strategy can be calculated from (40) to result in a desired level of ripples.

Furthermore, for simple –boost control, the average voltage applied to the VSI during active state, as given by,

$$\overline{V}_{iA} = 2\overline{V}_c - E_s = \frac{2V_m}{(1-d_s)}; \tag{41}$$

Substituting for $\overline{V}_c$ in (39) from (41), it can be simplified as,

$$\lambda = \frac{2V_m}{E_s};$$

$$d_s = \frac{(2V_m - E_s)}{(4V_m - E_s)}; \tag{42}$$

With the substitution of λ and ds from (43) in (40) and (41) respectively, it can be found that

$$\overline{V}_c = 2V_m;$$
$$I = \frac{2V_m I_0}{Es}; \qquad (43)$$

$$C = \frac{I_0 T_s(2V_m - E_s)}{2kE_s(4V_m - E_s)}; \qquad (44)$$
$$L = \frac{E_s T_s(2V_m - E_s)}{2kI_0(4V_m - E_s)};$$

4.4 CALCULATION PROCEDURE:

The design process based on approximate method is shown below:

Let a 3-phase,50Hz,400V(line-line),25A,Y-connected resistive load be supplied by a ZSI operating at 10kHz under simple- boost control with a constant input dc source voltage of 200V.

For this case, the circuit parameters required for the design procedure can be calculated as, T_s=10^-4 ;E_s=200V;V_m=√2.400/√3=326.6V.From (27),it can be found that λ=3.266,ds=0.41 and M=0.59.Using (28),it can be determined that $\overline{V}_c = 653.2$ and then from (26),the equivalent dc link voltage can be found as, $\overline{V}_{iA}$ =1106.4V.The input current of VSI due to the load can be determined by considering power balance as , Io=3VmIm/(2 $\overline{V}_{iA}$ (1-ds))=26.53Awhere I_m is the peak phase current of the load . The average inductor can then be found from (24) asI_l=86.66A.The capacitor and inductor values are given by (24) or (29) as C=2.72kμF and L=0.154/kmH where factor k is chosen to limit the ripples of capacitor voltage and inductor current .For the ripples to be 5% of their average values, k=0.05 and then C=54.4μF and L=3.09mH.

CHAPTER 5

CHAPTER 5

SIMULATION OF WIND ENERGY CONVERSION SYSTEM WITH ZSI.

5.1 MATLAB

MATLAB is a high-performance language for technical computing. It Integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. In this project the modeling and simulation of the proposed controller is done in matlab using simulink and power system block set tool boxes. Typical uses include

1. Math and computation
2. Algorithm development
3. Data acquisition Modeling, simulation, and prototyping
4. Data analysis, exploration, and visualization
5. Scientific and engineering graphics
6. Application development, including graphical user interface building

5.1.1 SIMULINK

Simulink is a software package for modeling, simulating, and analyzing non linear dynamical systems. It is a graphical mouse-driven program that allows somebody to model a system by drawing a block diagram on the screen and manipulating it dynamically.

5.1.2 POWER SYSTEM BLOCK SET

The Power System Block set allows scientists and engineers to build models that simulate power systems. The block set uses the Simulink environment, allowing a model to be built using click and drag procedures. Not only can the circuit topology be drawn rapidly, but also the analysis of the circuit can include its interactions with mechanical, thermal, control, and other disciplines.

5.2 BLOCKS USED FOR SIMULATION

The blocks used for simulation are

5.2.1 PERMANENT MAGNET SYNCHRONOUS GENERATOR

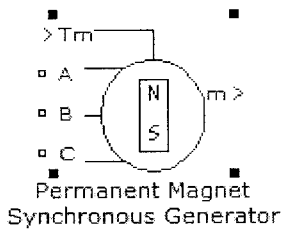


Figure 5.1 Simulation Block of PMSG

Permanent magnet generators are preferred over induction generators, in view of this improved efficiency. The Permanent Magnet Synchronous Machine block operates in either generator or motor mode. The mode of operation is dictated by the sign of the mechanical torque (positive for motor mode, negative for generator mode). The electrical and mechanical parts of the machine are each represented by a second-order state-space model. The sinusoidal model assumes that the flux established by the permanent magnets in the stator is sinusoidal, which implies that the electromotive forces are sinusoidal.

5.2.2 UNIVERSAL BRIDGE

The Universal Bridge block implements a universal three-phase power converter that consists of up to six power switches connected in a bridge configuration. The types of power switch and converter configuration are selectable from the dialog box.

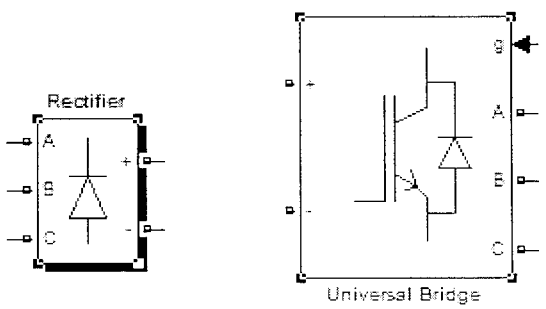
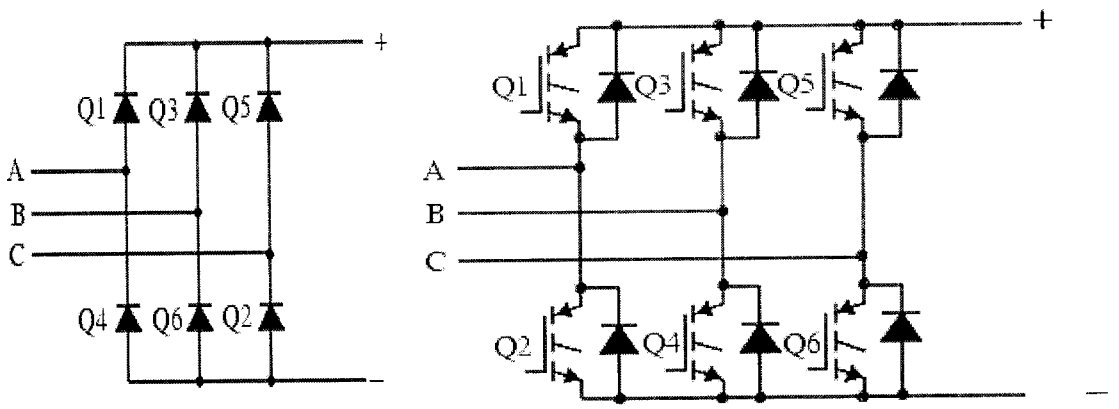


Figure 5.2 Simulation Block of Universal Bridge used in Diode Rectifier and IGBT Inverter



Diode Rectifier and IGBT Inverter

The Universal Bridge block allows simulation of converters using either naturally commutated (or line-commutated) power electronic devices (diodes or thyristors) and forced-commutated devices (GTO, IGBT, MOSFET). The Universal Bridge block is the basic block for building two-level voltage-sourced converters (VSC).

5.2.3 PULSE GENERATOR (PWM GENERATOR)

Generate pulses for a carrier-based two-level pulse width modulator (PWM) in Converter Bridge

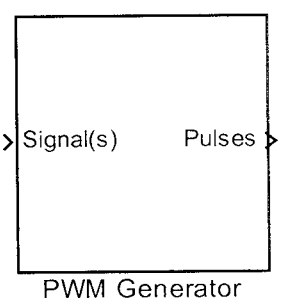


Figure 5.3 Simulation Block of PWM Generator

The PWM Generator block generates pulses for carrier-based pulse width modulation (PWM) converters using two-level topology. The block can be used to fire the forced-commutated devices (FETs, GTOs, or IGBTs) of single-phase, two-phase, three-phase, two-level bridges or a combination of two three-phase bridges.

The number of pulses generated by the PWM Generator block is determined by the number of bridge arms you have to control:

- Six pulses are generated for a three-arm bridge. Pulses 1, 3, and 5 fire the upper devices of the first, second, and third arms. Pulses 2, 4, and 6 fire the lower devices.

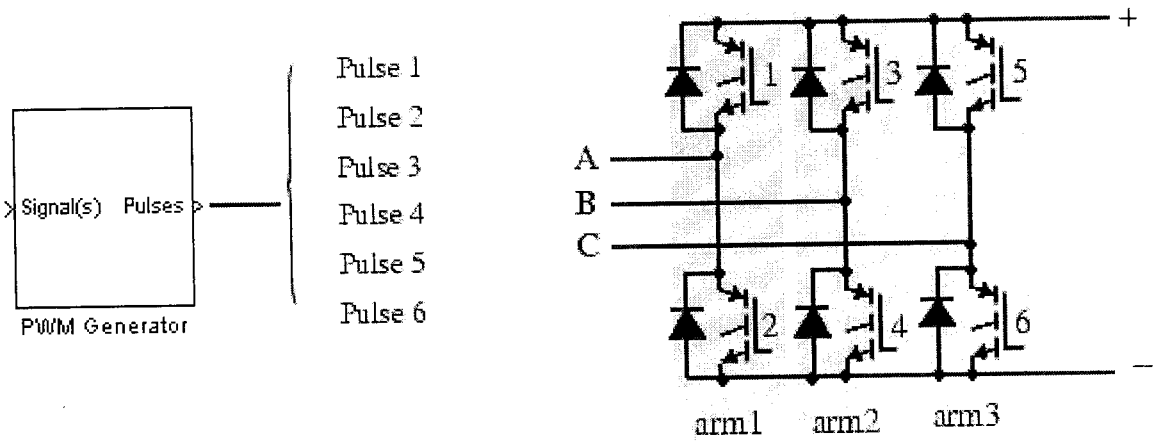


Figure 5.4 PWM Generator with Six Pulses

For each arm the pulses are generated by comparing a triangular carrier waveform to a reference modulating signal. The modulating signals can be generated by the PWM generator itself, or they can be a vector of external signals connected at the input of the block. One reference signal is needed to generate the pulses for a single- or a two-arm bridge, and three reference signals are needed to generate the pulses for a three-phase, single or double bridge.

The amplitude (modulation), phase, and frequency of the reference signals are set to control the output voltage (on the AC terminals) of the bridge connected to the PWM Generator block.

5.2.4 THREE PHASE LOAD

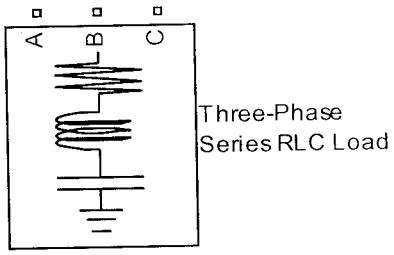


Figure 5.5 Simulation Block of Three Phase Load

The Three-Phase Series RLC Load block implements a three-phase balanced load as a series combination of RLC elements. At the specified frequency, the load exhibits constant impedance. The active and reactive powers absorbed by the load are proportional to the square of the applied voltage.

SPECIFICATIONS

Sl.No	Source/Elements	Parameter specification
1	PMSG	Preset model- 0.8 Nm 300 Vdc 3000 RPM -0.8 Nm
2	Rectifier (Universal Bridge)	Ron(Ohm) = 1e-3 Ohm Inductance Lon (H) = 0 H Snubber resistance Rs (Ohms) = 1e5 Ohm Snubber capacitance Cs (F) = inf
3	IGBT	Snubber resistance Rs (Ohms) = 5e6 Ohm Snubber capacitance Cs (F) = inf Internal Resistance Ron (Ohms) = 5e-3
4	Inductance (L1&L2)	Inductance (H) = 7e-3 H
5	Capacitance (C1&C2)	Capacitance (F) = 120e-6 F

Table.3. Specifications

5.3 SIMULATION MODEL OF WIND ENERGY CONVERSION SYSTEM WITH ZSI

The proposed wind energy conversion system with ZSI is modeled in MATLAB/SIMULINK as shown in Fig.5.6.

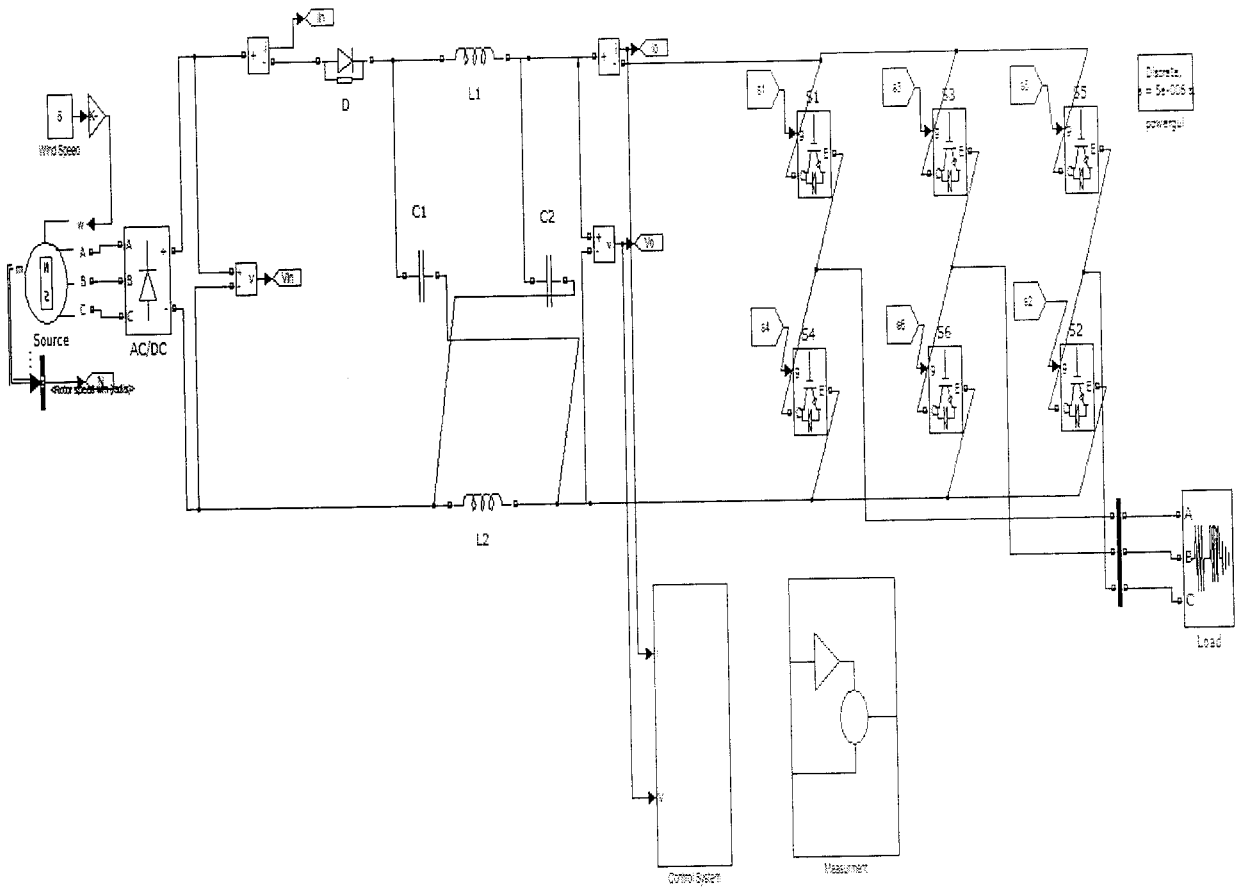


Figure 5.6 Simulation model of wind energy conversion system with ZSI.

5.3.1 IMPEDANCE SOURCE INVERTER CONTROL CIRCUIT

The control circuit for the Impedance Source Inverter is shown in the figure 5.7. The control circuit consists of PWM generator. The PWM generator is used to generate the six PWM signals and these signals are used to trigger the six switches used in the Z-Source inverter and thus the output voltage is maintained constant by controlling these triggering pulses.

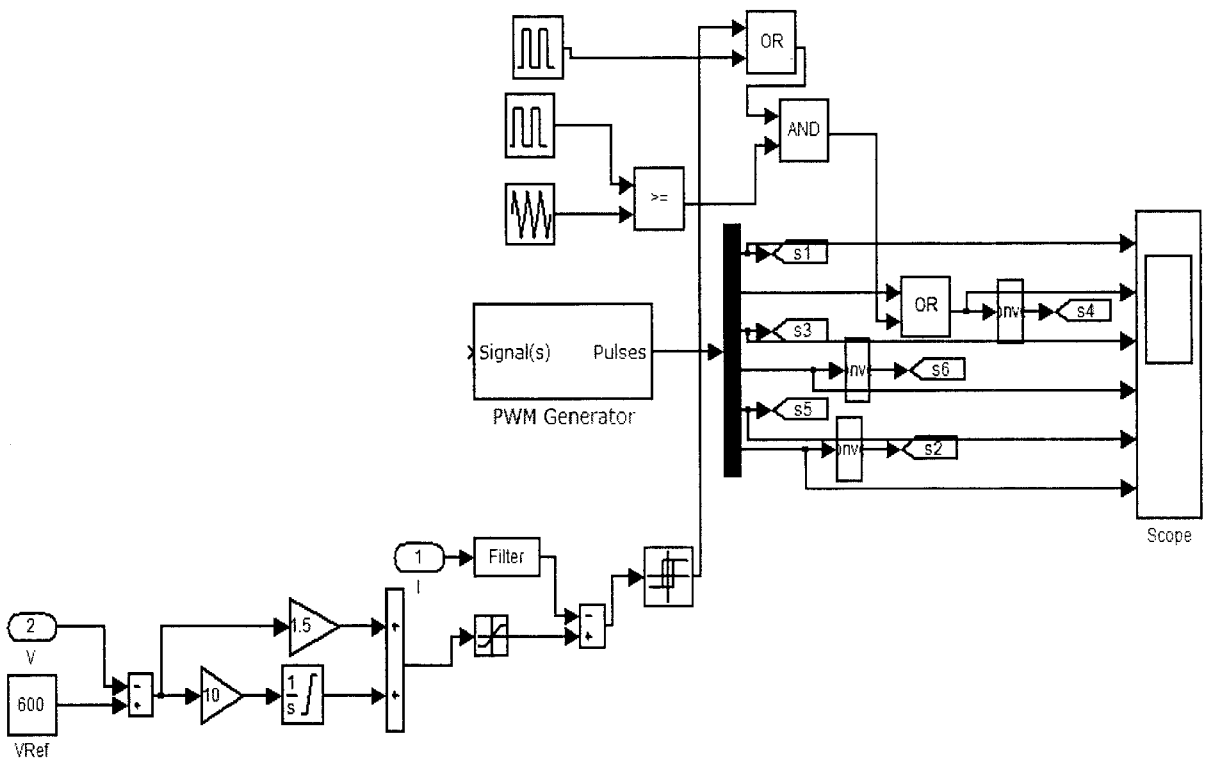


Figure 5.7 Control circuit for ZSI

5.4 SIMULATION RESULTS

5.4.1 RECTIFIER OUTPUT VOLTAGE

For getting desired voltage the PMSG generated voltage is given to power converters. The diode rectifier is used here to rectify the generated voltage.

Rectifier output voltage for wind speed 8 m/s

Figure 5.8 shows the rectifier output voltage for wind speed 8 m/s. The rectifier output voltage is 286 V for wind speed 8 m/s.

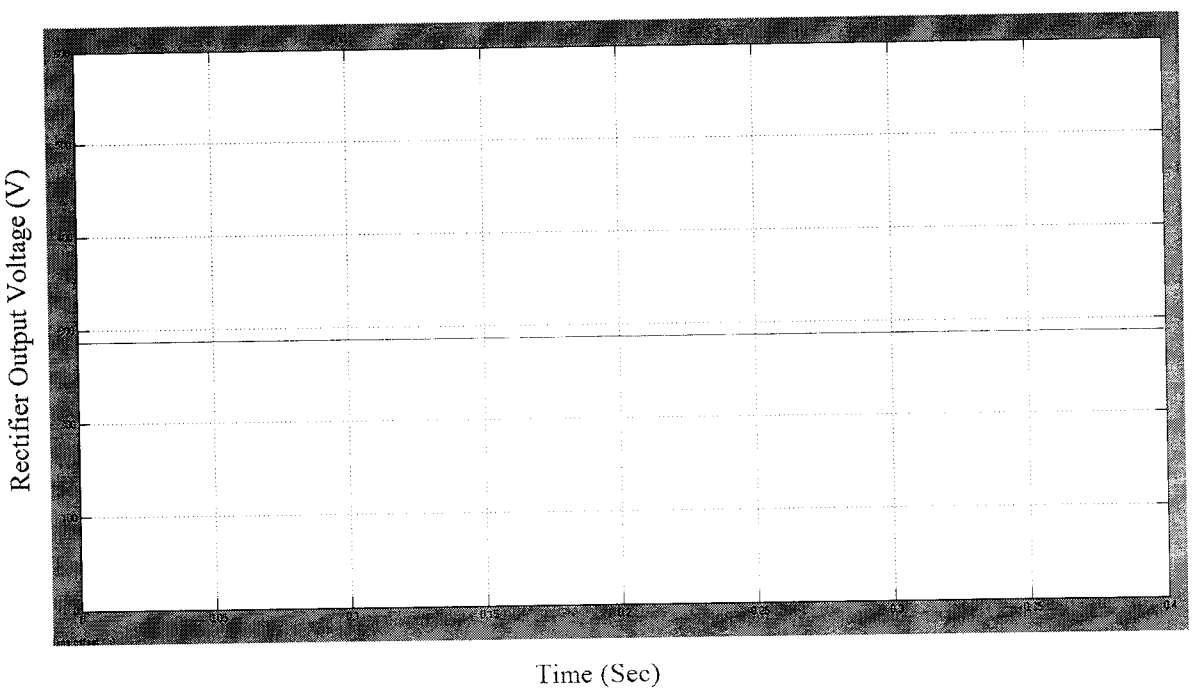


Figure 5.8 Rectifier Output Voltage for wind speed 8 m/s

Rectifier output voltage for wind speed 13 m/s

Figure 5.9 shows the rectifier output voltage for wind speed 13 m/s. The rectifier output voltage is 343 V for wind speed 8 m/s.

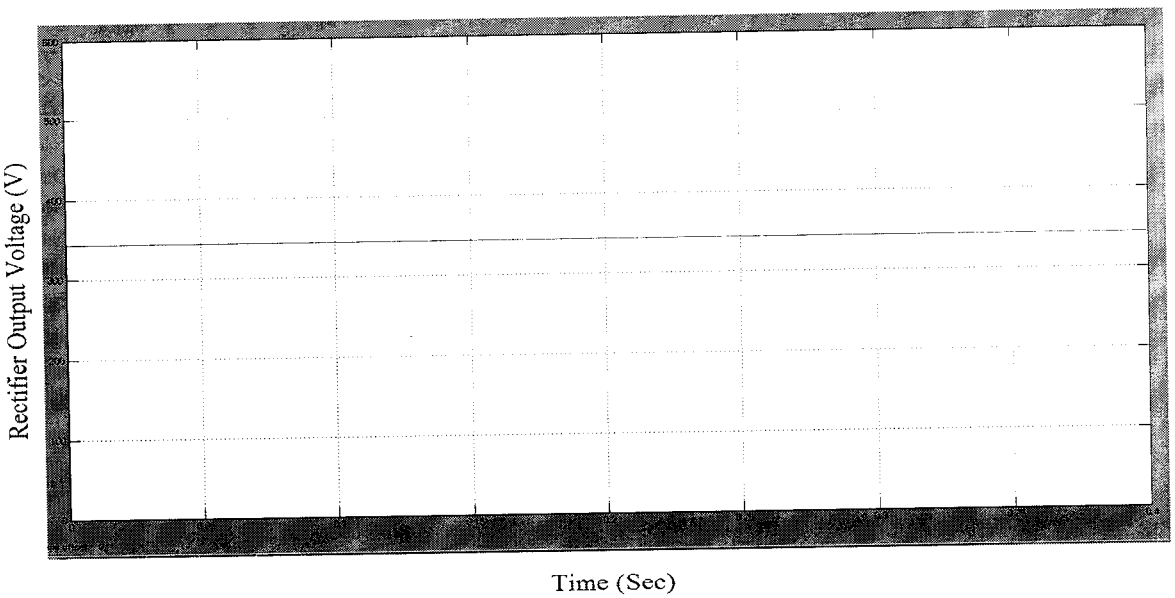


Figure 5.9 Rectifier Output Voltage for wind speed 13 m/s

Rectifier output voltage for wind speed 8 m/s

Figure 5.10 shows the rectifier output voltage for wind speed 8 m/s. The rectifier output voltage is 400 V for wind speed15 m/s.

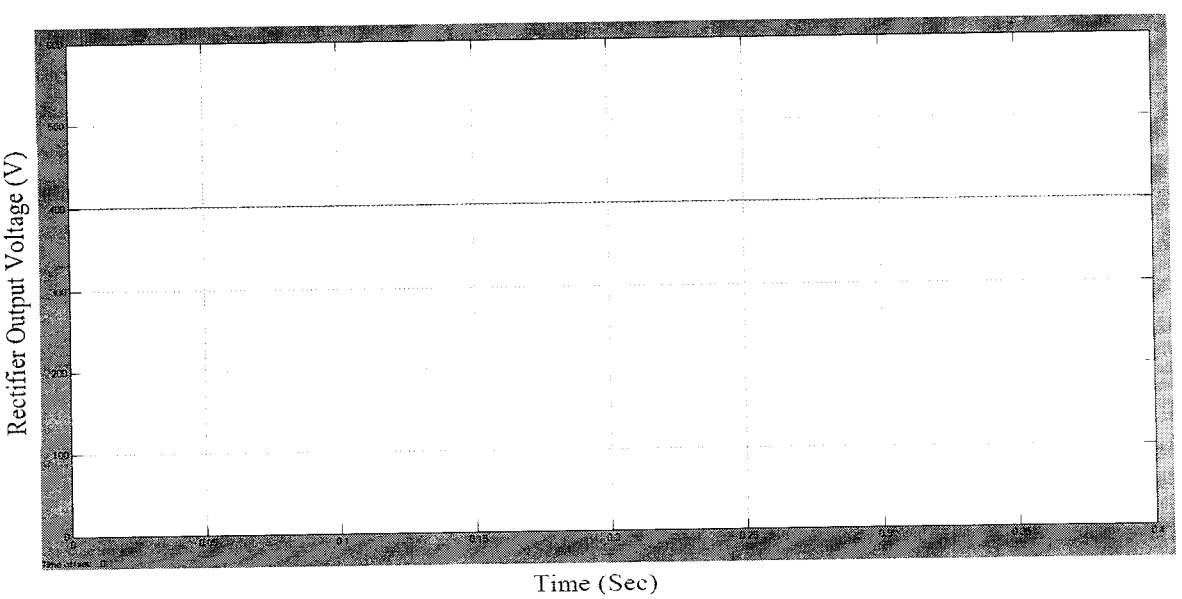


Figure 5.10 Rectifier Output Voltage for wind speed 15 m/s

5.4.2 ZSI OUTPUT VOLTAGE

The rectified voltage is given to ZSI for getting the desired voltage. During shoot thro' zero states of the gating pulse, the two inductors induce high voltages which appear across the two capacitors. During active state, the capacitors provide the stiff voltage across the inverter circuit. The Z-Source inverter output voltage is shown in the figure 5.11. The output shows that the peak to peak voltage is maintained constant at 415 V for various wind speed.

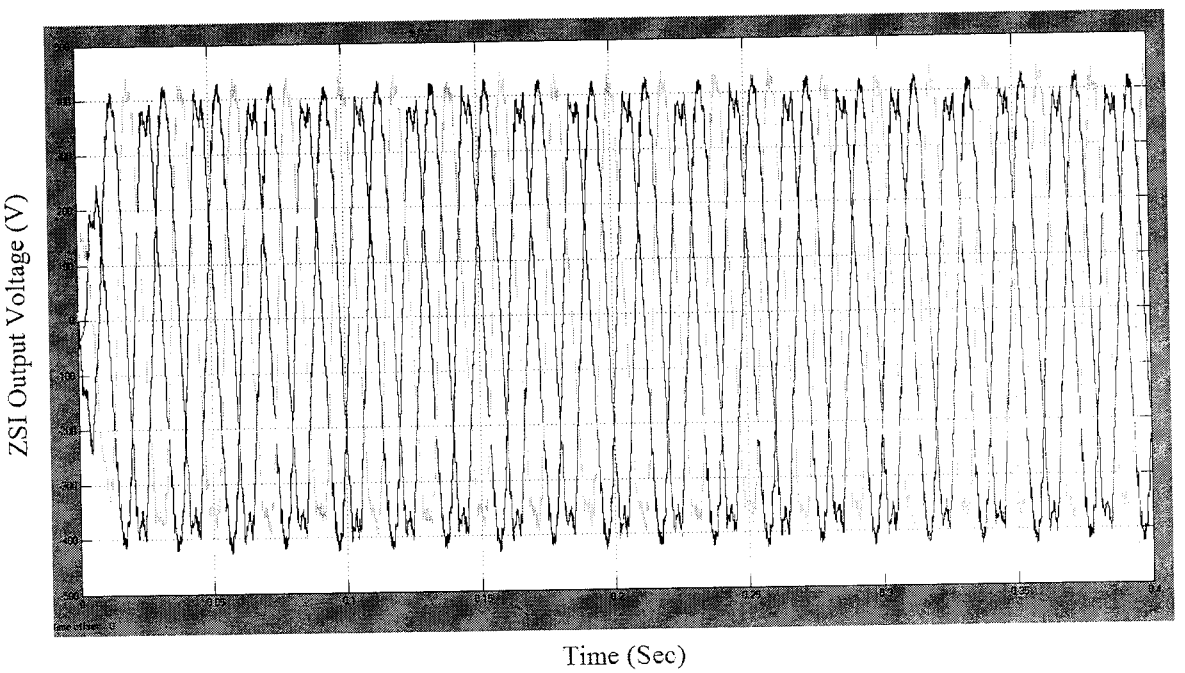


Figure 5.11 ZSI Output Voltage for various wind speed

CHAPTER 6

CHAPTER 6

HARDWARE IMPLEMENTATION OF WECS WITH ZSI

6.1 BLOCK DIAGRAM

This chapter explains the block diagram and components used for the hardware prototype of the proposed system. It includes the photographs of the fabricated model. It consists of DC Source, Impedance Network, Inverter and PIC16F877A Microcontroller. Figure 6.1 shows the hardware block diagram.

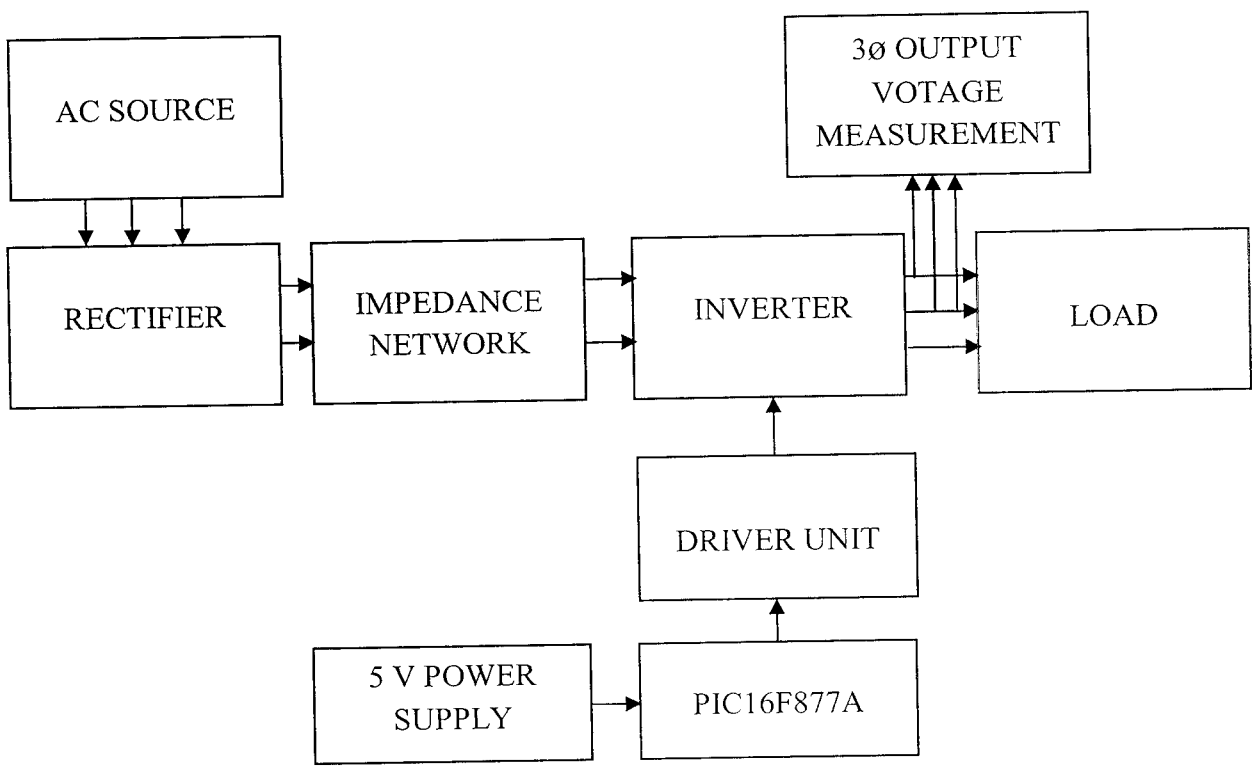


Fig 6.1 Hardware Block Diagram

The gate pulse for the inverter switches are generated by PIC16F877A controller. This micro controller circuit works in 5V power supply. So separate step down rectifier unit is made for the controller. This controller is isolated from the main circuits by means of Opto-coupler.

6.2 IMPEDANCE SOURCE INVERTER CIRCUIT DIAGRAM

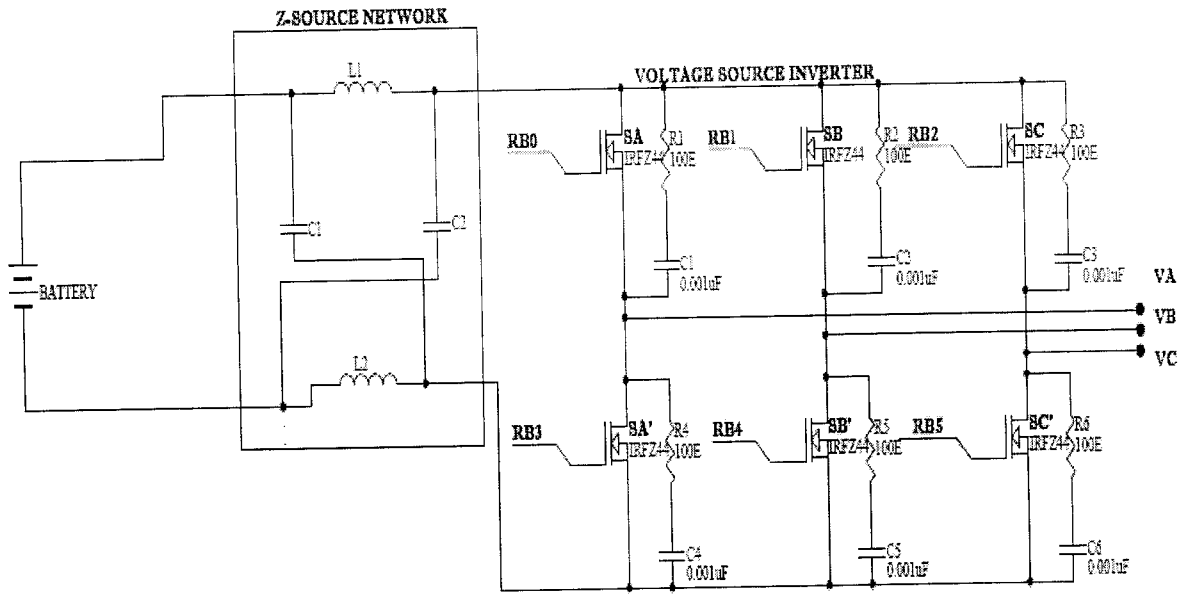


Figure 6.2 Hardware Circuit for Z-Source Inverter

6.2.1 IMPEDANCE SOURCE

In traditional inverters either a capacitor or an inductor is involved in the dc link. In voltage source inverters a capacitor is used where as in the current source inverters an inductor is used. But in this Impedance source inverter both the capacitor and an inductor is involved so that the rectifier output can be boosted as well as bucked as per the requirement. Here the capacitor and the inductor is connected in a manner so as the bridge looks like X. This bridge boosts the rectifier output so that the output of the inverter bridge is maintained as per the requirement.

6.2.2 INVERTER BRIDGE

The circuit involves a three phase inverter which consists of six MOSFETs as switching devices. They are named as SA, SB, SC, SA', SB', SC'. The snubber circuit has resistors and capacitors for protecting the bridge from over voltages and over current.

6.3 PIC MICROCONTROLLER

16F877A PIC Microcontroller is used for controlling the width of the pulses from PWM generator, by fixing either the frequency or voltage so that the MOSFETs are turned ON and OFF in the desired sequence

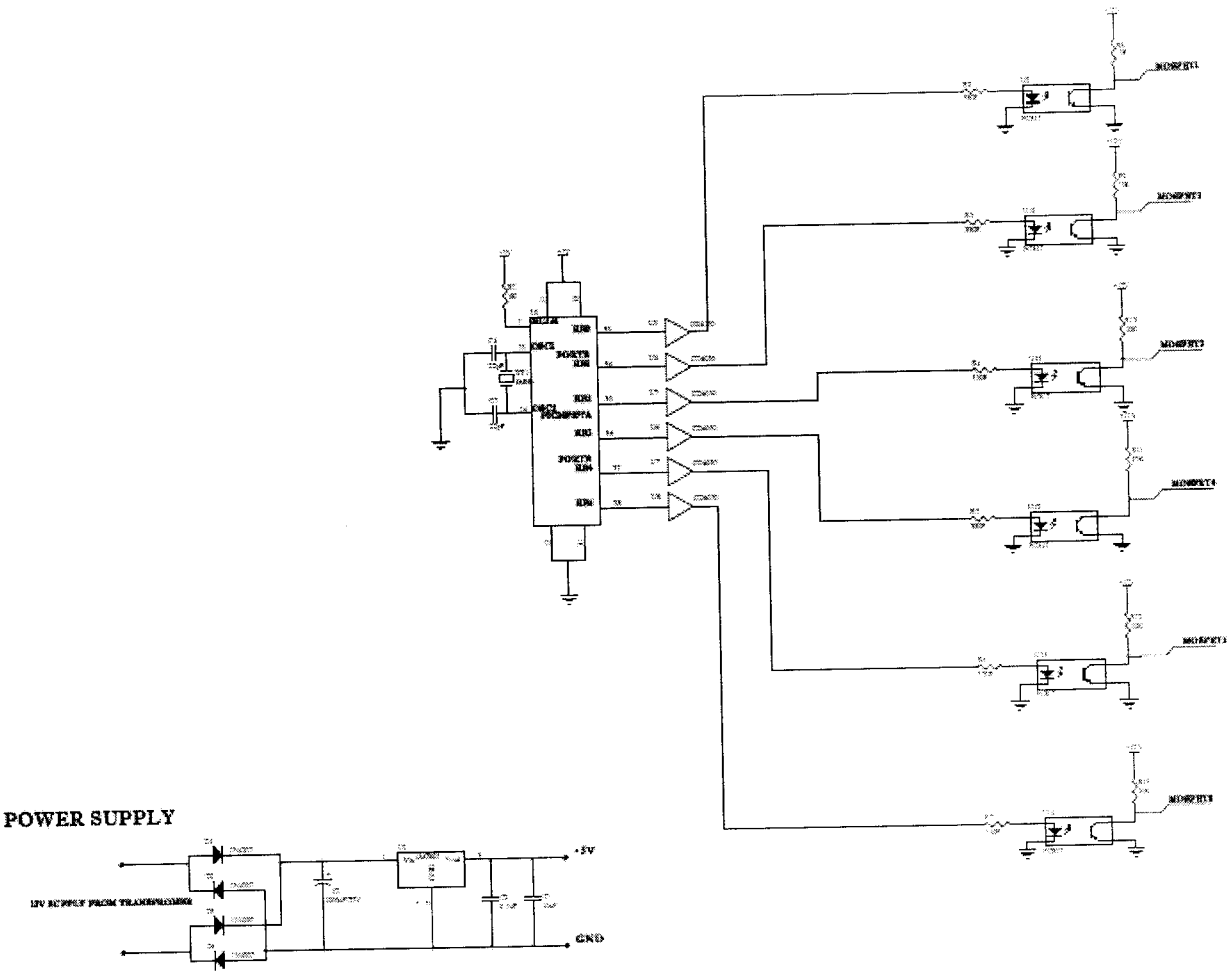
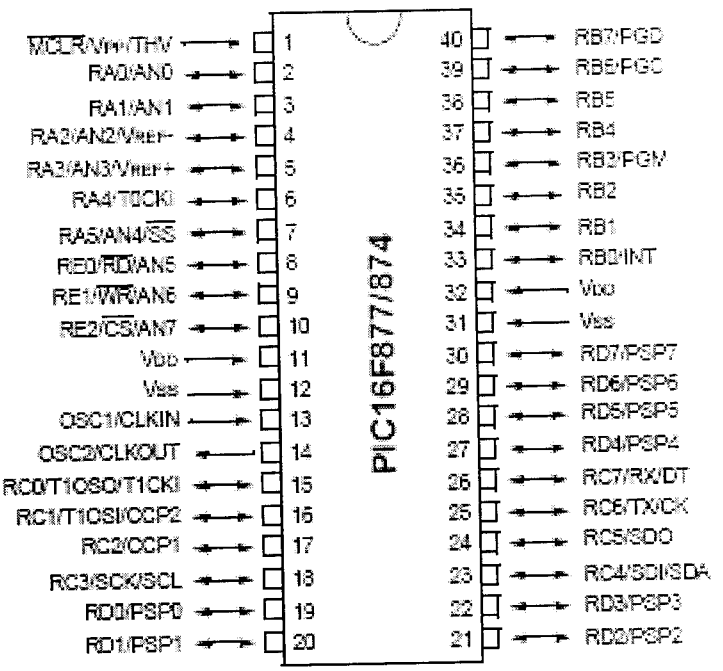


Figure 6.3 PIC 16F877A based control circuit for ZSI

Figure 6.3 shows the complete triggering circuit for the three phase impedance source inverter. The outputs G1, G2, G3, G4, G5 and G6 are the gate pulses applied to the MOSFET switches. The sequence of switching is controlled by the microcontroller.

6.3.1 PIN CONFIGURATION OF PIC16F877A



Pin Configuration of PIC16F877A

6.3.2 THE NEED FOR MICRO CONTROLLER BASED PWM GENERATION

- Micro controller has inbuilt functions such as timer, ADC, PWM, oscillator which reduce the hardware components used.
- PWM technique used enables the reduction of harmonics
- Wide variation in speed since frequency is used as control parameter.
- Digital circuits used employ a faster response.
- Automatic speed control is achieved since no manual parts all involved.

- The Micro controller IC Chip senses the input speed requirement and gives the output in favor of the input.
- No external commutation circuits are required.

6.3.3 CORE FEATURES

- High-performance RISC CPU
- Only 35 single word instructions to learn
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

- Up to 8K x 14 words of Flash Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM data memory
- Interrupt capability (up to 14 internal/external
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Low-power consumption:
  < 2 mA typical @ 5V, 4 MHz
  20mA typical @ 3V, 32 kHz
  < 1mA typical standby current

6.3.4 MEMORY ORGANIZATION

The organization of memory in PIC 16F877 is shown in the following table.

Table-4 Memory of PIC16F877

DEVICE	PROGRAM FLASH	DATA MEMORY	DATA EEPROM
PIC 16F877	8K	368 Bytes	256 Bytes

PROGRAM MEMORY ORGANIZATION

The PIC16f877 devices have a 13-bit program counter capable of addressing 8K *14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

6.3.5 DATA MEMORY ORGANIZATION

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the special functions Registers. Bits RP1 (STATUS<6) and RP0 (STATYUS<5>) are the bank selected bits.

Table 5 Bank Selection

RP1:RP0	Banks
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (1238 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM.

All implemented banks contain special function registers. Some frequently used special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

6.3.6 PERIPHERAL FEATURES

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescalar
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules

  Capture is 16-bit, max resolution is 12.5 ns,

  Compare is 16-bit, max resolution is 200 ns,

  PWM max. resolution is 10-bit

- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- USART/SCI with 9-bit address detection.
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls

These are all some of the important features of the peripherals available in PIC16F77A Microcontroller.

6.4 HARDWARE TESTING AND RESULTS

The fabricated hardware model is shown in figure.6.4. The output voltage waveform of the proposed inverter system with voltage is shown in figure 6.5. The four main parts of the proposed system

(i) Supply unit

(ii) Impedance Network

(iii) Inverter circuit

(iv) Controller

Figure 6.4 Hardware photograph

6.4.1 ZSI OUTPUT VOLTAGE

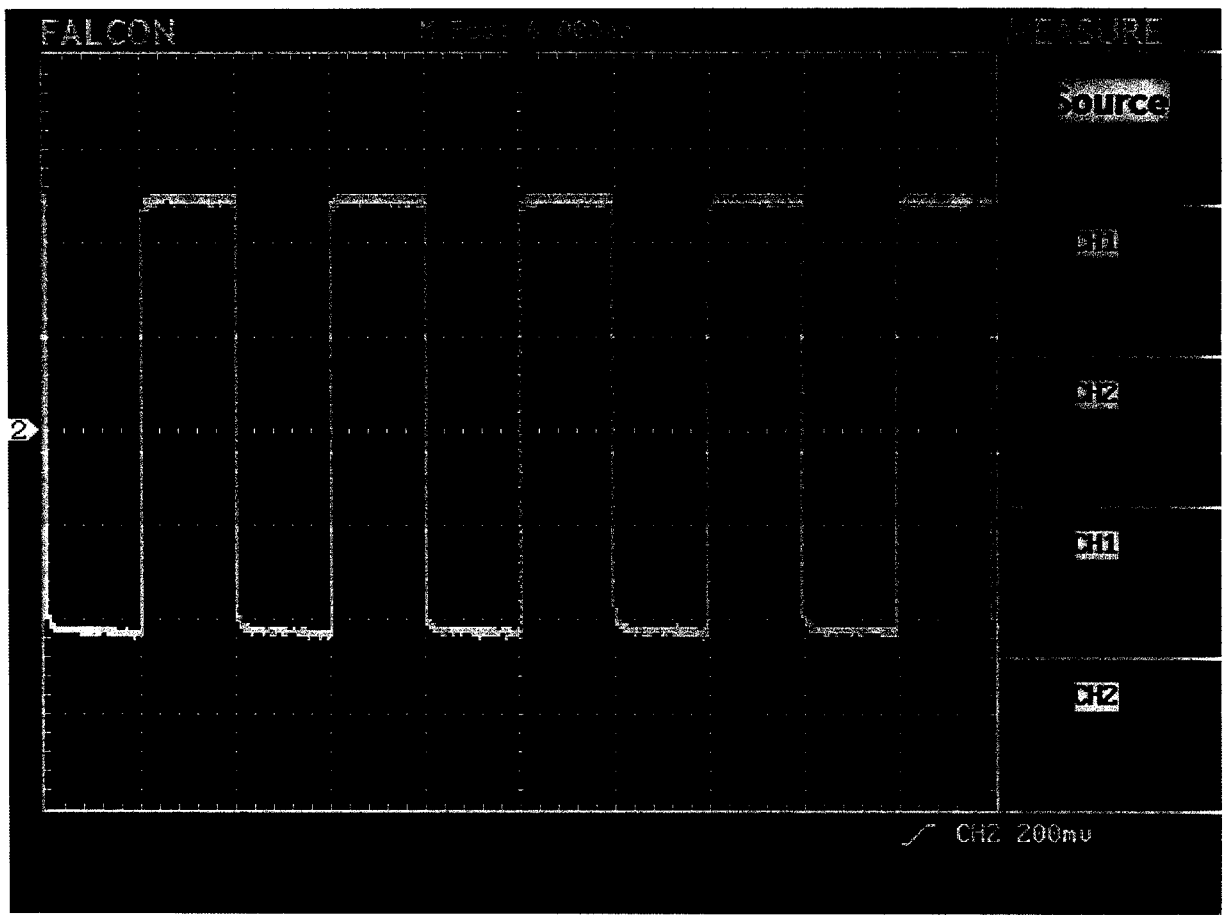


Fig 6.5 ZSI Output Voltage

CHAPTER 7

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

An Impedance source inverter for wind energy conversion system has been proposed and corresponding simulated waveforms are verified. The Impedance source inverter is specially suited for above applications. With unique features like single stage power conversion and improved reliability, the Impedance source technology can be applied to the entire spectrum of power conversion. The output voltage of the ZSI entirely depends on the shoot thro' states. If we increase the shoot thro' time period we can get any desired voltage. The shoot thro' time is varied according to wind velocity.

7.2 FUTURE SCOPE

In the future scope of the work, the characteristics of Impedance Source Inverter is used for Maximum Power Tracking control and delivering power to grid. To obtain the maximum power output at different generator speeds for different wind velocity.

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[2] F. Z. Peng, "Z-Source inverter," *IEEE Trans. Ind. Applicat.*, vol. 39, pp.504-510, Mar. /Apr. 2003.

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[4] ShigeoMorimoto,Hideaki Nakayama, Masayuki Sanada, Yoji Takeda:"Sensorless Output Maximization Control for Variable- Speed Wind Generation System using IPMSG", *IEEE Transactions on Industrial Applications* 2003,pp. 1464-1471.

[5] Tomonobu Senjyu, Sathoshi Tamaki, Naomitusu Urasaki, Katsumi Uezato Toshihisa Funabashi, Hideki Fujita "Wind Velocity and Position Sensorless Operation for PMSG Wing Generator", *Proceedings of IEEE Power Electronics Conference*. pp787-791, 2006.

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[7] A.B. Raju, K.Chatterjee and B.G. Femandes, "A Simple Power Point Tracker for Grid connected Variable Speed Wind Energy Conversion System with reduced Switch Count Power Converters", *IEEE conference on Power Electronic specillists*,2003. pp 456-462.

APPENDIX I

PROGRAM CODING

```
#include<pic.h>
unsigned int S;
//__CONFIG(0x1F71);
__CONFIG(0x20A4);
__CONFIG(0x3FFF);
void main()
{
        ADCON1=0x8E;
        ANSEL=0;
        ANSELH=0;
        PR2=99;
        CCPR1L=50;
        CCP1CON=0X0C;
        T2CON=0X04;
        TRISD=0XFF;
        TRISC=0X80;
        TRISB=0;
        TRISA=0x0F;
        PORTC=0;
        PORTB=0;
        OPTION=0x87;
        TMR0=0;

//      GIE=PEIE=INTE=T0IE=TMR1IE=1;
//      T1CON =0x01;
//      TMR1L = 0x00;
//      TMR1H = 0x00;

 while(1)
```

```
        {
                        PORTB=0x09;
                        while(TMR0<4);
                        PORTB=0x29;
                        while(TMR0<22);
                        PORTB=0x21;
                        while(TMR0<26);
                        PORTB=0x24;
                        while(TMR0<30);
                        PORTB=0x26;
                        while(TMR0<48);
                        PORTB=0x06;
                        while(TMR0<52);
                        PORTB=0x12;
                        while(TMR0<56);
                        PORTB=0x1A;
                        while(TMR0<74);
                        PORTB=0x19;
                        while(TMR0<78);
                        TMR0=0;
        }
        while(1);
}
delay_adc()
{
        unsigned int i;
        for(i=0;i<400;i++);
}


//                      ADCON0=0X81;
```

```
//                  delay_adc();
//                  ADGO=1;
//                  while(ADGO);        //status check
//                  S=ADRESH*256+ADRESL;  //right
//                  if(S>820)
//                  {
//                          CCPR1L++;
//                          if(CCPR1L>70)
//                                  CCPR1L=70;
//                  }
//                  else if(S<800)
//                  {
//                          CCPR1L--;
//                          if(CCPR1L<30)
//                                  CCPR1L=30;
//                  }
```

APPENDIX II

IRF840B/IRFS840B

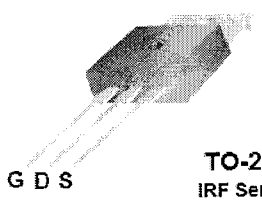
500V N-Channel MOSFET

General Description

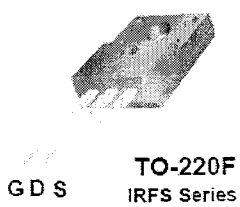
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

Features

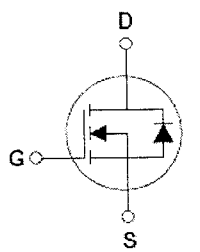
- 8.0A, 500V, $R_{DS(on)}$ = 0.8Ω @V_{GS} = 10 V
- Low gate charge (typical 41 nC)
- Low Crss (typical 35 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220
IRF Series



TO-220F
IRFS Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	IRF840B	IRFS840B	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous (T_C = 25°C)	8.0	8.0	A
	- Continuous (T_C = 100°C)	5.1	5.1	A
I_{DM}	Drain Current - Pulsed (Note 1)	32	32	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	320		mJ
I_{AR}	Avalanche Current (Note 1)	8.0		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	3.5		V/ns
P_D	Power Dissipation (T_C = 25°C)	134	44	W
	- Derate above 25°C	1.08	0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	IRF840B	IRFS840B	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max.	0.93	2.86	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.55	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 400 V, T_C = 125°C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.0 A	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.0 A (Note 4)	--	7.3	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1400	1800	pF
C_{oss}	Output Capacitance		--	145	190	pF
C_{rss}	Reverse Transfer Capacitance		--	35	45	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 8.0 A, R_G = 25 Ω (Note 4, 5)	--	22	55	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	125	260	ns
t_f	Turn-Off Fall Time		--	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 8.0 A, V_{GS} = 10 V (Note 4, 5)	--	41	53	nC
Q_{gs}	Gate-Source Charge		--	6.5	--	nC
Q_{gd}	Gate-Drain Charge		--	17	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8.0 A, dI_F / dt = 100 A/µs (Note 4)	--	390	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.2	--	µC

Notes:

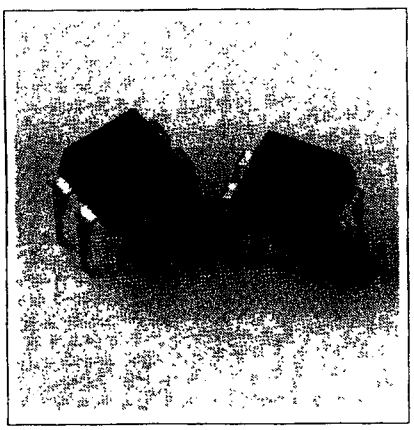
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 9.0mH, I_{AS} = 8.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 8.0A, di/dt ≤ 200A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

SIEMENS

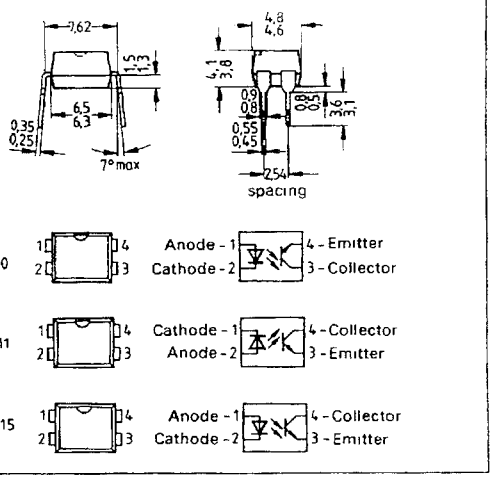
SFH 610
SFH 611
SFH 615

2.8 kV TRIOS*® OPTOCOUPLERS
HIGH RELIABILITY

T-41-83



Package Dimensions mm



FEATURES

- **Isolation Test Voltage: 2800 V**
- **High Current Transfer Ratios at 10 mA: 40-320% at 1 mA: 60% typical (>13)**
- **Fast Switching Times**
- **Minor CTR Degradation**
- **100% Burn-In**
- **Field-Effect Stable by TRIOS**
- **Temperature Stable**
- **Good CTR Linearity Depending on Forward Current**
- **High Collector-Emitter Voltage V_{CEO}=70 V**
- **Low Saturation Voltage**
- **Low Coupling Capacitance**
- **End-Stackable in 2.54 mm Spacing**
- **High Common-Mode Interference Immunity (Unconnected Base)**
- **UL Approval #52744**
- **VDE Approval 0883**
- **VDE Approval 0884 (Optional with Option 1)**

DESCRIPTION

The optically coupled isolators SFH 610, SFH 611 and SFH 615 feature a high current transfer ratio, low coupling capacitance and high isolation test voltage. They employ a GaAs LED as emitter, which is optically coupled with a silicon planar phototransistor as detector.

The components are incorporated in a plastic plug-in DIP-4 package.

The coupling devices are designed for signal transmission between two electrically separated circuits. The potential difference between the circuits to be coupled is not allowed to exceed the maximum permissible reference voltages.

The couplers are end-stackable in a 2 54 mm spacing and are considered as successor types for the couplers in metal case. The SFH 610, SFH 611 and SFH 615 differ in their arrangement of the terminal pins. Multicouplers can thus easily be implemented and conventional multicouplers can be replaced.

*TRansparent IOn Shield

Maximum Ratings

Emitter (GaAs LED)
Reverse Voltage ..... 6 V
DC Forward Current ..... 60 mA
Surge Forward Current ($t \leq 10$ µs) ..... 2.5 A
Total Power Dissipation ..... 100 mW

Detector (Silicon Phototransistor)
Collector-Emitter Voltage ..... 70 V
Collector Current ..... 50 mA
Collector Current ($t \leq 1$ ms) ..... 100 mA
Total Power Dissipation ..... 150 mW

Optocoupler
Storage Temperature Range ..... -55°C to +150°C
Ambient Temperature Range ..... -55°C to +100°C
Junction Temperature ..... 100°C
Soldering Temperature (max. 10 s)[1] ..... 260°C
Isolation Test Voltage[2]
(between emitter and detector referred to standard climate 23/50 DIN 50014) ..... 2800 VDC
Isolation Resistance (V_{IO}=500 V) ..... 10^{11} Ω

Notes:
1 Dip soldering minimum clearance from bottom edge of package 1.5 mm. Special soldering conditions apply when through-contacted circuit boards are used. Please request appropriate specification.
2 DC test voltage in accordance with DIN 57883, draft 4/78

Characteristics (T_A=25°C)

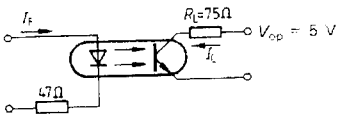
Emitter (GaAs LED)			
Forward Voltage (I_F=60 mA)	V_F	1.25 (≤1.65)	V
Breakdown Voltage (I_R=10 µA)	V_{BR}	30 (≥6)	V
Reverse Current (V_R=6 V)	I_R	0.01 (≤10)	µA
Capacitance (V_R=0 V, f=1 MHz)	C_o	25	pF
Thermal Resistance	R_{thJA}	750	K/W
Detector (Silicon Phototransistor)			
Capacitance (V_{CE}=5 V, f=1 MHz)	C_{CE}	6.8	pF
Thermal Resistance	R_{thJA}	500	K/W
Optocoupler			
Collector-Emitter Saturation Voltage (I_F=10 mA, I_C=2.5 mA)	V_{CEsat}	0.25 (≤0.4)	V
Coupling Capacitance	C_K	0.25	pF

The optocouplers are grouped according to their current transfer ratio I_C/I_F at V_{CE}=5 V, marked by dash numbers

	-1	-2	-3	-4	
I_C/I_F (I_F=10 mA)	40–80	63–125	100–200	160–320	%
I_C/I_F (I_F=1 mA)	30 (>13)	45 (>22)	70 (>34)	90 (>56)	%
Collector-Emitter Leakage Current (V_{CE}=10 V) (I_{CEO})	2 (≤50)	2 (≤50)	5 (≤100)	5 (≤100)	nA

SWITCHING TIMES

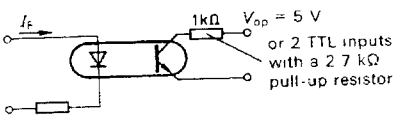
Linear Operation (without saturation)

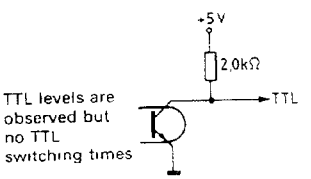


I_F=10 mA, V_{OP}=5 V, T_A=25°C

Load Resistance	R_L	75	Ω
Turn-On Time	t_{ON}	3.0 (≤5.6)	µs
Rise Time	t_R	2.0 (≤4.0)	µs
Turn-Off Time	t_{OFF}	2.3 (≤4.1)	µs
Fall Time	t_F	2.0 (≤3.5)	µs
Cut-Off Frequency	F_{CO}	250	kHz

Switching Operation (with saturation)





Group	-1 (I_F=20 mA)	-2 and -3 (I_F=10 mA)	-4 (I_F=5 mA)	
Turn-On Time t_{ON}	3.0 (≤5.5)	4.2 (≤8.0)	6.0 (≤10.5)	µs
Rise Time t_R	2.0 (≤4.0)	3.0 (≤6.0)	4.6 (≤8.0)	µs
Turn-Off Time t_{OFF}	18 (≤34)	23 (≤39)	25 (≤43)	µs
Fall Time t_F	11 (≤20)	14 (≤24)	15 (≤26)	µs
V_{CEsat}	0.25 (≤0.4)			V

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							µA µA
C-	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Typical Characteristics

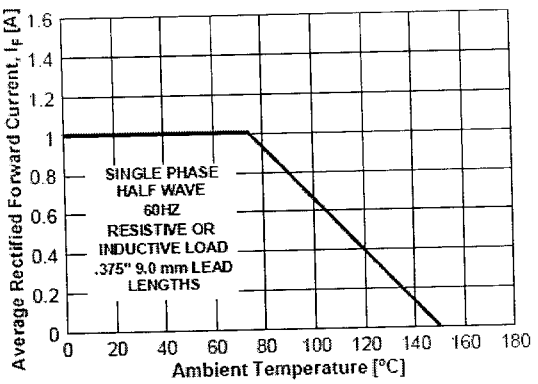


Figure 1. Forward Current Derating Curve

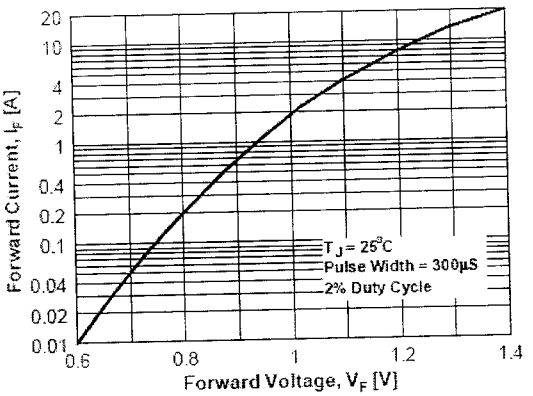


Figure 2. Forward Voltage Characteristics

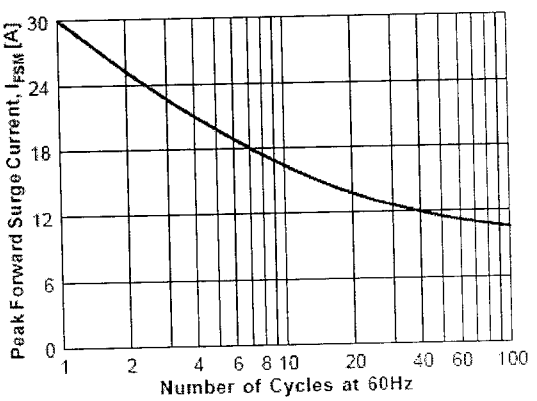


Figure 3. Non-Repetitive Surge Current

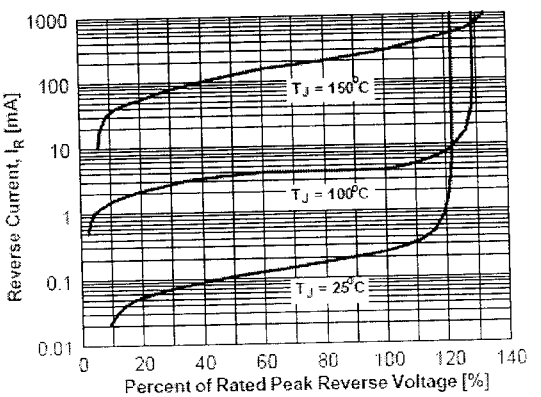
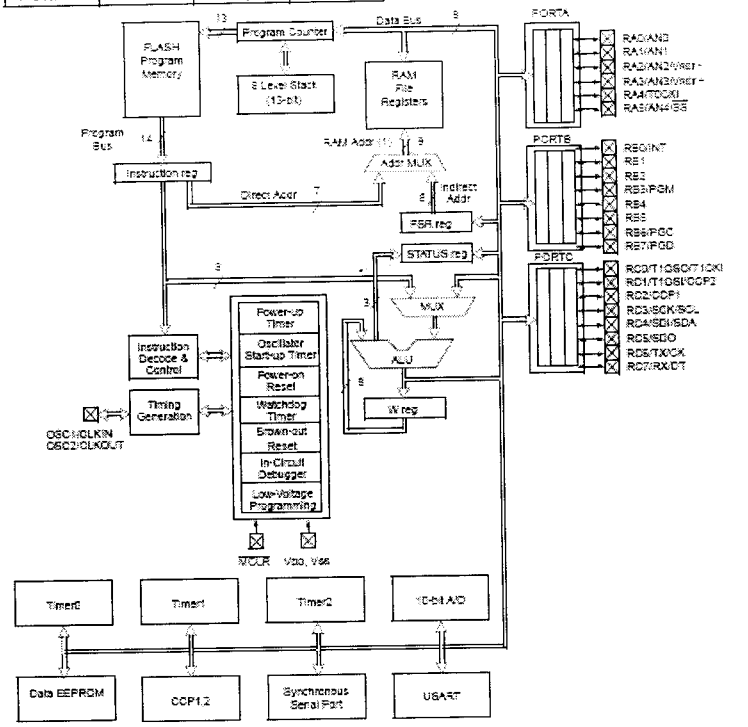


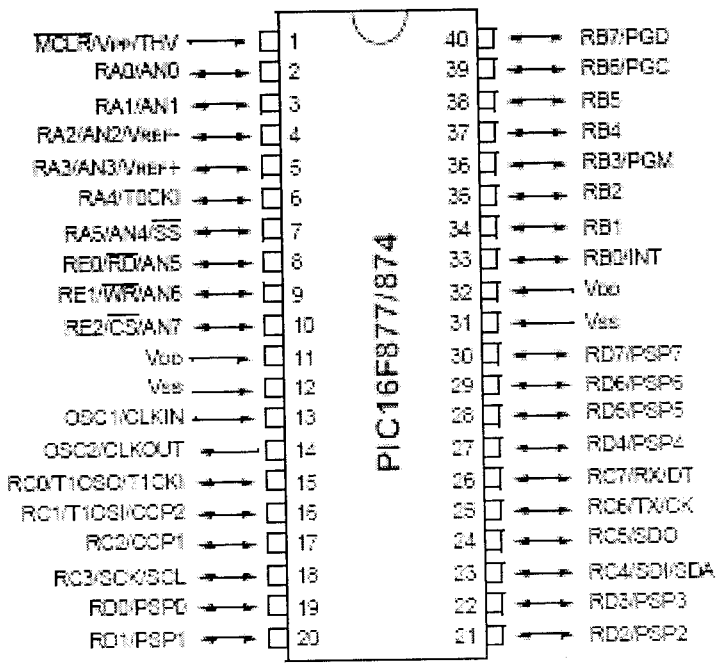
Figure 4. Reverse Current vs Reverse Voltage

ARCHITECTURE OF PIC 16F877A

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F873	4K	192 Bytes	128 Bytes
PIC16F876	8K	368 Bytes	256 Bytes



Pin Configuration of PIC16F877A



TIMER 0 CONTROL REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7: **RBPU**

bit 6: **INTEDG**

bit 5: **T0CS**: TMR0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

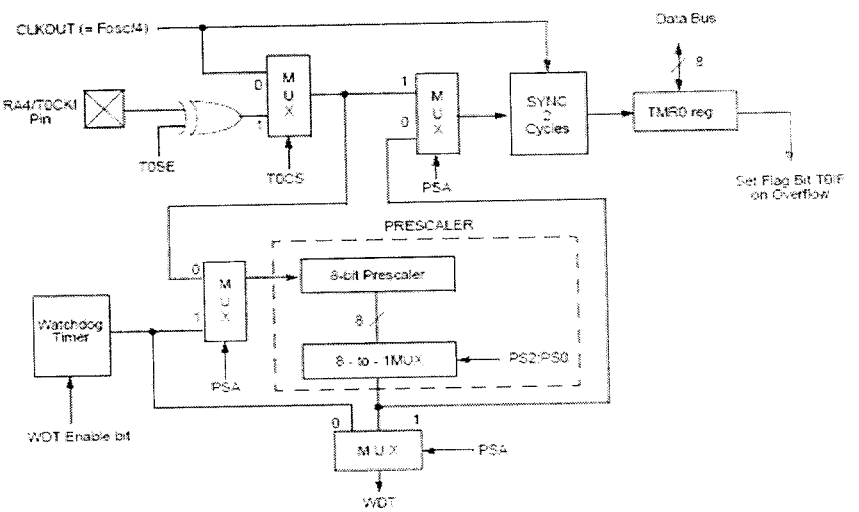
bit 3: **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

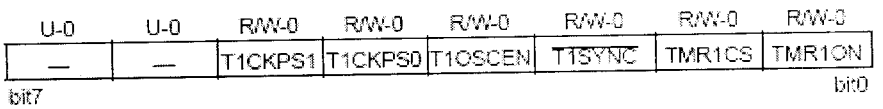
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2 PS1 PS0**: Prescaler Rate Select bits

TIMER 0 BLOCK DIAGRAM:



TIMER 1 CONTROL REGISTER:



bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled

0 = Oscillator is shut off (The oscillator inverter is turned off to eliminate power drain)

bit 2: **T1SYNC**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1

1 = Do not synchronize external clock input

0 = Synchronize external clock input

TMR1CS = 0

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)

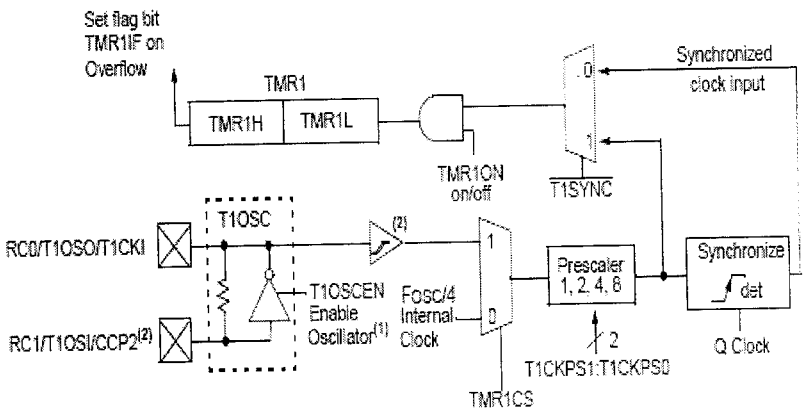
0 = Internal clock (FOSC/4)

bit 0: **TMR1ON**: Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

TIMER 1 BLOCK DIAGRAM:



TIMER 2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale

0001 = 1:2 Postscale

0010 = 1:3 Postscale

1111 = 1:16 Postscale

bit 2: **TMR2ON**: Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

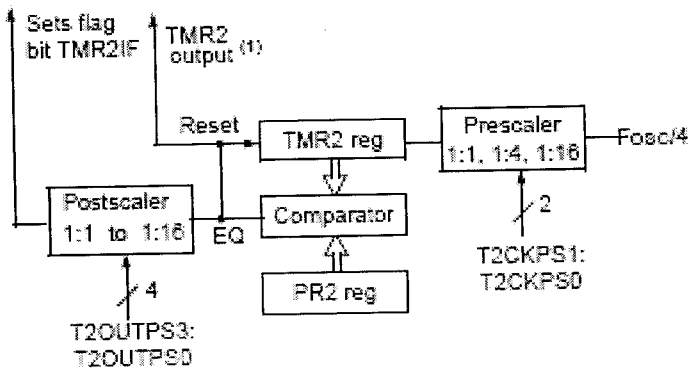
bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

TIMER2 BLOCK DIAGRAM:



CCP1CON REGISTER/CCP2CON REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX :CCPxY**: PWM Least Significant bits

Capture Mode: Unused

Compare Mode: Unused

PWM Mode: These bits are the two LSB s of the PWM duty cycle. The eight MSB s are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets CCPx module)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (CCPxIF bit is set)

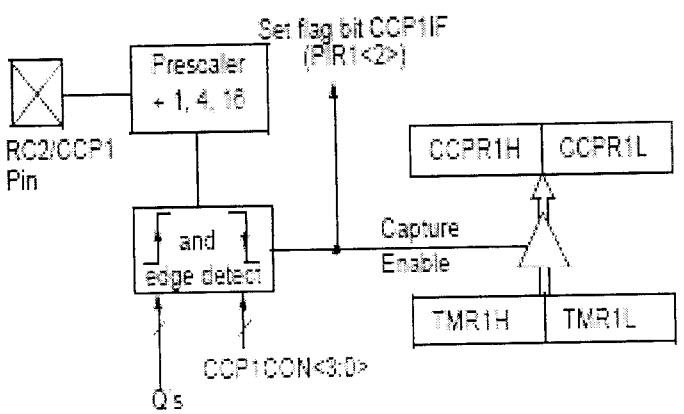
1001 = Compare mode, clear output on match (CCPxIF bit is set)

1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)

1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)

11xx = PWM mode

CAPTURE MODE OPERATION BLOCK DIAGRAM:



COMPARE MODE OPERATION BLOCK DIAGRAM: