P-3530

Energy management strategy for Coupling Super Capacitor and Battery with DC-DC Converters

A Project Report

Submitted By

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in partial fulfillment for the award of the degree
of

Master of Engineering
in
Power Electronics and Drives

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY
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Ms.Revathy Vijayan - Register No. 0920105009

Who carried out the project work under my supervision.

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ACKNOWLEDGEMENT

I humbly submit all the glory and thanks to the almighty for showering the blessings and giving the necessary wisdom for accomplishing this project.

I would like to express my deep sense of graduate and profound thanks to my guide **Mr.G.N.Murugananthan**,Assistant Professor, Electrical and Electronics Engineering Department, for his valuable guidance, support, constant encouragement and co-operation rendered throughout the project.

I take immense pleasure in thanking **Dr.Rani Thottunkal.Ph.D.**, Department of Electrical and Electronics Engineering, Kumaraguru College of Technology, for her constant encouragement and support.

I would like to express my heartfelt thanks to our beloved Principal **Dr.S.Ramachandran Ph.D.**, for his support.

I am also thankful to all my **teaching and technical supporting staffs** of Electrical and Electronics Engineering department, for their kind help and encouragement.

Last but not least, I extend my sincere thanks to my **parents and friends** who have contributed their ideas and encouraged me for completing this project.

ABSTRACT

Energy storage and power boost are major problems in development of electric vehicle. Installing a super capacitor as an auxiliary source to improve the performance of electric vehicles is a feasible and realistic solution. In this system the structure of a auxiliary energy system and principles of flow of energy was introduced. This project investigates the application of a super capacitor bank when used as a power buffer to smooth rapid power fluctuations in and out of the battery of an electric or hybrid vehicle. To achieve optimal performance, the super capacitor bank is connected to battery through a DC/DC converter. The variation of the current drawn by the load was smoothed due to the working of the super capacitor, which provided better working conditions for the battery and increased the operating life of the battery. Despite the wide variations of the SC terminal voltage, the voltage across the load remains constant.A model of super capacitor and battery, based on Matlab/Simulink was built up and results are verified. Results of simulations are presented to verify that the proposed technique is feasible. The prototype model is also designed, fabricated and tested.

CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

SC	Super Capacitor
PWM	Pulse Width Modulation
DC	Direct Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PIC	Peripheral Interface Controller
PI	Proportional Integral

CHAPTER 1

1. INTRODUCTION

Pollution problems and their effects on the environment in the long term continue to worry vehicle manufacturers. Nowadays, much research has been undertaken on technologies for future vehicles. Among these technologies in the short term, the hybrid vehicle is a promising solution. A hybrid vehicle is a vehicle that combines, in addition to its main energy source (oil or gas), reversible energy storage devices like fly-wheels, ultra capacitors, super capacitors and batteries. The advantage of HEVs in the passenger car context is that they improve fuel consumption, with consequential reduction in the greenhouse gas CO_2, and they also reduce pollutants. These pollutants include emissions of oxides of nitrogen and sulphur (NOX and SOX) and particulates. HEVs reduce pollutants not only because less fuel is burned, but also because the bum is cleaner and the temperature of the catalytic converter is better controlled. The reduction in CO2 is important because CO, is the major greenhouse gas and because transport accounts for almost 20% of CO_2 emissions. The reduction in NOX, SOX, and particulates is important because pollution in cities is almost entirely due to transport. This urban pollution is responsible for the death of about one person per 100,000 per year and causes asthmatic illnesses in many more people

A hybrid electric vehicle (HEV) is a type of hybrid vehicle and electric vehicle which combines conventional internal combustion engine (ICE) propulsion system with an electric propulsion system. The presence of the electric power train is intended to achieve either better fuel economy than a conventional vehicle, or better performance. The auxiliary power unit (APU) of an HEV is designed to provide the normal average power required by the vehicle, while the battery is sized to provide power surges needed during acceleration and hill climbing and to accept momentary powers during breaking. While EVs and HEVs are more efficient than conventional vehicles in urban areas, the electric load profile consists of high peaks and steep valleys due to repetitive acceleration and deceleration. The resulting current surges in and out of the battery tend to generate extensive heat inside the battery, which leads to increased battery internal resistance thus lower efficiency and ultimately premature failure. One of the main weak points of the battery is slow dynamics dominated by a temperature and fuel-delivery system (pumps, valves, and, in some cases, a hydrogen reformer). As a

result, fast load demand will cause a high voltage drop in a short time. which is recognized as a fuel-starvation phenomenon. Thus for vehicle applications, the electrical system must have at least an auxiliary power source to improve system performance when electrical loads demand high energy in a short time. The possibilities of using a super capacitor or a battery bank as an auxiliary source with battery main source are presented in detail. Super capacitors (also referred to as ultra capacitors or electrochemical capacitors) have much greater advantage over batteries when capturing and supplying short bursts of power due to their higher power density limits, and ability to charge and discharge very quickly. Hence adding a super capacitor bank will assist the battery during vehicle acceleration and hill climbing, and with its quick recharge capability, it will assist the battery in capturing the regenerative braking energy.

In order to reduce the size and cost of the battery and efficiently capture the breaking energy, a super-capacitor bank is connected in between the battery and the drive train. When compare to the battery, super capacitor is more resistant to sudden load changes and can handle sharp current bursts. A boost converter is employed to connect the battery to the super-capacitor and a two-quadrant bi-directional dc/dc converter is used to connect the super-capacitor to the load bus. The boost converter is used to draw the filtered and smoothened load current which reduces the stress on battery and increases its life. On the other hand, the two-quadrant dc/dc converter captures the raking energy and supplies the rest of the load demand.

Proposed battery/super-capacitor system, which is capable of meeting the demands that vehicle may encounter under any condition. Battery bank is capable of supplying the main power to drive the load; however it is not able to supply large bursts of power in short durations. For this reason, the use of super-capacitor can be considered to relieve battery pack from peak power transfer stress. due to capacitor's higher specific power and cycling efficiency. By combining battery bank and capacitor tank. it is possible to use a smaller battery with less peak-output power capability. Therefore, the cost would decrease significantly and the efficiency of the energy sources would increase. Generally, a compact, lightweight, efficient power system is desired for electrical vehicles.

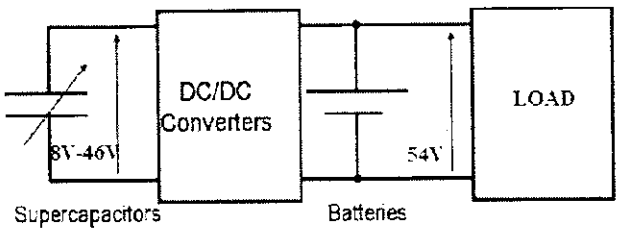

Figure 1.1 General Topology of Hybrid Sustem

To ensure the dynamic exchange of energy between the super capacitor modules and the batteries, various converter topologies are proposed. In this paper, an auxiliary super capacitor bank using a bi-directional DC-DC converter has been implemented as shown in Figure 1. Here, an auxiliary energy storage device such as a super capacitor (S.C.) is regarded as a key device for assisting the operation of the main battery against the repetitive charging/discharging operation and abrupt energy demands from the loads. The desired connection is then addressed by using a DC/DC converter in the boost mode when discharging, and in the buck mode when charging the super capacitor bank. This system always maintains constant voltage across load.

1.1 SUPER CAPACITORS

Super capacitors, also known as ultra capacitors or electrochemical capacitors, utilize high surface area electrode materials and thin electrolytic dielectrics to achieve capacitances several orders of magnitude larger than conventional capacitors. Super capacitors have a power density that is 10–100 times larger than that of batteries, but they have a density of energy that is smaller than that of batteries. Thus, super capacitors follow the evolution of the future energy need for vehicles and find their place in being a complement of or a replacement for batteries. However, it is necessary for the production of this storage device of high power energy to be cost effective. Moreover, these high-power storage devices present less risk of pollution than batteries.

In hybrid vehicles equipped with batteries and super capacitors, the super capacitors allow the following:

1) Assisting the batteries during hard transient states

2) Increasing the batteries lifespan and decreasing their size;

3) Offering performances independent of the battery state.

4) Improving the energetic efficiency while regenerative braking is employed

Super capacitors can thus be used in a lot of applications for energy storage and management. The main application for super capacitors is to use them as energy buffers to limit the power constraints on energy sources such as batteries, fuel cells, or decentralised power networks. The use of super capacitors requires power electronics in order to guarantee an efficient management of such devices. Both the design and the control of their state of charge are sensitive points because they are often connected to several energy sources.

1.1.1 PERFORMANCE COMPARISON BETWEEN SUPER CAPACITOR AND BATTERY.

Most traditional power applications for capacitors focus on 'power delivery' issues, like peak shaving and load levelling. There are fundamental differences in the characteristics between super capacitors and batteries with regard to energy density (Watt Hours) and power density (Kilowatts). Batteries can store a lot of energy, but are limited in terms of power density and response (ability to discharge and charge quickly). Due to the chemical reactions that are occur within a battery, they have a limited life with regard to cycling. Super capacitors, however, have no chemical reaction during charge/discharge, and can be cycled hundreds of thousands of times. These devices have applications in computer power back-up, power electronics, electric vehicles and space flight technology. However, power and energy demands of these applications vary significantly. Super capacitors can be charged and discharged almost an unlimited number of times. They can discharge in matters of milliseconds and are capable of producing enormous currents. Hence they are very useful in load levelling applications and fields where a sudden boost of power is needed in a fraction of a second. They do not release any thermal heat during discharge.

Function	Super capacitor	Battery
Charge time	1–10 seconds	10–60 minutes
Cycle life	1 million or 30,000h	500 and higher
Cell voltage	2.3 to 2.75V	3.6 to 3.7V
Specific energy (Wh/kg)	5 (typical)	100–200
Specific power (W/kg)	Up to 10,000	1,000 to 3,000
Cost per Wh	$20(typical)	$2 (typical)
Service life (in vehicle)	10 to 15 years	5 to 10 years
Charge temperature	–40 to 65°C (–40 to 149°F)	0 to 45°C (32°to 113°F)
Discharge temperature	–40 to 65°C (–40 to 149°F)	–20 to 60°C (–4 to 140°F)

Table 1.1 Comparison between super capacitor and battery

1.1.2 ADVANTAGES AND LIMITATIONS OF SUPER CAPACITORS

Advantages

- unlimited cycle life; can be cycled millions of time
- High specific power; low resistance enables high load currents
- Charges in seconds; no end-of-charge termination required
- Simple charging; draws only what it needs; not subject to overcharge
- Excellent low-temperature charge and discharge performance
- Good reversibility
- Improved safety, no corrosive electrolyte and low toxicity of materials.
- Simple charge methods—no full-charge detection is needed; no danger of overcharging.
- Extremely low internal resistance (ESR) and consequent high cycle efficiency (95% or more) and extremely low heating levels

Limitations

- Low specific energy; holds a fraction of a regular battery
- Linear discharge voltage prevents using the full energy spectrum

- High self-discharge; higher than most batteries
- Low cell voltage; requires serial connections with voltage balancing
- High cost per watt.

Table 1.2 Advatages and limitations of super capacitor

1.2. OBJECTIVE OF THE PROJECT

The objective of this project is to establish the dynamic control strategy of the dc/dc converters for energy management between the batteries and super capacitors. This dynamic control strategy is based on current control because the dc-link voltage level is imposed by the battery module. The main aim of this system is to maintaining suitable current sharing and constant voltage across load. Also to investigate the performance of the proposed system by examining the voltage and current waveforms using MATLAB/ SIMULINK Software.

1.5 LITERATURE SURVEY

The super capacitor is ideal for energy storage that undergoes frequent charge and discharge cycles at high current and short duration. This topology was first described by Lambert, S.M.; Pickert V in his paper "Comparison of super capacitor and lithium-ion capacitor technologies for power electronics applications".

The dc-dc converter topology for electric vehicles was first realised by M.Marchesoni and A. Vacca in his paper "A new DC-DC converter topology for power management in fuel cell electric vehicles with energy storage systems". All previous works have focussed attention to use neural networks and polynomial control strategy. Here a new control strategy is proposed for energy management.

An investigation on the implementation of DC-DC converter to share energy between super capacitor and battery was done by Camera M.B, Gualous H in his paper "Design and New Control of DC/DC Converters to share energy between Super capacitors and Batteries in Hybrid Vehicle".

An experimental setup was proposed by Camera M.B ,F.Gustin in his paper "Energy management strategy for coupling Super capacitors and battery with DC-DC converter". Excellent results like proper current sharing and good voltage regulation has been achieved by the system.

1.6 ORGANISATION OF THE THESIS:

This report presents an energy management control strategy for coupling super capacitor and battery system .Chapter 1 gives an overview of the super capacitor and difference between super capacitor and battery. Chapter 2 details the existing super capacitor and battery system coupling with DC-DC converter with its MATLAB Simulation model. Chapter 3 describes the proposed super capacitor-battery system with parallel DC-DC converter system along with the control strategies. Chapter 4 deals with the MATLAB Simulation model of the proposed system is also obtained and compared with the base paper model. Chapter 5 deals with the hardware modelling of the proposed system, results of hardware testing and the process coding of the PIC controller. In Chapter 6 the conclusion and future scope of the project is discussed.

CHAPTER 2

2. THE EXISTING SUPER CAPACITOR-BATTERY SYSTEM WITH DC-DC CONVERTER.

The existing system includes a power source (super capacitors), an energy source (batteries), load, and a buck–boost converter. The super capacitor module is connected to the dc link using a bidirectional converter to ensure the charge and discharge of the electric power storage devices. The converter control depends on the energy-management strategy between the hybrid sources and the load request. This converter modelling includes the boost and buck operating modes.

2.1 BLOCK DIAGRAM OF THE EXISTING SYSTEM

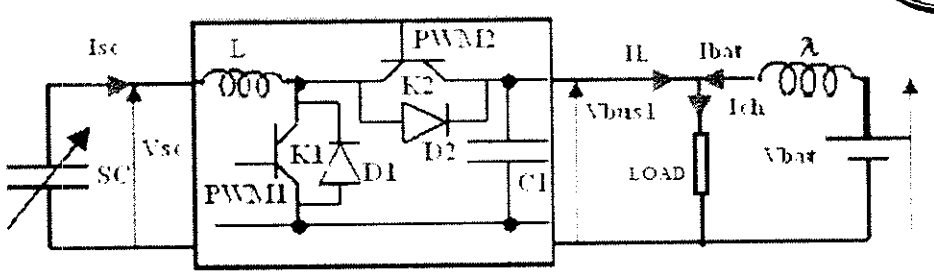

Figure.2.1 Buck–boost converter topology

The main objective is to establish the dynamic control strategy of the dc/dc converters for energy management between the batteries and super capacitors. This dynamic control strategy is based on current control because the dc-link voltage level is imposed by the battery module.

For this topology, a bidirectional buck–boost converter ensures energy exchange between the super capacitor and battery modules. The converter topology is presented in Figure. 2.1.

2.2 MODES OF OPERATION

2.2.1 BOOST CONVERTER MODE

In Boost mode, switch *K*1 is on, and *K*2 is off, and the super capacitor module provides energy to the dc bus. The *I*sc super capacitor current direction is presented in Figure 2.2.

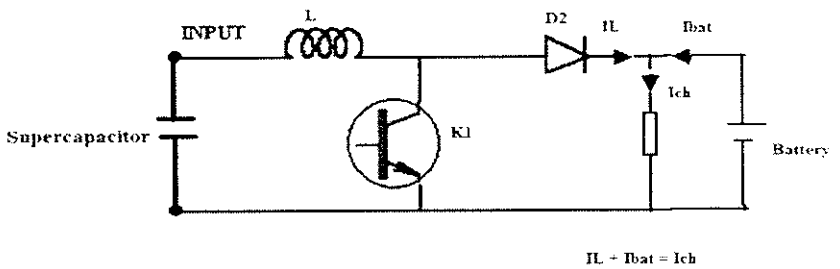

Figure.2.2 Boost converter topology

During this operation, the power demand of the drive train becomes positive and the K1 switch is activated according to the PWM pulses. Turning ON of switch K1 will put voltage Vsc on one end of the inductor. This voltage will tend to cause the inductor current to rise. When the switch is OFF, the current will continue flowing through the inductor but now flowing through the diode. That is super capacitor modules are discharged from their maximum voltage to nominal voltage .During this period, the significant portion of load current is delivered by super capacitor module. The rest portion of load current is supplied by battery.

$$VL = L * d/dt\ (isc) = Vsc - (1 - \alpha 1) \cdot Vbus1 \quad (1)$$

$$Ich = IL + Ibat \quad (2)$$

$$V\lambda = \lambda * d/dt\ (ibat) = Vbat - Vbus1 \quad (3)$$

2.2.2 BUCK CONVERTER MODE

Contrary to boost mode, here, $K2$ is on, and $K1$ is off, and the super capacitor module is charged by a battery. The Isc and IL currents direction are shown in Figure 2.3

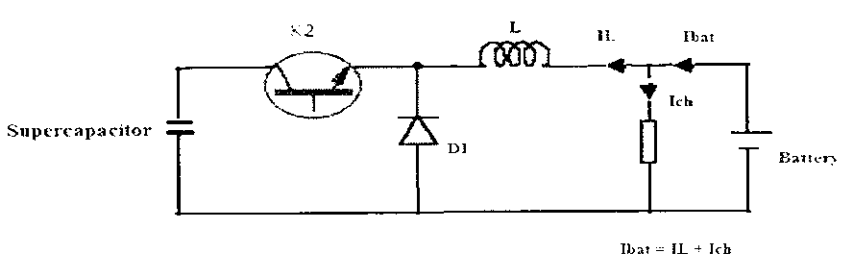

Figure.2.3 Buck converter topology

Buck operation is accomplished with a controlled operation on K2. When K2 is switched ON, the energy goes from the battery pack to the super capacitor. Here battery current will be the sum of load current and DC bus current.

$$VL = L * d/dt\ (isc) = \alpha 2 * V\text{bus1} - V\text{sc} \quad (4)$$

$$I\text{bat} = IL + I\text{ch} \quad (5)$$

$$V\lambda = \lambda * d/dt\ (i\text{bat}) = V\text{bat} - V\text{bus1}. \quad (6)$$

2.3 SIMULATION OF THE EXISTING SYSTEM USING MATLAB 7.0.4

2.3.1 The Overall System Structure

Simulations were realized in two steps . Simulation of Buck converter mode and boost converter mode are simulated using MATLAB. The switching frequency of 10 kHz was used to investigate the characteristics of buck and boost converter. The battery voltage is fixed at 54V and the super capacitor voltage is varied between 19V to 38V.This topology is tested using RL load. The measurements are taken from the measurement block.

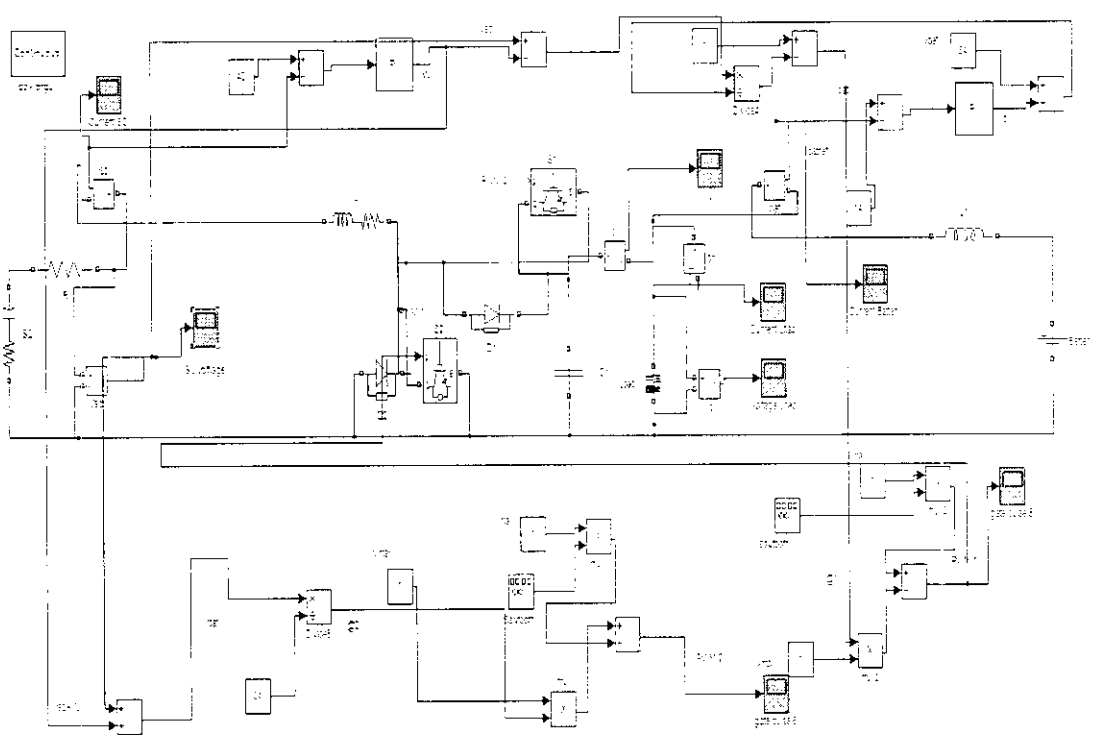

Figure.2.4 The MATLAB/SIMULINK model of the existing system

2.4 SIMULATION RESULTS

The operation of the base paper system is evaluated by computer simulation using MATLAB/SIMULINK.

2.4.1 Buck Converter Simulation Results:

Here the power flow is from battery to super capacitor. With this single converter the super capacitor module is charged in very small range that is from 27 V to 38V. The *I*sc and *IL* currents directions are shown in Figure 2.6 and 2.7. The *I*scref super capacitor reference current is fixed at 60 A. Figure. 2.5–2.6 gives the simulation results of the super capacitor voltage and current respectively. Due to the battery current, the load voltage (*VL*) drops slightly, but it remains between 3%-4% of the rated voltage (54 V) as shown in Figure. 2.10.

In buck operation, battery alone feeds the load, that is

$$I_{bat} = I_l + I_{ch} \qquad (12)$$

The current delivered by the battery will be the sum of dc bus current is ensured by super capacitor module and load current as shown in Figures 2.7-2.9, that is the control strategy used is satisfactory.

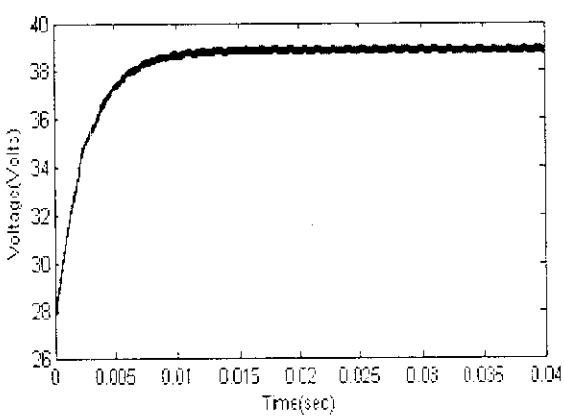

Figure.2.5 Super capacitor Voltage

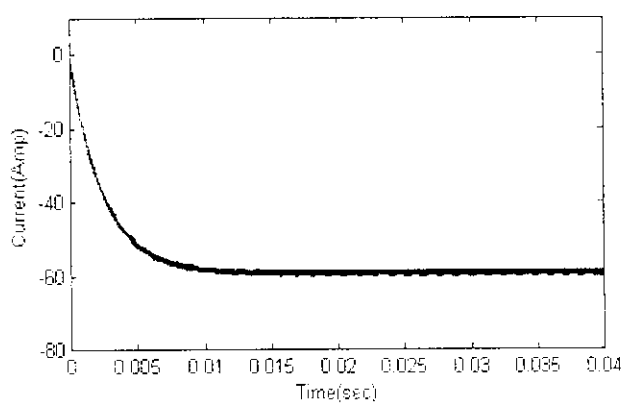

Figure.2.6 Super capacitor Current

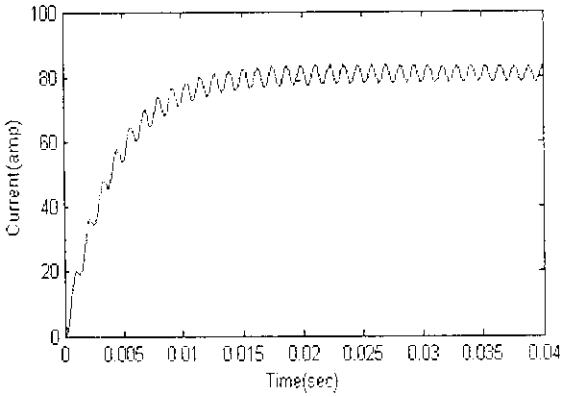

Figure. 2.7 DC bus Current (IL)

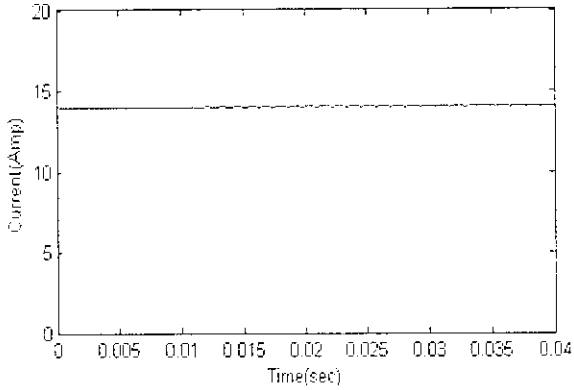

Figure. 2.8 Load Current (Ich)

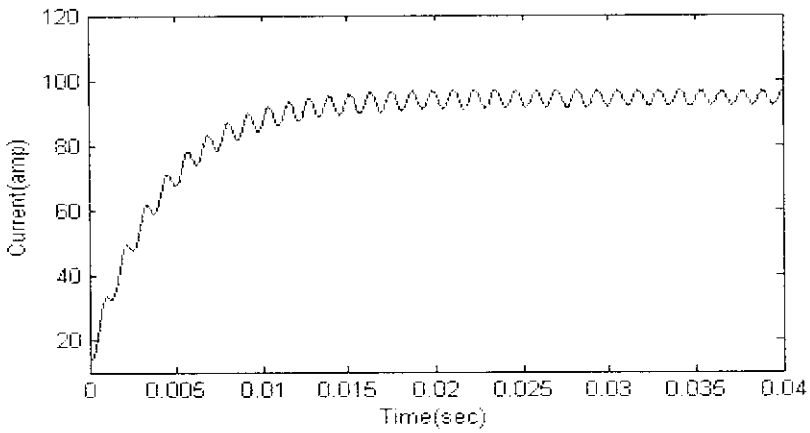

Figure 2.9 Battery Current (Ibat=IL+Ich)

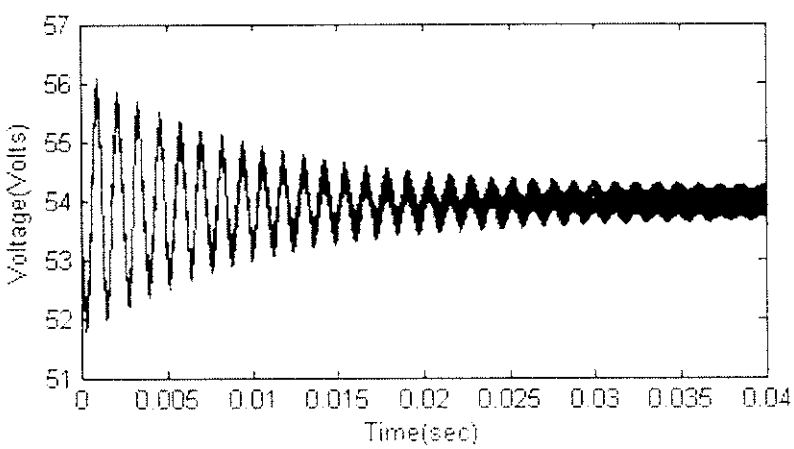

Figure. 2.10 Load Voltage (VL)

2.4.2 **Boost Converter Simulation Results**:

The load request (Ich) is fixed at 14 A, and the *I*batref reference current is also fixed at 5 A. The power flow is from super capacitor to load. The super capacitor module discharge is compensated by the super capacitor current control loop, which allows an increase in the *I*sc current value when its voltage decreases, as in Figure.2.11 and 2.12. This control enables maintaining the super capacitor power constant. With this single converter the super capacitor module can discharge only in small range that is it discharges from 27 V to 19 V.

In this time interval, only 57% of the energy required by the load is ensured by the super capacitor module and remaining 43% supplied by battery. This condition will create overload on battery and chance for breakdown of battery is high. Here simulation results of current control strategy as shown in Figures.2.13-2.15. The battery module enables maintenance of the *V*L of the load voltage between 56and 52V as indicated in Figure 2.16.

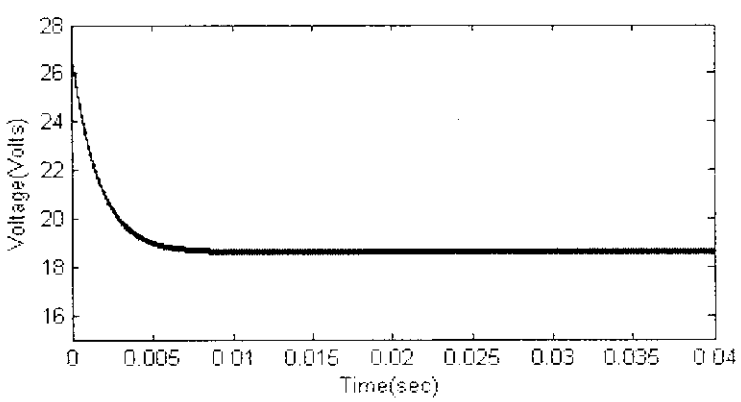

Figure.2.11Super capacitor voltage

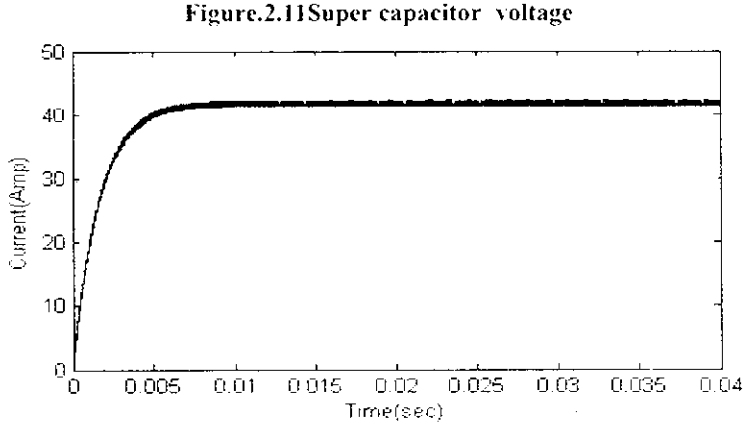

Figure.2.12 Super capacitor Current

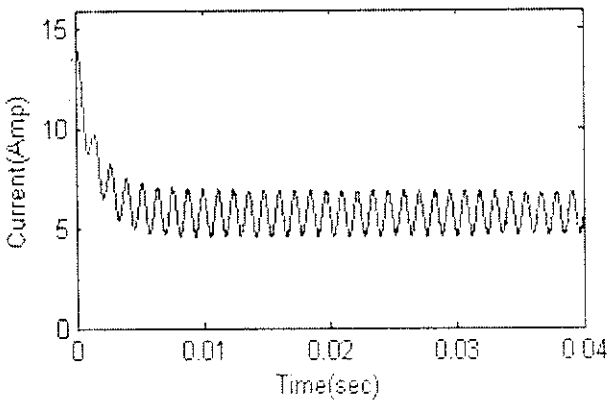

Figure. 2.13 Battery Current (Ibat)

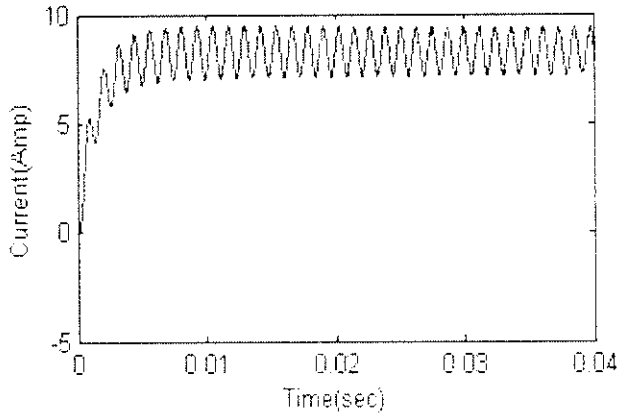

Figure. 2.14 DC bus Current (IL)

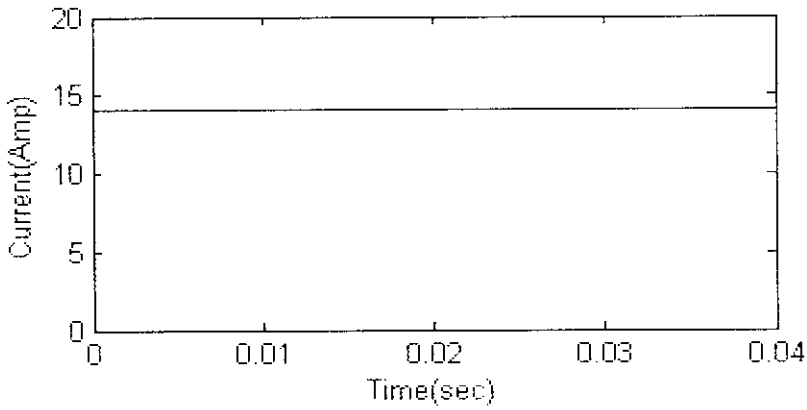

Figure. 2.15 Load Current (Ich=IL+Ibat)

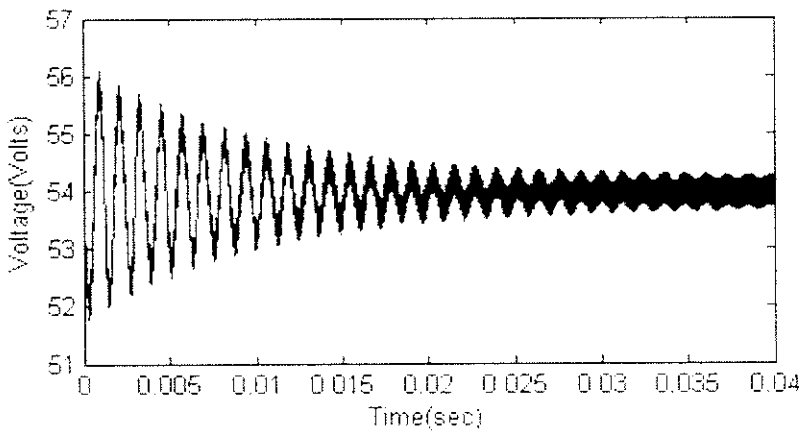

Figure. 2.16 Load Voltage (VL)

2.5 CONCLUSION

The simulations were realized in two steps .Buck converter mode and Boost converter modes are simulated using MATLAB. With single DC-DC converter, the output voltage drops slightly, but it remains between 3% −4% of the rated voltage (54 V).The current sharing by battery and super capacitor is not efficient in this system. In boost mode of existing system, the current shared by battery and super capacitor are almost equal, this condition may leads to overheating of battery and that in turn lead to breakdown of battery. And same situation may arise in buck mode also. In order to reduce the fluctuations in output voltage parallel connected DC-DC converter system is proposed.

CHAPTER 3

3. PROPOSED SUPER CAPACITOR-BATTERY SYSTEM WITH PARALLEL BUCK BOOST CONVERTER.

The power distribution between Battery and Super capacitors is managed by intelligent energy management system. As a result the battery exhibited a rather smooth power profile while peak power demand was covered by the capacitors. In this paper because of converter saturation, the parallel topology of two buck–boost converters is proposed to satisfy the load request. The super capacitor modules are connected to the dc bus by two buck–boost converters that ensure the charge and discharge of the super capacitors. The control of these converters depends on hybrid vehicle energy management. This converter topology is presented in Fig. 12. The system is made up of two super capacitor modules, a battery module, an active load, and two buck–boost converters that ensure the energy exchange between the hybrid sources and the dc bus

3.1 PARALLEL CONNECTION OF DC-DC CONVERTER

There are many reasons for paralleling power circuits or converters. Current/power ratings of available components (power semiconductors, transformer core) may be too small to handle the needed power. Different power levels and input/output specifications are configured with parallel and/or series connection of one type of modular power supply. The need for redundant and reliable operation is also a reason for parallel combinations of circuits.

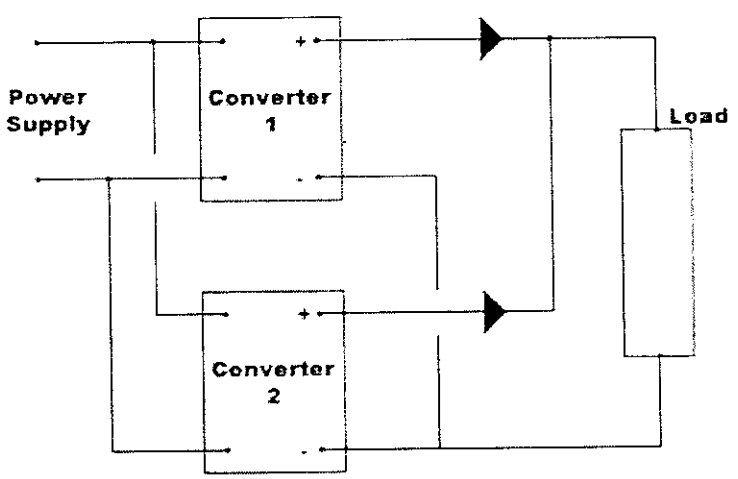

Figure 3.1 Parallel Connection Of Buck Boost Converter

- Ideally, the modules should be connected in parallel as it is shown on the Figure 3.1.
- Ideally, the Output current will be shared equally between two converters, if they are identical.
- It is important that each of the paralleled modules have approximately the same impedance between their Outputs and then the common load on the Output connection should be symmetrical.
- If one or more parameters are different, imbalance of output converter current will occur.
- When connecting two converters in parallel, the +Vout signals should be tied together with a low impedance connection by a large plane type connection of the circuit board. The same configuration should be implemented for the –Vout signal.
- To reduce the ripple current at the minus input connection and to improve paralleled performance of DC-DC converters connected in parallel, it is recommended that a capacitor be placed at the input of each module.
- When redundancy is required or when 3 and more converters are connected, a diode needs to be connected in series with the positive output of each paralleled module. This will prevent a unit that has short failure at the Output from shorting out the entire load.

3.1.1 The advantages of the parallel connected DC-DC converter are:

Some of the applications for connecting power modules in parallel include:

- To increase the Output Power capability on the supplying unit by connecting 2 or more converters in parallel.
- To provide redundancy and to ensure that the system remains functional should a single power module fail.

There are other advantages to using parallel connections of power converters, such as:

- In applications where space is limited, using 2 or more lower power converters often consumes less of the
- Valuable space on the PCB board than a single higher power module.
- The use of multiple power modules distributes the thermal heat load over a larger board area.

- Higher power requirements can be achieved using lower power modules in parallel.

3.2 BLOCK DIAGRAM OF PARELLEL TOPOLOGY OF BUCK BOOST CONVERTER

To avoid overloads with only one buck boost converter a parallel structure has been proposed, to satisfy the energy request of the load. This topology is shown on Figure 3.2.

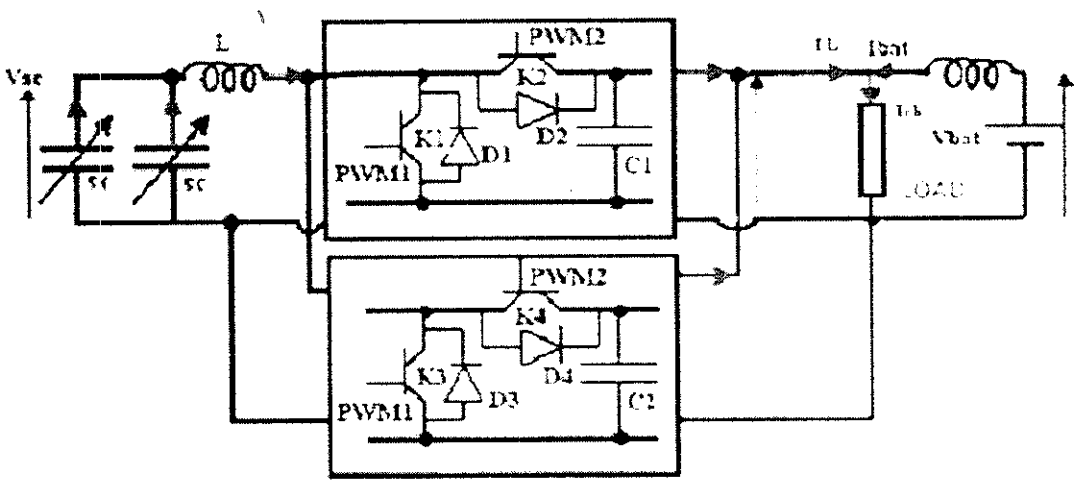

Figure.3.2 Proposed Parallel **Topology Of The Buck–Boost Converters**

3.3 THE CONVERTER OPERATION

The objective of this paper is to present results on of a parallel connected bidirectional DC-DC converter (Buck-Boost), which is placed between a super capacitor and a 54V DC-link. This topology aims to adapt the constant current and the voltage levels across load.

3.3.1 BOOST CONVERTER MODE

Here two converters are connected in parallel to ensure the energy management between super capacitor and battery. In Boost mode, switch *K*1 is on, and *K*2 is off, and the super capacitor module provides energy to the dc bus. The *I*sc super capacitor current direction is presented in Figure 3.3. The working of parallel connected converter is same as first converter operation. In this converter switch K3 is on, and K4 is off.

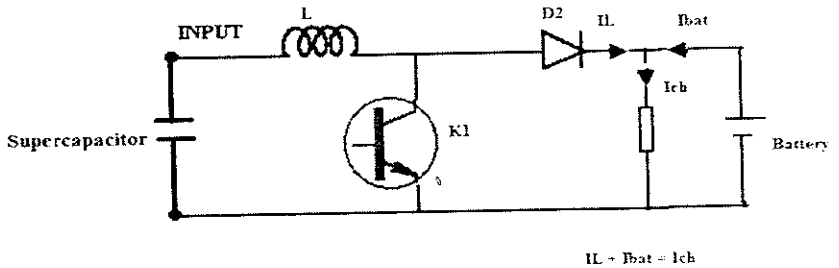

Figure 3.3 Boost Converter Mode

$$VL = L * d/dt\ (isc) = Vsc - (1 - \alpha 1)\ \cdot\ Vbus1 \qquad (1)$$

$$Ich = IL + Ibat \qquad (2)$$

$$V\lambda = \lambda * d/dt\ (ibat) = Vbat - Vbus1 \qquad (3)$$

3.3.2 BUCK CONVERTER MODE

Contrary to boost mode, here, $K2$ is on, and $K1$ is off, and the super capacitor module is charged by a battery. The Isc and IL currents direction are shown in Figure 3.4.The operation of parallel converter is same as that of buck mode operation of first converter.

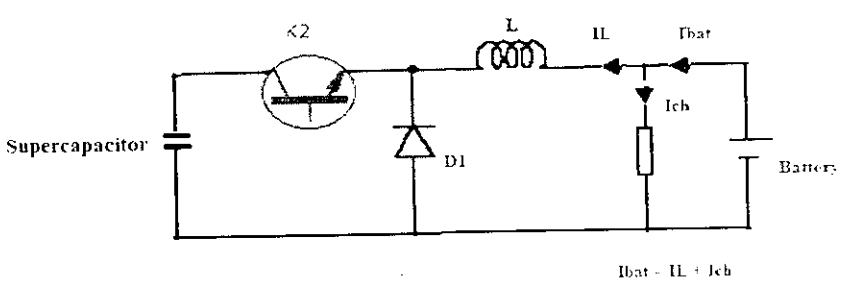

Figure.3.4. Buck Converter Mode

$$VL = L * d/dt\ (isc) = \alpha 2 * Vbus1 - Vsc \qquad (4)$$

$$Ibat = IL + Ich \qquad (5)$$

$$V\lambda = \lambda * d/dt\ (ibat) = Vbat - Vbus1. \qquad (6)$$

3.4 CONTROL STRATEGY

The voltages drops in the L and λ inductances are respectively given by VL and V_{λ}. The converter average model has a nonlinear behaviour because of crosses between the control variable ($\alpha 1$) and the (Isc, Vbus1) state variables. The Vbus1, Vsc, Ich and Vbat variables are likely to disturb the control; they must be measured and used in the estimate of the control law to ensure a dynamics of control.

Control frequency f is fixed at 10 kHz. Damping ratio ε and super capacitor current smoothing inductance L are fixed at 0.707 and 100 μH, respectively. The system bandwidth is limited to 10% of the control frequency. To choose Kpsc and Kisc values inside the bandwidth, a β parameter was introduced. This variable is included between 0 and 1, and it gives all possible values of the bandwidth. The gain expressions are given in expression (7)

$$\omega_n = 2000 \cdot \pi \cdot \beta$$

$$Kp\text{sc} = 0.89 \cdot \beta \qquad (7)$$

$$Ki\text{sc} = 3947.84 \cdot \beta^2$$

$$0 < \beta \leq 1.$$

By analogy with the super capacitor current loop, the battery current gain correctors are given in expression (8)

$$Kp = 2 \cdot \varepsilon \cdot \lambda \cdot \omega_n$$

$$Ki = \lambda \cdot \omega_n^2 \qquad (8)$$

$$\omega_n \leq 2 \cdot \pi \cdot f/10 .$$

The final control laws are now given by the standardized voltage equations are presented in expressions (9) and (10)

3.4.1 Standardized Voltage in Boost Mode:

For this operating mode, the super capacitor module discharges, and its voltage decreases from 27V to 8V. The control strategy used is to store all measurement errors

samples of the super capacitors and battery currents to estimate the voltage drops in L and λ inductors.

The VL estimation is obtained by the Isc super capacitor current control. The methodology of this estimation is presented

in Figure 3.5. As for $V\lambda$ estimation, it is obtained by the battery current control diagram presented in Figure.3 6.

The boost converter law control is given by,

$$\alpha_1 = 1 - \frac{Vsc - V_L}{Vbat - V_\lambda} \tag{9}$$

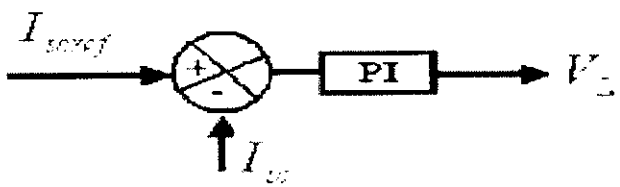

Figure 3. 5 VL Voltage Estimation.

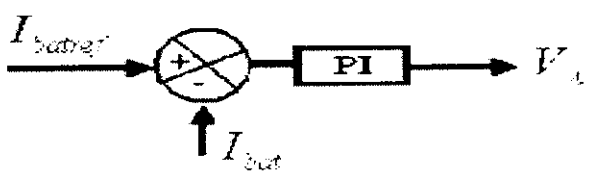

Figure 3.6. Iλ Voltage Estimation

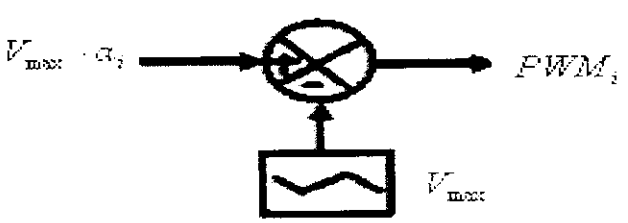

Figure. 3.7. Buck–Boost Converter Control Diagram.

3.4.2 Standardized Voltage in Buck Mode:

Contrary to standardized voltage in boost mode, the super capacitor module is charged, and its voltage changes from 27V to 50V.The VL voltage estimation is identical to the boost converter mode as shown in Figure 3.5. Super capacitor current value is the desired charging current of the capacitor module. The resulting control law is given by

$$\alpha_2 = \frac{Vsc + V_L}{V_{bus1}} \tag{10}$$

3.4.3 Control Diagram:

The standardized voltages ($\alpha 1$ and $\alpha 2$) are compared to the triangular carrier wave, with amplitude Vmax equal to 1 V and switching frequency f equal to 10 kHz, to generate pulse width modulation (PWM) signals PWM1 and PWM2, as indicated in Figure. 3.7. PWM1 and PWM2 signals are given by expression (11)

$$PWM_i = V_{\max} * \alpha_i - \frac{V \max \alpha(\cos(2\Pi fi))}{\Pi}$$
$$i = \{1,2\} \tag{11}$$

where i = 1 for the boost mode, and i = 2 for the buck mode.

CHAPTER 4

SIMULATION OF THE PROPOSED SYSTEM USING MATLAB 7.0.4

4.1 THE OVERALL SYSTEM STRUCTURE

The MATLAB/SIMULINK based simulation model of the proposed system is shown in figure 3.11. Simulations were realized in two steps because of the computer memory size limitation. Simulation of Buck converter mode and boost converter mode are simulated using MATLAB. The switching frequency of 10 kHz was used to investigate the characteristics of buck and boost converter. The battery voltage is fixed at 54V and the super capacitor voltage is varied between 8V to 50V.This topology is tested using RL load.

To define the converters control laws and to carry out simulations, the following assumptions are made.

1) The semiconductors are ideal, that is to say, there are no losses in semiconductors during their conduction and switching.

2) There are no losses in the connecting devices.

The measurements are taken from the measurement block. The MOSFET switches are controlled by the controller block.

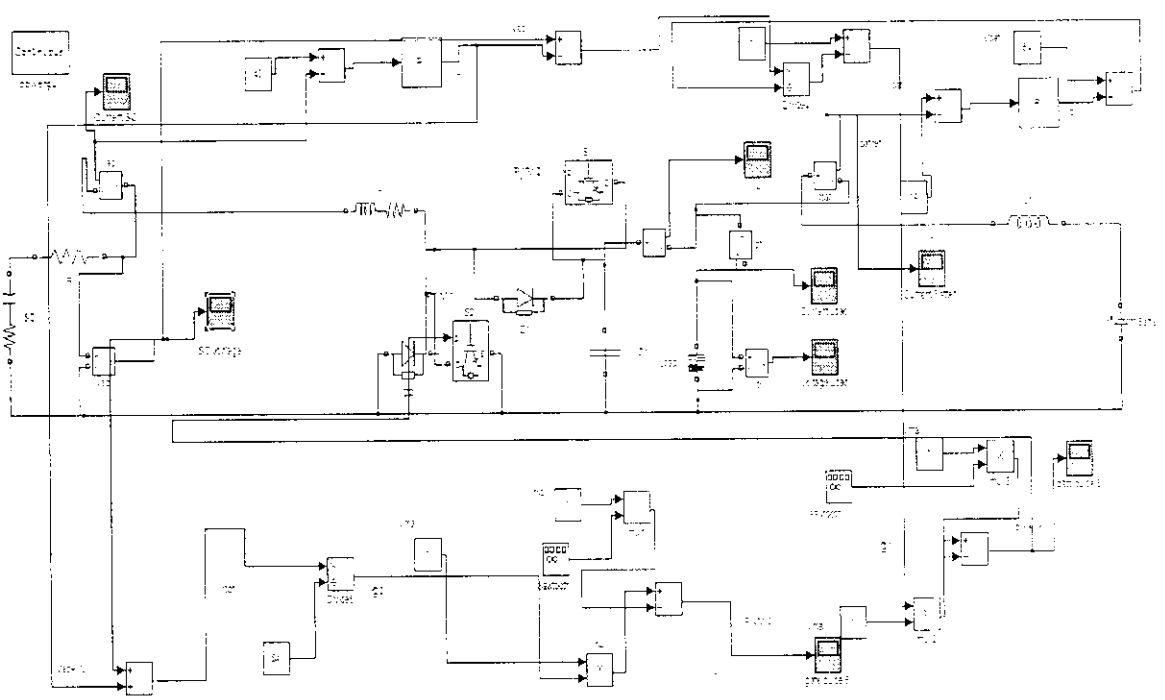

Figure.4.1 MATLAB/SIMULINK MODEL of the proposed circuit

4.2 SIMULATION RESULTS

The simulation is done with a load of 3.8 Ohms 8mH.Super capacitor value of a1750 F and battery voltage of 54 V is selected for simulation purpose. A capacitor of value 50 microF is chosen for filtering purpose. The output voltage is remaining constant with an rms value of around 54 V. In both modes of operation the current sharing by super capacitor and battery are efficient as compared to existing system.

4.2.1 Buck Converter Simulation Results:

Here the power flow is from battery to super capacitor. The super capacitor module is charged from 27 V to 50V. The *I*sc and *IL* currents directions are shown in Figure 4.3 and 4.5. The *I*scref super capacitor reference current is fixed at 60 A. Figure. 4.2–4.3 gives the simulation results of the super capacitor voltage and current, respectively. Here the load voltage remains in the rated voltage (54 V) as shown in Figure.4.6.

In buck operation, battery alone feeds the load , that is

$$I_{bat} = I_L + I_{ch} \qquad (12)$$

The current delivered by the battery will be the sum of dc bus current is ensured by super capacitor module and load current as shown in Figures 4.4-4.6, that is the control strategy used is satisfactory.

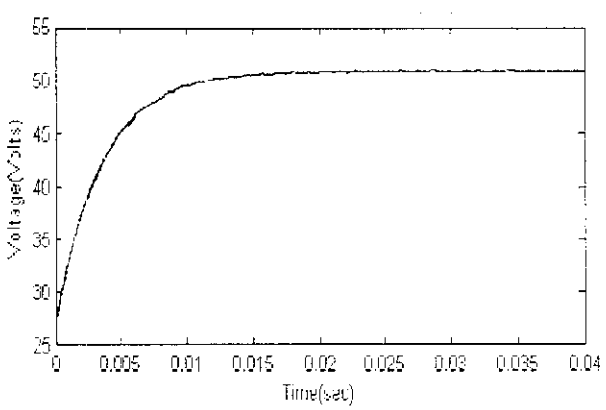

Figure 4.2 Super capacitor Voltage

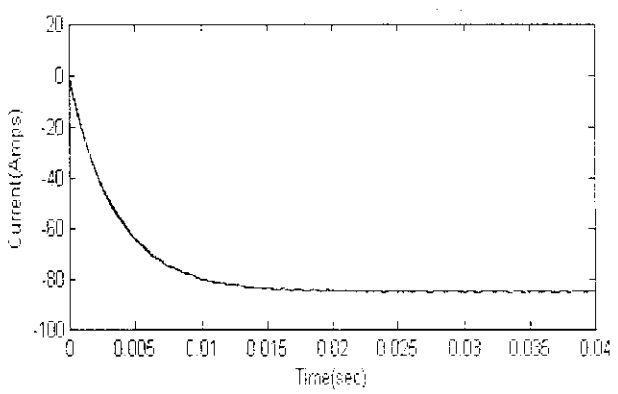

Figure 4.3 Super capacitor Current

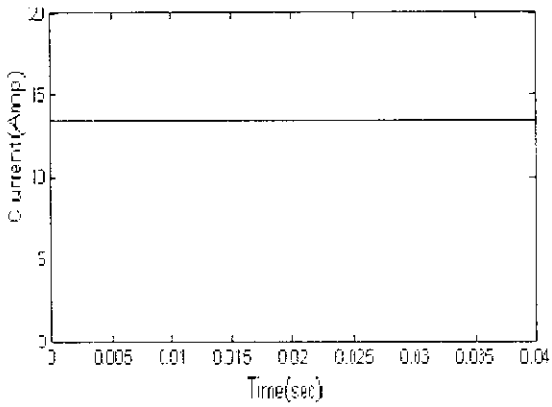

Figure.4.4 Load Current (Ich)

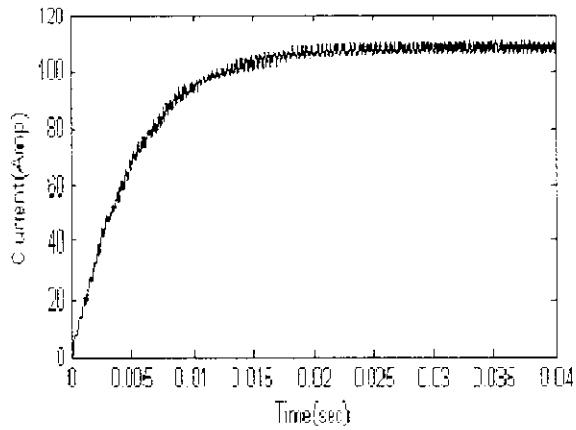

Figure.4.5 DC bus Current (IL)

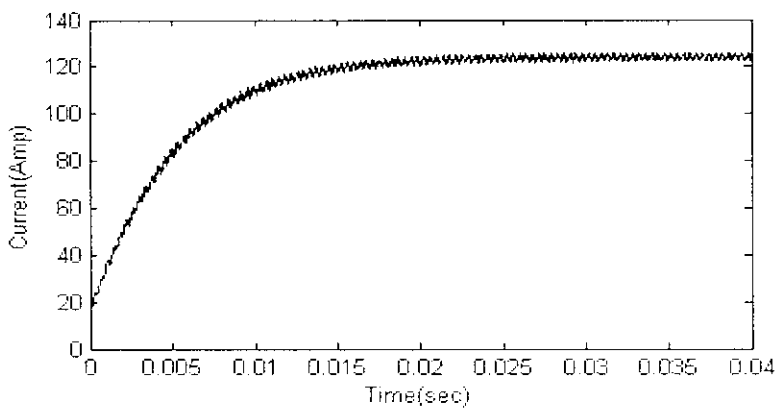

Figure. 4.6 Battery Current (Ibat=IL+Ich)

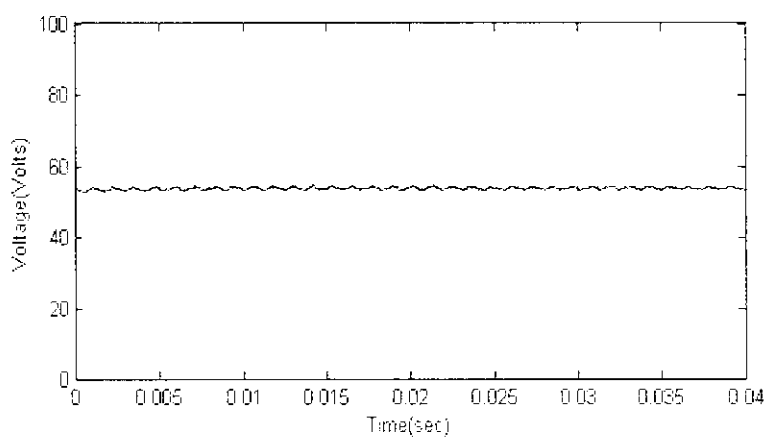

Figure 4.7 Load Voltage (VL)

4.2.2 Boost Converter Simulation Results:

The load request (Ich) is fixed at 14 A, and the *I*batref reference current is also fixed at 5 A. The power flow is from super capacitor to load. The super capacitor module discharge is compensated by the super capacitor current control loop, which allows an increase in the *I*sc current value when its voltage decreases, as in Figure.4.8 and 4.9. This control enables maintaining the super capacitor power constant. In this time interval, 79% of the energy required by the load is ensured by the super capacitor module and only remaining 21% of energy supplied by battery. This type of current sharing is efficient and it will not create a problem like break down or overloading of battery. In boost converter simulation.

$$I_{ch} = I_{bat} + I_L \qquad (13)$$

Here simulation results validate the current control strategy as shown in Figures. 4.10-4.12. The load voltage remains in 54V.

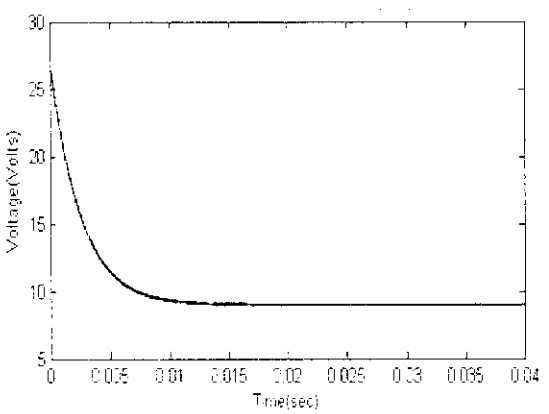

Figure 4.8 Super capacitor Voltage

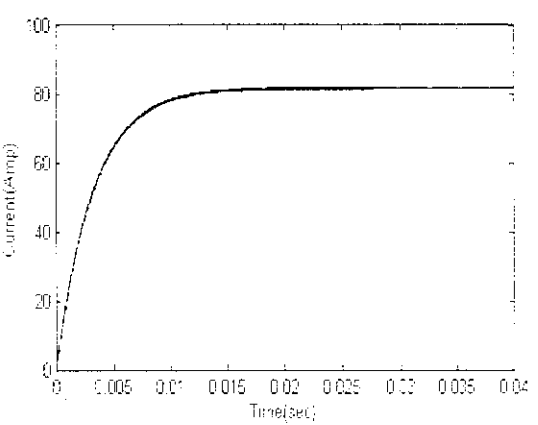

Figure 4.9 Super capacitor Current

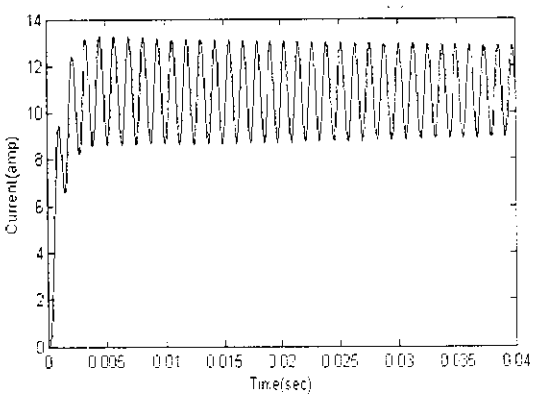

Figure.4.10 DC Bus Current (IL)

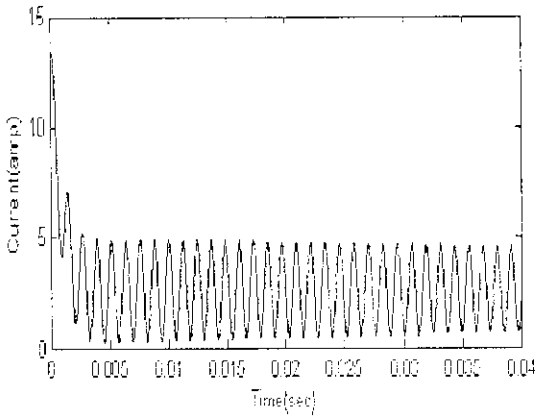

Figure.4.11 Battery Current (Ibat)

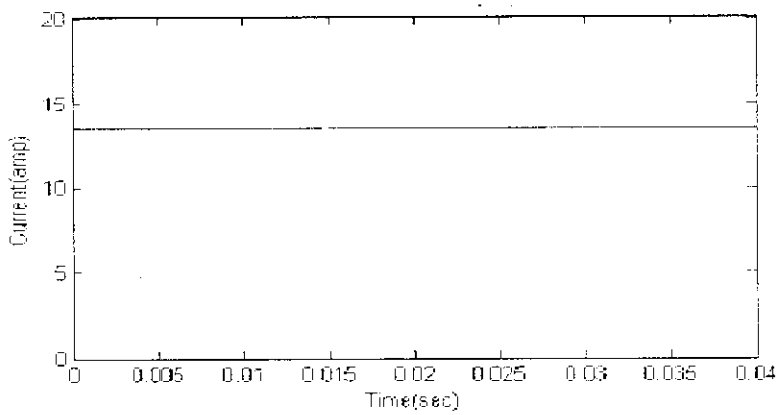

Figure.4.12 Load Current (Ich=IL+Ibat)

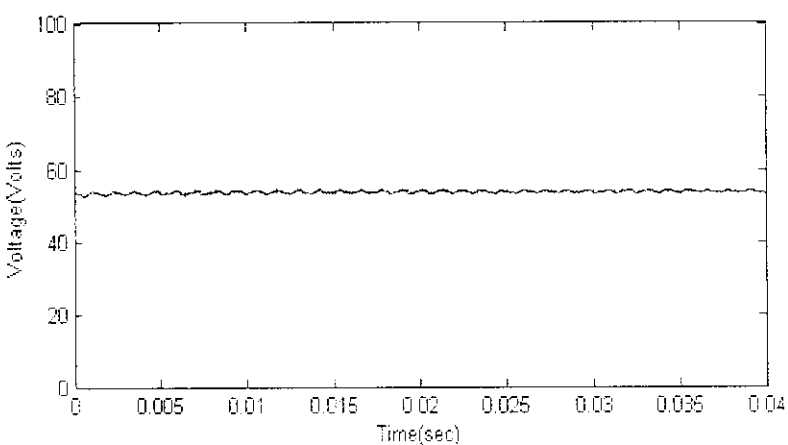

Figure.4.13 Load Voltage (VL)

4.3 COMPARISON OF THE SIMULATION RESULTS

The comparison of the existing super capacitor-battery system with the proposed parallel system is shown using the simulation results through figures 4.13 to 4.14 .In the existing super capacitor –battery system with single DC-DC converter, the rms value of the output voltage is found to be fluctuate between 3%-4% of rated value compared to the proposed parallel topology of buck boost converter system with SC and battery. The performance of the converter and the power quality of the output voltage are improved by incorporating the PARALLEL TOPOLOGY OF BUCK-BOOST CONVERTER.

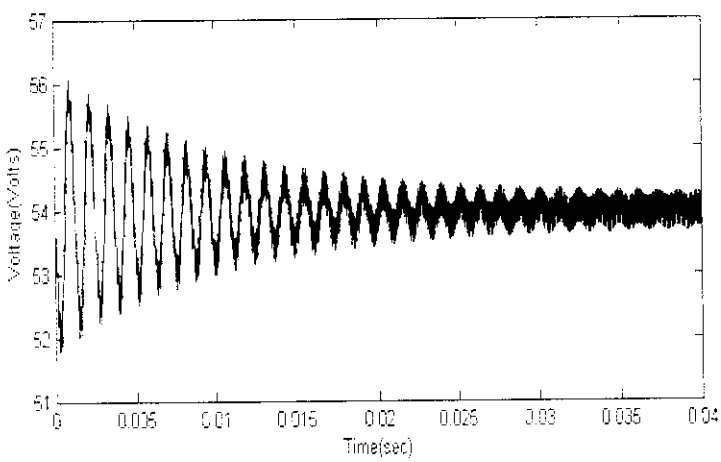

Figure.4.14 (Existing system)

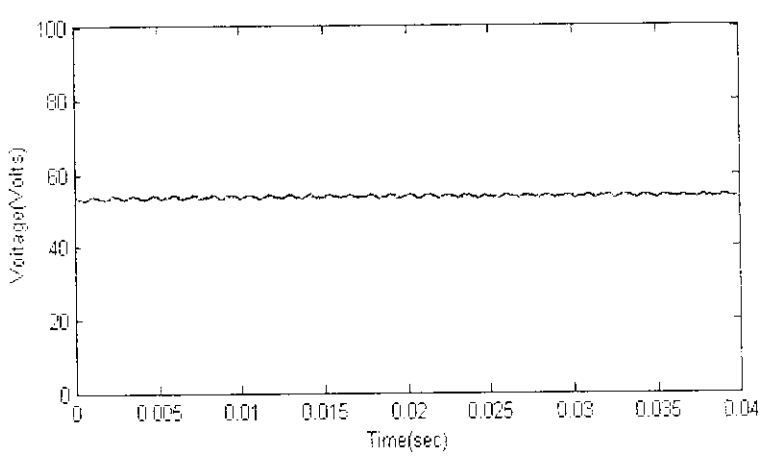

Figure.4.15 (Proposed system)

CHAPTER 5

5. HARDWARE MODEL OF PARALLEL CONNECTED SC-BATTERY SYSTEM

5.1 HARDWARE BLOCK DIAGRAM

The system was implemented using PIC 16F877 Microcontroller at the heart of its real-time control. There are three major sections that includes; a) Super capacitor module b) Buck Boost converter and c) battery system d) RL load which will be described subsequently which is shown in figure 5.1.

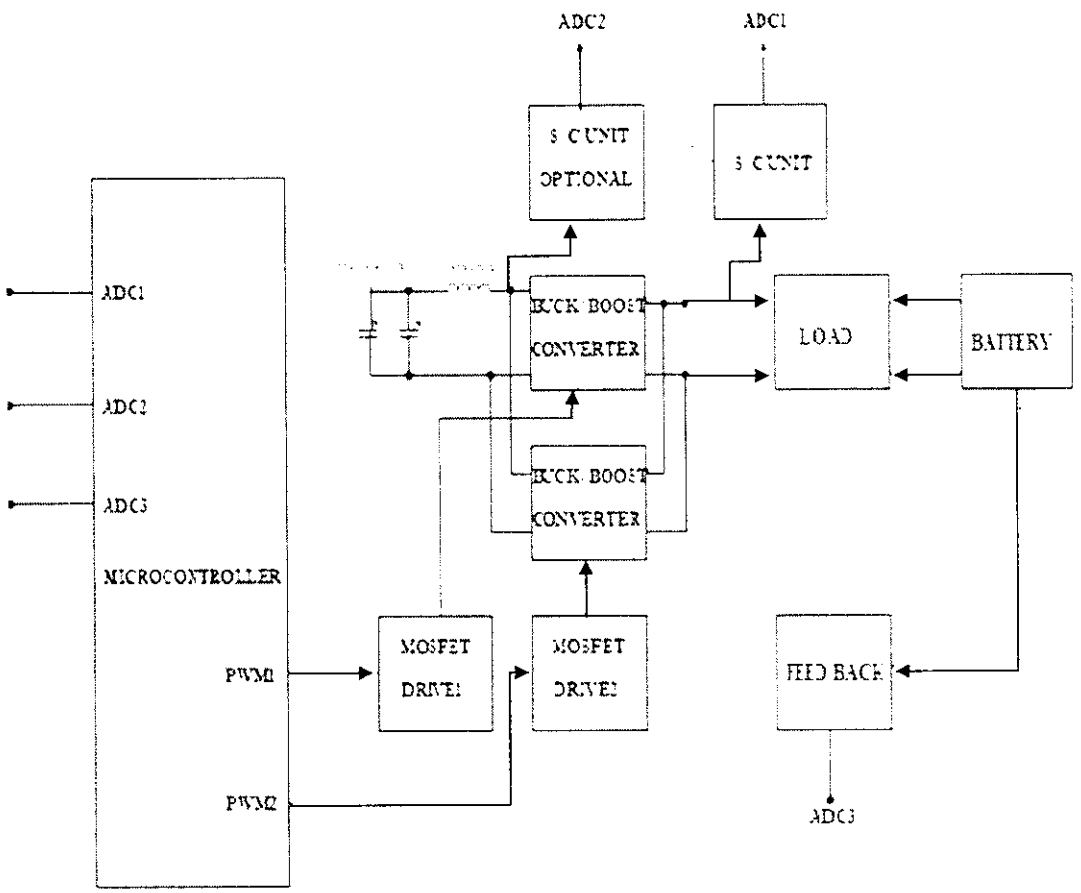

Figure 5.1 Hardware Block Diagram Super Capacitor-Battery System

This experimental test bench includes two super capacitor modules, a battery module, RL load, and dc/dc converters, which ensure energy management between the batteries and the super capacitors. The hybrid vehicle will take lot of starting current, so suddenly the battery voltage will drop from its rated voltage to below for few milliseconds. In order to avoid that we are placing some super capacitor banks. To implement the hardware for this project we have to always maintain the boost output

little below the battery voltage. For Example: battery voltage 12v (full charge) to 11v and boost voltage 10v to 9v.So if the battery voltage in full range (12v) the boost circuit will maintain 11v. if the battery voltage decreases to 10v (it will not happen suddenly in smooth running condition) booster circuit will reduce the output voltage to 9v but slowly. If any sudden drop occurs booster circuit will deliver the supply immediately to the load for few milliseconds.

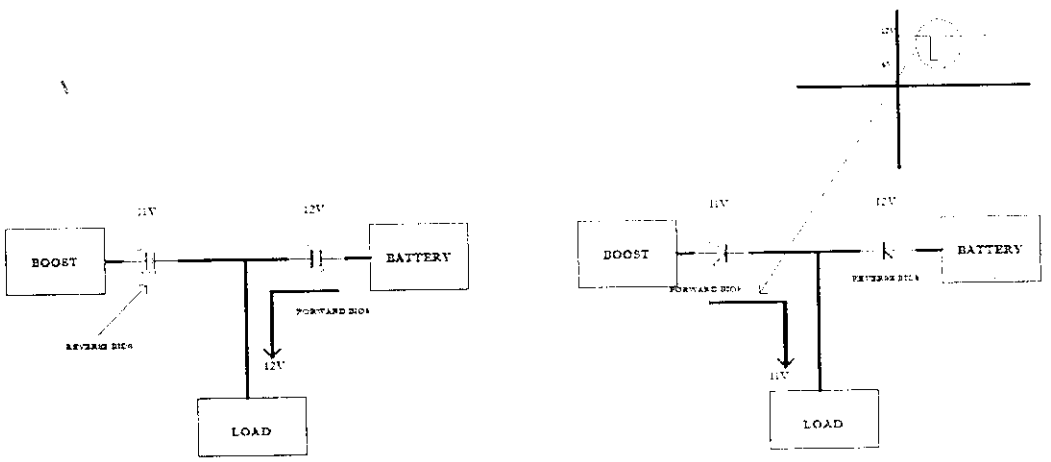

Figure 5.2 Super Capacitor-Battery System

The nonlinear load was constructed using RL circuit. The super capacitor and battery are coupled through a parallel connected dc-dc converter. The bidirectional switch uses MOSFET which is controlled using a gate drive circuit to control the power flow between super capacitor and battery in both buck and boost modes of operation to maintain the constant output voltage across the load

The digital system uses a peripheral interface controller (PIC) that contains algorithms for the operation of a subtractor, PI controller and a comparator. The voltage across battery is continuously monitored by PIC16F887 microcontroller and by using current control technique the PWM signals are generated.

5.2 SCHEMATIC DIAGRAM

5.2.1 SCHEMATIC DIAGRAM OF PARALLEL CONNECTED BUCK BOOST CONVERTER SYSTEM WITH SC AND BATTERY.

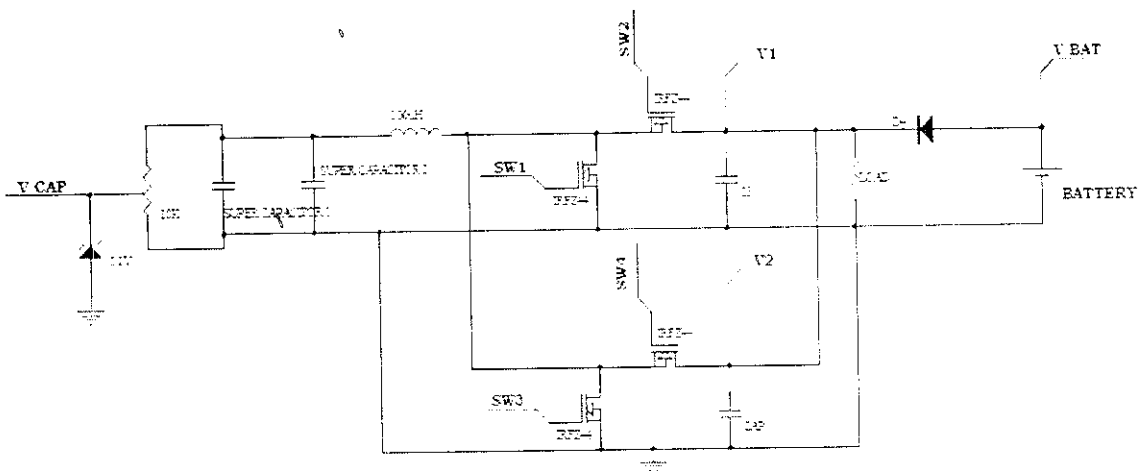

Figure 5.3 Parallel Topology of Buck-Boost Converter

Fig-6.2 shows the schematic diagram of parallel topology of buck-boost converter with super capacitor and battery.Here the super capacitor module and battery are connected through a bidirectional buck boost converter. By charging and discharging the super capacitor, the MOSFET switch is turned on and off. The operation of this system is evaluated in two modes. During normal period battery will serve the load demand. In this mode super capacitor charging and stores energy. If there is any change in load battery alone is not sufficient to meet the load demand, fast load demand will cause high voltage drop for short time. To compensate this voltage drop across load super capacitor discharges suddenly and maintains constant voltage across load.

The voltage is sensing from the battery and it is compared with the one reference signal. The zener diode is connected across the super capacitor to maintain the voltage as a constant value.

Advantages of MOSFET

- MOSFET provides much better system reliability.
- Driver circuitry is simpler and cheaper.
- MOSFET's fast switching speed permit much higher switching

frequencies and thereby the efficiency are increased.

- Overload and peak current handling capacity is high
- MOSFETs have better temperature stability
- MOSFET's leakage current is low
- Drain-source conduction threshold voltage is absent which eliminates electrical noise.

5.2.2 SCHEMATIC DIAGRAM OF DUAL POWER SUPLLY UNIT

The rectifier block contains a step down transformer, which step downs the input voltage from 220V to 12V. In addition, the step downed voltage is rectified to DC. This is done by uncontrolled single phase diode rectifier. The output of this block is 12V dc. Then this 12V dc is stepped down into 5V and is given to the PIC microcontroller.

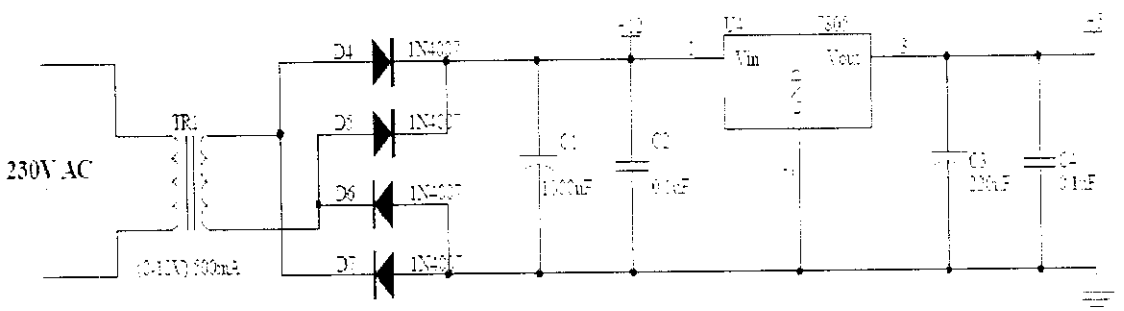

Figure 5.4 Schematic Of Dual Power Supply Unit

5.2.3 SCEMATIC OF MICRO CONTROLLER

The gate pulse for the converter switches are is generated by PIC16F877A controller. This micro controller circuit works in 5V power supply. So a separate step down rectifier unit is made for the controller. The detail about PIC16F877A is given in APPENDIX I. This controller is isolated from the main circuits by means of opto-coupler. The schematic of micro-controller circuit is show in fig-6.5.

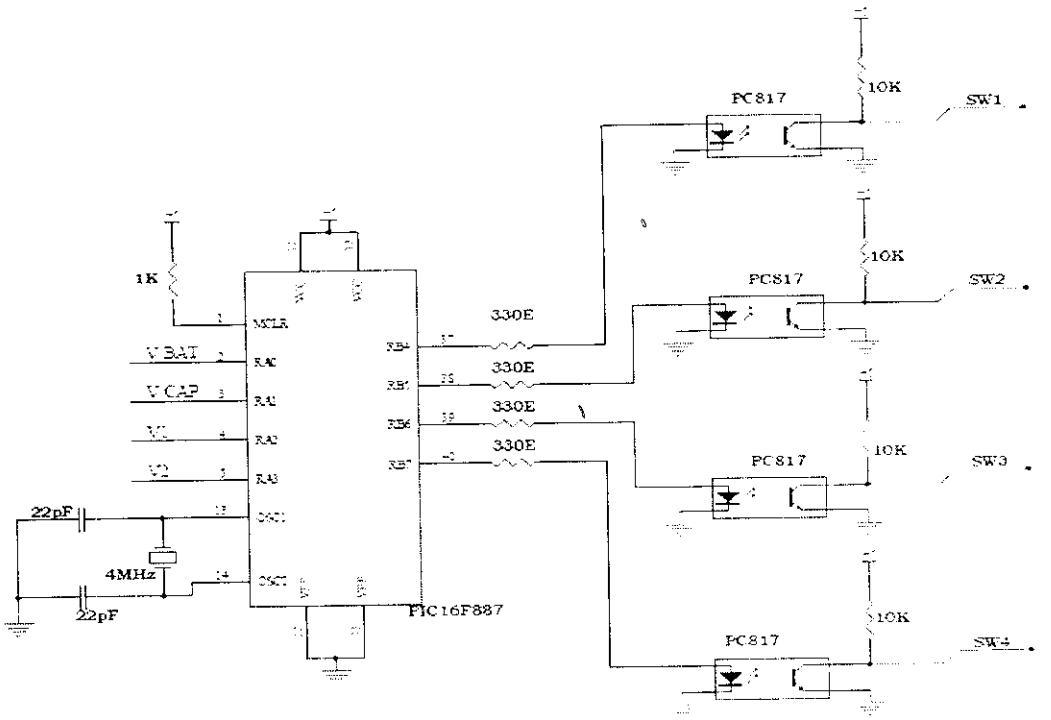

Figure 5.5 Schematic Of Micro Controller Unit

Features of PIC16F887

High-Performance RISC CPU

- Only 35 single word instructions to learn
- Operating speed: DC - 20MHz clock input.
- All single-cycle instructions except branches

Peripheral Features:

- 36 I/O pins
- High sink/source current 25 mA
- Interrupt-on-pin change option
- Two 8-bit timer/counter (TMR0, TMR2) with 8-bit programmable prescalar.
- Two Capture/Compare PWM (CCP) Modules.

Special Micro controller Features

- Power-Saving Sleep mode
- Power-on Reset (POR)
- Selectable Brown-out Reset (BOR) voltage
- Extended Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Master Synchronous Serial Port (MSSP)
- High-endurance Flash/EEPROM cell
- Self-reprogrammable under software control
- Programmable code protection.
- 10-bit 14 channel Analog-to-Digital (A/D) Converter
- PWM output steering control.
- 368 bytes RAM memory
- 256 bytes EEPROM memory
- Analogue comparator module with
    - Two analogue comparators
    - Fixed voltage reference (0.6V)
    - Programmable on-chip voltage reference

Optocoupler:

Optocoupler is also termed as optoisolator. Optoisolator a device which contains a optical emitter, such as an LED, neon bulb, or incandescent bulb, and an optical receiving element, such as a resistor that changes resistance with variations in light intensity, or a transistor, diode, or other device that conducts differently when in the presence of light. These devices are used to isolate the control voltage from the controlled circuit.

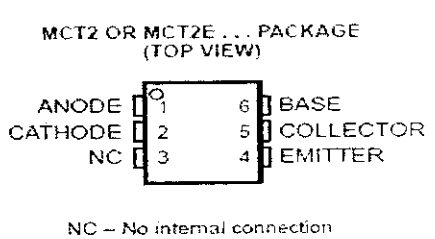

Figure.5.5 Optocoupler

- Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor
- High Direct-Current Transfer Ratio
- Base Lead Provided for Conventional Transistor Biasing
- High-Voltage Electrical Isolation . . .
- 1.5-kV, or 3.55-kV Rating
- Plastic Dual-In-Line Package
- High-Speed Switching:

5.3 HARDWARE TESTING AND RESULTS

The test bench of this topology includes a super capacitor module (SC) with 2 .9 V , a battery , a buck–boost converter, a dc-bus filtering capacitor ($C2$), a super capacitor current smoothing inductance (L), and the second inductance for the battery current smoothing (λ). The system is controlled by a PIC16F887 microcontroller.

The fabricated hardware model is as shown in fig.5.6. The output waveform of the boost converter is shown in the figure 5.7. The control pulses for the boost mode operation is shown in figure 5.8 and thus voltage across the load remains constant.

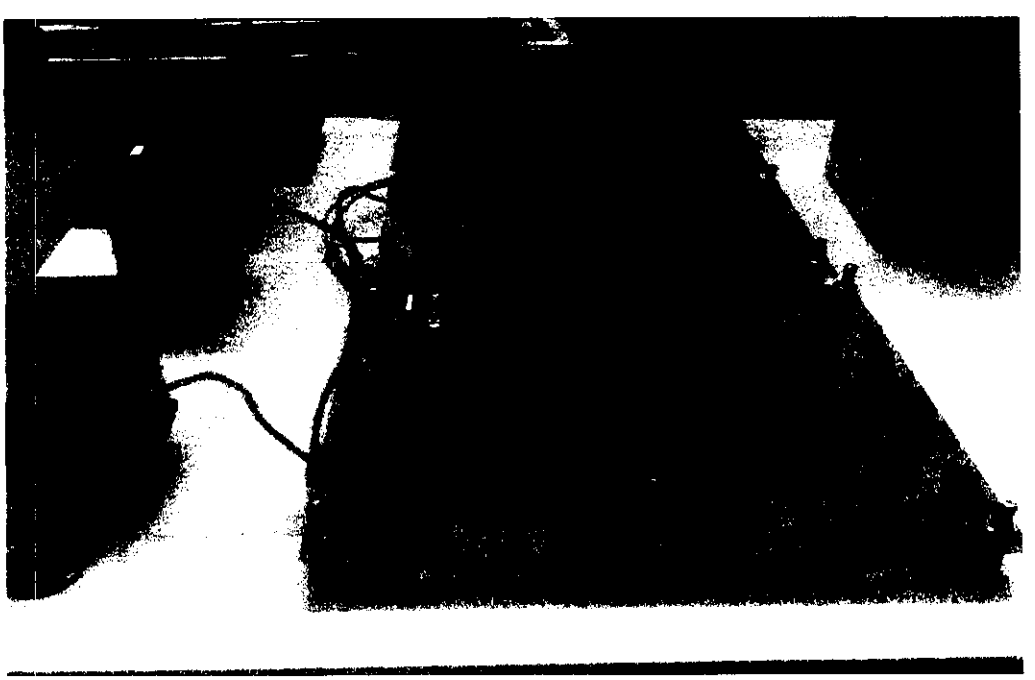

Figure.5.6 Prototype Photo

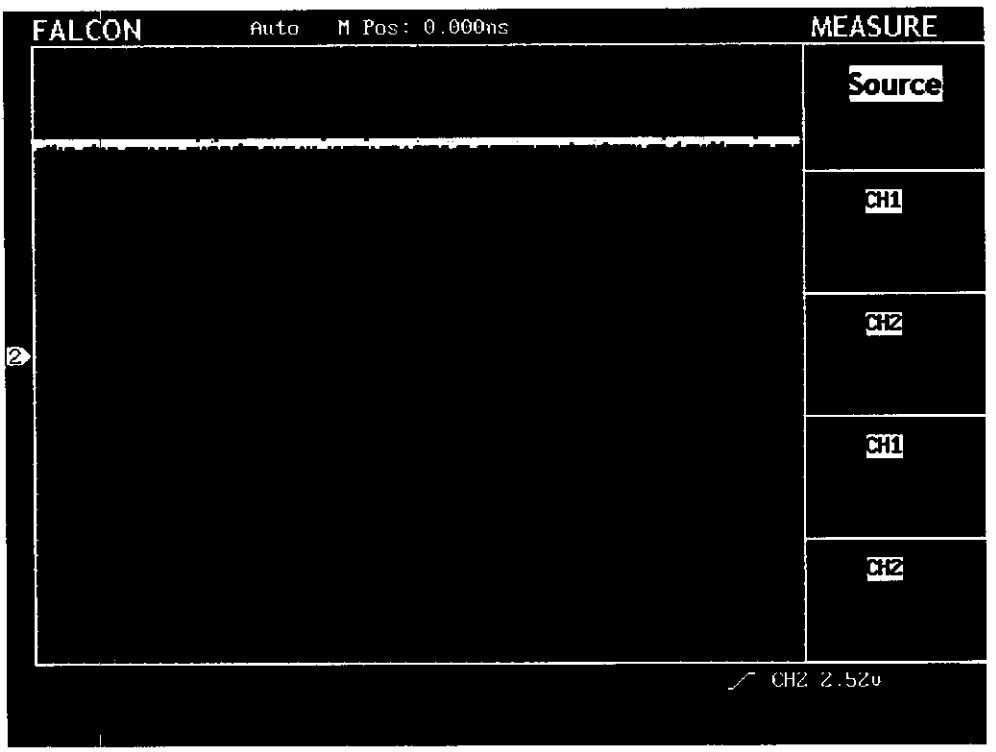

Figure.5.7 Output Voltage

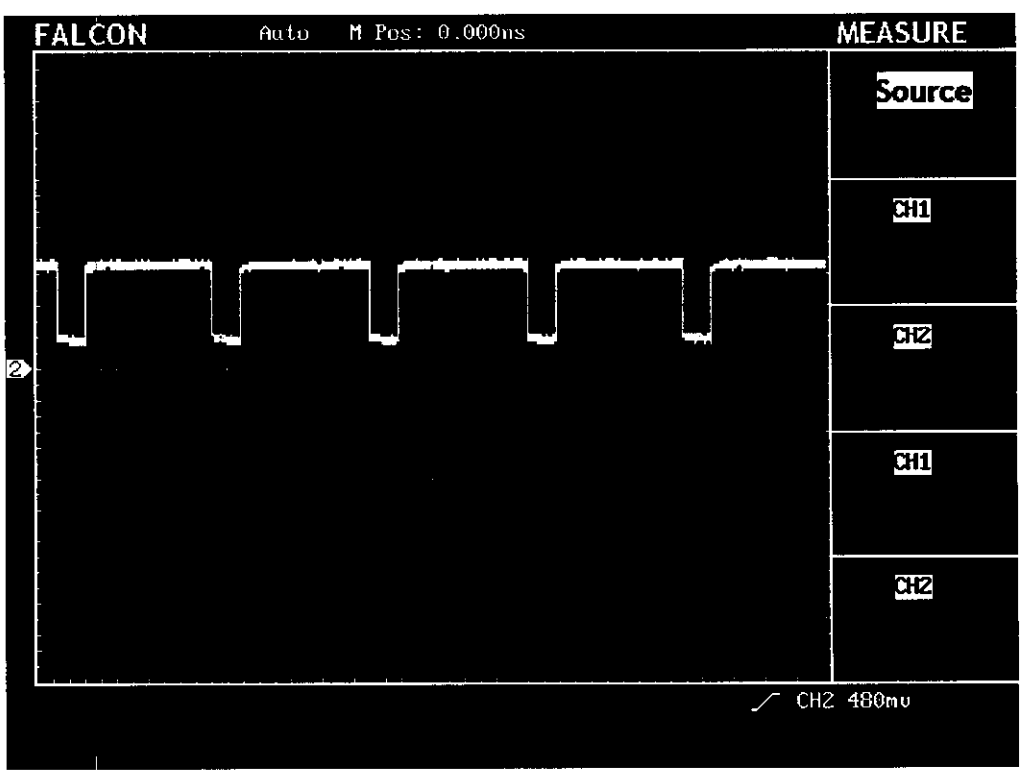

Figure.5.8 PWM For Boost Operation

CHAPTER 6

6. CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

An efficient power system combining batteries and super capacitors for hybrid vehicle system has been presented. The purpose of this strategic energy management is to share the power demand between the battery and super capacitors pack. It is observed that super capacitor can be charged up to required voltage level during boost operation and also it can successfully deliver energy to the load during buck operation. Therefore, despite the wide variations of the super capacitor terminal voltage, the voltage across the load remains constant. The simulation of both the existing and proposed systems is done using MATLAB/ SIMULINK software and the results of the proposed technique are verified through prototype model.

6.2 FUTURE SCOPE

The proposed system could be developed for a perfect energy management between battery and super capacitor, for modern distributed generation system, particularly for future fuel cell vehicle applications.

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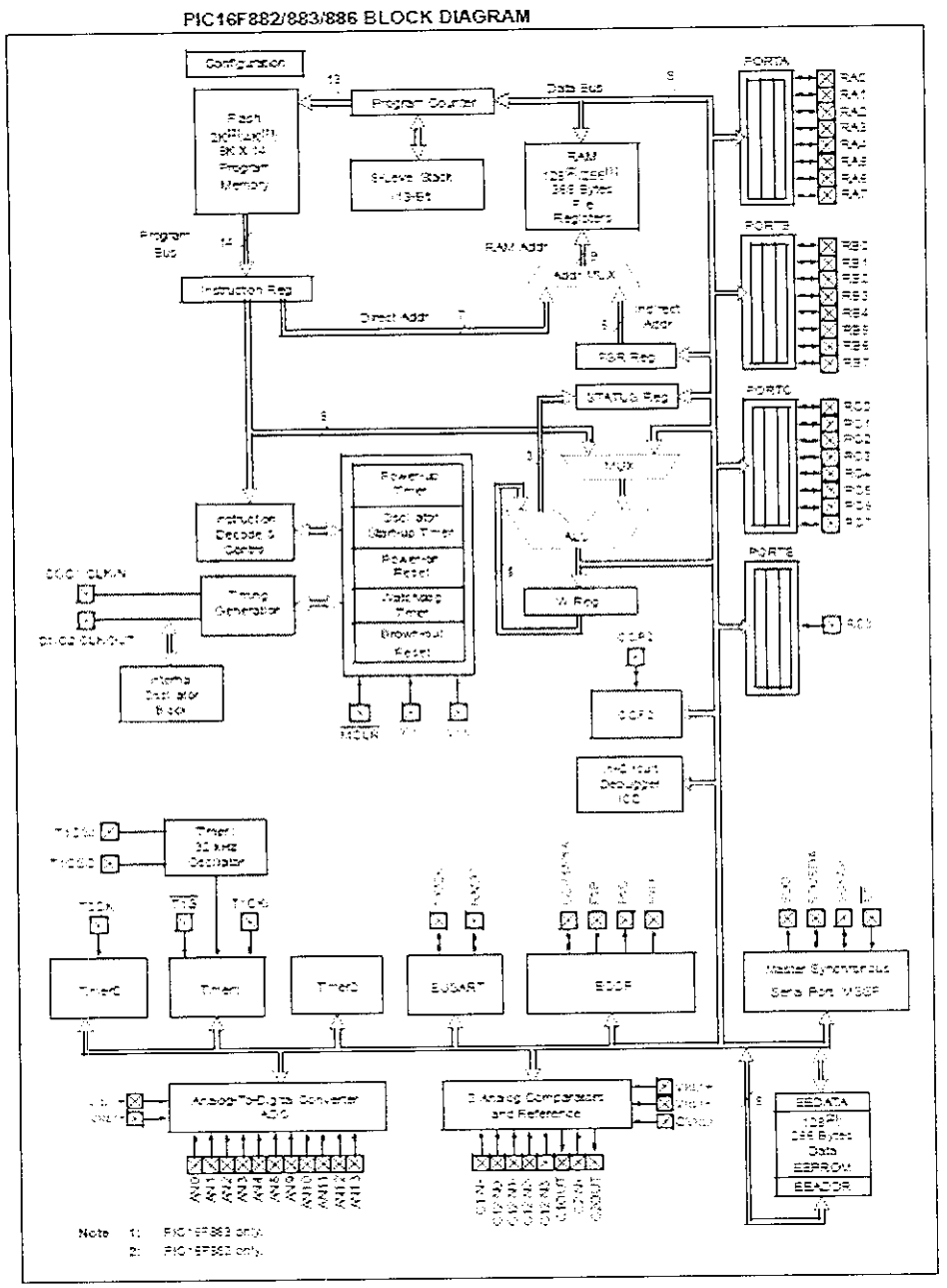
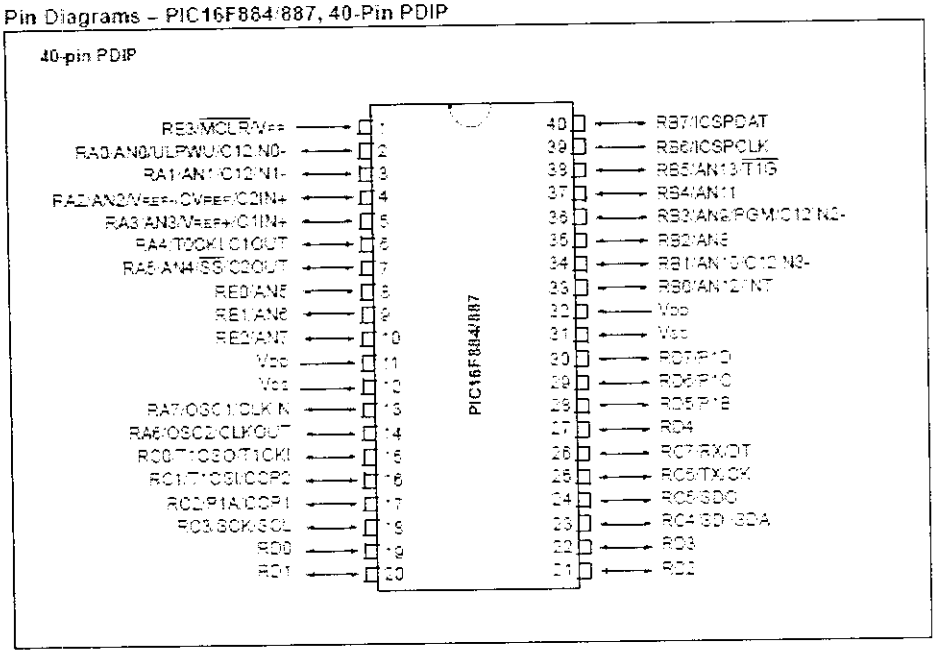
APPEDIX-I

ARCHITECTURE OF PIC 16F887

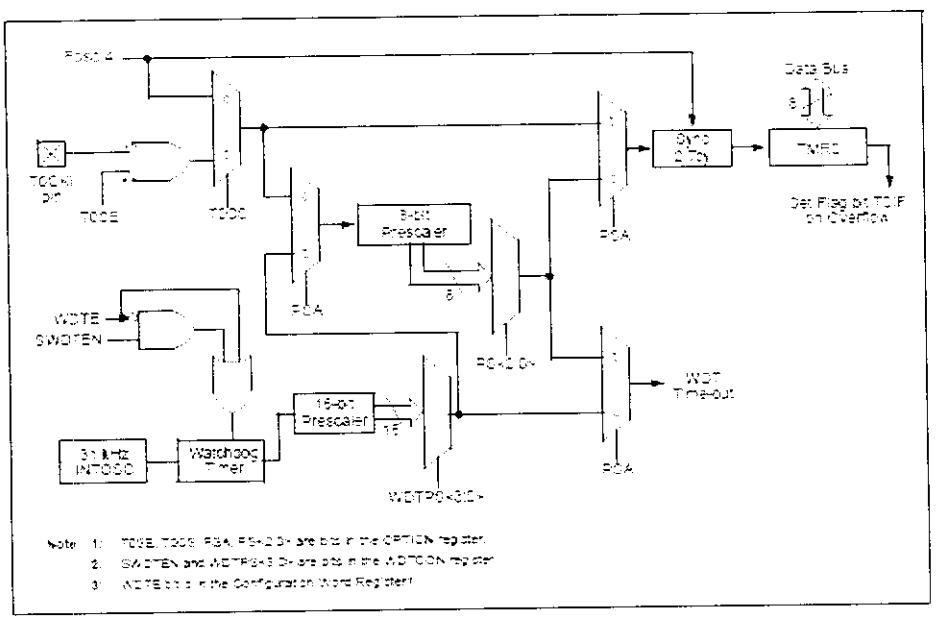


Pin Configuration of PIC16F877A

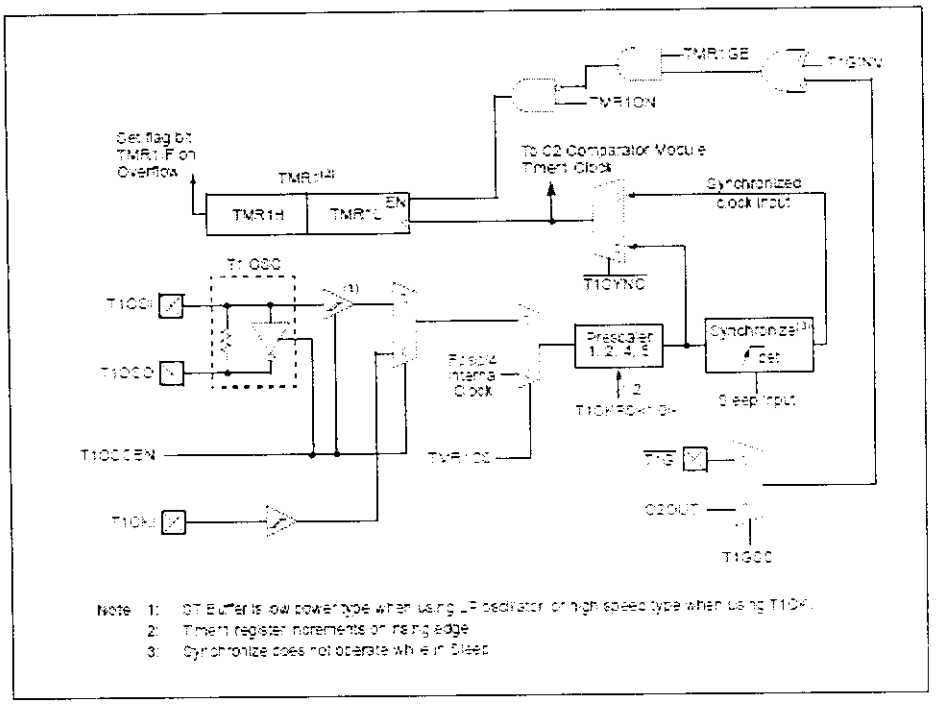
Pin Diagrams – PIC16F884/887, 40-Pin PDIP



TIMERS 0 BLOCK DIAGRAM:

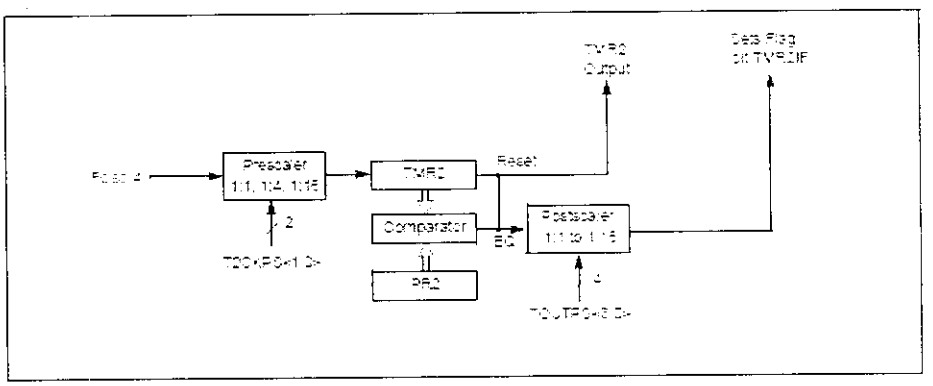


TIMER 1 BLOCK DIAGRAM:

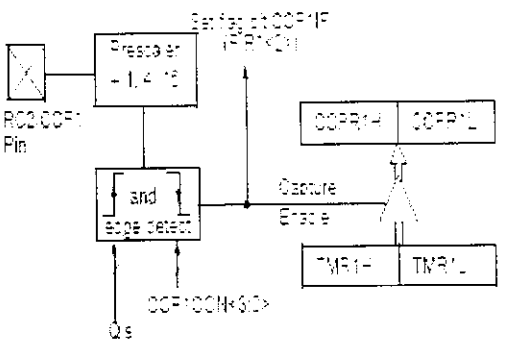


Note 1: GT Buffer is low power type when using LP oscillator or high speed type when using T1OSC.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

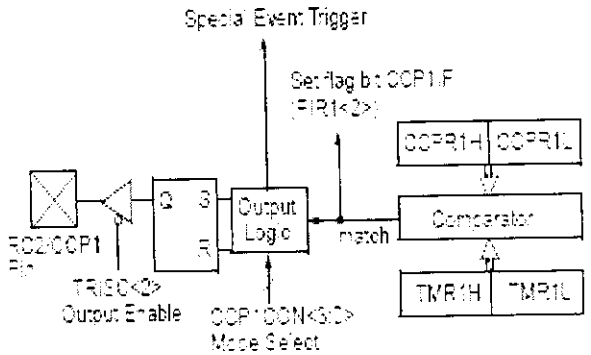
TIMER 1 BLOCK DIAGRAM:



CAPTURE MODE OPERATION BLOCK DIAGRAM:



COMPARE MODE OPERATION BLOCK DIAGRAM:



FEATURES OF PIC:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- Operating speed: DC - 20 MHz clock input
- Precision Internal Oscillator:
  - Factory calibrated to ±1%
  - Software selectable frequency range of
  - 8 MHz to 32 kHz
  - Software tunable
  - Two-Speed Start-Up mode
  - Fail-safe clock monitoring for critical applications
  - Clock mode switching during operation for low-power operation

  Power-Saving Sleep mode
- Power-on Reset (POR)
- Selectable Brown-out Reset (BOR) voltage
- Extended Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- High-endurance Flash/EEPROM cell:
  - 100,000 erase/write cycle enhanced Flash program memory, typical
  - 1,000,000 erase/write cycle data EEPROM memory, typical

- Data EEPROM retention > 40 years

- Self-reprogrammable under software control
- Programmable code protection
- Peripheral Features:
- Timers:
  - TMR0: 8-bit timer/counter with 8-bit prescalar
  - TMR1 enhanced: 16-bit timer/counter with prescalar,
  - External Gate Input mode and dedicated low- power 32kHz oscillator
  - TMR2: 8-bit timer/counter with 8-bit period register, prescalar and postscalar
- Capture/Compare/PWM (CCP) module
- Enhanced Capture/Compare/PWM (ECCP) module with auto-shutdown and PWM steering
- Master Synchronous Serial Port (MSSP) module SPI™ mode. I2C™ mode with address mask capability
- Enhanced Universal Synchronous Asynchronous
  - Receiver Transmitter (EUSART) module:
  - Supports RS-485, RS-232 and LIN compatibility
  - Auto-Baud Detect
  - Auto-wake-up on Start bit
- Ultra Low-Power Wake-up (ULPWU)
- Analog Features:
  - 10-bit 14 channel Analog-to-Digital (A/D) Converter
- Analog Comparator modules with:
  - Programmable on-chip Voltage Reference
  - (CVREF) module (% of VDD)
  - Fixed 0.6 Vref
  - Comparator inputs and outputs externally accessible
  - SR Latch mode

APPENDIX II

PIC PROGRAMMING

```
#include<pic.h>
__CONFIG(0X20E4);
__CONFIG(0X3FFF);


unsigned int REFF1,INPUT1,REFF2,INPUT2;
unsigned char count;

delay(void);
delay1(void);

void main()
{
        TRISC=0;
        PORTC=0;

        TRISA=0XFF;

        ANSEL=0X0F;
        ANSELH=0;
        ADCON1=0X80;

        PR2=99;
        T2CON=0X04;


        CCP1CON=0X0F;
        CCPR1L=25;

        CCP2CON=0X0C;
        CCPR2L=75;

        while(1)
        {
/****************** ADC SCAN *****************/
                ADCON0=0X81;      // adc AN0
                delay();
                GODONE=1;
                while(GODONE);
                REFF1=(ADRESH*256)+ADRESL;


                ADCON0=0X89;      // adc AN1
                delay();
                GODONE=1;
                while(GODONE);
```

```
                REFF2=(ADRESH*256)+ADRESL;


    /****************** ADC SCAN END ********************/

    /******************  PWM LIMIT  ********************/

                        if(CCPR1L<30)
                                CCPR1L=30;
                        if(CCPR1L>85)
                                CCPR1L=85;

                        if(CCPR2L<30)
                                CCPR2L=30;
                        if(CCPR2L>85)
                                CCPR2L=85;

    /************** OUTPUT REGULATION*****************/

                        delay1();
                        if(REFF1>600)
                                CCPR1L--;
                        delay();
                        if(REFF1<600)
                                CCPR1L++;
                        delay1();

                        delay1();
                        if(REFF2>600)
                                CCPR2L++;
                        delay();
                        if(REFF2<600)
                                CCPR2L--;
                        delay1();

                }
        }
        delay()

        {
                unsigned int i;
                for(i=0;i<100;i++);
        }
        delay1()
        {
                unsigned int j;
                for(j=0;j<10000;j++);
        }
```

APPENDIX-III

Advanced Power MOSFET — IRFZ44

FEATURES

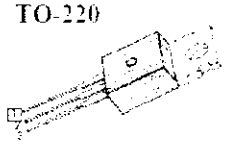
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current: 10μA (Max.) @ V_{DS} = 60V
- Lower $R_{DS(ON)}$: 0.020Ω (Typ.)

BV_{DSS} = 60 V

$R_{DS(on)}$ = 0.024Ω

I_D = 50 A

TO-220



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current (T_C=25°C)	50	A
	Continuous Drain Current (T_C=100°C)	35.4	
I_{DM}	Drain Current-Pulsed (1)	200	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy (2)	657	mJ
I_{AR}	Avalanche Current (1)	50	A
E_{AR}	Repetitive Avalanche Energy (1)	12.6	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	5.5	V/ns
P_D	Total Power Dissipation (T_C=25°C)	126	W
	Linear Derating Factor	0.84	W/°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
R_{thJC}	Junction-to-Case	--	1.19	°C/W
R_{thCS}	Case-to-Sink	0.5	--	
R_{thJA}	Junction-to-Ambient	--	62.5	

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	60	--	--	V	V_{GS}=0V, I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.063	--	V/°C	I_D=250μA *See Fig 7*
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V, I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-20V
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V_{DS}=60V
		--	--	100		V_{DS}=48V, T_C=150°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.024	Ω	V_{GS}=10V, I_D=25A (4)
g_{fs}	Forward Transconductance	--	32.6	--	Ω	V_{DS}=30V, I_D=25A (4)
C_{iss}	Input Capacitance	--	1770	2300	pF	V_{GS}=0V, V_{DS}=25V, f =1MHz *See Fig 5*
C_{oss}	Output Capacitance	--	590	680		
C_{rss}	Reverse Transfer Capacitance	--	220	255		
$t_{d(on)}$	Turn-On Delay Time	--	20	40	ns	V_{DD}=30V, I_D=50A, R_G=9.1Ω *See Fig 13* (4)(5)
t_r	Rise Time	--	16	40		
$t_{d(off)}$	Turn-Off Delay Time	--	68	140		
t_f	Fall Time	--	70	140		
Q_g	Total Gate Charge	--	64	83	nC	V_{DS}=48V, V_{GS}=10V, I_D=50A *See Fig 6 & Fig 12* (4)(5)
Q_{gs}	Gate-Source Charge	--	12.3	--		
Q_{gd}	Gate-Drain (Miller.) Charge	--	23.6	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	50	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current (1)	--	--	200		
V_{SD}	Diode Forward Voltage (4)	--	--	1.8	V	T_J=25°C, I_S=50A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	85	--	ns	T_J=25°C, I_F=50A
Q_{rr}	Reverse Recovery Charge	--	0.24	--	μC	di_F/dt=100A/μs (4)

Notes:

(1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

(2) L=0.4mH, I_{AS}=50A, V_{DD}=25V, R_G=27Ω, Starting T_J=25°C

(3) I_{SD}≤ 50A, di/dt ≤ 350A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C

(4) Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%

(5) Essentially Independent of Operating Temperature

MC78XX/LM78XX

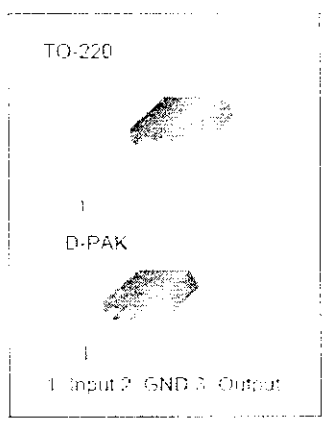
3-terminal 1A positive voltage regulator

Features

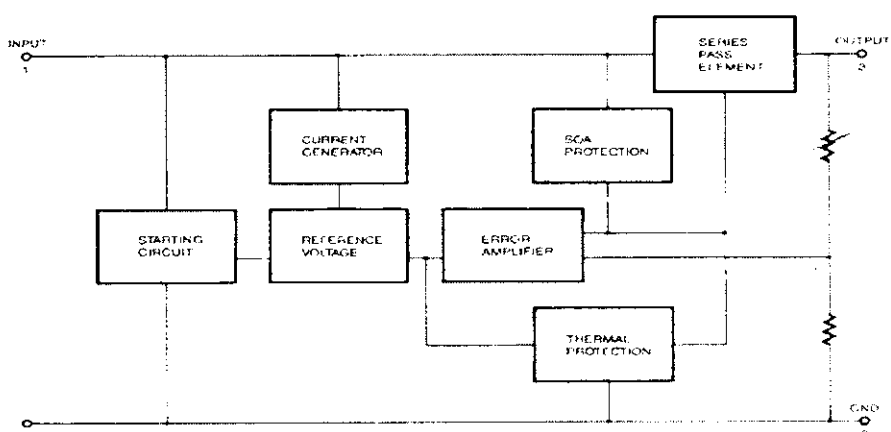
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 11, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating area Protection

Description

The MC78XX/LM78XX series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Digram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C/W
Operating Temperature Range (MC78XXCT/LM78XXCT/MC78XXCDT)	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ Io ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V V_I = 8V to 20V		4.75	5.0	5.25	
Line Regulation	ΔV_O	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation	ΔV_O	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	μV
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_O	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	R_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

• Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806)

(Refer to test circuit ,0°C < T_J < +125°C, I_O = 500mA, V_I = 11V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7806			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		5.75	6.0	6.25	V
		5.0mA ≤ I_O ≤ 1.0A, P_D ≤ 15W V_I = 8.0V to 21V V_I = 9.0V to 21V		5.7	6.0	6.3	
Line Regulation	ΔV_O	T_J =+25 °C	V_I = 8V to 25V	-	5	120	mV
			V_I = 9V to 13V	-	1.5	60	
Load Regulation	ΔV_O	T_J =+25 °C	I_O =5mA to 1.5A	-	9	120	mV
			I_O =250mA to750A	-	3	60	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 8V to 25V		-	-	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-0.8	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C		-	45	-	μV
Ripple Rejection	RR	f = 120Hz V_I = 9V to 19V		59	75	-	dB
Dropout Voltage	V_O	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	R_O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A=+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41

COLOR BAND DENOTES CATHODE

General Purpose Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_R	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							µA µA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Typical Characteristics

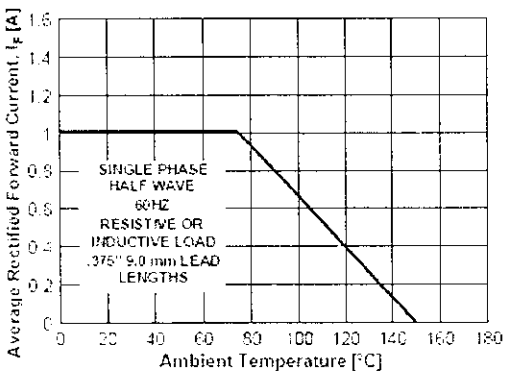


Figure 1. Forward Current Derating Curve

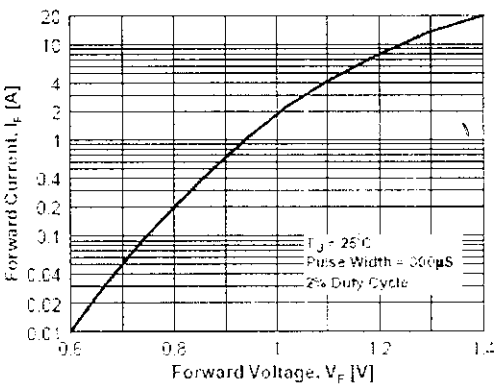


Figure 2. Forward Voltage Characteristics

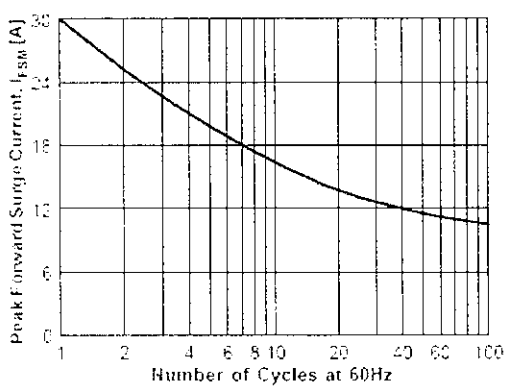


Figure 3. Non-Repetitive Surge Current

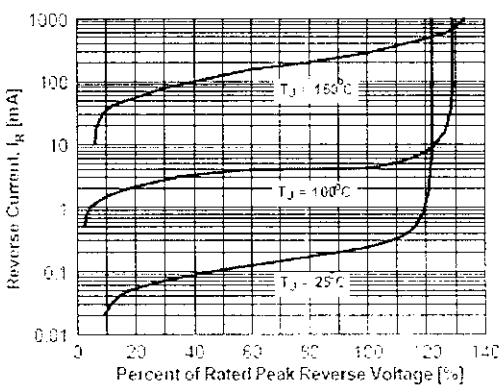


Figure 4. Reverse Current vs Reverse Voltage