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Implementation of Inverted Sine Carrier for Fortification in Asymmetric Cascaded Seven Level Inverter

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A Project Report

Submitted by

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BONAFIDE CERTIFICATE

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CONTENTS

ABSTRACT

Multilevel inverter (MLI) is a new breed of power converter that is suited for high power applications. Multilevel inverter is an effective and practical solution for increasing power and reducing harmonics in ac waveforms. The various topologies of multilevel inverter are diode-clamped, capacitor clamped and cascaded H bridge inverter. Among the three, cascaded multilevel inverter is the most widely used topology. This paper focuses on the implementation of inverted sine PWM technique for asymmetric cascaded multilevel inverter with unequal DC sources. This technique combines the advantage of inverted sine PWM technique and asymmetric cascaded multilevel inverter with unequal DC sources. Performance evaluation of the proposed PWM strategy and inverter topology is done using MATLAB/SIMULINK for both single and three phase asymmetric multilevel inverter. For a seven level output, the proposed inverter topology comprises of two H bridges and two DC sources which is of unequal in nature is simulated using MATLAB. With the implementation of Inverted Sine Carrier Pulse-Width Modulation (ISCPWM) technique there exists an enhancement in fundamental output voltage along with the reduction in Total Harmonic Distortion. The prototype model is also designed, fabricated and tested.

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ABREVIATIONS

AC	-	Alternating Current
DC	-	Direct Current
PWM	-	Pulse Width Modulation
THD	-	Total Harmonic Distortion
MLI	-	Multi-Level Inverter
SHE	-	Selective Harmonic Elimination
SVM	-	Space Vector Modulation
SPWM	-	Sinusoidal Pulse Width Modulation
ISPWM	-	Inverted Sine Pulse Width Modulation
VFISPWM	-	Variable Frequency Inverted Sine Pulse Width Modulation
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
IGBT	-	Insulated Gate Bipolar Transistor

LIST OF SYMBOLS

f_r	-	Frequency of reference wave
f_c	-	Frequency of carrier wave
m_f	-	Frequency Modulation ratio
N_p	-	Number of pulses per cycle
A_r	-	Amplitude of reference wave
A_c	-	Amplitude of carrier wave
V_s	-	Source Voltage

CHAPTER 1

CHAPTER 1
INTRODUCTION

1.1 NEED FOR THE PROJECT:

Implementation of Inverted Sine Pulse Width Modulation (ISPWM) technique for fortifying an Asymmetric Cascaded 7 level inverter using two H- Bridges, as ISPWM technique reduces Total Harmonic Distortion (THD) and also enhances the fundamental output voltage.

1.2 OBJECTIVE OF THE PROJECT:

The aim of this project is

- To design and simulate single and three phase Asymmetric Cascaded 7 level inverter with two H- Bridges
- To generate switching pulses for the cascaded H Bridge 7 level inverter by comparing Unipolar Inverted Sine wave of high switching frequency with that of the reference wave.
- To implement Phase Disposition multi-carrier technique with carriers of same frequency and of same amplitude.
- To evaluate the performance of seven level output based on Total Harmonic Distortion (THD) and Fundamental Output Voltage in comparison with conventional PWM technique.
- Further evaluation in the performance of seven level output is carried out by implementing Variable Frequency Inverted Sine PWM(VFISPWM) based on Total Harmonic Distortion (THD) in comparison with Unipolar ISPWM technique.

1.3 ORGANISATION OF THE THESIS:

Chapter 1 deals with the introduction to the project.

Chapter 2 deals with overview of Multilevel Inverter

Chapter 3 gives the overview on Conventional modulation Strategies of MLI

Chapter 4 deals about Inverted Sine Wave Pulse Width Modulation (ISPWM)

Chapter 5 deals with Conventional Cascaded MLI employing proposed ISCPWM Technique

Chapter 6 deals with Asymmetric Cascaded MLI

Chapter 7 deals with Asymmetric Cascaded employing proposed ISCPWM Technique

Chapter 8 deals with the hardware implementation.

Chapter 9 gives the conclusion of the project

CHAPTER 2

CHAPTER 2
MULTILEVEL INVERTER

2.1 INTRODUCTION:

Multilevel inverter synthesizes a desired voltage from several levels of dc voltages with low harmonics. As the number of levels increases, the harmonic distortion of the output wave decreases. Further, for reducing harmonics, PWM or space vector modulation is used. It gives complexity in switching frequency in operation. Another approach is to find the switching angles in order to eliminate the specified harmonics. The mathematical theory of resultant is used to compute optimum switching angle.

The multilevel inverters have drawn tremendous interest in the power industry. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to the multilevel inverter system for a high power application. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

2.1.2 FEATURES OF MULTILEVEL INVERTERS:

Multi-level inverters have been attracting increasing interest recently, particularly because of their increased power rating, improved harmonic performance and reduced EMI emission. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM).

The attractive features of a multilevel converter can be briefly summarized as follows.

- Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore Electro Magnetic Compatibility (EMC) problems can be reduced.
- Common-Mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, using advanced modulation strategies eliminate CM voltage.
- Input current: Multilevel converters can draw input current with low distortion.
- Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Compared to conventional two level inverters, multilevel inverters have advantages of:

- Improved output voltage waveform,
- Reduced output voltage harmonic contents under the same switching frequency byintroducing several voltage levels at output,
- Reduced voltage stress on the switching semiconductors,
- Decreased Electromagnetic Interference (EMI) problems.

2.2 TYPES OF MULTILEVEL INVERTERS:

The multilevel inverters can be classified into three types:

A) Diode-clamped multilevel inverters

B) Flying-capacitors multilevel inverters

C) Cascaded multilevel inverter.

Among these inverter topologies, the flying capacitor inverter is difficult to realize because each capacitor must be charged with different voltages as the voltage level increases. Moreover, the diode-clamped inverter is difficult to expand to multilevel because of the natural problem of the dc link voltage unbalancing, the increase in the number of clamping diodes, and the difficulty of the disposition between the dc link capacitors and the devices as the voltage increases. Though the cascaded inverter has the disadvantage of needing separate dc sources, the modularized circuit layout and package are possible, and the problem of the dc link voltage

unbalancing is not occurred. Therefore it is easily expanded to multilevel. Because of these the cascaded inverter bridge has been widely applied to such areas as HVDC, SVC, stabilizers, and high-power motor drives.

2.3 CONVENTIONAL CASCADED MULTILEVEL INVERTER

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$M=2s+1$$

Where's' is the number of dc sources. Separate DC source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter.

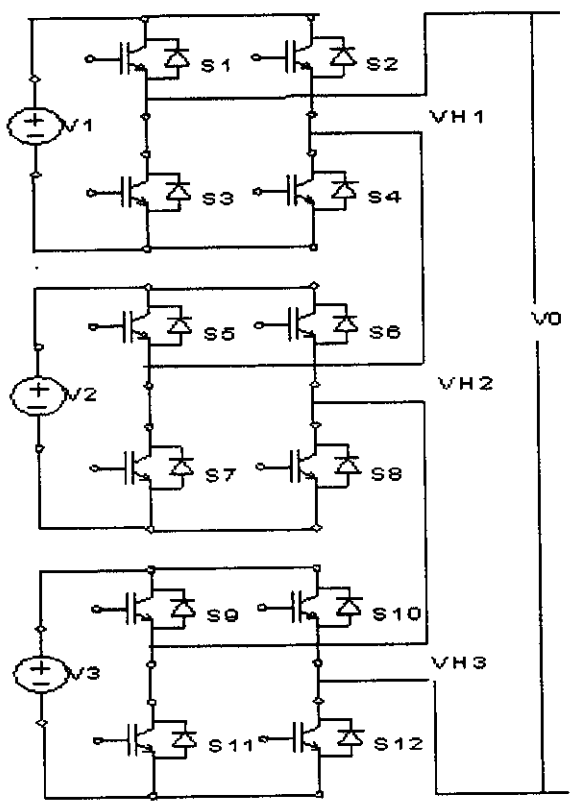


Fig.2.1 Conventional Cascaded Seven Level Inverter

The basic seven-level cascaded-cell inverter is shown in Fig.2.1.This circuit features three conventional full-bridges serially connected together with their power rails connected to separate isolated dc voltage supplies. Each full-bridge inverter cell can apply three voltage levels to the load terminals. Complementary pairs of switches are turned in each H Bridge in order to avoid shoot-through condition. By opening and closing of the first bridge appropriately the output voltage V_{H1} can be made equal to $-V_1$, 0, or $+V_1$ while the output voltage of the second bridge V_{H2} can be made equal to $-V_2$, 0 or + V_2 and that for the third bridge V_{H3}, the output voltage can be made equal to $-V_3$, 0 or + V_3. Therefore the output voltage of the converter is a combination of V_1, V_2 and V_3 that has seven possible values 0, + V_1, (+ V_1+V_2), (V_1+V_2+V_3), -V_1, (-V_1-V_2), (-V_1-V_2-V_3).

The voltage level of the inverter can be increased in multiples of two by adding additional bridge inverter cells to each phase limb. The cascaded inverter uses the least number of power components, but requires separate isolated power sources for each inverter cell. This would normally entail using a large isolation transformer. However, the topology does look attractive for power conditioning applications where the separate dc supplies can be self-powered in the converter.

2.3. 1 ADVANTAGES OF CONVENTIONAL CASCADED INVERTER

- It requires reduced no. of switches for same level output voltages
- It reduces dv/dt stresses on power switching devices resulting in low audio and RF noise.
- The output voltage is compatible with the load. Hence output transformer is not needed.
- The power circuit is designed to have modular structure.
- During faulty conditions, the faulty H-Bridge unit can be bypassed and taken out for maintenance and the inverter can still be used with reduced power rating.
- Reqiures least number of components among all multilevel inverters to achieve the same number of voltage levels.
- Soft switching can be used in this structure to avoid bulky resistor-capacitor snubbers

CHAPTER 3

CHAPTER 3

CONVENTIONAL MODULATION STRATEGIES FOR MULTILEVEL INVERTER

3.1 INTRODUCTION TO MODULATION STRATEGIES:

Several modulation techniques have been proposed for cascaded multilevel inverters. A high number of power electronic devices and switching redundancies bring a higher level of complexity compared with a two-level inverter counterpart. However, this complexity could be used to add additional capabilities to the modulation technique, namely, reducing the switching frequency, minimizing the common-mode voltage, or balancing the dc voltages.

Modulation techniques for cascaded multilevel inverters are usually an extension of the two-level modulations. According to their switching frequency, they can be classified as follows:

- Multistep, staircase or fundamental frequency switching strategies.
- Space Vector Control strategy.
- Carrier based PWM strategies.

3.2 FUNDAMENTAL SWITCHING FREQUNENCY:

Fundamental frequency switching techniques can be applied to cascaded multilevel inverters using two approaches. The first one is to consider one commutation angle per inverter; thus, the number of harmonics that can be eliminated is $N_{inv} - 1$. In multistep, staircase or fundamental frequency switching strategies, which synthesise the AC voltage by adding rectangular waveforms by means of the multilevel concept, uses pre-calculated switching angles. In the fundamental switching scheme, the switching angles are calculated and later they are transferred to a digital system. This technique eliminates low order harmonics in order to reduce the distortion in the output voltage.

The switching pattern of fundamental switching frequency (multilevel Selective Harmonic Elimination (SHE)) can be obtained by solving a set of equations, based on the number of levels. Numeric mathematical methods such as Newton, resultant theory and genetic algorithms are used for solving the obtained equations.

The typical waveform obtained by this technique is shown in Fig. 3.1

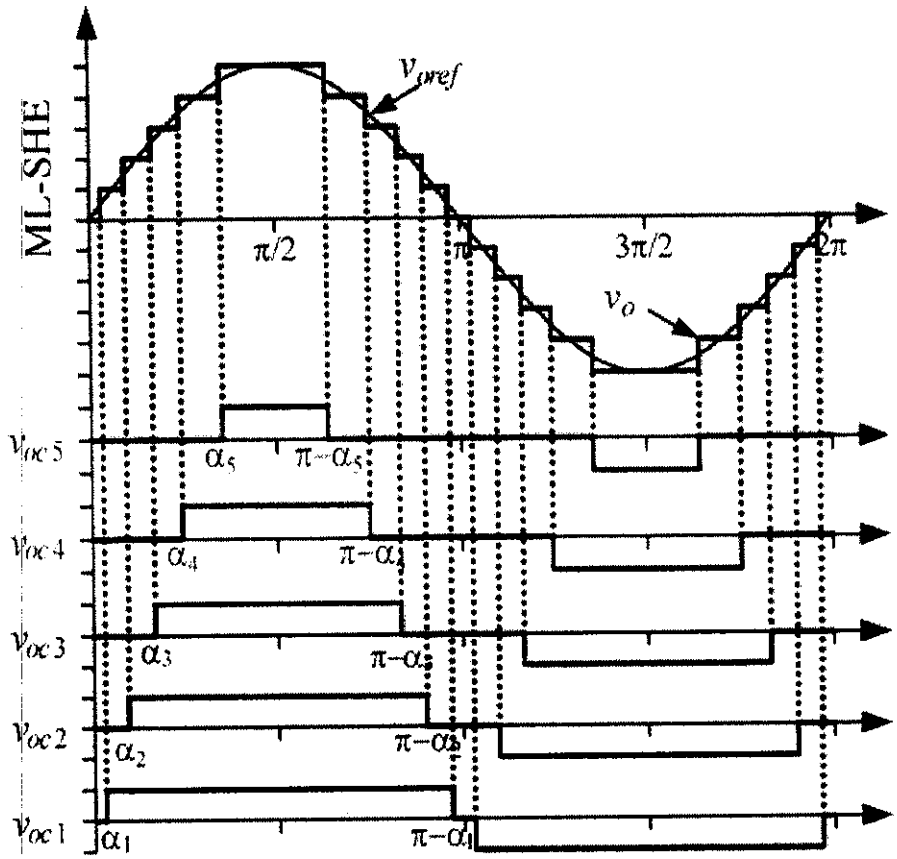


Fig 3.1 One angle per voltage level in Multilevel SHE technique

In these waveforms, it is possible to note that there exists a high difference among the conducting times, which produces an unbalanced power distribution. If a multi-pulse transformer is used, this power unbalance can lead to a distorted input current. Hence this modulation technique can be applied to symmetrical inverters when the number of output voltage levels is high or when the inverter has non-equal dc links.

The second approach is to combine the original SHE with the multilevel version as it can be seen on the waveform of Fig.3.2, where there are several switching angles per voltage level. In this case, the number of harmonics eliminated is independent from the number of output voltage levels, and the switching frequency is higher than the fundamental. It is possible to note that

there are several different possibilities to synthesize the output voltage, allowing a further optimization in terms of switching frequency.

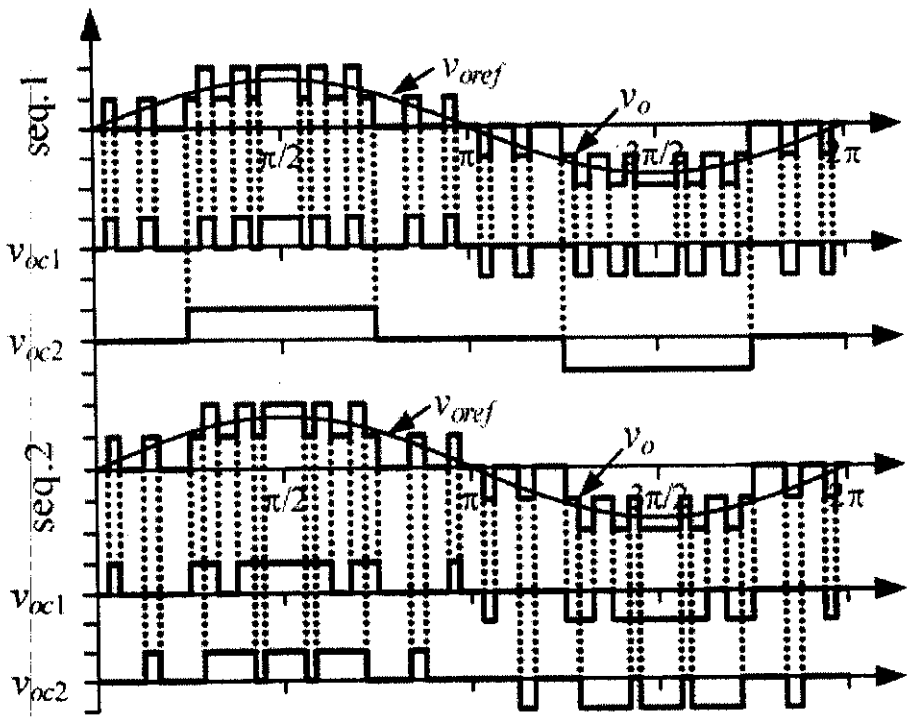


Fig 3.2 Multiple angles per voltage level in Multilevel SHE technique

In Fig. 3.2, the seq. 1 produces a high switching frequency in cell 2 but a fundamental switching frequency in cell 1. Alternatively, seq. 2 produces the same output voltage, but each cell has the same switching frequency.

Advantages of Fundamental Switching Frequency:

- Eliminates low order harmonics in order to reduce the distortion in the output voltage.

Disadvantages of Fundamental Switching Frequency:

- It has no significant effect on higher order harmonics.
- Complex calculations are involved in calculating the switching angles.
- Results in unbalanced power distribution.
- Switching losses are high.

3.3 SPACE VECTOR CONTROL STRATEGY

In order to overcome the disadvantages of fundamental switching frequency, space vector PWM strategies are employed for inverters. Multilevel converters have a large number of vector states which can be used to modulate the reference. Moreover, each state vector has a number of redundancies, as shown in Fig.5 Multilevel SVM must take care of this behaviour to optimize the search of the modulating vectors and to apply an appropriate switching sequence . However, the same properties of state and switching redundancy allow the improvement of the modulation technique to fulfil additional objectives like reducing the common-mode output voltage , reducing the effect of over-modulation on the output currents , improving the voltage spectrum .

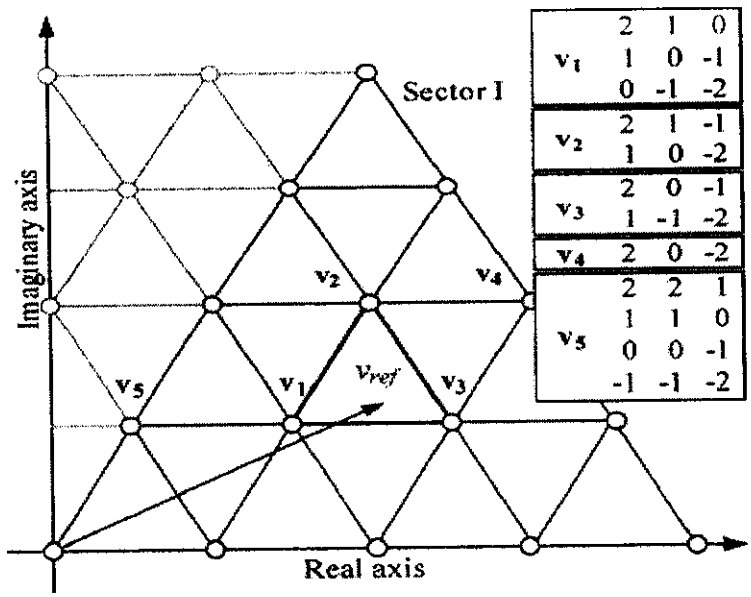
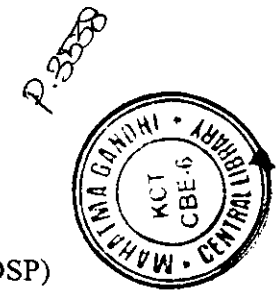


Fig 3.3 Multilevel Space Vector Control Strategy

The space vector control technique can be used to obtain the optimal commutation state for the switches and due to their complexity it is implemented in a Digital Signal Processor (DSP). The implementation of this technique becomes more complex when the number of levels in the inverter is increased. This technique is obtained mainly to the diode clamped topology to solve the problems of unbalanced voltages in the dc bus.

Advantages of Space Vector PWM Strategies:

- Enhanced output voltage.
- Reduction of harmonics.
- Considerable reduction in Total Harmonic Distortion(THD)



Disadvantages of Space Vector PWM Strategies:

- Implementation of space vectors requires Digital Signal Processor (DSP)
- High Cost and Complexity involved in implementation.

3.4 CARRIER BASED PWM CONTROL STRATEGIES:

Pulse Width Modulation (PWM) is normally used as a controller in power conversion and motion control. There are various kinds of modulating modes available such as sinusoidal PWM, space vector PWM, current tracking PWM, harmonic elimination PWM and others. These techniques have merits and demerits but the most widely used in industrial applications are the sinusoidal PWM and space vector PWM. Digital Signal Processors (DSP) and/or Microcontrollers, where reprogramming of the carrier Frequencies are simple. The Sinusoidal Pulse Width Modulation (SPWM) is a well known wave shaping technique. For realization, a high frequency triangle carrier signal (W shape), Vc, is compared with a sinusoidal reference signal, Vr, as desired frequency. The crossover points are used to determine the switching instants.

High switching frequency PWM strategies are the most popular methods because they can be easily implemented. Three major carrier-based techniques used in a conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third harmonic injection PWM (THPWM), and space vector PWM (SVM). SPWM is a very popular method in industrial applications. It uses several triangle carrier signals, one carrier for each level and one reference, or modulation, signal per phase. With the cascaded H-bridge multilevel inverter, the maximum modulation index for linear operation can be as high as 2.42 under fundamental frequency mode. This means it can output a boosted AC voltage to increase the output power, and the output voltage depends on the displacement power factor of the load. The highest voltage is determined when the load is determined. This feature makes the inverter suitable for EV/HEV applications. Moreover, in consideration of the implementation of modulation control methods, the

fundamental frequency and PWM methods can be chosen for high power and low power stage in practical application.

PWM TECHNIQUES

The commonly used PWM control techniques are

1. Single pulse width modulation
2. Multiple pulse width modulation
3. Sinusoidal pulse width modulation

3.4.1 SINGLE PULSE WIDTH MODULATION

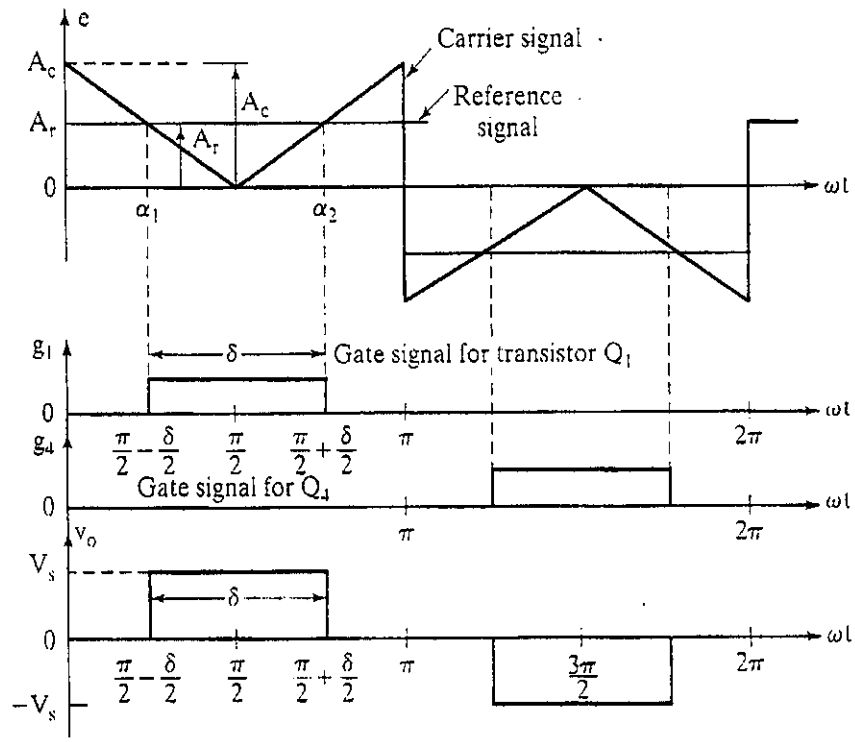


Figure 3.4 Single Pulse Width Modulation

In single pulse width modulation control, there is only one pulse per half cycle and width of the pulse is varied to control the inverter output voltage. The gating signals are generated by comparing the rectangular reference signal of amplitude A_r with the triangular carrier wave of amplitude A_c. The fundamental frequency of the output voltage is determined. By the frequency of the reference signal. Pulse width can be varied from 0 to 180 by varying A_r from 0 to A_c. The

ratio of the amplitude of the reference signal to the amplitude of the carrier signal is called amplitude modulation index. In this type of voltage control scheme as great deal of harmonic content is introduced in the output voltage, particularly at low output voltage levels.

3.4.2 MULTIPLE PULSE WIDTH MODULATION

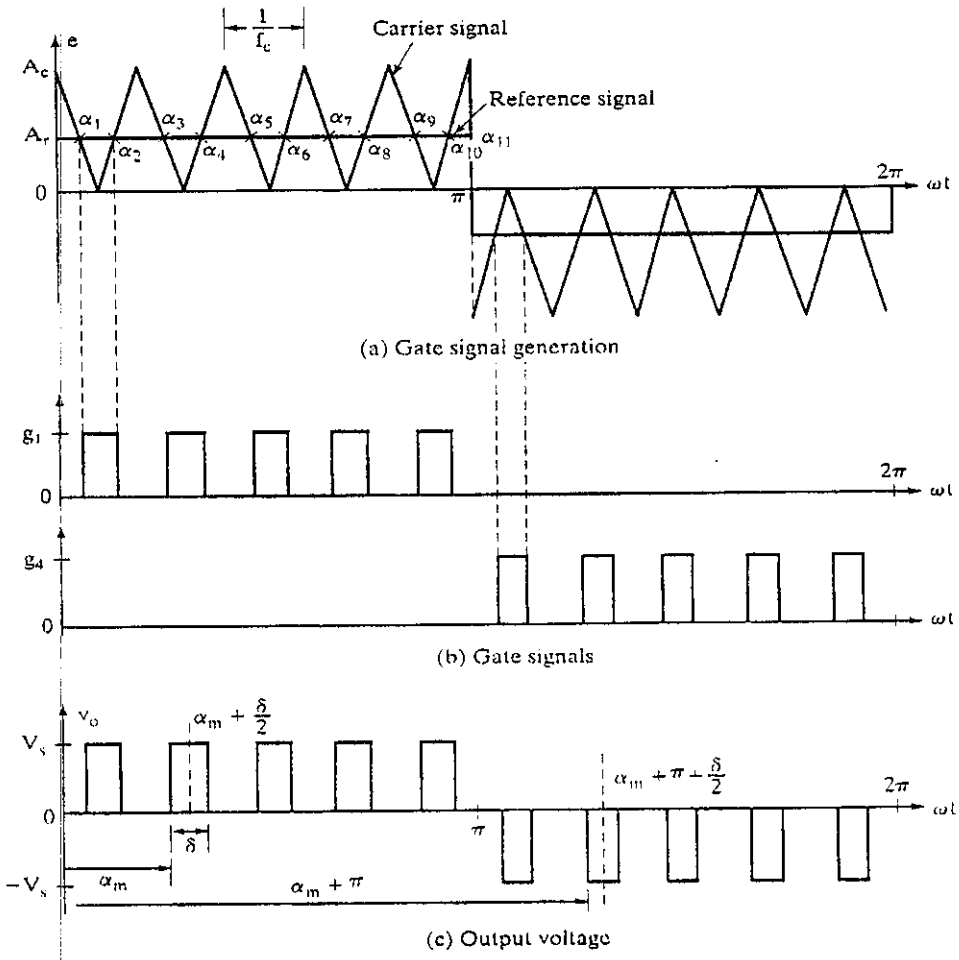


Figure 3.5 Multiple Pulse Width Modulation

In this method of pulse width modulation, the harmonic content can be reduced using several pulses in each half cycle of the output voltage. By comparing the reference signal with a triangular carrier wave, the gating signals are generated for turning on and turning off of a thyristor. The frequency of the reference signal sets the output Frequency f_o and the carrier frequency f_c determines the number of pulses per half cycle. The modulation index controls the

output voltage. This type of modulation is known is known as uniform pulse width modulation. The number of pulses per half cycle is found from the expression $N_p = m_f / 2$ Where $m_f = f_c / f_o$ is the frequency modulation ratio. The variation of modulation index from 0 to 1 varies the pulse width from 0 to Π / N_p and the output voltage from 0 to E_{dc}. With this method, since the voltage control is achieved with a simultaneous reduction of lower order harmonics when compared to single pulse width modulation. However due to large number of pulses per half cycle, frequent turning on and turning off of thyristors is required which increases the switching losses.

3.4.3 SINUSOIDAL PULSE WIDTH MODULATION

Instead of maintaining the width of all pulses the same as in the case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of the sine

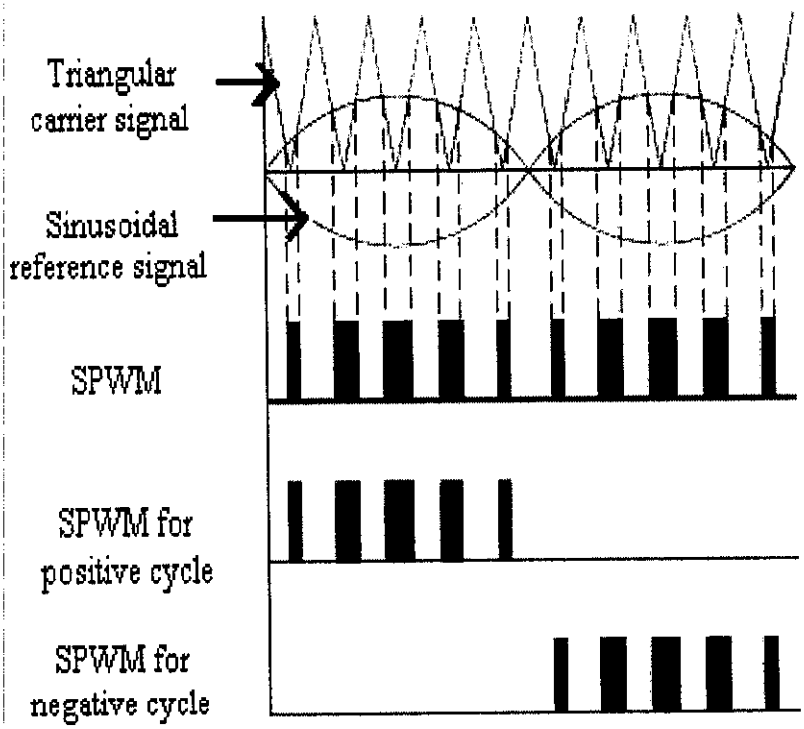


Figure 3.6 Sinusoidal Pulse Width Modulation

wave evaluated at the centre of the same pulse. The gating signals are generated by comparing the sinusoidal reference signal with the triangular carrier wave of frequency f_c .This sinusoidal

pulse width modulation is commonly used in industrial applications. The frequency of the reference signal determiners the inverter output frequency and its peak amplitude controls the modulation index M.Comparing the bidirectional carrier signal with two sinusoidal reference signals V_r and $-V_r$ as shown in the fig. and produces the gating signals as shown. The number of pulses per half cycle depends on the carrier frequency.

Advantages

The main advantages are

1) Low harmonics can be eliminated or minimized.

2) Higher order harmonics can be filtered. Easily the filtering requirements are minimized.

3) The output voltage can be controlled internally without external components.

Thus the harmonics in the output voltage of power electronic converters can be reduced using Pulse-Width Modulation (PWM) switching techniques.PWM methods mentioned above reduce the harmonics by shifting frequency spectrum to the vicinity of high frequency band of carrier signal. In the case of sinusoidal PWM (SPWM) scheme, the control signal is generated by comparing a sinusoidal reference signal and a triangular carrier. The SPWM technique, however, inhibits poor performance with regard to maximum attainable voltage and power. A novel PWM technique, called Inverted-Sine PWM (ISPWM), for harmonic reduction in the output voltage of ac-dc converters is proposed in this research work. In addition, the control scheme based on ISPWM can maximize the output voltage for each modulation index. Thus the proposed ISPWM switching technique can be employed for controlling VSC based inverters has it povides lower Total Harmonic Distortion (THD) and higher fundamental voltage when compared to Conventional PWM techniques.

CHAPTER 4

CHAPTER- 4

INVERTED- SINE PULSE WIDTH MODULATION TECHNIQUE

Multi-level inverters have become an effective and practical solution for increasing power and reducing harmonics of AC waveforms. By synthesizing the AC output voltage from several levels of DC voltages, staircase output waveform can be produced. The modulation strategy employed in this research work is phase disposition (PD) based unipolar inverted sine PWM (ISPWM) technique.

4.1 Multicarrier PWM Technique

The multicarrier PWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an 'n' level inverter is employed, 'n-1' carriers will be needed. The carriers will have the same frequency and the same peak to peak amplitude and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Multicarrier PWM method can be categorized into 2 groups.

1) **Carrier disposition methods (CD)** - where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude,

2) **Phase shifted PWM method**- where the multiple carriers are phase shifted accordingly. Among these classifications, the phase disposition method is more is employed in this simulation as it gives least total harmonic distortion.

In the conventional PD-PWM method, triangular wave is used as carrier wherein they are replaced by inverted sine carrier waves in this proposed strategy. In order to produce a m-level output, generally (m-1) carriers are needed. But this paper employs a PWM technique which uses only three inverted sine wave carriers for producing a seven-level output. The ISPWM technique has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM without any pulse dropping. Also, there is a reduction in the total harmonic

distortion (THD) and switching losses. An inverted sine wave of high switching frequency is taken as a carrier wave and is compared with that of the reference sine wave. The pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.PIC microcontroller is used to obtain the gating pattern for the individual IGBTS. The total harmonic distortion for the different values of switching frequencies is obtained and is found to be lesser than the conventional method. The output voltage waveform which comprises of seven levels is obtained by modulating the inverted sine carriers with optimum frequency. By employing the proposed modulation technique it has been proved that the fundamental voltage is improved throughout the working range and is greater than the voltage obtained using conventional method which employs triangular carriers for modulation.

4.2 Unipolar Inverted Sine Carrier PWM Strategy (UISCPWM):

ISCPWM technique is classified into two types based upon the frequency of carrier waves

- Unipolar ISCPWM - employed carriers are of same frequency
- VFISCPWM - employed carriers are of variable in frequency

Unipolar Inverted Sine PWM control strategy uses the same reference (synchronized sinusoidal signal) as the conventional PWM.

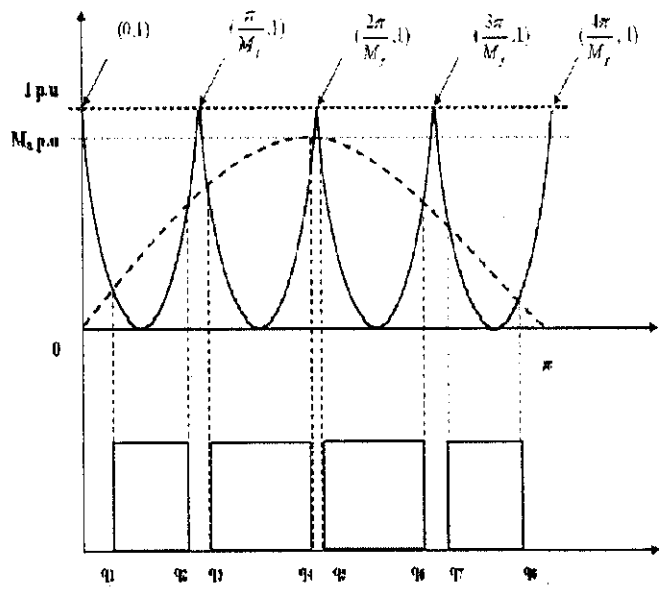


Fig .4.1 Generation of pulse using ISPWM

The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater

The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater pulse area. The difference in pulse widths (hence area) resulting from triangle wave and inverted sine wave with the low (output) frequency reference sine wave in different sections can be easily understood. In the gating pulse generation of the proposed ISCPWM scheme shown in Fig. 4.1, the triangular carrier waveform of PWM is replaced by an inverter sine waveform.

For the ISCPWM pulse pattern, the switching angles may be computed as the same way as PWM scheme. The equations of inverted sine wave are given by (1) and (2) for its odd and even cycles respectively.

$$y = 1 - \sin \{M_f x - \pi/2 (i-1)\} \quad (1)$$

$$y = 1 - \sin \{M_f x - \pi/2 (i-2)\} \quad (2)$$

The switching angles for ISCPWM scheme can be obtained from (3) and (4)

$$M_a \sin q_i + \sin(M_f q_i - \pi/2 (i-1) = 1, i = 1,3,5... \quad (3)$$

$$M_a \sin q_i + \sin(M_f q_i - \pi/2 (i-2) = 1, i = 2,4,6... \quad (4)$$

Unipolar Inverted Sine Carrier Pulse Width modulation (UISCPWM) technique is implemented for single and three phase Conventional Cascaded Seven Level Inverter using MATLAB. The performance parameters considered for comparing the proposed PWM with the conventional method are output voltage quality, Total Harmonic Distortion (THD) and Fundamental Output Voltage.

CHAPTER 5

CHAPTER-5

SIMULATION OF CONVENTIONAL CASCADED SEVEN LEVEL INVERTER

5.1 Simulation of Conventional Cascaded Inverter employing Conventional PWM:

In conventional PWM technique, triangular carrier waves are modulated with reference sine wave for pulse generation. The pulses are generated whenever the amplitude of the reference sine wave is greater than that of the triangular carrier wave.

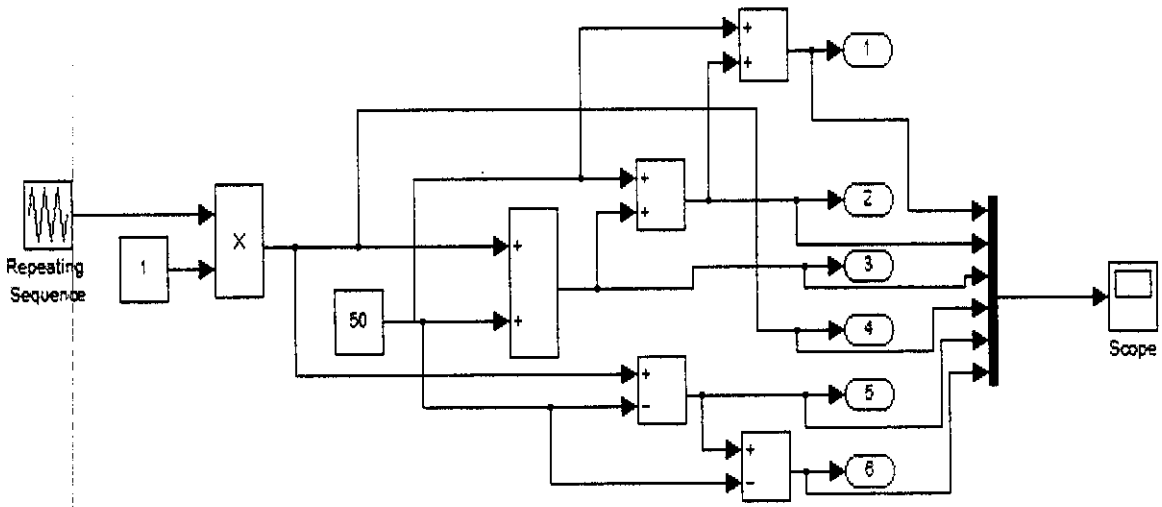


Fig 5.1 Simulation circuit for the generation of triangular wave

The carrier waveforms employed for conventional PWM technique are shown in the Fig.5.2

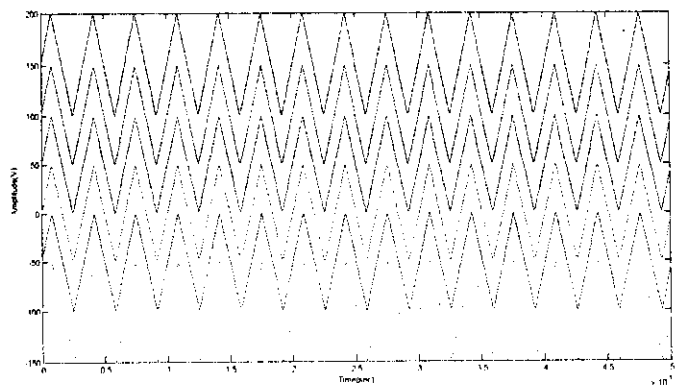


Fig.5.2 Triangular carrier waves

The generated carrier waves of frequency 3950Hz are then modulated with reference sine wave of frequency 50Hz for pulse generation. The obtained pulses are then applied to Conventional Cascaded Seven Level Inverter and the obtained output voltage waveform is shown in fig 5.3

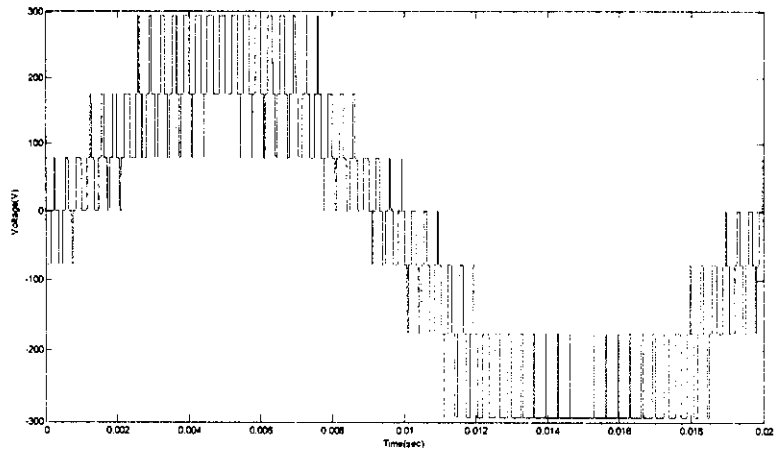


Fig 5.3 Output volta ge of Conventional Cascaded Inverter (Conventional PWM)

5.2 Simulation of Conventional Cascaded Inveter employing Unipolar ISCPWM:

When Unipolar ISCPWM technique is employed for conventional cascaded multilevel inverter, there exists considerable reduction in THD and improvement in fundamental voltage component throughout the working range.

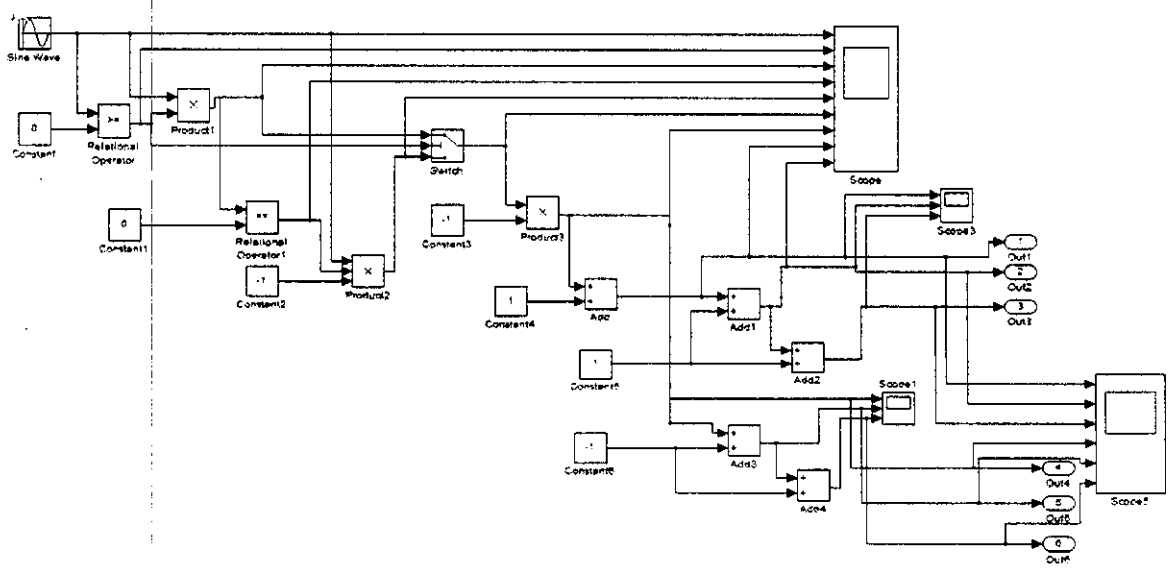


Fig.5.4 Simulation circuit for the generation of unipolar inverted sine carrier waves

The generated carrier waves of frequency 3950Hz are then modulated with reference sine wave of frequency 50Hz for pulse generation.

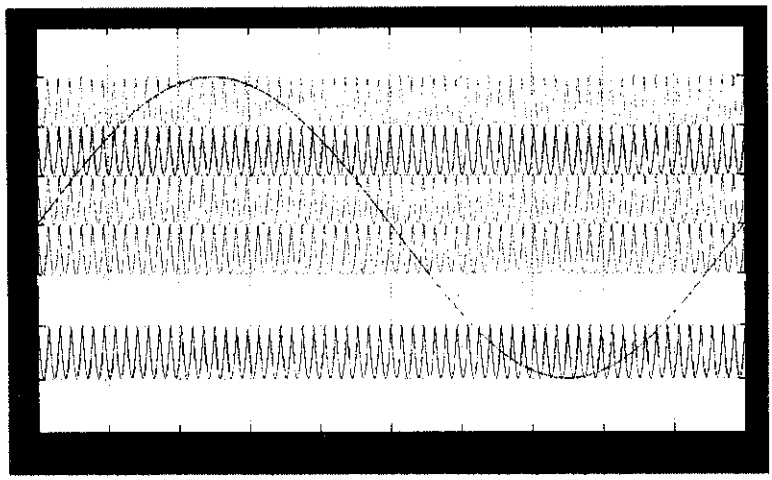


Fig.5.5 Carrier and Inverted Sine Waveforms for Unipolar ISCPWM Technique

The obtained pulses are applied to the conventional cascaded multilevel inverter.

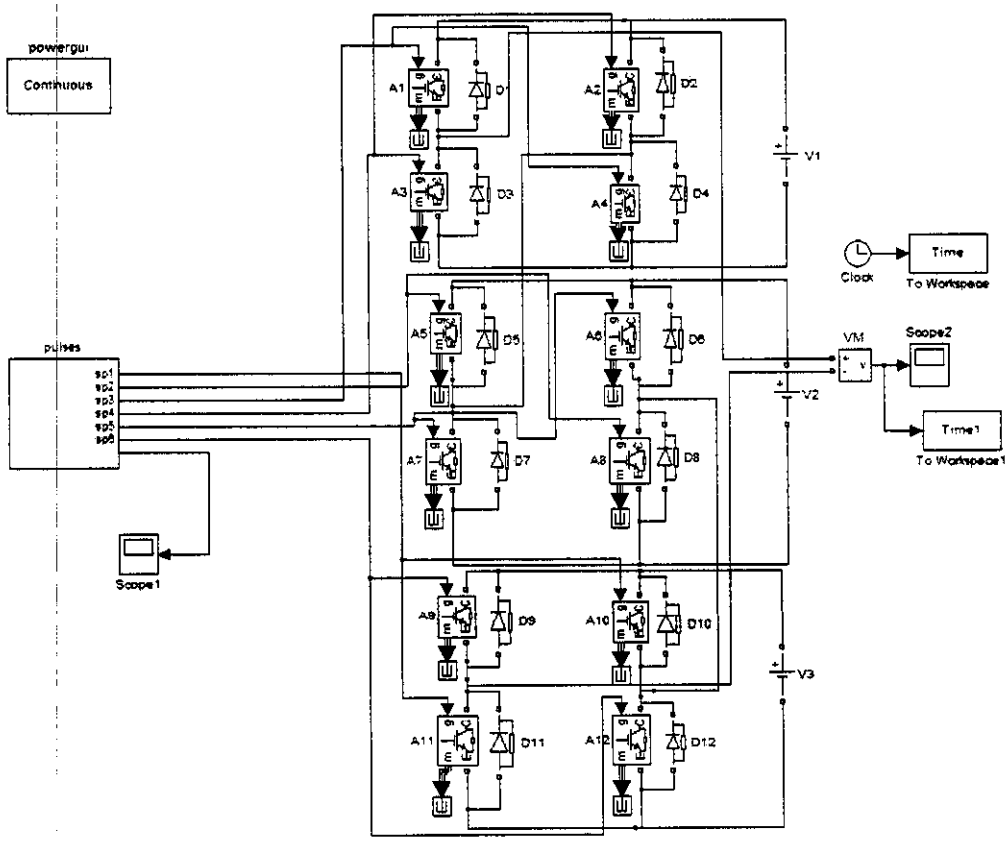


Fig.5.6 Simulation circuit of conventional Cascaded MLI

Output voltage waveform of Conventional Cascaded Seven Level Inverter employing unipolar ISPWM technique is shown in Fig.5.7

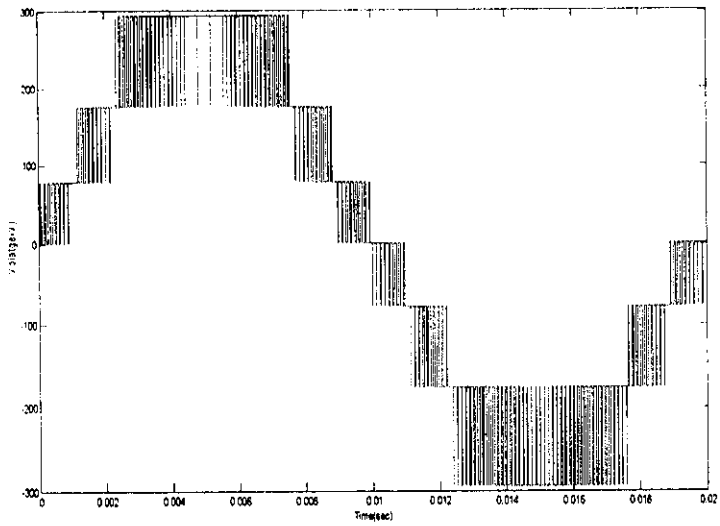


Fig.5.7 Output voltage of Conventional Cascaded Seven Level Inverter employing Unipolar ISCPWM

With the optimum frequency of 3950Hz, in Conventional PWM method the obtained fundamental component and THD values are 265.6V and 30.99% respectively.

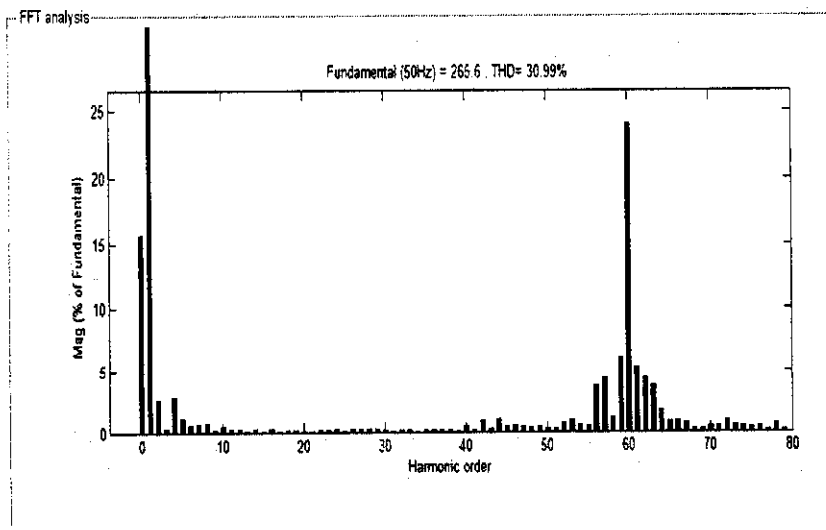


Fig 5.8 FFT Window for output voltage (Conventional PWM)

With the proposed Unipolar ISCPWM technique, the obtained fundamental component and THD values are 278.9V and 21.82% respectively.

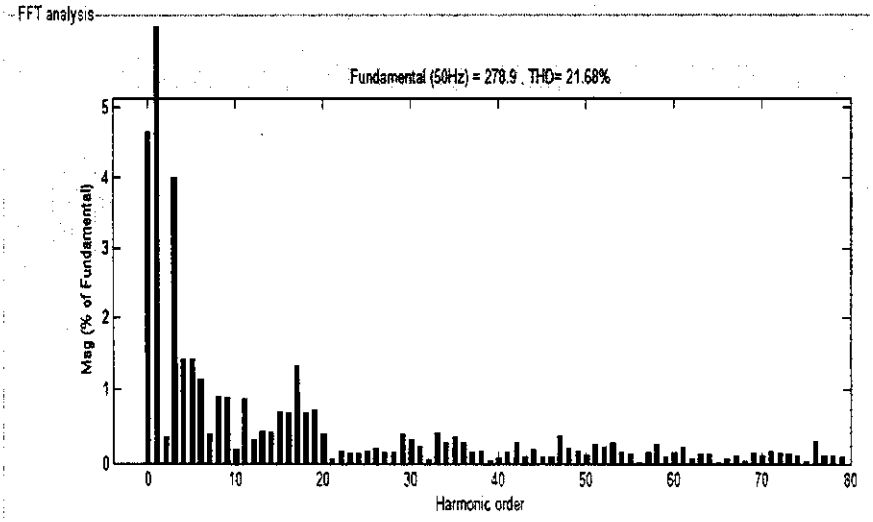


Fig.5.9 FFT Window for output voltage (ISPWM)

5.3 Comparison of Unipolar ISPWM with Conventional PWM technique for conventional Cascaded MLI:

Table 5.1Comparison Unipolar ISCPWM with Conventional PWM

PWM Technique	THD (%)	Fundamental output voltage(V)
Conventional PWM	30.97	266.6
Unipolar ISCPWM	21.82	278.9

Inferences made from above waveforms on implementing Unipolar ISPWM technique for Conventional Cascaded MLI are:

• It has a better spectral quality and a higher fundamental component compared to the conventional PWM

• The Unipolar ISCPWM strategy enhances the fundamental output voltage and reduces THD.

• Harmonics of carrier frequencies or its multiples are not produced.

On implementing Unipolar ISPWM technique for conventional Cascaded MLI, THD is reduced considerably by a factor of around 9%. Hence Unipolar ISCPWM technique is extended for the proposed Asymmetric Cascaded MLI, in order to overcome the disadvantages of Conventional Cascaded Multilevel Inverter.

CHAPTER 6

CHAPTER-6

ASYMMETRIC CASACADED MULTILEVEL INVERTER

6.1 Introduction:

Traditionally, each phase of a cascaded multilevel inverter requires 'n' dc sources for 2n+1 levels. For many applications, it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H- bridge multilevel inverter, an asymmetric topology is proposed as shown in Fig.6.1.This provides the capability to produce higher voltages at higher speeds with low switching frequency. The advantages of asymmetric topology are:

- Reduced number of dc sources
- Low output switching frequency
- Low switching losses
- High conversion efficiency
- Flexibility to enhance
- Reduction in complexity and cost

6.2 Asymmetric Cascaded Seven Level Inverter

The seven - level cascaded multilevel inverter consists of two H-Bridges.

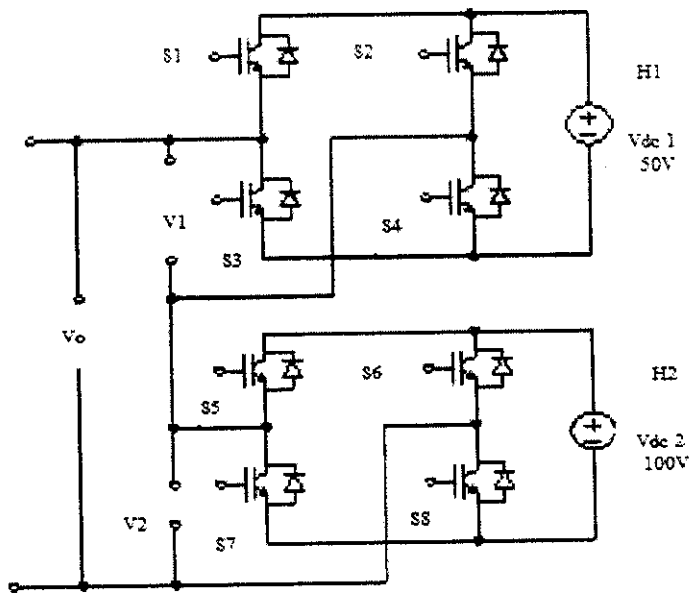


Fig.6.1 Asymmetric Cascaded Seven Level Inverter

The first H-Bridge H1 consists of a separate DC source Vdc, whereas the second H-Bridge H2 consists of a dc source Vdc/2. Let the output of H-Bridge-1 be denoted as v1 (t) and the output of H-Bridge-2 be denoted as v2 (t). Hence the total output voltage is given by v(t)=v1(t)+v2(t).By alternately opening and closing the switches S1,S4 and S2,S3 of H-Bridge-1 appropriately, output of H1 *v1(t)* can be made equal to +Vdc, 0 or -Vdc. Similarly the output voltage of H-Bridge-2 v2(t) can be made equal to –Vdc/2, 0 or +Vdc/2 by opening and closing the switches of H2.Hence v(t) takes values -3/2Vdc, -Vdc, -1/2Vdc, 0, +1/2Vdc, +Vdc, +3/2Vdc.

SWITCHING SEQUENCE FOR ASYMMETRIC CASCADED SEVEN LEVEL INVERTER

POSITIVE HALF CYCLE:

SWITCH IN CONDUCTION	REVERSE DIODE IN CONDUCTION
S1, S4, S8	S7
S4, S5, S8	S3
S1, S4, S5, S8	---
S4, S5, S8	S3
S1, S4, S8	S7

NEGATIVE HALF CYCLE:

SWITCH IN CONDUCTION	REVERSE DIODE IN CONDUCTION
S2, S3, S7	S8
S3, S6, S7	S4
S2, S3, S6, S7	---
S3, S6, S7	S4
S2, S3, S7	S8

CHAPTER 7

CHAPTER-7
SIMULATION OF ASYMMETRIC CASCADED SEVEN LEVEL INVERTER

7.1 Asymmetric Cascaded Inverter employing Unipolar ISCPWM:

PWM signal for the asymmetric cascaded multilevel inverter is generated by comparing inverted sine carrier wave of high switching frequency (3950Hz) with that of reference sine wave.To produce a seven-level output, Unipolar ISCPWM strategy uses six carriers. The simulation circuit for pulse generation is shown in the Fig.7.1

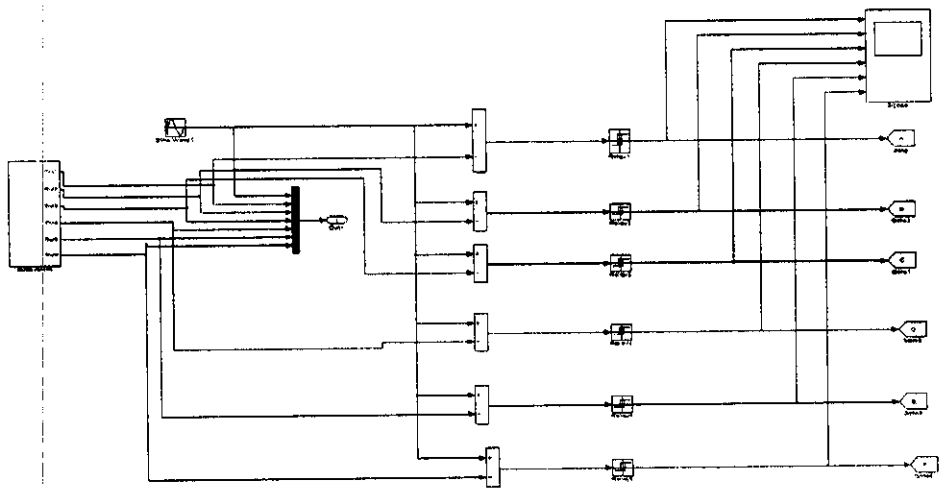


Fig.7.1 Simulation circuit for pulse generation

The generated pulses are then applied to asymmetric cascaded MLI. Output voltage waveform of single phase asymmetric cascaded seven level inverter employing Unipolar ISCPWM technique is shown in Fig.7.2

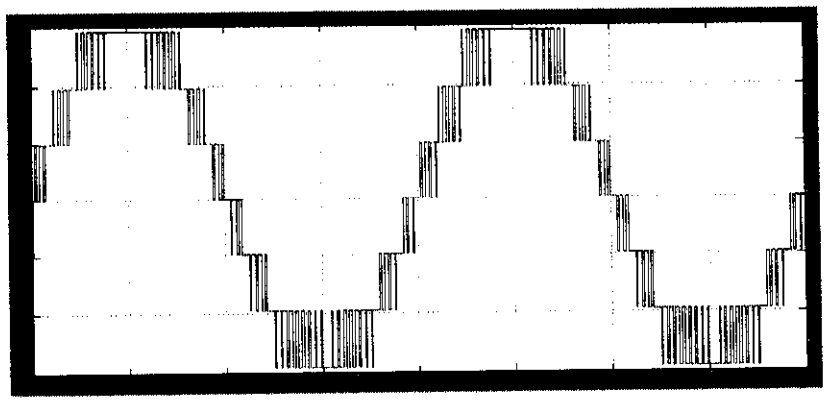


Fig.7.2 Output Voltage Waveform of single phase Asymmetric Cascaded Seven Level Inverter.

The proposed PWM strategy is also extended for three phase asymmetric cascaded MLI by introducing a phase displacement of 120 degrees between each phase. The simulation circuit for three phase asymmetric cascaded MLI is shown in Fig 7.3

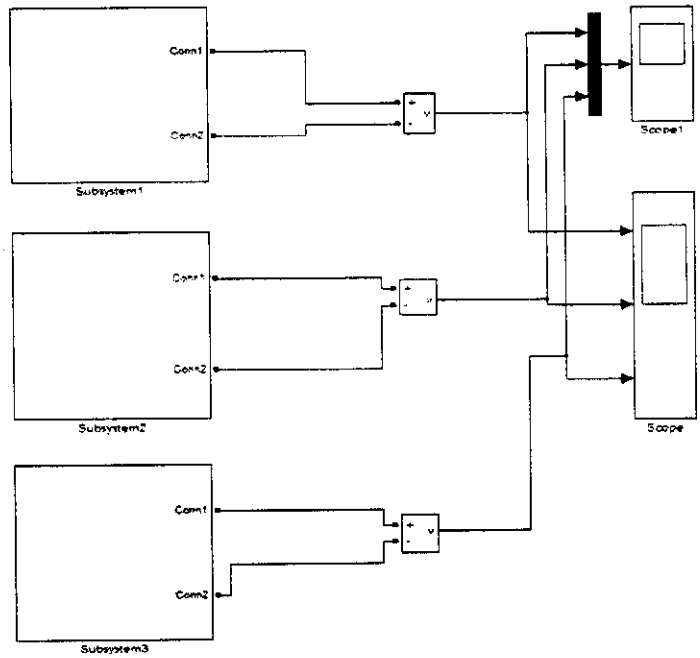


Fig.7.3 Simulation circuit for three phase asymmetric cascaded MLI

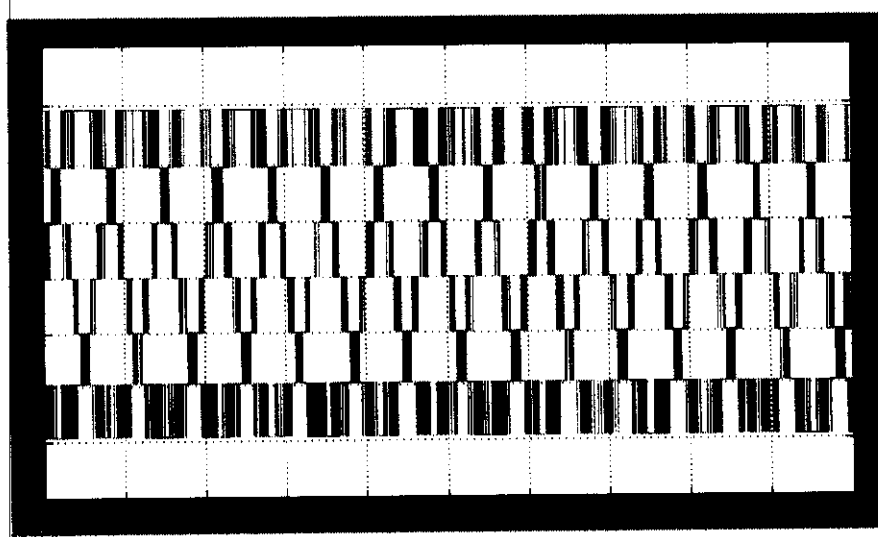


Fig.7.4 Output Voltage Waveform of three phase Asymmetric Cascaded Seven Level Inverter. (Unipolar ISCPWM)

7.2 Asymmetric Cascaded Inverter employing Variable frequency ISCPWM:

The proposed control strategy replaces the conventional fixed frequency carrier waveform by variable frequency inverted sine wave. The variable frequency inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the Unipolar ISCPWM strategy. Also in order to balance the number of active switching among the levels the carrier frequencies are chosen based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all levels. The reference carrier frequency was chosen as **3950Hz.** With the carrier reference frequency of 3950Hz applied to the band-1, the new frequencies for bands 2 and 3 are assigned proportional to their respective slopes.

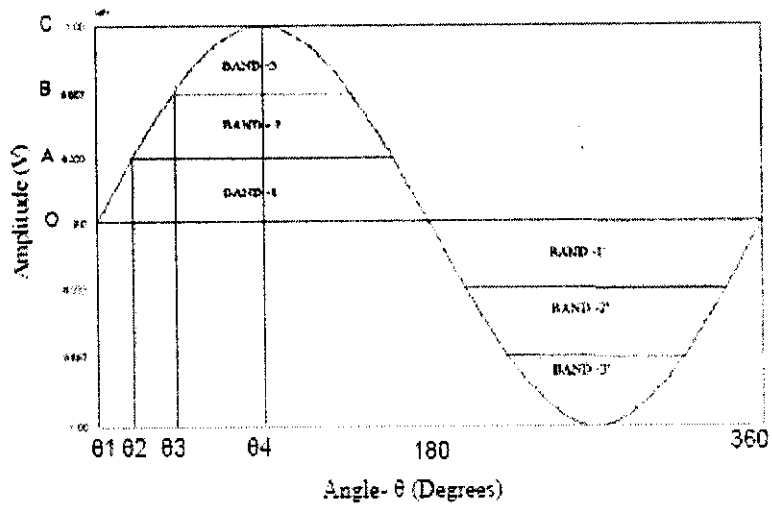


Fig.7.5 Reference modulating wave – Three bands for different carrier frequency

In Fig.7.5 the modulating wave is defined as, $V(t) = \sin\theta$ (1)

The calculation of the slope values for the three bands is shown below:

$\theta_1 = \sin^{-1}0 = 0$ radians (2)

$\theta_2 = \sin^{-1}(1/3) = 0.339$ radians (3)

$\theta_3 = \sin^{-1}(2/3) = 0.728$ radians (4)

$\theta_4 = \sin^{-1}(1) = 1.5707$ radians (5)

Slope C_1: Slope C_2: Slope C_3 = 1: 0.8716: 0.4040 (6)

Frequency C_1: FrequencyC_2: FrequencyC_3

3950 : 3443 : 1596

Simulation circuit for variable frequency inverted sine carrier waves is shown in Fig 7.6. Pulses for the asymmetric cascaded MLI are generated by modulating carrier waves with reference sine wave of frequency 50Hz.

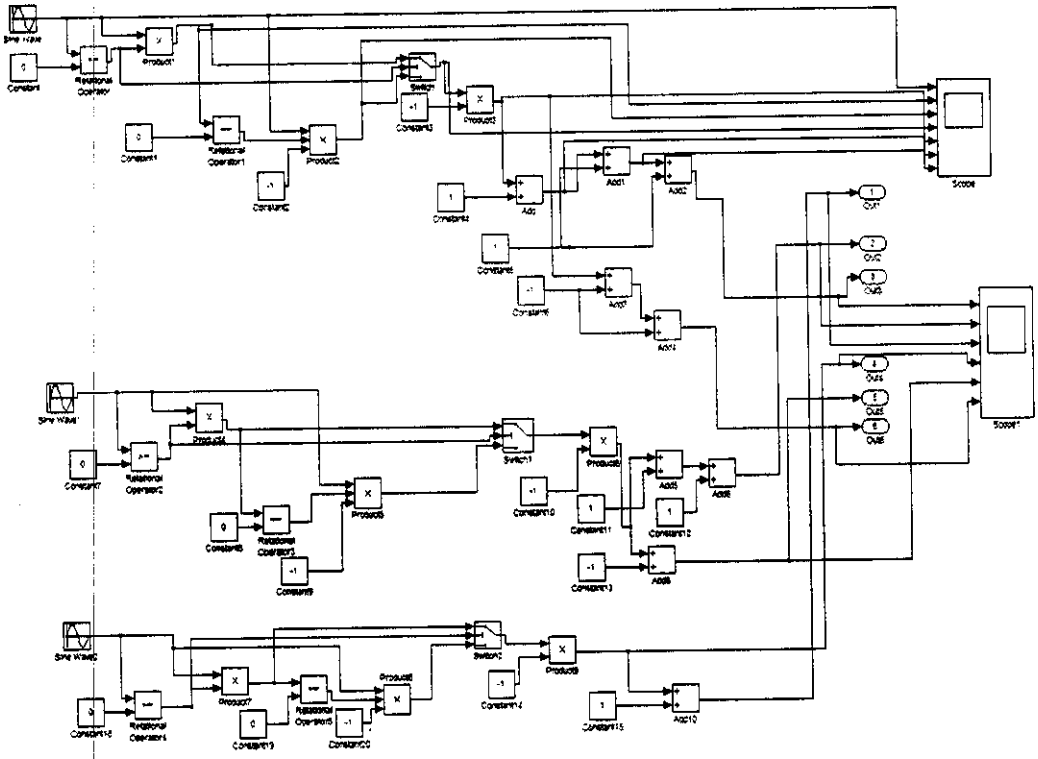


Fig.7.6 Simulation circuit for the generation of variable frequency inverted sine carrier waves

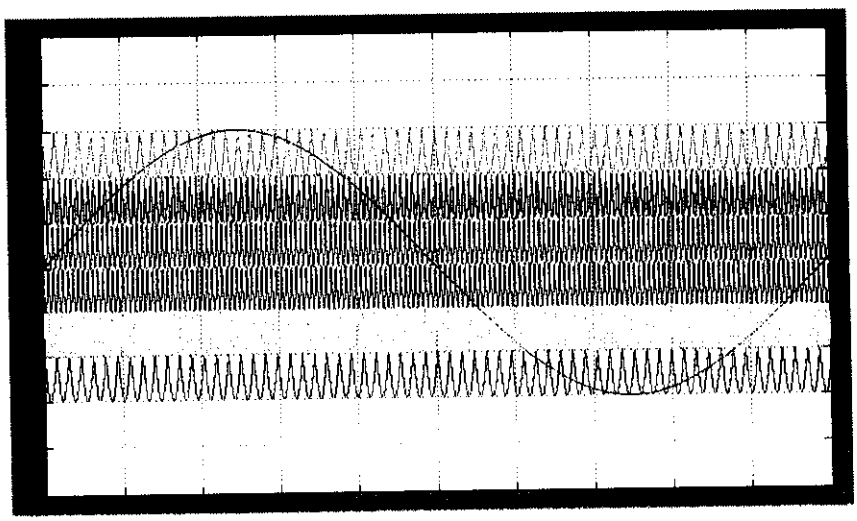


Fig.7.7 Carrier and Inverted Sine Waveforms for VFISCPWM Technique

The obtained pulses from VFISPWM strategy are then applied to the asymmetric cascaded MLI. Output voltage waveform of cascaded seven level inverter employing VFISCPWM technique is shown in Fig 7.8

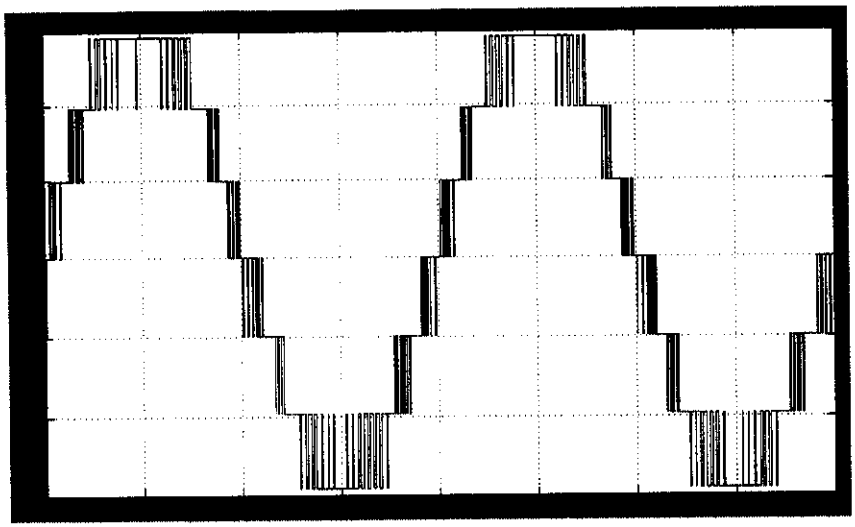


Fig 7.8 Output voltage waveform of single phase asymmetric cascaded MLI employing VFISCPWM

The proposed PWM strategy is also extended for three phase asymmetric cascaded MLI by introducing a phase displacement of 120 degrees between each phase.

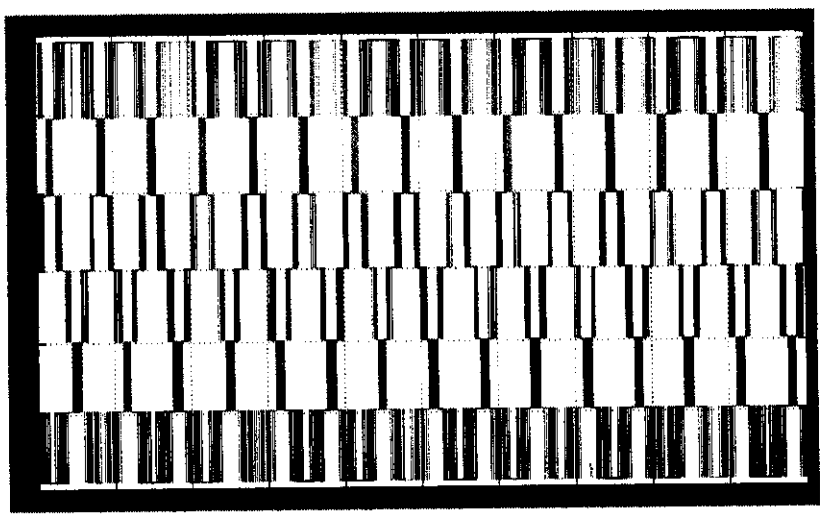


Fig.7.9 Output Voltage Waveform of three phase Asymmetric Cascaded Seven Level Inverter.

On implementing VFISPWM technique for asymmetric cascaded MLI, THD is reduced by a factor of around 2% when compared to Unipolar ISCPWM strategy. The VFISPWM provides an enhanced fundamental voltage, lower total harmonic distortion (THD) and minimizes the switch utilization among the various levels in inverters. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The carrier frequencies are so selected that the number of switching in each band are equal. The proposed modulation technique for the proposed inverter topology maximizes the output voltage and gives a low THD of 5.80%. The FFT window for the ouput voltage waveform of asymmetric cascaded MLI employing Unipolar ISCPWM is shown in Fig 7.10

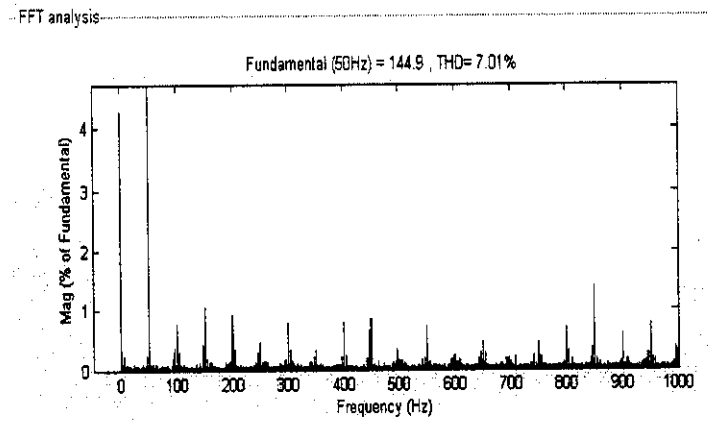


Fig 7.10 FFT Window for output voltage (Unipolar ISPWM)

The FFT window for the ouput voltage waveform of asymmetric cascaded MLI employing VFISPWM is shown in Fig.7.11

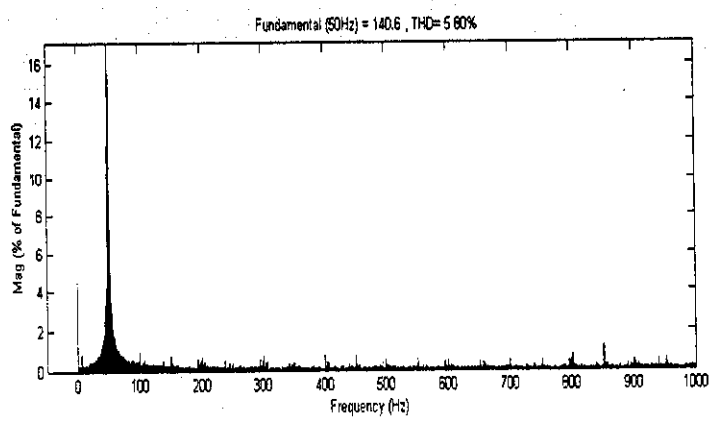


Fig 7.11 FFT Window for output voltage (VFISPWM)

7.3 Comparison of VFISCPWM with Unipolar ISCPWM technique:

Table 7.1Comparison of VFISCPWM with Unipolar ISCPWM

PWM Technique	THD (%)
Unipolar ISCPWM	7.01
Variable Frequency ISCPWM	5.80

Some inferences made from above waveforms are:

- VFISCPWM technique provides better spectral quality and reduced THD when compared to Unipolar ISCPWM technique.
- Harmonics of carrier frequencies and its multiples are not produced in ISCPWM along with minimum utilization of switches.

CHAPTER 8

CHAPTER 8

HARDWARE IMPLEMENTATION

8.1 BLOCK DIAGRAM OF CASCADED MULTILEVEL INVERTER

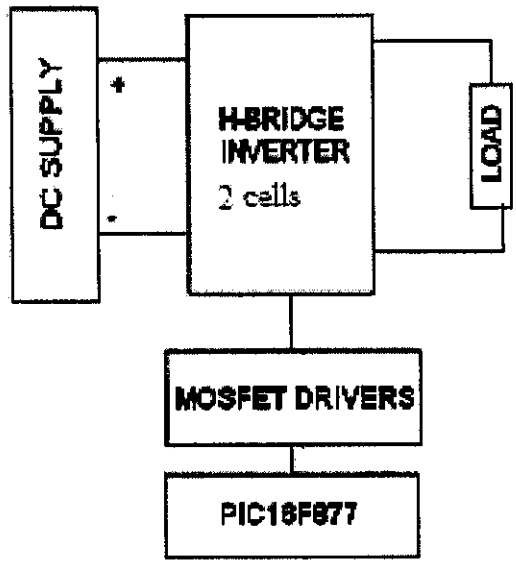


Figure 8.1 Block diagram of cascaded multilevel inverter

8.2 MOSFET IRFZ44:

8.2.1 CHARACTERISTICS OF MOSFET:

The practical mosfet has the following switching and conduction Characteristics:

1. Limited power handling capabilities, that is, limited conduction current when the switch is in the on-state and limited blocking voltage when the switch is in the Off-state.

2. Limited switching speed caused by the finite turn-on and turn-off times. This limits the maximum operating frequency of the device.

3. Finite on-state and off-state resistances, that is, forward voltage drop exists when in the on-state, and reverse current flow (leakage) exists when in the off state.

4 .Because of characteristics 2 and 3, the practical switch experiences power losses in the on- and off-states (known as conduction loss), and during switching transitions (known as switching loss).

8.2.2 MOSFET ADVANTAGES:

MOSFETs provide much better system reliability.

- Driver circuitry is simple and cheaper.
- MOSFET's fast switching speeds, permit much higher switching frequencies and there by the efficiency are increased.
- Overload and peak current handling capacity is high.
- MOSFETs have better temperature stability.
- MOSFET's leakage current is low.
- Drain-source conduction threshold voltage is absent which eliminates electrical noise.
- MOSFETs are able to operate in hazardous radiation environments

8.3 MOSFET DRIVER IR2110:

8.3.1 DESCRIPTION

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts. It can be used for voltage protection, shut down protection and stable operation. the pin diagram is shown in figure 8.3

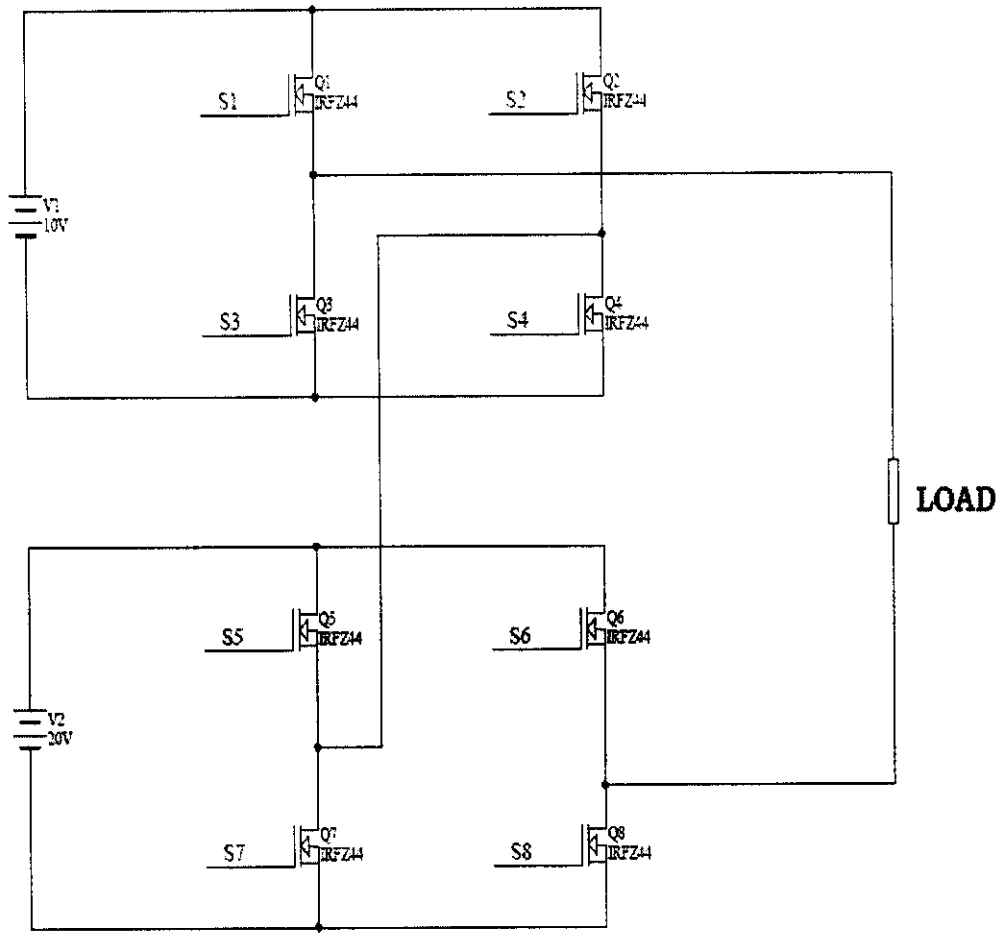


Figure 8.2 Circuit diagram of a seven level inverter

8.3.2 FEATURES

- Floating channel designed for bootstrap operation fully operational to +500V or +600V tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for both channels
- 3.3V logic compatible Separate logic supply range from 3.3V to 20V Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic

• Matched propagation delay for both channels

• Outputs in phase with inputs

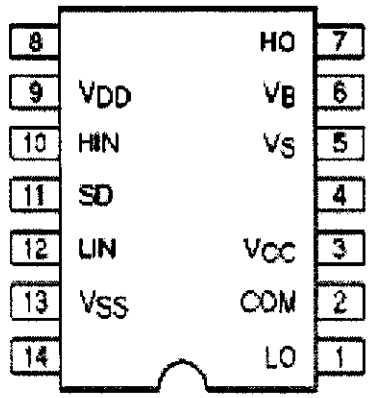


Figure 8.3 Pin diagram of IR2110

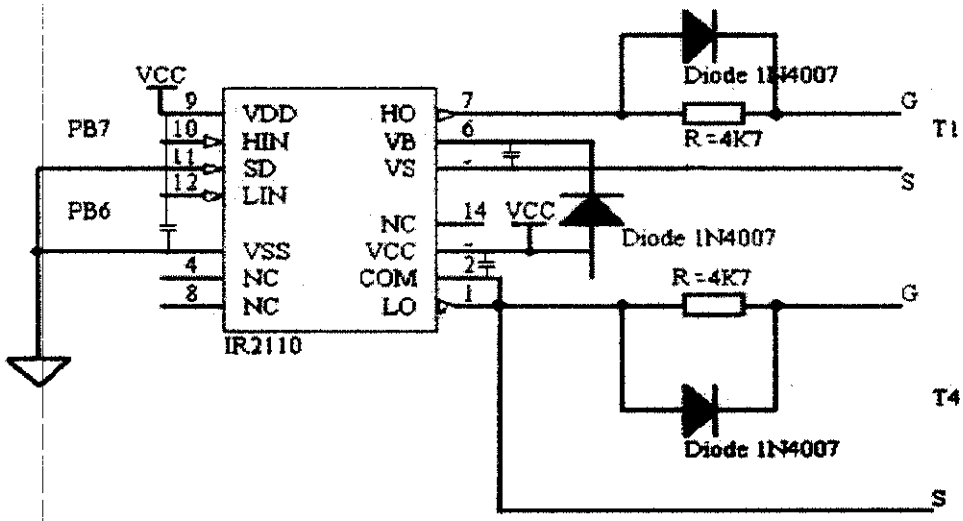
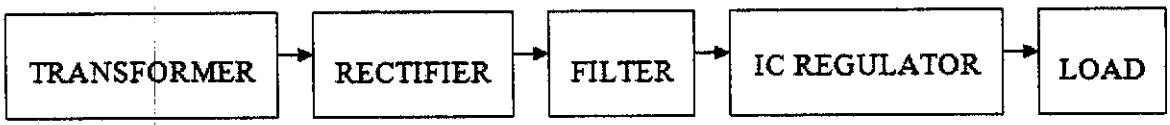


Figure 8.4 Driver circuit of IR2110

8.4 POWER SUPPLY:



8.4.1 RECTIFIER BLOCK

The rectifier block contains a step down transformer, which step downs the input voltage from 220V to 12V. In addition, the step downed voltage is rectified to DC. This is done by uncontrolled single phase diode rectifier. The output of this block is 12V DC. The schematic of rectifier is shown in the fig.8.5.

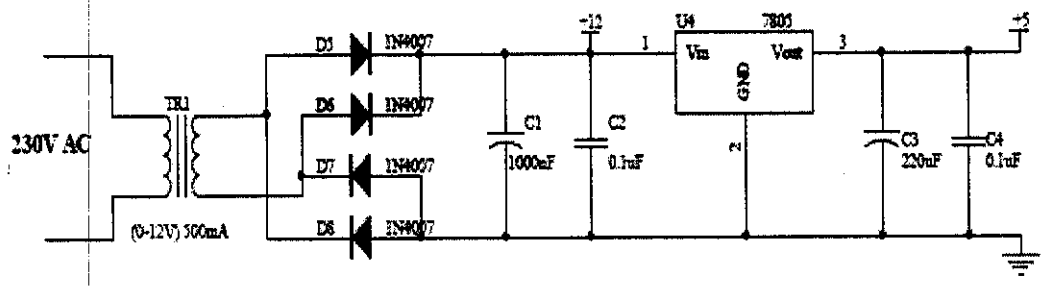


Fig 8.5 Schematic of rectifier

8.4.2 UNIPOLAR ISPWM PULSE GENERATION

The sine wave oscillator is used to generate inverted sine wave of certain carrier frequency is then compared with sine wave using OP-AMP LM358. The details of the LM358 is given in APPENDIX I

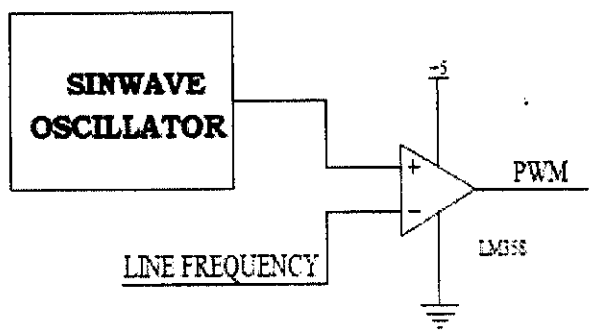


Fig 8.6 Schematic of PWM Generation

8.4.3 MICROCONTROLLER FOR ASYMMETRIC CASCADED MLI

The gate pulse for the inverter switches and the switches in soft-switching module is generated by PIC16F877A controller. This micro controller circuit works in 5V power supply. So separate step down rectifier unit is made for the controller. The details about PIC16F877A is given in APPENDIX II. This controller is isolated from the main circuits by means of opto-coupler. The schematic of micro controller circuit is shown in fig.8.7.

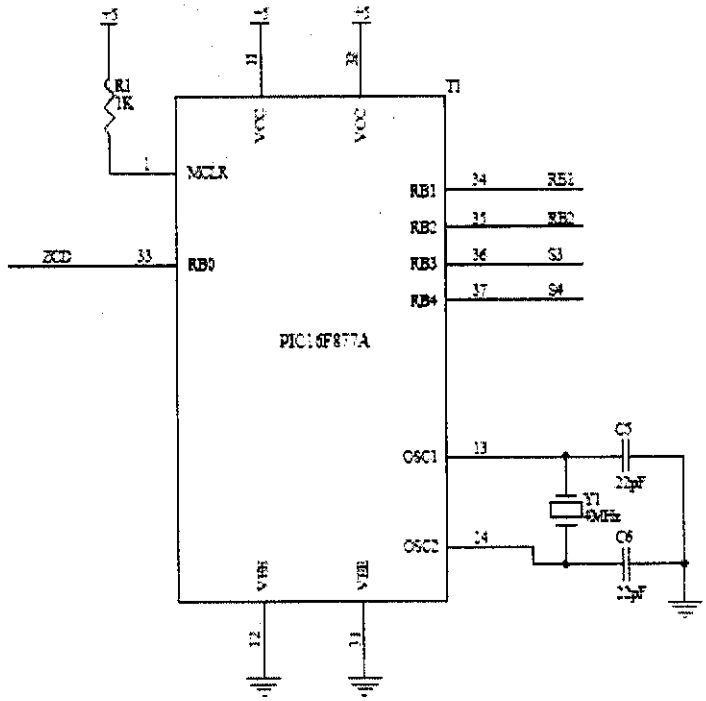


Fig 8.7 Schematic of micro controller circuit

8.5 PIC CONTROLLER

8.5.1 CONCEPTS OF CONTROLLER:

Controller is a general purpose device, which integrates a number of the components of a microprocessor system on to single chip. It has inbuilt CPU, memory and peripherals to make it as a mini computer. A Controller combines on to the same microchip:

- The CPU core
- Memory(both ROM and RAM)
- Some parallel digital i/o

Controllers will combine other devices such as:

- A timer module to allow the Controller to perform tasks for certain time periods.
- A serial I/O port to allow data to flow between the Controller and other devices such as a PIC or another Controller.
- An ADC to allow the Controller to accept analogue input data for processing.

Controllers are

- Smaller in size
- Consumes less power
- Inexpensive

Micro Controller is a standalone unit, which can perform functions on its own without any requirement for additional hardware like I/O ports and external memory.

The heart of the Controller is the CPU core. In the past, this has traditionally been based on a 8-bit microprocessor unit. For example Motorola uses a basic 6800 microprocessor core in their 6805/6808 Controller devices.

In the recent years, Controllers have been developed around specifically designed CPU cores, for example the microchip PIC range of Controllers.

8.5.2 INTRODUCTION TO PIC (16F877A):

The Controller that has been used for this project is from PIC series. PIC Controller is the first RISC based Controller fabricated in CMOS (complementary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

Various Controllers offer different kinds of memories. EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in pic16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

8.5.3 FEATURES OF PIC:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- Operating speed: DC - 20 MHz clock input
- DC - 200 ns instruction cycle
- Up to 8K x 14 words of Flash Program Memory,
- Up to 368 x 8 bytes of Data Memory (RAM)
- Up to 256 x 8 bytes of EEPROM data memory
- Interrupt capability (up to 14 internal/external)
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- In-Circuit Serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial and Industrial temperature ranges
- Low-power consumption:< 2 mA typical @ 5V, 4 MHz,20mA typical @ 3V, 32 kHz

< 1mA typical standby current

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules

- Capture is 16-bit, max resolution is 12.5 ns,
- Compare is 16-bit, max resolution is 200 ns,
- PWM max. Resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- USART/SCI with 9-bit address detection.
- Parallel Slave Port (PSP) 8-bits wide, external RD, WR and CS controls

8.5.4 Pin diagram of PIC 16F877A

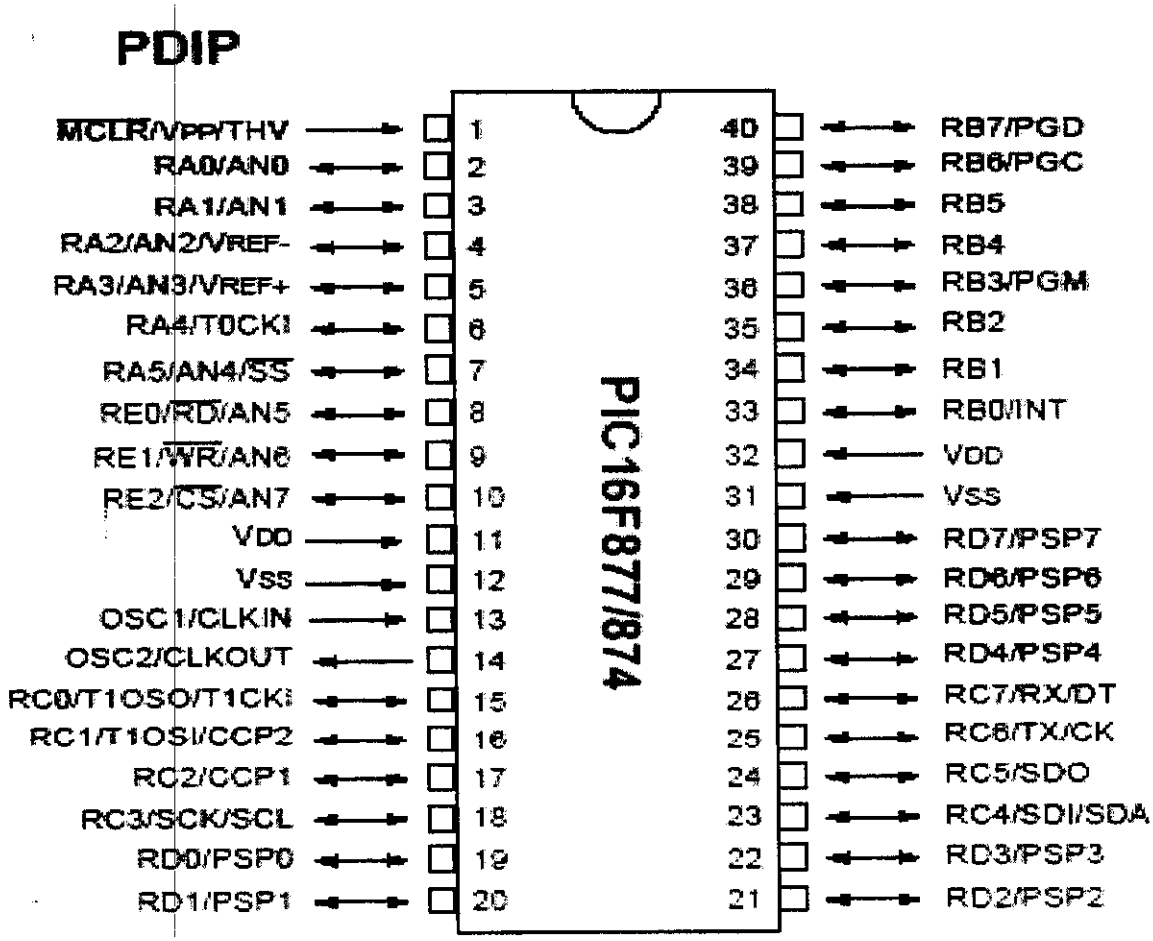
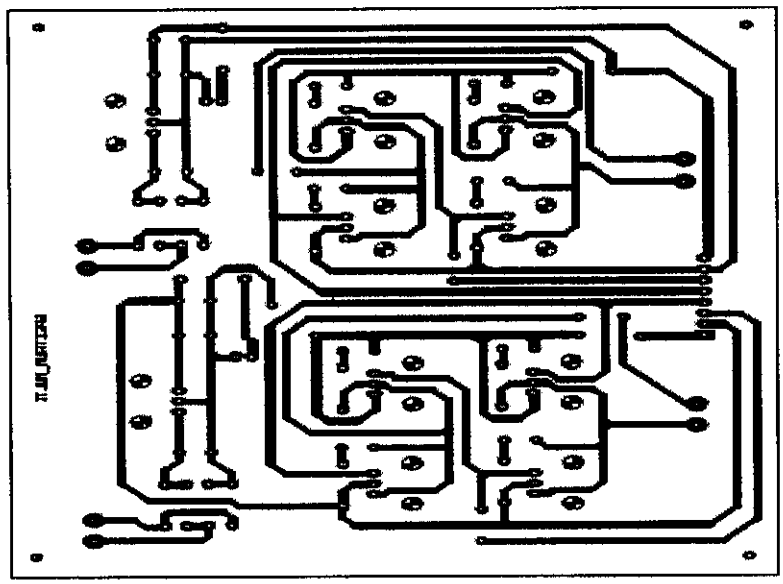


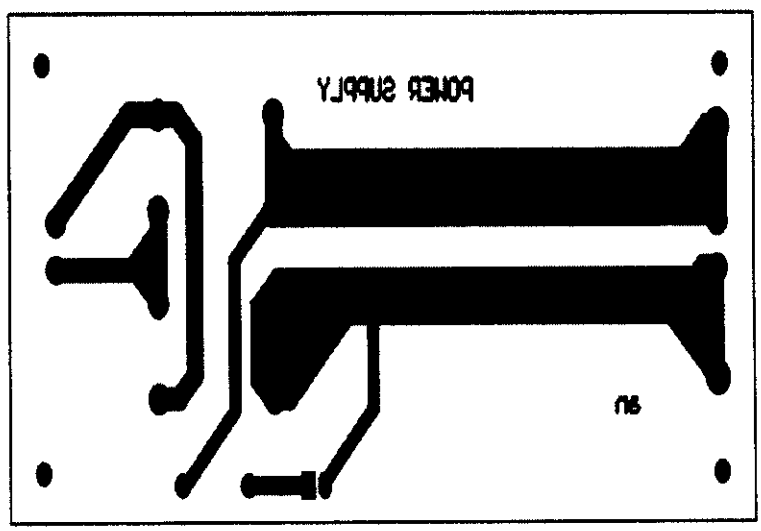
Fig. 8.8 Pin diagram of PIC 16F877A

8.6. PCB LAYOUT

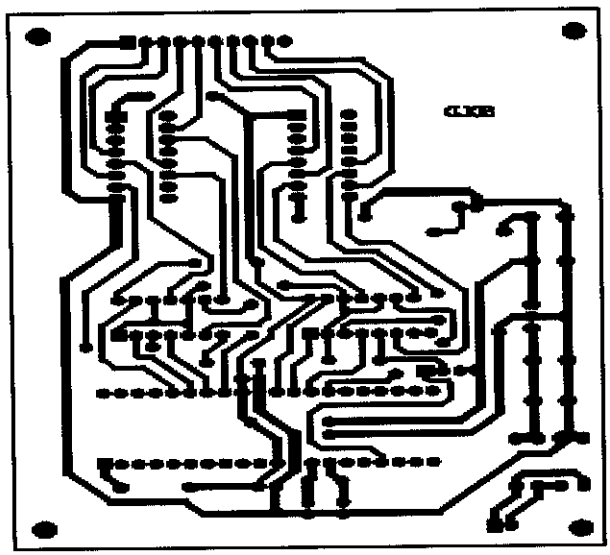
8.6.1 LAYOUT OF SINGLE BRIDGE OF CASCADED INVERTER



8.6.2 LAYOUT OF POWER SUPPLY



8.6.3 LAYOUT OF PIC BOARD



8.7 HARDWARE PROTOTYPE AND RESULTS

Fig 8.9 Hardware Photograph

8.7.1 HARDWARE OUTPUT WAVEFORMS

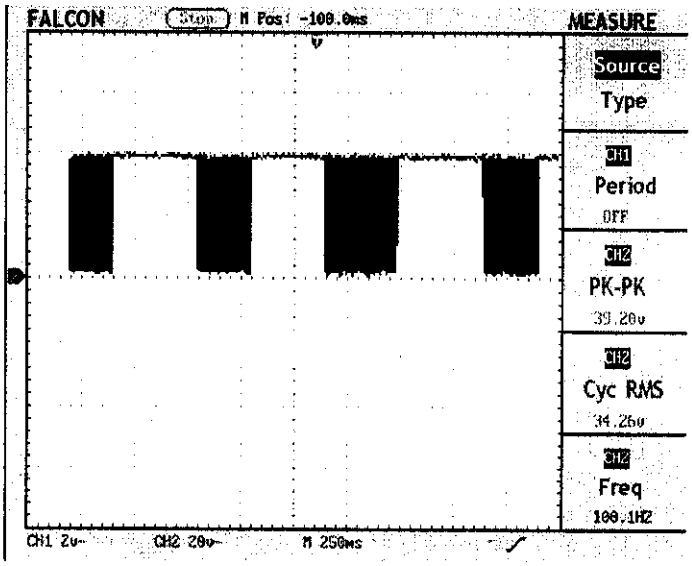


Fig.8.10 Generated pulses using ISPWM technique in CRO

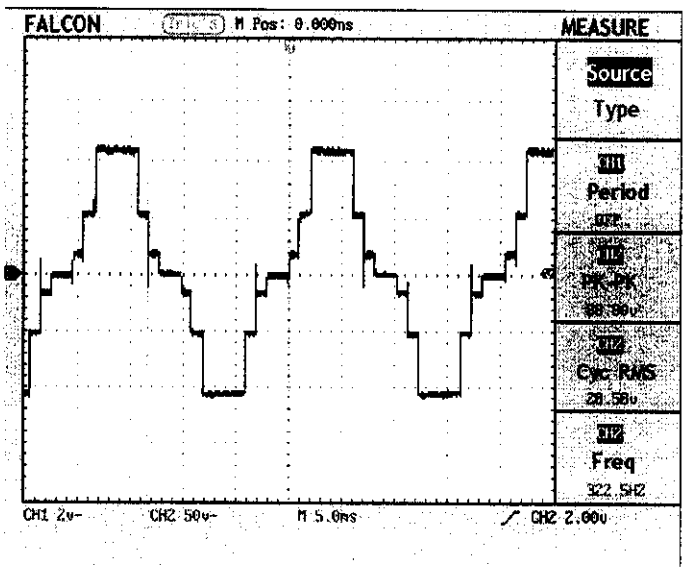


Fig.8.11 Cascaded 7 level inverter output waveform in CRO

CHAPTER 9

CHAPTER-9
CONCLUSION AND FUTURE SCOPE

9.1 CONCLUSION

The line voltage yields better spectral performance for VFISCPWM hence this technique reduces the need for output filter. Asymmetric cascaded multilevel inverter using two unequal dc sources for each phase requires minimum number of switching devices. An inverted sine wave carrier frequency modulation strategy gives maximum fundamental voltage for a given THD.By employing this new technique the fundamental voltage is improved throughout the working range and thereby resulting in enhanced fundamental voltage. Also the range of THD is reduced when compared to conventional PWM technique. Reduction in number of DC sources and switches reduces the complexity and cost of the circuit. By increasing the number of steps, waveform approaches the desired sinusoidal shape accompanied with reduction in THD. Further reduction in THD can be obtained by employing PI or PID controller. The proposed inverter topology along with proposed PWM strategy has a greater scope of application in fuel cells and electric vehicles.

9.2 FUTURE SCOPE:

- Future reduction can be obtained by Phase Shifted multicarrier technique.
- By increasing the number of steps, waveform approaches the desired sinusoidal shape accompanied with reduction in THD
- Further reduction in THD can be obtained by employing PI or PID controller.
- The proposed inverter topology along with proposed PWM strategy has a greater scope of application in fuel cells and electric vehicles.

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APPENDIX I

FAIRCHILD
SEMICONDUCTOR®

www.fairchildsemi.com

LM2904,LM358/LM358A,LM258/ LM258A

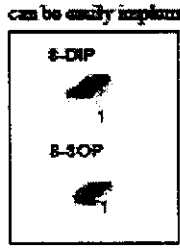
Dual Operational Amplifier

Features

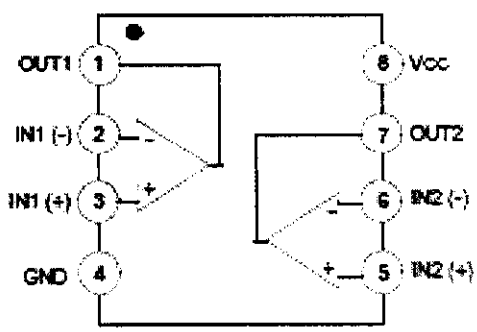
- Internally Frequency Compensated for Unity Gain
- Large DC Voltage Gain: 100dB
- Wide Power Supply Range:
  LM258/LM258A, LM358/LM358A: 3V~32V (or ±1.5V ~ 16V)
  LM2904 : 3V~26V (or ±1.5V ~ 13V)
- Input Common Mode Voltage Range Includes Ground
- Large Output Voltage Swing: 0V DC to Vcc -1.5V DC
- Power Drain Suitable for Battery Operation.

Description

The LM2904/LM358/LM358A, LM258/LM258A consist of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP-AMP circuits which now can be easily implemented in single power supply systems.

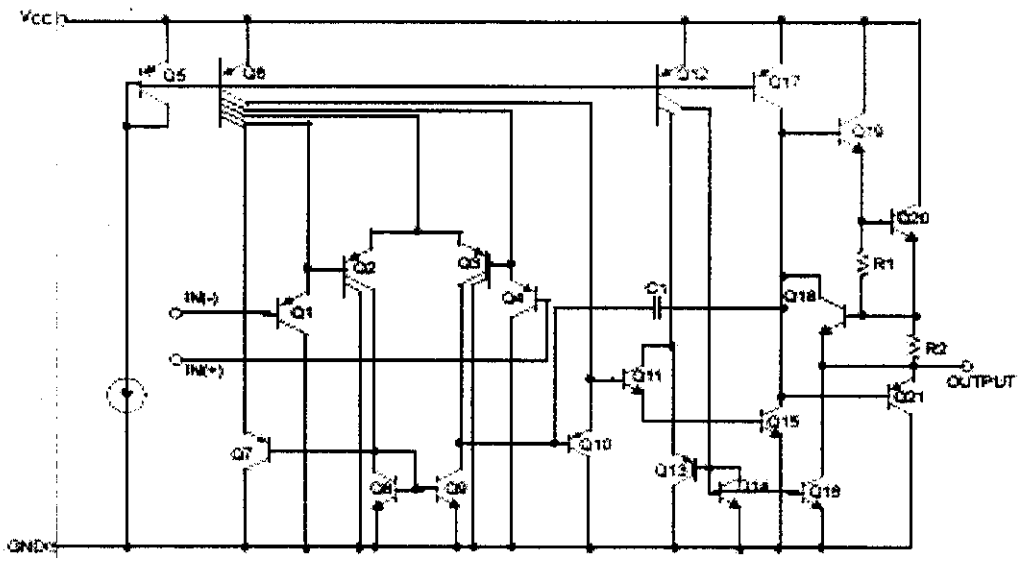


Internal Block Diagram



Schematic Diagram

(One section only)



Absolute Maximum Ratings

Parameter	Symbol	LM258/LM258A	LM358/LM358A	LM2904	Unit
Supply Voltage	V_{CC}	±16 or 32	±16 or 32	±13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	32	26	V
Input Voltage	V_I	-0.3 to +32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND V_{CC}≤15V, T_A = 25°C(One Amp)	-	Continuous	Continuous	Continuous	-
Operating Temperature Range	T_{OPR}	-25 ~ +85	0 ~ +70	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	-65 ~ +150	-65 ~ +150	°C

Electrical Characteristics

(V_{CC} = 5.0V, V_{EE} = GND, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	LM258			LM358			LM2904			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} -1.5V, $V_{O(P)}$ = 1.4V, R_S = 0Ω	-	2.9	5.0	-	2.9	7.0	-	2.9	7.0	mV
Input Offset Current	I_{IO}	-	-	3	30	-	5	50	-	5	50	nA
Input Bias Current	I_{BIAS}	-	-	45	150	-	45	250	-	45	250	nA
Input Voltage Range	$V_{I(R)}$	V_{CC} = 30V (LM2904, V_{CC}=26V)	0	-	V_{CC} -1.5	0	-	V_{CC} -1.5	0	-	V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V (LM2904, V_{CC}=26V)	-	0.8	2.0	-	0.8	2.0	-	0.8	2.0	mA
		R_L = ∞, V_{CC} = 5V	-	0.5	1.2	-	0.5	1.2	-	0.5	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L = 2kΩ, $V_{O(P)}$ = 1V to 11V	50	100	-	25	100	-	25	100	-	V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC}=30V (VCC =26V for LM2904) R_L = 2kΩ	26	-	-	26	-	-	22	-	-	V
		V_{CC}=30V (VCC =26V for LM2904) R_L= 10kΩ	27	28	-	27	28	-	23	24	-	V
	$V_{O(L)}$	V_{CC} = 5V, R_L= 10kΩ	-	5	20	-	5	20	-	5	20	mV
Common-Mode Rejection Ratio	CMRR	-	70	85	-	65	80	-	50	80	-	dB
Power Supply Rejection Ratio	PSRR	-	65	100	-	65	100	-	50	100	-	dB
Channel Separation	CS	f = 1kHz to 20kHz (Note1)	-	120	-	-	120	-	-	120	-	dB
Short Circuit to GND	I_{SC}	-	-	40	60	-	40	60	-	40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V, V_{CC} = 15V, $V_{O(P)}$ = 2V	20	30	-	20	30	-	20	30	-	mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V, V_{CC} = 15V, $V_{O(P)}$ = 2V	10	15	-	10	15	-	10	15	-	mA
		$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V, V_{CC} = 15V, $V_{O(P)}$ = 200mV	12	100	-	12	100	-	-	-	-	μA
Differential Input Voltage	$V_{I(DIFF)}$	-	-	-	V_{CC}	-	-	V_{CC}	-	-	V_{CC}	V

Note:

1. This parameter, although guaranteed, is not 100% tested in production.

FAIRCHILD
SEMICONDUCTOR®

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MC78XX/LM78XX/MC78XXA

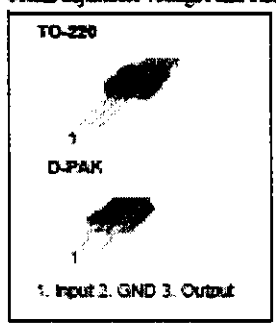
3-Terminal 1A Positive Voltage Regulator

Features

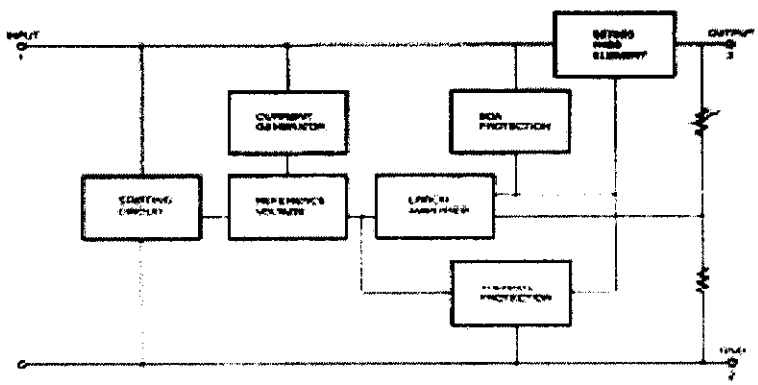
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Digram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V		4.75	5.0	5.25	
Line Regulation (Note1)	Regline	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation (Note1)	Regload	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	μV/Vo
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics

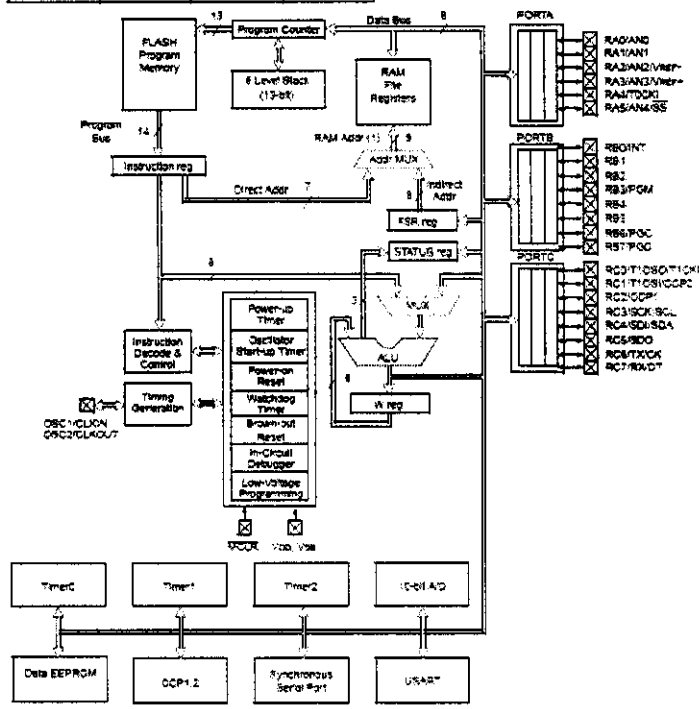
T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C	5.0							µA
	T_A = 100°C	500							µA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

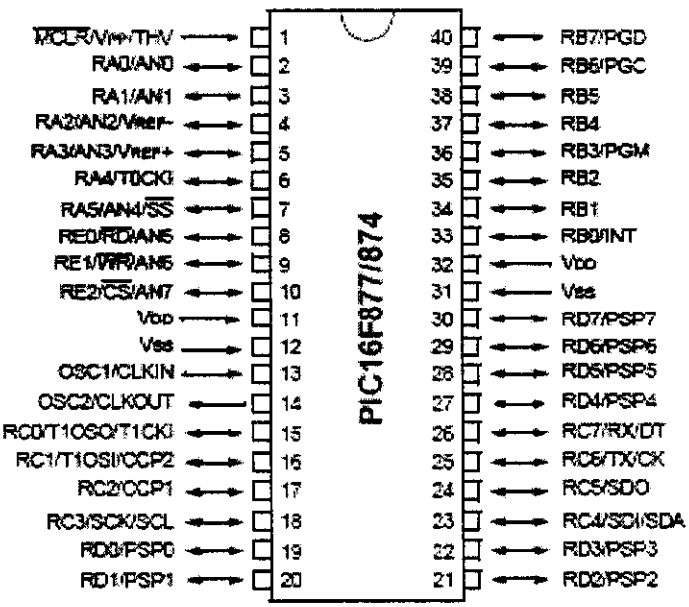
APPENDIX II

ARCHITECTURE OF PIC 16F877A

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F873	4K	192 Bytes	128 Bytes
PIC16F876	8K	368 Bytes	256 Bytes



Pin Configuration of PIC16F877A



TIMER 0 CONTROL REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7: **RBPU**

bit 6: **INTEDG**

bit 5: **T0CS**: TMR0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

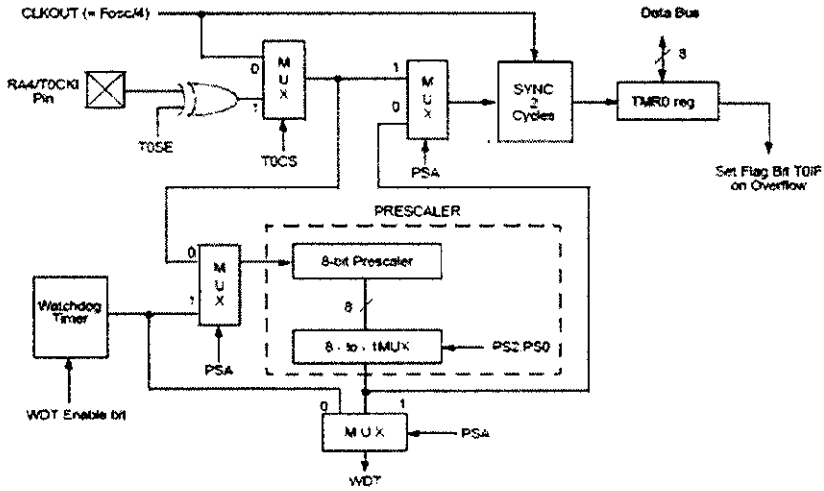
bit 3: **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2 PS1 PS0**: Prescaler Rate Select bits

TIMER 0 BLOCKS DIAGRAM:



TIMER 1 CONTROL REGISTERS:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled

0 = Oscillator is shut off (The oscillator inverter is turned off to eliminate power drain)

bit 2: **T1SYNC**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1

1 = Do not synchronize external clock input

0 = Synchronize external clock input

TMR1CS = 0

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)

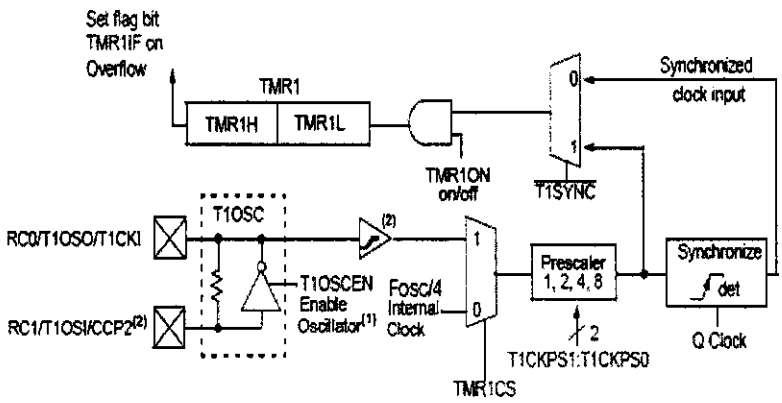
0 = Internal clock (FOSC/4)

bit 0: **TMR1ON**: Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

TIMER 1 BLOCK DIAGRAM:



TIMER 2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale

0001 = 1:2 Postscale

0010 = 1:3 Postscale

1111 = 1:16 Postscale

bit 2: **TMR2ON**: Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

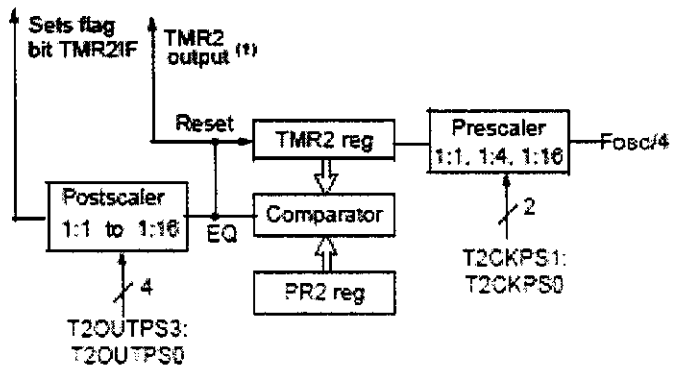
bit 1-0: **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

TIMER2 BLOCK DIAGRAM:



CCP1CON REGISTER/CCP2CON REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX :CCPxY**: PWM Least Significant bits

Capture Mode: Unused

Compare Mode: Unused

PWM Mode: These bits are the two LSB s of the PWM duty cycle. The eight MSB s are found in CCPRxL

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets CCPx module)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (CCPxIF bit is set)

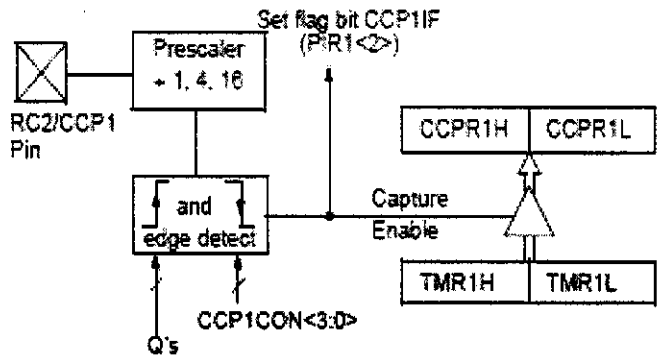
1001 = Compare mode, clear output on match (CCPxIF bit is set)

1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)

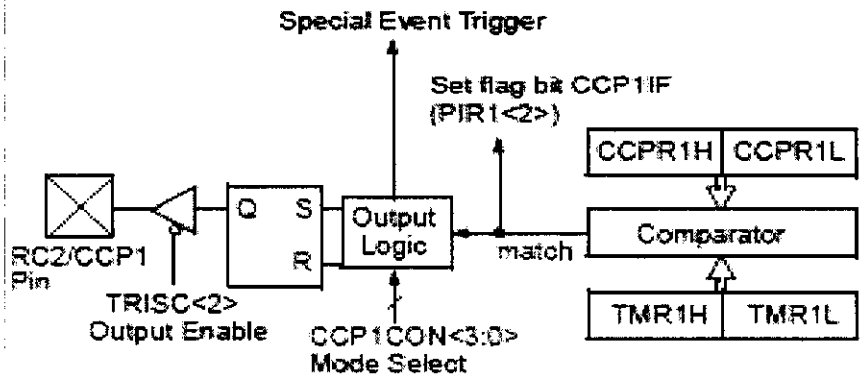
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)

11xx = PWM mode

CAPTURE MODE OPERATION BLOCK DIAGRAM:



COMPARE MODE OPERATION BLOCK DIAGRAM:



N-channel enhancement mode TrenchMOS™ transistor

IRFZ44N

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in switched mode power supplies and general purpose switching applications.

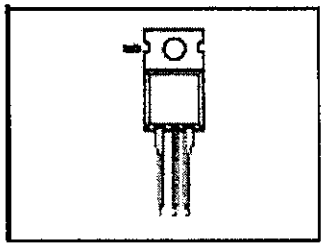
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	49	A
P_{tot}	Total power dissipation	110	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	22	mΩ

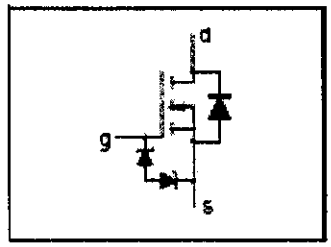
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	49	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	35	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	110	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\,j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.4	K/W
$R_{th\,j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55°C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175°C	1.0	-	-	V
		T_j = -55°C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175°C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	22	mΩ
		T_j = 175°C	-	-	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1350	1800	pF
C_{oss}	Output capacitance		-	330	400	pF
C_{rss}	Feedback capacitance		-	155	215	pF
Q_g	Total gate charge	V_{DD} = 44 V; I_D = 50 A; V_{GS} = 10 V	-	-	62	nC
Q_{gs}	Gate-source charge		-	-	15	nC
Q_{gd}	Gate-drain (miller) charge		-	-	26	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	50	75	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	40	50	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	49	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

APPENDIX III

```
#include<pic.h>
//__CONFIG(0x1F71);
__CONFIG(0x20E4);
__CONFIG(0x3FFF);
unsigned int V1,V2;
void main()
{
        ANSEL=0;
        ANSELH=0;
        ADCON1=0x80;
        PR2=99;
        CCPR1L=50;
        CCP1CON=0X0C;
        T2CON=0X04;
        TRISD=0XFF;
        TRISC=0XF0;
        TRISB=0;
        TRISA=0x0F;
        PORTC=0;
        PORTB=0xff;
        OPTION=0x87;
//      TMR0=0;
//      GIE=PEIE=INTE=T0IE=TMR1IE=1;
//      T1CON =0x01;
//      TMR1L = 0x00;
//      TMR1H = 0x00;
        while(1)
        {
                PORTB=0x00;
                while(TMR0<4);
```

```
PORTB=0x39;
while(TMR0<8);
PORTB=0x96;
while(TMR0<12);
PORTB=0x93;
while(TMR0<16);
PORTB=0x99;
while(TMR0<20);
PORTB=0x99;
while(TMR0<24);
PORTB=0x93;
while(TMR0<28);
PORTB=0x96;
while(TMR0<32);
PORTB=0x39;
while(TMR0<36);
PORTB=0x00;
while(TMR0<40);
PORTB=0x00;
while(TMR0<44);
PORTB=0x36;
while(TMR0<48);
PORTB=0x66;
while(TMR0<60);
PORTB=0x66;
while(TMR0<64);
PORTB=0x63;
while(TMR0<68);
PORTB=0x69;
while(TMR0<72)
```

```
                PORTB=0x36;
                while(TMR0<76);
                PORTB=0x00;
                while(TMR0<80);
                TMR0=0
                }
        while(1);
        }
delay_adc()
{
        unsigned int i;
        for(i=0;i<=400;i++);
}
```