P-3539

Design and implementation of Hybrid regenerative three phase power supply system combining Grid-Tie and UPS functions

A Project Report

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APRIL 2011

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Certified that this project report entitled **"Design and implementation of Hybrid regenerative three phase power supply system combining Grid-Tie and UPS functions"** is the bonafide work of

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Who carried out the project work under my Supervision

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ABSTRACT

A hybrid regenerative power system including photovoltaic (PV) and wind powers and combining the functions of the grid–tie system and uninterruptible power supply (UPS) for critical load applications is presented. The proposed system employs Three phase rectifier and Three phase inverter topology , Also the circuit employs three arm converter (DEF Arms) one arm for battery discharging and two arms for power conversion of the PV module and wind turbine generator. The operation modes include the grid–tie mode and the UPS mode depending on the grid status. A power balance control scheme is presented, which can reduce the grid power and utilize the regenerative power in the most effective way for fulfilling the two requirements of a three-stage power supply without the interruption of the load. Also, the PV and wind powers can be utilized with priority in order to provide the flexibility for adapting to local circumstances. A three-phase 1.2 kW/400 V three phase system is designed and implemented, and the effectiveness of the proposed system and control methodology are verified with some experimental results

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ABBREVATION

PWM	Pulse Width Modulation
WTG	Wind Turbine Generator
PV	Photo Voltaic
MPPT	Maximum Power Point Tracking

CHAPTER 1

CHAPTER 1

1. INTRODUCTION

Due to the fact that environmental concerns have constrained the use of polluted energy resources for electric power generation, the interest in looking for possible alternatives concerning clean and renewable energy sources is growing worldwide. The increasing number of renewable energy sources and distributed generators requires new control strategies for the operation and management of the power converters in order to maintain the reliability and improve the flexibility and quality of the new power supply system embedded with complex energy conversion units. In recent years, the wind turbine generator (WTG) and photovoltaic (PV) generation technologies have brought opportunities for utilizing wind and solar resources for electric power generation.

It is well known that renewable energy sources have unpredictable random behaviors; however, some of them, such as solar radiation and wind speed, have complementary features in many aspects. It has been reported that , the WTG/PV hybrid systems better than a single WTG or PV generation since it suppresses rapid changes in the output power of the single source such as the wind turbine system. In addition, based on the research results reported in, the grid interface of the WTG/PV hybrid system equipped with a battery storage/supply unit can greatly improve the system reliability and operating flexibility. Based on the operating functions, there are a number of possible system configurations in designing the WTG/PV hybrid system.

The stand-alone system configuration can provide a well-regulated load voltage but the reliability of power supply cannot be fully guaranteed, to overcome the above shortcoming a grid-supported stand-alone system configuration that has a well-regulated load voltage and also has a reliable three stage supply to the load by the means of (Grid, WTG & PV, battery bank). A grid–tie hybrid system allowing the injection of extra power from the WTG and PV to the load. In some design cases, the stand-alone and grid–tie configurations are combined to achieve better operating flexibility. It should be noted that the load voltage in these two configurations is not regulated and will be floating with the grid voltage.

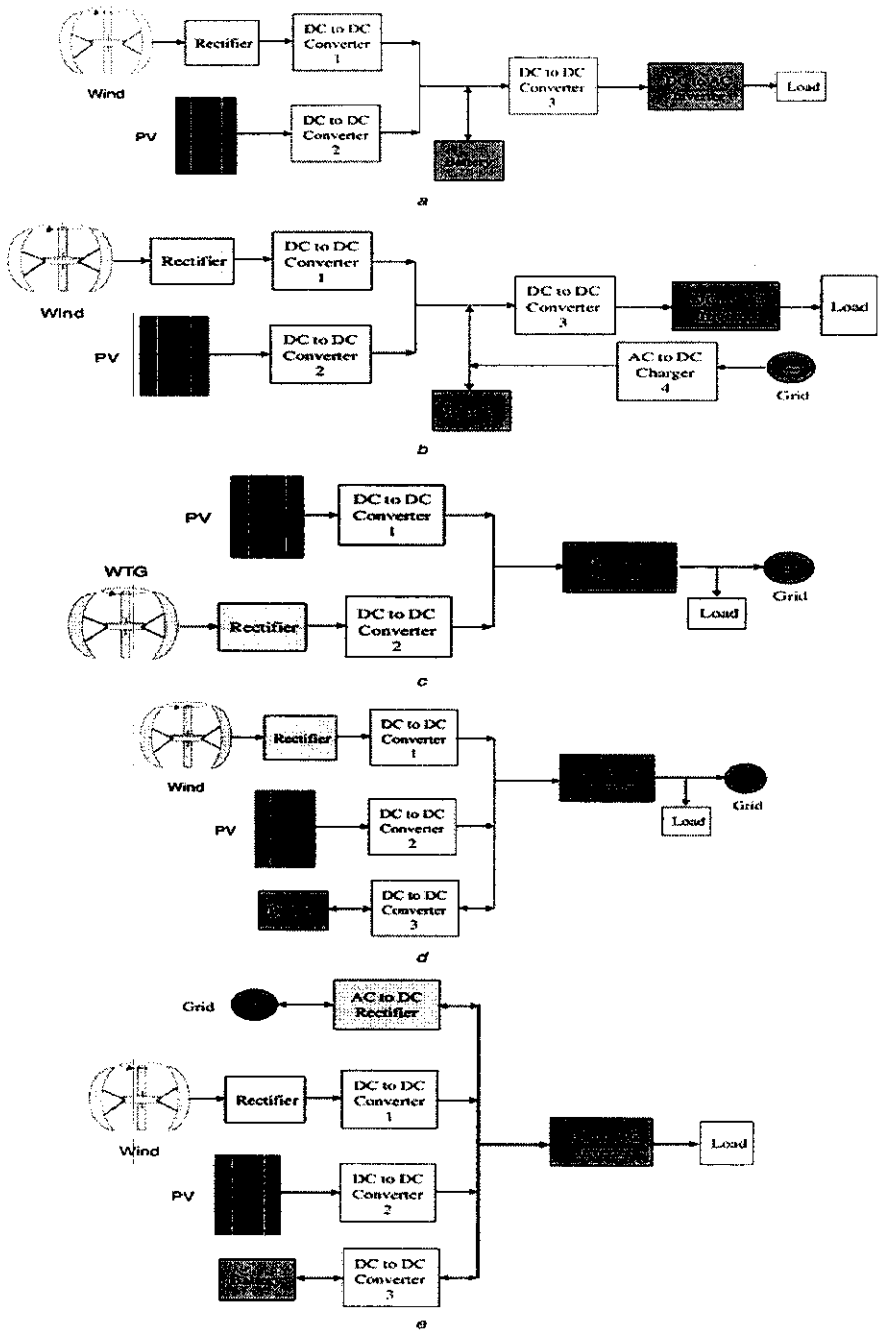


Fig 1.1 Possible system configurations in designing the WTG/PV hybrid system

a The stand-alone system

b The grid-supported stand-alone system configuration

c The grid–tie hybrid system configuration

d The combined stand-alone and grid–tie configuration

e The combined UPS and grid–tie configuration

1.1 MODES OF OPERATION

Based on the operating functions, there are a number of possible system configurations in designing the WTG/PV hybrid system as shown above in Fig. 1.1. The stand-alone system configuration shown in Fig. 1.1a can provide a well-regulated load voltage but the reliability of power supply cannot be fully guaranteed. To overcome the above shortcoming, Fig. 1.1b shows a grid-supported stand-alone system configuration that has a well-regulated load voltage and also has a reliable charging source for the battery bank . In low-battery voltage applications such as those shown in Figs. 1.1a and 1.1b, the **DC-to-DC Converter** is required to boost the voltage to a level that is high enough for the rear stage DC-to-AC Inverter; otherwise this stage can be omitted. A grid–tie hybrid system allowing the injection of extra power from the WTG and PV to the grid is shown in Fig. 1.1c . In some design cases, the stand-alone and grid–tie configurations are combined as shown in Fig. 1.1d to achieve better operating flexibility.

It should be noted that the load voltage in these two configurations is not regulated and will be floating with the grid voltage. So, for the critical load applications, the configuration combining on-line uninterruptible power supply (UPS) shown in Fig. 1.1e must be used. In this paper, we propose a Three phase rectifier and Three phase Inverter that Grid-Tie mode by connecting Grid and Load through AC-DC-AC conversion and a Three-arm (DEF Arm) converter Topology with three arms for the PV, WTG and battery to combine the on-line UPS and the grid–tie regenerative power system.

A novel power balance control scheme is presented. It is designed so as to reduce the grid power and utilize the regenerative power in the most effective way and, most importantly, to satisfy the two requirements of a three-stage supply to the load and no interruption of the load for high reliability. In addition, the utilization of PV and wind powers can be designed with priority. This feature is important for adapting to weather variations and local circumstances to enhance the flexibility and performance of the system. The detailed modeling and controller design of the converter is provided. A three-phase 1.2 kW/400 V system is designed and implemented, and the effectiveness of the proposed system and control methodology is verified with some experimental results.

1.2 OBJECTIVES OF THE PROJECT

The objective of this project is to

- To reduce the grid power as much as possible on the premise of ensuring system stability.
- To utilize the regenerative power in the most effective way to the load end.
- Utilizing Hybrid power generation for efficient power delivery

1.3 ORGANIZATION OF THESIS

Report Layout

CHAPTER 1

It describes the general introduction, aim and objective of the project.

CHAPTER 2

It describes the Circuit configuration and Operation modes of the proposed Hybrid generation system.

CHAPTER 3

Deals with the design of input voltage controllers for the PV and WTG converters

CHAPTER 4

Provides the simulation results of existing paper.

CHAPTER 5

Deals with discussion on results

CHAPTER 6

Deals with conclusion

CHAPTER 7

Future scope

CHAPTER 8

Gives the references.

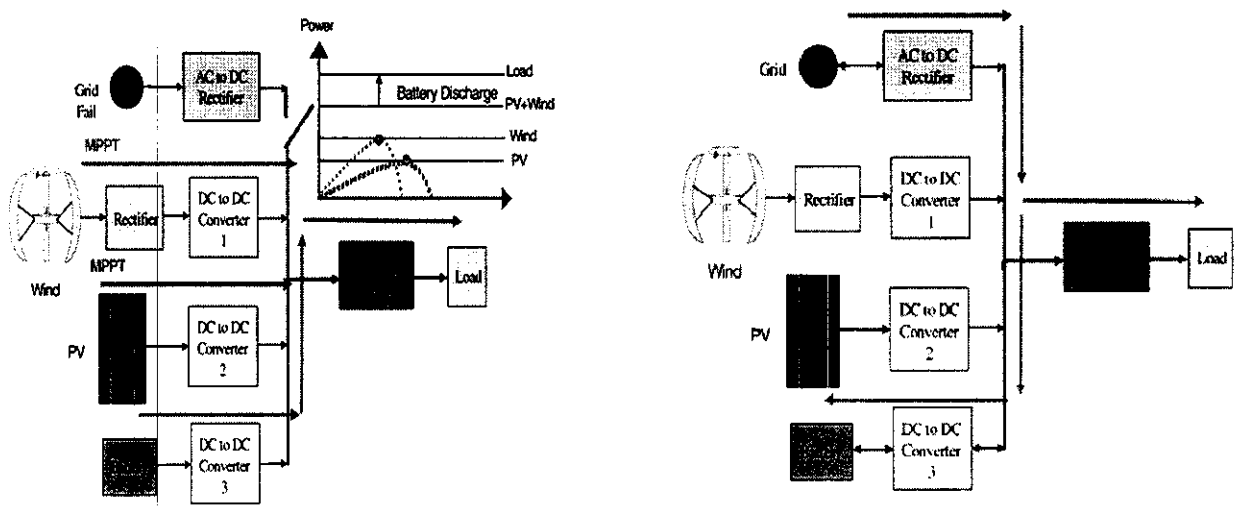
CHAPTER 2

CHAPTER 2

CIRCUIT CONFIGURATION AND OPERATION MODE OF THE PROPOSED HYBRID GENERATION SYSTEM

2.1 SYSTEM DESCRIPTION AND OPERATING MODES:

According to the status of the grid, the proposed system can be divided into the grid–tie mode and the UPS mode. In practical operations, the grid–tie mode and the UPS mode also can be catalogued into two and three operation modes, respectively, based on various conditions of the PV, WTG, battery bank and the grid. In the grid–tie mode, the PV and WTG are operated at their maximum power point (MPP). As shown in Fig. 2.1a, if the total output power from the PV and WTG is higher than the load demand, The power from the (PV, WTG, BATTERY) is supplied to the load, At the same time as shown in the Fig. 2.1b if the GRID power fails as in the mode 2 the (PV, WTG, BATTERY) supplies the load until the grid status works again and this mode is meant as UPS mode.



(a) The discharge mode **(b)** The grid supply mode

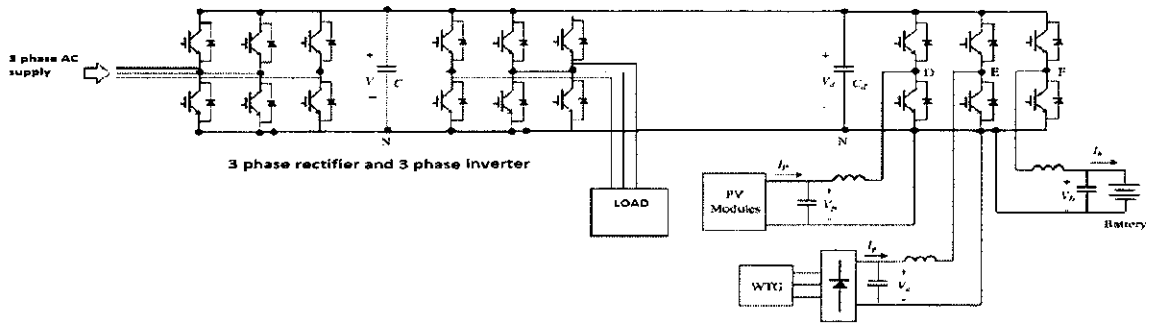
fig 2.1 Modes of Operation

2.2 POSSIBLE SYSTEM CONFIGURATION IN DESIGNING THE WTG/PV HYBRID SYSTEM :

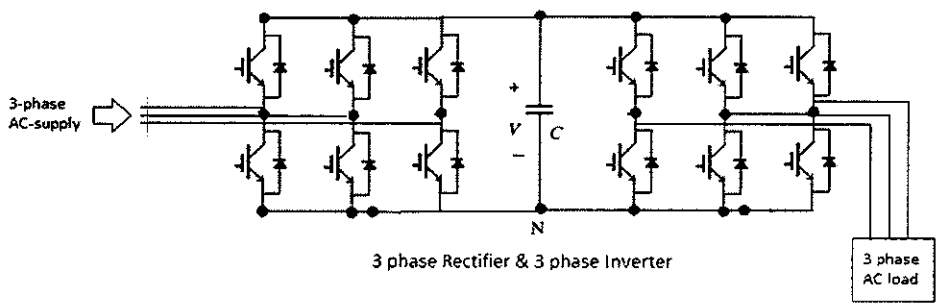
The three phase rectifier and three phase inverter for AC-DC-AC conversion is proposed in this paper, This connects the Grid and the load, Along with that a three arm converter topology with three arms for the UPS rectifier–inverter and three arms for the PV, WTG and battery to combine the on-line UPS and the grid–tie regenerative power system. A novel power balance control scheme is presented. It is designed so as to reduce the grid power and utilize the regenerative power in the most effective way and most importantly to satisfy the two requirements of a three-stage supply to the load demand and no interruption of the load for high reliability. In addition, the utilization of PV and wind powers can be designed with priority. This feature is important for adapting to weather variations and local circumstances to enhance the flexibility and performance of the system. The detailed modeling and controller design of the converter is provided. A three phase 1.2 kW/400 V system is designed and implemented, and the effectiveness of the proposed system and control methodology is verified with some experimental results.

2.3 THREE PHAS RECTIFIER AND THREE PHASE INVERTER:

The three phase rectifier and three phase inverter for AC-DC-AC conversion is proposed in this paper, This connects the Grid and the load. This circuit employs a Three phase rectifier and three phase inverter , The 400V, 50 Hz voltage obtained at secondary of the Wye/Delta transformer is first rectified by a six pulse diode bridge. The filtered DC voltage is applied to an IGBT two-level inverter generating 50 Hz. The IGBT inverter uses Pulse Width Modulation (PWM) at a 2 kHz carrier frequency. The circuit is discredited at a sample time of 2.



(a)



(b)

Fig 2.2 **a.** Three phase rectifier and Three phase inverter and 3 Arm converter (DEF Arms)

b. Three phase rectifier and Three phase inverter.

CHAPTER 3

CHAPTER 3

MODELLING AND CONTROLLER DESIGN OF THE 3 ARM CONVERTERS (DEF ARMS):

Based on the need of balancing power flow and performing the energy management functions developed in all operating modes shown in Fig. 2.1 , the required controllers designed for the DEF arms are presented in Fig. 4.2 b. For both the PV module and WTG, the same control structure can be applied; that is, the outer loop is designed for performing MPPT functions and to give the voltage commands, whereas the inner loop is dedicated for the required voltage controller to track the voltage commands. The duty parameters for the converters can then be decided by the regulated voltages operating with a PWM unit. Since the F-arm is designed for charging and discharging the battery bank, regulating DC-link voltage and balancing Power in real time, the related controllers is to be designed.

3.1 DESIGN OF INPUT VOLTAGE CONTROLLERS FOR THE PV AND WTG CONVERTERS:

Due to that fact that the same control structure and design method can be used for developing the related voltage controllers used in the PV and WTG, in this subsection, only the design details concerning the PV module are addressed. In this particular application case, the voltage to be regulated is on the input side of the converter rather than the voltage at its output terminal. To design the voltage controller, the transfer function describing the input voltage and the controlled voltage must be derived first. The designed converter system can be treated as a boost-type converter as shown in Fig. 4, in which the outputs of PV or WTG are modeled as a current source. Although the PV module characteristic is equivalent to a voltage source in series with a resistance near the MPP as well as the negative dP/dVp region, it can also be equivalent to a current source like the positive dP/dVp equations can be formulated

$$LdIi/dt = Vp- (1 - D) Vd \quad (1)$$

$$CdV/dt =Ip - Ii \quad (2)$$

$$ReCdV/dt þ V =Vp \quad (3)$$

In the continuous current mode (CCM), the ratio of input voltage and output voltage must satisfy the following expression

$$Vp =(1 - D)Vd \quad (4)$$

In the steady state

$$Ip=Ii \quad (5)$$

Applying a small disturbance to and using linearization techniques, one can have the small signal model of the converter formulated as follows

$$LdI\ i/dt =Vp + VdD \quad (6)$$

$$CdV/dt= - I\ i \quad (7)$$

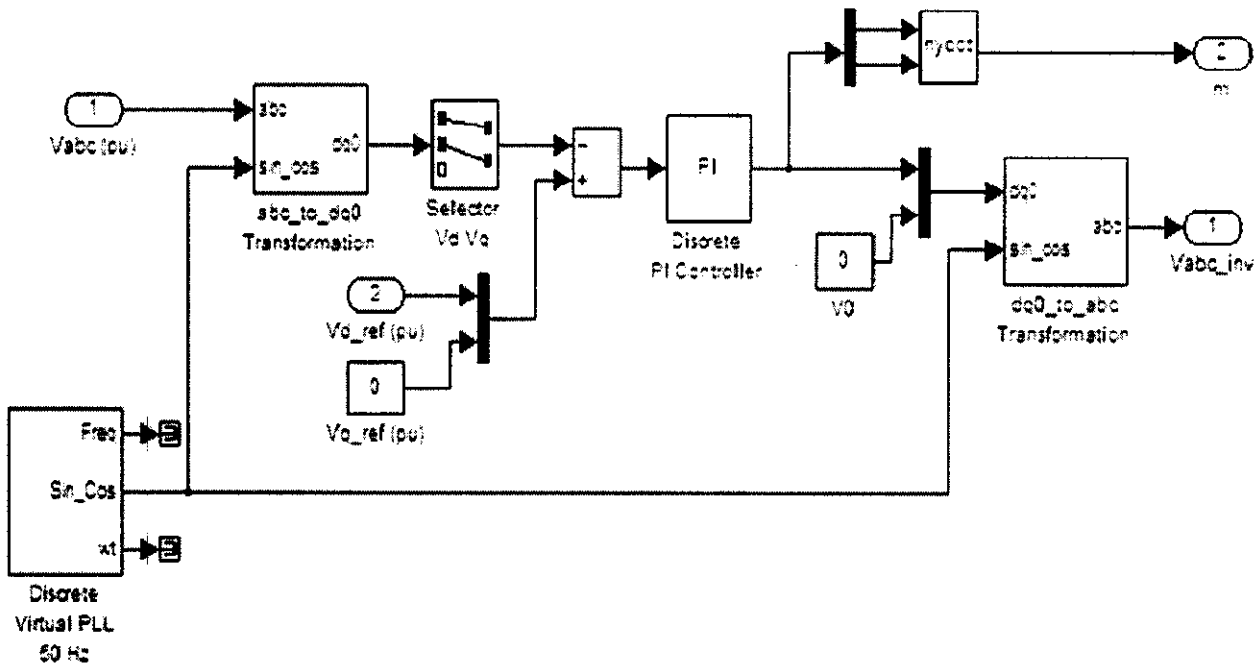
$$ReC\ dV/dt + V= Vp \quad (8)$$

By applying the Laplace transformation to (6 to 8) the transfer function of input voltage of the converter to thecontrol duty can be obtained as expressed in

$$V\ þ/D=[-(ReVb=L)\ (s\ þ\ (1=CRe)]\ /\ [S2\ þ\ Re=L)sþ(1=LC)] \quad (9)$$

3.2CONTROL CIRCUITS:

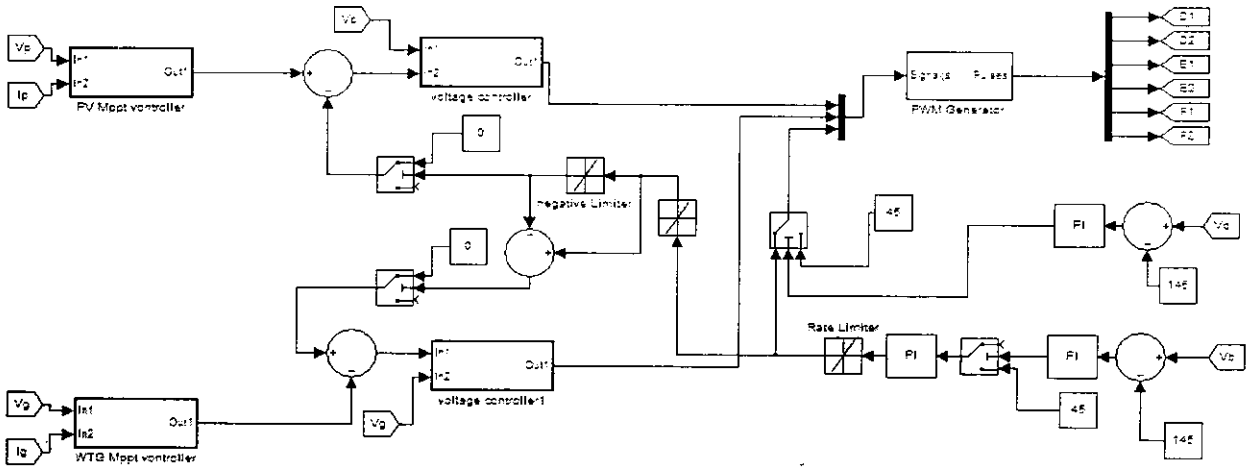
3.2.1 CONTROL CIRCUIT OF THREE PHASE RECTIFIER AND THREE PHASE INVERTER:



3.1 a. control circuit of three phase rectifier and three phase inverter

The load voltage is regulated at 1 pu by a PI voltage regulator using abc_to_dq and dq_to_abc transformations. The first output of the voltage regulator is a vector containing the three modulating signals used by the PWM Generator to generate the 6 IGBT pulses. The second output returns the modulation index.

3.2.2CONTROL CIRCUIT OF 3 ARM CONVERTER (DEF ARMS):



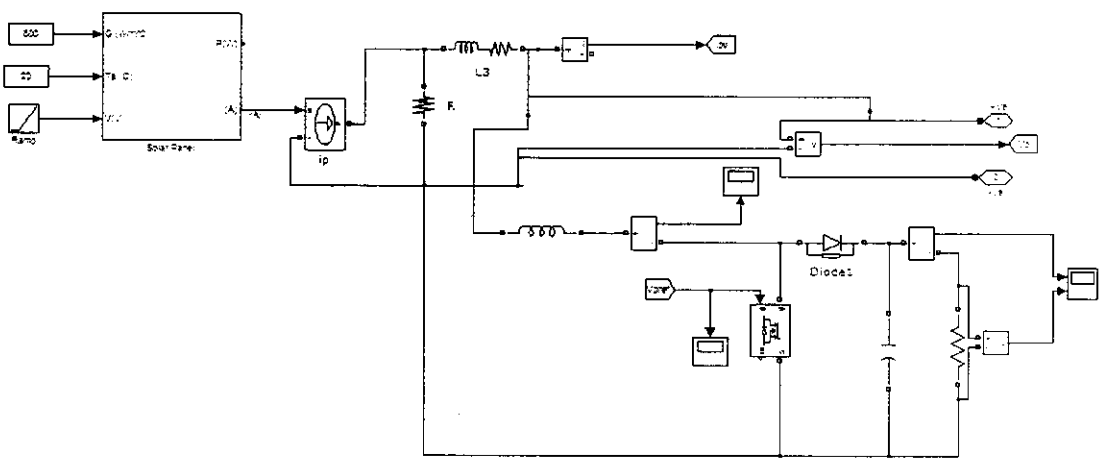
3.1 b control circuit of 3 arm converter (def arms)

In Figs. 3.1b MS1–MS3 is, respectively, the mode selecting switches for the PV, WTG and battery charger. In the grid– Tie operating mode, as shown in Figs. 2.1 a and b,

The DC-link voltage is regulated by the rectifier of the three-arm rectifier and three phase inverter. Both MS1 and MS2 are set to 0 to allow the PV and WTG to be operated at their MPP by the Designed MPPT controllers, and the MS3 of the battery arm (F-arm) is switched to receive the control signals from the battery charger. The charging current command is obtained from the voltage regulator of the charge controller with a limiter for setting the constant charging current level. The inner control loop of the charging controller is a current regulator designed to track the charging current command via a PWM control signal. When a grid blackout occurs, the system is switched to the UPS mode and the rectifier-arm (A-arm) of the three-arm rectifier–inverter is stopped. In this case, the MS3 will immediately connect the control signal of the battery-arm to the output of the DC voltage controller to take over the DC-link voltage regulation. For preventing over-current during the grid–tie mode and UPS-mode transition Period, the battery-arm has added a current limitation loop to provide damping of the response and protect the power switches as well.

This voltage control signal with direction information is accumulated with a memory cell and operated with a gain factor (Gain 2) to adjust the control voltage within a proper range. The summation of this control voltage and a given initial voltage (init voltage) passes through a limiter (Limiter 2). The open loop voltage of the PV module is chosen as the initial voltage to make the MPPT start working from that voltage and Limiter 2 is designed for setting the voltage operating range of the PV module. In this particular arrangement, the proposed MPPT controller is adaptive, that is, its adjusting speed of the MPPT is proportional to the slope of DP/DVp and the maximum adjusting speed is limited by Limiter 1. This design enables the MPPT to achieve a fast and precise tracking objective. The HCS method of the WTG in the proposed paper also employs the same MPPT controller as the PV module, except that the sampling time is longer to consider the WTG having a larger mechanical time constant.

3.4 PHOTO VOLTAIC CELL MODEL:



3.4 Photo voltaic cell connected to Boost converter circuit

Photo voltaic cell connected to boost converter circuit shown in Fig 3.4 .The inputs of PV module are irradiance, temperature and the output is converted to a current source and then boosted, After boosting the DC voltage the terminals are connected to one of the arms of the DEF Arm controller. The output depends upon the amount of irradiance and temperature.

CHAPTER 4

CHAPTER 4

SIMULATION MODULE OF THE PROPOSED HYBRID REGENERATIVE SYSTEM

4.1 MATLAB

The name MATLAB stands for matrix laboratory. MATLAB is a high-performance language for technical computing. It Integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. In this project the modeling and simulation of the proposed system is done using MATLAB (using simulink and power system block set tool boxes).

SIMULINK

Simulink is a software package for modeling, simulating, and analyzing non linear dynamical systems. It is a graphical mouse-driven program that allows somebody to model a system by drawing a block diagram on the screen and manipulating it dynamically. Simulink is a platform for multi domain simulation and Model-Based Design for dynamic systems. It provides an interactive graphical environment and a customizable set of block libraries, and can be extended for specialized applications.

POWER SYSTEM BLOCK SET

The Power System Block set allows scientists and engineers to build models that simulate power systems. The block set uses the Simulink environment, allowing a model to be built using click and drag procedures. Not only can the circuit topology be drawn rapidly, but also the analysis of the circuit can include its interactions with mechanical, thermal, control, and other disciplines. Sim Power Systems extends Simulink with tools for modeling and simulating basic electrical circuits and detailed electrical power systems. These tools let you model the generation, transmission, distribution, and consumption of electrical power, as well as its conversion into mechanical power. Sim Power Systems is well suited to the development of complex, self-contained power systems, such as those in automobiles, aircraft, manufacturing plants, and power utility applications

4.2 SIMULATION CIRCUIT:

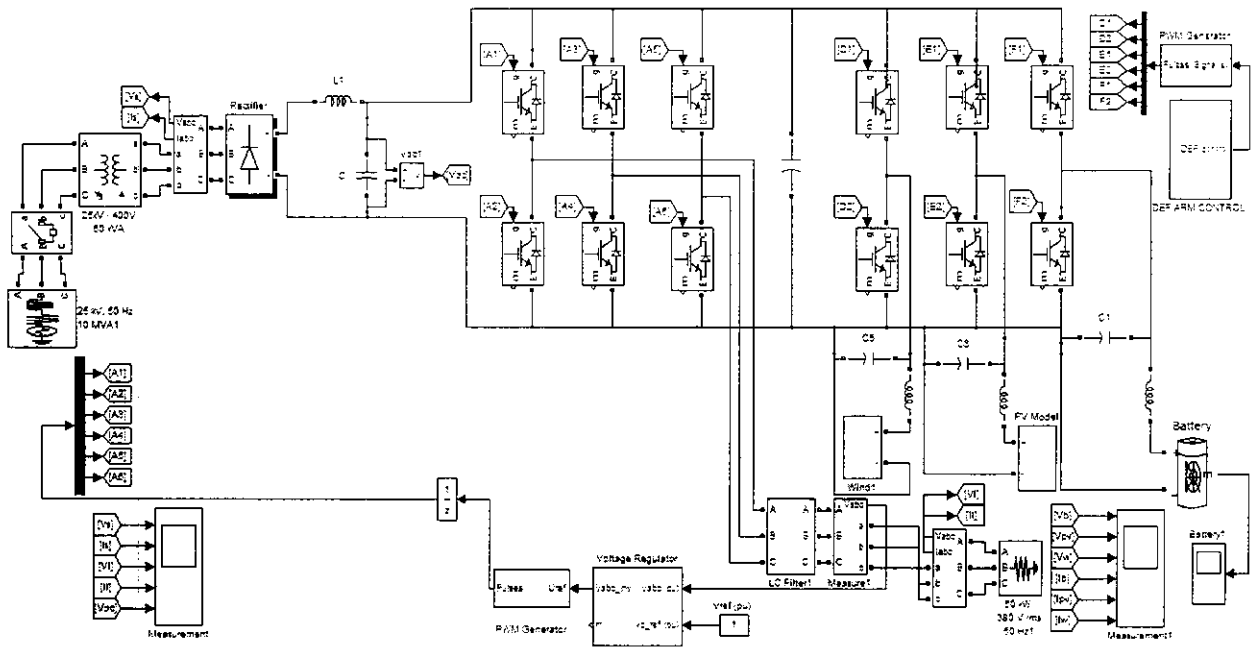


Fig 4.1 overall simulation circuit

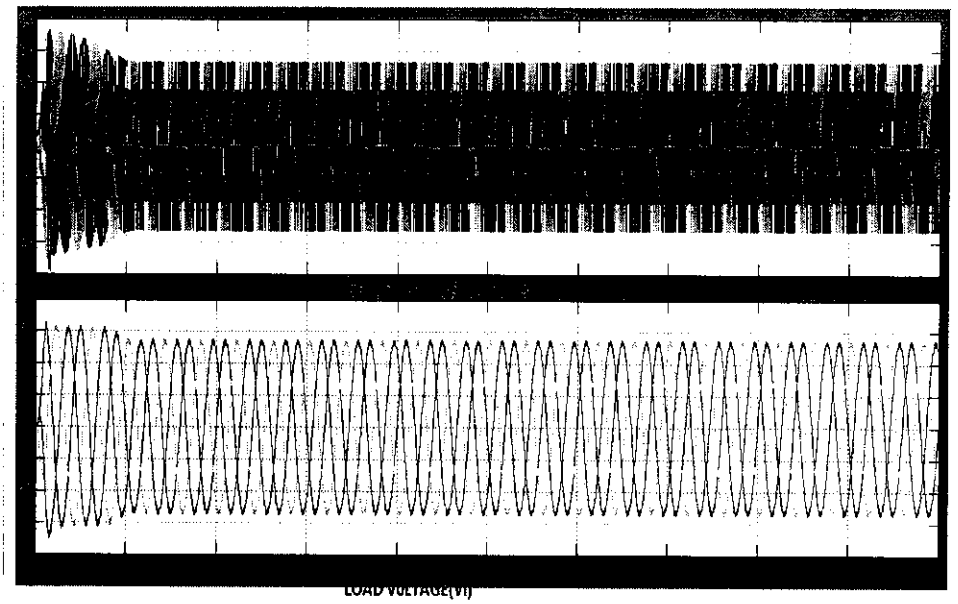
In the Fig 4.1 the circuit can be classified into two parts as Grid-Tie mode and UPS mode operation. The input is 1.2KV/400 V three phase supply .The DC link voltage Vdc is taken as reference and is monitored by the DEF Arms controller. The load is regulated by the PI controller when the grid is working properly, when the grid fails immediately the DEF arm switches starts controlling the Load regulation by switching the PV, Wind Turbine Generator WTG and Battery as per the available renewable energy power from individual renewable energy source and battery. The control is provided from the 6 pulse PWM control. Either one of the mode is operated at a time.

TABLE.1 Specifications of the Simulation Circuit

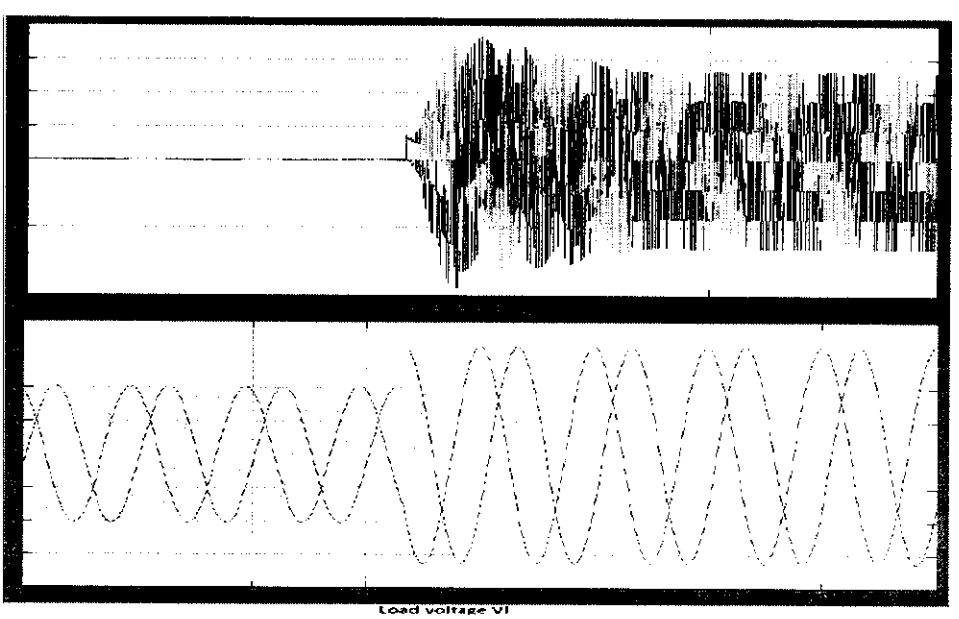
Sl.No	Source/Elements	Parameter specification
1	AC Source	1.2KV/400 50 Hz
2	DC Link Voltage	400 V
2	IGBT	Resistance Ron(Ohm) = 0.001 Ohm Inductance Lon (H) = 0 H Forward voltage V_f = 1 V Current 10% fall time T_f = 1e-6 s Current tail time T_t = 2e-6 s Initial Current Ic = 0 A Snubber resistance Rs (Ohms) = 1e5 Ohm Snubber capacitance Cs (F) = inf
3	Rectifier	Resistance Ron(Ohm) = 0.001 Ohm Inductance Lon (H) = 0 H Forward voltage V_f = 0.8 V Initial Current I_c = 0 A Snubber resistance Rs (Ohms) = 100 Ohm Snubber capacitance Cs (F) = 0.1e-6 F
4	Inductance (L_r)	Inductance (H) = 200e-6 H Resistance Ron(Ohm) = 0.001 Ohm Inductance Lon (H) = 0 H Forward voltage V_f = 0.8 V
5	Capacitance (C_r)	Capacitance (F) = 5000e-6 F
6	DC Link Capacitance (Cdc)	Capacitance(F) = 5000e-6F
7	Pulse (P1) Pulse (P2)	Pulse type = Time based Time (t) = use simulation time Amplitude = 1 Period (Secs) = 0.001 sec Pulse Width (% of period) = 25 Phase delay (Secs) = 0 sec Pulse type = Time based Time (t) = use simulation time Amplitude = 1 Period (Secs) = 0.001 sec Pulse Width (% of period) = 50 Phase delay (Secs) = 0.00025 sec
8	Resistance (R)	Resistance (Ohms) = 80 (Ohms)

9	Wind Power Generator module (3 phase Asynchronous Generator)	Rotor type : Squirrel Cage Nominal power = 275e3 Voltage = 400V Frequency = 50Hz Stator Resistance Rs, Inductance Ls = 0.016 ohm, 0.06H Rotor Resistance Rr, Inductance Lr = 0.015 ohm, 0.06H Mutual Inductance Lm = 3.5 pu
10	P V module	Irradiance = 800 W/m^2 Temprature = 20° C Output Boost voltage (Vpv) = 250 V
11	Battery	Battery type = Lithium-Ion Nominal voltage = 400 V Rated capacity = 4 AH Initial state of charge = 100%

4.3 SIMULATION RESULTS:



(a)



(b)

4.3 a. Grid- tie mode,

b. discharge mode.

CHAPTER 5

HARDWARE IMPLEMENTATION

5.1 BLOCK DIAGRAM

In order to assess the performance of the proposed MPPT based PV power system, as shown in fig.1.13 is designed. In this prototype, module consists of PV panel, boost converter and five-level inverter (MOSFET IRFZ44), MOSFET Driver circuit and PIC microcontroller. Control algorithm is implemented in PIC Microcontroller, to maintain constant Inverter output voltage.

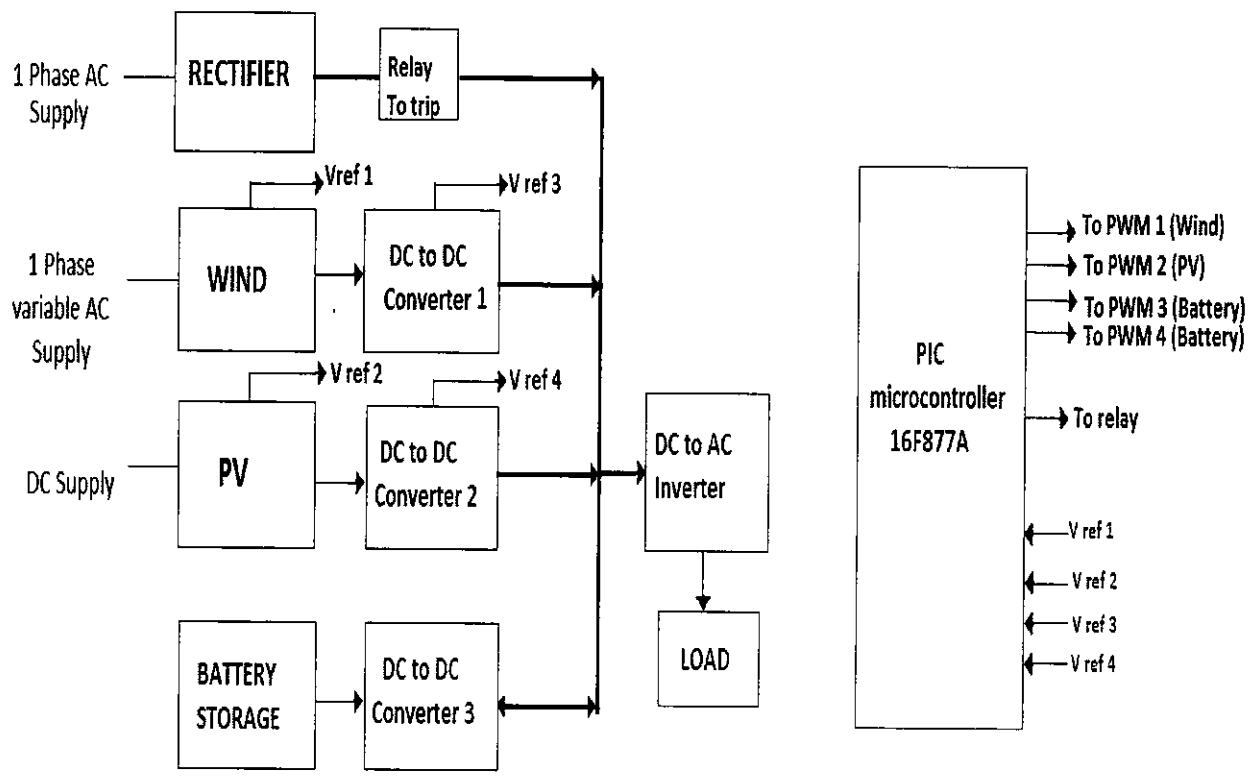


Fig. 5.1. Block diagram of the Prototype

5.2 SCHEMATIC DIAGRAM OF PROPOSED SYSTEM

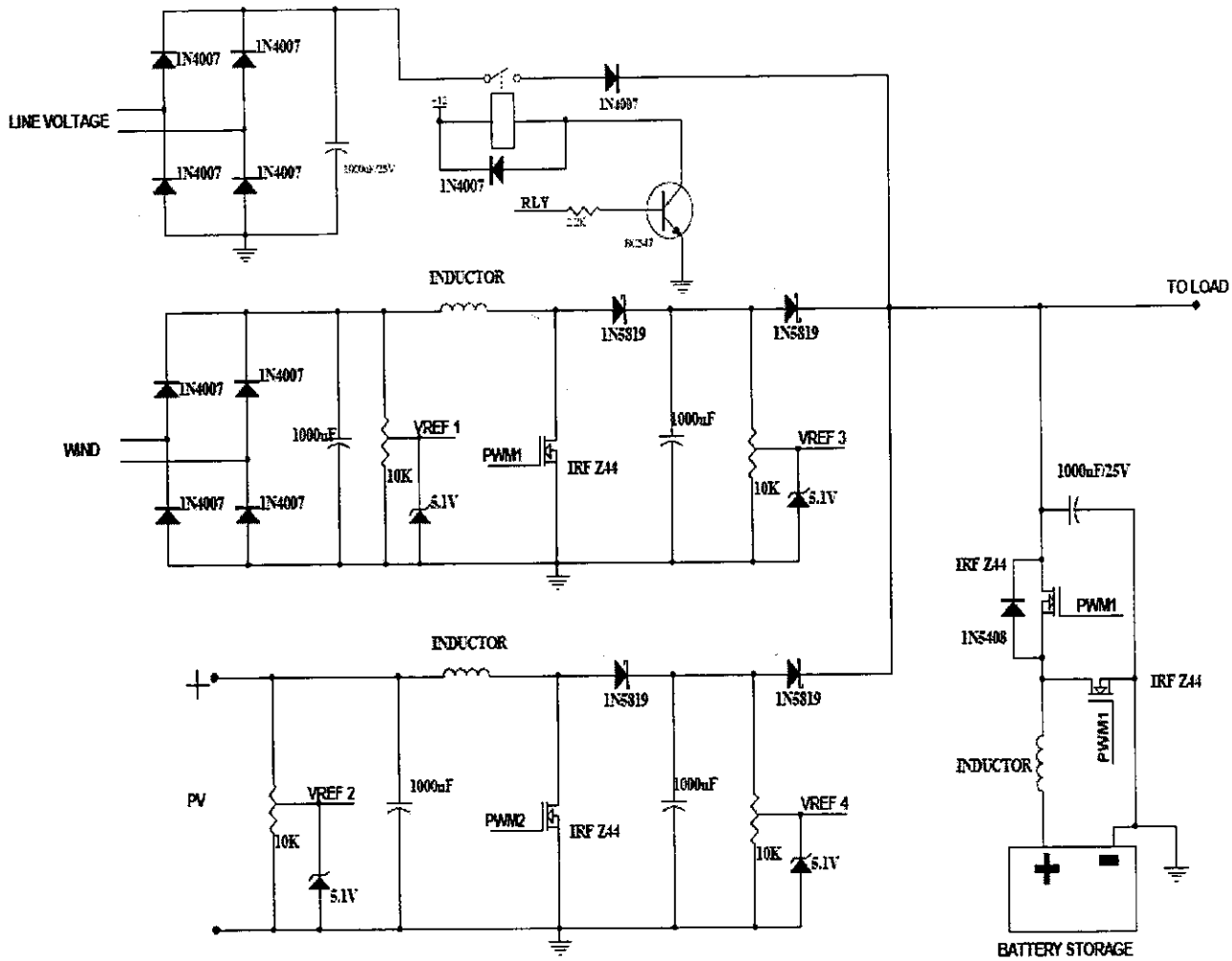


Fig 5.2. Schematic diagram of proposed system

The Fig 5.2 shows the schematic diagram of proposed system, The line voltage is considered as the grid supply voltage , The circuit is designed for single phase system. The PIC microcontroller PIC 16F877A provides the switching signals to the MOSFETS (PWM1, PWM2). The PV, WTG, battery are considered is DEF arms, The line voltage is of 12 V, If the line voltage falls below the reference value automatically the microcontroller switches on the battery, WTG, or PV as per available power, The line voltage (grid supply) is tripped by the means of relay.

5.3DRIVER CIRCUIT

PC817 optocoupler consists of LED and photo diode. TIP 122 is a NPN transistor its collector is connected with the +12V and Emitter is connected with the ground. It is placed between optocoupler and FET because signal from optocoupler is not sufficient to run a FET. This drive is suitable for high current applications. MOSFET driver circuit is shown in fig.1.14. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complementary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory. The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. Flash technology is used in PIC16F877, so that data is retained even when the power is switched off. Easy programming and Erasing are other features of PIC 16F877.

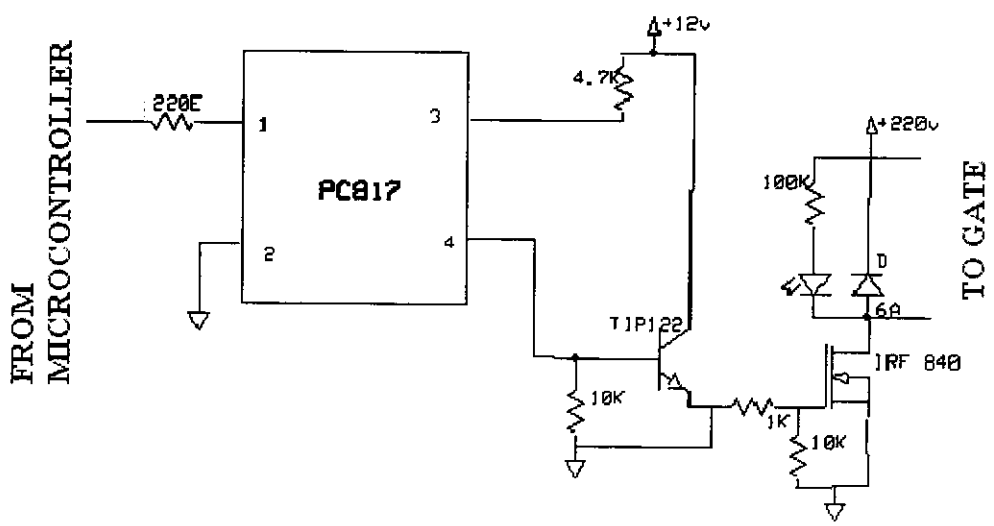


fig.5.3 Driver Circuit

5.4 PIC16F877A MICROCONTROLLER

The microcontroller that has been used for this project is from PIC series. PIC microcontroller is the first RISC based microcontroller fabricated in CMOS (complementary metal oxide semiconductor) that uses separate bus for instruction and data allowing simultaneous access of program and data memory.

The main advantage of CMOS and RISC combination is low power consumption resulting in a very small chip size with a small pin count. The main advantage of CMOS is that it has immunity to noise than other fabrication techniques.

PIC(16F877): Various microcontrollers offer different kinds of memories.EEPROM, EPROM, FLASH etc. are some of the memories of which FLASH is the most recently developed. Technology that is used in PIC16F877 is flash technology, so that data is retained even when the power is switched off. Easy Programming and Erasing are other features of PIC 16F877.

5.4.1. SPECIAL FEATURES OF PIC MICROCONTROLLER:

CORE FEATURES:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed:

  DC-20 MHz clock input

  DC-200 ns instruction cycle
- Up to 18K × 14 words of Flash Program Memory
- Up to 368 × 8 bytes of Data Memory (RAM)
- Up to 256 × 8 bytes of EEPROM data memory
- Pin out compatible to the PIC 16C73/74/76/77
- Interrupt capability (up to 14 internal/ external)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC Oscillator for reliable operation
- Programmable code-protection

- Power saving SLEEP mode
- Selectable Oscillator options
- Low-Power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- In-circuit serial Programming (ICSP) via two pins
- Only single 5V source needed for programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.5V to 5.5V
- High Sink/Source Current: 25mA
- Commercial and Industrial temperature ranges
- Low-power consumption:

Less than 2mA typical @ 5V, 4MHz

Less than 20mA typical @ 3V, 32 KHz

Less than 1mA typical standby current

PERIPHERAL FEATURES:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI. (Master Mode) and I2C. (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIN DIAGRAM OF PIC 16F877A:

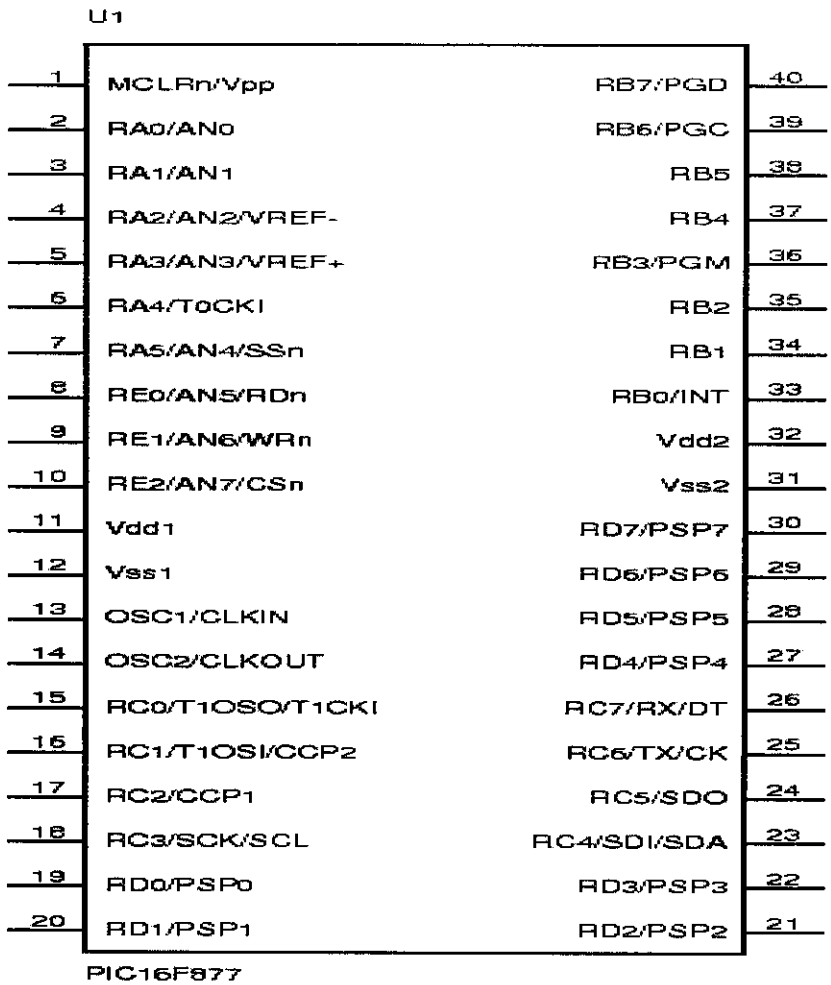


Fig 5.4. Pin diagram of PIC 16F877A

- It has on chip Timers. There are 3 Timers for usage
- It has in built Analog to Digital Converter
- In built Multiplexer availability for signal Selection
- It has serial as well as parallel Communication facilities
- In built Capture, Compare and Pulse width modulation
- It has 5 Ports for Internal and External usage

5.5 HARDWARE TESTING AND RESULTS:

The fabricated Hardware of the proposed system is shown in fig 5.5, The pwm pulses are obtained from the microcontroller, The switching pulses to mosfet is shown in fig 5.6 and 5.7, A

constant 6 V is obtained , Finaly the ac voltage is obtained by the inverter that is connected to the load, The output peak to peak voltage is 24V AC.

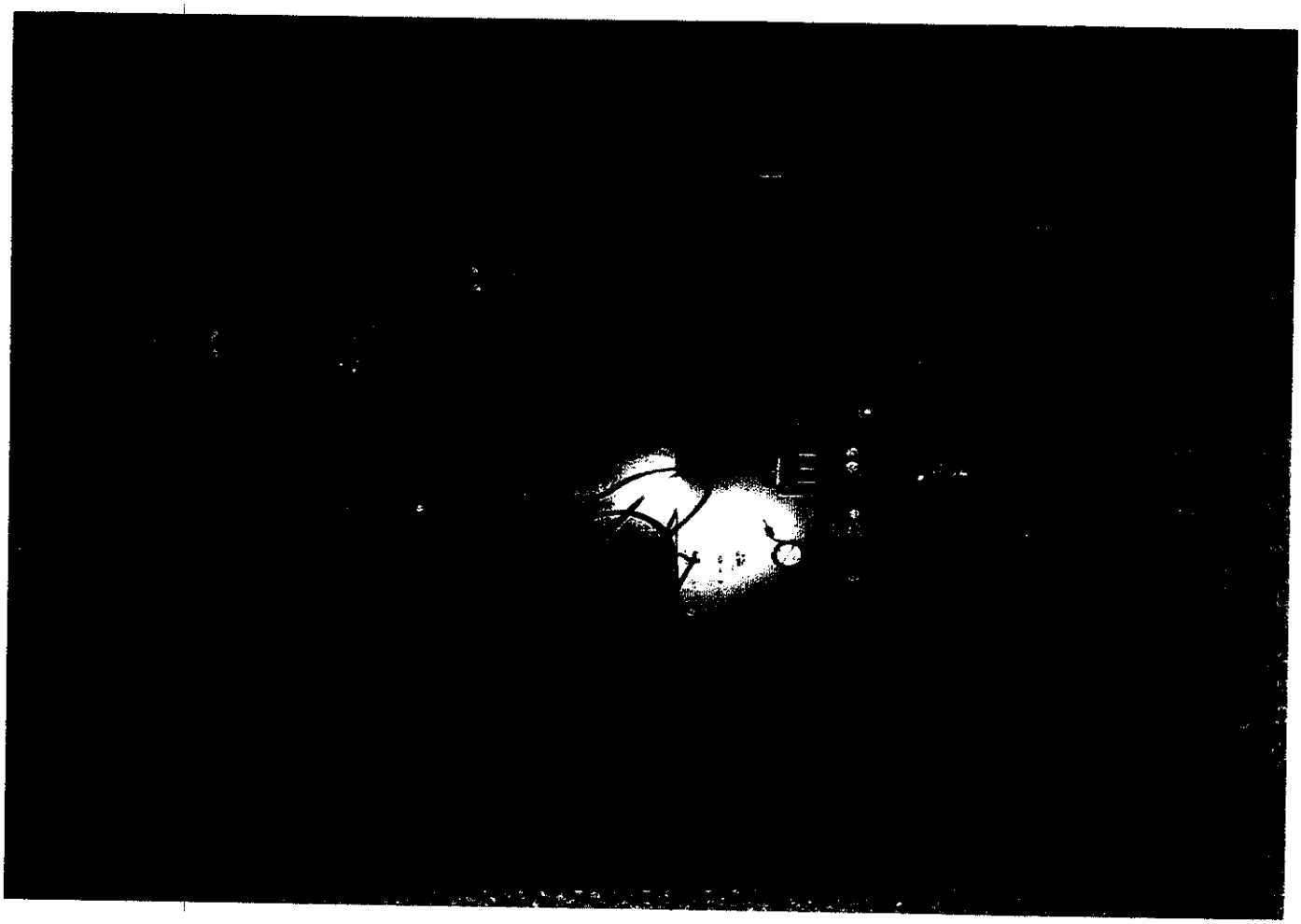


Fig 5.5 photograph of hardware

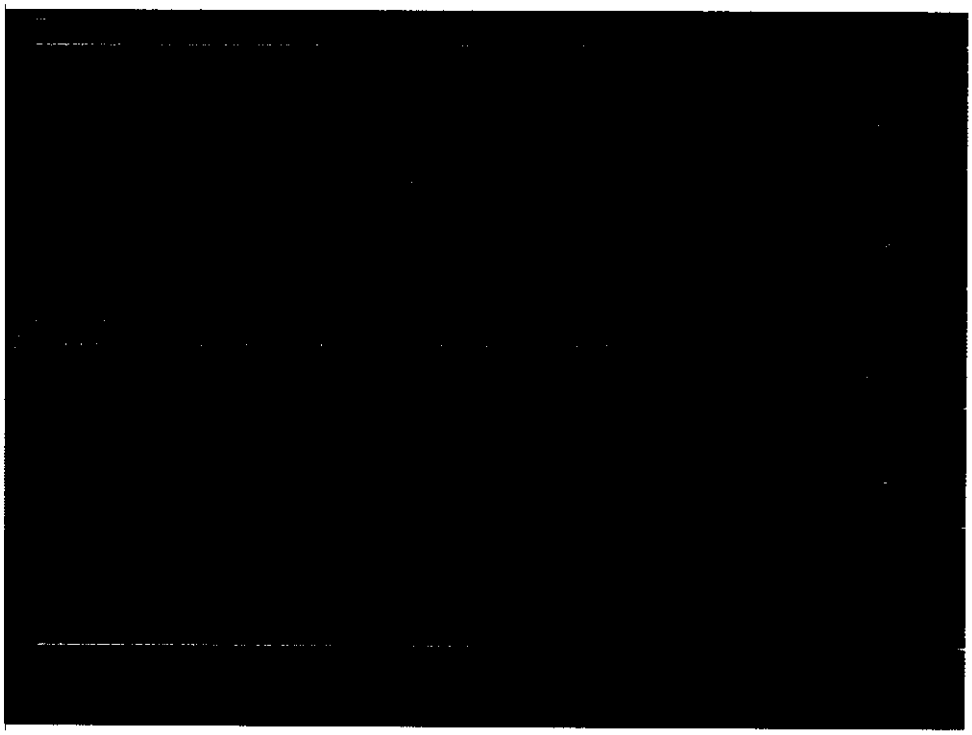


Fig5.6 Switching waveforms of MOSFET Switches

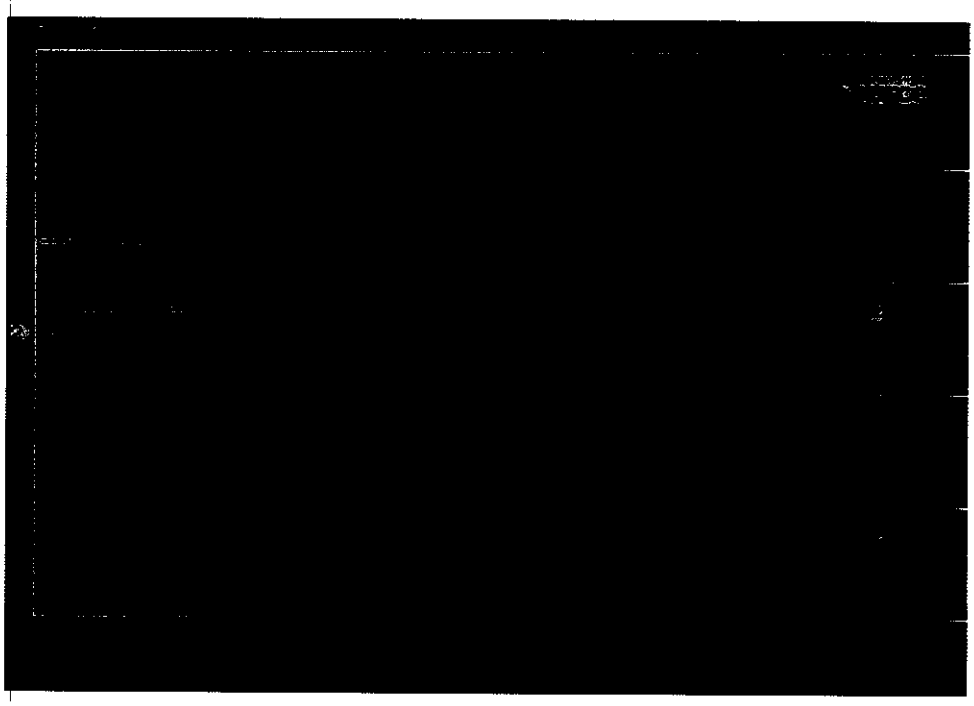


Fig5.7 Switching waveforms of MOSFET Switches

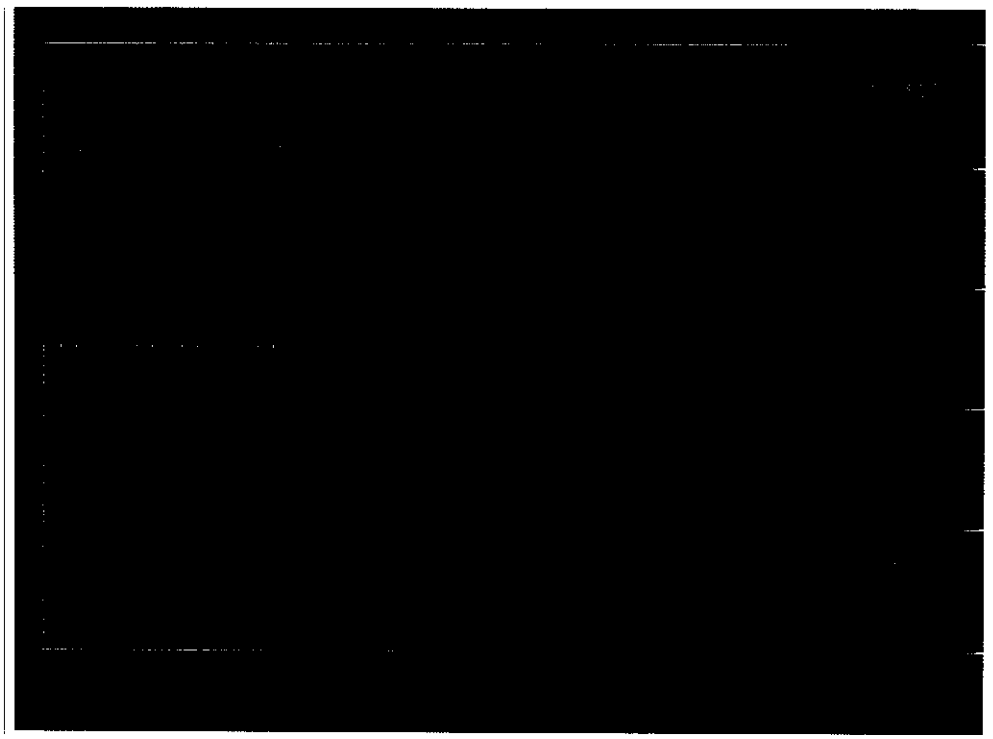


Fig5.8 Output DC voltage

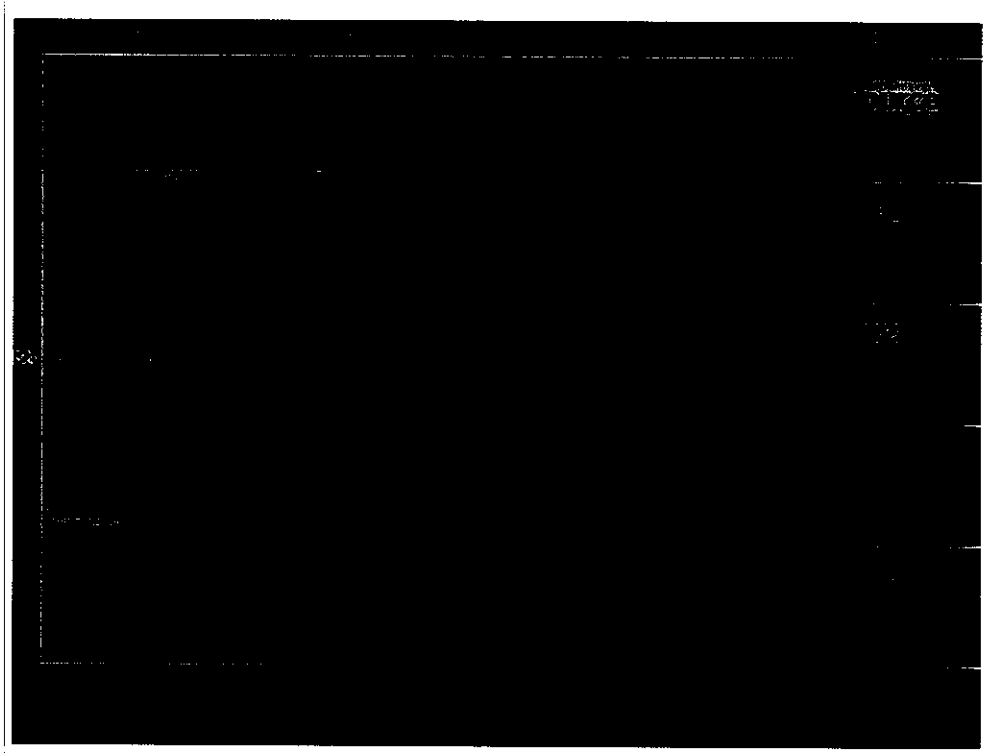


Fig5.9 Inverter output voltage

CHAPTER 6

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1. CONCLUSION:

This paper presented a single phase multilevel inverter for PV application. It utilizes two reference signals and a carrier signal to generate PWM switching signals. The circuit topology, modulation law and operational principle of the proposed inverter were analysed in detail. A PI current control algorithm is implemented in microcontroller to optimize the performance of the inverter. Experimental results indicate that the THD of the five-level inverter is much lesser than that of the conventional three-level inverter. Output voltage and current are in phase at near-unity power factor.

6.2. SCOPE FOR FUTURE WORK:

The system proposed can further be modified by reducing the number of switches which will reduce switching losses and cost of the system, Further this system can be implemented in real time by connecting a Network based computer to the system and its attributes can be monitored through the computer.

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APPENDIX

IRF840B/IRFS840B

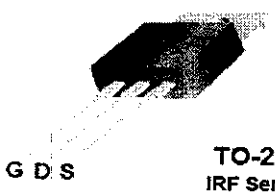
500V N-Channel MOSFET

General Description

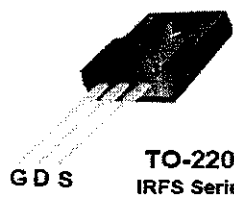
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

Features

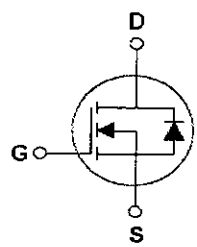
- 8.0A, 500V, $R_{DS(on)}$ = 0.8Ω @V_{GS} = 10 V
- Low gate charge (typical 41 nC)
- Low Crss (typical 35 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220
IRF Series



TO-220F
IRFS Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		IRF840B	IRFS840B	Units
V_{DSS}	Drain-Source Voltage		500		V
I_D	Drain Current - Continuous (T_C = 25°C)		8.0	8.0	A
	- Continuous (T_C = 100°C)		5.1	5.1	A
I_{DM}	Drain Current - Pulsed	(Note 1)	32	32	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	320		mJ
I_{AR}	Avalanche Current	(Note 1)	8.0		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13.4		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	3.5		V/ns
P_D	Power Dissipation (T_C = 25°C)		134	44	W
	- Derate above 25°C		1.08	0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	IRF840B	IRFS840B	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max.	0.93	2.86	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.55	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 400 V, T_C = 125°C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.0 A	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.0 A (Note 4)	--	7.3	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1400	1800	pF
C_{oss}	Output Capacitance		--	145	190	pF
C_{rss}	Reverse Transfer Capacitance		--	35	45	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 8.0 A, R_G = 25 Ω (Note 4, 5)	--	22	55	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	125	260	ns
t_f	Turn-Off Fall Time		--	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 8.0 A, V_{GS} = 10 V (Note 4, 5)	--	41	53	nC
Q_{gs}	Gate-Source Charge		--	6.5	--	nC
Q_{gd}	Gate-Drain Charge		--	17	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8.0 A, dI_F / dt = 100 A/µs (Note 4)	--	390	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.2	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 9.0mH, I_{AS} = 8.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 8.0A, di/dt ≤ 200A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

MC78XX/LM78XX

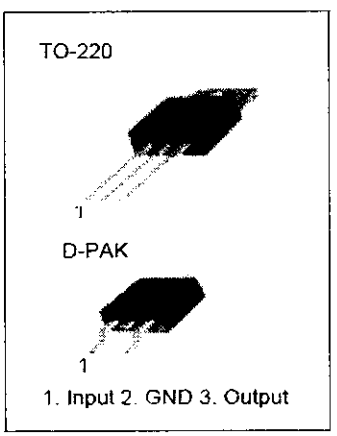
3-terminal 1A positive voltage regulator

Features

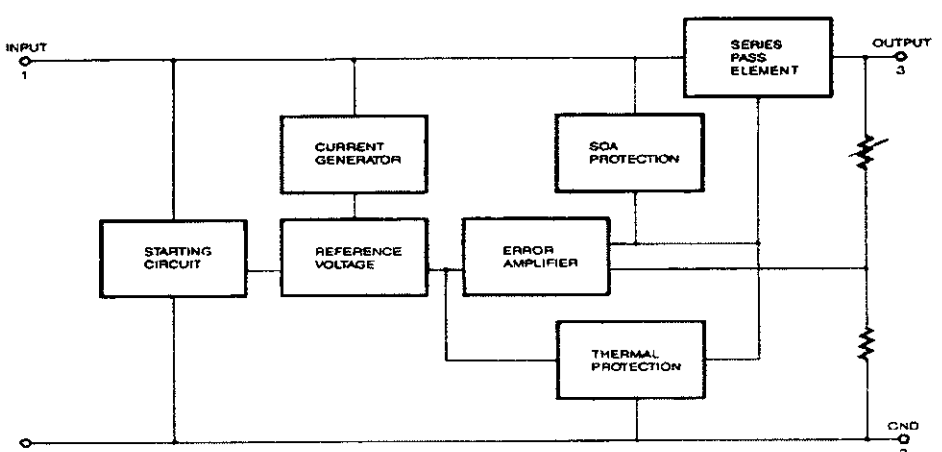
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 11, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating area Protection

Description

The MC78XX/LM78XX series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Digram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C/W
Operating Temperature Range (MC78XXCT/LM78XXCT/MC78XXCDT)	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V V_I = 8V to 20V		4.75	5.0	5.25	
Line Regulation	ΔV_O	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation	ΔV_O	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	μV
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_O	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	R_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

- Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806)

(Refer to test circuit .0°C < T_J < +125°C, I_O = 500mA, V_I = 11V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7806			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		5.75	6.0	6.25	V
		5.0mA ≤ I_O ≤ 1.0A, P_D ≤ 15W V_I = 8.0V to 21V V_I = 9.0V to 21V		5.7	6.0	6.3	
Line Regulation	ΔV_O	T_J =+25 °C	V_I = 8V to 25V	-	5	120	mV
			V_I = 9V to 13V	-	1.5	60	
Load Regulation	ΔV_O	T_J =+25 °C	I_O =5mA to 1.5A	-	9	120	mV
			I_O =250mA to750A	-	3	60	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 8V to 25V		-	-	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C		-	45	-	μV
Ripple Rejection	RR	f = 120Hz V_I = 9V to 19V		59	75	-	dB
Dropout Voltage	V_O	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	R_O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A=+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

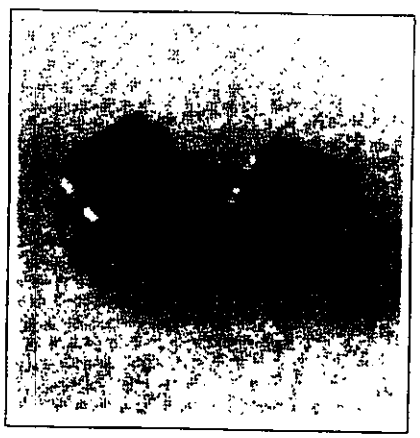
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

SIEMENS

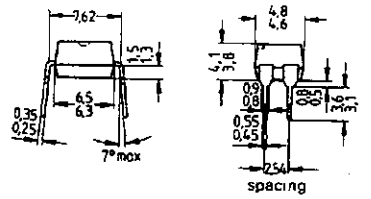
SFH 610
SFH 611
SFH 615

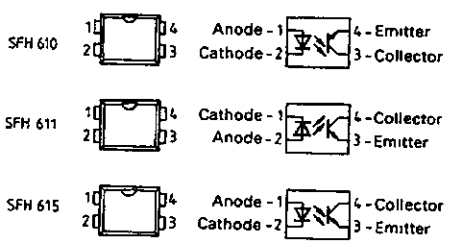
2.8 kV TRIOS*® OPTOCOUPLERS
HIGH RELIABILITY

T-41-83



Package Dimensions mm





FEATURES

- **Isolation Test Voltage: 2800 V**
- **High Current Transfer Ratios**
  at 10 mA: 40-320%
  at 1 mA: 60% typical (>13)
- **Fast Switching Times**
- **Minor CTR Degradation**
- **100% Burn-In**
- **Field-Effect Stable by TRIOS**
- **Temperature Stable**
- **Good CTR Linearity Depending on Forward Current**
- **High Collector-Emitter Voltage V_{CEO}=70 V**
- **Low Saturation Voltage**
- **Low Coupling Capacitance**
- **End-Stackable in 2.54 mm Spacing**
- **High Common-Mode Interference Immunity (Unconnected Base)**
- **UL Approval #52744**
- **VDE Approval 0883**
- **VDE Approval 0884 (Optional with Option 1)**

DESCRIPTION

The optically coupled isolators SFH 610, SFH 611 and SFH 615 feature a high current transfer ratio, low coupling capacitance and high isolation test voltage. They employ a GaAs LED as emitter, which is optically coupled with a silicon planar phototransistor as detector.

The components are incorporated in a plastic plug-in DIP-4 package.

The coupling devices are designed for signal transmission between two electrically separated circuits. The potential difference between the circuits to be coupled is not allowed to exceed the maximum permissible reference voltages.

The couplers are end-stackable in a 2.54 mm spacing and are considered as successor types for the couplers in metal case. The SFH 610, SFH 611 and SFH 615 differ in their arrangement of the terminal pins. Multicouplers can thus easily be implemented and conventional multicouplers can be replaced.

*TRansparent IOn Shield

Maximum Ratings

Emitter (GaAs LED)

Reverse Voltage	6 V
DC Forward Current	60 mA
Surge Forward Current (t≤10 µs)	2.5 A
Total Power Dissipation	100 mW

Detector (Silicon Phototransistor)

Collector-Emitter Voltage	70 V
Collector Current	50 mA
Collector Current (t ≤1 ms)	100 mA
Total Power Dissipation	150 mW

Optocoupler

Storage Temperature Range	-55°C to +150°C
Ambient Temperature Range	-55°C to +100°C
Junction Temperature	100°C
Soldering Temperature (max. 10 s)[1]	260°C
Isolation Test Voltage[2] (between emitter and detector referred to standard climate 23/50 DIN 50014)	2800 VDC
Isolation Resistance (V_{IO}=500 V)	10^{11} Ω

Notes:
1 Dip soldering: minimum clearance from bottom edge of package 1.5 mm. Special soldering conditions apply when through-contacted circuit boards are used. Please request appropriate specification.
2 DC test voltage in accordance with DIN 57883, draft 4/78

Characteristics (T_A=25°C)

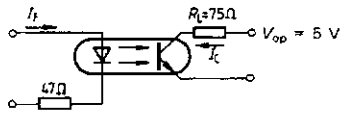
Emitter (GaAs LED)			
Forward Voltage (I_F=60 mA)	V_F	1.25 (≤1.65)	V
Breakdown Voltage (I_R=10 µA)	V_{BR}	30 (≥6)	V
Reverse Current (V_R=6 V)	I_R	0.01 (≤10)	µA
Capacitance (V_R=0 V, f=1 MHz)	C_o	25	pF
Thermal Resistance	R_{thJA}	750	K/W
Detector (Silicon Phototransistor)			
Capacitance (V_{CE}=5 V, f=1 MHz)	C_{CE}	6.8	pF
Thermal Resistance	R_{thJA}	500	K/W
Optocoupler			
Collector-Emitter Saturation Voltage (I_F=10 mA, I_C=2.5 mA)	V_{CEsat}	0.25 (≤0.4)	V
Coupling Capacitance	C_K	0.25	pF

The optocouplers are grouped according to their current transfer ratio I_C/I_F at V_{CE}=5 V, marked by dash numbers

	-1	-2	-3	-4	
I_C/I_F (I_F=10 mA)	40–80	63–125	100–200	160–320	%
I_C/I_F (I_F=1 mA)	30 (>13)	45 (>22)	70 (>34)	90 (>56)	%
Collector-Emitter Leakage Current (V_{CE}=10 V) (I_{CEO})	2 (≤50)	2 (≤50)	5 (≤100)	5 (≤100)	nA

SWITCHING TIMES

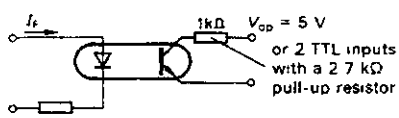
Linear Operation (without saturation)

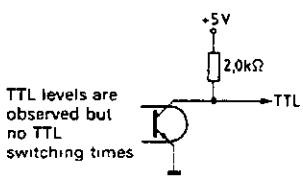


I_F=10 mA, V_{OP}=5 V, T_A=25°C

Load Resistance	R_L	75	Ω
Turn-On Time	t_{ON}	3.0 (≤5.6)	µs
Rise Time	t_R	2.0 (≤4.0)	µs
Turn-Off Time	t_{OFF}	2.3 (≤4.1)	µs
Fall Time	t_F	2.0 (≤3.5)	µs
Cut-Off Frequency	F_{CO}	250	kHz

Switching Operation (with saturation)





Group		-1 (I_F=20 mA)	-2 and -3 (I_F=10 mA)	-4 (I_F=5 mA)	
Turn-On Time	t_{ON}	3.0 (≤5.5)	4.2 (≤8.0)	6.0 (≤10.5)	µs
Rise Time	t_R	2.0 (≤4.0)	3.0 (≤6.0)	4.6 (≤8.0)	µs
Turn-Off Time	t_{OFF}	18 (≤34)	23 (≤39)	25 (≤43)	µs
Fall Time	t_F	11 (≤20)	14 (≤24)	15 (≤26)	µs
	V_{CEsat}	0.25 (≤0.4)			V

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							µA µA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Typical Characteristics

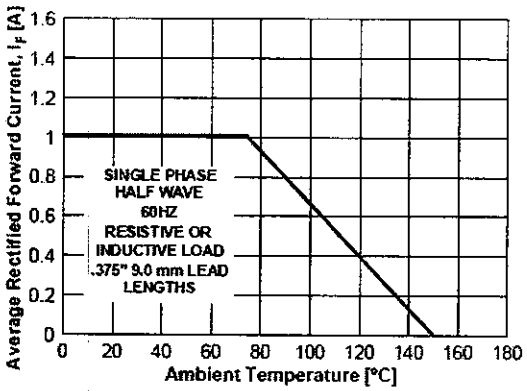


Figure 1. Forward Current Derating Curve

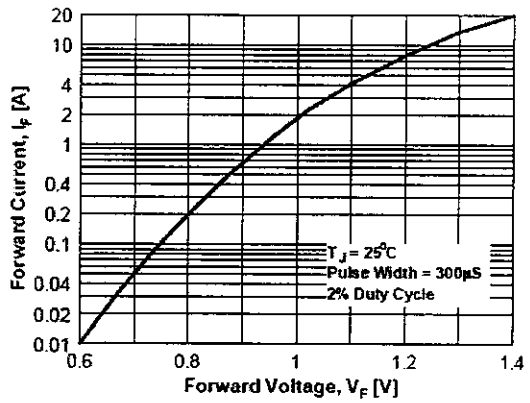


Figure 2. Forward Voltage Characteristics

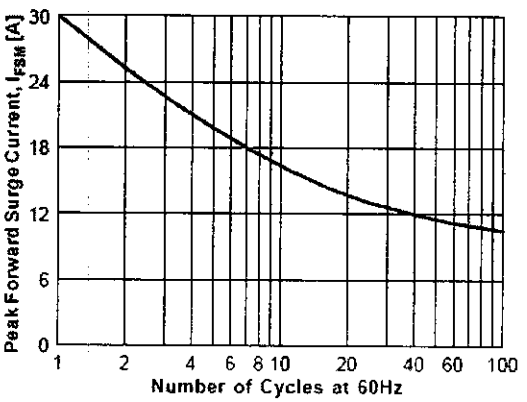


Figure 3. Non-Repetitive Surge Current

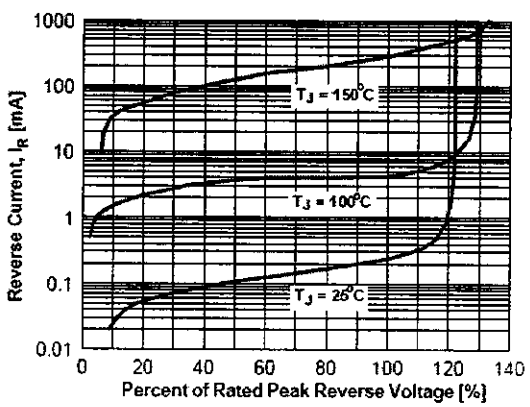
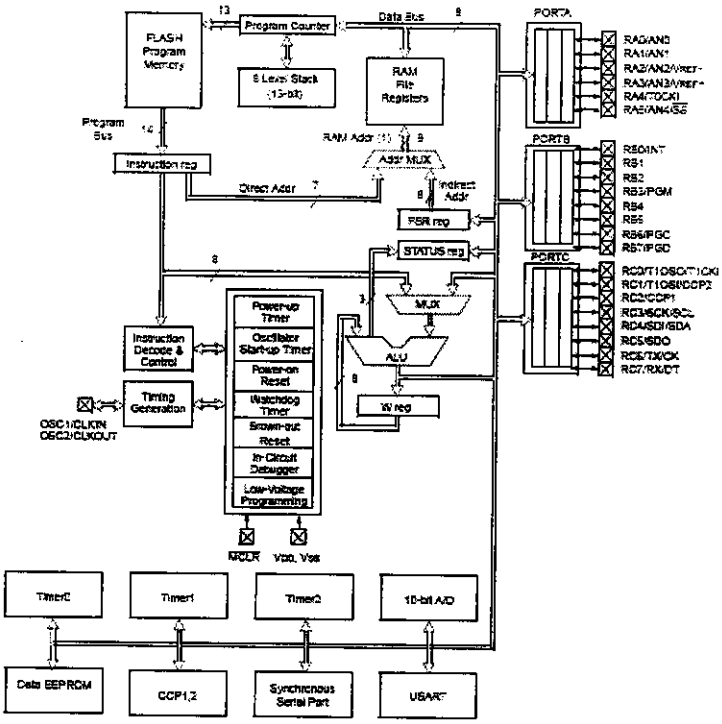


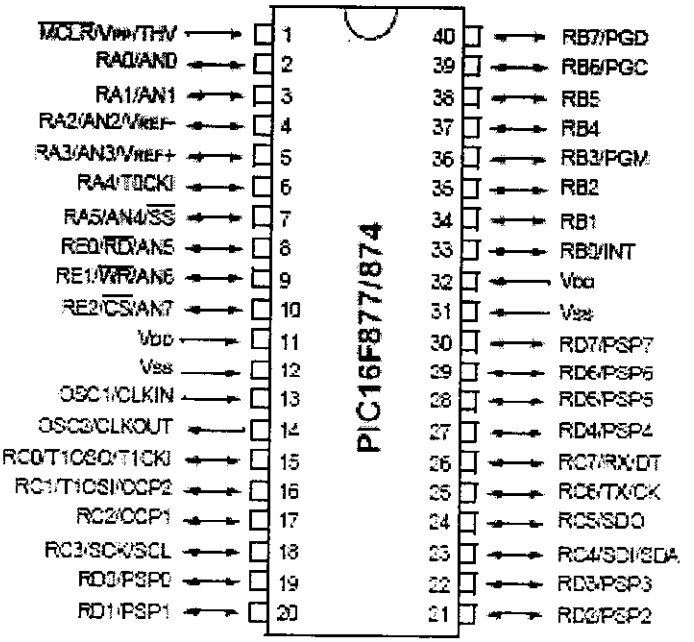
Figure 4. Reverse Current vs Reverse Voltage

ARCHITECTURE OF PIC 16F877A

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F873	4K	192 Bytes	128 Bytes
PIC16F876	8K	368 Bytes	256 Bytes



Pin Configuration of PIC16F877A



TIMER 0 CONTROL REGISTER:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7: **RBPU**

bit 6: **INTEDG**

bit 5: **T0CS**: TMR0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

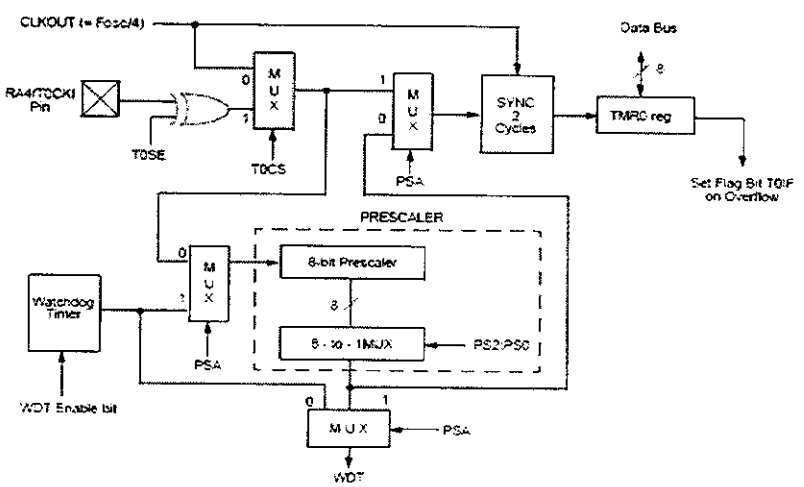
bit 3: **PSA**: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

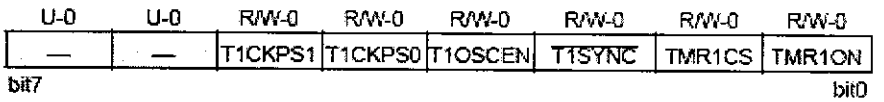
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2 PS1 PS0**: Prescaler Rate Select bits

TIMER 0 BLOCK DIAGRAM:



TIMER 1 CONTROL REGISTER:



bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3: **T1OSCEN**: Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled

0 = Oscillator is shut off (The oscillator inverter is turned off to eliminate power drain)

bit 2: **T1SYNC**: Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1

1 = Do not synchronize external clock input

0 = Synchronize external clock input

TMR1CS = 0

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS**: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)

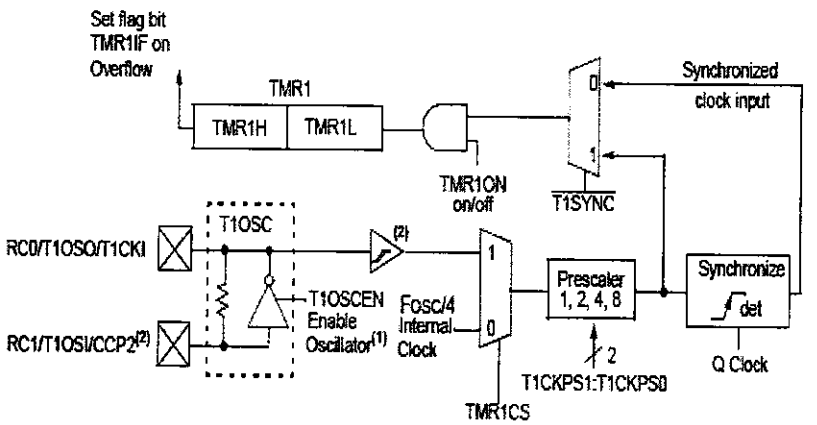
0 = Internal clock (FOSC/4)

bit 0: **TMR1ON**: Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

TIMER 1 BLOCK DIAGRAM:



TIMER 2 CONTROL REGISTER:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits

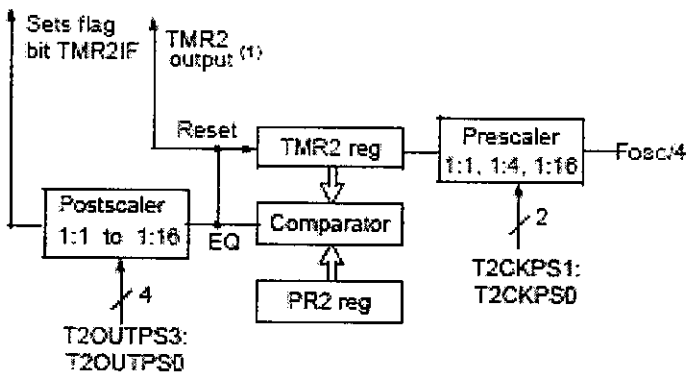
0000 = 1:1 Postscale

0001 = 1:2 Postscale

0010 = 1:3 Postscale

1111 = 1:16 Postscale

TIMER2 BLOCK DIAGRAM:



CCP1CON REGISTER/CCP2CON REGISTER:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCPxX :CCPxY**: PWM Least Significant bits

Capture Mode: Unused

Compare Mode: Unused PWM Mode: These bits are the two LSB s of the PWM duty cycle. The eight MSB s are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets CCPx module)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (CCPxIF bit is set)

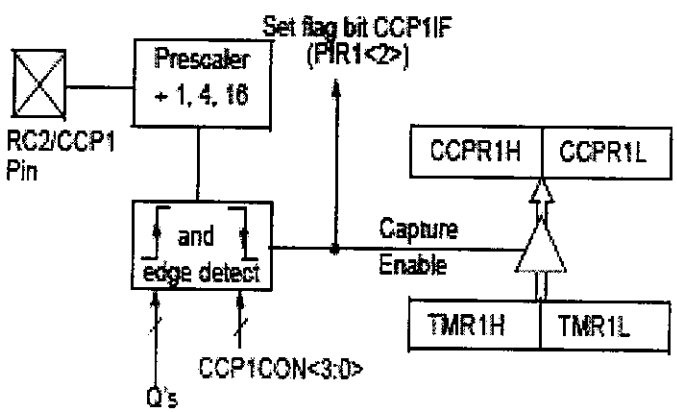
1001 = Compare mode, clear output on match (CCPxIF bit is set)

1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)

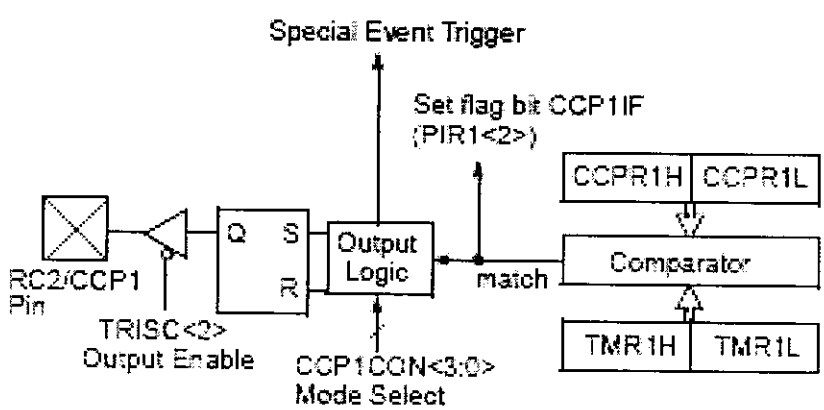
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)

11xx = PWM mode

CAPTURE MODE OPERATION BLOCK DIAGRAM:



COMPARE MODE OPERATION BLOCK DIAGRAM:



PIC PROGRAMMING:

```
#include<pic.h>
__CONFIG(0X20E4);
__CONFIG(0X3FFF);

#define S1 RB0
#define S2 RB1
#define S3 RB2
#define S4 RB3

#define SW RB5

unsigned int REFF1,INPUT1,REFF2,INPUT2;
unsigned char count;

delay(void);
delay1(void);

void main()
{
      TRISC=0;
      PORTC=0;

      TRISB=0;
      PORTB=0;

      TRISA=0XFF;

      RC2=1;
      ANSEL=0X0F;
      ANSELH=0;
      ADCON1=0X80;

      PR2=99;
      T2CON=0X04;

      CCP1CON=0X0C;
      CCPR1L=75;

      CCP2CON=0X0C;
      CCPR2L=75;


      T1CON=0X01;
      TMR1L=0XF0;
      TMR1H=0XD8;


      GIE=PEIE=TMR1IE=1;
```

```
        while(1)
        {
/****************** ADC SCAN *****************/
            ADCON0=0X81;
            delay();
            GODONE=1;
            while(GODONE);
            REFF1=(ADRESH*256)+ADRESL;

            ADCON0=0X85;
            delay();
            GODONE=1;
            while(GODONE);
            INPUT1=(ADRESH*256)+ADRESL;

            ADCON0=0X89;
            delay();
            GODONE=1;
            while(GODONE);
            REFF2=(ADRESH*256)+ADRESL;

            ADCON0=0X8D;
            delay();
            GODONE=1;
            while(GODONE);
            INPUT2=(ADRESH*256)+ADRESL;
/****************** ADC SCAN END ********************/


/******************   PWM LIMIT   *********************/
            if(INPUT1>410 && INPUT2>410)
            {
                  if(CCPR1L<45)
                        CCPR1L=45;
                  if(CCPR1L>85)
                        CCPR1L=85;

                  if(CCPR2L<45)
                        CCPR2L=45;
                  if(CCPR2L>85)
                        CCPR2L=85;
            }
/************** OUTPUT REGULATION*****************/

            if(INPUT1>410 && INPUT2>410)
            {
                  delay1();
                  if(REFF1>600)
                        CCPR1L++;
```

```
                delay();
                if(REFF1<605)
                      CCPR1L--;
                delay1();

                delay1();
                if(REFF2>600)
                      CCPR2L++;
                delay();
                if(REFF2<605)
                      CCPR2L--;
                delay1();
          }
/*************************************************/


          if(INPUT1>700 && INPUT2>700)
                SW=1;


          if(INPUT1<600)
          {
                SW=0;
                if(INPUT1<400)
                {
                      SW=0;
                      CCPR1L=100;
                }
          }

          if(INPUT2<600)
          {
                SW=0;
                if(INPUT2<400)
                {
                      SW=0;
                      CCPR2L=100;
                }
          }



     }

}
void interrupt isr()
{
     if(TMR1IF==1)
     {
          TMR1IF=0;
```

```
                TMR1L=0XF0;
                TMR1H=0XD8;

                count++;
                if(count==1)
                {
                      PORTB=0;
                      S1=1;
                      S2=1;
                }
                if(count==2)
                {
                      count=0;
                      PORTB=0;
                      S3=1;
                      S4=1;
                }
        }

}

delay()

{
      unsigned int i;
      for(i=0;i<100;i++);
}
delay1()
{
      unsigned int j;
      for(j=0;j<10000;j++);
}
```