MEMS BASED INERTIAL NAVIGATION SYSTEM

by

RAAJENDRAKUMAR.M	**Reg No: 0710107072**
RAJESH.R	**Reg No: 0710107073**
RAJTHILAK.D	**Reg No: 0710107076**
RAMPRASATH.K	**Reg No: 0710107079**

of

KUMARAGURU COLLEGE OF TECHNOLOGY,

COIMBATORE - 641049.

(An Autonomous Institution affiliated to Anna University of Technology, Coimbatore)

A PROJECT REPORT

Submitted to the

FACULTY OF ELECTRONICS AND COMMUNICATION ENGINEERING

In partial fulfillment of the requirements

for the award of the degree

Of

BACHELOR OF ENGINEERING

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

APRIL 2011

BONAFIDE CERTIFICATE

Certified that this project report entitled **"MEMS Based Inertial Navigation System"** is the bonafide work of **Mr.Raajendrakumar.M**[Reg. no. 0710107072], **Mr.Rajesh.R** [Reg. no. 0710107073], **Mr.Rajthilak.D** [Reg. no. 0710107076], and **Mr.Ramprasath.K** [Reg. no. 0710107079] who carried out the project work under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

D. Mo

Project Guide

Mrs.D.Mohana Geetha

Head of the Department

Dr. Rajeswari Mariappan

The candidate with university Register no. 0710107072, 0710107073, 0710107076, 0710107079 is examined by us in the project viva-voce examination held on 19/4/11

Internal Examiner 19/4/11

External Examiner

ACKNOWLEDGEMENT

First I would like to express my praise and gratitude to the Lord, who has showered his grace and blessing enabling me to complete this project in an excellent manner.

I express my sincere thanks to our beloved Director **Dr.J.Shanmugam, ME, Ph.D.,** Kumaraguru College of Technology, for his kind support and for providing necessary facilities to carry out the work.

I express my sincere thanks to our beloved Principal **Dr.S.Ramachandran, M.Tech, Ph.D.,** Kumaraguru College of Technology, who encouraged me in each and every steps of the project work.

I would like to express my deep sense of gratitude to our HOD, the ever active **Dr.Rajeswari Mariappan, M.E, Ph.D.,** Department of Electronics and Communication Engineering, for her valuable suggestions and encouragement which paved way for the successful completion of the project work.

In particular, I wish to thank with everlasting gratitude to the project coordinator **Mrs.K.Kavitha,M.E.,** Assistant Professor-SRG , Department of Electronics and Communication Engineering, for her expert counseling and guidance to make this project to a great deal of success.

I am greatly privileged to express my heartfelt thanks to my project guide **Mrs.D.Mohana Geetha,M.E,(Ph.D).,** Associate Professor, Department of Electronics and Communication Engineering, throughout the course of this project work and I wish to convey my deep sense of gratitude to all the teaching and non-teaching staffs of ECE Department for their help and cooperation.

Finally, I thank my parents and my family members for giving me the moral support and abundant blessings in all of my activities and my dear friends who helped me to endure my difficult times with their unfailing support and warm wishes.

ABSTRACT

Inertial navigation system is equipment designed to provide services for a user within a building or GPS denied environments such as tunnels and caves. This system is used to identify a person's position within a building or any indoor known area. The person can be easily found by an outside person in case of an emergency. This is particularly useful in defense applications where members of a battle squad need to know each other's position all the time and in all the places during a critical operation. Our project aims to design an inertial navigation system equipped with Wireless Personal Area Network (WPAN) technology which is able to monitor and track location of a person by showing the path of the person on the graphics LCD display if he moves inside the indoor location.

The system is designed using inertial sensors, such as Micro Electrical Mechanical System (MEMS) accelerometers for linear movement and MEMS gyroscope for angular movement, to estimate relative displacement, starting with the known initial user location. The sensored data with exact displacement values are send to other motes via IEEE 802.15.4 data packet.WPAN is the wireless network technology using IEEE 802.15.4 radio modules that enable long distance, low traffic, and low power wireless data transmissions, suitable in GPS denied environments like a building. The microcontroller chosen is based on ARM Cortex M3 architecture.

ARM Cortex M3 is the next generation high performance 32-bit ARM core developed specifically for microcontroller applications with thumb-2 technology based on ARM v7-M architecture. The device is designed to be operated on battery and consumes very low power.

TABLE OF CONTENT

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Future mobile users will expect services to be more specialized to their personal needs by knowing their current location in space at a given time. Although GPS navigation systems provide a solution for this they tend to fail in indoor scenarios. So, to provide services for a user within a building or GPS denied environments such as tunnels and caves, special equipment is needed. Several applications are possible once a person's position within a building or any indoor area is known.

1.1 OBJECTIVE OF THE PROJECT

The goal of this project is to design an equipment to track the location of a person in GPS denied environments such as tunnels and caves and also it can be useful in defense applications where members of a battle squad need to know each other's position all the time and in all the places during a critical operation. The person could be easily found by an outside person in case of an emergency. The device is designed to be operated on battery and consumes very low power.

1.2 OVERVIEW OF THE PROJECT

The project consists of two sections, Tracker and Receiver sections. The circuit diagram of the project is as follows,

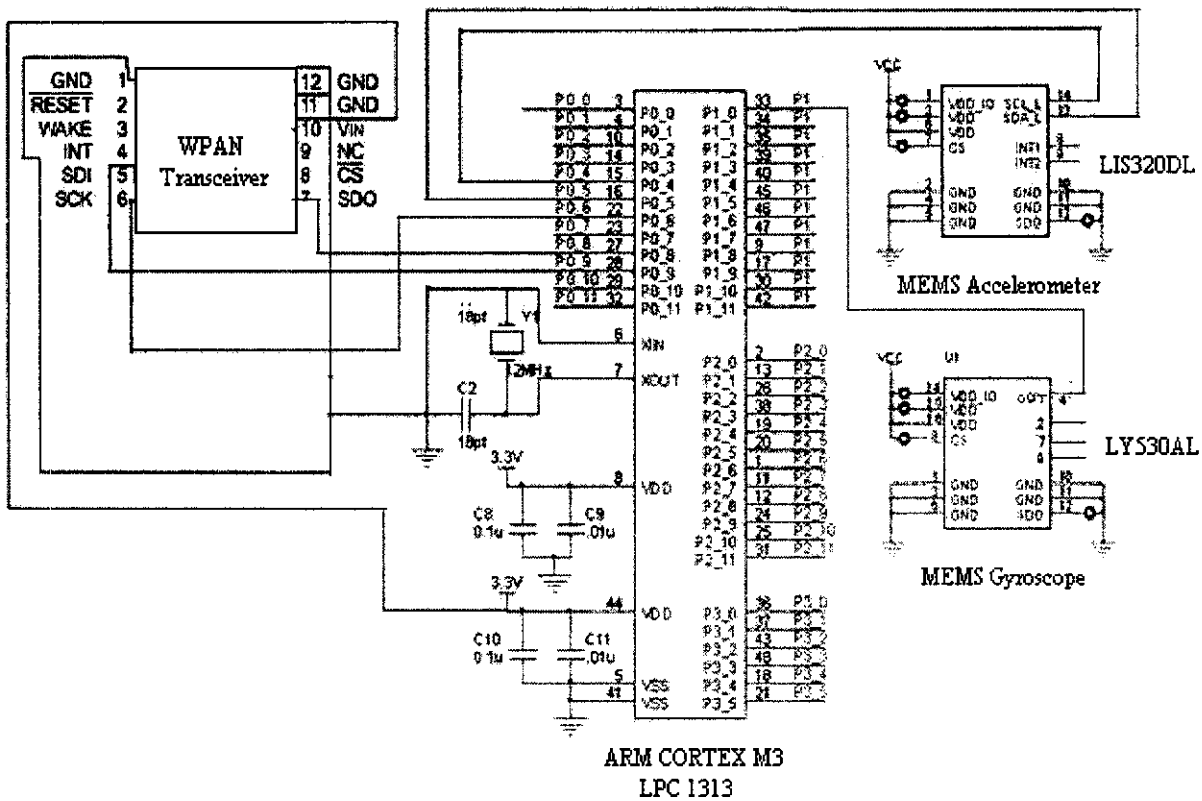

FIGURE 1.1 TRACKER SECTION

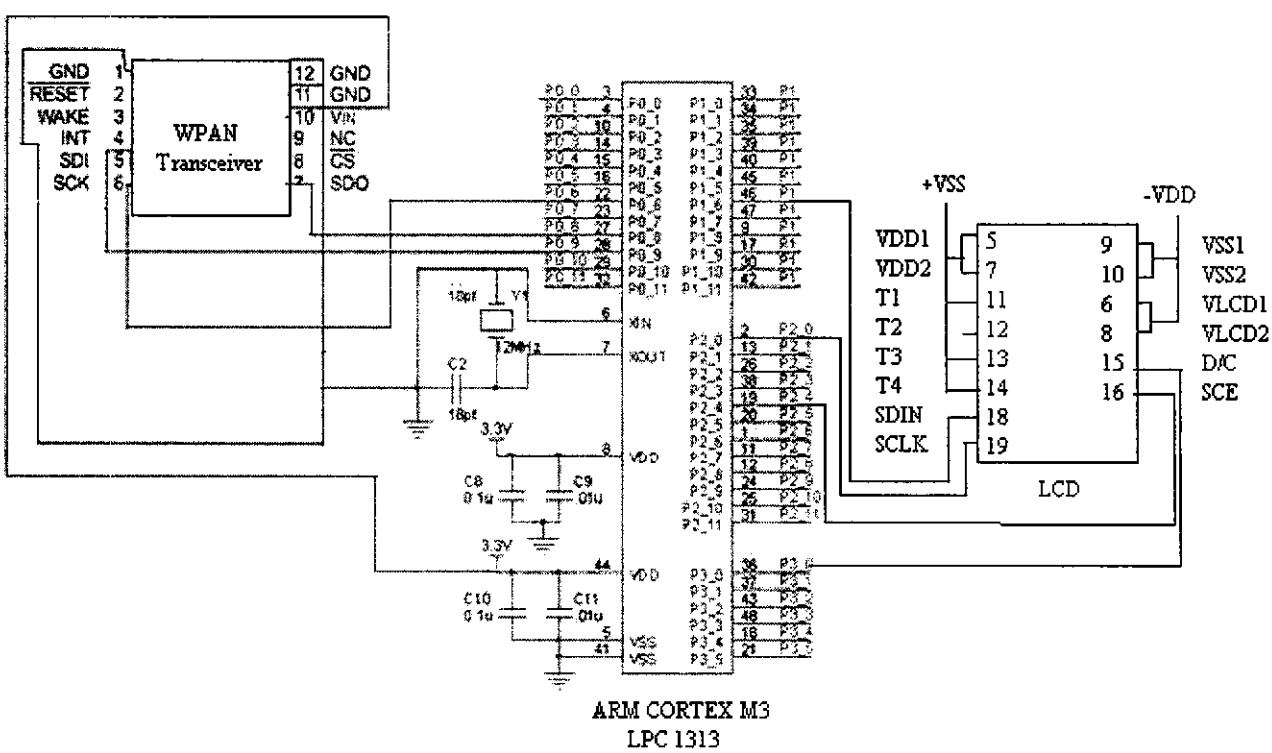

FIGURE 1.2 RECEIVER SECTION

1.2.1 DESCRIPTION OF THE BLOCKS

The description of the blocks present in the project is as follows,

ARM CORTEX M3-LPC1313

The LPC1313 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration. The LPC1313 operate at CPU frequencies of up to 72 MHz the ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal pre -fetch unit that supports speculative branching. The peripheral complement of the LPC1313 includes up to 32 kB of flash memory, up to 8 kB of data memory

WIRELESS PROTOCOL

The Microchip MiWi P2P Wireless Protocol is a variation of IEEE 802.15.4, using Microchip's MRF24J40MA 2.4 GHz transceiver and any Microchip 8, 16 or 32-bit microcontroller with a Inter Integrated Circuit (I^2C). The protocol provides reliable direct wireless communication via an easy-to-use programming interface. It has a rich feature set that can be compiled in and out of the stack to meet a wide range of customer needs – while minimizing the stack footprint.

MICRO ELECTRO MECHANICAL SYSTEMS ACCELEROMETER

An accelerometer is a device for measuring acceleration and gravity induced reaction forces. Single- and multi-axis models are available to detect magnitude and direction of the acceleration as a vector quantity. Accelerometers can be used to sense inclination, vibration, and shock. They are increasingly present in portable electronic devices. Mechanically the accelerometer behaves as a mass-damper-spring system. The LIS302DL is an ultra compact low-power three axes linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I^2C/SPI serial interface.

MICRO ELECTRO MECHANICAL SYSTEMS GYROSCOPE

Micro Electrical Mechanical System (MEMS) gyroscopes are angular sensing devices used to find out the angular movements.MEMS sensor used is Y530AH.Angle is measured with respect to the casing. The mass is rotated with an initial θ. When the gyroscopes rotate the mass continues to rotate in the same direction. Angular rate is measured by adding a driving frequency. No change in performance due to temperature. Advantages are Lower voltage noise Stronger signal to noise ratio Better communication with external devices Higher sensitivity.

GRAPHICS LCD

The PCD8544 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCD8544 interfaces to microcontrollers through a serial bus interface. The PCD8544 is manufactured in n-well CMOS technology.

1.2 ORGANIZATION OF THE REPORT

- **Chapter 1** discusses about the Introduction, Objective of the project, Overview of the project and the organization of the report.
- **Chapter 2** discusses about the ARM Cortex M3 processor and its operation.
- **Chapter 3** deals about the Communication protocols, their features and their characteristics.
- **Chapter 4** explains about the Microchip MiWi P2P Wireless Protocol.
- **Chapter 5** discusses about the functions of Micro Electro Mechanical Systems.
- **Chapter 6** explains about the Graphical Liquid Crystal Display.
- **Chapter 7** discusses about Algorithm of the project.
- **Chapter 8** discusses about Circuit diagram and Result of the project.
- **Chapter 9** shows the Conclusion of the project.

CHAPTER 2
ARM CORTEX M3

2.1 INTRODUCTION

The ARM Cortex M3 processor is the industry-leading 32-bit processor for highly deterministic real-time applications and has been specifically developed to enable partners to develop high-performance low-cost platforms for a broad range of devices including microcontrollers, automotive body systems, industrial control systems and wireless networking and sensors.

The processor delivers outstanding computational performance and exceptional system response to events while meeting the challenges of low dynamic and static power constraints. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology through to extremely cost sensitive devices requiring minimal area.

2.2 IMPORTANCE OF ARM CORTEX –M3

➢ Delivering higher performance and richer features

Introduced in 2004 and recently updated with new technologies and configurability, the Cortex-M3 is the mainstream ARM processor developed specifically with microcontroller applications in mind.

➢ Performance and Energy Efficiency

With high performance and low dynamic power consumption the Cortex-M3 processor delivers leading power efficiency 12.5 DMIPS/mW based on 90nmG. Coupled with integrated sleep modes and optional state retention capabilities the Cortex-M3 processor ensures there is no compromise for applications requiring low power and excellent performance.

➢ Full featured

The processor executes Thumb-2 instruction set for optimal performance and code size, including hardware division, single cycle multiply, and bit-field manipulation. The Cortex-M3 NVIC is highly configurable at design time to deliver up to 240 system interrupts with individual priorities, dynamic reprioritization and integrated system clock.

- **Rich connectivity**

The combination of features and performance enables Cortex-M3 based devices to efficiently handle with multiple I/O channels and protocol standards such as ZIGBEE, CAN, ETHERNET and USB OTG.

2.3 ARCHITECTURE OF LPC1313

The LPC1313 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration. The LPC1313 operate at CPU frequencies of up to 72 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal pre -fetch unit that supports speculative branching. The peripheral complement of the LPC1313 includes up to 32 kB of flash memory, up to 8 kB of data memory, USB Device (LPC1342/43 only), one Fast-mode Plus I2C-bus interface, one UART, four general purpose timers, and up to 42 general purpose I/O pins.

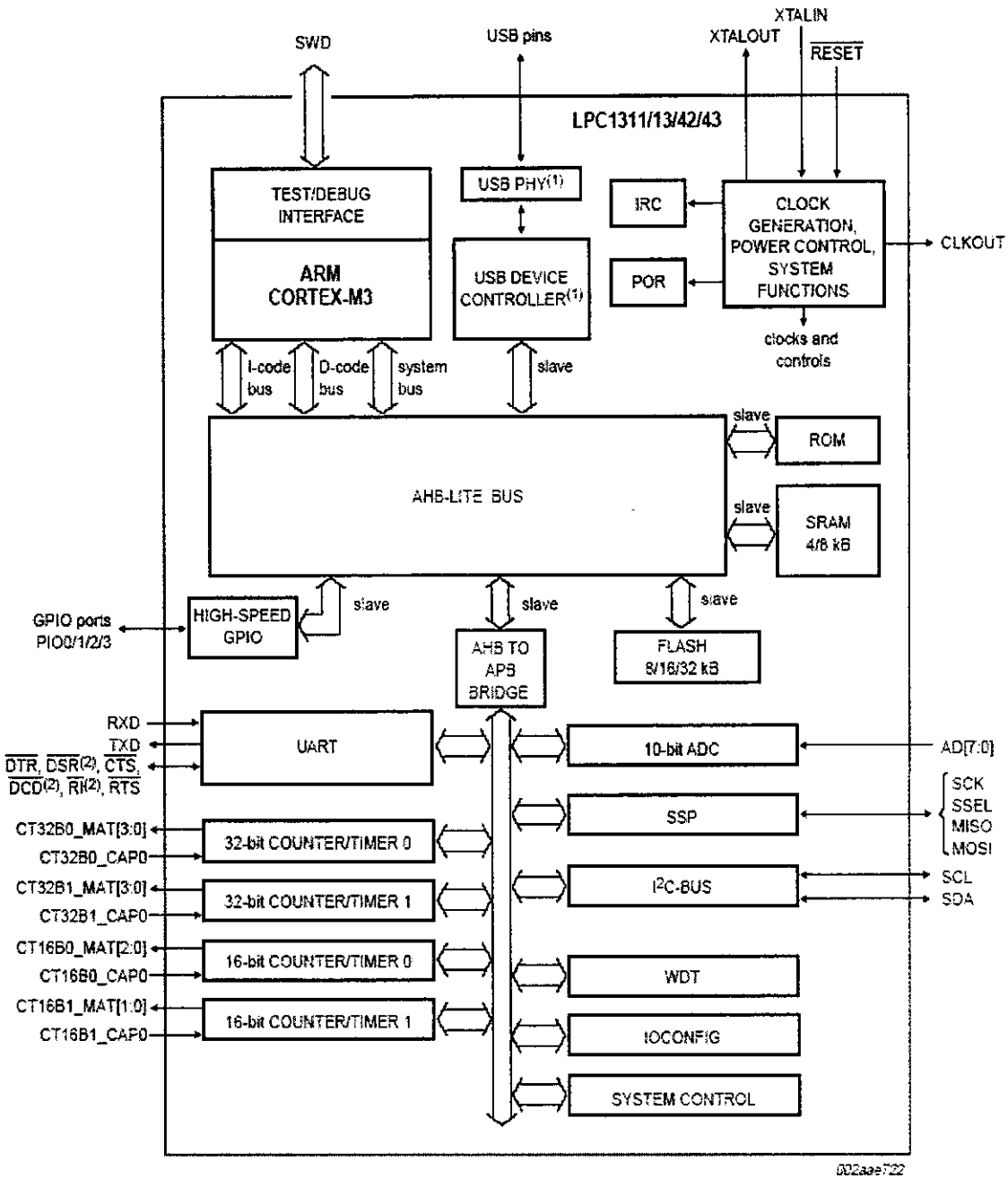

FIGURE: 2.1 ARCHITECTURE OF LPC 1313

2.3.1 FEATURES

- ARM Cortex-M3 processor, running at frequencies of up to 72 MHz.
- ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
- 32 kB (LPC1343/13)/16 kB (LPC1342)/8 kB (LPC1311) on-chip flash programming memory.
- 8 kB (LPC1343/13)/4 kB (LPC1342/11) SRAM.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip boot-loader software.
- Selectable boot-up: UART or USB (USB on LPC134x only).
- On-chip boot-loader drivers for MSC and HID (LPC134x only).
- Serial interfaces:
  - USB 2.0 full-speed device controller with on-chip PHY for device (LPC1342/43 only).
  - UART with fractional baud rate generation, modem, internal FIFO, and RS-485/EIA-485 support.
  - SSP controller with FIFO and multi-protocol capabilities.
- I^2C-bus interface supporting full I2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Other peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - Four general purpose timers/counters with a total of four capture inputs and 13 match outputs.
  - Programmable Watchdog Timer (WDT).
  - System tick timer.
- Serial Wire Debug and Serial Wire Trace port.
- High-current output driver (20 mA) on one pin.
- High-current sink drivers (20 mA) on two I2C-bus pins in Fast-mode Plus
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
- Three reduced power modes:
- Sleep, Deep-sleep, and Deep power-down.
- Single 3.3 V power supply (2.0 V to 3.6 V).
- 10-bit ADC with input multiplexing among 8 pins.
- GPIO pins can be used as edge and level sensitive interrupt sources.

- ❖ Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, or the watchdog clock.
- ❖ Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 40 of the functional pins.
- ❖ Brownout detect with four separate thresholds for interrupt and one threshold for forced reset.
- ❖ Power-On Reset (POR).
- ❖ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- ❖ 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.

2.3.3 PIN DIAGRAM

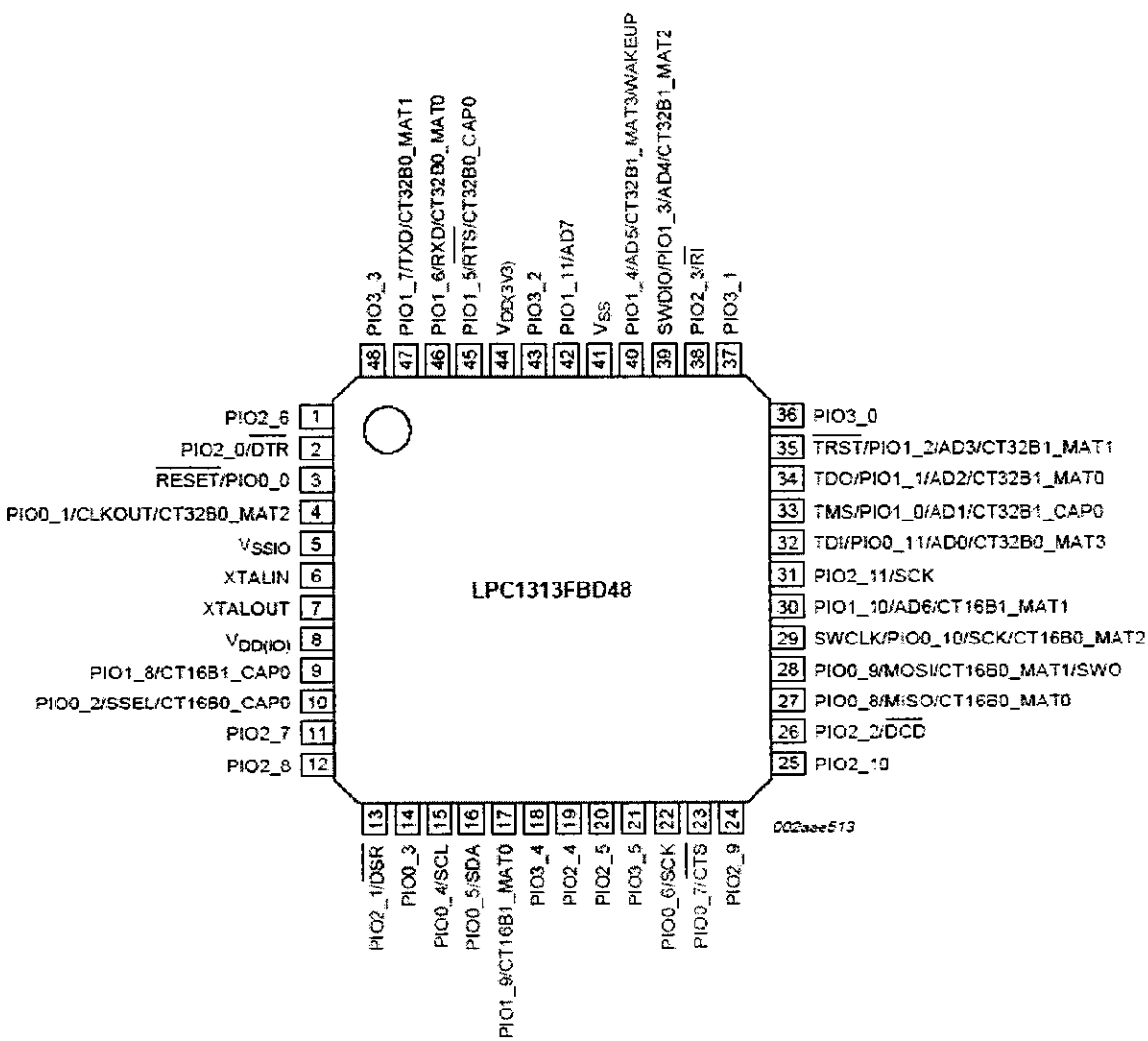

FIGURE: 2.2 PIN DIAGRAM OF LPC1313

The pin description of LPC1313 is as follows,

- Pin 8: 3.3V input voltage.
- Pin 44: 3.3V supply voltage to the internal regulator and ADC.it is used as ADC reference voltage.
- Pin 5:Ground
- Pin 41: Ground.
- Pin 33: General purpose digital input/output pin.
  A/D converter pin, input for timer.
- Pin 15: General purpose digital input/output pin.
  Serial clock for interface using software control.
  I^2Cbus clock input and output.
- Pin 16: General purpose digital input/output pin.
  Clear to send signal from interface.
- Pin 6: Input to the oscillator circuit and clock generator circuit. Input voltage is 1.8V
- Pin 7: Output from oscillator amplifier.
- Pin 27: General purpose digital input/output pin.
  A/D converter pin.
  Master in slave out for SPI.
- Pin 28: General purpose digital input/output pin.
  Master out slave in for SPI.
- Pin 29: General purpose digital input/output pin.
  Serial wire clock for interface.

CHAPTER 3
COMMUNICATION PROTOCOL

3.1 I²C PROTOCOL INTRODUCTION

I²C is a multi-master serial computer bus invented by Philips that is used to attach low-speed peripherals to a motherboard, embedded system, or cell phone. The name stands for **Inter-Integrated Circuit** and is pronounced I-squared-C

I²C uses only two bidirectional open-drain lines, Serial Data (SDA) and Serial Clock (SCL), pulled up with resistors. The I²C reference design has a 7-bit address space with 16 reserved addresses, so a maximum of 112 nodes can communicate on the same bus. The maximum number of nodes is obviously limited by the address space, and also by the total bus capacitance of 400 pF.

To maximize hardware efficiency and circuit simplicity, Philips developed a simple bi-directional 2-wire bus for efficient inter-IC control. This bus is called the Inter IC or I²C-bus. All I2C-bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I²C-bus. This design concept solves the many interfacing problems encountered when designing digital control circuits. Here are some of the features of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode.

- On-chip filtering rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

For 8-bit oriented digital control applications, such as those requiring microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders
- The cost of connecting the various devices within the system must be minimized
- A system that performs a control function doesn't require high-speed data transfer
- Overall efficiency depends on the devices chosen and the nature of the interconnecting bus structure.

To produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer IC connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must b e defined. All these criteria are involved in the specification of the I2C-bus.

3.1.1 DESIGNER BENEFITS

I^2C-bus compatible ICs allow a system design to rapidly progress directly from a functional block diagram to a prototype. Moreover, since they 'clip' directly onto the I^2C-bus without any additional external interfacing, they allow a prototype system to be

modified or upgraded simply by 'clipping' or 'unclipping' ICs to or from the bus. Here are some of the features of I^2C-bus compatible ICs which are particularly attractive to designers:

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic.
- No need to design bus interfaces because the I^2C-bus interface is already integrated on-chip.
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I^2C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules.

3.1.2 I^2C BUS CONCEPT

The I^2C-bus supports any IC fabrication process (NMOS, CMOS, bipolar). Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address (whether it's a microcontroller, LCD driver, memory or keyboard interface) and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers.

A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

TABLE 3.1 DEFINITION OF I^2C BUS TERMINOLOGY

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus.
Receiver	The device which receives data to the bus.
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master.
Multi-Master	More than one master can attempt to control the bus at the same time without corrupting the message.
Arbitration	If more than one bus simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted.
Synchronisation	Procedure to synchronize the clock signals of two or more devices.

The I^2C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. The possibility of connecting more than one microcontroller to the I^2C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I^2C interfaces to the I^2C-bus. If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line.

Generation of clock signals on the I^2C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line or by another master when arbitration occurs.

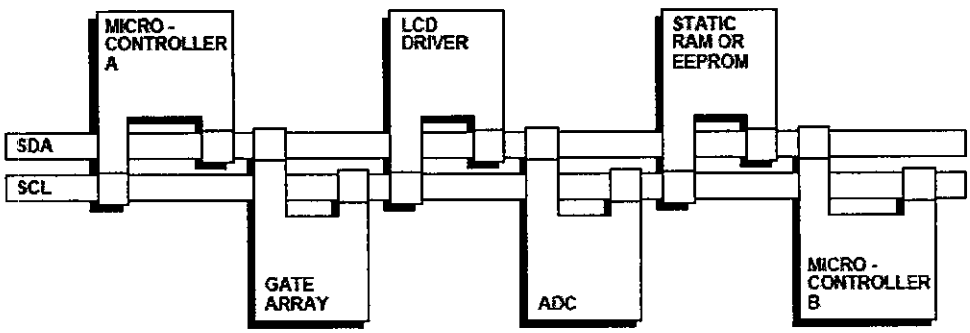

FIGURE: 3.1 I^2C BUS CONFIGURATIONS

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current-source or pull-up resistor (see Fig.3). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I^2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF.

3.2 SERIAL PERIPHERAL INTERFACE

Serial Peripheral Interface is a simple interface which enables to communicate microcontroller and peripheral chips or intercommunicate between two or more microcontrollers. Serial Peripheral Interface bus sometimes called four wire interfaces may be used to interface such chips or devices like: LCD, sensors, memories, ADC, RTC. The range of usage is huge.

SPI Bus uses synchronous protocol, where transmitting and receiving is guided by clock signal generated by master microcontroller. SPI interface allows connecting several

SPI devices while master selects each of them with CS (Chip Select) signal – (Underline means that active is LOW).

SPI bus consists of four signal wires:

- ❖ Master Out Slave In (MOSI),
- ❖ Master In Slave Out (MISO),
- ❖ Serial Clock (SCLK or SCK)
- ❖ Chip Select (CS) for the peripheral.

- o Some microcontrollers have a dedicated chip select for SPI interfacing called Slave Select (SS).
- o MOSI signal is generated by master – recipient is Slave. MOSI may also be labelled as SI or SDI.
- o MISO signals are generated by slave. In some chips you might find labels SO or SDO.
- o SCLK or SCK are generated by master to synchronize data transfers.
- o CS (SS) signal is also generated by master to select slave chip or device.

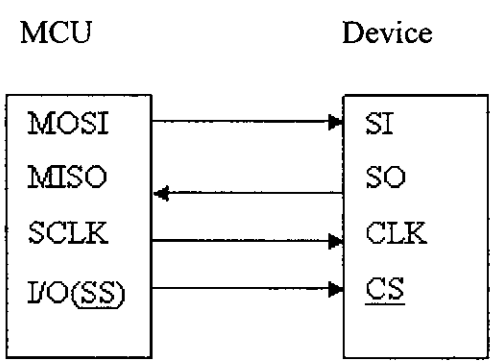

FIGURE: 3.2 FLOW OF DATA TRANSFER

Data transfer is organized by using Shift register in both: master and slave. While master shifts register value out through MOSI line then slave shifts data in to its shift register. If there is full duplex used, then send and receive is performed at the same time:

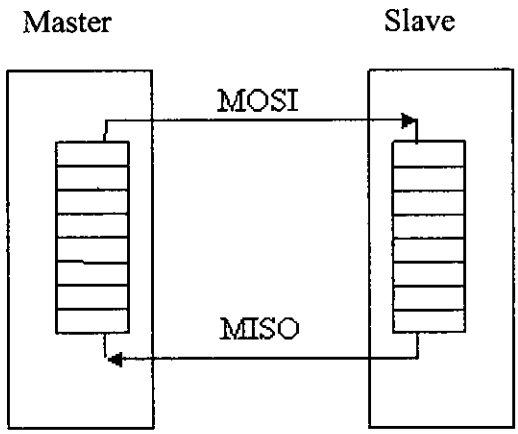

FIGURE: 3.3 FULL DUPLEX IN SPI

There also is multiple byte stream modes available with SPI bus interface. In this mode master can shift bytes continuously. Using this type of transfer slave select (SS) must remain low until all stream process continues. For example you can write to memory by sending address bytes and then data in the same stream operation. In this way kilobytes or more can be sent using multiple byte transfer mode

3.2.1 MODE OF OPERATION

Some chips have ability when you can connect multiple SPI devices in series and data can be transferred to all devices though other. For instance if you connect three devices to microcontroller in series MCU-A-B-C, then MCU will have to send three bytes of information. The first byte goes to C device, second to B and third byte to A:

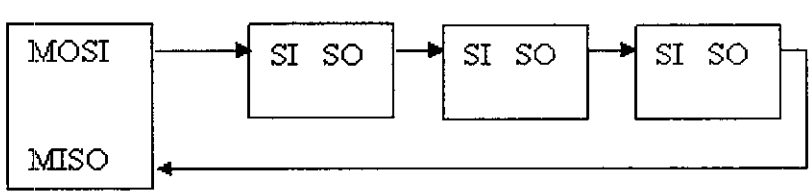

FIGURE: 3.4 DAISY CHAIN MODES

Daisy-chain won't work with devices which support or require multiple bytes operation (memory chips).For instance AD8403 - 4-Channel Digital Potentiometer can be connected in daisy-chain circuit:

Depending on Clock (SKC) polarity, there may be four operation modes of SPI:

- Low clock polarity – when clock is low in idle and toggles in high;
- High clock polarity – when clock is high in idle and toggles in low stage
- Clock phase zero – MOSI and MISO outputs are valid on rising edge of clock signal (from low to high);
- Clock phase one – MOSI and MISO outputs are valid on falling edge of SCK signal (high to low)

CHAPTER 4
MIWI P2P WIRELESS PROTOCOL

4.1 INTRODUCTION

The Microchip MiWi P2P Wireless Protocol is a variation of IEEE 802.15.4, using Microchip's MRF24J40MA 2.4 GHz transceiver and any Microchip 8, 16 or 32-bit microcontroller with a Inter Integrated Circuit (I^2C). The protocol provides reliable direct wireless communication via an easy-to-use programming interface. It has a rich feature set that can be compiled in and out of the stack to meet a wide range of customer needs – while minimizing the stack footprint.

4.2 PROTOCOL OVERVIEW

The MiWi P2P protocol modifies the IEEE 802.15.4 specification's Media Access Control (MAC) layer by adding commands that simplify the handshaking process. It simplifies link disconnection and channel hopping by providing supplementary MAC commands. However, application-specific decisions, such as when to perform an energy detect scan or when to jump channels, are not defined in the protocol. Those issues are left to the application developer.

4.3 PROTOCOL FEATURES

- Provides 16 channels in the 2.4 GHz spectrum (using an MRF24J40 transceiver)
- Operates on Microchip PIC18, PIC24, dsPIC33 and PIC32 platforms
- Supports Microchip C18, C30 and C32 compilers, Enables frequency agility (channel hopping)
- Supports a sleeping device at the end of the communication
- Enables Energy Detect (ED) scanning to operate on the least-noisy channel
- Provides active scan for detecting existing connections
- Supports all of the security modes defined in IEEE 802.15.4.

4.4 PROTOCOL CONSIDERATIONS

The MiWi P2P protocol is a variation of IEEE 802.15.4 and supports both peer-to-peer and star topologies. It has no routing mechanism, so the wireless communication coverage is defined by the radio range.

Guaranteed Time Slot (GTS) and beacon networks are not supported, so both sides of the communication cannot go to sleep at the same time. If the application requires wireless routing instead of P2P communication; or interoperability with other vendors' devices; or a standard-based solution, for marketability.

4.5 IEEE 802.15.4 SPECIFICATION

After the initial 2003 release of the IEEE specification, a 2006 revision was published to clarify a few issues. Referred to as IEEE 802.15.4b or 802.15.4-2006, the revision added two PHY layer definitions in the sub-GHz spectrum and modified the security module.

Most of the market's current products, however, use the original, IEEE 802.15.4a specification – also called IEEE 802.15.4-2003 or Revision A.

The Microchip MRF24J40MA radio supports Revision A of the specification

.

4.6 PHYSICAL LAYERS

The MiWi P2P stack uses only a portion of the IEEE 802.15.4 specification's rich PHY and MAC layers' definitions. The specification defines three PHY layers, operating on a spectrum of 868 MHz, 915 MHz and 2.4 GHz. The MRF24J40MA radio operates on the 2.4 GHz, Industrial, Scientific and Medical (ISM) band – freely available worldwide.

That spectrum has 16 available channels and a maximum packet length of 127 bytes, including a two-byte Cyclic Redundancy Check (CRC) value. The total bandwidth for the IEEE 802.15.4, 2.4 GHz ISM band is, theoretically, 250 kbps. In reality, for reliable communication, the bandwidth is 20-30 kbps.

4.7 SUPPORTED TOPOLOGIES

IEEE 802.15.4 and the MiWi P2P stack support two topologies: Star and Peer-to-Peer.

4.7.1 STAR TOPOLOGY

A typical star topology is shown in Figure 1. From a device role perspective, the topology has one Personal Area Network (PAN) coordinator that initiates communications and accepts connections from other devices. It has several end devices that join the communication. End devices can establish connections only with the PAN coordinator. As to functionality type, the star topology's PAN coordinator is a Full Function Device (FFD). An end device can be an FFD with its radios on all the time, or a Reduced Function Device (RFD) with its radio off when it is Idle. Regardless of its functional type, end devices can only talk to the PAN coordinator.

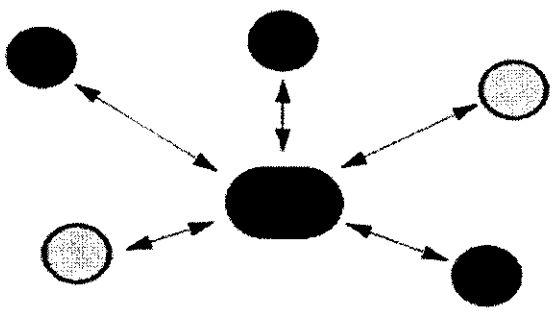

FIGURE: 4.1 STAR TOPOLOGY

4.7.2 PEER-TO-PEER (P2P) TOPOLOGY

A typical P2P topology is shown in Figure 2. From a device role perspective, this topology also has one PAN coordinator that starts communication and the end devices. When joining the network, however, end devices do not have to establish their connection with the PAN coordinator. As to functional types, the PAN coordinator is an FFD and the end devices can be FFDs or RFDs. In this topology, however, end devices that are FFDs can have multiple connections. Each of the end device RFDs, however, can connect to only one FFD and cannot connect to another RFD.

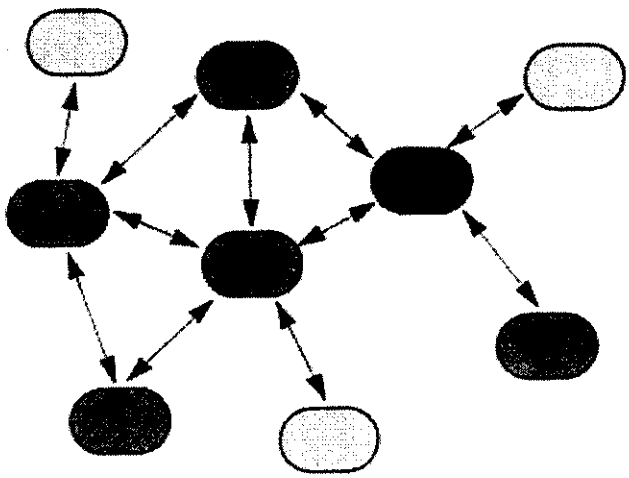

FIGURE: 4.2 PEER -TO - PEER TOPOLOGY

4.8 IEEE802.15.4 WIRELESS TRANCIEVER

The MRF24J40MA is a 2.4 GHz IEEE Std. 802.15.4™ compliant, surface mount module with integrated crystal, internal voltage regulator, matching circuitry and PCB antenna. The MRF24J40MA module operates in the non-licensed 2.4 GHz frequency band and is FCC, IC and ETSI compliant. The integrated module design frees the integrator from extensive RF and antenna design, and regulatory compliance testing, allowing quicker time to market.

The MRF24J40MA module is compatible with Microchip's ZigBee, MiWi and MiWi P2P software stacks. The MRF24J40MA module has received regulatory. Approvals for modular devices in the United States (FCC), Canada (IC) and Europe (ETSI). Modular approval removes the need for expensive RF and antenna design and allows the end user to place theMRF24J40MA module inside a finished product and not require regulatory testing for an intentional radiator (RF transmitter).

4.8.1 OPERATIONAL FEATURES

- Operating Voltage: 2.4-3.6V (3.3V typical)
- Temperature Range: -40°C to +85°C Industrial
- Simple, Four-Wire SPI Interface
- Low-Current Consumption:

TABLE: 4.1 PIN DESCRIPTION OF TRANSCEIVER

PIN	SYMBOL	TYPE	DESCRIPTION
1	GND	Power	Ground
2	RESET	DI	Global hardware Reset Pin
3	WAKE	DI	External Wake-Up Trigger
4	INT	DO	Interrupt pin to microcontroller
5	SDI	DI	Serial interface data input
6	SCK	DI	Serial interface clock
7	SDO	DO	Serial interface data output from MRF24J40
8	CS	DI	Serial interface enable
9	NC	_	No connection
10	VIN	Power	Power supply
11	GND	Ground	Ground
12	GND	Ground	Ground

4.8.2 NETWORK TYPE

The MiWi P2P stack supports only non-beacon networks. In a non-beacon network, any device can transmit data at any time, as long as the energy level (noise) is below the predefined level. Non-beacon networks increase the power consumption by FFD devices because they must have their radios on all the time. These networks reduce the power consumption of RFD devices, however, because the RFDs do not have to perform the frequent synchronizations

4.8.3 NETWORK ADDRESSING

The IEEE 802.15.4 specification defines two kinds of addressing mechanisms:

• Extended Organizationally Unique Identifier (EUI) or long address – An eight-byte address that is unique for each device, worldwide. The upper three bytes are purchased from IEEE by the company that releases the product. The lower five bytes are assigned by the device manufacturer as long as each device's full EUI is unique.

• Short Address – A two-byte address that is assigned to the device by its parent when it joins the network. The short address must be unique within the network.

The MiWi P2P stack supports only one-hop communication, so it transmits messages via EUI – or long addresses addressing. Short addressing is used only when the stack transmits a broadcast message. This is because there is no predefined broadcast long address defined in the IEEE 802.15.4 specification.

4.8.4 MESSAGE FORMAT

The message format of the MiWi P2P stack is a subset of the IEEE 802.15.4 specification's message format. Figure 3 shows the stack's packet format and its fields.

Bytes	2	1	2	2/8	0/2	8	Variable	2
	Frame Control	Sequence Number	Destination PAN ID	Destination Address	Source PAN ID	Source Address	Pay Load	Frame Check Sequence

Addressing Fields

FIGURE: 4.3 WIRELESS PROTOCOL STACK PACKET FORMAT

4.8.5 FRAME CONTROL

The three-bit frame type field defines the type of packet. The values can be:

- Data frame = 001
- Acknowledgement = 010
- Command frame = 011

In the stack, however, the Acknowledgement frame is not used, since all Acknowledgement packets are handled by hardware in the MRF24J40 radio. The security enabled bit indicates if the current packet is encrypted. If encryption is used, there will be an additional security header which will be detailed in later sections on the security feature.

The frame pending bit is used only in the Acknowledgement packet handled by the MRF24J40MA radio hardware. The bit indicates if an additional packet will follow the Acknowledgement after a data request packet is received from a RFD end device.

The intra PAN bit indicates if the message is within the current PAN. If this bit is set to '1', the source PAN ID field in the addressing fields will be omitted. In the stack, this bit is always set to '1', but it could be set to '0' to enable inter-PAN communication. Resetting the bit to '0' can be done in the application layer, if necessary.

The Destination Address mode can be either:

- 16-Bit Short Address mode = 10
- 64-Bit Long Address mode = 11

In the MiWi P2P stack, the Destination Address mode is usually set to the Long Address mode. The Short Address mode is used only for a broadcast message. For broadcast messages, the destination address field in the addressing fields will be fixed to 0xFFFF. The Source Address mode for the MiWi P2P stack can only be the 64-Bit Long Address mode

➢ SEQUENCE NUMBER

The sequence number is eight bits long. It starts with a random number and increases by one each time a data or command packet has been sent. The number is used in the Acknowledgement packet to identify the original packet. The sequence number of the original packet and the Acknowledgement packet must be the same

➢ DESTINATION PAN ID

This is the PAN identifier for the destination device. If the PAN identifier is not known, or not required, the broadcast PAN identifier (0xFFFF) can be used.

➢ DESTINATION ADDRESS

The destination address can either be a 64-bit long address or a 16-bit short address. The destination address must be consistent with the Destination Address mode defined in the frame control field. If the 16-bit short address is used, it must be the broadcast address of 0Xffff.

➢ SOURCE PAN ID

The source PAN identifier is the PAN identifier for the source device and must match the intra-PAN definition in the frame control field. The source PAN ID will exist in the packet only if the intra-PAN value is '0'. In the current MiWi P2P stack implementation, all communication is intra-PAN. As a result, all packets do not have a source PAN ID field. However, the stack reserves the capability for the application layer to transmit the message inter-PAN. If a message needs to transmit inter-PAN, the source PAN ID will be used.

➢ SOURCE ADDRESS

The source address field is fixed to use the 64-bit extended address of the source device.

➢ TRANSMITTING AND RECEIVING

The MiWi P2P stack transmits and receives packets according to the IEEE 802.15.4 specification, with a few exceptions.

➢ TRANSMITTING MESSAGES

There are two ways to transmit a message: broadcast and unicast. Broadcast packets have all devices in the radio range as their destination. IEEE 802.15.4 defines a specific short address as the broadcast address, but has no definition for the long address. As a result, broadcasting is the only situation when the MiWi P2P stack uses a short address. There is no Acknowledgement for broadcasting messages.

Unicast transmissions have only one destination and use the long address as the destination address. The MiWi P2P stack requires Acknowledgement for all unicast messages. If the transmitting device has at least one device that turns off its radio when Idle, the transmitting device will save the message in RAM and wait for the sleeping

device to wake-up and request the message. This kind of data transmitting is called indirect messaging. If the sleeping device fails to acquire the indirect message, it will expire and be discarded. Usually, the indirect message time-out needs to be longer than the pulling interval for the sleeping device.

➢ RECEIVING MESSAGES

In the MiWi P2P stack, only the messaged device will be notified by the radio. If the messaged device turns off its radio when Idle, it can only receive a message from the device to which it is connected. For the idling device with the turned off radio to receive the message, the device must send a data request command to its connection peer. Then, it will acquire the indirect message if there is one.

CHAPTER 5
MICRO ELECTRO MECHANICAL SYSTEMS

5.1 MICRO ELECTRO MECHANICAL SYSTEMS ACCELEROMETER

An accelerometer is a device for measuring acceleration and gravity induced reaction forces. Single- and multi-axis models are available to detect magnitude and direction of the acceleration as a vector quantity. Accelerometers can be used to sense inclination, vibration, and shock. They are increasingly present in portable electronic devices.

Modern accelerometers are often small micro electro-mechanical systems (MEMS), and are indeed the simplest MEMS devices possible, consisting of little more than a cantilever beam with a proof mass (also known as seismic mass). Mechanically the accelerometer behaves as a mass-damper-spring system; the damping results from the residual gas sealed in the device. As long as the Q-factor is not too low, damping does not result in a lower sensitivity.

Under the influence of gravity or acceleration the proof mass deflects from its neutral position. This deflection is measured in an analog or digital manner. Most commonly the capacitance between a set of fixed beams and a set of beams attached to the proof mass is measured. This method is simple and reliable; it also does not require additional process steps making it inexpensive. Integrating piezoresistors in the springs to detect spring deformation, and thus deflection, is a good alternative, although a few more process is needed. For very high sensitivities quantum tunnelling is also used; this requires specific fabrication steps making it more expensive. Optical measurement has been demonstrated on laboratory scale.

Another, far less common, type of MEMS-based accelerometer contains a small heater at the bottom of a very small dome, which heats the air inside the dome to cause it to rise. A thermocouple on the dome determines where the heated air reaches the dome and the deflection off the center is a measure of the acceleration applied to the sensor.

Most micromechanical accelerometers operate in-plane, that is, they are designed to be sensitive only to a direction in the plane of the die. By integrating two devices perpendicularly on a single die a two-axis accelerometer can be

made. By adding an additional out-of-plane device three axes can be measured. Such a combination always has a much lower misalignment error than three discrete models combined after packaging.

Micromechanical accelerometers are available in a wide variety of measuring ranges, reaching up to thousands of g's. The designer must make a compromise between sensitivity and the maximal acceleration that can be measured.

5.2 MEMS ACCELEROMETER LIS302DL

The LIS302DL is an ultra compact low-power three axes linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I2C/SPI serial interface. The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon. The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit which is trimmed to better match the sensing element characteristics. The LIS302DL has dynamically user selectable full scales of ±2g/±8g and it is capable of measuring accelerations with an output data rate of 100Hz or 400Hz. A self-test capability allows the user to check the functioning of the sensor in the final application. The device may be configured to generate inertial wake-up/free-fall interrupt signals when a programmable acceleration threshold is crossed at least in one of the three axes. Thresholds and timing of interrupt generators are completely programmable by the end user on the fly. The LIS302DL is available in plastic Thin Land Grid Array package (TLGA) and it is guaranteed to operate over an extended temperature range from -40°C to +85°C. The LIS302DL belongs to a family of products suitable for a variety of applications:

– Free-Fall detection

– Motion activated functions

– Gaming and Virtual Reality input devices

– Vibration Monitoring and Compensation

5.2.1 FEATURES:

- Three axes
- SPI/I2C digital interface
- Innovative embedded functionalities
- Two highly flexible and programmable interrupt request outputs

- Programmable thresholds and timing of interrupt signals
- 2.16V to 3.6V supply voltage
- 1.8V compatible I/Os
- <1mW power consumption
- Temperature range -40 to +85°C
- ±2/±8g selectable full scale range
- Embedded high pass filter
- Embedded self-test
- 10,000g high shock survivability
- LGA package 3x5x0.9mm3
- ECOPACK® – RoHS Directive and green compliant

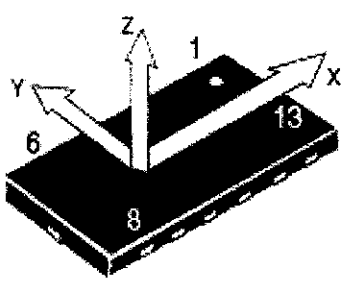

FIGURE 5.1: ACCELEROMETER

TABLE: 5.1 PIN DESCRIPTION OF MEMS ACCELEROMETER

PIN	Name	Function
1	Vdd IO	Power supply for I/O pins
2	GND	0V supply
3	Reserved	Connect to Vdd
4	GND	0V supply
5	GND	0V supply
6	Vdd	Power supply
7	CS	SPI enable I2C/SPI mode selection (1: I2C mode; 0:SPenabled)
8	INT 1	Inertial interrupt 1
9	INT 2	Inertial interrupt 2
10	GND	0V supply
11	Reserved	Connect to Gnd
12	SDO	SPI Serial Data Output I^2C less significant bit of the device address
13	SDA SDO SDI	I2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
14	SCL SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)

5.2.2 SENSITIVITY

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (point to the sky) and noting the output value again. By doing so, ±1g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one and dividing the result by 2 leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The Sensitivity Tolerance describes the range of Sensitivities of a large population of sensor.

5.2.3 ZERO-G LEVEL

Zero-g level Offset (Off) describes the deviation of an actual output signal from the ideal output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0g in X axis and 0g in Y axis whereas the Z axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress to a precise MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature; see "Zero-g level change vs. temperature". The Zero-g level of an individual sensor is stable over lifetime. The Zero-g level tolerance describes the range of Zero-g levels of a population of sensors.

5.2.4 FUNCTIONALITY

The LIS302DL is an ultracompact, low-power, digital output 3-axis linear accelerometer packaged in a LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an I^2C/SPI serial interface.

5.2.5 SENSING ELEMENT

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows carrying out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on

top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation. When acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor. At steady state the nominal value of the capacitors is few pF and when acceleration is applied the maximum variation of the capacitive load is in FF range.

5.2.6 IC INTERFACE

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by analog-to-digital converters. The acceleration data may be accessed through an I2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller. The LIS302DL features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in digital system employing the device itself. The LIS302DL may also be configured to generate an inertial Wake-Up and Free-Fall interrupt signal accordingly to a programmed acceleration event along the enabled axes. Both Free-Fall and Wake-Up can be available simultaneously on two different pins.

5.3 MEMS GYROSCOPE INTRODUCTION

Micro machined inertial sensors, consisting of accelerometers and gyroscopes are one of the most important types of silicon- based sensors. Micro accelerometers alone have the second largest sales volume after pressure sensors. It is believed that gyroscopes will soon be mass-produced at similar volumes once manufacturers are able to meet a $10 price target. Applications for gyroscopes are very broad. Some example for these applications are; automotive; vehicle stability control, rollover detection, navigation, load levelling/suspension control, event recording, collision avoidance; consumers, computer input devices, handheld computing devices, game controllers, virtual reality gear, sports equipment, camcorders, robots; industrial., navigation of autonomous (robotic) guided vehicles, motion control of hydraulic equipment or robots, platform stabilization of heavy machinery, human transporters, yaw rate control of wind-power plants; aerospace/military; platform stabilization of avionics, stabilization of pointing systems for antennas, unmanned air vehicles, or land vehicles, inertial measurement units for inertial navigation, and many more. This paper presents a review of silicon MEMS gyroscopes (rate sensors), their production status, and challenges towards fabrication of the next generation of low cost

gyroscopes. Following a brief introduction to gyroscope operating principles and performance specifications, the present status in the commercialization of micro-machined rate sensors are discussed. Inertial sensors have seen a steady improvement in their performance and their fabrication technology, and today, micro accelerometers are among the highest volume MEMS sensors for the automotive. While the performance of gyroscopes has improved by a factor of 10 every two years, their costs have not dropped as was originally predicted. The initial drive for lower cost, greater functionality, higher levels of integration, and higher volume had slowed down during the optical bubble, when the sensor market was over taken with high potential returns promised by the telecom market. Although the telecom boom had slowed the wide spread development in gyroscopes, it poured billions of dollars into development of next generation MEMS technologies, equipment, modelling tools, foundries, and micro machine experts. This paper will discuss some of these advancements in MEMS development and their potential use in the creation of the next generation of advanced, integrated MEMS gyroscopes that can meet the market cost expectations, and further their performance.

5.3.1 MICROMACHINED GYROSCOPE TECHNOLOGY

Operating Principles and Specifications Almost all reported micro machined gyroscopes use vibrating mechanical elements (proof-mass) to sense rotation. They have no rotating parts that require bearings, and hence they can be easily miniaturized and batch fabricated using micromachining techniques. All vibratory gyroscopes are based on the transfer of energy between two vibration modes of a structure caused by Coriolis acceleration. Coriolis acceleration, named after the French scientist and engineer G. G. de Coriolis (1792–1843), is an apparent acceleration that arises in a rotating reference frame and is proportional to the rate of rotation, Fig. 1.

Vibratory gyroscopes were demonstrated in the early 1980's. An examples of this type of devices is quartz tuning forks like the Quartz Rate Sensor by Systron Donner. Although quartz vibratory gyroscopes can yield very high quality factors at atmospheric pressure with improved level of performance, due to use of quartz as the primary material, their batch processing is not compatible with IC fabrication technology. In the late 1980's, after successful demonstration of batch- fabricated silicon accelerometers, some efforts were initiated to replace quartz with silicon in micro machined vibratory gyroscopes. Charles Stark Draper Laboratory demonstrated one of the first batch fabricated silicon micro machined rate gyroscopes in 1991.

In general, gyroscopes can be classified into three Figure1- Coriolis accelerometer concept different categories based on their performance: inertial - grade, tactical-grade, and rate-grade devices. Table 1 summarizes the requirements for each of these categories. Over the past decade, much of the effort in developing micro machined silicon gyroscopes has concentrated on "rate-grade" devices, primarily because of their use in automotive Applications. Automotive applications generally requires a full-scale range of at least 50°-300° /s and a resolution of about 0.5°- 0.05 °/s in a bandwidth of less than 100 Hz depending on the application. The operating temperature is in the range from -40 to 85° C. Tuning fork gyroscopes contain a pair of masses that are driven to oscillate with equal amplitude but in opposite directions. When rotated, the Coriolis force creates an orthogonal vibration that can be sensed by a variety of mechanisms. The Draper Lab gyro, figure 2, uses comb-type structures to drive the tuning fork into resonance, and rotation about either in-plane axis results in the moving masses to lift, a change that can be detected with capacitive electrodes under the mass.

Vibrating-Wheel Gyroscopes have a wheel that is driven to vibrate about its axis of symmetry, and rotation about either in-plane axis results in the wheel's tilting, a change that can be detected with capacitive electrodes under the wheel, Figure 3. It is possible to sense two axes of rotation with a single vibrating wheel. A surface micro machined polysilicon vibrating wheel gyro, Figure 4, has been designed at the U.C. Berkeley Sensors and Actuators Center that demonstrated this capability

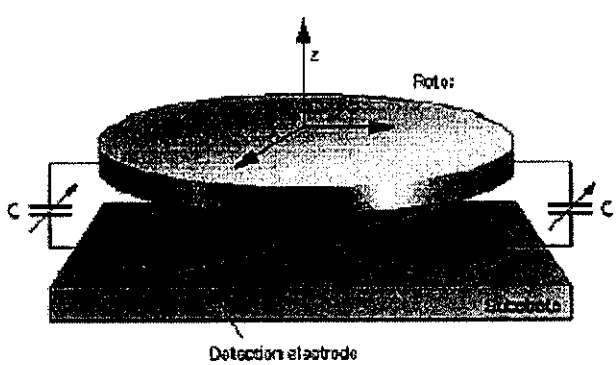

FIGURE 5.2: GYRO WHEEL

CHAPTER 6
GRAPHICS LCD

6.1 INTRODUCTION

The PCD8544 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCD8544 interfaces to microcontrollers through a serial bus interface. The PCD8544 is manufactured in n-well CMOS technology.

6.1.1 FEATURES

- Single chip LCD controller/driver
- 48 row, 84 column outputs
- Display data RAM 48*84 bits
- On-chip:
  - Generation of LCD supply voltage (external supply also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External RES (reset) input pin
- Serial interface maximum 4.0 Mbits/s
- CMOS compatible inputs
- Mux rate: 48
- Logic supply voltage range VDD to VSS: 2.7 to 3.3 V
- Display supply voltage range VLCD to VSS
  - 6.0 to 8.5 V with LCD voltage internally generated (voltage generator enabled)
  - 6.0 to 9.0 V with LCD voltage externally supplied (voltage generator switched-off).
- Low power consumption, suitable for battery operated systems
- Temperature compensation of VLCD
- Temperature range: − 25 deg □to +70 deg

6.1.2 PIN DESCRIPTION

TABLE 6.1: PIN DESCRIPTION OF GRAPHICS LCD

SYMBOL	DESCRIPTION
R0 to R47	LCD row driver outputs
C02 to C83	LCD column diver outputs
Vss1,Vss2	Ground
Vdd1,Vdd2	Supply Voltage
Vlcd1,Vlcd2	LCD supply voltage
T1	Test 1 input
T2	Test 2 output
T3	Test 3 input/output
T4	Test 4 input
SDIN	Serial data input
SCLK	Serial clock input
D/C	Data/command
SCE	Chip enable
OSC	Oscillator
RES	External reset input
Dummy 1,2,3,4	not connected

- **R0 TO R47 ROW DRIVER OUTPUTS**

  These pads output the row signals.

- **C0 TO C83 COLUMN DRIVER OUTPUTS**

  These pads output the column signals.

- **VSS1, VSS2: NEGATIVE POWER SUPPLY RAILS**

  Supply rails VSS1 and VSS2 must be connected together.

- **VDD1, VDD2: POSITIVE POWER SUPPLY RAILS**

  Supply rails VDD1 and VDD2 must be connected together.

- **VLCD1, VLCD2: LCD POWER SUPPLY**

  Positive power supply for the liquid crystal display. Supply rails VLCD1 and VLCD2 must be connected together.

- **T1, T2, T3 AND T4: TEST PADS**

  T1, T3 and T4 must be connected to VSS; T2 is to be left open. Not accessible to user.

- **SDIN: SERIAL DATA LINE**

  Input for the data line.

- **SCLK: SERIAL CLOCK LINE**

  Input for the clock signal: 0.0 to 4.0 Mbits/s.

- **D/C: MODE SELECT**

  Input to select either command/address or data input.

- **SCE: CHIP ENABLE**

  The enable pin allows data to be clocked in. The signal is active LOW.

- **OSC: OSCILLATOR**

  When the on-chip oscillator is used, this input must be connected to VDD. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to VSS, the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power-down mode before stopping the clock.

- **RES: RESET**

  This signal will reset the device and must be applied to properly initialize the chip. The signal is active LOW.

6.2 FUNCTIONAL DESCRIPTION

❖ **Oscillator**

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to VDD. An external clock signal, if used, is connected to this input.

❖ **Address Counter (AC)**

The address counter assigns addresses to the display data RAM for writing. The X-address X6 to X0 and the Y-address Y2 to Y0 are set separately. After a write operation, the address counter is automatically incremented by 1, according to the V flag.

❖ **Display Data RAM (DDRAM)**

The DDRAM is a 48 ′ 84 bit static RAM which stores the display data. The RAM is divided into six banks of 84 bytes (6 ′ 8 ′ 84 bits). During RAM access, data is transferred to the RAM through the serial interface. There is a direct correspondence between the X-address and the column output number.

❖ **Timing generator**

The timing generator produces the various signals required to drive the internal circuits. Internal chip operation is not affected by operations on the databuses. 7.5 Display address counter. The display is generated by continuously shifting rows of RAM data to the dot matrix LCD through the column outputs. The display status (all dots on/off and normal/inverse video) is set by bits E and D in the 'display control' command.

❖ **LCD row and column drivers**

The PCD8544 contains 48 row and 84 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.

❖ **Addressing**

Data is downloaded in bytes into the 48 by 84 bits RAM data display matrix of PCD8544. The columns are addressed by the address pointer. The address ranges are: X 0 to 83 (1010011), Y 0 to 5 (101) Addresses outside these ranges are not allowed. In the vertical addressing mode (V = 1), the Y address increments after each byte .After the last Y address (Y = 5), Y wraps around to 0 and X increments to address the next column. In the horizontal addressing mode (V = 0), the X address increments after each byte (see Fig.6). After the last X address (X = 83), X wraps around to 0 and Y increments to address the next row. After the very last address (X = 83 and Y = 5), the address pointers wrap around to address (X = 0 and Y = 0).

CHAPTER 7

ALGORITHM OF THE PROJECT

7.1 TRACKER SECTION

- Initialize the header files.
- Define the P2P connection index.

  #define MOTE_1 0

  #define MOTE_2 1
- Buffer size is declared. This buffer size is used to store the values from accelerometer and gyroscope.
- Initialize the variable distance for accelerometer and angle for gyroscope.
- In order to give continuous flow of data from accelerometer and gyroscope, Digital LPF is declared.
- Initialize the function I^2C and adc.

Accessing the data

- Count variable is set to 0.It gets incremented when the data flow from abuffer and gbuffer.
- Delay is set to 32ms.

  delay32ms (0, 100);
- I^2C function gets the values from accelerometer.
- ADC function gets the values from gyroscope.
- Each data is having the transfer rate of 8 bits.
- For loop is used inside I^2C function, to get accelerometer values.
- For loop is used inside ADC function, to get gyroscope values.
- Next step is to write the data.
- In the digital low pass filter function, by using present value and previous value mean is taken.
- If the mean is greater than buffer size limit, the previous value is taken.

7.2 RECEIVER SECTION

- Define the mote for receiver.

  #define MOTE_0 0
- Define the angle threshold value.
- Initialize the variables distance, angle and direction.
- Delay is set to 32ms.

  delay32ms (0, 100);
- Move the values from transmitted data variables to received data variables.
- In order to receive the data one after another, shift them by 8 bits as per the order transmitted from the mote 1(tracker).
- If angle > threshold value, then direction is plotted in the LCD display.

CHAPTER 8

CIRCUIT DIAGRAM AND RESULT OF THE PROJECT

8.1 TRACKER SECTION

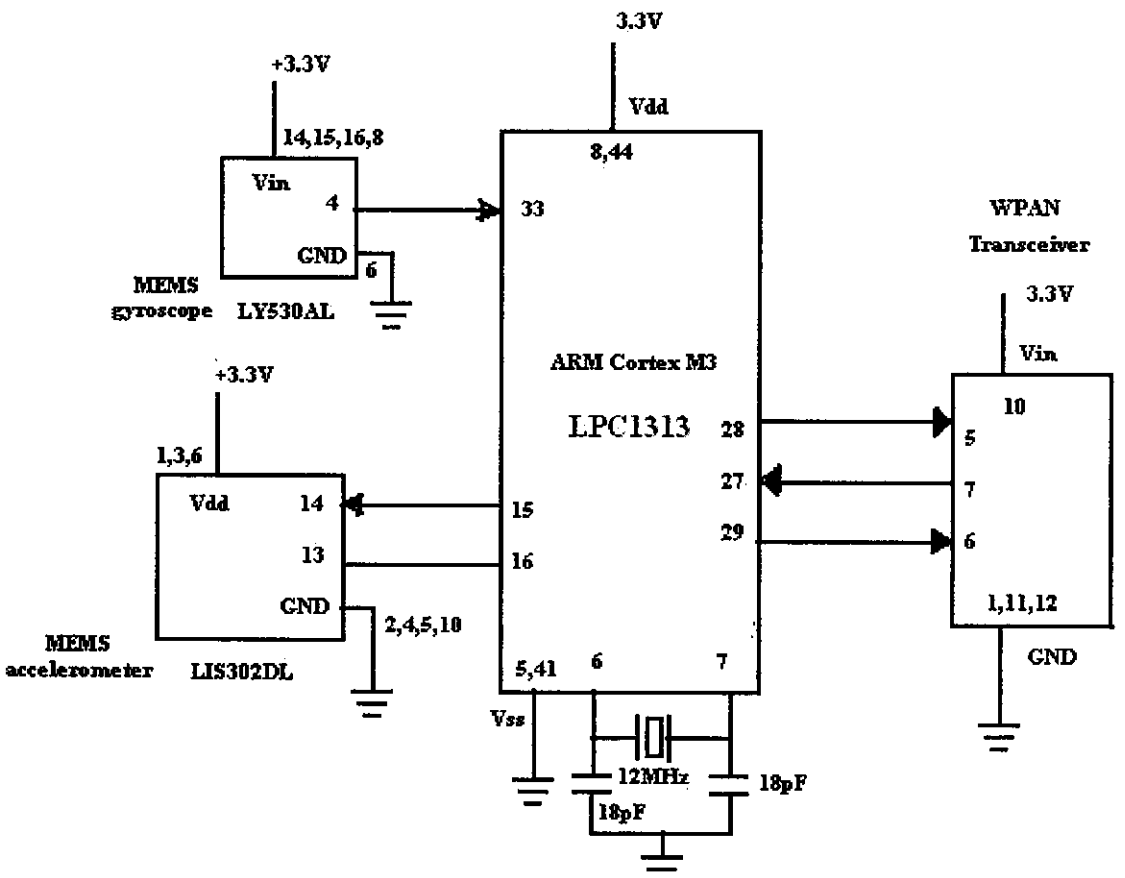

FIGURE 8.1: TRACKER SECTION

8.2 RECEIVER SECTION

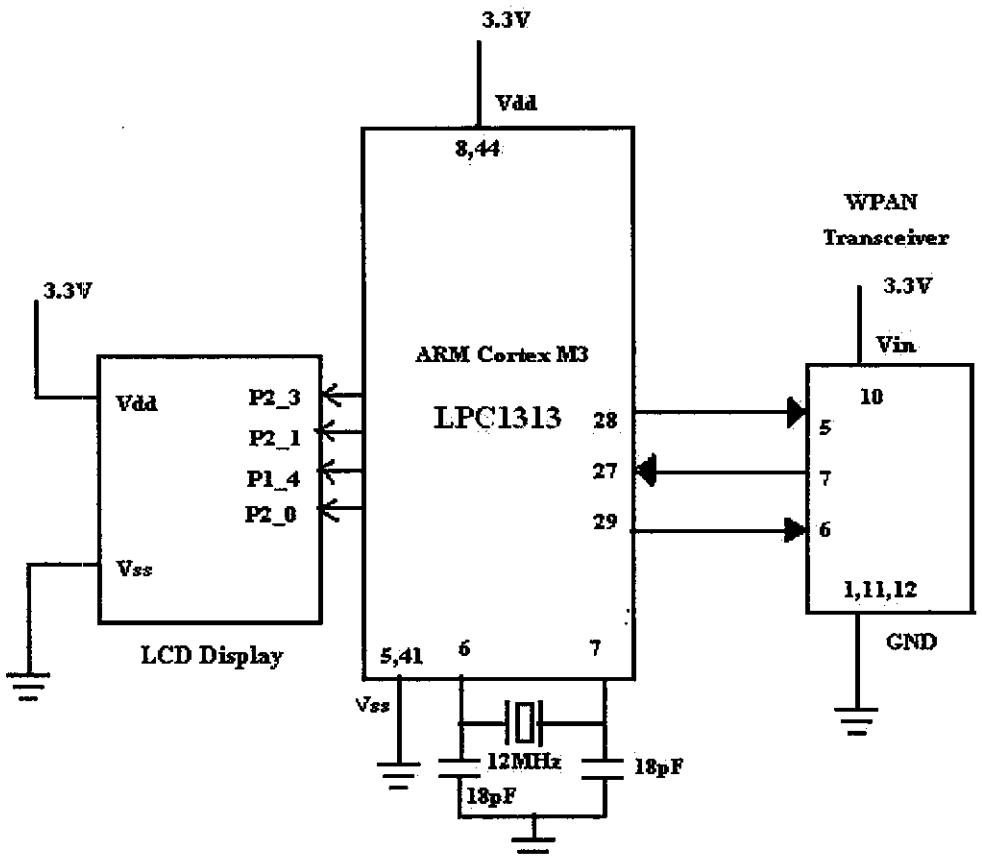

FIGURE 8.2: RECEIVER SECTION

8.3 CIRCUIT CONNECTIONS OF THE PROJECT

ARM CORTEX M3

- Pin 8: 3.3V input voltage.
- Pin 44: 3.3V supply voltage to the internal regulator and ADC.it is used as ADC reference voltage.
- Pin 5,41: Ground.
- Pin 33: General purpose digital input/output pin.
  A/D converter pin, input for timer.
- Pin 15: General purpose digital input/output pin.

Serial clock for interface using software control.

I^2Cbus clock input and output.

- Pin 16: General purpose digital input/output pin.

  Clear to send signal from interface.
- Pin 6: Input to the oscillator circuit and clock generator circuit. Input voltage is 1.8V
- Pin 7: Output from oscillator amplifier.
- Pin 27: General purpose digital input/output pin.

  A/D converter pin.

  Master in slave out for SPI.
- Pin 28: General purpose digital input/output pin.

  Master out slave in for SPI.
- Pin 29: General purpose digital input/output pin.

  Serial wire clock for interface.

MEMS ACCELEROMETER

- Pin 1,6:power supply.
- Pin 3:serial to pin 1.
- Pin 13:I^2C serial data

  Serial data input

  Interface serial data output
- Pin 14:I^2C serial clock

  Serial port clock
- Pin 2,4:ground.
- Pin 5,10:ground.

MEMS GYROSCOPE

- Pin 14: Supply voltage 2.7V to 3.6V.
- Pin 6: Ground
- Pin 4: Output to ARM.

- Pin 15,16: Supply voltage.
- Pin 12,8: Supply voltage.
- Pin 9,10: leave unconnected

WIRELESS PROTOCOL

- Pin 10:Supply voltage 3.3V.
- Pin 1,11,12: ground.
- Pin 5: SPI data input (master output slave input).
- Pin 7: SPI data output (master input slave output).
- Pin 6: clock signal.

8.4 RESULT

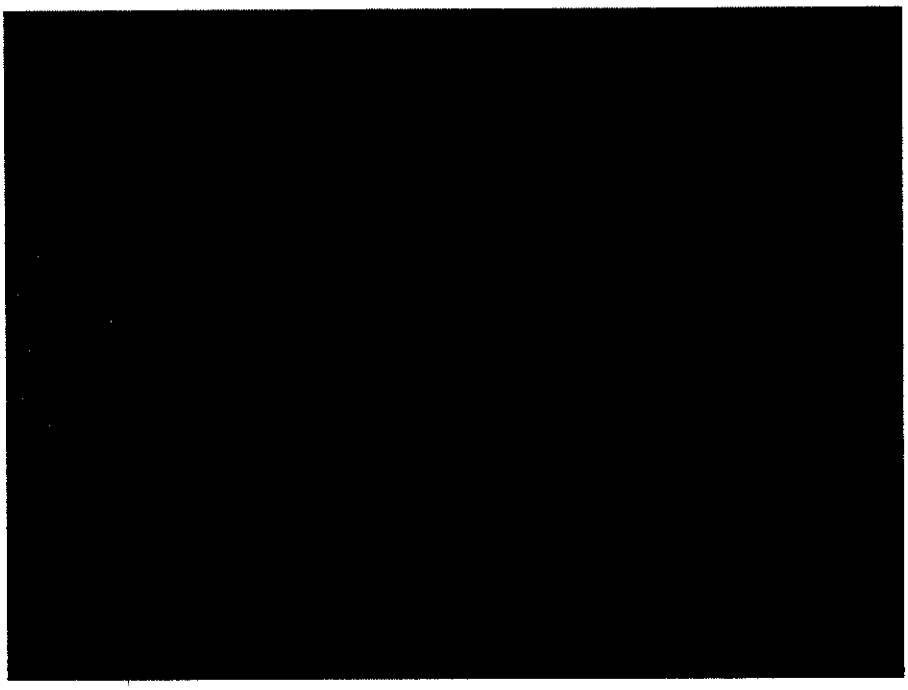

FIGURE 8.3: CIRCUIT OF TRACKING SECTION

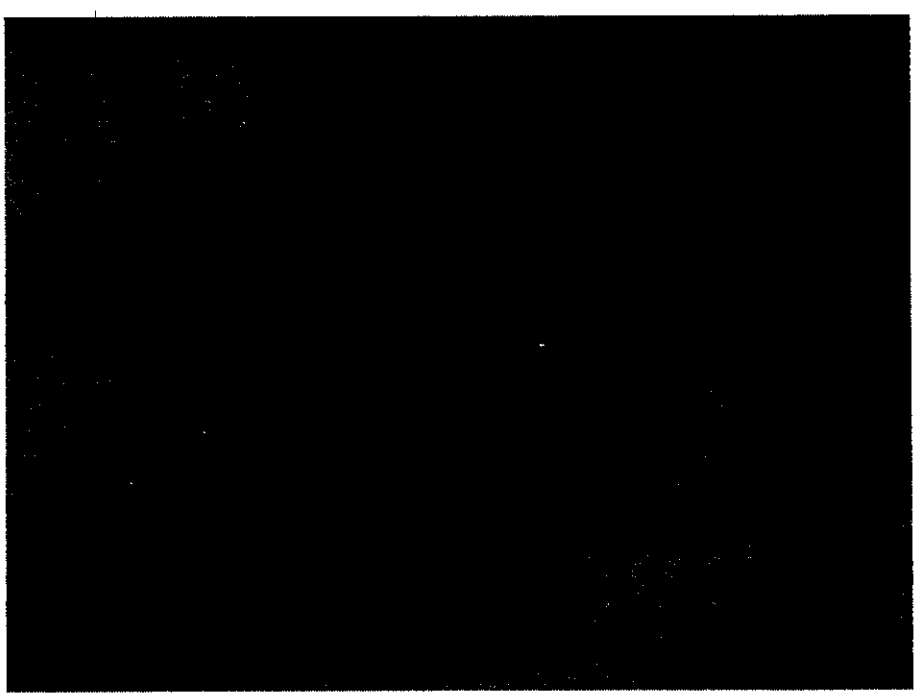

FIGURE 8.4: CIRCUIT OF RECEIVER SECTION

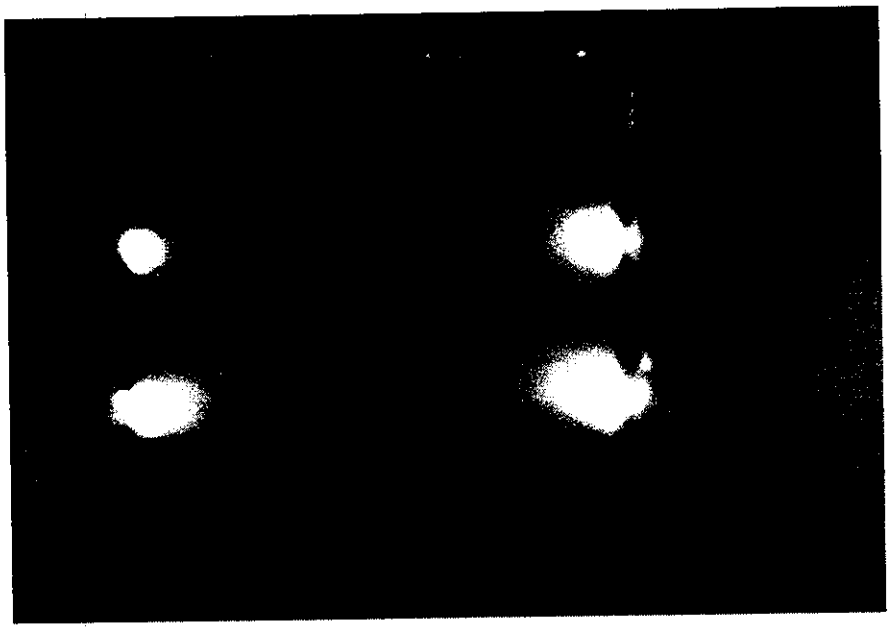

FIGURE 8.5: FINAL RESULT

RESULT

Thus the project is designed to track the location of a person in GPS denied environments such as tunnels and caves and also it can be useful in defence applications where members of a battle squad need to know each other's position all the time and in all the places during a critical operation. The person could be easily found by an outside person in case of an emergency. The device is designed to be operated on battery and consumes very low power.

CHAPTER 9
CONCLUSION

In this project, we have designed MEMS based wireless indoor tracking scheme which uses ARM Cortex microcontroller, MEMS Accelerometer and MEMS Gyroscope. Thus the project can track the location of a person in GPS denied environments such as tunnels and caves and also it can be useful in defence applications where members of a battle squad need to know each other's position all the time and in all the places during a critical operation. It is designed by using battery so it consumes in low power.

REFERENCES

[1] Ray, J., "Advanced GPS Receiver Technology", Lecture Notes, Geometrics Engineering, University of Calgary, Canada, 2002

[2] Hide C. and T. Moore , " GPS and low cost INS integration for positioning in the urban environment", Proceedings of ION GPS 2005, 13-16 September, Long Beach, CA, USA, pp. 1007-1015,2005

[3] Shin, E-H, "Estimation Techniques for Low-Cost Inertial Navigation". PhD Thesis, UCGE Report No. 20219, Department of Geometrics' Engineering, University of Calgary, Canada, 2005

[4] Wang, J-H. And Y. Gao, "High sensitivity GPS data classification based on signal degraded conditions", IEEE Transactions on Vehicular Technology, 2009

[5] Rell, J.L., "Inertial instrument error characterization", Proceedings of ION AM , 27-29 June, Cambridge, MA, USA, pp.1020-1025, 2008

[6] Joseph Yiu,"LPC1313 ARM Cortex M3 Microcontroller" Product datasheet Rev.01-11, 2009