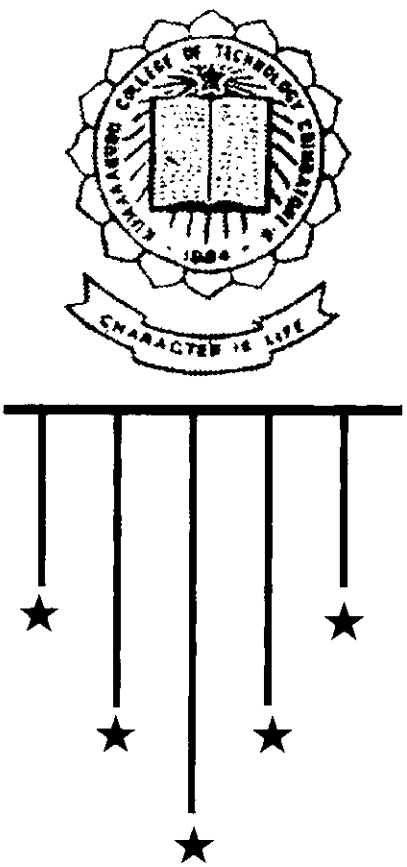
AUTOMOTIVE VOLTAGE VARIATION TESTS

PROJECT WORK P-358



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Submitted in partial fulfilment of the requirements
for the award of the degree of
BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING
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DEPARMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE-641 006

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to Certify that this Project Entitled

AUTOMOTIVE VOLTAGE VARIATION TESTS

has been submitted by

.....

in Partial fullfilment of the requirements for the award of the Degree of

BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING of the Bharathiyar University, Coimbatore-6. during the academic year 1999-2000.

Guide *Head of the Department*

Certified that the Candidate was examined by us in the Project Work.

Viva Voce Examination held on .....

University Register Number .....

Internal Examiner *External Examiner.*

SYNOPSIS

In automobile Industry, the Electronic Instruments have many advantages over the existing Mechanical Instruments such as High reliability, Quality and accuracy. Also the Complexity of the Mechanical devices can be reduced by the use of Electronic devices.

These Electronic Instruments may be affected by the voltage variations generated by the Electrical loads such as lamps, horns, motors, etc., in automobiles.

If a batery is not charged perfectly, it drains, which results in variation of voltage levels.

So to test whether the Electronic circuits could withstand these voltage variations, the **"AUTOMOTIVE VOLTAGE VARIATION TESTS"** which generate three voltage waveforms, to the specifications of automobile Industries as per International Standard. Further it checks for any malfunctioning of the Electronic Instuments against the variation in battery voltages under certain test conditions.

The Voltage waveforms generated are applied to the electronic Instrument which is to be tested, along with the frequency signal to check for any malfunctioning of the Instrument.

CONTENTS

1. AUTOMOBILE ELECTRICAL SYSTEM

The Electrical system of a modern automobile contain four main circuits as being the generating circuit, the starting circuit, the ignition circuit and the lighting circuit. Branches serve special purpose lights, audio, gasoline gage, heater, windshield wiper, defroster and several other accessory units. All the main circuits are connected together and linked to the battery as shown.

The starting or cranking motor is connected directly to the battery through cables and a switch to provide a low-resistance path for the large currents required by the motor.

The generating circuit (generator and control) is connected to one end of the car ammeter, if there is one, so that the meter registers in the 'charge' direction when current is being sent to the battery. A wire connects the other end of the ammeter or the generator directly to the cable leading to the ungrounded pole of the battery.

The ignition primary circuit, the lighting circuit and all the branch circuits are connected to the same side of the ammeter as if the generator so that, when the generator is operating, they receive current directly from it without going through the ammeter. When

2. VOLTAGE VARIATION TESTS.

As framed by many automobile industries as per the international Standards, three tests are to be conducted to check for any malfunctioning of the electronic instruments called as AUTOMOTIVE VOLTAGE VARIATION TESTS which has the following tests,

a) Momentary Interruption of Power Test

b) Supply Voltage Fluctuation Test I

c) Supply Voltage Fluctuation Test II

3. MOMENTARY INTERRUPTION OF POWER TEST

This test is conducted to check for any malfunctioning of the Instrument against possible variation in battery voltage , for instance at switching on the starter.

This has to carried out under the following conditions,

Voltage - 12volt

No. of cycles - 100 or more

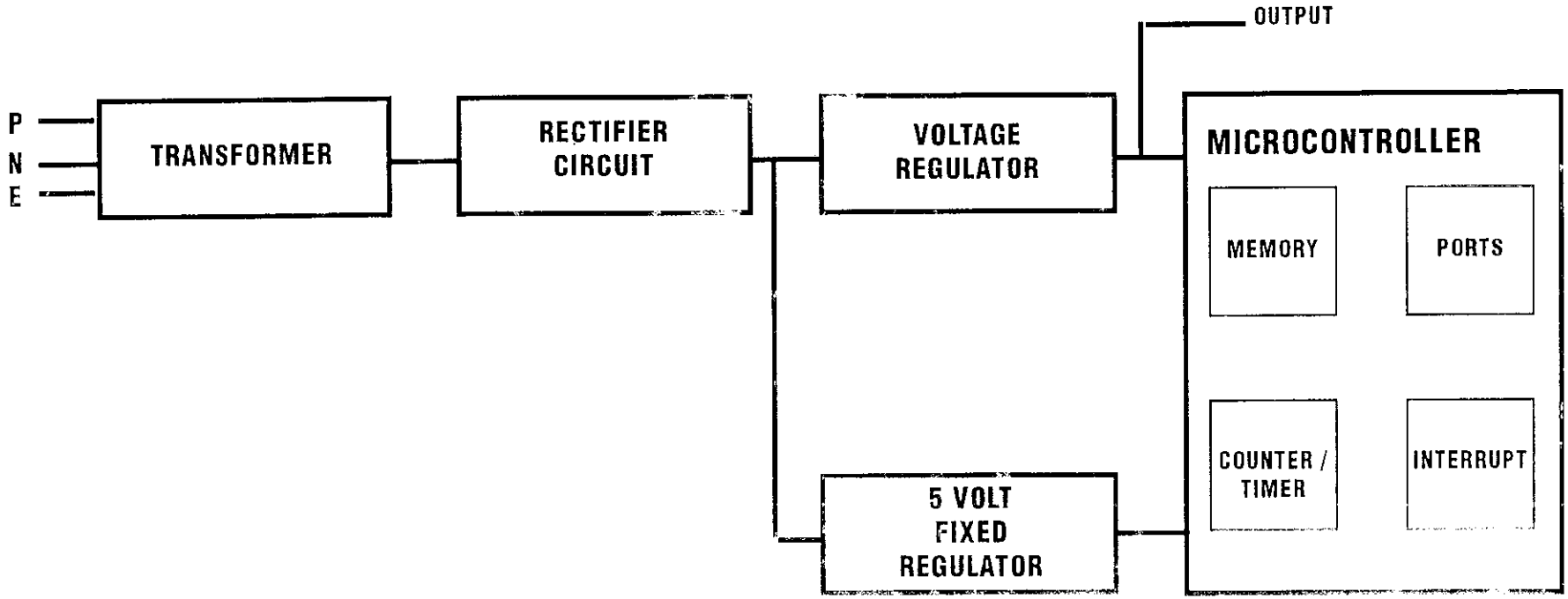
Operating Conditions - Speed - 0 Kmph

RPM- 0 rpm

Fuel - Full

Temperature- centre

BLOCK DIAGRAM :



Circuit Description

Transformer:

A step down tranformer is used whose input is 230v and output at 20v with 1amps current level.

Rectifier:

This block uses Diodes which rectifies the output from transformer. It uses four diodes which are biased accordingly.

Voltage Regulator:

The Voltage regulator outputs the voltage to a fixed level. 3v and 5v fixed Voltage regulators are used.

Micro Controller:

The Micro Controller uses is ZILOG Z86E04 which is Programmed. It is an 8 be CMos, 18 Pin, 124 bytes of Gereral purpose RAM, schmitt triggered micro controller.

4. SUPPLY VOLTAGE FLUTUATION TEST I

This test is conducted to check for possible fluctuation in supply voltage;at startup of the starter, under the following test conditions.

Voltage - 12volt

No. of cycles - 1000 or more

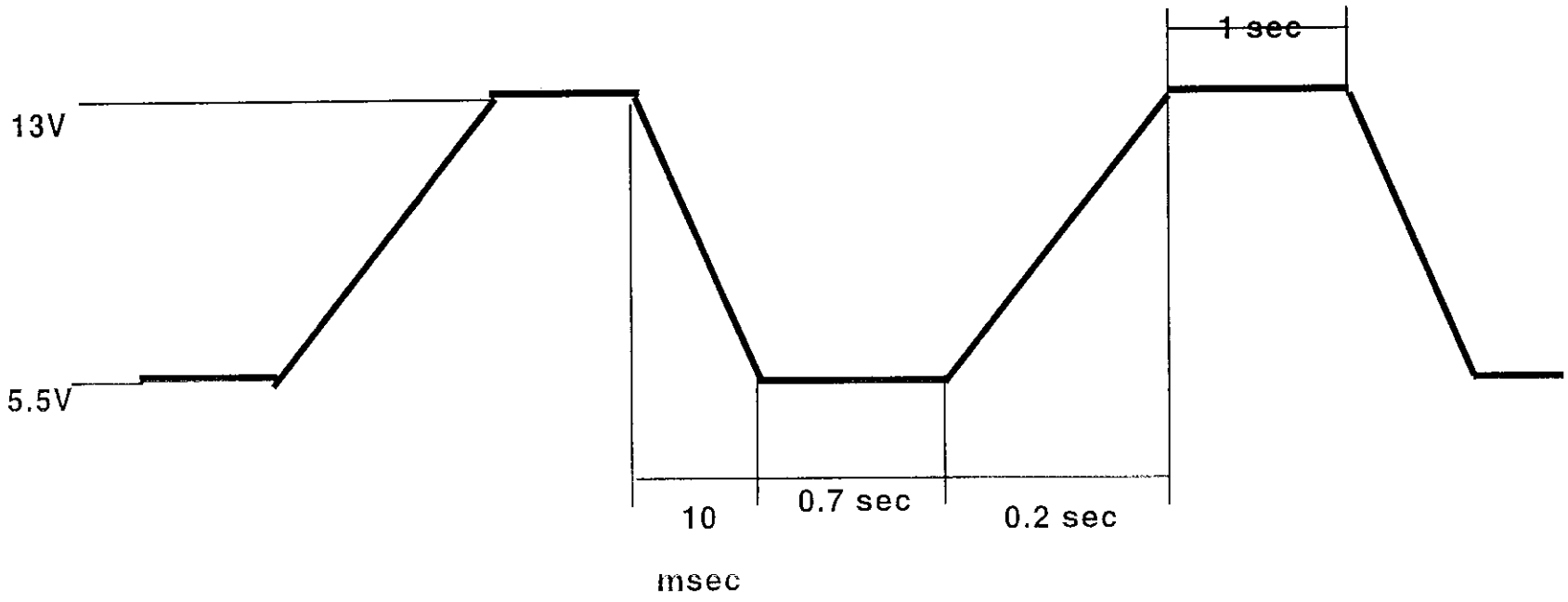
Operating Conditions - Speed - 0 Kmph

RPM- 0 rpm

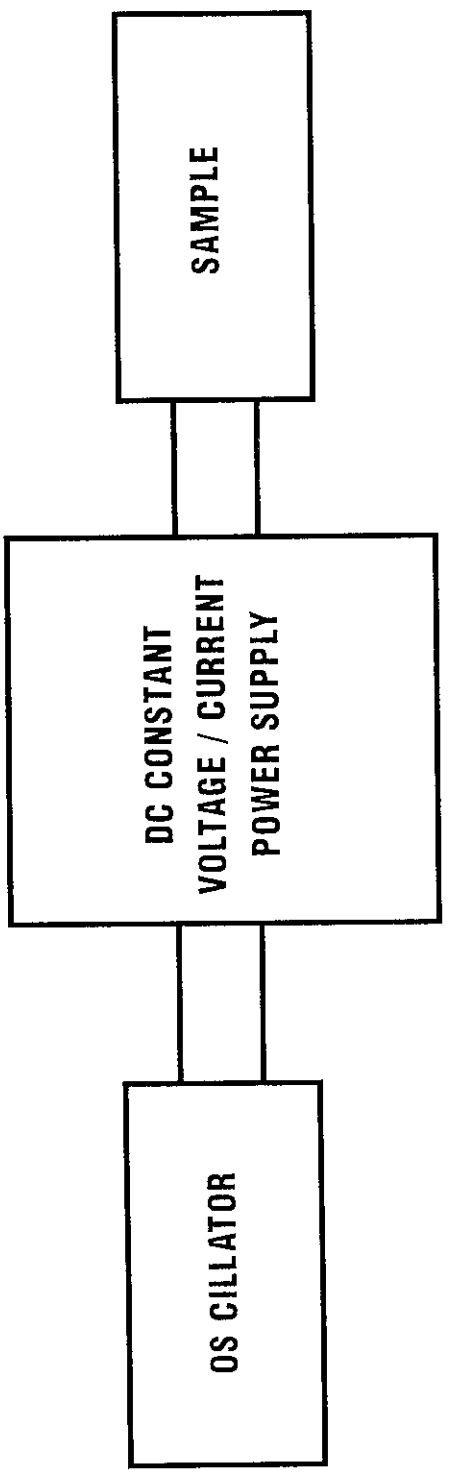
Fuel - Full

Temperature- centre

The Cyclic pattern of the test is shown below.



Applying the waveform to the line between the sample's power terminals, using the test circuit given below.



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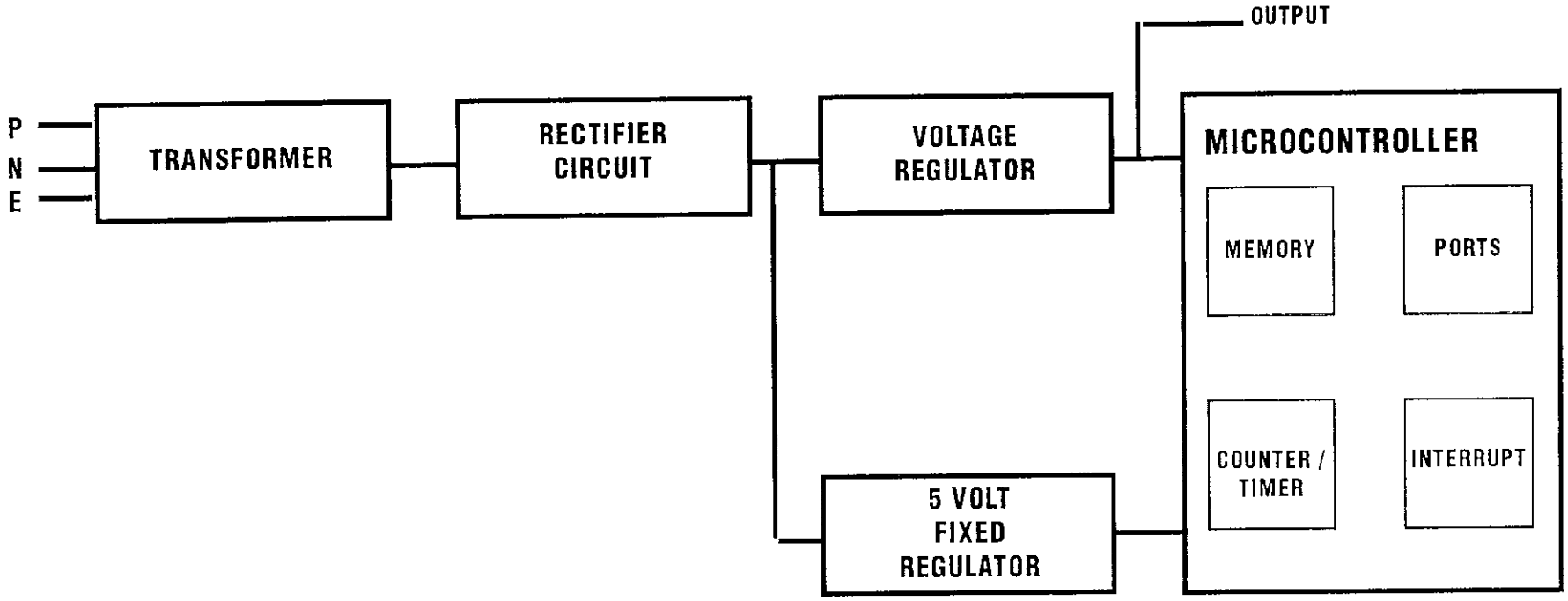

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This block uses Diodes which rectifies the output from transformer. It uses four diodes which are biased accordingly.

Voltage Regulator:

The Voltage regulator outputs the voltage to a fixed level. 3v and 5v fixed Voltage regulators are used.

Micro Controller:

The Micro Controller uses is ZILOG Z86E04 which is Programmed. It is an 8 be CMos, 18 Pin, 124 bytes of Gerera purpose RAM, schmitt triggered micro controller.

5. SUPPLY VOLTAGE FLUTUATION TEST II

This test is conducted to check for possible fluctuaticns in supply voltage; including ripple voltage to be output from the generator,under the following test conditions.

Voltage - 12volt
No. of cycles - 1000 or more
Operating Conditions - Speed - 0 Kmph
RPM- 0 rpm
Fuel - Full
Temperature- centre

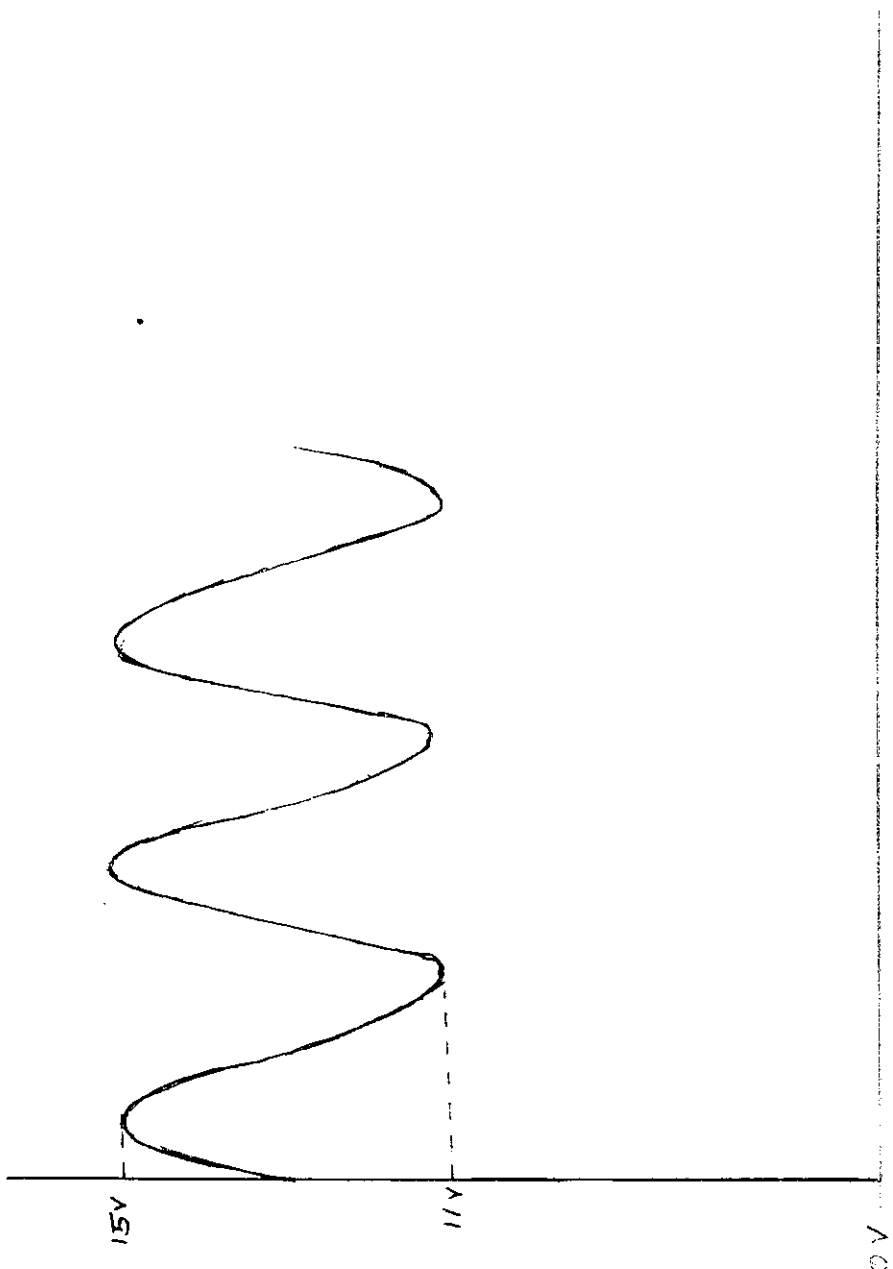
f -- ripple frequency to be fluctuated between 10 Hz and 10KHz during test.

Vr-- # **7±1v** for a product to be directly connected to the alternator output.

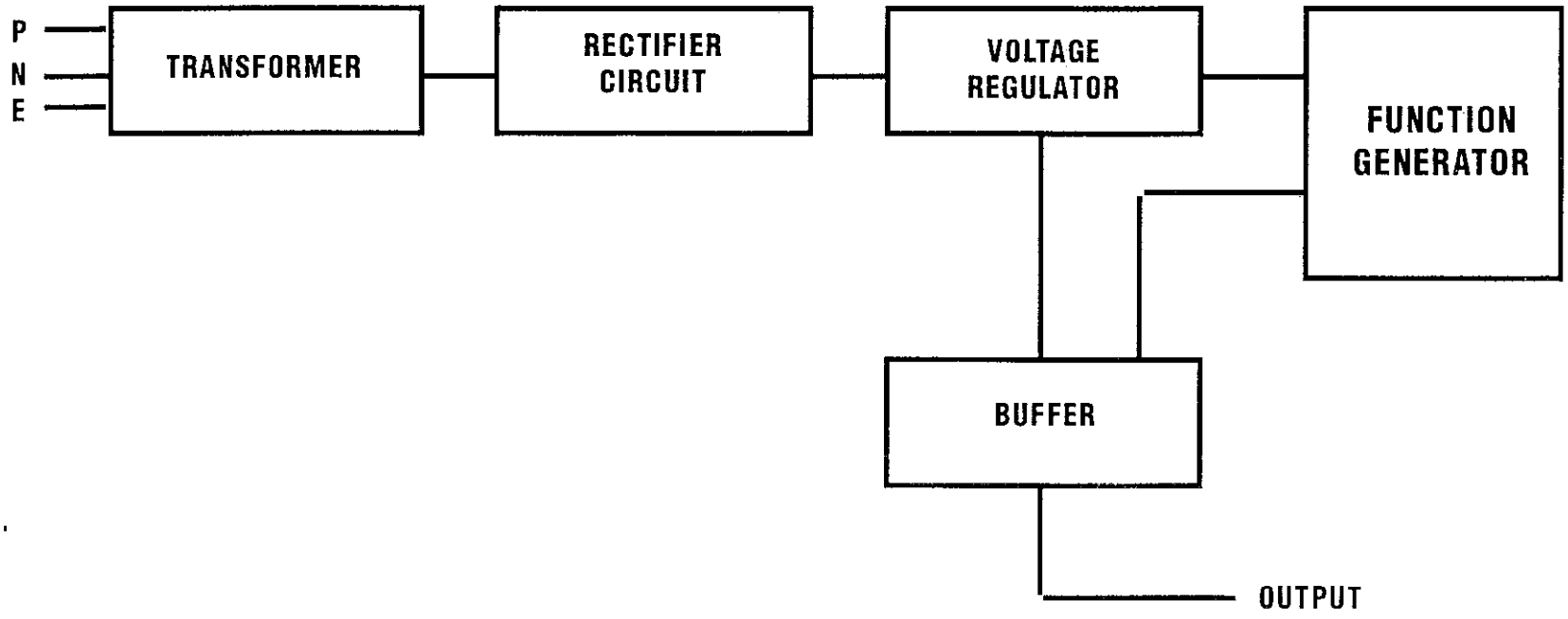
4±0.2v for a product whose voltage is to supplied from a battery and includes a large ripple voltage.

2±0.1v for a product whose voltage to be supplied from a battery, but which is excluded from above.

The Cyclic pattern of the test is shown below.



BLOCK DIAGRAM :



Circuit Description

Transformer:

A step down tranformer is used whose input is 230v and output at 20v with 1amps current level.

Rectifier:

This block uses Diodes which rectifies the output from transformer. It uses four diodes which are biased accordingly.

Voltage Regulator:

The Voltage regulator outputs the voltage to a fixed level. 3v and 5v fixed Voltage regulators are used.

Buffer:

It is also caused as Driver circuit. The main function of an buffer is to amplify the voltage or current level. Here it acts as an current amplifier.

Function Generator:

A 16 pin Monolithic function generator named XR2206. The main application of XR2206 is for waveform generation. The frequency of operation depends on timing Pesistor and timing capacitor. Its frequency ranges from 0.001Hz to more than 1 Mhz.

6. TEST SPECIFICATIONS

Momentary Interruption of Power Test

Voltage - 12V

Period - 2sec

No. of cycles - 100 or more

Operating Conditions -

Speed - 0 Kmph

RPM - 0 rpm

Fuel - Full

Temp - Center

Supply Voltage Fluctuation Test I and II

Operating Conditions -

Speed - 0 Kmph

RPM - 0 rpm

Fuel - Full

Temp - Center

f -- ripple frequency to be fluctuated between 10 Hz and 10KHz during test.

Vr-- # 7 ± 1v for a product to be directly connected to the alternator output.

4 ± 0.2v for a product whose voltage is to supplied from a battery and includes a large ripple voltage.

2 ± 0.1v for a product whose voltage to be supplied from a battery, but which is excluded from above.

7. MICROCONTROLLER

Z86E04 OTP CMOS 8-BIT MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 18-Pin DIP Package
- Low Noise Programmable
- ROM Protect Programmable
- 4.5 to 5.5 V Operating Range
- Low Power Consumpsion - 50 mW (Typical)
- Two Standby Modes - STOP and HALT
- 14 Input/Output Lines
- 124 Bytes of General Purpose RAM
- Six Vectored, Priority Interrupt from six different sources
- Clock Speed upto 8 MHz
- Watch-Dog Timer
- Power-On Reset
- Two On-Board Comparators
- Programmable Interrupt Polarity
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator.

GENERAL DESCRIPTION

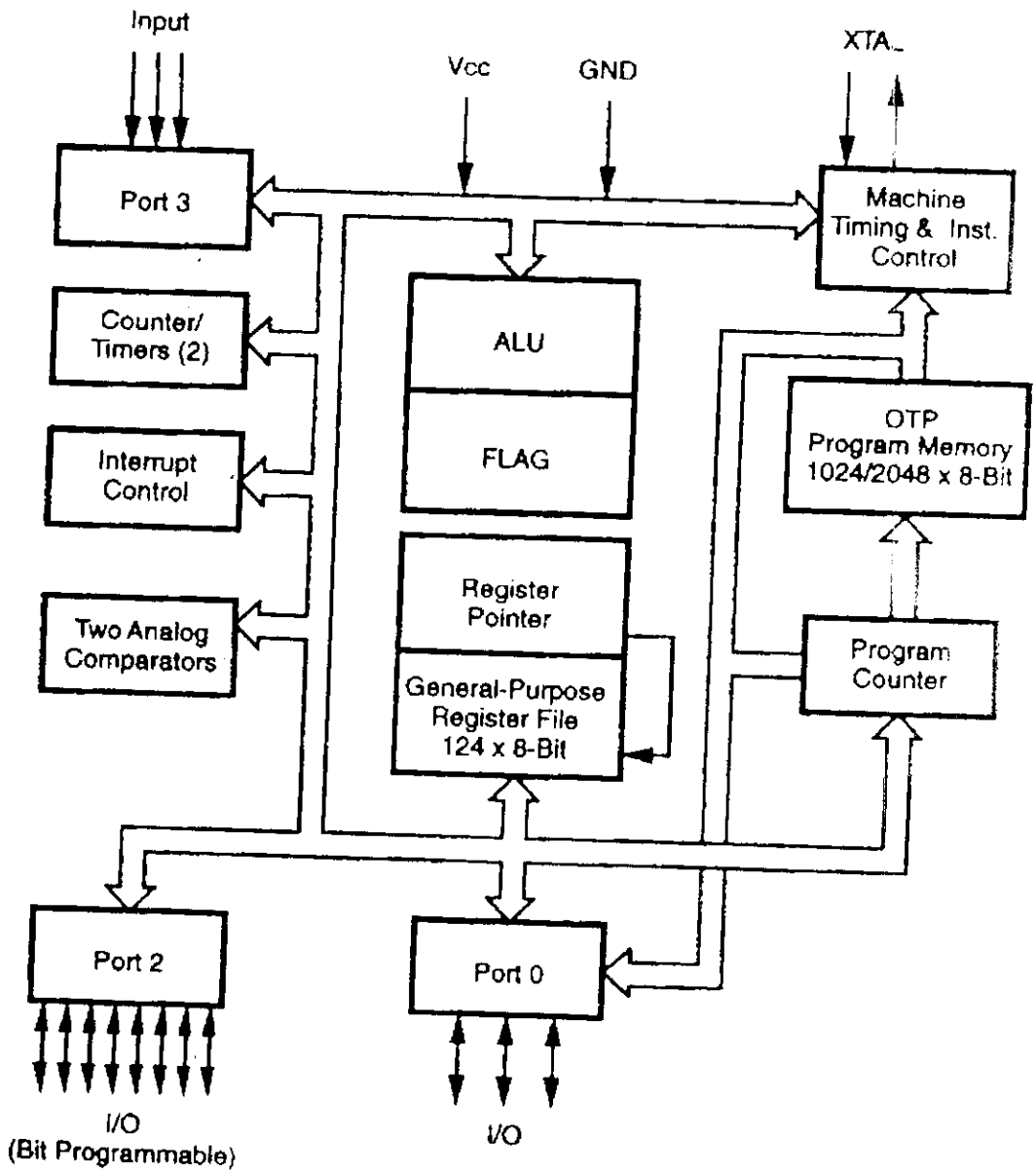
The Z86E04 microcontrollers introduce a new level of sophistication to single chip architecture. The Z86E04 is a member of the Z8 single chip microcontroller family with 1K bytes of one-time PROM . The device is housed in an 18-Pin DIP, and is manufactured in CMOS technology. The devices allow easy software devlopment and debug, prototyping and small production runs not economically desirable with a masked ROM version.

The Z86E04 have a flexible I/O scheme, an efficient register and address space structure. Also, they have a number of ancillary features that are usefull in many consumer, industrial and commercial appliations.

For applications which demand powerful I/O capabilities, theZ86E04 provide 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing and status signals.

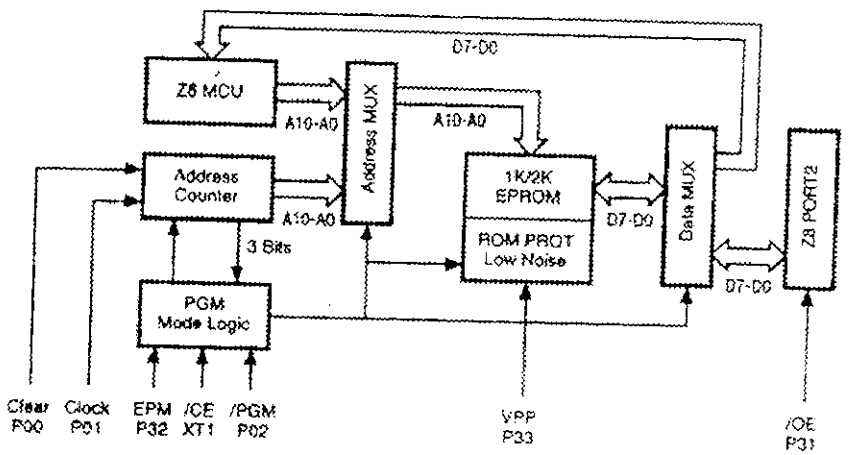
These are two basic address spaces available to support this wide range of configurations; program memory and 124 bytes of general-purpose registers.

The Z86E04 each offer programmable EPROM protect and programmable Low Noise. When the part is programmed for EPROm protect, the low Noise feature will automatically be enabled. When programmed for low noise, the EPROM protect feature is optional.



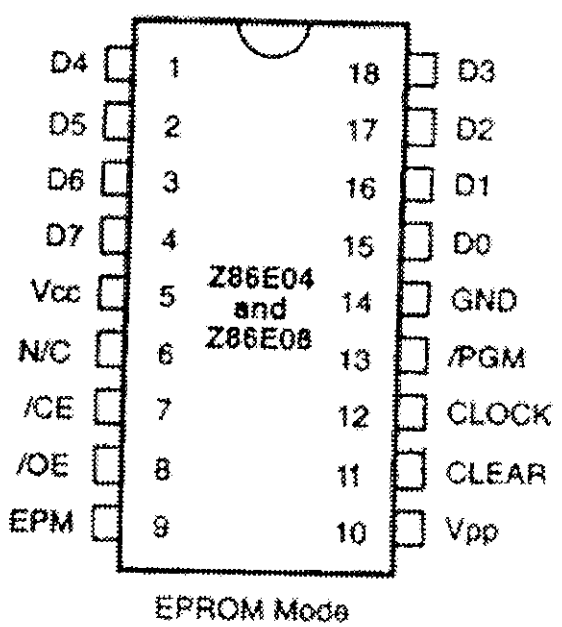
Functional Block Diagram

Fig. 3



EPROM MODE Block Diagram

Fig. 4



EPROM MODE Pin Configuration

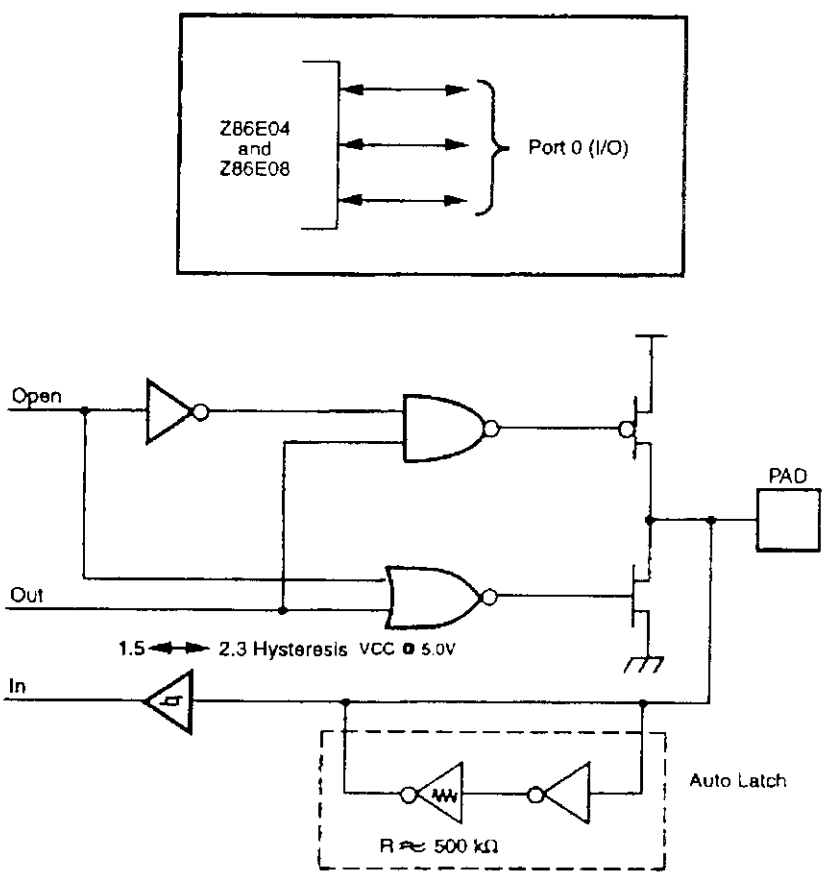
Fig. 5

To understand the program from copying with real-time tasks such as counting/timing and I/O data communications, the Z86E04 offers two on-chip counter/timers with a large number of user selectable modes.

PORTS

PORT 0, P02-P00

Port 0 is a 3-bit bi-directional,Schmitt triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be an input or output.



PORT 0 Configuration

Fig. 6

PORT 2, P27-P20

Port 2 is an 8-bit bidirectional, Schmitt triggered CMOS compatible I/O port. These eight I/O lines can be configured under software control to be input or output, independently. Bits programmed as outputs can be globally programmed as either Push-Pull or Open Drain.

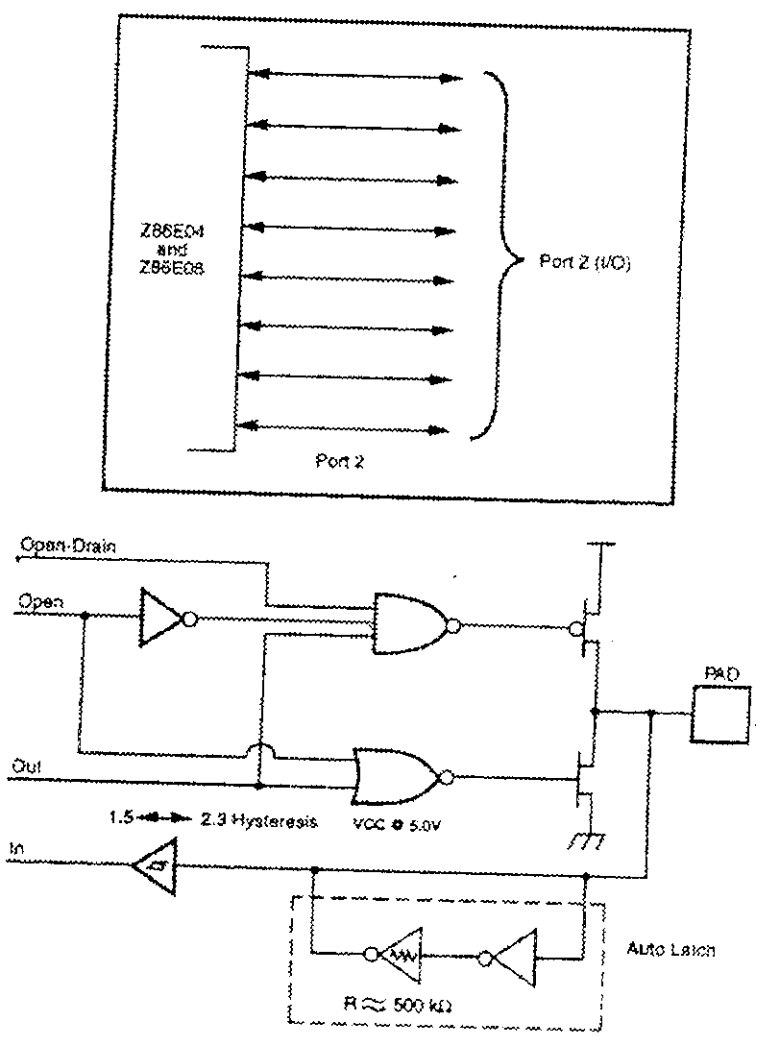
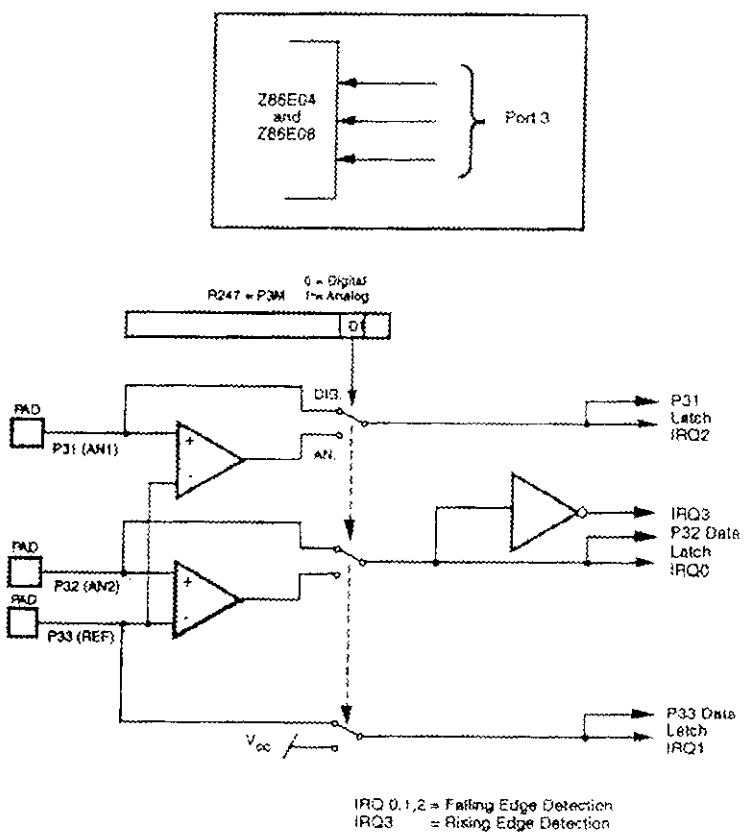


Figure 7. Port 2 Configuration

Fig. 7

PORT 3, P33-P31

Port 3 is a 3-bit CMOS compatible port with three fixed input lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal.



PORT 3 Configuration

Fig. 8

COMPARATOR INPUTS

Two analog comparators are added to input of port3,P31 and P32 for interface flexibility. The Comparator reference voltage P3 is common to both comparators.

Typical applications for the on-board comparators;Zero crossing detector, A/D convertor, voltage scaling and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparator.

The dual comparator features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4V when the Vcc is 5V; the power supply and common mode rejection ratios are 90dB and 60dB respectively.

PROGRAM MEMORY

The Z86E04 addresses upto 1Kbytes of the internal program memory. The first12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1024 are on-chip one time programmable ROM.

REGISTER FILE

The Register file consists of three I/O port registers, 124 general-purpose registers and 14 control and status registers. General purpose registers occupy the 04H to 7FH address space. I/O

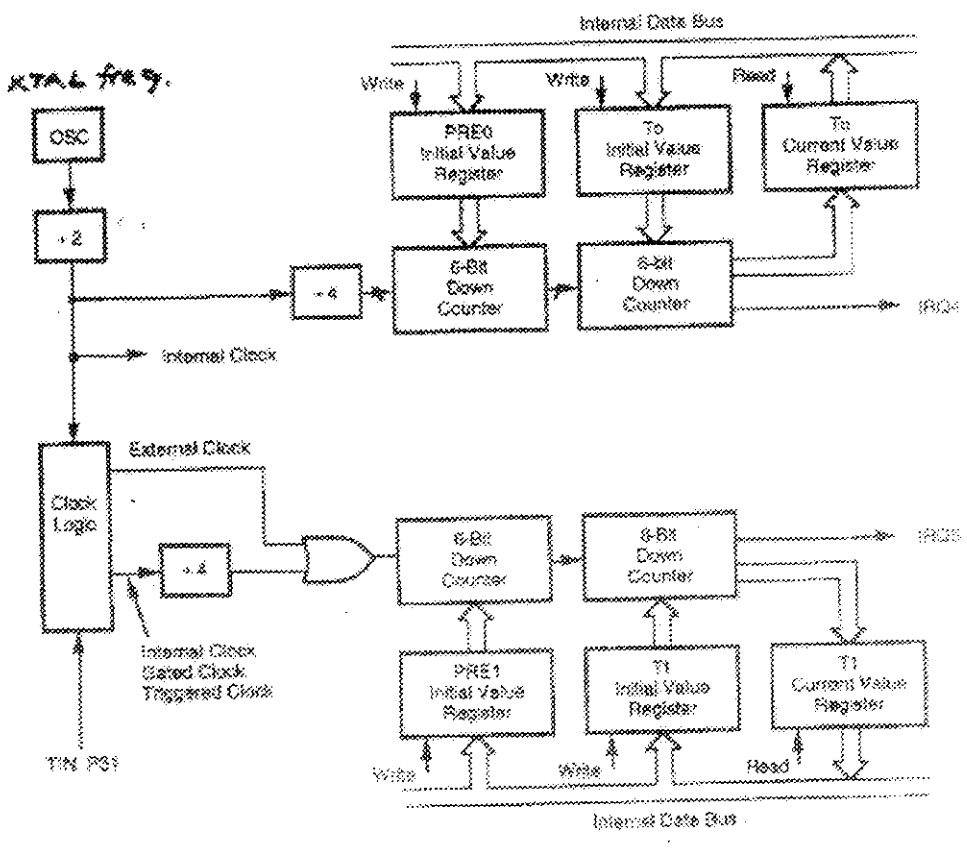
ports are mapped as per the existing CMOS Z8. The Z86E04 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the register Pointer. In the 4-bit mode the register file is divided into eight working register groups, each occupying 16 continuous locations. The register Pointer addresses the starting location of the active working-register group.

COUNTER/TIMER

There are two 8-bit programmable Counter/Timers, each divided by its own 6-bit programmable prescalar. The T1 prescalar is divided by internal or external clock source; however, the T0 can be divided by the internal clock source only.

The 6-bit prescalar divide the input frequency of the clock source by any integer number from 1 to 64. Each prescalar drives its counter, which decrements the value that has been loaded into the counter. When both counter and prescalar reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to stop, restart, continue or restart from the initial value. The counter's are also programmed to stop upon reaching zero or to automatically reload the initial value and continue counting.



COUNTER / TIMERS Block Diagram

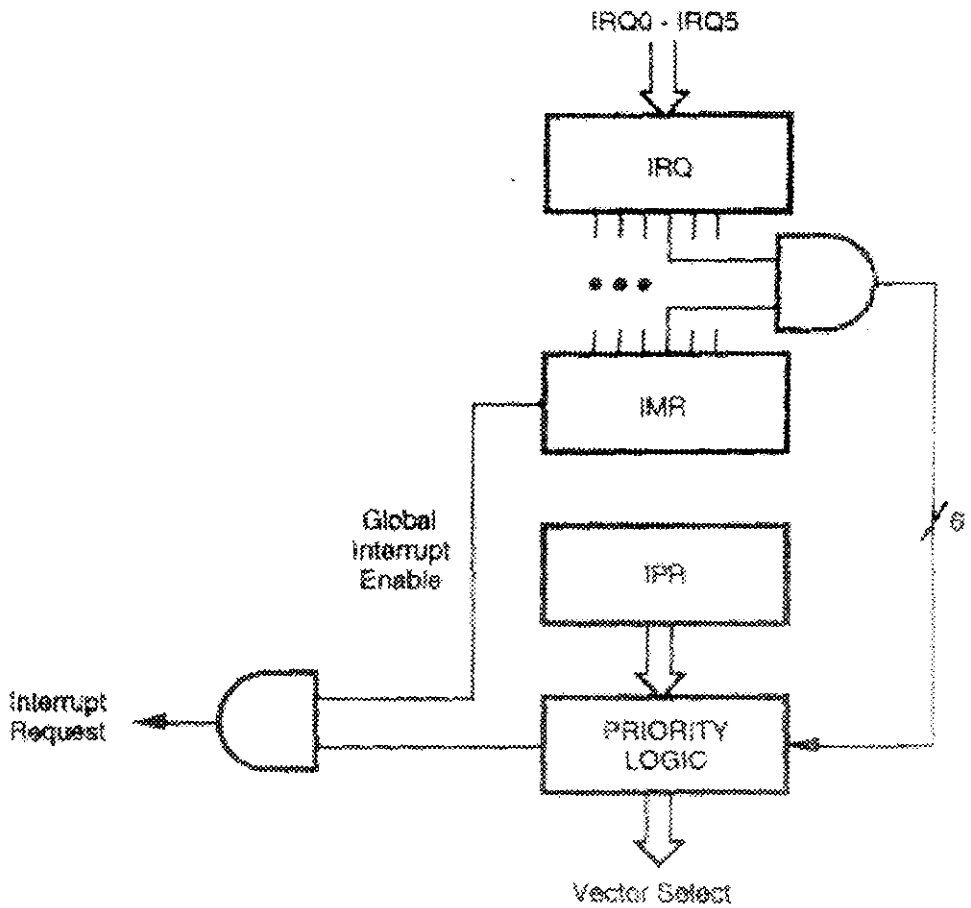
Fig. 9

INTERRUPTS

The Z86E04 has six interrupts from five different sources. These interrupts are maskable and prioritized . The sources are divided as follows: the falling edge of P31,P32,P33. The interrupt Mask register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.All Z86E04 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an interrupt Request is granted. This disables all subsequent interrupts, saves the program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service for the particular interrupt request.

To accomadate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.



INTERRUPT Block Diagram

Fig. 10

CLOCK

The Z86E04 on-chip oscillator has a high gain, parallel - resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source. The crystal should be AT cut, 8MHz max, with a series resistance of less than or equal to 100 ohms.

The Crystal should be connected accross XTAL1 and XTAL2, using the vendors crystal recommended capacitors from each pin directly to device grounded pin. The crystal capacitor loads should be connected to Vss, pin 14 to reduce Ground noise injection.

HALT MODE

Turns off the internal CPU clock but not the cryatal oscillation. The counter/timers and external interrupts remains active. The device is recovered by interrupts, eitherexternally or internally generated. An interrupt service routine, the program continues from the instruction after the HALT

STOP MODE

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10uA. The STOP mode is released by a RESET through a Stop-Mode recovery. A low input condition on P27 releases the STOP mode. Program execution begins at location 000C. However, when P27 is used to release the STOP mode, the I/O port mode registers are not

reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed. from glitching to an unknown state.

WATCH-DOG TIMER

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, cannot be stopped by the instruction. With the WDTinstruction, theWDT is refreshed when it is enabled with every 1Twdt period; otherwise, the Z86E04 resetsitself. The WDT instruction affects the flags accordingly; Z=0, S=0, V=0.

WDT = 5F (Hex)

LOW EMI EMISSION

The Z86E04 can be programmed to operate in a low EMI emission mode by means of a EPROM programmable bit option.Use of this feature results in

- Less than 1 mA consumed during HALT mode.
- All drivers slew rates reduced to 10 ns.
- Output drivers have resistances of 200 ohms.
- Oscillator divide-by-two circuitary eliminated.

The Z86E04 offers programmable ROM protect and programmable Low noise features. When programmed to Low noise, the ROM protect feature is Optional.

ROM PROTECT

ROM Protect fully protects the Z86E04 ROM code from being read externally. When the ROM protect is selected, the Z86E04 will disable the instructions LDC and LDCI. When the device is programmed for ROM protect, the low noise feature will automatically be enabled.

ALGORITHM :

1. Start

2.Initialise first byte address location

3.Let count = 0

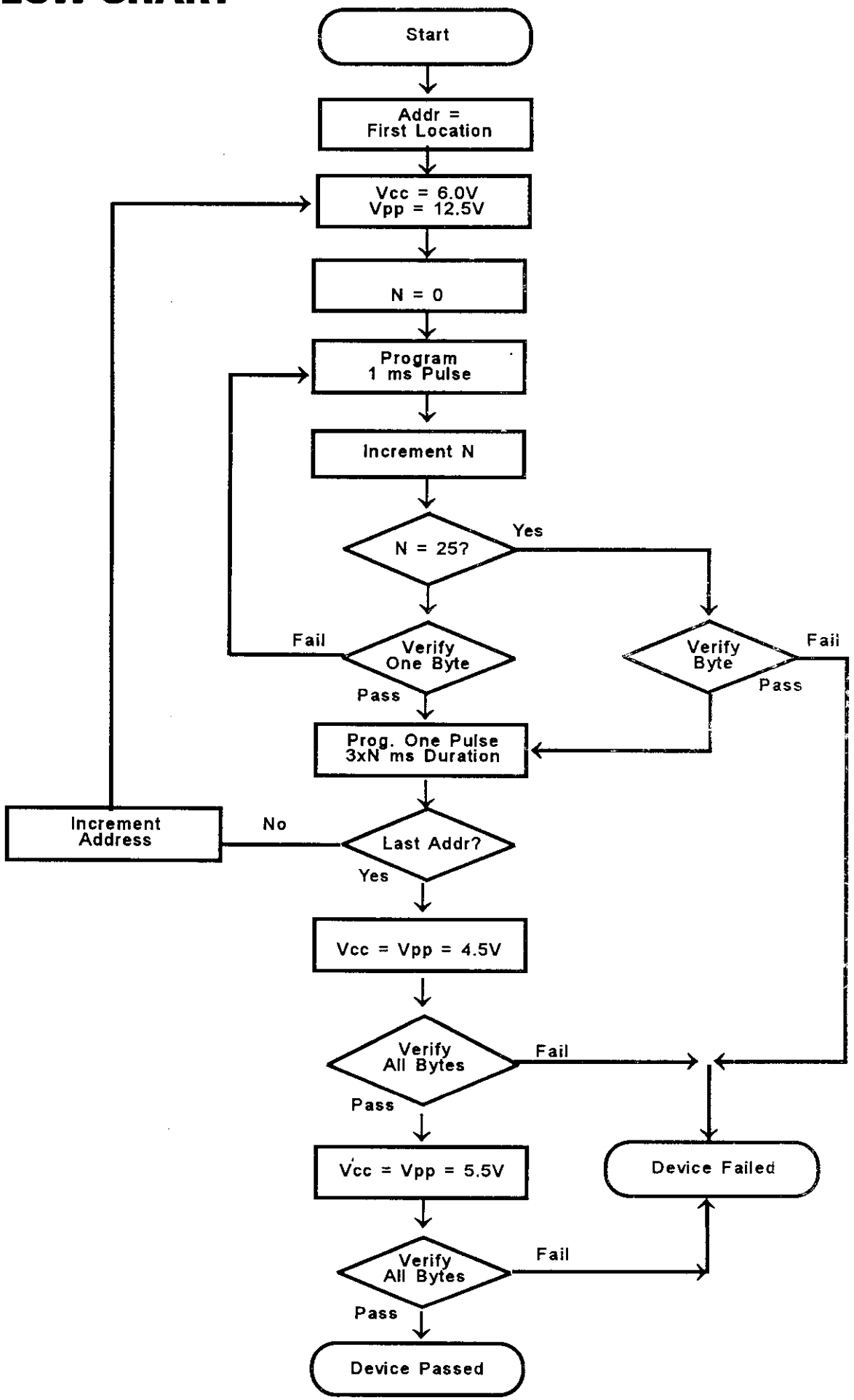
4. Apply delay

5. Increment count

6. Check for last address byte or else increment address

7. Verify all bytes to find device passed or failed.

FLOW CHART


Start
Addr = First Location
Vcc = 6.0V Vpp = 12.5V
N = 0
Program 1 ms Pulse
Increment N
N = 25?
Yes
Fail
Verify One Byte
Pass
Verify Byte
Fail
Pass
Prog. One Pulse 3xN ms Duration
Increment Address
No
Last Addr?
Yes
Vcc = Vpp = 4.5V
Verify All Bytes
Fail
Pass
Vcc = Vpp = 5.5V
Device Failed
Verify All Bytes
Fail
Pass
Device Passed

8. SOFTWARE

```
;          SOFTWARE FOR MOMENTARY INTERRUPTION OF
POWER TEST
;           STANDARD  DENSO
;           IC 86 E 04 ZILOG
;           CRYSTAL 8 MHZ
;          PROGRAMME  START
;*****************************************************************************

                    CPU   "Z8.tbl"
                HOF   "int8"


;Standard control registers:

        P0      :       EQU     00H
        P2      :       EQU     02H
        P3      :       EQU     03H
        TMR     :       EQU     0F1H
        T1      :       EQU     0F2H
        PRE1    :       EQU     0F3H
        T0      :       EQU     0F4H
        PRE0    :       EQU     0F5H
        P2M     :       EQU     0F6H
        P3M     :       EQU     0F7H
```

```
P01M :          EQU     0F8H
IPR  :          EQU     0F9H
IRQ  :          EQU     0FAH
IMR  :          EQU     0FBH
FLAGS:          EQU     0FCH
RP   :          EQU     0FDH
SPL  :          EQU     0FFH
SPH  :          EQU     0FEH
WDTMR:          EQU     00FH
SMR:            EQU     00BH
        bit0:   EQU1h
        bit1:   EQU2h
        bit2:   EQU4h
        bit3:   EQU8h
        bit4:   EQU10h
        bit5:   EQU20h
        bit6:   EQU40h
        bit7:   EQU80h

        nbit0:      EQU0feh
        nbit1:      EQU0fdh
        nbit2:      EQU0fbh
        nbit3:      EQU0f7h
        nbit4:      EQU0efh
        nbit5:      EQU0dfh
        nbit6:      EQU0bfh
        nbit7:      EQU7fh
```

```
position1 :     EQU01h
position2 :     EQU02h
position3 :     EQU03h

running_bit     :     EQUbit0
test_prog_bit   :     EQUbit0
test_comp_bit   :     EQUbit1

;General purpose register equates-
ctr                   :       equ  4
addr_ctr              :       equ  5
COUNT                 :       equ  6
POSITION              :       equ  7
START_DEBOUNCER:      equ  8
RESET_DEBOUNCER:      equ  9
TIMER                 :       equ  10
TIMER_10              :       equ  11
FLAG1:                        equ  12
CYCLE_COUNT:          equ  13
;equate interrupt vectors

        ORG  0
        DWM     start
        ORG  2
        DWM     start
        ORG  4
        DWM  start
```

```
                ORG  6
                DWM     start

                ORG  8
                DWM     t0_isr          ;dis_int

                ORG  10
                DWM     start           ;timer interrupt T1

                ORG      12

                start:

                    nop

                    nop

                    nop

                    srp  #0f0h

                    ldr  spl-240 , #070h

                    ldr  sph-240, #0

                    call initialize

                    call init_ram

                start1:

                    wdt

                    call switch_check

                    jp   start1

initialize:

    ldr   p3m-240 , #00000001b

    ldr   p2m-240 , #00000000b

    ldr   p01m-240 , #00000100b

    ldr   tmr-240 , #00000011b          ;2ch

    ldr   t0-240 , #250

    ldr   pre0-240 , #00000101b         ;prescaler 1      - 20

;   ldr   ipr-240 , #00100111b
```

```
        ldr   imr-240 , #00010000b
        ldr   irq-240 , #00000000b
        srp   #0
        ret
init_ram:
        wdt
        ldr   ctr , # 60
        ldr   addr_ctr , # 0
loop20:
        ld    4 ( rctr ) , raddr_ctr
        djnzr  ctr , loop20
        clr   FLAG1
        clr   TIMER
        clr   TIMER_10
        clr   CYCLE_COUNT
        ld    p2, #0
        ld    p0, #0
        ld    START_DEBOUNCER, #10
        ld    RESET_DEBOUNCER, #10
        and   FLAG1, #nbit0              ;running_bit
        ret
switch_check:
        tm    FLAG1, #running_bit
        jr    nz, switch_check_ret
        tm    p3, #bit1
        jr    z, switch_check_ret
        dec   START_DEBOUNCER
        jr    nz, switch_check_ret
```

```
        ei
        or    imr, #90h
        ld    POSITION, #position1
        or    FLAG1, #running_bit
        or    p0, #test_prog_bit
        and   p0, #nbit1                ;clr  test_comp_bit
        ld    COUNT,#3
        ld    p2, #0ffh
        ld    START_DEBOUNCER, #10
        ret
switch_check_ret:
        tm    p3, #bit2
        jr    z, switch_check_ret1
        dec   RESET_DEBOUNCER
        jr    nz, switch_check_ret1
        ld    p2, #0
        di
        clr   CYCLE_COUNT
        and   p0, #nbit1                ;clr  test_comp_bit
        and   p0, #nbit0                ;test_prog_bit
        and   FLAG1, #nbit0             ;running_bit
        ld    RESET_DEBOUNCER, #10
switch_check_ret1:
        ret

t0_isr:
        inc   TIMER
        cp    TIMER, #40
```

```
        jr    c, isr_ret
        clr   TIMER
;       xor   p0, #bit2
        inc   TIMER_10
        cp    POSITION, #position1
        jr    nz, isr1
        clr   TIMER
        dec   COUNT
        jr    nz, isr_ret
        and   p2, #nbit0
        ld    POSITION, #position2
        ld    COUNT, #6
        jp    isr_ret
isr1:
        cp    POSITION, #position2
        jr    nz, isr2
        rcf
        rlc   p2
        clr   TIMER
        dec   COUNT
        jr    nz, isr_ret
        ld    POSITION,#position3
        clr   TIMER_10
        jp    isr_ret
isr2:
        cp    TIMER_10, #1
        jr    ugt, isr3
```

```
        or    p0, #bit2
        jp    isr4
isr3:
        and   p0, #nbit2
isr4:
        cp    TIMER_10, #200
        jr    c, isr_ret
        clr   TIMER
        clr   TIMER_10
        ld    COUNT, #3
        ld    p2, #0ffh
        ld    POSITION, #position1
        inc   CYCLE_COUNT
        cp    CYCLE_COUNT, #100
        jr    c, isr_ret
        and   p0, #nbit0                ;test_prog_bit
        or    p0, #test_comp_bit
        clr   CYCLE_COUNT
        di
        and   imr, #6fh
        ld    p2, #0
        and   FLAG1, #nbit0             ;running_bit
isr_ret:
        iret
```

```
;SUPPLY VOLTAGE FLUCTUATION TEST
;STANDARD DENSO
;IC 86 E 04
;CRYSTAL OSC 8MHZ
        CPU   "Z8.tbl"
        HOF   "int8"

;Standard control registers:
P0      :       EQU     00H
P2      :       EQU     02H
P3      :       EQU     03H
TMR     :       EQU     0F1H
T1      :       EQU     0F2H
PRE1    :       EQU     0F3H
T0      :       EQU     0F4H
PRE0    :       EQU     0F5H
P2M     :       EQU     0F6H
P3M     :       EQU     0F7H
P01M    :       EQU     0F8H
IPR     :       EQU     0F9H
IRQ     :       EQU     0FAH
IMR     :       EQU     0FBH
FLAGS   :       EQU     0FCH
RP      :       EQU     0FDH
SPL     :       EQU     0FFH
SPH     :       EQU     0FEH
WDTMR   :       EQU     00FH
SMR     :       EQU     00BH
```

```
bit0:       EQU1h
bit1:       EQU2h
bit2:       EQU4h
bit3:       EQU8h
bit4:       EQU10h
bit5:       EQU20h
bit6:       EQU40h
bit7:       EQU80h

nbit0:          EQU0feh
nbit1:          EQU0fdh
nbit2:          EQU0fbh
nbit3:          EQU0f7h
nbit4:          EQU0efh
nbit5:          EQU0dfh
nbit6:          EQU0bfh
nbit7:          EQU7fh

position1:EQU01h
position2:EQU02h
position3:EQU03h
position4:equ  04h

running_bit:    EQUbit0
test_prog_bit: EQUbit0
test_comp_bit:      EQUbit1
```

```
;General purpose register equates-
ctr:        equ  4
addr_ctr:   equ  5
COUNT:      equ  6
POSITION:   equ  7
START_DEBOUNCER:  equ  8
RESET_DEBOUNCER:  equ  9
TIMER:          equ  10
FLAG1:          equ  11
TIMER_16:       equ  12
TIMER1_16:      equ  13
CYCLE_COUNT:        equ  14

rr12:           equ  12

        ;equate interrupt vectors
        ORG  0
        DWM     start

        ORG  2
        DWM     start

        ORG  4
        DWM  start

        ORG  6
        DWM     start

        org  8
        DWM     t0_isr          ;dis_int

        ORG  10
        DWM     start           ;timer interrupt T1

        ORG      12
```

```
start:
        nop
        nop
        nop
        srp   #0f0h
        ldr   spl-240 , #070h
        ldr   sph-240, #0
        call  initialize
        call  init_ram
start1:
        wdt
        call  switch_check
        jp    start1


initialize:
        ldr   p3m-240 , #00000001b
        ldr   p2m-240 , #00000000b
        ldr   p01m-240 ,#00000100b
        ldr   tmr-240 , #00000011b
        ldr   t0-240 ,  #160
        ldr   pre0-240 ,#00000101b
        ldr   imr-240 , #00010000b
        ldr   irq-240 , #00000000b
        srp   #0
        ret
  init_ram:                        ;RAM CLEAR
        wdt
        ldr    ctr , # 60
        ldr    addr_ctr , # 0
```

```
loop20:
        ld      4 ( rctr ) , raddr_ctr
        djnzr   ctr , loop20
        clr     FLAG1
        clr     TIMER
        clr     TIMER_16
        clr     TIMER1_16
;       clr     CYCLE_COUNT
        ld      p2, #0
        ld      p0, #0
        ld      START_DEBOUNCER, #10
        ld      RESET_DEBOUNCER, #10
        and     FLAG1, #nbit0           :running_bit
        ret

switch_check:                           ;START SENSE
        tm      FLAG1, #running_bit
        jr      nz, switch_check_ret
        tm      p3, #bit1
        jr      z, switch_check_ret
        dec     START_DEBOUNCER         ; DELAY LOOP
        jr      nz, switch_check_ret
        ei
        or      imr, #90h
        ld      POSITION, #position1
        or      FLAG1, #running_bit
        or      p0, #test_prog_bit
```

```
        and  p0, #nbit1                 ;clr  test_comp_bit
        ld   COUNT,#5
;       ld   p2, #0ffh
        ld   p2, #01h
        ld   START_DEBOUNCER, #10
        ret
switch_check_ret:
        tm   p3, #bit2
        jr   z, switch_check_ret1
        dec  RESET_DEBOUNCER
        jr   nz, switch_check_ret1
        ld   p2, #0
        di
        clr  CYCLE_COUNT
        or   p0, #bit1              ;clr  test_comp_bit
        and  p0, #nbit0                 ;test_prog_bit
        and  FLAG1, #nbit0              ;running_bit
        ld   RESET_DEBOUNCER, #10
switch_check_ret1:
        ret

t0_isr:
        inc  TIMER
        cp   TIMER, #10
        jr   c, isr_ret
        clr  TIMER
        incw rr12       ;1.6ms
```

```
        cp   POSITION, #position1
        jr   nz, isr1
        scf
        rlc  p2
        dec  COUNT
        jr   nz, isr_ret
        ld   POSITION, #position2
;       ld   COUNT, #6
        clr  TIMER_16
        clr  TIMER1_16
        jp   isr_ret
isr1:
        cp   POSITION, #position2
        jr   nz, isr2
        cp   TIMER_16, #1h
        jr   c, isr_ret
        cp   TIMER1_16, #0eeh
        jr   c, isr_ret
        rcf
        rlc  p2
        ld   POSITION,#position3
        clr  TIMER_16
        clr  TIMER1_16
        ld   COUNT, #5
        jp   isr_ret
isr2:
        cp   POSITION, #position3
        jr   nz, isr5
        cp   TIMER1_16, #21
        jr   c, isr_ret
        rcf
```

```
        rlc   p2
        clr   TIMER_16
        clr   TIMER1_16
        dec   COUNT
        jr    nz, isr_ret
        ld    POSITION, #position4
        jr    nz, isr_ret
isr5:
        cp    TIMER_16, #2h
        jr    c, isr_ret
        cp    TIMER1_16, #71h
        jr    c, isr_ret
        clr   TIMER
        clr   TIMER_16
        clr   TIMER1_16
        ld    COUNT, #5
;       ld    p2, #0ffh
        scf
        rlc   p2
        ld    POSITION, #position1
;       inc   CYCLE_COUNT
;       cp    CYCLE_COUNT, #100
;       jr    c, isr_ret
;       and   p0, #nbit0              ;test_prog_bit
;       or    p0, #test_comp_bit
;       clr   CYCLE_COUNT
;       di
;       and   imr, #6fh
;       ld    p2, #0
        and   FLAG1, #nbit0           ;running_bit
isr_ret:
        iret
```

9. FUNCTION GENERATOR

FEATURES

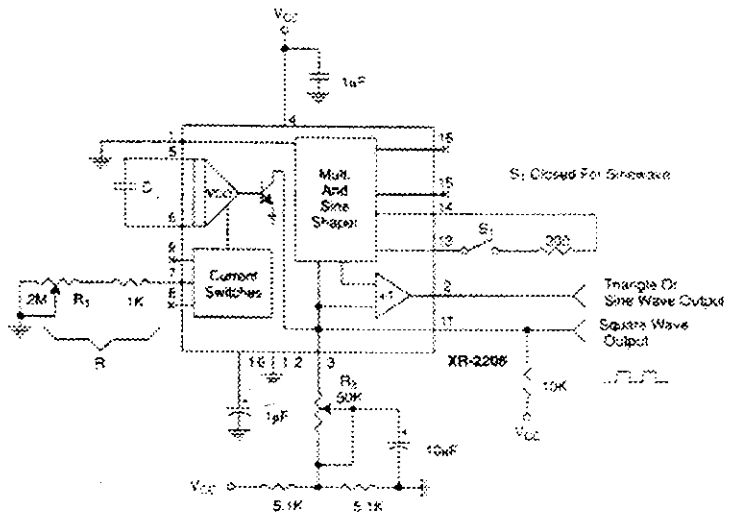
- Low- sine wave Distortion
- Excellent Temperature Stability
- Wide Sweep Range
- Low-Supply Sensitivity
- Linear Amplitude Modulation
- TTL compatible FSK Controls
- Wide Supply Range
- Adjustable Duty Cycle

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

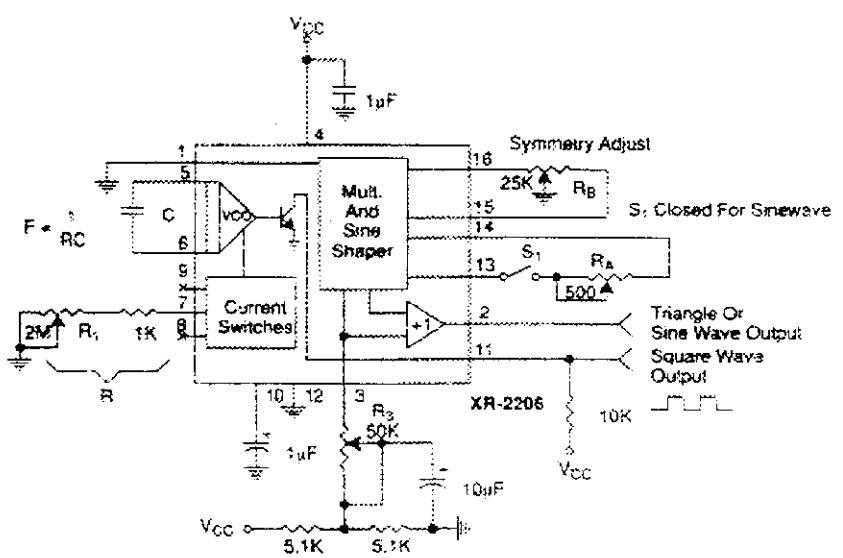
CIRCUIT FOR SINEWAVE GENERATIONA

Temperature.



Without External Adjustment

Fig. 12



With Minimum Harmonic Distortion

Fig. 13

10. VOLTAGE REGULATORS

3-TERMINAL POSITIVE REGULATORS (7805)

FEATURES

- Output voltage tolerences of =5%
- Output current of 100mA
- Internal thermal overload protection
- Internal Shortcircuit current limit

GENERAL DESCRIPTION

The LM7805, three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a Zener diode/ resistor combination replacement, the LM7805 usually results in an effective output impedence improvement of two orders of magnitude and lower quiescent current. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM7805 to be used in logic systems, instrumentation, HiFi and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

With adequate Heat sinking the regulator can deliver 100mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transis-

11. FABRICATION

The Automotive Voltage Variation Tests that comprises of the three voltage waveform generating circuits (PCBs) are placed inside a single setup. The whole test equipment consists of five blocks namely

- CRO - 10MHz Dual Scope Oscilloscope.
- Momentary Interruption of Power Test Block
- Supply Voltage Flutuation Test I Block
- Supply Voltage Flutuation Test II Block
- Voltage and Current Measuring Block

The three Voltage waveform generating circuits, generates their respective Voltage waveforms and can be viewed by a CRO placed at the top of the equipment. The Lower part of the equipment has a Voltmeter and Ammeter to detect for any shortcircuit , so that it could be rectified.

The three Voltage blocks are facilated with

- Test ON/OFF Switch
- Output Signal Knobs
- Start Button
- Stop Button
- Test on Process Indication
- Test Completed Indication.

12. ADVANTAGES

ADVANTAGE OF USING ELECTRONICS

- Low Cost
- High Reliability
- Improvement in Efficiency
- Accuracy
- High Quality
- Less Complexity

ADVANTAGE OF AUTOMOTIVE VOLTAGE VARIATION TESTS :

- Used to check for any Malfunctioning of the electronic Instrument against possible variation in battery voltage.
- Used to check for possible Fluctuation in supply voltage; including ripple voltage to be output from the generator.
- Used to check for possible Fluctuation in supply voltage at Startup of the Starter.

13. CONCLUSION

Our Project " AUTOMOTIVE VOLTAGE VARIATION TESTS" is designed for use in all vehicle testing. The Automotive Voltage Variation test equipment is a device suitable for International Standards. The value of the Voltage levels in the waveform are quite accurate. The Automotive voltage variation Tests equipment is designed in such a way that facilities available at present can be expanded.

This Project can be expended by including all the electrical loads like horns motors etc., and their Voltage and Current level can be monitored from the Volt meter and Ammeter fitted below and can be tested. Further A PC can be attached so that the waveform can be stored and printed out.

14. BIBLIOGRAPHY

1. ZILOG MICROCONTROLLER DATA BOOK

2. LINEAR IC DATA BOOK - NATIONAL SEMICONDUCTOR

3. AUTOMOTIVE MECHANICS - JOSEPH HEITNER

4. EXAR DATA BOOK

5. NATIONAL SEMICONDUCTOR DATA BOOK

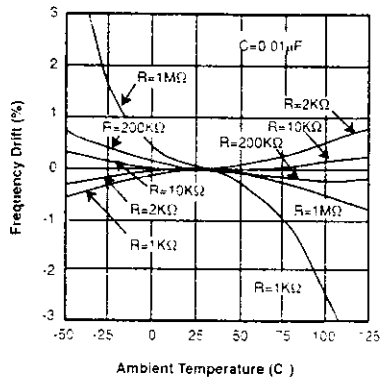


Figure 9. Frequency Drift versus Temperature.

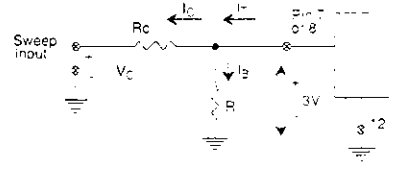


Figure 10. Circuit Connection for Frequency Sweep.

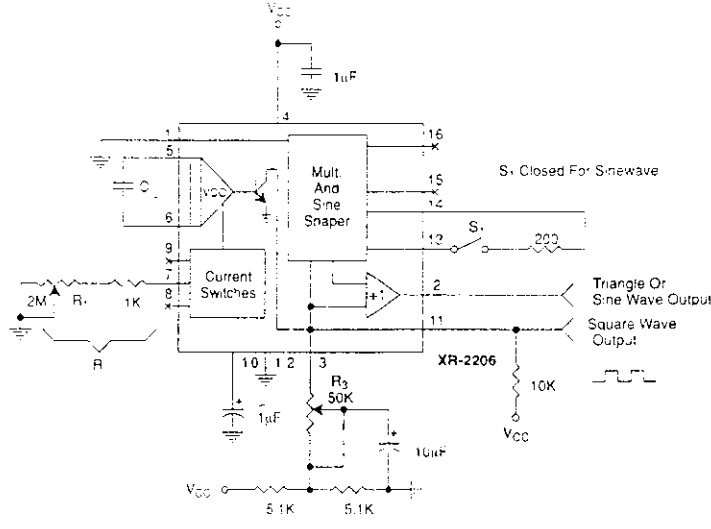


Figure 11. Circuit for Sine Wave Generation without External Adjustment.
(See *Figure 3* for Choice of R_3)

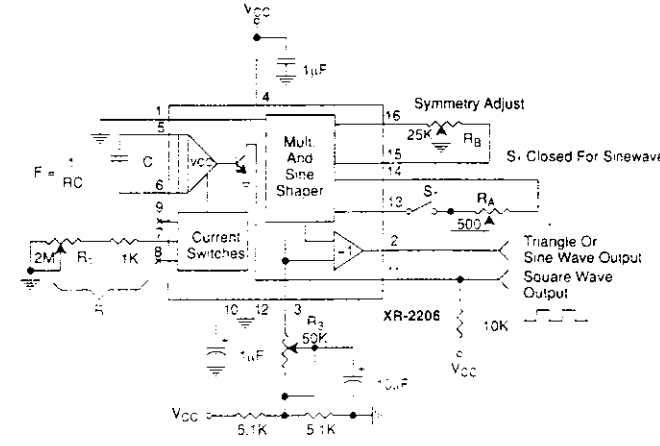


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion.
(R_3 Determines Output Swing - See *Figure 3*)

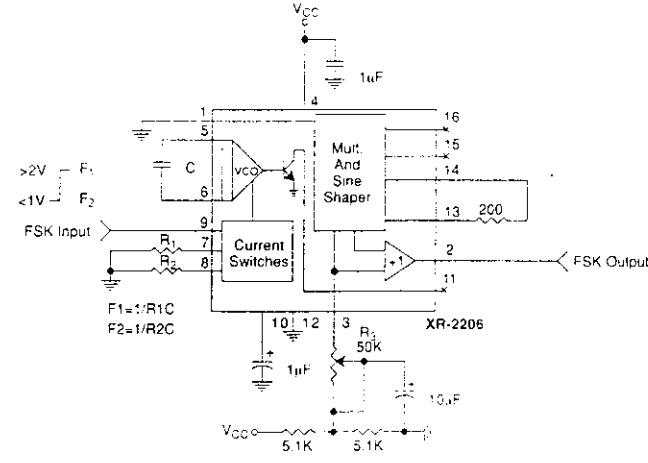


Figure 13. Sinusoidal FSK Generator

National Semiconductor

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

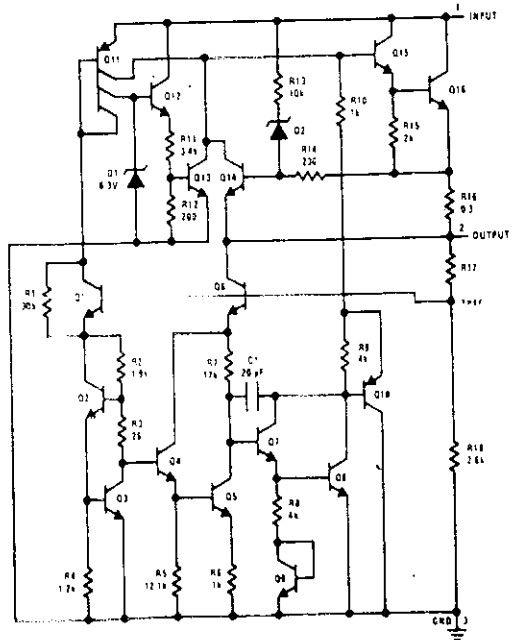
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

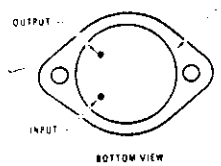
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams

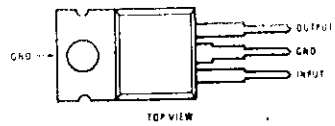


Metal Can Package
TO-3 (K)
Aluminum



Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

Plastic Package
TO-220 (T)



Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

Absolute Maximum Ratings

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	125°C ✓
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ T_J ≤ 125°C unless otherwise noted.

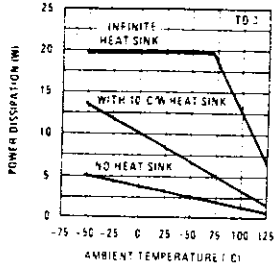
OUTPUT VOLTAGE			5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			UN
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C, 5 mA ≤ I_O ≤ 1A	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}	4.75 (7 ≤ V_{IN} ≤ 20)		5.25	11.4 (14.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (17.5 ≤ V_{IN} ≤ 30)		15.75	
ΔV_O	Line Regulation	I_O = 500 mA, T_J = 25°C, ΔV_{IN}		3	50		4	120		4	150	
			(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			
		I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, ΔV_{IN}			50			120			150	
			(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			
		I_O ≤ 1A, T_J = 25°C, ΔV_{IN}			50			120			150	
			(7.3 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			
		I_O ≤ 1A, 0°C ≤ T_J ≤ +125°C, ΔV_{IN}			25			60			75	
			(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			
V_O	Load Regulation	T_J = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	
		250 mA ≤ I_O ≤ 750 mA			25			60			75	
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_J ≤ +125°C			50			120			150	
	Quiescent Current	I_O ≤ 1A, T_J = 25°C			8			8			8	
		0°C ≤ T_J ≤ +125°C			8.5			8.5			8.5	
		5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5	
	Quiescent Current Change	T_J = 25°C, I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}			1.0			1.0			1.0	
			(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			
		I_O ≤ 500 mA, 0°C ≤ T_J ≤ +125°C, V_{MIN} ≤ V_{IN} ≤ V_{MAX}			1.0			1.0			1.0	
			(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			
	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		
$\frac{V_{IN}}{V_{OUT}}$	Ripple Rejection	f = 120 Hz, I_O ≤ 1A, T_J = 25°C or I_O ≤ 500 mA, 0°C ≤ T_J ≤ +125°C	62	80		55	72		54	70		
			62			55			54			
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		2.0			2.0			2.0		
	Output Resistance	f = 1 kHz		8			18			19		
	Short-Circuit Current	T_J = 25°C		2.1			1.5			1.2		
	Peak Output Current	T_J = 25°C		2.4			2.4			2.4		
	Average TC of V_{OUT}	0°C ≤ T_J ≤ +125°C, I_O = 5 mA		0.6			1.5			1.8		mV
	Input Voltage Required to Maintain Line Regulation	T_J = 25°C, I_O ≤ 1A	7.3			14.6			17.7			

TE 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of 220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

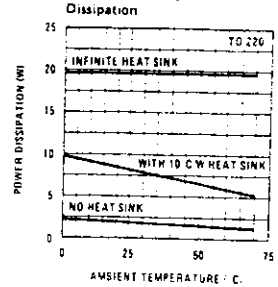
TE 2: All characteristics are measured with capacitor across the inut of 0.22 µF, and a capacitor across the output of 0.1 µF. All characteristics t noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes du nges in internal temperature must be taken into account separately.

Typical Performance Characteristics

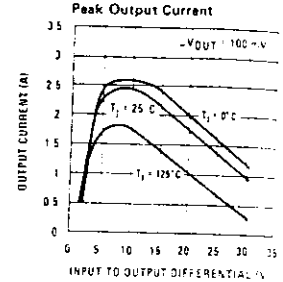
Maximum Average Power Dissipation



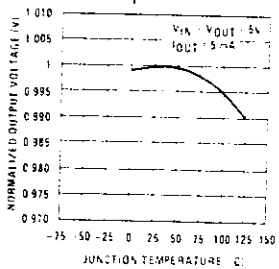
Maximum Average Power Dissipation



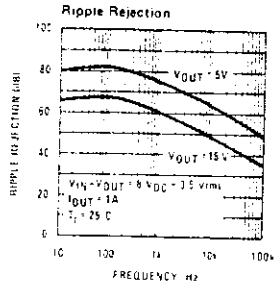
Peak Output Current



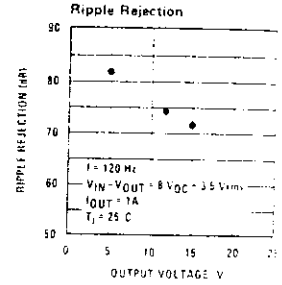
Output Voltage (Normalized to 1V at T_j = 25°C)



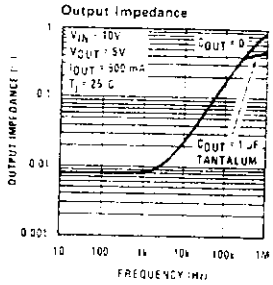
Ripple Rejection



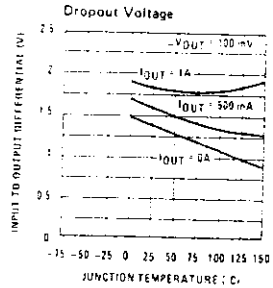
Ripple Rejection



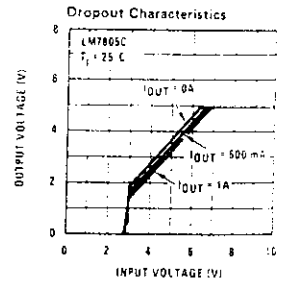
Output Impedance



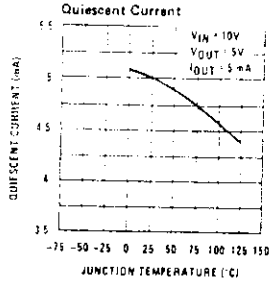
Dropout Voltage



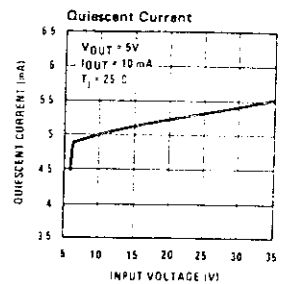
Dropout Characteristics



Quiescent Current



Quiescent Current



National Semiconductor

Voltage Regulators

LM78LXX Series 3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78LXX is available in the metal three lead TO-5 (H) and the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

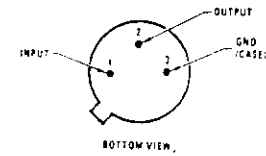
- Output voltage tolerances of ±5% (LM78LXXAC) and ±10% (LM78LXXC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 low profile packages

Voltage Range

LM78L05	5V
LM78L12	12V
LM78L15	15V

Connection Diagrams

Metal Can Package

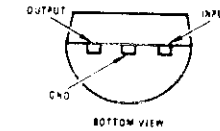


Order Numbers:

LM78L05ACH	LM78L05CH
LM78L12ACH	LM78L12CH
LM78L15ACH	LM78L15CH

See Package H03A

Plastic Package



Order Numbers:

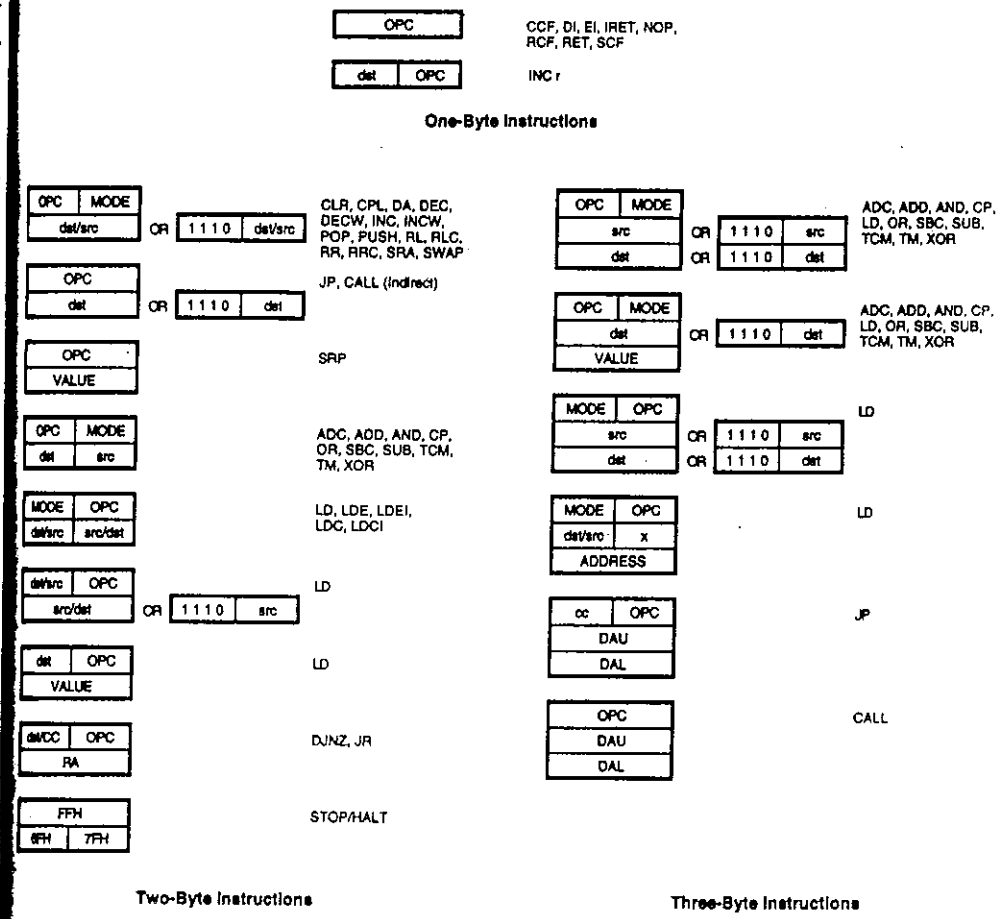
LM78L05ACZ	LM78L05CZ
LM78L12ACZ	LM78L12CZ
LM78L15ACZ	LM78L15CZ

See Package Z03A

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Unsigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C = 0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	F	Never true (Always False)	---

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol '←'. For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

refers to bit 7 of the destination operand.

4

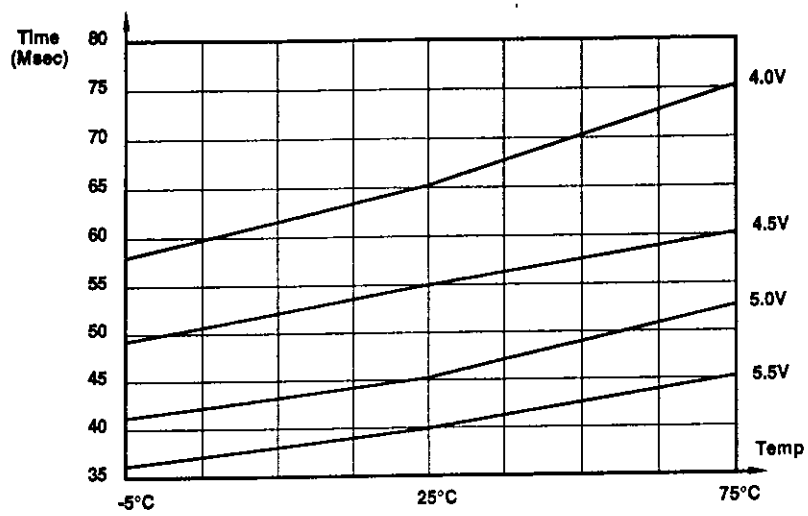


Figure 42. Typical POR Time Out Period vs Temperature

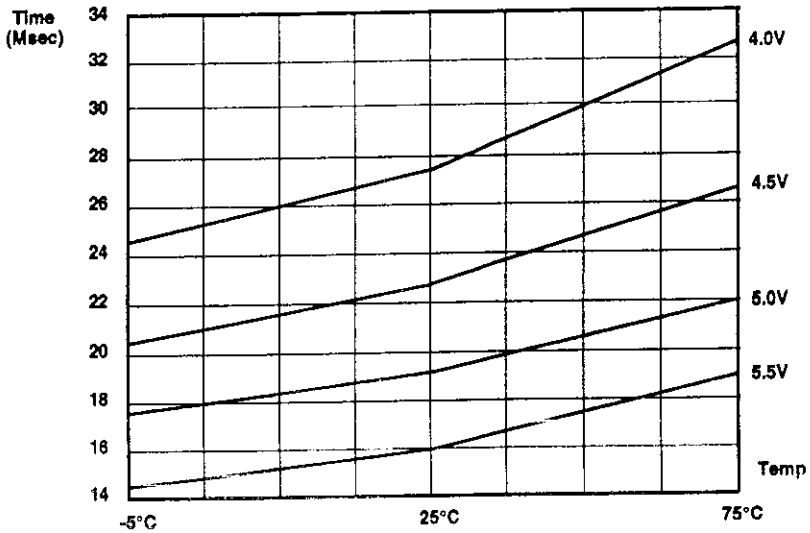


Figure 43. Typical WDT Time Out Period vs Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONTROL REGISTERS

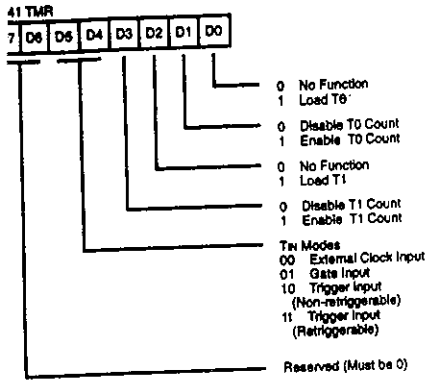


Figure 24. Timer Mode Register
(F1H: Read/Write)

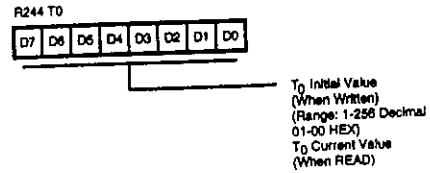


Figure 27. Counter/Timer 0 Register
(F4H: Read/Write)

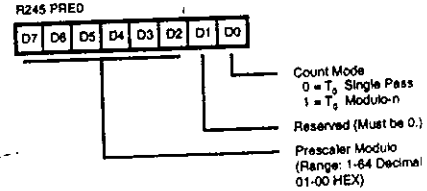


Figure 28. Prescaler 0 Register
(F5H: Write Only)

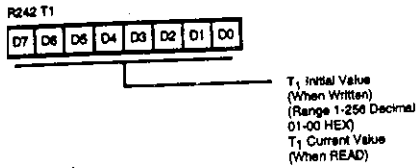


Figure 25. Counter Timer 1 Register
(F2H: Read/Write)

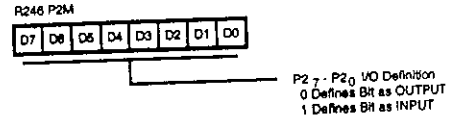


Figure 29. Port 2 Mode Register
(F6H: Write Only)

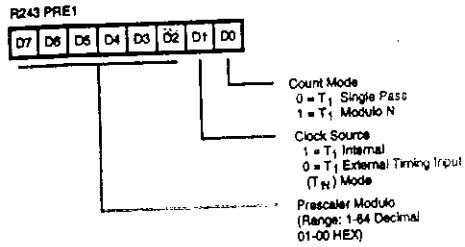


Figure 26. Prescaler 1 Register
(F3H: Write Only)

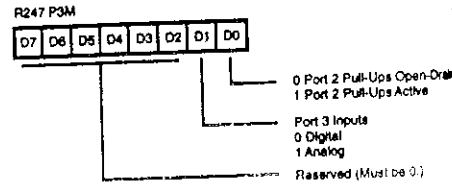


Figure 30. Port 3 Mode Register
(F7H: Write Only)

Z8 CONTROL REGISTERS (Continued)

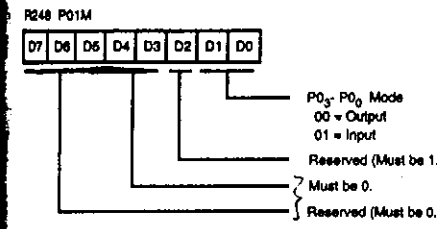


Figure 31. Port 0 and 1 Mode Register
(F8H: Write Only)

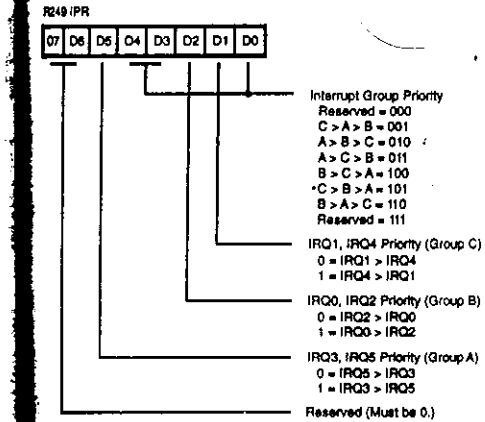


Figure 32. Interrupt Priority Register
(F9H: Write Only)

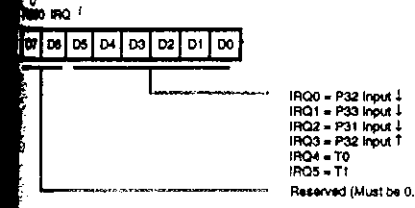


Figure 33. Interrupt Request Register
(FAH: Read/Write)

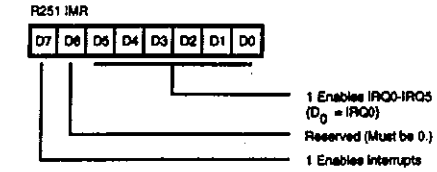


Figure 34. Interrupt Mask Register
(FBH: Read/Write)

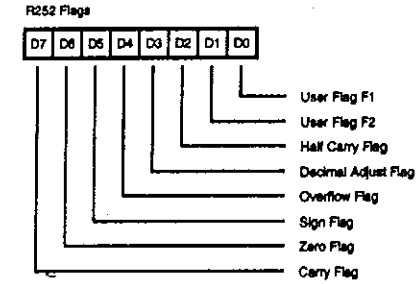


Figure 35. Flag Register
(FCH: Read/Write)

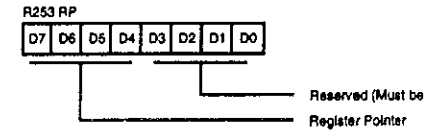


Figure 36. Register Pointer
(FDH: Read/Write)

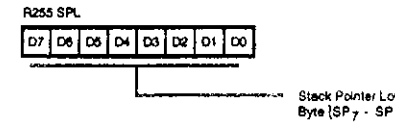


Figure 37. Stack Pointer
(FFH: Read/Write)

4

SPECIAL FUNCTIONS (Continued)

Table 4. Z86E04/08 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset.
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U		
FA	IRQ	U	0	0	0	0	0	0		IRQ3 is used for positive edge detection.
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0		
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E04/08 addresses up to 1K bytes of internal program memory (Figure 10). The first bytes of program memory are reserved for the interr bytes of program memory are reserved for the interru vectors. These locations contain six 16-bit vectors th correspond to the six available interrupts. Bytes 0-102 2048 are on-chip one-time programmable ROM.

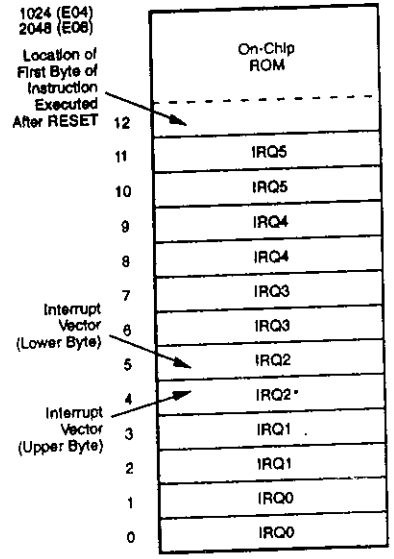


Figure 10. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 11). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The Z86E04/08 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 12) addresses the starting location of the active working-register group.

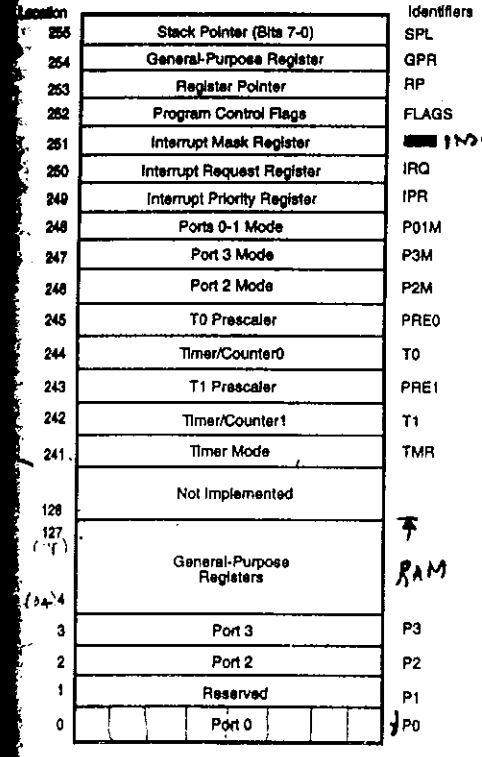


Figure 11. Register File

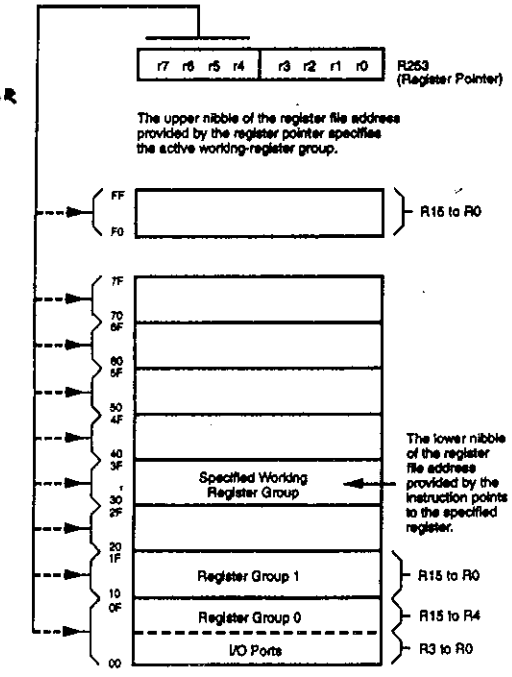


Figure 12. Register Pointer