COMPARATIVE ANALYSIS OF FAULT COVERAGE METHODS

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BONAFIDE CERTIFICATE

Certified that, this project report entitled "**COMPARATIVE ANALYSIS OF FAULT COVERAGE METHODS**" is the bonafide work of **Mrs.KEERTHANA.K.P [Reg.No:1020106010]** who carried out the project under my supervision. Certified further, that to the best of my knowledge the work reported herein does not form part of any other project or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this or any other candidate.

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The candidate with university Register no. 1020106010 is examined by us in the project viva-voce examination held on ……

INTERNAL EXAMINER **EXTERNAL EXAMINER**

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ABSTRACT

The testing is examining the product, to ensure the function and exhibits the properties and capabilities that it was define to process. It is an important factor in proving the successful outcome of the product. The testing is interrupted by faults if there is any malfunction. The faults that are causing increased the concern in the semiconductor industry in the recent decade at the higher rate such faults are the delay faults .Scan based application methods are used for finding the faults in the delay models. But some faults like transition delay faults are undetectable in scan based application method.

Fault coverage is a very important concept in VLSI testing. It is referred as the percentage of faults that can be detected during the test in any system. Different test may induce different fault set which will result in variation of fault coverage of the same circuit. The fault coverage usually refers to the efficiency of test. The main objective is to improve the fault coverage of transition delay faults.

The hazard based detection method is carried out for the ISCAS S_27 circuit. The circuit has been simulated for the fault free condition. For the same circuit fault has been injected and simulated for the broadside, functional broadside and skewed load test. The fault coverage has been calculated based on the faults detected. From the simulation it is inferred that the use of hazard-based detection conditions improves the delay fault coverage achievable for a circuit. A fault is detected if the value of a hazard is sampled. The circuit is designed using VHDL, and simulated using Model Sim 6.3g.

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LIST OF ABBREVIATIONS

ATPG	**-------**	**Automatic Test Pattern Generation**
ATE	**-------**	**Automatic Test Equipment**
CUT	**-------**	**Circuit Under Test**
CI	**-------**	**Control Input**
CO	**-------**	**Control Output**
D-ALG	**-------**	**D- Clark's Algorithm**
FF	**-------**	**Flip Flop**
ISCAS	**-------**	**International Symposium on Circuits and Systems**
LION	**-------**	**Line Information of Open Networks**
OP	**-------**	**Observation Points**
PODEM	**-------**	**Path Oriented Decision Making**
PR	**-------**	**Pseudorandom**
RPR	**-------**	**Random Pattern Resistant**
SFF	**-------**	**Scan Flip Flop**
ST0	**-------**	**Stuck at Zero**
ST1	**-------**	**Stuck at One**
TC	**-------**	**Test Control**

CHAPTER 1

INTRODUCTION

The presence of delay-inducing defects is causing increasing concern in the semiconductor industry today. To test for such delay-inducing defects, scan-based transition fault testing techniques are being implemented. There exist organized techniques to generate test patterns for the transition fault model. The principle goal of testing would thus be to check the manufactured product completely, making sure that it functions according to its requirements and detect malfunctions and defects in the product. We define a new type of detection conditions for delay faults, referred to as hazard-based detection conditions, to enhance the coverage of delay faults using the standard scan test application methods. Some delay faults, including irredundant faults, may be undetectable under the conventional detection conditions. These faults may be detectable under the hazard-based detection conditions. The use of hazard-based detection conditions thus improves the delay fault coverage achievable for a circuit.

The testing is important aspect in arriving the output of the process or processor. The testing process verifies the correctness of hardware. The testing is an important factor in providing the successful outcome of the product. The testing is done for finding the fault in the circuit. The reasons of testing are quality assurance, verification and validating the product before it goes in the market, defect free and user friendly, meets the requirements of the product. So in order to fulfill the above needs, testing is being carried out. The fault coverage is a method of correcting the faults in the circuit.

There are different types of testing available which can detect the faults in three different conditions objective of delay faults is to detect the timing defects and ensure that the design meets the desired performance specification. The growing need for delay testing is a result of advances in VLSI technology and the increase of the design speed. Testing delay faults is a complex problem. Testing delays in high speed circuit requires the availability of high speed testers. Estimating the delay fault coverage requires knowledge about the total no of faults and the number of faults detected by the given set .The testing method used here is the exhaustive method.

There are various testing methodologies in combinational and sequential circuits. In sequential circuits, enhanced scan and standard scan testing are performed. Enhanced scan testing, two bits are stored in memory elements instead of one bit. The design of such flip flop allows a pre-scan of any two-vector test. The two vectors are applied to the circuit in two consecutive clock cycles. The disadvantage of this method is high area overhead and long test application time.

Standard scan testing, generating test for delay faults for standard scan designs corresponds to a two line frame sequential circuit test generation in the first time line frame, all primary inputs and present state lines are fully controllable, where as in second time frame, only the primary inputs are fully controllable .Testing schemes of standard scan have also been processed . These techniques use functional broadside ,functional justification (also known as the broadside test) or scan shifting (also known as the SKEWED LOAD test), and. to obtain the second vector in functional justification the second vector is derived using the capture mode and represents the set of next state values obtained after the application of first vector.

1.1 GOAL OF THE PROJECT

The principle goal of testing would thus be to check the manufactured product completely. Making sure that it functions according to its requirements and detect malfunctions in the product. To enhance the coverage of delay faults using the standard scan test application methods the testing is done. The testing is carried out by the following method using the exhaustive test sets.

- Broad side tests
- Functional broadside tests
- Skewed-load tests.

The testing is carried out under the three types of testing mentioned above. The circuit used for the detection of fault is ISCAS-89 benchmark s27, LION circuit. By the hazard based detection condition the fault is identified, by the switching over from 0(zero) to 1(one) or 1(one) to (0) zero, and is proved as the best method of transition fault coverage than

the conventional method of fault coverage. By doing this way the transition fault delay is detected correctly, than the other methods. The circuit is designed using VHDL and simulated using Modelsim 6.3g. A fault is detected when an output value is different from the expected fault-free value under the second pattern of a test.

1.2 SOFTWARE USED

The circuits are designed using VHDL and simulated using Modelsim 6.3g.

1.3 ORGANIZATION OF THE REPORT

- **Chapter 2** Discusses the overview of the testing methods
- **Chapter 3** Discusses the existing methods.
- **Chapter 4** Discusses the proposed methods.
- **Chapter 5** Discusses the simulation results.
- **Chapter 6** Discusses the conclusion and the future work.

CHAPTER 2

OVERVIEW OF THE TESTING METHODS

The testing is important aspect in arriving the output of the process or processor. The testing process verifies the correctness of hardware. The testing is an important factor in providing the successful outcome of the product. Testing in its broadest sense means to examine a product and to ensure that it functions and exhibits the properties and capabilities that it was designed to possess. Main purpose of testing is to detect malfunctions in the product hardware and to locate their causes so that they may be eliminated. The testing is done for finding the fault in the circuit. The reasons of testing are:

- Quality Assurance
- Verification and validating the product before it goes in the market
- Defect free and user friendly
- Meets the requirements of the product.

So in order to fulfill the above needs, testing is being carried out. The fault coverage is a method of correcting the faults in the circuit .There are different types of testing available which can detect the faults in three different conditions objective of delay faults is to detect the timing defects and ensure that the design meets the desired performance specification. The growing need for delay testing is a result of advances in VLSI technology and the increase of the design speed. Testing delay faults is a complex problem. Testing delays in high speed circuit requires the availability of high speed testers. Estimating the delay fault coverage requires knowledge about the total no of faults and the number of faults detected by the given set .The testing method used here is the exhaustive method. The testing methods include three types, they are

- Broad side tests
- Functional broadside tests
- Skewed-load tests.

2.1 TESTING METHODS

There are different methods of tests available for various type of test generation method. Tests are categorized into off-chip, on-chip and also can be according to the test application methods. The test methods are the

- Exhaustive tests
- Pseudo exhaustive tests
- Pseudo random tests
- Deterministic tests

2.1.1 EXHAUSTIVE TESTS

A test pattern is a combination of the values applied on the primary inputs of the circuit under test. It is convincible to use all possible combinations and apply in the circuit. The exhaustive approach to testing has the advantage of being easy to generate and of yielding higher fault coverage. However, such a testing method is efficient only for purely combinational small circuits. This exhaustive testing is not applicable for sequential circuits. In exhaustive test, all 2n input combinations for an n-input CUT are applied during the test process. Exhaustive test does not have the problem of random pattern resistant faults, so it can get 100% stuck-at fault coverage. However, test time becomes too long with large number of inputs. Test time can be reduced by partitioning the primary inputs of the CUT into sub-groups and testing each sub circuit exhaustively. But the partitioning method is very difficult and the fault coverage is lower.

2.1.2 PSEUDO EXHAUSTIVE TESTS

This is an alternative to exhaustive test. The approach is to check the component of a circuit exhaustively without having to apply an exhaustive test on the circuit. This type of testing requires an efficient way of partitioning the circuit. It is considered as an approach to design in order to ease the testability. Another special case of testing known as verification testing. It is applicable to circuits where each primary output is a function of only a subset of primary inputs. The length of the test set used for the exhaustive test will be more than the pseudo exhaustive.

2.1.3 PSEUDORANDOM TESTS

Test pattern may also be generated in a random order. The cost of generating test is minimal. A fault simulator is needed is to grade the test and access the fault coverage. The advantage of random test is that it has been shown to detect the large percentage (85%) of stuck-at-faults. Consequently many commercial ATPG s use random testing as a first stage of test pattern generation and then apply heuristics to deal with the still undetected faults, which are called as the RPR. In purely random testing a test pattern may be generated more than once. However the PR test generation is more appropriate to ensure that there is no repetition of pattern.

Pseudorandom testing is popular due to the simplicity of the linear feedback shift registers (LFSRs) used as TPG to generate a sub-set of the 2n test patterns. Fault coverage is estimated by probabilistic methods. The number of random patterns to be applied is decided by the detection probability of the faults, Not all 2**n input combinat ions, Random patterns generated deterministically & repeatably, pattern with/without replacement, applicable to both combinational and sequential circuits. There are two methods available. They are,

- **Weighted** : Non-uniform distribution of 0's & 1's, improved fault coverage, using LFSR added with combinational circuits.
- **Adaptive** : Using intermediate results of fault simulation to modify 0's & 1's weights, more efficient, more hardware complexity.

2.1.4 DETERMINISTIC TESTS

Deterministic tests are fault oriented tests. In this case, patterns are generated targeting the specific fault model. Generating these patterns is NP-complete problem and required heuristics to speed up the process. In contrast to pseudorandom test, deterministic tests have to be generated off chip. category of testing techniques is based on deterministic test set embedding. In deterministic test, the circuit under test (CUT) is analyzed prior to testing to determine the appropriate test set to be applied. After the test set has been obtained, the test pattern generator is designed to generate the predetermined test set. The disadvantage of this strategy is that it can only be applied to circuits with small size or regular structures due to the high complexity.

The testing method used in this project is the exhaustive test method. Because the other methods of testing is not suitable for sequential circuits. And in the exhaustive test only the transition delay fault delay occur.

2.2 NEED FOR TESTING

The increased complexity of embedded systems and the reduced access to internal nodes has made it not only more difficult to diagnose and locate faulty components, but also the functions of embedded components may be difficult to measure. Creating testable designs is the key to developing complex hardware and/or software systems that function reliably throughout their operational life. Testability can be defined with respect to a fault. A fault is testable if there exists a well-specified procedure (e.g., test pattern generation, evaluation, and application) to expose it and the procedure is implementable with a reasonable cost using current technologies. Testability of the fault therefore represents the inverse of the cost in detecting the fault. A circuit is testable with respect to a fault set when each and every fault in this set is testable.

Design-for-testability techniques improve the controllability and observability of internal nodes, so that embedded functions can be tested. Two basic properties determine the testability of a node: controllability, which is a measure of the difficulty of setting internal circuit nodes to 0 or 1 by assigning values to primary inputs (PIs), and observability, which is a measure of the difficulty of propagating a node's value to a primary output (PO). A node is said to be testable if it is easily controlled and observed. For sequential circuits, some have added predictability, which represents the ability to obtain known output values in response to given input stimuli.

The factors affecting predictability include initializability, races, hazards, oscillations, etc. DFT techniques include analog test busses and scan methods. Testability can also be improved with BIST circuitry, where signal generators and analysis circuitry are implemented on chip. Without testability, design flaws may escape detection until a product is in the hands of users; equally, operational failures may prove difficult to detect and diagnose. In particular, path delay faults have become more common due to higher clock rates and higher process variability caused by shrinking geometries. Therefore, at-speed path delay testing is gaining importance. Delay fault testing requires the application of two test vectors.

The first test vector, referred to as the initialization vector, initializes the logic to a known state. The second vector, referred to as the activation vector, activates the targeted fault, causing a transition to be propagated along the path under test. It is well-known that at-speed application of test vector pairs to the primary inputs has low path delay fault coverage. However, improved fault coverage can be achieved by using scan chaining, which has already become the design-for-test (DFT) technique of choice for stuck-at fault testing.

2.3 DIFFICULTIES IN TESTING

- Shortage of I/O points.
- Signal distortions in interface connections.
- Noise disturbances.
- Uncertainties in input feeding.
- Uncertainties in output sensing. (Rejection of good parts reduces apparent yield.)
- Difficulty in synchronizing test objects timing with tester timing.
- High costs for test equipment, test generation and execution.
- Large volume of data to be processed

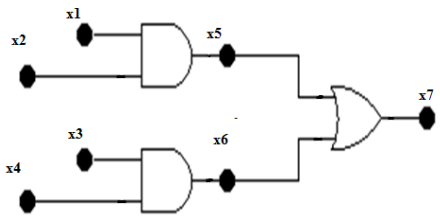

Fig 2.1 Circuit For Illustration

2.4 KINDS OF FAULTS

In the above fig 2.1, the faults are

- Single faults
- Multiple faults.

No of single fault locations : 7

No of single faults : 2 * 7 = 14

No of double fault combinations. : $2 * 2 * {}^{7}C_{2} = 84$

Fault combinations are not unique. A test for SA0 at x1 also covers SA0 at x5 and x7.

2.5 FAULT EQUIVALENCES

- One or more inputs to an OR gate at SA1 is equivalent to an OR gate whose output is at SA1.
- One or more inputs to an AND gate at SA0 is equivalent to an AND gate whose output is at SA0.
- All inputs to an OR gate at SA0 is equivalent to an OR gate whose output is at SA0.
- All inputs to an AND gate at SA1 is equivalent to an AND gate whose output is at SA1.

Thus any gate output fault has an equivalent single stuck fault or multiple stuck faults.

2.6 TRANSITION DELAY FAULT

The common problem faced by the semi-conductor industry is that designs that function properly at low clock frequencies fail at rated speed. The need for delay testing arose from this problem. The objective of delay testing is to detect and ensure that the design meets the desired performance specifications. A delay fault can be modelled using either of the five delay fault models namely transition fault model, gate delay fault model, line delay fault model, path delay fault model and segment delay fault model.

It is assumed that in the nominal design each gate has a given fall (rise) delay from each input to the output pin. The interconnects are assumed to have rise (fall) delays. Since the gate pin-to-pin delays and the interconnect delays can be combined together, the term “gate delay” is used to denote this sum. Transition, gate and line delay models are used for representing delay defects lumped at gates while the path and segment delay models address defects that are distributed over several gates.

2.7 FAULT MODELS

Two popular structural fault models are prevalent in the industry today and they are the stuck-at fault model and the transition fault model. Stuck-at faults affect the logical behaviour of the system, while transition faults affect the timing/temporal behaviour of the system. An additional fault model being used is the path-delay fault model, which is also based on the timing behaviour of the system, but cumulative delays along paths are considered, in lieu of delays at each net as in the transition fault model. In this project, we deal with structural faults alone, and mainly concentrate on transition faults.

2.7.1 STUCK-AT FAULT MODEL

The main assumption made by the stuck-at fault model is that the components of a circuit are fault-free and only their interconnections are defective. However, it has been shown that stuck-at fault tests are effective in capturing a wide range of defects on manufactured chips. This model represents faults caused by opens, shorts with power or ground, and internal faults in the components driving signals that keep them stuck-at a logic value. To test for stuck-at faults, two steps are involved.

The first step is to generate a test vector that excites the fault and the next step is to propagate the faulty effect to a primary output or a scan flip-flop. ATPG tools are typically used to generate the test vectors. The stuck-at fault model is being used virtually everywhere in the industry to screen defects caused by stuck-at faults. It is relatively easy to generate patterns for stuck-at faults and pattern volume is also comparatively low

2.7.2 TRANSITION FAULT MODEL

The transition fault model is similar to the stuck-at fault model in many respects. The effect of a transition fault at any point P in a circuit is that any transition at P will not reach a scan flip-flop or a primary output within the stipulated clock period of the circuit. According to the transition fault model, there are two types of faults possible on all lines in the circuit: a STR and a STF. A slow-to rise fault at a node means that any transition from 0 to 1 on the node does not produce the correct result when the device is operating at its maximum operating frequency. Similarly, a slow-to-fall fault means that a transition from 1 to 0 on a node does not produce the correct result at full operating frequency. In any circuit, slack of a path can be defined as the difference between the clock periods, when the circuit outputs are latched and the propagation delay of the path under consideration. For a gate level delay fault to cause an incorrect value to be latched at a circuit output, the size of the delay fault must be such that it exceeds the slack of at least one path from the site of the fault to the site of an output pin or scan flip-flop. If the propagation delays of all paths passing through the fault site exceed the clock period, such a fault is referred to as a gross delay fault. Any test pattern that successfully detects a transition fault comprises of a pair of vectors {V1, V2}, where V1 is the initial vector that sets a target node to the initial value, and V2 is the next vector that not only launches the transition at the corresponding node, but also propagates the effect of the transition to a primary output or a scan flip-flop.

In other words, a set of test vectors that test for a delay fault at the output or input of a gate are such that:

- A desired transition is launched at the site of the fault.
- If the fault is a slow-to-rise fault, the final pattern is a test for a corresponding stuck-at-0 fault, and if the fault is a slow-to-fall fault, the final pattern is a test for a corresponding stuck-at-1 fault.

When compared with tests for stuck-at faults, it can be seen that the only additional requirement to test for transition faults is the presence of a pattern that initializes a node to the required value, just before the application of a stuck-at fault pattern. One might expect that the fault coverage attained by testing transition fault patterns will be close to that attained by testing stuck-at fault patterns. However, we should remember that the fault coverage obtained for transition fault patterns represent only gross delay faults.

More detailed analysis will be necessary to evaluate for smaller delay faults. Transition fault model assumes that the delay fault affects only one gate in the circuit. There are two transition faults associated with each gate viz. a slow-to-rise fault and a slow-to-fall fault. The extra delay (delay above the nominal delay of a fault-free circuit) caused by the fault is assumed to be large enough to prevent the transition from reaching any primary output at the time of observation. Thus, the delay fault can be observed independent of whether the transition propagates through a long or short path to any primary output. This model is therefore called the gross delay fault model

2.7.2.1 COMBINATIONAL CIRCUITS

The transition fault model in combinational circuits does not take into account the fault size. To detect a transition fault it is necessary to apply two input vectors, $V = \{v1, v2\}$. The first vector, *v1*, initializes the circuit while the second vector, *v2*, activates the fault and propagates its effect to some primary output. Vector *v2* can be found using stuck-at fault test generation tools. For example, to test a slow-to-rise transition, the first vector initializes the fault site to 0 whereas the second vector is a test for s-a-0 fault at the fault site. A transition fault is considered detected if a transition occurs at the fault site and a sensitized path extends from the fault site to some primary output.

As described above, testing a transition fault requires more than one vector. As a result fault equivalence rules for transition faults are more restrictive than those for stuck-at faults. Only two rules can be applied for fault equivalence collapsing for transition faults: (1) if a gate has a single input, then the input transition faults are equivalent to the output transition faults, and (2) if a gate has only one fanout, then the output transition faults are equivalent to the input transition faults on the fanout gate. Therefore, the number of collapsed transition faults for a given circuit is larger than the number of collapsed stuck-at faults.

The main advantage of the transition fault model in comparison with other delay fault models is that the number of faults in the circuit increase linearly with the number of gates. The stuck-at fault test generation and fault simulation tools can be easily modified for handling transition faults.

On the other hand, the expectation that the delay fault is long enough for the effect to propagate through any path passing through the fault site may not be realistic as short paths may have a large slack. The assumption that the delay fault affects only one gate in the circuit

might also not be realistic. A delay defect can affect more than one gate and even though none of the individual delay faults is large enough to affect the performance of the circuit, several faults can together result in performance degradation. For practical simplicity, the transition fault model is frequently used as a qualitative delay model and circuit delays are not considered in deriving tests.

2.7.2.2 SEQUENTIAL CIRCUITS

If the clock is applied at the rated speed then the transition model described above cannot be used for sequential circuits because it does not take into account the fault size. The transition fault model for a sequential circuit is characterized by the fault-site, the fault type and the fault size. As before, the fault type id slow-to-rise or slow-to-fall transition. The fault size represents the amount of extra delay caused by the defect. In sequential circuits, different fault sizes will result in different faulty next states. It depicts two time-frames of a sequential circuit. It is assumed that input vectors that the input vectors are applied at the rated speed. The clock pulse for latching is applied before the next input vector is applied. Now, suppose there is a slow-to-rise fault between signals C and D. Assume that the clock interval is 20 ns. The inputs are applied at 0 ns (reference time) for time-frame k and a rising transition occurs at signal C at 5 ns. There are two sensitized paths from C to the next state signals, E and F. Assume that the propagation delays along the two paths are 10 ns and 8 ns respectively. The transition at E and F for the fault-free circuit and the times at which they occur are shown in the figure

If the fault-size of the slow-to-rise fault at C is less than 5 ns, the next state of the faulty circuit will be the same as that of the fault-free circuit, i.e., (E, F) = (1, 0). If the fault size is greater than 5 ns but less than 7 ns, flip-flop E will catch the fault effect but flip-flop F will not (when the clock is applied at 20 ns). The faulty next state, along with the next input vector, will produce a new logic value at each signal in time-frame *k+1*. Next, let the longest and shortest sensitized paths from C to any next state signal in time-frame *k*+1 have delays of 9ns and 7 ns respectively. If the value at C in time-frame *k*+1 is logic 1 and if the fault size is in the range of (7 ns, 26 ns), the value at signal D in time-frame *k* =1 will be 1. The effects of the delayed transition will be stabilized at the next state signals in time-frame *k*+1 before the following clock pulse is applied at 40 ns.

On the other hand, if the new value at C is logic 0, regardless of the fault size, the delayed transition will be completely suppressed and the value at D in time-frame *k*+1 will be 0. If the value at C in time-frames *k*+1 is a logic 1 and if the fault size is in the range of (26 ns, 28 ns), the effects of the delayed transition will be propagated to signal E and stabilized before next clock pulse is applied. However, the next state signal F will not catch the fault effect in this case.

From the above discussion, it is clear that it impossible to guarantee the detection of a transition fault in a sequential circuit under the at-speed test application scheme without considering the size of the fault. Different fault sizes result in completely different circuit behaviours. However, the computation costs of dividing the fault sizes into hundreds of fine-grained ranges and simulating them is prohibitive. This problem can be solved using units of clock cycle as suggested. A fault can then be specified as a triple (*s*, *t*, *i*) where *s* is the faulty signal, *t* is either slow-to-rise or slow-to-fall and *i* is an integer specifying the fault size in units of clock cycles.

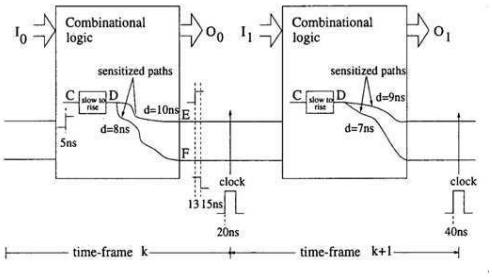

Fig 2.2 Faults Of Different Size Result In Different States

The testing methods include three modules of test sets, and the processing of the fault coverage is explained by,

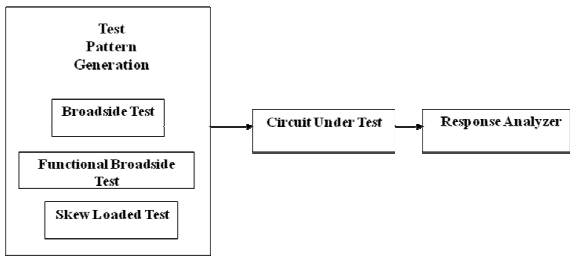

Fig. 2.3 Block Diagram Of The Project

The overall block diagram of the project is given, and they include three major categories, are

- Test pattern generation
- Circuit under test
- Response analyzer

2.8 TEST PATTERN GENERATION

These are the algorithm based test pattern generation,

2.8.1 Exhaustive Test Generation

- Completely exercise the fault-free behavior
- Appropriate only when the number of PIs is small
- Detects all the universal faults (i.e., all combinational faults)

2.8.2 Pseudo Exhaustive Test Generation

- Test most of universal faults by applying exhaustive test on subsets

2.8.3 Pseudorandom Test Generation

- Generate test pattern deterministically
- Patterns have many characteristics of random patterns but are repeatable

2.8.4 Deterministic Test Generation

- **Algebraic (symbolic) Techniques**
  - Line condition equations
  - Boolean difference
- **Path-oriented Techniques**
  - Single-path sensitization
  - D-algorithm
  - PODEM
  - FAN
  - Produces higher-efficiency test patterns, but its cost is more expensive.

2.9 CIRCUIT UNDER TEST

Testing an electronic circuit is a process of applying suitable stimuli to the circuit under test and analyzing the circuit response to ascertain that the circuit behaves as expected. Circuit is taken for the testing under the three test methods and the tests are carried out for the different pattern of tests and the efficient method is obtained for the next analysis of response for the efficient fault coverage methods

2.10 RESPONSE ANALYSER

The response analyzer is for analyzing, if the expected output is not observed then the error must exist in the circuit. By analyzing the test data of the faulty, the causes for the fault can be found. So that the fault can be identified and the analysis can be made in such away the irredundant faults can also be found. This helps in improving the design and the manufacturing process.

2.11 FAULT COVERAGE

Fault coverage is a very important concept in VLSI test. We usually use fault coverage to evaluate the efficiency of the test. The efficiency of different test structures can be measured by different test algorithms and different test strategies in terms of fault coverage. Usually the process intends to pursue high fault coverage to achieve high chip quantity. In general, the coverage of combinational circuit is high and the coverage of sequential circuit is low. To improve the fault coverage of the sequential circuit, many efforts were made such as using scan method to change sequential circuit into combinational circuit to enhance the fault coverage. Fault coverage is also a concept related with the test type. Different test may induce different fault set which will result in different fault coverage of the same circuit. Fault coverage is used to estimate the product quality. Fault coverage refers to the percentage of some type of fault that can be detected during the test of any engineered system. High fault coverage is particularly valuable during manufacturing test, and techniques such as DFT and ATPG are used to increase it.

In electronics for example, stuck-at fault coverage is measured by sticking each pin of the hardware model at logic '0' and logic '1', respectively, and running the test vectors. If at least one of the outputs differs from what is to be expected, the fault is said to be detected. Conceptually, the total number of simulation runs is twice the number of pins (since each pin is stuck in one of two ways, and both faults should be detected). However, there are many optimizations that can reduce the needed computation. In particular, often many non-interacting faults can be simulated in one run, and each simulation can be terminated as soon as a fault is detected.

A fault coverage test passes when at least a specified percentage of all possible faults can be detected. If it does not pass, at least three options are possible. First, the designer can augment or otherwise improve the vector set, perhaps by using a more effective ATPG tool. Second, the circuit may be re-defined for better fault deductibility (improved controllability and observability). Third, the designer may simply accept the lower coverage.

CHAPTER 3
EXISTING METHOD

Testing in its broadest sense means to examine a product and to ensure that it functions and exhibits the properties and capabilities that it was designed to possess. Main purpose of testing is to detect malfunctions in the product hardware and to locate their causes so that they may be eliminated .The existing methods of testing methods include the broadside, functional broadside and skewed load test formation. There are three main methods that can be used to generate and apply transition fault tests.

The first method, termed Broad-side delay test, is also referred to as functional justification or the launch-from-capture technique. In this technique, the first vector of the pair is scanned into the chain and the second vector is derived as the combinational circuit's response to the first vector.

The second method, termed Skewed load transition testing, is also referred to as the launch-from-shift technique. In this method, both the first and second vectors of the pair are delivered through the scan cells themselves. If the scan-chain is N bits long, an N-bit vector is loaded by scanning in the first (N-1) bits. The last shift clock is used to launch the transition, followed by a quick capture.

In the third method, termed Enhanced-scan transition testing, the two vectors (V1, V2) are stored in the tester memory. Vector V1 is first applied and this initializes the circuit. Vector V2 is then scanned in, followed by applying it to the circuit under test and capturing its response. The important point is that it is assumed that the initialization provided by V1 is not lost while loading V2. Therefore, this type of test assumes a hold-scan design. For inclusion of hold-scan cells, an area overhead is evident and there is an additional routing requirement for the control signal. As a result, such hold-scan cells are not used in the ASIC industry and thus, enhanced scan-design is not always useful in a practical environment. The main focus of this thesis is to compare the implementation, performance and tradeoffs with using Broad-side and Skewed-load transition fault testing techniques on industrial designs.

3.1 BROADSIDE TESTS

A broad-side delay test is a form of a scan-based delay test, where the first vector of the pair is scanned into the chain and the second vector of the pair is the combinational circuit's response to this first vector. This delay test form is called "broad-side" since the second vector of the delay test pair is provided in a broad-side fashion, namely through the logic. A deterministic broadside test generation procedure is proposed for transition path delay faults.

Under this fault model, a path delay fault is detected if and only if all the individual transition faults along the path are detected by the same test. This is important for detecting both small and large delay defects. We denote a broadside test by <si ai ,sj aj>, where si is the scan-in state, ai and aj are the primary input vectors, and sj is the state reached after si is scanned-in and ai is applied in functional mode

- In scan-based circuits, a broadside test specifies a scan-in state denoted by s, and two primary input vectors denoted by a1 and a2. We denote a broadside test by (s, a1, a2). The testing is carried out with the ISCAS-89 benchmark s27 circuit.

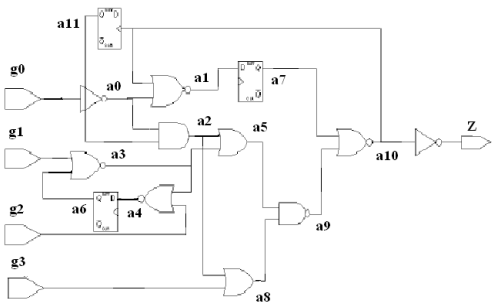

Fig 3.1 ISCAS-89 Benchmark S27 Circuit

In the broad side testing, the first pattern of the transition fault is applied through the scan chain, and the second chain is applied through the functional path of the circuit. Since the second pattern of a two pattern generation is determined by the response of the combinational logic of the circuit to the first pattern. It is more difficult to obtain a second pattern by controlling the first pattern. To overcome this problem we use the technique of stuck at tests, corresponding to the first pattern of a two pattern test for a transition fault. In the hazard based detection condition the stuck at faults help in pointing out the presence of fault when an output value is different from the expected fault free value under the second pattern of test.

Due to the constraints imposed on scanning element S2, broadside tests result in a loss of fault coverage compared to enhanced scan test. To address the reduced fault coverage of skewed-load and broadside tests, several design-for-testability approaches were developed. These methods provide better control over the state of the circuit under the second pattern of a test, thus improving the delay fault coverage that can be achieved for the circuit. Improving the fault coverage is important since undetected faults may imply reliability issues that will show up as faults that affect functional operation**.**

3.1.1 ALGORITHMS FOR THE BROADSIDE TESTING

- The Input and the memory elements will be given all possible combinations. We denote broadside test by Si Vi,Sj Vj , where Si is the scan in state,Vi,Vj are the primary input vectors, Sj is the state reached after si is scanned in, and the vi is applied in the functional mode
- Clock only is necessary to give during simulation process, every other processing are done as the consecutive processing.
- Sout and Vout are the scan and vector outputs. Fault injected here is the stuck at fault.
- Tmp_ ram gives the fault covered in testing process. Fa, fa1 are the fault free and faulty outputs respectively

3.2 FUNCTIONAL BROADSIDE TEST

Functional broadside tests were defined to avoid over testing that may occur under structural scan-based tests. Over testing occurs due to non-functional operation conditions created by unreachable scan-in states. Functional broadside tests were computed assuming that functional operation start after the circuit is synchronized. Scan-based structural tests may cause over testing, or unnecessary yield loss, by operating the circuit in states that the circuit cannot enter during functional operation. Such states are called unreachable states. An unreachable state may be entered during a scan-based test, if an unreachable state is used as the scan-in state of the test. Functional scan-based tests were defined to address the issue.

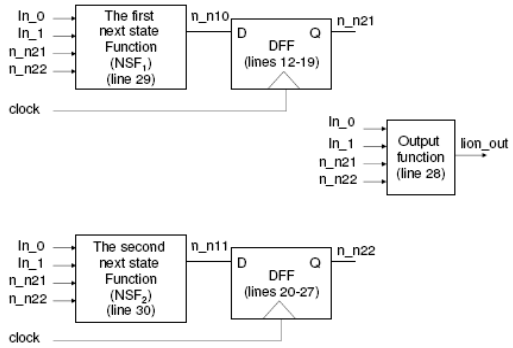

Fig 3.2 Lion Circuit - Line Information For Open Networks

In a functional scan-based test, the scan-in state is a reachable state, or a state that the circuit can enter during functional operation. The definition of a functional scan-based test was applied to two-pattern scan-based tests for delay faults. The resulting definition is that of a functional broadside test. A broadside test applies two primary input vectors in functional mode after the initial state is scanned in for enhanced-scan transition testing; two vectors (V1, V2) are scanned in and stored in the scan FFs simultaneously. Enhanced scan transition test has two primary advantages: higher fault coverage and lower test data volume. Enhanced-scan gives better fault coverage's than both skewed-load transition test and broadside transition test because there is no dependency between the two vectors in enhanced-scan test pattern. In addition, compact transition tests can be achieved to reduce the test data volume and application time for enhanced scan.

However, one drawback of the enhanced-scan testing is that a hold-scan design is needed. Although the hold-scan model has been used in some high-performance circuits, such as microprocessors, the area overhead and the additional routing requirement for control signal still limit the hold-scan cell model from wide use in the ASIC community. Moreover, because any state combination for V1 and V2 is possible, many untestable faults are detected.

In a functional broadside test si is a reachable state. After si is scanned in, the circuit makes state-transitions, from si to sj under ai , and from sj under aj , that it can also make during functional operation. Scan input first given with respect to the vector (input state transition from s1 to s2 under v1) to avoid over testing.

3.2.1 ALGORITHM FOR FUNCTIONAL BROADSIDE TESTING

- Scan input first given with respect to the vector (input state transition from s1 to s2 under v1) to avoid over testing.
- Here the fault is injected in the s2.
- Clock only is necessary to give during simulation process, every other processing are done as the consecutive processing.
- Sout and vout are the scan and vector outputs. fault injected here is the stuck at fault .
- Tmp_ ram gives the fault covered in testing process. Fa, fa1 are the fault free and faulty outputs respectively

3.3 SKEWED LOAD TESTS

Under skewed-load tests, after s2 is scanned in, s1 is obtained by a single additional shift of the scan chain(s). Both skewed-load and broadside tests result in a loss of fault coverage compared to enhanced scan tests. To address the reduced fault coverage of skewed-load and broadside tests, several design-for-testability approaches were developed .These methods provide better control over the state of the circuit under the second pattern of a test, thus improving the delay fault coverage that can be achieved for the circuit.

Improving the fault coverage is important since undetected faults may imply reliability issues that will show up as faults that affect functional operation .In addition, the presence of undetected faults may invalidate tests for other faults For skewed-load transition testing (also called last shift, an N-bit vector is loaded by shifting in the first N-1 bits, where N is the scan-chain length. The last shift clock is used to launch the transition. This is followed by a quick capture. For skewed-load testing, only one vector is stored for each transition pattern in tester scan memory; the second vector is a shifted version of the stored vector.

Therefore, skewed-load testing is constrained by the correlation of the bits in the test pattern based on scan chain ordering .The slow-to-fall on line is untestable in skewed-load testing.

3.3.1 ALGORITHMS FOR THE SKEWED LOAD TESTS

To detect the slow-to-fall fault on line d, we need to set the second vector V2=000 to detect the d s-a-1, therefore the initial vector must be 00X, the previously shifted version V2.

- However, this V1, 00X, is unable to initialize the line to logic 1.
- Since 000 is the only vector that can detect the d s-a-1 fault, thus d slow-to-fall is untestable in skewed-load testing. Based on this observation, skewed-load may miss some functionally testable faults because of the data dependency between the two vectors, resulting in under testing of the functionally testable faults.
- Clock only is necessary to give during simulation process, every other processing are done as the consecutive processing.
- Sout and vout are the scan and vector outputs. fault injected here is the stuck at fault .
- Tmp_ ram gives the fault covered in testing process. Fa, fa1 are the fault free and faulty outputs respectively

CHAPTER 4
PROPOSED METHOD

4.1 DESIGNS FOR TESTABILITY TECHNIQUES

Design for testability (DFT) refers to those design techniques that make the task of subsequent testing easier. There is definitely no single methodology that solves all embedded system-testing problems. There also is no single DFT technique, which is effective for all kinds of circuits. DFT techniques can largely be divided into two categories, i.e., ad hoc techniques and structured (systematic) techniques. DFT methods for digital circuits: The DFT methods for the digital circuits include

- Ad-hoc method
- Structured method:
  - Scan
  - Partial Scan
  - Built-in self-test
  - Boundary scan

The testing is done to improve the fault coverage; the testing process concentrates on the structured tests. They are mainly concentrating on the scanning (full scan) and the partial scanning than the boundary scan testing and BIST.

4.2 DEMERITS OF BIST

- Additional silicon area and fabrication processing requirements for the BIST circuits
- Reduced access times
- Additional pin (and possibly bigger package size) requirements, since the BIST circuitry need a way to interface with the outside world to be effective.
- Possible issues with the correctness of BIST results, since the on-chip testing hardware itself can fail.

4.3 DEMERITS OF BOUNDRY SCAN

- The disadvantage is very long shifting sequences to deliver test patterns to each component, and to shift out test responses. This leads to expensive time on the external tester
- The test patterns are half as long and test time is roughly halved.

4.4 AD-HOC DFT METHODS

Good design practices learnt through experience are used as guidelines for ad-hoc DFT. Some important guidelines are given below.

- Large circuits should be partitioned into smaller sub-circuits to reduce test costs. One of the most important steps in designing a testable chip is to first partition the chip in an appropriate way such that for each functional module there is an effective (DFT) technique to test it. Partitioning must be done at every level of the design process, from architecture to circuit, whether testing is considered or not. Partitioning can be functional (according to functional module boundaries) or physical (based on circuit topology). Partitioning can be done by using multiplexers and/or scan chains.
- Test access points must be inserted to enhance controllability & observability of the circuit. Test points include CP and OP. The CPs is active test points, while the OPs are passive ones. There are also test points, which are both CPs and OPs. Before exercising test through test points that are not PIs and POs, one should investigate into additional requirements on the test points raised by the use of test equipments.
- Circuits (flip-flops) must be easily initializable to enhance predictability. A power-on reset mechanism controllable from primary inputs is the most effective and widely used approach.
- Test control must be provided for difficult-to-control signals.
- ATE requirements such as pin limitation, tri-stating, timing resolution, speed, memory depth, driving capability, analog/mixed-signal support, internal/boundary scan support, etc., should be considered during the design process to avoid delay of the project and unnecessary investment on the equipments.

- Analog and digital circuits should be kept physically separate. Analog circuit testing is very much different from digital circuit testing. Testing for analog circuits refers to real measurement, since analog signals are continuous (as opposed to discrete or logic signals in digital circuits). They require different test equipments and different test methodologies. Therefore they should be tested separately.

4.4.1 THINGS TO BE AVOIDED

- Asynchronous (unclocked) logic feedback in the circuit must be avoided. A feedback in the combinational logic can give rise to oscillation for certain inputs. Since no clocking is employed, timing is continuous instead of discrete, which makes tester synchronization virtually impossible, and therefore only functional test by application board can be used.
- Monostables and self-resetting logic should be avoided. A monostable (one-shot) multivibrator produces a pulse of constant duration in response to the rising or falling transition of the trigger input. Its pulse duration is usually controlled externally by a resistor and a capacitor (with current technology, they also can be integrated on chip). One-shots are used mainly for pulse shaping, switch-on delays, switch-off delays, and signal delays. Since it is not controlled by clocks, synchronization and precise duration control are very difficult, which in turn reduces testability by ATE. Counters and dividers are better candidates for delay control.
- Redundant gates must be avoided.
- High fanin/fanout combinations must be avoided as large fan-in makes the inputs of the gate difficult to observe and makes the gate output difficult to control.
- Gated clocks should be avoided. These degrade the controllability of circuit nodes.

4.4.2 DRAWBACK OF AD-HOC METHOD

The drawback of the ad-hoc methods are given below

- There is a lack of experts and tools.
- Test generation is often manual
- This method cannot guarantee for high fault coverage.
- It may increase design iterations.
- This is not suitable for large circuits

4.7 SCAN DESIGN APPROACHES FOR DFT

The scan designs for the testing process is given below , the processing goes on with the flow of what all the things to be followed, the requirements, design rules for scanning and partial and the reason for going for partial scanning method.

4.7.1 OBJECTIVES OF SCAN DESIGN

- Scan design is implemented to provide controllability and observability of internal state variables for testing a circuit.
- It is also effective for circuit partitioning.
- A scan design with full controllability and observability turns the sequential test problem into a combinational one.

4.7.2 SCAN DESIGN REQUIREMENTS

- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design.
  - One (or more) TC pin at the primary input is required.
  - Flip-flops are replaced by (SFF) and are connected so that they behave as a shift register in the test mode. The output of one SFF is connected to the input of next SFF. The input of the first flip-flop in the chain is directly connected to an input pin (denoted as SCAN In), and the output of the last flip-flop is directly connected to an output pin (denoted as SCANOUT). In this way, all the flip-flops can be loaded with a known value, and their value can be easily accessed by shifting out the chain. Fig 4.1shows a typical circuit after the scan insertion operation.
  - Input/output of each scan shift register must be available on PI/PO.
- Combinational ATPG is used to obtain tests for all testable faults in the combinational logic.
- Shift register tests are applied and ATPG tests are converted into scan sequences for use in manufacturing test.

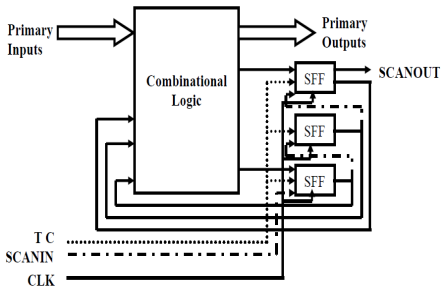

Fig 4.1 Scan Structure to a Design

Fig 4.1 shows a scan structure connected to design. The scan flip-flips (FFs) must be interconnected in a particular way. This approach effectively turns the sequential testing problem into a combinational one and can be fully tested by compact ATPG patterns. Unfortunately, there are two types of overheads associated with this technique. These are the hardware overhead (including three extra pins, multiplexers for all FFs, and extra routing area) and performance overhead (including multiplexer delay and FF delay due to extra load).

4.7.3 SCAN DESIGN RULES

- Only clocked D-type master-slave flip-flops for all state variables should be used.
- At least one PI pin must be available for test. It is better if more pins are available.
- All clock inputs to flip-flops must be controlled from primary inputs (PIs). There will be no gated clock. This is necessary for FFs to function as a scan register.
- Clocks must not feed data inputs of flip-flops. A violation of this can lead to a race condition in the normal mode.

4.7.4 SCAN OVERHEADS

The use of scan design produces two types of overheads. These are area overhead and performance overhead. The scan hardware requires extra area and slows down the signals.

- **IO pin overhead:** At least one primary pin necessary for test.
- **Area overhead:** *Gate overhead* = [4 n_{sff}/(n_g+10n_{ff})] x 100%, where n_g = number of combinational gates; n_{ff} = number of flip-flops; n_{sff} = number of scan flip-flops; For full scan number of scan flip-flops is equal to the number of original circuit flip-flops. Example: n_g = 100k gates, n_{ff} = 2k flip-flops, overhead = 6.7%. For more accurate estimation scan wiring and layout area must be taken into consideration.
- **Performance overhead:** The multiplexer of the scan flip-flop adds two gate-delays in combinational path. Fanouts of the flip-flops also increased by 1, which can increase the clock period.

4. 8 PARTIAL SCAN DESIGN

Functional broadside tests were defined to address over testing that may occur due to the detection of delay faults under non-functional operation conditions. Such conditions are made possible by scanning in unreachable states. Functional broadside tests were defined and studied in the context of full-scan circuits. In this work, we study the definition of broadside and functional broadside tests in partial-scan circuits. A unique property we show is that if the unscanned state variables are observable (through the application of input sequences or through observation points), the fault coverage achievable with functional broadside tests is independent of the level of scan and the subset of scanned state variables. This implies that when functional broadside tests are used to avoid over testing, using lower percentages of scanned state variables may be possible without reducing the fault coverage significantly.

In this approach only a subset of flip-flops is scanned. The main objectives of this approach are to minimize the area overhead and scan sequence length. It would be possible to achieve required fault coverage. In this approach sequential ATPG is used to generate test patterns. Sequential ATPG has number of difficulties such as poor initializability, poor controllability and observability of the state variables etc. The reason for adopting the partial scan method is because generalized scan method is used here; scan varying from 0 to 100%.Partial-scan has lower overheads (area and delay) and reduced test length .Partial-scan

allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned

Number of gates, number of FFs and sequential depth give little idea regarding testability and presence of cycles makes testing difficult. Therefore sequential circuit must be simplified in such a way so that test generation becomes easier. Removal of selected flip-flops from scan improves performance and allows limited scan design rule violations. It also allows automation in scan flip-flop selection and test generation .Fig 4.2 shows a design using partial scan architecture. Sequential depth is calculated as the maximum number of FFs encountered from PI line to PO line.

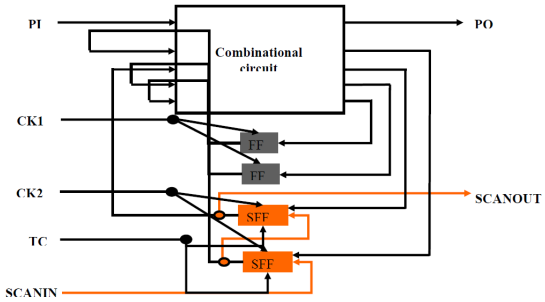

Fig 4.2 Partial Scan Architecture

4.8.1 THINGS TO BE FOLLOWED

- A minimum set of flip-flops must be selected, removal of which would eliminate all cycles.
- Break only the long cycles to keep overhead low.
- All cycles other than self-lops should be removed

4.9 HAZARD BASED DETECTION CONDITION

The hazard-based detection conditions, we consider the a→ a□ transition fault on a line g, where a ∈ {0,1} Under the conventional detection conditions, the fault is assumed to delay an the a→ a□ transition on g, during the second pattern of a test. The fault is detected by a two-pattern test that sets g = a under the first pattern g = a□ under the second pattern, and detects the fault g stuck-at a during the second pattern.

The hazard-based detection conditions for the fault require a hazard or a pulse on g under which g will make the transition a□→ a → a□ during the second pattern of a test. The fault is assumed to delay the transition a → a□ of the pulse. Thus, in the presence of the fault, g is assumed to make the transition a → a□, and stay at a instead of switching back to a□ during the second pattern of the test. Such a fault is detected by a two-pattern test that sets g = a□ under the first pattern, creates the pulse on g during the second pattern, and detects the fault g stuck-at a during the second pattern.

- The testing is done under the hazard based detection condition for the broadside test method.
- A fault is still detected when an output value is different from the expected fault-free value under the second pattern of a test.
- The detection of fault is correctly identified.
- By the occurrence of switching from o to 1.
- And the change stays at the same place, gives the information that the fault has occurred at this stage

4.9.1 ADVANTAGES OF HAZARD BASED DETECTION

- Does not change the test application process or the analysis of test responses.
- In the case of hazard-based detection conditions, a fault is detected if the value of a hazard (or a pulse) is sampled.
- The fault causes the pulse to be longer, thus causing a faulty value to be sampled.

CHAPTER 5

SIMULATION RESULT

Simulation can be used to show the eventual real effects of alternative conditions and courses of action. Simulation is also used when the real system cannot be engaged, because it may not be accessible, or it may be dangerous or unacceptable to engage, or it is being designed but not yet built, or it may simply not exist .The simulation is carried out for the different set of test to prove that the proposed method is efficient for the improved fault coverage. For the illustration, the tests are carried for the broadside, functional and skewed loaded tests.

In the normal way of testing the faults that are present in the circuit, is not detected. Due to this concern the product is not successfully sold in the market. The testing process is carried, to check whether it meet the consumer requirement. So the product which satisfies the requirements is successful in the market. But the testing methods that is carried here is not much efficient in the fault coverage.

So a new method called the hazard based detection condition is introduced. Due to this method, the irredundant faults are also detected. The simulation results are compared for normal testing mode of the broadside test, functional broadside tests, and the skewed load test along with the hazard based detection condition and the results are compared. In the same way the testing process, inputs are given in scan method only. A new method of scanning called partial scanning is also done and the results are compared .The simulation results are listed in the below figures. And the table 5.20 describes the comparisons, and the chart gives out the easier understanding.

5.1 BROADSIDE TESTS

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. The inputs are all already assigned for each and every gate in ISCAS-89 BENCHMARK S27 CIRCUIT in fig 3.1; the STO fault is injected at the fa1. The fault free output is the fa. By comparing the fa (fault free circuit) with fa1 (faulty circuit). The output z is observed for the presence of fault in the 12th pattern and the indication of fault is identified by the hazard (or a pulse) sampled is observed. The fault is detected in the 7th pattern, like the switching over from 1 to 0

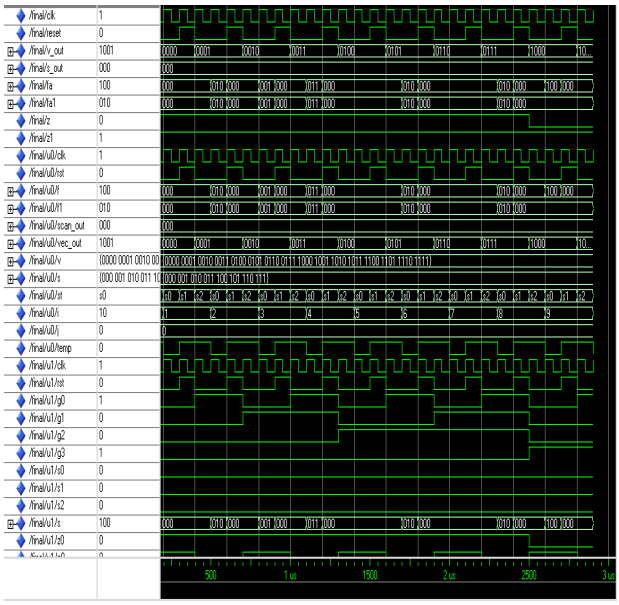

Fig 5.1 Simulation Result of the Broadside Test of Hazard S-27

5.2 BROADSIDE TEST USING LION CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. The inputs are all already assigned for each and every gate in the LION circuit; the STO fault is injected at the fa1. The fault free output is the fa. By comparing the fa (fault free circuit) with fa1 (faulty circuit).The input and the memory elements are given all possible combinations. Once the scan element s1 is given it gets incremented to the next bit according to the no of bits given for the input. Vout is the vector input, s out is the input giving vector. Fa,fa1 are the memory elements. Tmp_ram gives out the faults that are detected. N and the n_n21 are the interconnections.

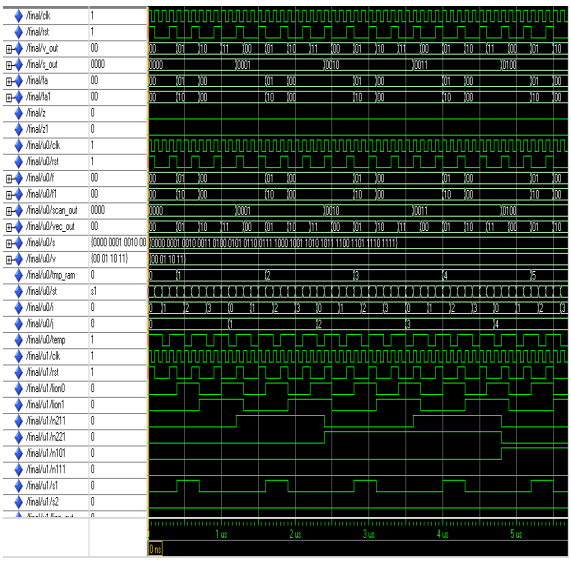

Fig 5.2 Simulation Result Obtained by Broadside Test Using LION Circuit

5.3 BROADSIDE - HAZARD TEST USING LION CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. The STO fault is injected at the fa1. The fault free output is the fa. By comparing the fa (fault free circuit) with fa1 (faulty circuit).The input and the memory elements are given all possible combinations. The LION circuit is given in fig 3.2, where n and the n_n21 are the interconnections. Once the scan element s1 is given it gets incremented to the next bit according to the no of bits given for the input. Vout is the vector input, s out is the input giving vector. Fa, fa1 are the memory elements. Tmp_ram gives out the faults covered. The fault covered in the hazard based detection condition is better than that of the normal broadside testing.

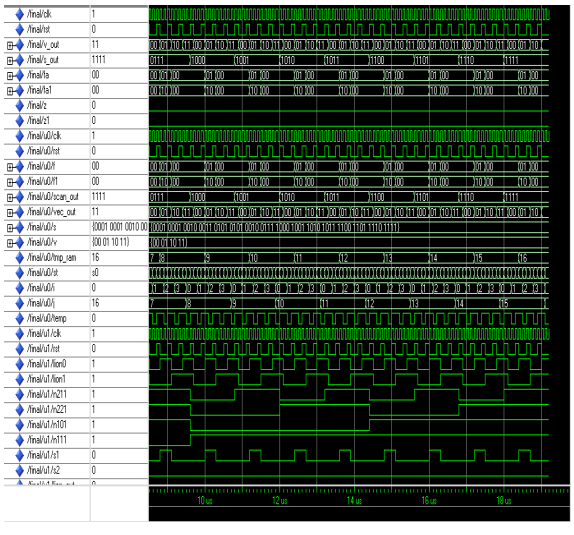

Fig 5.3 Simulation Result Obtained by Broadside - Hazard Test Using LION Circuit

5.4 FUNCTIONAL BROADSIDE TEST USING LION CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. S2 is the fault given here; the scan initializes the testing process and then allows the test to apply the vector inputs. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected. The LION circuit is given in the fig 3.2, where n and the n_n21 are the interconnections. Scan input first given with respect to the vector .The input state transition from s1 to s2 under v1, this is done to avoid over testing.

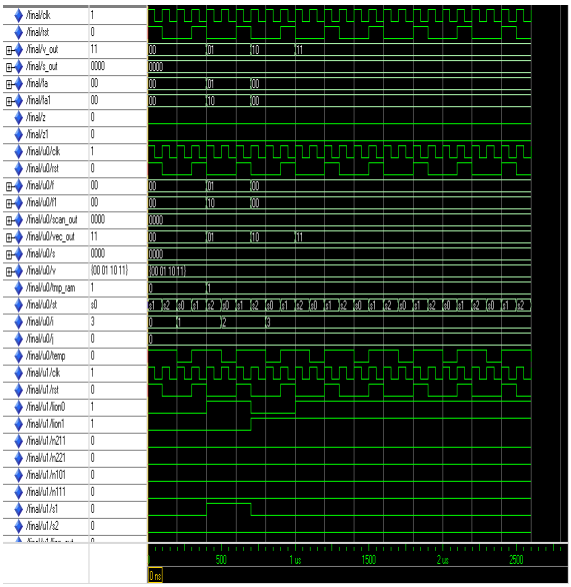

Fig 5.4 Simulation Result Obtained By Functional Broadside Test Using LION Circuit

5.5 FUNCTIONAL BROADSIDE- HAZARD TEST USING LION CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. S2 is the fault given here; the scan initializes the testing process and then allows the test to apply the vector inputs. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected. The LION circuit is given in fig 3.2, where n and the n_n21 are the interconnections. Scan input first given with respect to the vector. The fault coverage in the hazard based detection of the functional broadside testing is better than the convententional testing.

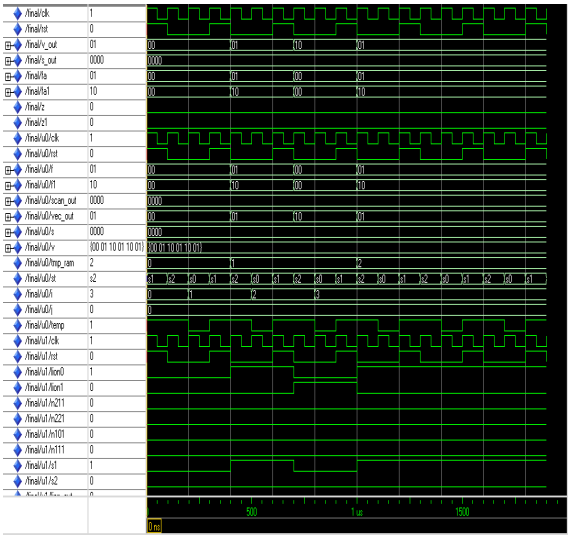

Fig 5.5 Simulation Result Obtained by Functional Broadside- Hazard Test Using LION Circuit

5.6 SKEWED LOAD TEST USING LION CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. In the skewed load test, scan element initializes the testing giving the inputs to the vector elements v followed by scan elements. The scan elements are incremented by the right shifting operation .They are also known as the scan shifting. The process is similar to the right shifting which is also known as the scan shifting. The LION circuit is given in fig 3.2, where n and the n_n21 are the interconnections. Vout is the vector input, s out is the input giving vector. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected.

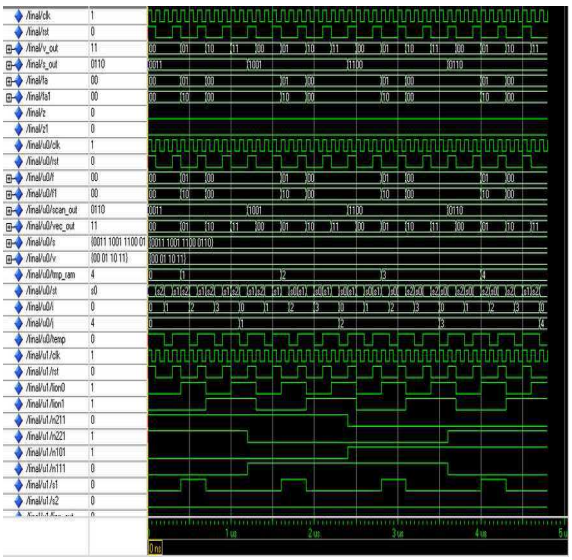

Fig 5.6 Simulation Result Obtained by Skewed Load Test Using LION Circuit

5.7 SKEWED LOAD - HAZARD TEST USING LION CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. In the skewed load test, scan element initializes the testing giving the inputs to the vector elements v followed by scan elements. The scan elements are incremented by the right shifting operation .They are also known as the scan shifting. The process is similar to the right shifting which is also known as the scan shifting. The LION is given in fig 3.2, where n and the n_n21 are the interconnections. Vout is the vector input, s out is the input giving vector. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected.

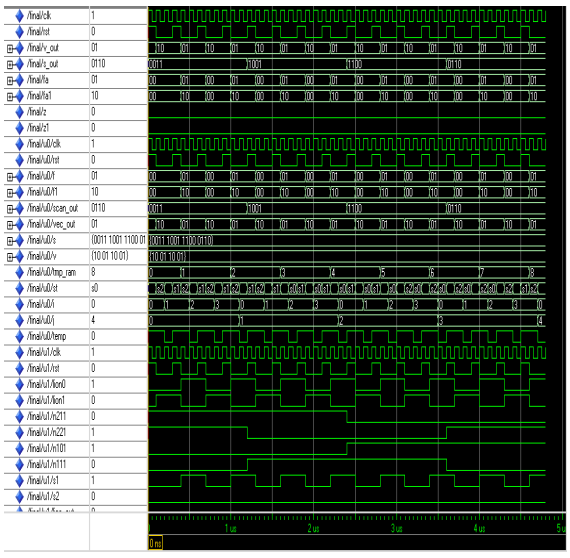

Fig 5.7 Simulation Result Obtained by Skewed Load – Hazard Test Using LION Circuit

5.8 BROADSIDE TESTS OF THE ISCAS BENCHMARK S-27 CIRCUIT.

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. The inputs are all already assigned for each and every gate in ISCAS-89 BENCHMARK S27 CIRCUIT in fig 3.1; the STO fault is injected at the fa1. The fault free output is the fa. By comparing the fa (fault free circuit) with fa1 (faulty circuit). The output z is observed for the presence of fault in the 12th pattern and the indication of fault is identified by the hazard (or a pulse) sampled is observed.

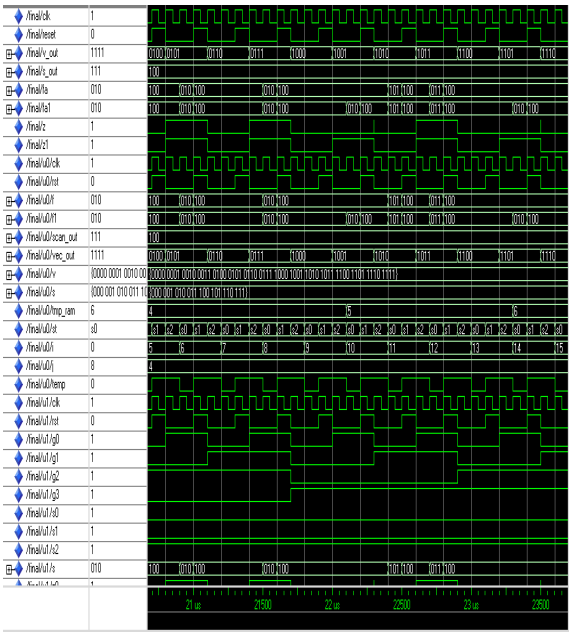

Fig 5.8 Simulation Result of Broadside Test of ISCAS Benchmark S-27 Circuit

5.9 HAZARD TEST OF THE ISCAS BENCHMARK S-27 BROADSIDE

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. The inputs are all already assigned for each and every gate in ISCAS-89 BENCHMARK S27 CIRCUIT; the STO fault is injected at the fa1. The fault free output is the fa. By comparing the fa (fault free circuit) with fa1 (faulty circuit). The fault is detected in the 7th pattern, like the switching over from 1 to 0. The fault covered here is nearly 70% than the normal broadside testing.

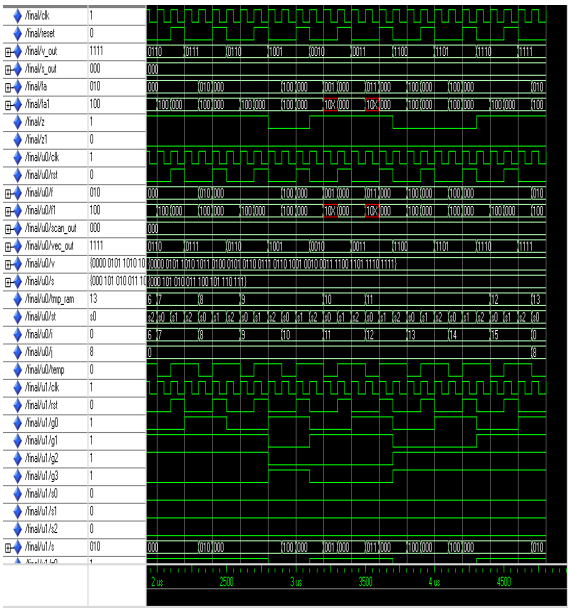

Fig 5.9 Simulation Result of the Broadside Hazard Test of ISCAS Benchmark S-27 Circuit

5.10 FUNCTIONAL BROADSIDE TEST ISCAS BENCHMARK S-27 CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. S2 is the fault given here; the scan initializes the testing process and then allows the test to apply the vector inputs. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected. N and the n_n21 are the interconnections. Scan input first given with respect to the vector .The input state transition from s1 to s2 under v1, this is done to avoid over testing

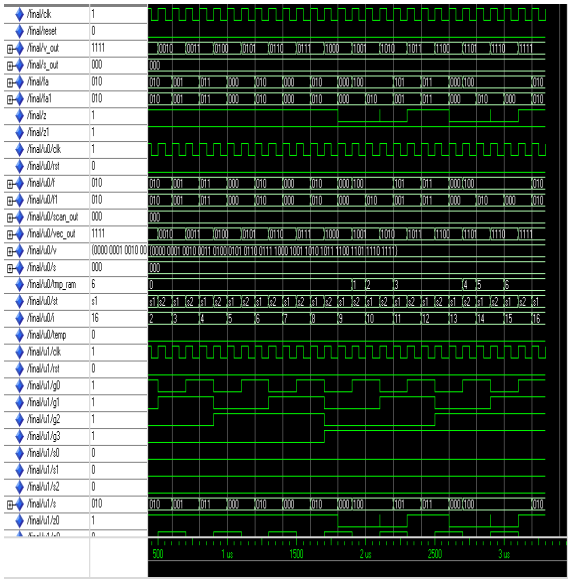

Fig 5.10 Simulation Result Obtained for Functional Broadside S27

5.11 FUNCTIONAL BROADSIDE HAZARD TEST OF ISCAS BENCHMARK S-27CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. S2 is the fault given here; the scan initializes the testing process and then allows the test to apply the vector inputs. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected. N and the n_n21 are the interconnections. Scan input first given with respect to the vector. In the hazard based detection the fault coverage is better as compared to the normal mode of the test set.

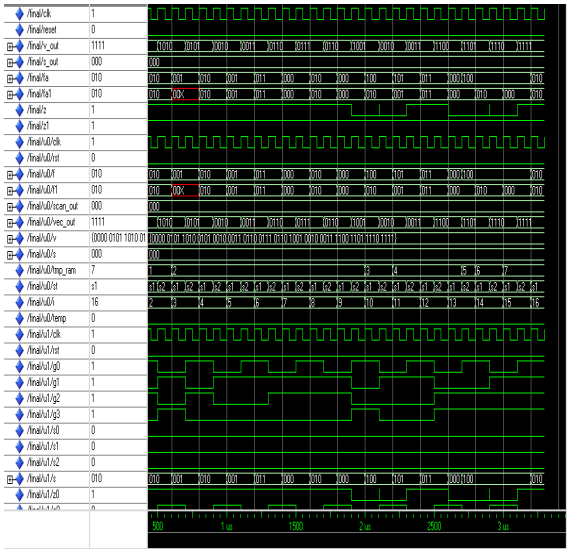

Fig 5.11 Simulation Result Obtained Functional Broadside Hazard Test of Benchmark S-27 Circuit

5.12 SKEWED LOAD TEST FOR BENCHMARK ISCAS S- 27 CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. In the skewed load test , scan element initializes the testing giving the inputs to the vector elements v followed by scan elements The process is similar to the right shifting which is also known as the scan shifting Vout is the vector input, s out is the input giving vector. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected.

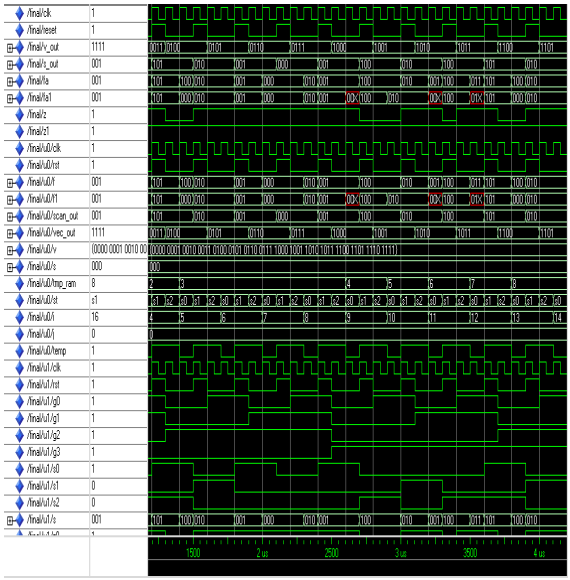

Fig 5.12 Simulation Result Obtained for Skewed Load Test for Benchmark ISCAS S-27 Circuit.

5.13 SKEWED LOAD TEST FOR BENCHMARK ISCAS S-27CIRCUIT HAZARD TEST.

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. In the skewed load test , scan element initializes the testing giving the inputs to the vector elements v followed by scan elements The process is similar to the right shifting which is also known as the scan shifting Vout is the vector input, s out is the input giving vector. Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected. The hazard based detection results in the fault coverage of nearly 68% improved stage.

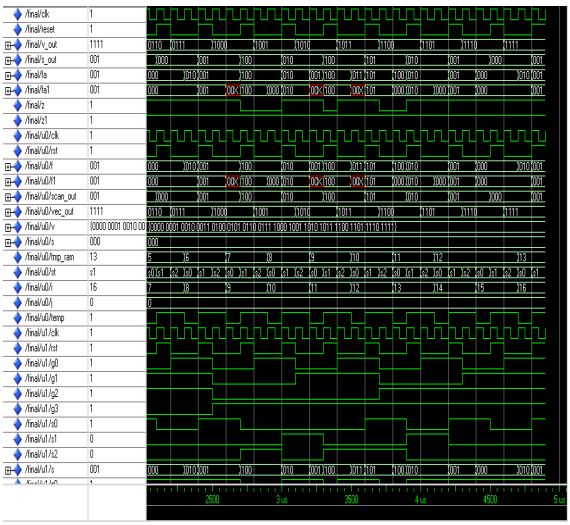

Fig 5.13 Simulation Result Obtained for Skewed Loaded Hazard Test for Benchmark ISCAS S-27

5.14 SCAN VS PARTIAL SCAN

The tests are carried out for the ISCAS S-27 for scan and partial scan method. The simulation results are obtained for the broadside test and functional broadside test for full scan and partial scan method

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5.14.1 BROADSIDE TESTS FOR THE BENCHMARK ISCAS S-27 CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. The inputs are all already assigned for each and every gate in ISCAS-89 BENCHMARK S27 CIRCUIT in fig 3.1; the STO fault is injected at the fa1. The fault free output is the fa. By comparing the fa (fault free circuit) with fa1 (faulty circuit). The output z is observed for the presence of fault in the 12th pattern and the indication of fault is identified by the hazard (or a pulse) sampled is observed.

Fig 5.14 Simulation Result Obtained for the Benchmark ISCAS S-27 - Broadside Test

5.14.2 PARTIAL SCAN OF THE BENCHMARK ISCAS S-27- BROADSIDE TEST

In the partial scanning method, the process of testing follows around, timing is reduced for reduced so that the fault coverage is concentrated more and the transition fault coverage is completed in minimum span of time. The number of inputs given is taken to be don't care condition so that the inputs can be given in selected order. Fault coverage is increased and time taken is also is low.

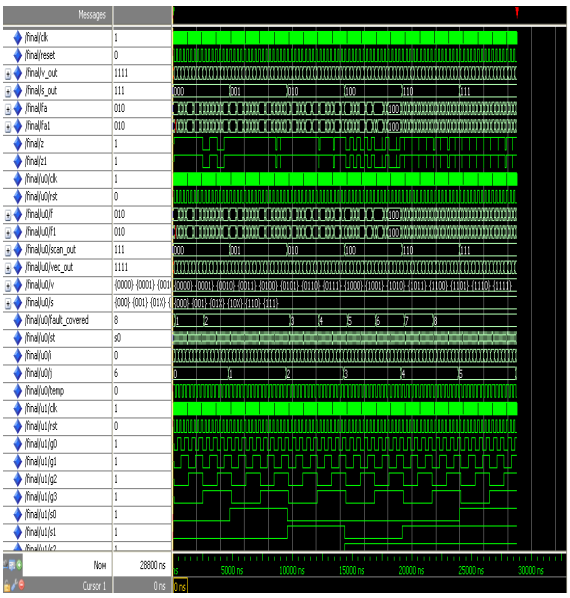

Fig 5.15 Simulation Result Obtained for Partial Scan of the Benchmark S- 27 Broadside Test.

5.14.3 FUNCTIONAL BROADSIDE TEST FOR THE ISCAS S-27 BENCHMARK CIRCUIT

The simulation is being carried out with Modelsim6.3g. The fault detection is identified by giving the input for the clock pulse alone. S2 is the fault given here; the scan initializes the testing process and then allows the test to apply the vector inputs. . Fa, fa1 are the memory elements. Tmp_ram gives out the faults that are detected. N and the n_n21 are the interconnections. Scan input first given with respect to the vector .The input state transition from s1 to s2 under v1, this is done to avoid over testing.

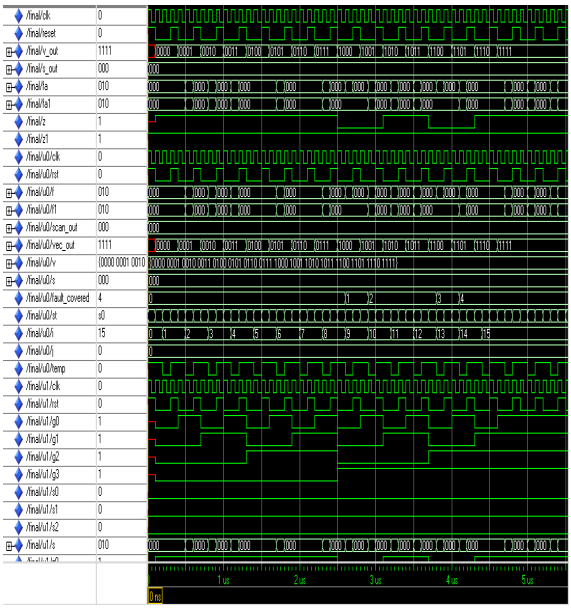

Fig5.16 Simulated Result Obtained for Functional Broadside Test for the ISCAS S-27 Circuit

5.14.4 PARTIAL SCAN OF THE BENCHMARK ISCAS S- 27 FUNCTIONAL BROADSIDE TEST

In the partial scanning method, the process of testing follows around, timing is reduced for reduced so that the fault coverage is concentrated more and the transition fault coverage is completed in minimum span of time. The number of inputs given is taken to be don't care condition so that the inputs can be given in selected order. Fault coverage is increased and time taken is also is low.

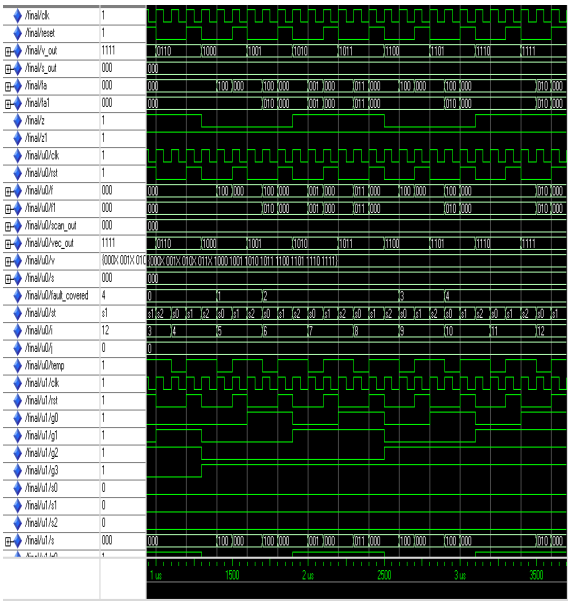

Fig 5.17 Partial Scan of ISCAS Benchmark S-27 Circuit for Functional Broadside

Table 5.1: Comparison Table of the ISCAS S-27 Circuit

Tests Carried	Fault Injected	Fault Covered In Normal Testing	Fault Covered In Hazard Test	Improved Percentage
Broadside Test	20	6	13	65
Functional Broadside Test	10	6	7	70
Skewed Load Test	20	8	13	65

The comparison table 5.1 for the ISCAS S-27 circuit for the hazard based and the normal testing methods are given. This illustrates that the fault coverage is improved in the hazard based detection condition than the normal testing.

Fig 5.18 Percentage of Fault Coverage in Benchmark ISCAS S-27 Circuit

Table 5.2: Comparison Table of the LION Circuit

Tests Carried	Fault Injected	Fault Covered In Normal Testing	Fault Covered In Hazard Test	Improved Percentage
Broadside Test	20	5	16	80
Functional Broadside Test	2	1	2	100
Skewed Load Test	10	4	8	80

The comparison table 5.1 for the LION circuit for the hazard based and the normal testing methods are given. The table 5.2 illustrates that the fault coverage is improved in the hazard based detection condition than the normal testing.

Fig 5.19 Percentage of Fault Coverage in LION Circuit

Table 5.3: Comparison Table of the ISCAS S-27 Circuit for scan and partial scan

Tests Carried	Fault Injected	Fault Covered In Scan	Fault Covered In Partial scan	Improved Percentage
Broadside Test	10	8	8	80
Functional Broadside Test	6	4	4	67

The comparison table 5.3 shows the result for the benchmark ISCAS s-27 circuit for the scan and the partial scanning. The final output is that there is no change in the fault coverage, where as to keep the overhead low, only long cycles may be eliminated .In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated. Complexity is reduced. Time taken is reduced.

Fig 5.20 Percentage of Fault Coverage in ISCAS S-27 Circuit Scan and Partial Scan

The simulation results obtained for the ISCAS S-27 and the LION circuit. The conclusion from the simulated results is , the testing methods used here for the fault coverage are not much efficient , so a new method called hazard based detection condition methods are carried out. In this method the fault covered in the testing methods of broadside, functional broadside, and skewed load tests are more than 60% improvement in fault coverage in the hazard based detection method. The comparison table and the graph are plotted for easy understanding. From the simulation result and the graph it is inferred that the normal testing of fault coverage below 40% percentage. When the simulation carried out for the hazard test the fault coverage obtained is nearly 70%. So compared to the normal testing, the hazard based detection condition is efficient.

CHAPTER 6
CONCLUSION AND FUTURE WORK

CONCLUSION

This project presents efficient fault coverage of transition delay fault using the broadside test, functional broadside test and skewed load test. The tests are performed for the s27 circuit, LION circuit. The circuit is simulated for fault free and faulty condition and the result is obtained for the presence of fault in the circuit and also the efficient fault coverage for the hazard based detection condition. the fault covered in the testing methods of broadside, functional broadside, and skewed load tests are more than 60% improvement in fault coverage in the hazard based detection method. The comparison table and the graph are plotted for easy understanding. From the simulation result and the graph it is inferred that the normal testing of fault coverage below 40% percentage. When the simulation carried out for the hazard test the fault coverage obtained is nearly 70%. So compared to the normal testing, the hazard based detection condition is efficient.

FUTURE WORK

The skewed loaded tests have to be carried for the circuit using the partial scanning method. The fault and fault free condition has to be tested and the result is compared among the various circuits and the efficient fault coverage is obtained.

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