TELEREMOTE CONTROL OF ELECTRICAL APPLIANCES

P-412

PROJECT REPORT

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CERTIFICATE

This is to certify that the Project Report entitled

"TELEREMOTE CONTROL OF ELECTRICAL APPLIANCES" has been submitted by

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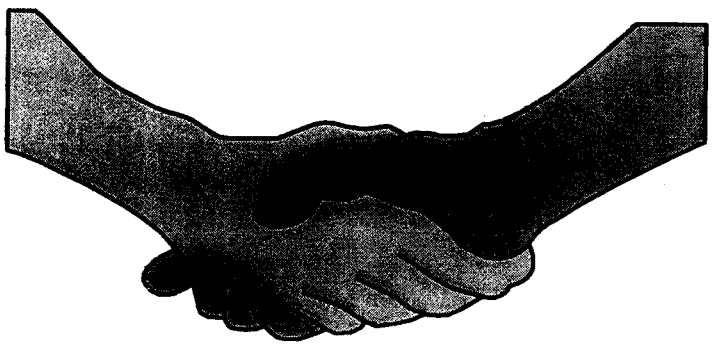
INTERNAL EXAMINER

EXTERNAL EXAMINER.



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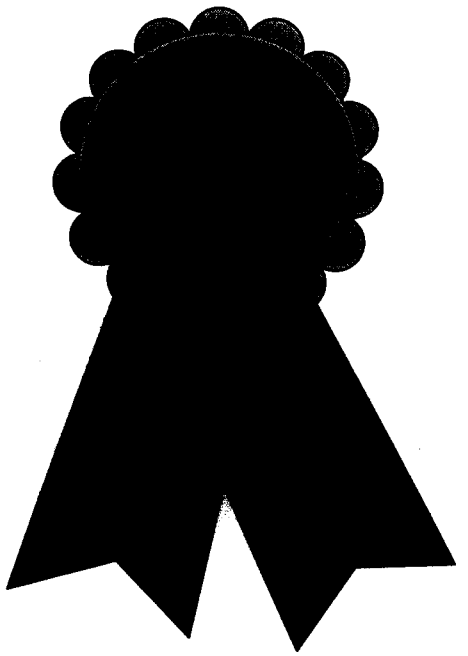

SYNOPSIS

SYNOPSIS

This project titled "TELEREMOTE CONTROL OF ELECTRICAL APPLIANCES" aims at switching on or off the various electrical appliances through telephone lines. The cicuit which is designed is capable of controlling upto nine electrical appliances. **A Dual Tone Multi Frequency** (DTMF) telephone set is used to send commands to the circuit and remotely control wide range of electrical appliances in and around the home or office.

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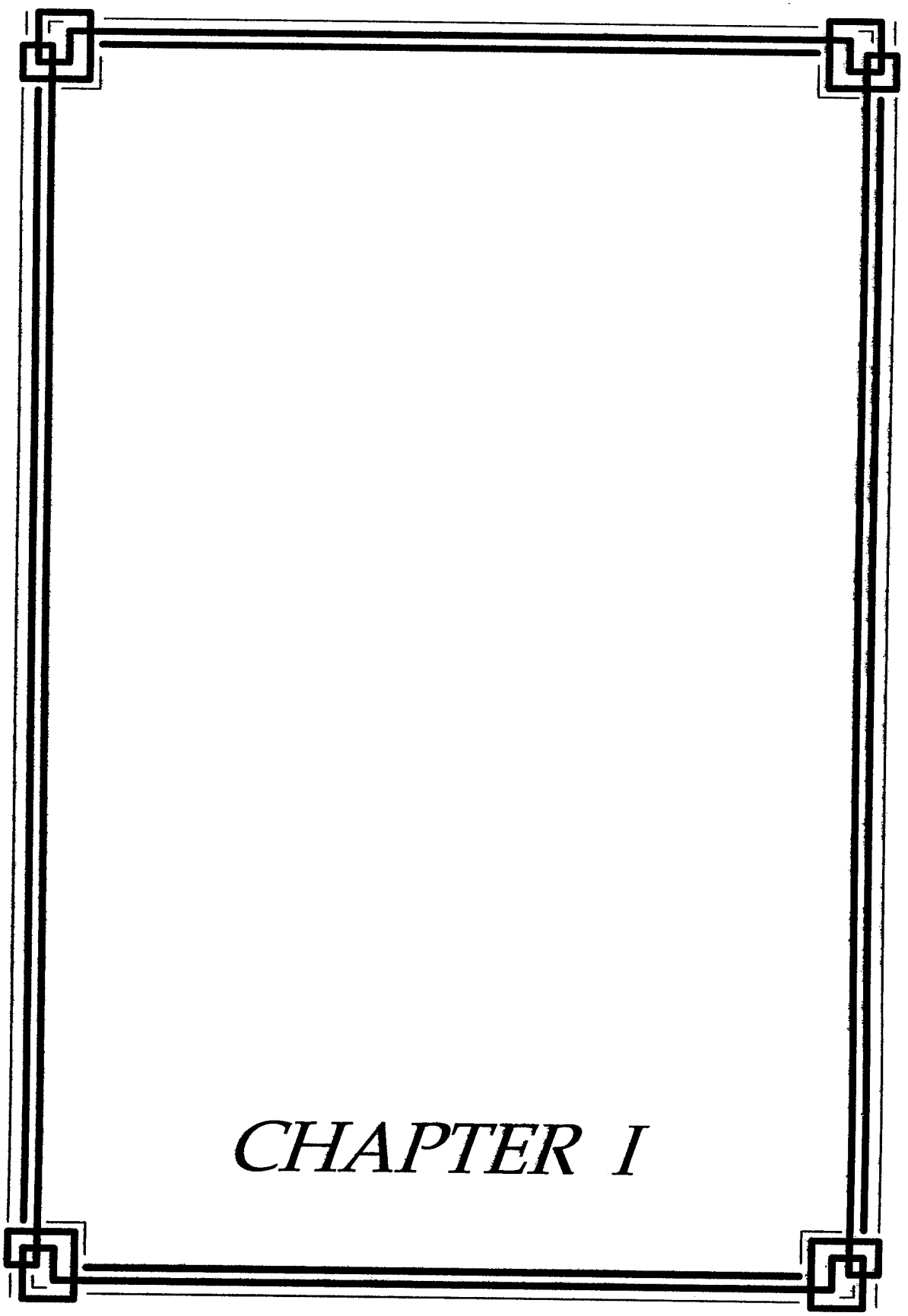
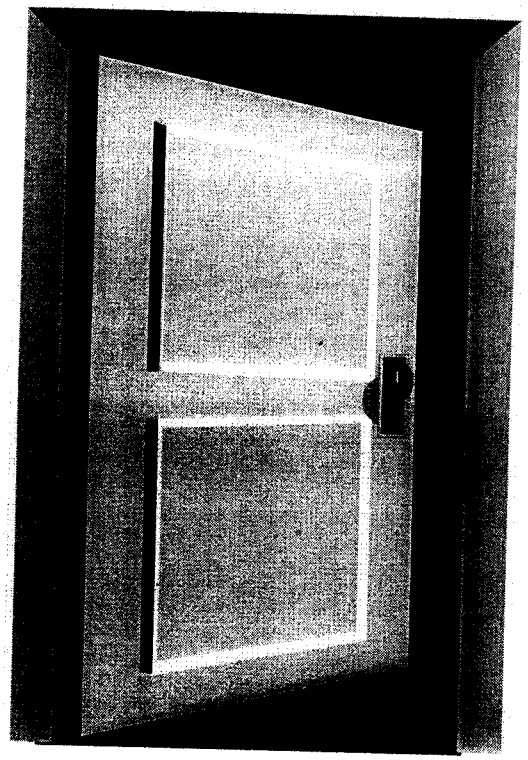
CONTENTS



CHAPTER 1



INTRODUCTION

CHAPTER I

INTRODUCTION

In this modern era of evergrowing electronics and telecommunication, telephone line communication is one of the most reliable forms of communication. Many times, need may arise to switch on or off a light, a fan or a coffee maker at home from office or any other place. The cost incurred is as per standard telephone rates.

1.1 BUILDING BLOCK OF A TELEPHONE:

A Telephone consists of seven main components.

1. Receiver
2. Transmitter
3. Speech network
4. Hook switch
5. Ringer
6. Dialer
7. Bridge rectifier

The block diagram in Fig 1.1 illustrates the interconnection of the seven main components within a subscriber set. The transmitter and receiver are normally located in the handset section of subscriber set. The transmitter converts user voice signal into electrical signals that are transmitted to the local switching center. The

receiver converts electrical signal into sound. The signal at the receiver consists of the voice band signals from the switching center and attenuated feedback from the transmitter. The feedback or "**SIDETONE**" function is performed by the speech network. The speech network also provides for separation of the transmit and receive signals at the subscriber set. Thus all signals between the switching center and subscriber set may be carried over a single wire pair.

The hook switch may be in either of two positions, on-hook or off-hook. These conditions correspond to idle and busy circuits respectively, with the off-hook condition normally activated by lifting the handset. When the handset is lifted, a current sensing device at the switching center detects the off-hook state. The switching centers logic circuitry will then turn off any ring signal and prepare to send and receive voice communication. If the subscriber is placing the call, the switching center will prepare to accept dial signals. The hook switch connects the telephone line to the ringer in an on-hook position and to the speech network in an off-hook position. In the off-hook position, the subscriber set circuitry receives a DC bias from the power supply at the switching center. In the on-hook position, a ring signal may be initiated by a caller. An electrical signal of about 75V and 20-30 HZ is typically generated of the switching center to activate the ringer at a subscriber set. The two methods commonly used to transmit dialling information to the switching center are pulse generation and tone generation. Rotary-type dialers generate pulses

on the line, and these pulses are sensed and counted by the switching center and electronic pulse dialers simulate the mechanical action of rotary dialer. Tone dialers generate tone combination of various frequencies, when electronic dialers are used in subscriber frequencies. When electronic dialers are used in a subscriber set, a bridge rectifier is used to prevent damage to the dialer due to line reversal. The bridge provides the dialer with the proper polarity of the DC line bias.

The simplest type of dialer in use today is the pulse dialer, which uses a series of pulses to transmit dial signals to the control office. The dial signal shown in Fig.1.2 has to make, break inter digit intervals that constitute the digits. There is one another dialling method which is called DUAL TONE MULTI FREQUENCY (DTMF) shown in Fig.1.3. The DTMF address signalling is used by the telephone industry to signal over the voice transmission path of a telephone system. DTMF signal has various advantages over pulse signalling, such as faster dialling speeds and the ability to signal over any voice grade transmission path.

1.2. PARAMETERS OF TELEPHONE

1.2.1 DC VOLTAGE

When the handset is in on-hook position the voltage across the telephone line is between 25 and 48 v. When the handset is in off-hook position the voltage across the telephone line is between 6 and 10 V.

1.2.2 LINE CURRENT

When the telephone is in off-hook the current drawn by the telephone is about 50-60mA.

1.2.3. RINGER

The ringer potential is about 75V.

1.2.4. DTMF DIALLING

This method of signalling uses 16 distinct voice based frequencies each consisting of two sinusoidal signals. One from a "low group" and one from a "high group" of frequencies. The characters that represent these DTMF signals are shown in Table 1.1.

1.2.5. PULSE DIALLING

Pulse dialers must have the following characteristics.

a) The dial pulse signal should consist of sequence of momentary breaks in the telephone loop current corresponding to the numerical value of each digit, except digit '0', which should be represented by 10 break intervals

b) For an automatic dialer, the make time should be between 32 and 35ms,break time between 65 and 68 ms, with interdigit period (IDP) of 720 and 880 ms.

1.2.6. SPECIAL KEY

PAUSE:

This key is used to introduce additional delays between two digits. The delay should be within 2 to 2.4 sec.

FLASH

This key produces a loop break, the duration of which is between 280 and 320ms.

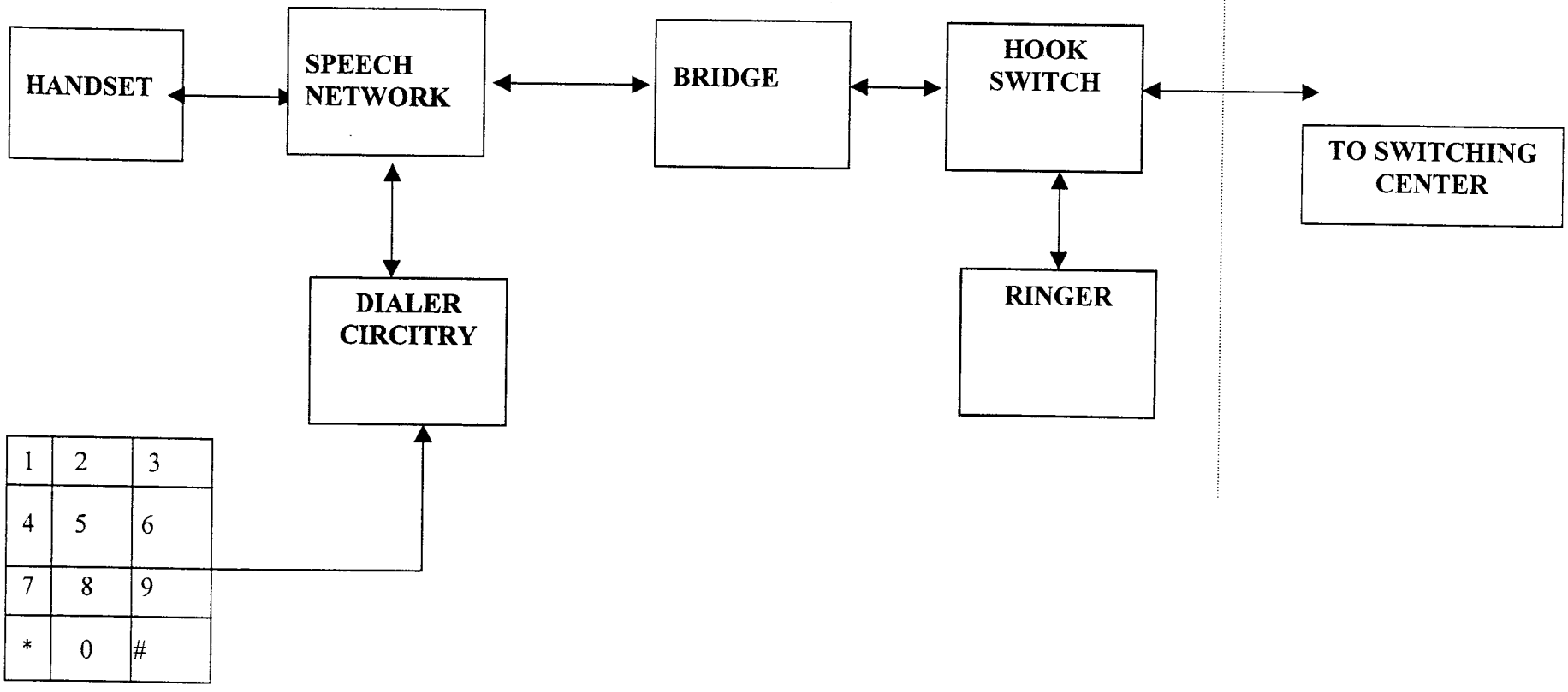


FIG. 1.1. BLOCK DIAGRAM OF TELEPHONE

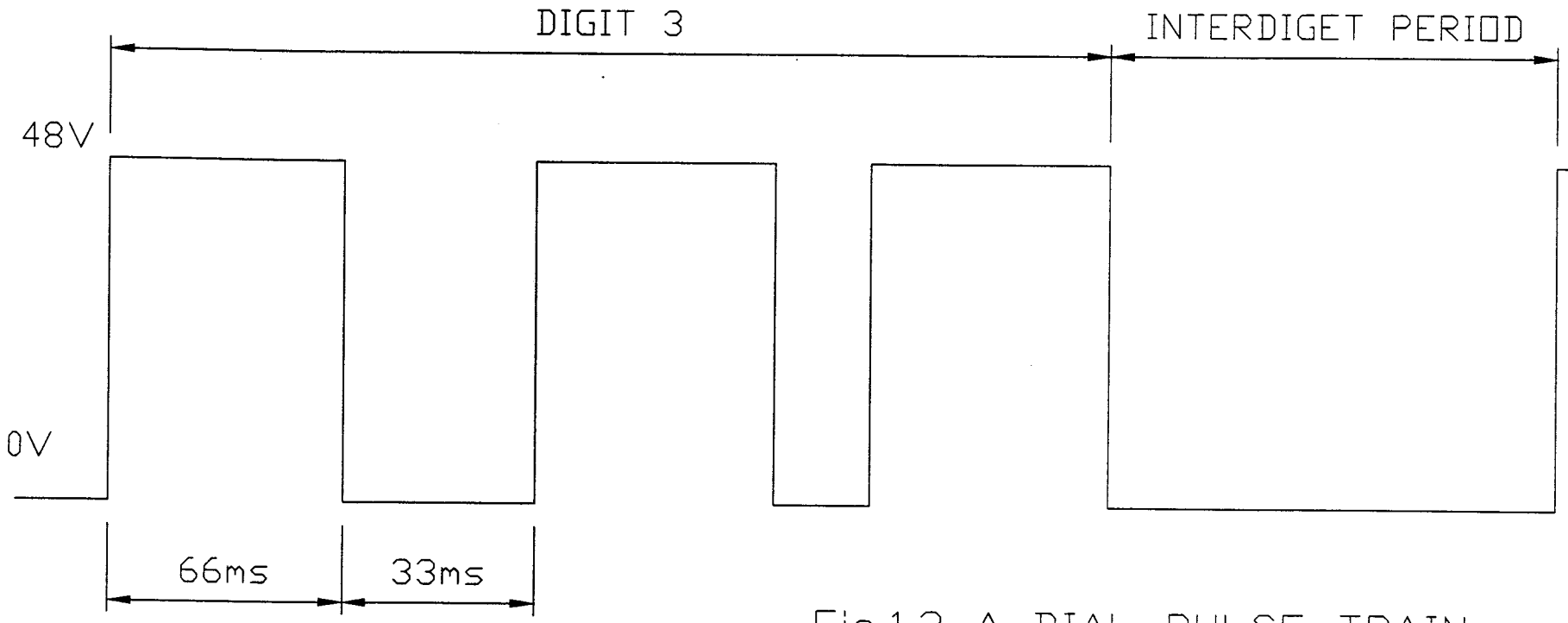


Fig.1.2 A DIAL PULSE TRAIN

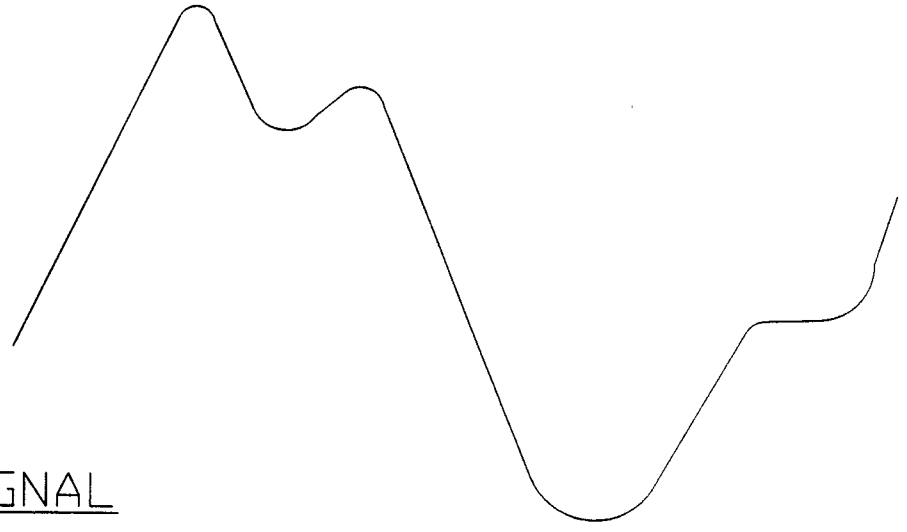


Fig.1.3. DTMF SIGNAL

NORMAL LOW GR PUP FREQUENCES (HZ)	NORMAL HIGH GROUP FREQUENCES (HZ)			
	1209	1336	1447	1663
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

TABLE 1.1 DTMF FREQUENCES

CHAPTER II

BLOCK DIAGRAM

CHAPTER -II

BASIC BLOCK DIAGRAM

The basic block diagram is shown Fig 2.1.

OPERATION:

The telephone number of the called terminal is dialed from the calling terminal. The central circuit is connected to the called terminal. Now as soon as the ring sound is heard the 'appliance mode' operation is selected using 'digit 0' in the telephone keyboard of the calling terminal. After selecting the appliance mode the corresponding digit of the electrical appliance, which is to 'ON' or 'OFF', is pressed from the calling terminal. This number (digit) is processed by the control unit and the output is used to energise a relay corresponding to the appliance which is of interest. This inturn switches the particular appliance on or off.

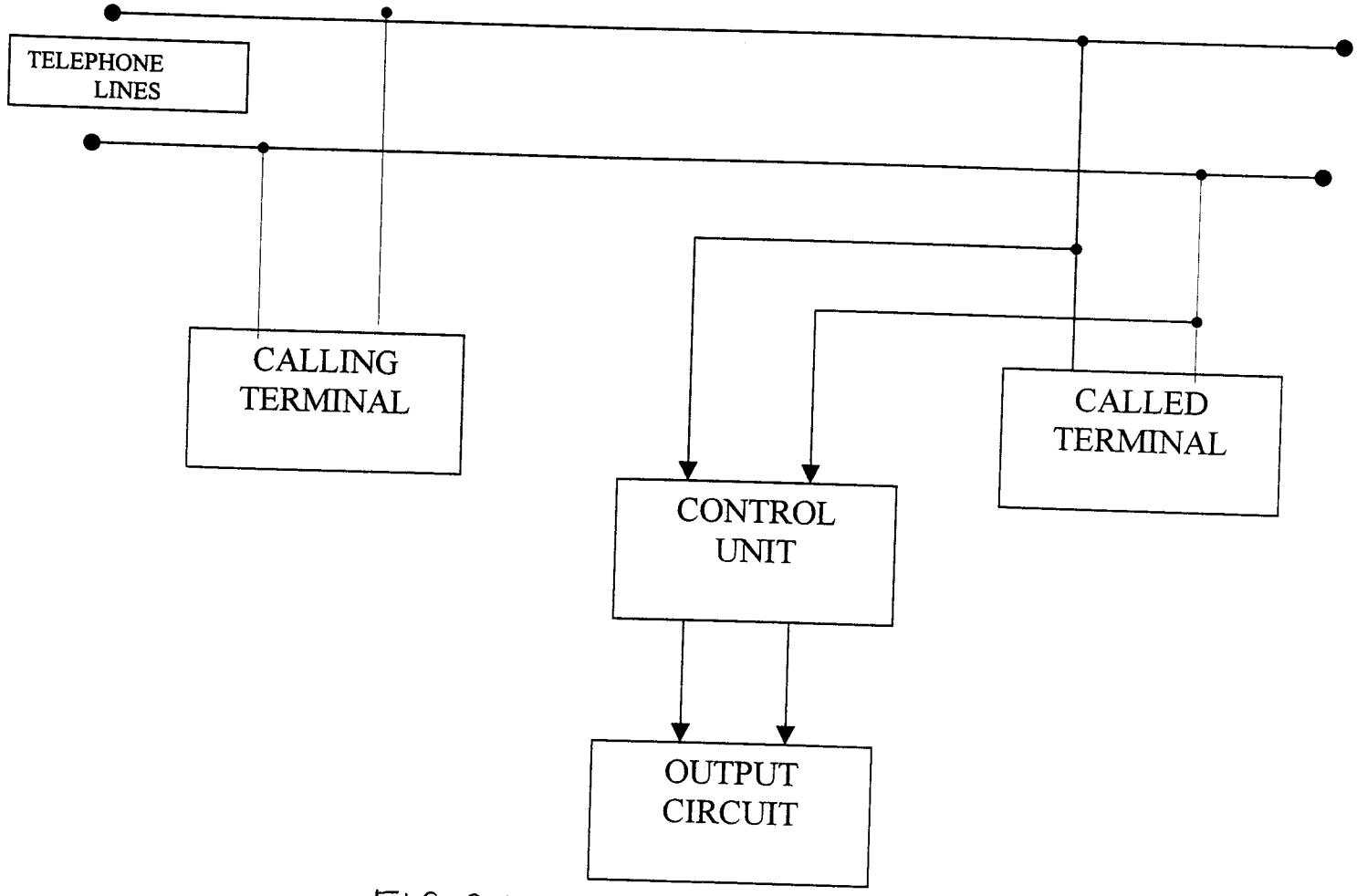


FIG 2.1 BASIC BLOCK DIAGRAM

CHAPTER III

CIRCUIT DIAGRAM

CHAPTER - III

CIRCUIT DIAGRAM

The teleremote circuit shown in Fig 3.1. enables switching 'ON' and 'OFF' of appliances through telephone lines. The circuit is to be connected paralled to the telephone instrument.

The circuit described here can be used to switch upto nine appliances corresponding to the digits 1 through 9 of the telephone key-pad). The DTMF signals on telephone instrument are used as control signals. The digit '0' in DTMF mode is used to toggle between the appliance mode and normal telephone operation mode.

The circuit IC CM 8870 is an DTMF to BCD convertor. Once a call is established (After hearing ring-back tone), dial '0' in DTMF mode. IC 8870 decodes this as '1010' which is further demultiplexed by 74154 IC (4 to 16 line demultiplexer). The active low output of after inversion by an inverter gate IC CD 4049 becomes logic 1. This is used to toggle flip-flop-1 and relay RL1 is energised. Relay R21 has two changeover contacts, RL1 (a) and RL1(b). The RLI (a) contact inject a 10KHZ tone on the line, which indicates to the caller that appliance mode has been selected. The 220-Ohm loop disconnects the ringer from the telephone line in the exchange.

After selection of appliance mode of operations, if digit '1' is dialed, it is decoded by IC8870 and its output is '001'. This is BCD code is then demultiplexed, inverted and is used to toggle the corresponding flipflop to alternate state. The flipflop output is used to drive corresponding relay which can switch 'ON' or switch 'OFF' the appliance connected to it.

Once the switching operation is over, the 220 - ohm loop resistance and 10 KHz tone needs to be removed from the telephone line. To achieve this, digit '0' (in DTMF mode) is dialed again to toggle flip flop -1 to deenergise relay RL1, which terminates the loop on line and 10kHz tone is also disconnected.

3.1 DEMULIPLEXERS

A demultiplexer basically reverses the multiplexing function. It takes data from one line and distributes them to a given number of outout lines. The input data line goes to all of the AND gates. The select gate enable only one gate at a time and the data appearing on the input line will pass through the selected gate to the associated output line.

3.1.1 74154 DEMULTIPLEXER.

The 74154 is a TTL MSI demultiplexer. The logic diagram is shown in Fig 3.2.

Each input is connected to the inpout of only one inverter. There is also an enable function provided on this particular device which is implemented with a NOR gate used as negative AND. A low level on each input, G1, and G2, is required in

order to make the enabel gate output (G) HIGH. The enable gate output is connected to an input of each NAND gate, so it must be HIGH for the gates to be enabled. If the enable gate is not activated then all 16 demultiplxer output will be HIGh regardless of the states of the four input variables A, B, C and D.The logic sysmbol of 74154 is shown in fig 3.2

3.2 FLIP- FLOPS

Flip-flops are synchronous bistable devices. The term synchronous means the output changes state only at a specified point on a triggering intput called the clock (Designated as the control input C); that is, changes in the output occur in synchronization with the clock.There are two types of flip-flops, edge-triggered fliflop and pulse triggered flipflops.

The term edge-triggered means that flip-flop changes state either at the positive edge (Rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of this clock.

3.2.1 D FLIP- FLOP

The D flip-flop is very useful when a single data bit (1 or 0) is to be stored. The D flip-flop is a positive edge-triggered type flip-flop.

The simple addition of an inverter to a S-R flip-flop creates a basic D flip-flop.The logic symbol of a D flip-flop is shown in fig 3.3

This flip-flop has only one input in addition to the clock. This is called the D input. If there is a HIGH on the D input when a clock pulse is applied, the flip-flop will SET. If there is a low on the D input when a clockpulse is applied the flip-flop will RESET, and the low on the D input is thus stored by the flip-flop on the leading edge of the clock pulse.The truth table for a positive edge triggered D flip-flop is given in table 3.1

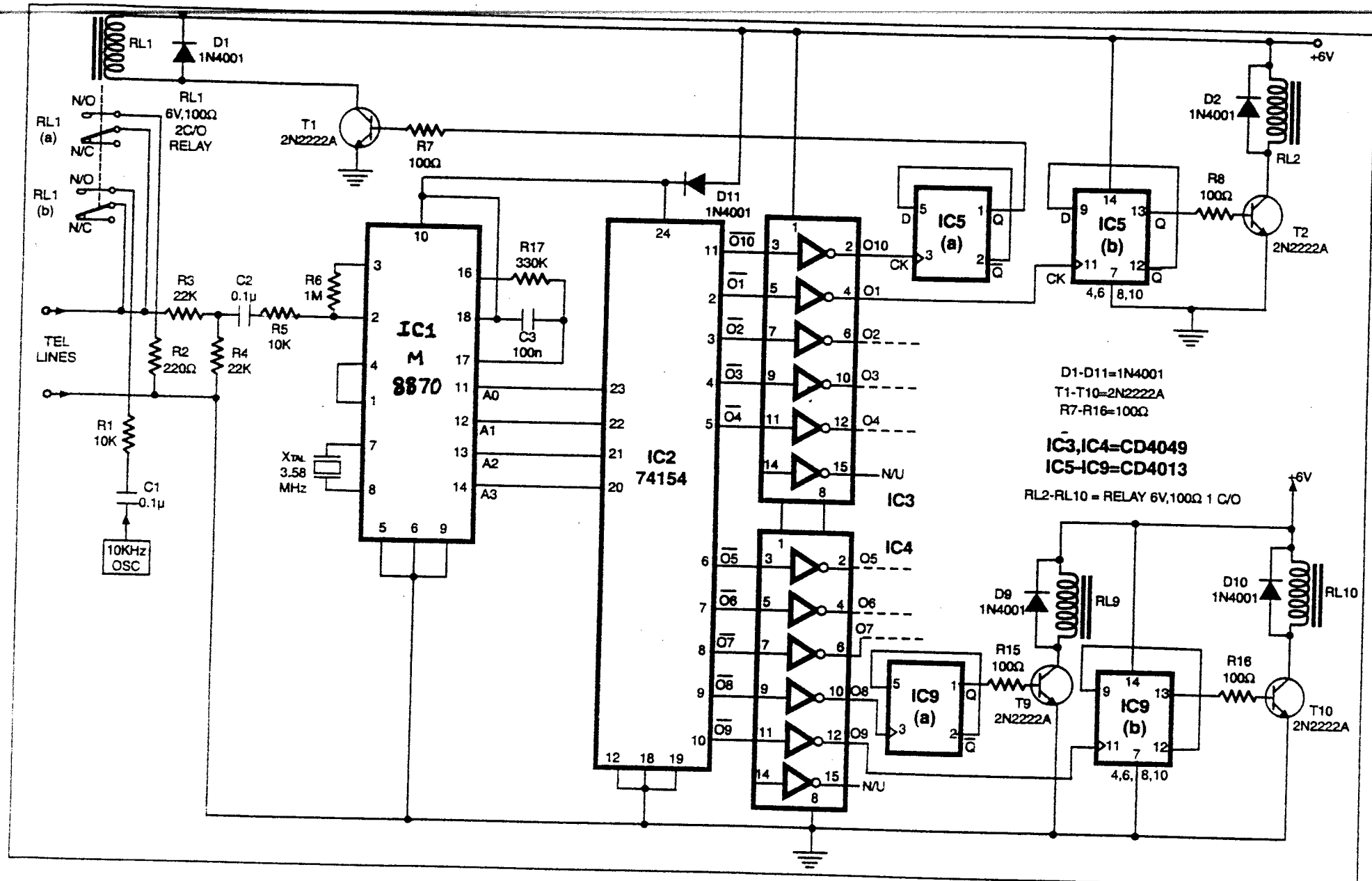


FIG 3-1 CIRCUIT DIAGRAM

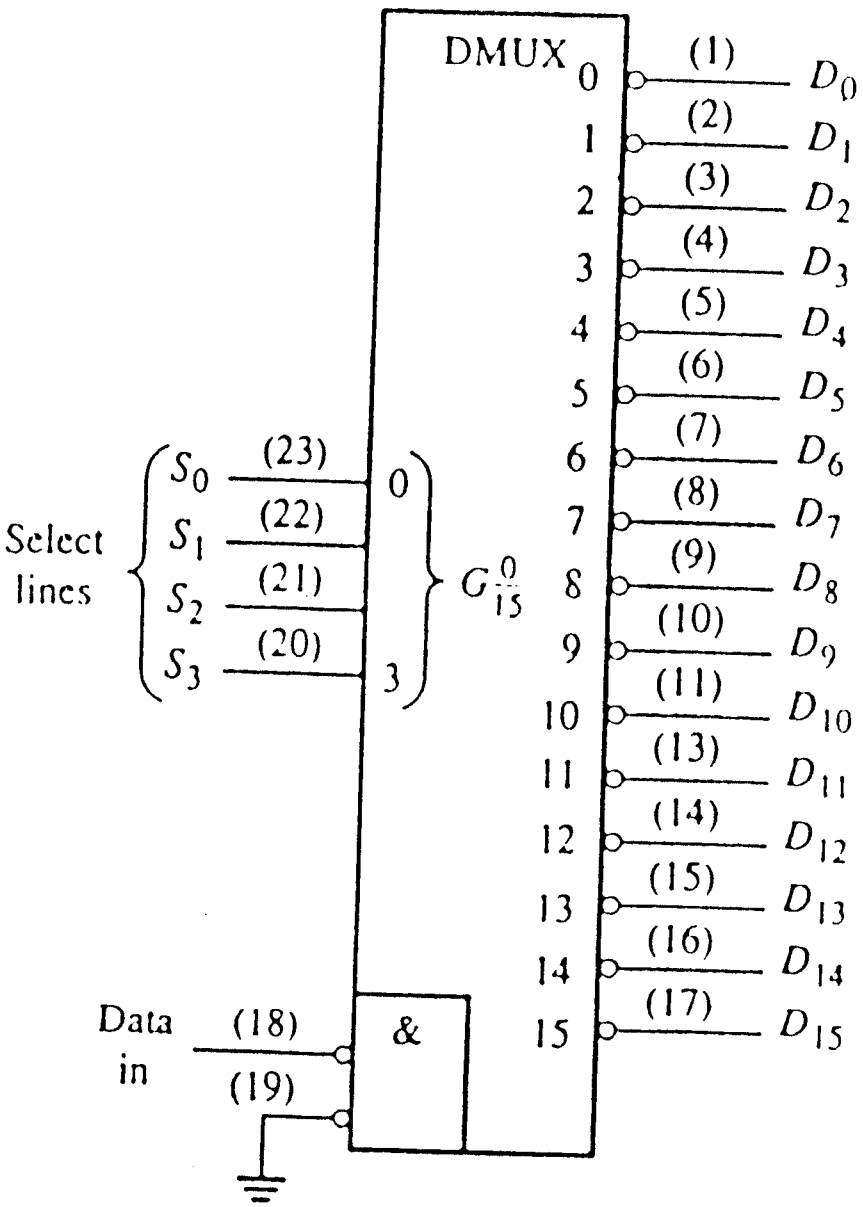


FIG 3.2.a PIN OUT DIAGRAM

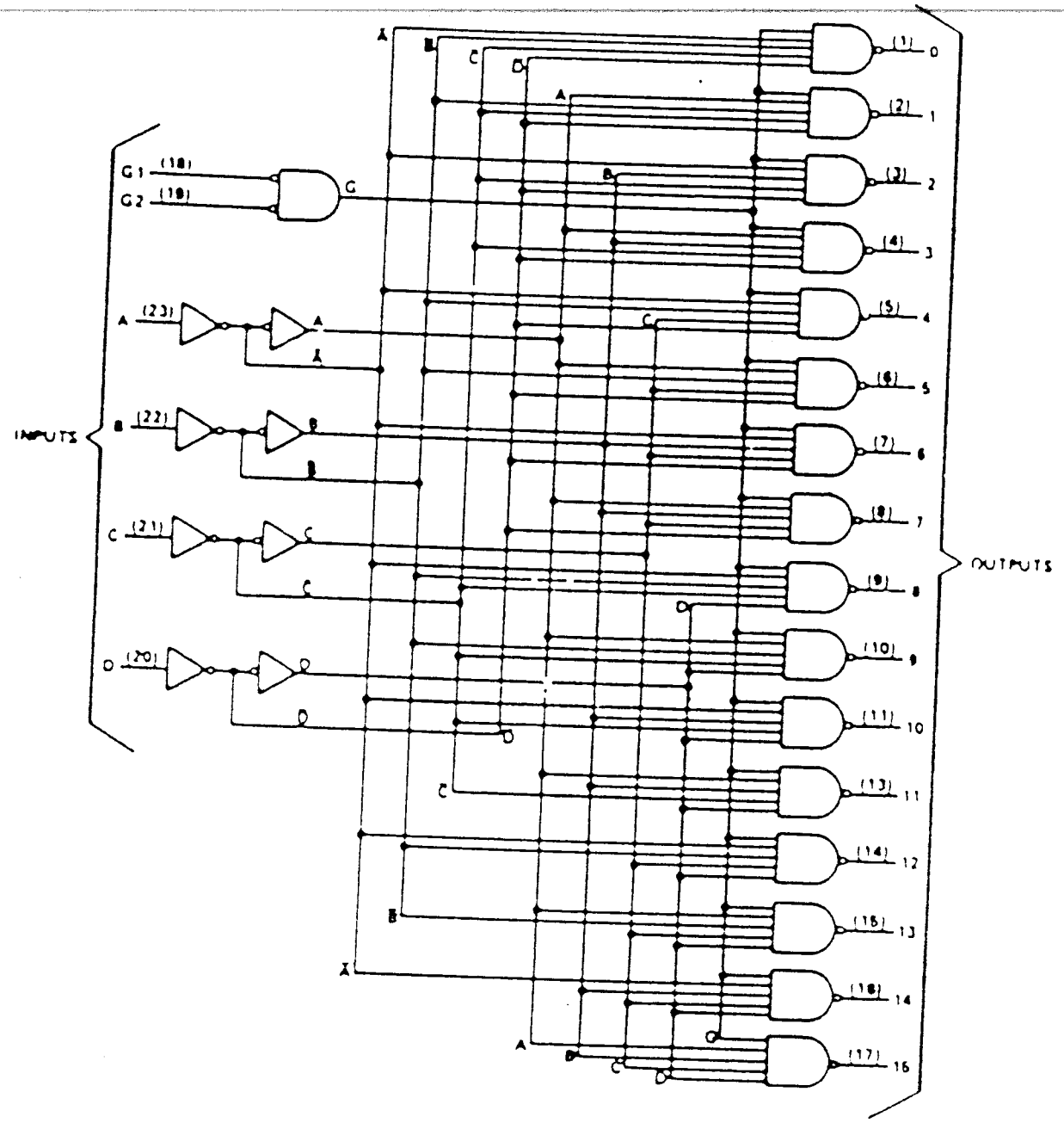


FIG 3.2.6 LOGIC SYMBOL OF 74154-IC

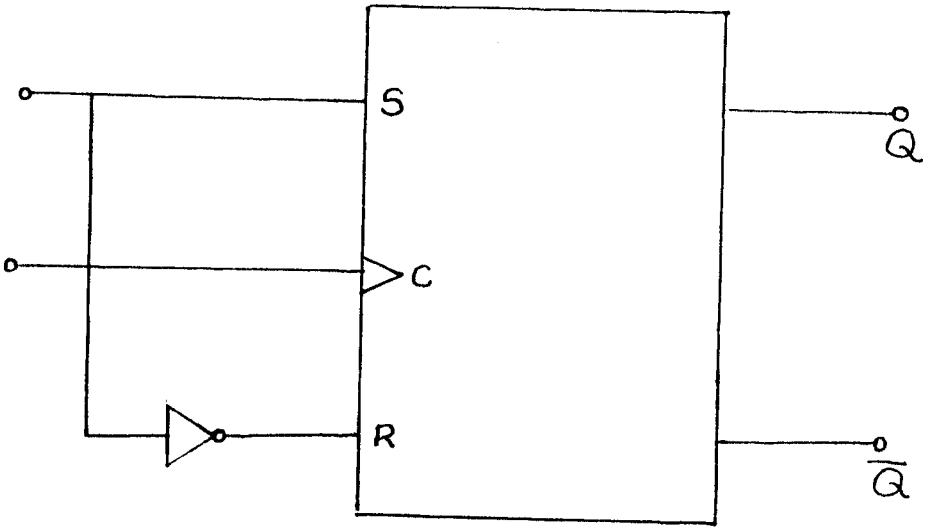


FIG 3.3 LOGIC SYMBOL OF D FLIP-FLOP

INPUTS		OUTPUTS		COMMENTS
D	C	Q	$\overline{Q}$	
1	↑	1	0	SET (STORES 1)
0	↑	0	1	RESET (STORES 0)

TABLE 3.1 TRUTH TABLE

CHAPTER IV

DTMF RECEIVER

CHAPTER - IV

M-8870 DTMF RECEIVER

4.1. INTRODUCTION:

The teletone converter M-8870 is a full DTMF receiver that integrates both bandsplit filter and decoder functions into a single 18-pin DIP package, manufactured using CMOS technolog. The M-8870 offers low power consumption (35MW max) and precise data handling. Its filter section uses switched capacitor technology for both the high and low group filters and for dial tone rejection. Its decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by provision of an on chip differential input amplifier, clock generator and latched tristate interface bus. Minimal external components required include a low cost 3.579545 MHZ color burst crystal, a timing resistor and a timing capacitor.

The M-8870-02 and M-8870-03 provide a "POWER - DOWN" option which, when enabled, drops consumption to less than 0.5 mW. The -02 and -03 versions can also inhibit the decoding of fourth column digits. The -03 version features increase input sensitivity.Pin configuration of M-8870 is shown in fig 4.1. and pin connections are shown in fig 4.2.

FEATURES

* Low power consumption
* Adjustable acquisition and release times
* Central office quality and performance
* Power down and inhibit modes (-02 and -03 versions)
* Inexpensive 3.58 Mhz time base single 5V power supply
* Dial tone suppression

4.2. APPLICATIONS

* Telephone switch equipment
* Mobile radio
* Remote control
* Remote data entry
* Paging system
* Personal computers
* Telephone answering machines
* Credit card systems

4.3. FUNCTIONAL DESCRIPTION

Fig 4.3. is the functional block diagram of M-8870. M-8870 operating functions include a bandsplit filter that seperates the high and low tones of the received pair, and a digital decoder that verifies both the frequency and duration of the received tones before passing the resulting 4 bit code to the output bus.

4.3.1. FILTER

The low and high group tones are separated by applying the dual tone signal to the inputs of two 6th order switched capacitor bandpass filters with bandwidths that corresponds to the bands enclosing the low and high group tones. The filter also incorporates notches at 350 and 440 HZ, providing excellent dial tone rejection. Each filter output is followed by a single order switched capacitor sect on that smoothes the signals prior to lifting. Signal limiting is performed by high gain comparators provided with hysteresis to prevent detection of unwanted low-level signals and noise. The comparator outputs provide full rail logic swings at the frequencies of incoming tones.

4.3.2. DECODER

The M-8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while tolerating small frequency variations. The algorithm ensures an optimum combination of immunity to talk off and tolerance to interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signals condition") , it raises the early steering flag (Est.). Any subsequent loss of signal condition will cause Est. to fall.

4.3.3. STEERING CIRCUIT

The steering circuit of M-8870 is shwn in fig 4.4.Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as "character recognition-condition"). This check is performed by an external RC time constant drive by Est. A logic high on Est causes Vc to rise as the capacitor discharges. Provided that signal condition is maintained (Est remains high) for the validation period (tGTF), Vc reaches the threshold (VIST) OF THE STEERING LOGIC TO REGISTER THE TONE PAIR,THUS LATCHING is corresponding 4-bit code into the output latch.At this point the GT output is activated and driven Vc to Vdd.GT continues to drive high as long as Est.remains high.

Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (STD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the tree state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the ability to select the steering time constant externally, allows the designer to tailor performance to meet a wide variety of system requirements.

4.3.4. GUARD TIME ADJUSTMENT

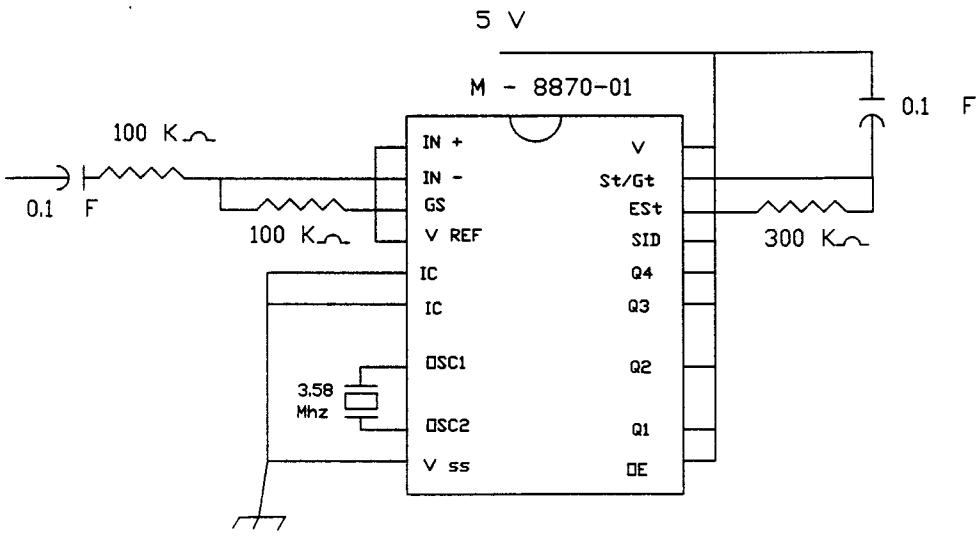
The guard time adjustment circuit is shown in fig 4.5. Where independent selection of signal duration and inter digit pause are not required, a simple steering circuit is applicable. Competent values are chosen according to the formula. tREC = tDP + tGTP tQTP =0.67 RC. The value of tDP is a parameter of the device and TREC is the minimum signal duration to be recognised by the receiver. A value for C of 0.1 microFarad is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a tREC of 40ms would be 300k ohm. The timing for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard times for tone-present (tGTP) and tone-absent (tGTA). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off performance. Since it reduces the probablity that tones simulated by speech will maintain signal condition long enough to be registered. On the other hand, a relatively short tREC with long tDO would be appropriate for extremely noisy enviornments where fast acquisition time and immunity to dropouts would be required. A logic high applied to pin 6 (PD) will place the device into standby mode to minimize power consumption . It stops the oscillator and the functioning of the filters. On -01 models, this pin is tied to ground (logic low).

4.3.5. TONE DECODING:

Inhibit mode is enabled by a logic high input to pin 5 (INH). It inhibits the detection of 1633 HZ. The output code will remain the same as te previous detected code. On -01 models, this pin is tied to ground (logic low). The input arrangement of the M-8870 provides a differential input operational amplifier as well as bias source (VREF) to bias the inputs at mid-rail. Provision is made for connection of feed back resistor to the op-amp output (GS) for gain adjustment.

4.3.6. DTMF CLOCK CIRCUIT:

The internal clock circuit is completed with the addition of a standard 3.579545 MHZ television color burst crystal. The crystal can be connected to a single M-8870s or a series of M-8870S - A single crystal can be used to connect a series of M-8870 by coupling the oscillator output of each M-8870 through a 30 PF capacitor to the oscillator input of the next M-8870.



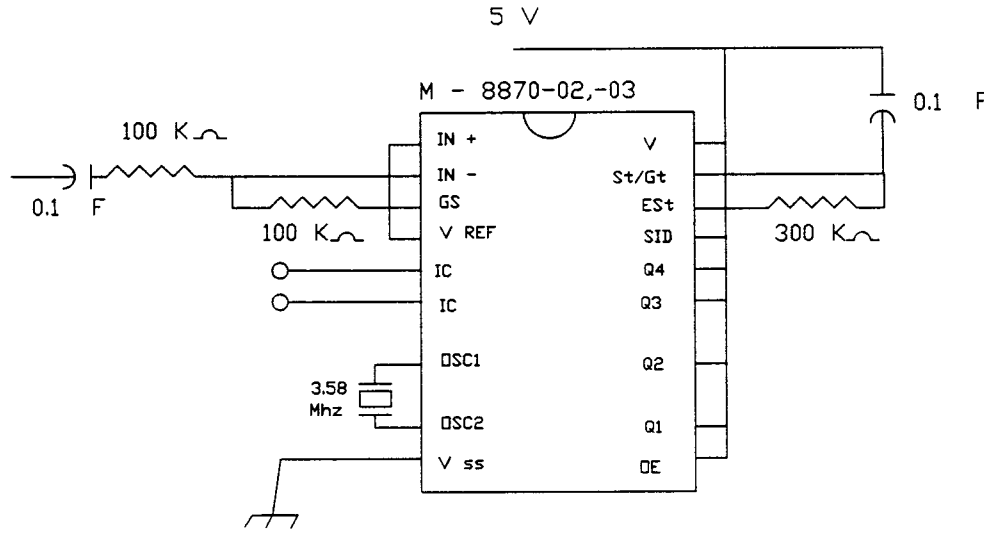


Fig 4.1 SINGLE ENDED INPUT CONFIGURATION

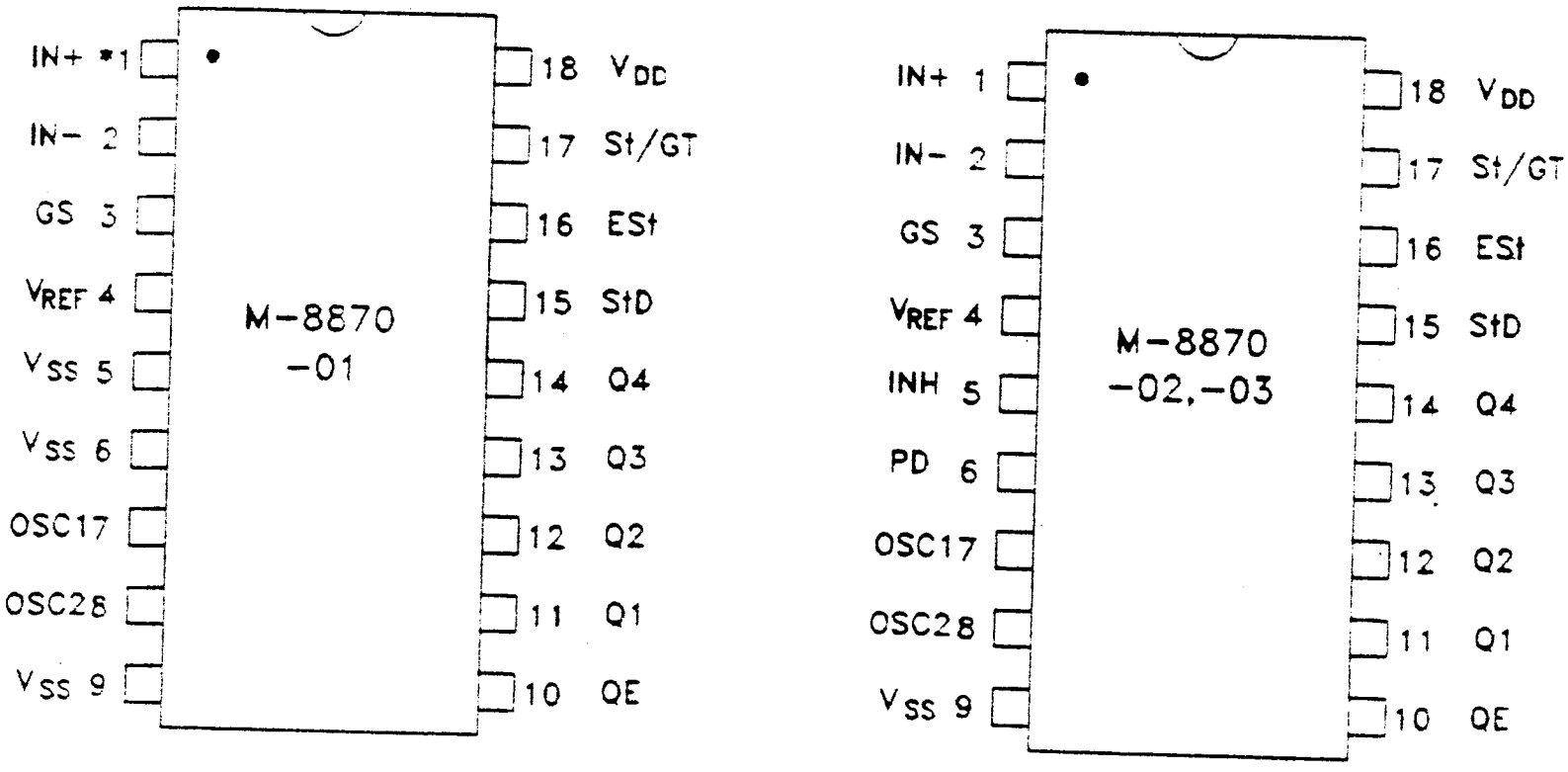


FIG 4.2 PIN CONNECTIONS

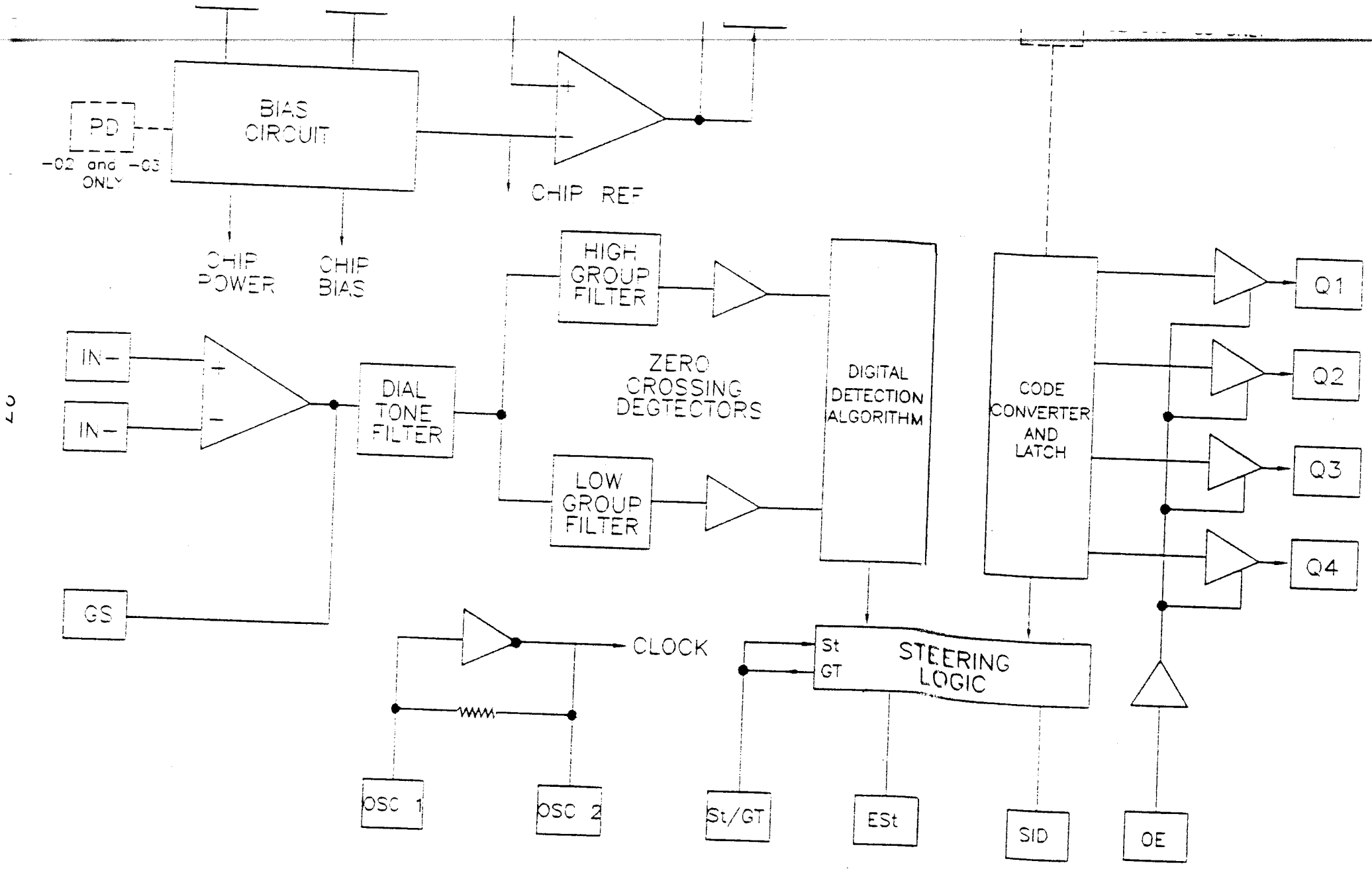
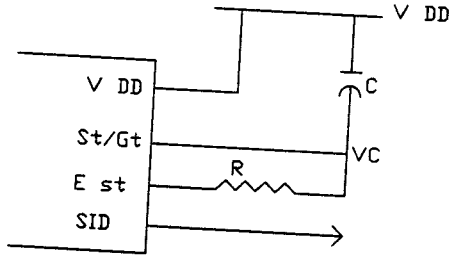


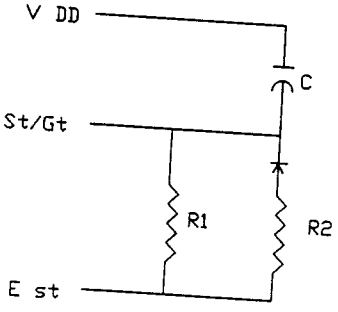
FIG 4.3 BLOCK DIAGRAM



$$t_{GTA} = RC \ln\left(\frac{V_{DD}}{V_{TST}}\right)$$

$$t_{GTP} = RC \ln\left(\frac{V_{DD}}{V_{DD} - V_{TST}}\right)$$

Fig 4.4 BASIC STEERING CIRCUIT

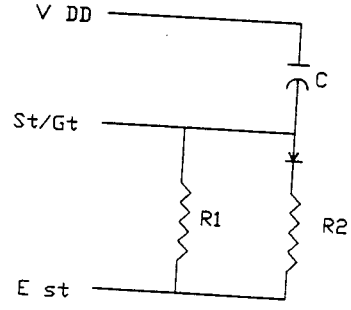


$$t_{GTP} = R_{pc} \ln\left(\frac{V_{DD}}{V_{DD} - V_{TST}}\right)$$

$$t_{GTA} = R_{1c} \ln\left(\frac{V_{DD}}{V_{TST}}\right)$$

$$R_p = \frac{R1\ R2}{R1+R2}$$

DECREASING t_{GTE} $(t_{GTP} < t_{GTP})$



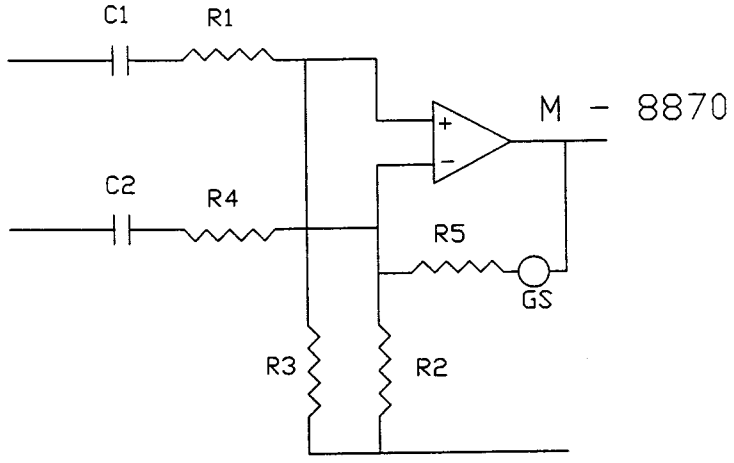
$$t_{GTP} = R_{1c} \ln\left(\frac{V_{DD}}{V_{DD} - V_{TS}}\right)$$

$$t_{GTA} = R_{pc} \ln\left(\frac{V_{DD}}{V_{TST}}\right)$$

$$R_p = \frac{R1\ R2}{R1+R2}$$

DECREASING t_{GTA} $(t_{GTP} > t_{GTP})$

Fig4.5. GUARD TIME ADJUSTMENT



DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2 = 10nF$

$R_1 = R_4 = R_S = 100K\Omega$

$R_2 = 60K\Omega \quad R_3 = 37.5K\Omega$

$$R_3 = \frac{R_2 R_3}{R_2 + R_3}$$

VOLTAGE GAIN (Av diff) = $\frac{R_5}{R_1}$

INPUT IMPEDANCE:

$$Z_{IN\ DIFF} = 2\sqrt{R_1^2 + \left(\frac{1}{wc}\right)^2}$$

Fig 4.6 DIFFERENTIAL INPUT CONFIGURATION

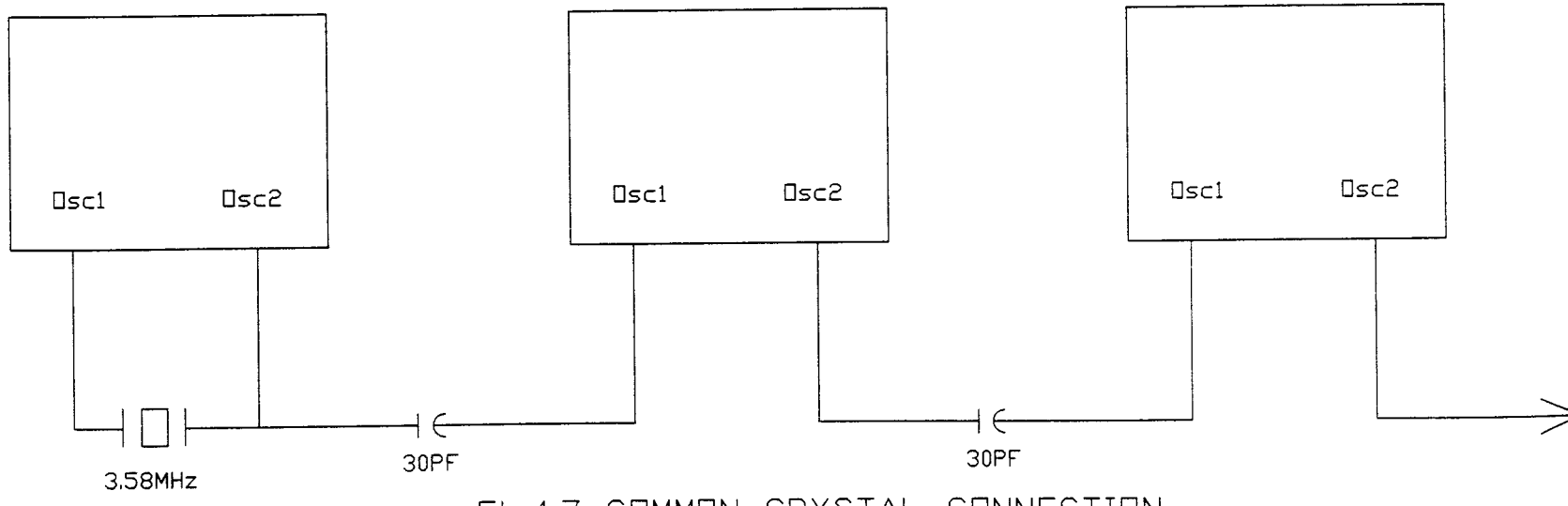


Fig4.7 COMMON CRYSTAL CONNECTION

CHAPTER V

FABRICATION & TESTING

CHAPTER -V

FABRICATION AND TESTING

The layout for the entire circuit is shown in fig 5.1. PCB fabrication is done for the entire circuit. The advantage of PCB is that the component can be fixed and connected as compact as possible. Hence the size of the circuit will be minimum. Risk of short circuit done due to running of the wires for connecting. The components is avoided. The circuit has been tested using the telephone connection in the college.

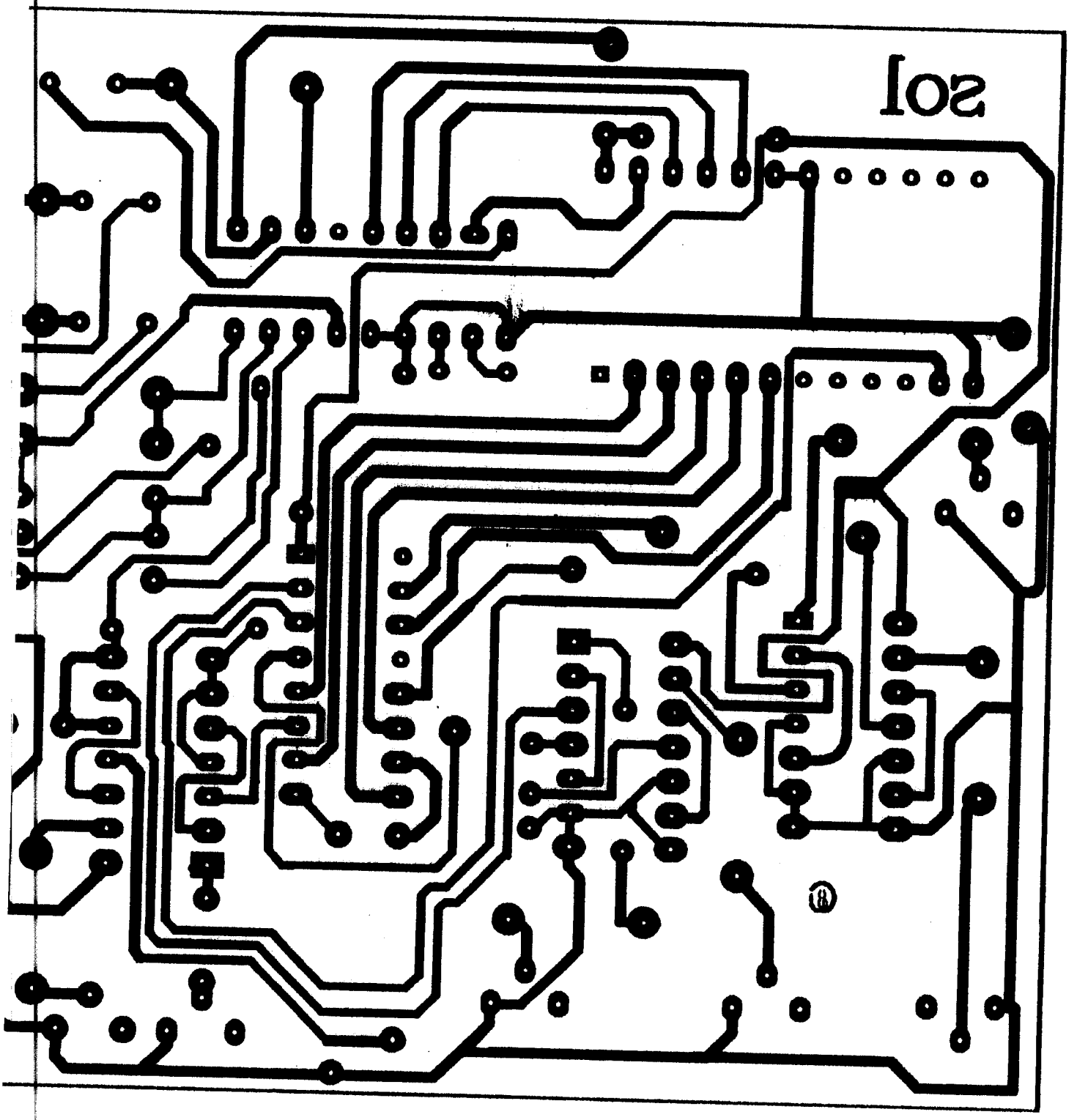
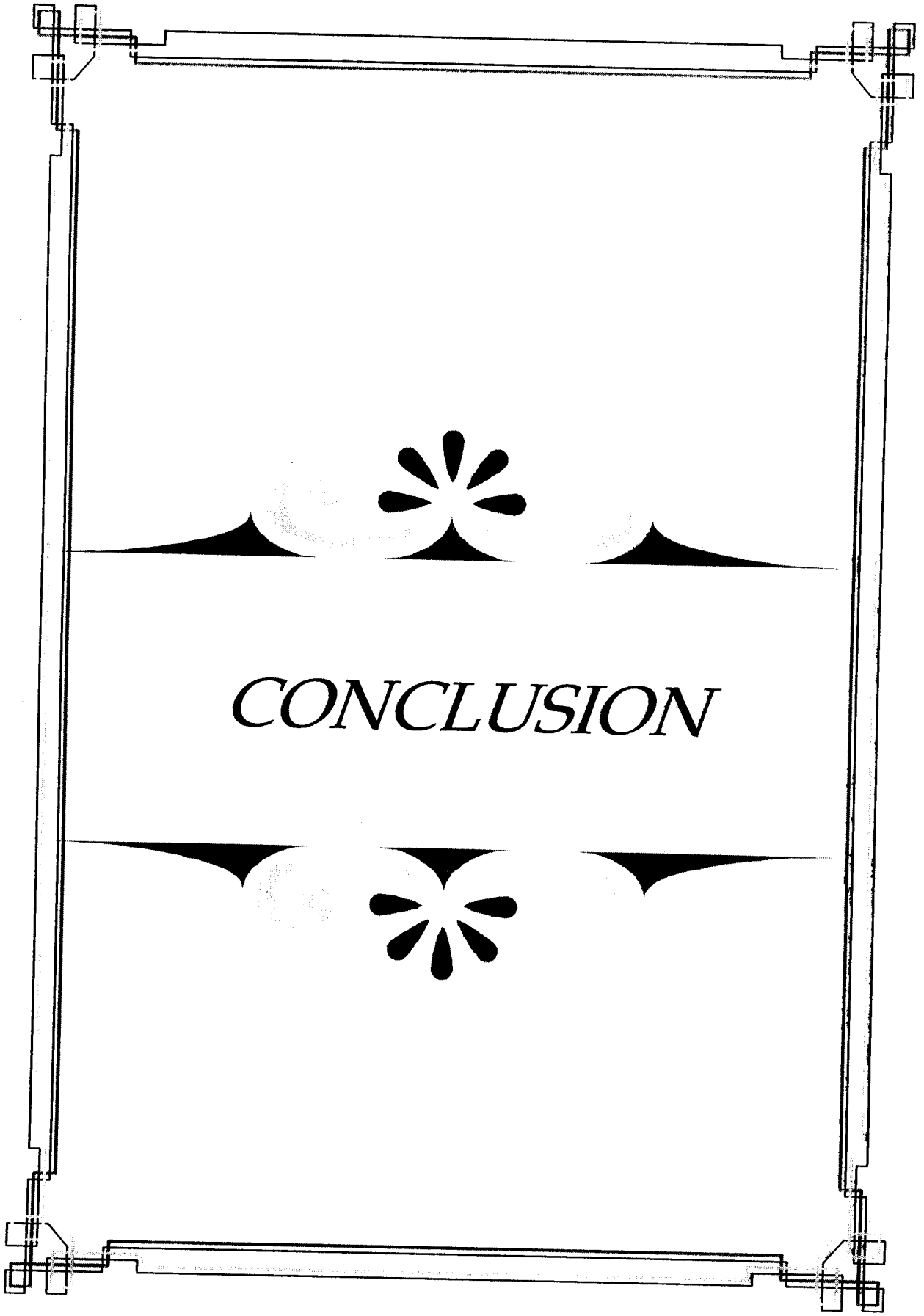


FIG 5.1 PCB LAYOUT

CHAPTER VI



CONCLUSION

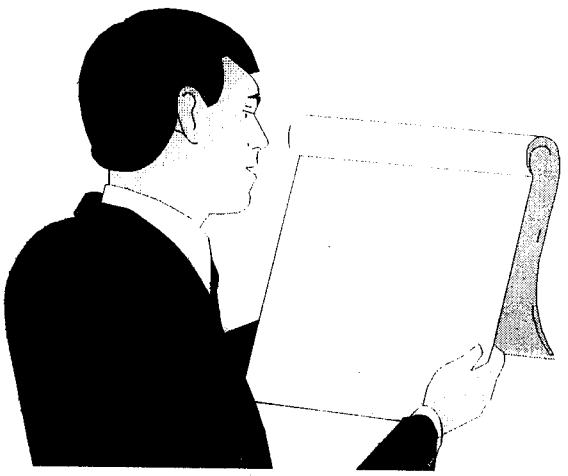
CHAPER-VI

CONCLUSION

In this project a Teleremote control unit has been constructed and tested. This unit can be used to control 9 electrical appliances from remote place through telephone. The electrical appliances are interfaced via relays.

The access code used in this project is an one digit number. By using 2 or 3 digit code number, many number of appliances may be controlled from remote place.

Test results indicate that the unit operates correctly.



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REFERENCES

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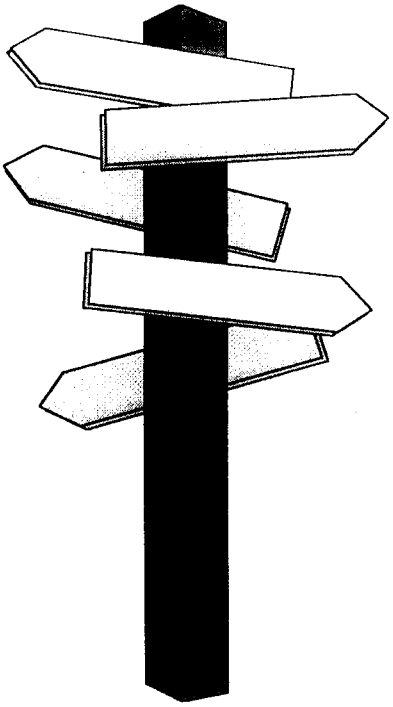


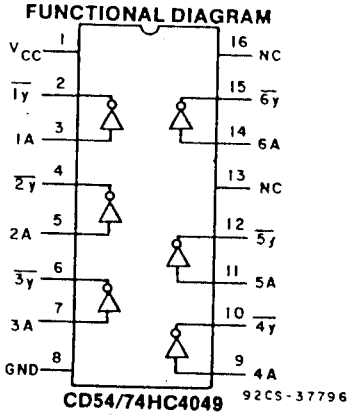
APPENDIX

CD54/74HC4049
CD54/74HC4050

File No. 1543

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC4049 92CS-37796

Hex Buffers, Inverting and Non-Inverting

Type Features

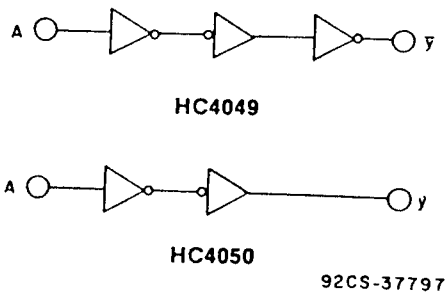
- *Typical propagation delay = 6 ns @ V_{CC} = 5 V, C_L = 15pF, T_A = 25°C*
- *High-to-low voltage level converter for up to V_I = 16 V*

The RCA-CD54/74HC4049 and CD54/74HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which will convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 0-V to 15-V input logic levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from both positive and negative electrostatic discharge. These parts can also be used as simple buffers or inverters without level translation. The CD54/74HC4049 and CD54/74HC4050 are enhanced versions of equivalent CMOS types.

The CD54HC4049 and CD54/74HC4050 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix) and in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

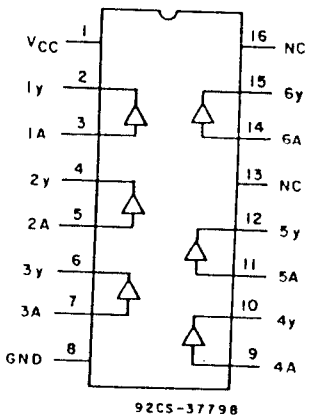
Family Features

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, V_{CC}, N_{IH} = 30% V_{CC}; @ V_{CC} = 5 V



LOGIC DIAGRAMS

FUNCTIONAL DIAGRAM



CD54/74HC4050

CD54/74HC4049
CD54/74HC4050

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CD54/74HC4049, CD54/74HC4050											UNITS
		TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES			
					+25°C			-40/ +85°C		-55/ +125°C			
		V_I V	I_O mA	V_{CC} V	Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
High-Level Input Voltage	V_{IH}			2	1.5	—	—	1.5	—	1.5	—		V
				4.5	3.15	—	—	3.15	—	3.15	—		
				6	4.2	—	—	4.2	—	4.2	—		
Low-Level Input Voltage	V_{IL}			2	—	—	0.5	—	0.5	—	0.5		V
				4.5	—	—	1.35	—	1.35	—	1.35		
				6	—	—	1.8	—	1.8	—	1.8		
High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—		V
				4.5	4.4	—	—	4.4	—	4.4	—		
				6	5.9	—	—	5.9	—	5.9	—		
TTL Loads (Standard Output)		V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—		V
			-5.2	6	5.48	—	—	5.34	—	5.2	—		
Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1		V
				4.5	—	—	0.1	—	0.1	—	0.1		
				6	—	—	0.1	—	0.1	—	0.1		
TTL Loads (Standard Output)		V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4		V
			5.2	6	—	—	0.26	—	0.33	—	0.4		
Input Leakage Current	I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1		μA
		15		6	—	—	±0.5	—	±5	—	±5		
Quiescent Device Current	I_{CC}	15 or Gnd	0	6	—	—	2	—	20	—	40		μA

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		SYMBOL	54HC AND 74HC	
			TYPICAL	UNITS
Propagation Delay, Data Input to Output (C_L = 15 pF)	HC4049 HC4050	t_{PLH}, t_{PHL}	6	ns
Power Dissipation Capacitance*		C_{PD}	35	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter
$P_D = V_{CC}^2 f_i(C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

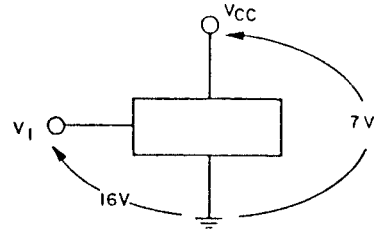
CHARACTERISTIC	SYMBOL	V_{CC}	25° C		-40° C to +85° C		-55° C to +125° C		UNITS
			HC		74HC		54HC		
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay nA to nȲ HC4049 nA to nY HC4050	t_{PLH}, t_{PHL}	2	—	85	—	105	—	130	ns
		4.5	—	17	—	21	—	26	
		6	—	14	—	18	—	22	
Transition Time	t_{TLH}, t_{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C_I	—	—	10	—	10	—	10	pF

CD54/74HC4049
CD54/74HC4050

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}) ..... -0.5 to +7 V
DC INPUT VOLTAGE, (V_I)
(Voltages referenced to ground) ..... -0.5 to +16 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

Voltage Relationships:
(Maximum Positive Limits)



92CS-37799RI

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
DC Output Voltage, V_O	0	V_{CC}	V
DC Input Voltage (V_I)	0	15	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

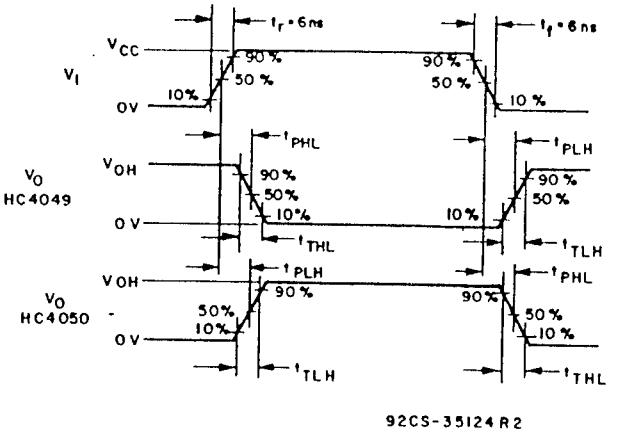
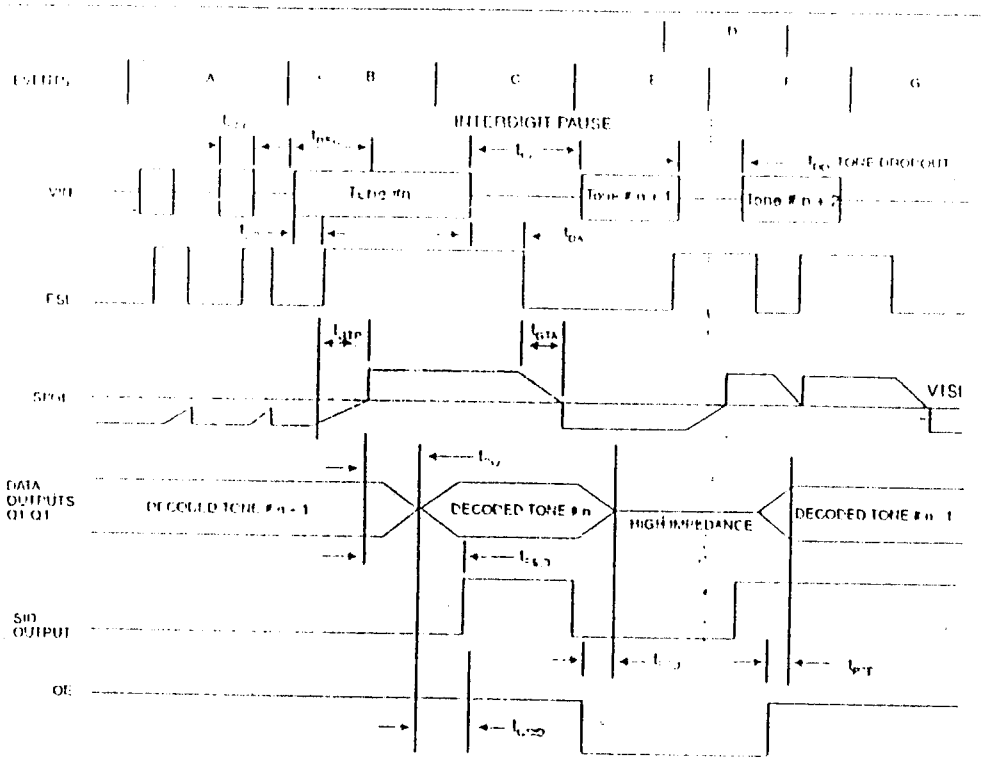


Fig. 1 - Transition times and propagation delay times, combination logic.



Explanation of Events

(A) Tone bursts detected, tone duration invalid, outputs not updated.
(B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
(C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
(D) Outputs switched to high impedance state.
(E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
(F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
(G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

VSI	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
StGt	Steering input/guard time output. Drives external RC timing circuit.
Q1 - Q4	4-bit decoded tone output.
StD	Delayed steering output. Indicates that valid frequencies have been present/absent for the required guardtime, thus constituting a valid signal.
OE	Output enable (input). A low level shifts Q1 - Q4 to its high impedance state.
t_{REC}	Maximum DTMF signal duration not detected as valid.
t_{DP}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid DTMF signals.
t_{TO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect the presence of valid DTMF signals.
t_{DA}	Time to detect the absence of valid DTMF signals.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Table 1 Pin Functions

PIN	NAME	DESCRIPTION	
1	IN+	Non-inverting input	Connections to the front-end differential amplifier
2	IN-	Inverting input	
3	GS	Gain select. Gives access to output of front-end amplifier for connection of feedback resistor.	
4	V_{REF}	Reference voltage output (nominally $V_{DD}/2$). May be used to bias the inputs at mid-rail.	
5	INH*	Inhibits detection of tones representing keys A, B, C, and D.	
6	PD*	Power down. Logic high powers down the device and inhibits the oscillator. Internal pulldown.	
7	OSC1	Clock input	3.579545 MHz crystal connected between these pins completes the internal oscillator.
8	OSC2	Clock output	
9	V_{SS}	Negative power supply (normally connected to 0 V).	
10	OE	Three-state output enable (input). Logic high enables the outputs Q1 - Q4. Internal pullup.	
11 - 14	Q1, Q2, Q3, Q4	Three-state data outputs. When enabled by OE, provides the code corresponding to the last valid tone pair received (see Table 5)	
15	StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V_{TSt}.	
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Figure 7).	
18	V_{DD}	Positive power supply. (Normally connected to +5V.)	
	-01 and -03 only. Connect to V_{SS} for -01 version		

M-8870

Table 5 Tone Decoding

F_{LOW}	F_{HIGH}	KEY (ref.)	OE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
ANY	ANY	ANY	L	Z	Z	Z	Z

= logic low, H = logic high, Z = high impedance

Table 2 Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE
[illegible] supply voltage (V_{DD} - V_{SS})	V_{DD}	6.0 V max
[illegible] any pin	V_{IS}	V_{SS} -0.3, V_{DD} +0.3
[illegible] any pin	I_{DD}	10 mA max
[illegible] temperature	T_A	-40° C to + 85 °C
[illegible] temperature	T_S	-65° C to + 150° C

Table 3 DC Characteristics

PARAMETER	SYMBOL	MIN	‡TYP	MAX	UNITS	TEST CONDITIONS
[illegible] supply	V_{DD}	4.75		5.25	V	
[illegible] current	I_{DD}		3.0	7.0	mA	
[illegible] current (see Note 3)	I_{DD}/Ω			100	µA	PD=V_{DD}
[illegible] dissipation	P_D		15	35	mW	f = 3.579 MHz, V_{DD} = 5.0 V
[illegible] impedance	V_R			1.5	V	
[illegible] voltage	V_{BG}	3.5			V	
[illegible] out	I_{IL}/I_{IH}		0.1		µA	V_{IN} = V_{SS} or V_{DD} (see Note 2)
[illegible] for OE	I_{OZ}		6.5	15.0	µA	OE = 0 V
[illegible] inputs 1, 2	R_{FB}	8	10		MΩ	@ 1 kHz
[illegible] voltage	V_{REF}	2.2		2.5	V	
[illegible] voltage	V_{OH}			0.03	V	No load
[illegible]	[illegible]	4.97			V	No load
[illegible]	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4 V
[illegible] current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
[illegible] V_{REF}	V_{REF}	2.4		2.7	V	No load
[illegible] from V_{REF}	R_{OR}		10		kΩ	

‡Typical figures are at 25° C and are for design aid only: not guaranteed and not subject to production testing.
Notes: 1. All voltages referenced to V_{SS} unless otherwise noted. For typical values, V_{DD} = 5.0V, V_{SS} = 0V, TA = 25°C.
2. Input pins defined as IN_+, IN_-, or OE.
3. Q2 and Q3, only.

Table 4 Operating Characteristics - Gain Setting Amplifier

PARAMETER	SYMBOL	MIN	‡ TYP	MAX	UNITS	TEXT CONDITIONS
[illegible] current	I_{IN}		±100		nA	V_{SS} < V_{IN} < V_{DD}
[illegible] resistance	R_{IN}	4			MΩ	
[illegible] offset voltage	V_{OS}		±25		mV	
[illegible] supply rejection	PSRR	50			dB	1 kHz
[illegible] mode rejection	CMRR	55			dB	-3.0V < V_{IN} < 3.0V
[illegible] open loop voltage gain	A_{VOL}	60			dB	
[illegible] unity gain bandwidth	f_C	1.2	1.5		MHz	
[illegible] voltage swing	V_O	3.5			V_{P-P}	RL ≥ 100 kΩ to V_{SS}
[illegible] capacitive load (GS)	C_L			100	pF	
[illegible] resistive load (GS)	R_L			50	kΩ	
[illegible] mode range	V_{CM}	2.5			V_{P-P}	No load

All voltages referenced to V_{SS} unless otherwise noted. For typical values V_{DD} = 5.0 V, V_{SS} = 0 V, TA = 25° C.
‡Typical figures are at 25° C and are for design aid only: not guaranteed and not subject to production testing.

Table 6 AC Specifications

PARAMETER	SYMBOL	MIN	‡TYP	MAX	UNITS	NOTES
Valid input signal levels (each tone of composite signal) (-01 and -02 only)		-29		+1	dBm	1,2,3,4,5,8
		27.5		869	mVRMS	
Valid input signal levels (each tone of composite signal) (-03 only)		-40		+1	dBm	1,2,3,4,5,8
		7.75		869	mVRMS	
Positive twist accept				10	dB	2,3,4,8
Negative twist accept				10	dB	
Frequency deviation accept limit				±1.5% ± 2 Hz	Nom	2,3,5,8,10
Frequency deviation reject limit		±3.5%			Nom	2,3,5
Third tone tolerance		-25	-16		dB	2,3,4,5,8,9,13,14
Noise tolerance			-12		dB	2,3,4,5,6,8,9
Dial tone tolerance		+18	+22		dB	2,3,4,5,7,8,9
Tone present detection time	t_{DP}	5	8	14	ms	See Figure 7
Tone absent detection time	t_{DA}	0.5	3	8.5	ms	
Minimum tone duration accept	t_{REC}			40	ms	
Minimum tone duration reject	t_{REC}	20			ms	User adjustable (see Figures 2 and 4)
Minimum interdigit pause accept	t_{ID}			40	ms	
Maximum interdigit pause reject	t_{DO}	20			ms	
Propagation delay (St to Q)	t_{PQ}		6	11	µs	OE = V_{DD}
Propagation delay (St to StD)	t_{PStD}		9	16	µs	
Output data setup (Q to StD)	t_{QStD}		4.0		µs	
Propagation delay (OE to Q), enable	t_{PTE}		50	60	ns	R_L = 10kΩ, C_L = 50 pF
Propagation delay (OE to Q), disable	t_{PTD}		300		ns	
Crystal clock frequency	f_{CLK}	3.5759	3.5795	3.5831	MHz	
OSC2 output (OSC2), capacitive load	C_{LO}			30	pF	

All voltages referenced to V_{SS} unless otherwise noted. For typical values V_{DD} = 5.0 V, V_{SS} = 0 V, T_A = 25 °C, fCLK = 3.579545 MHz.
‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

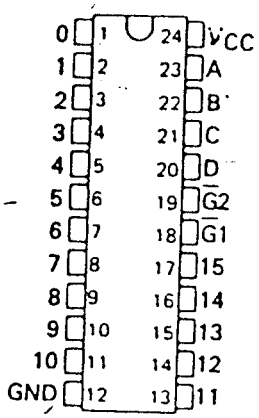
Notes:
1. dBm is defined above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Standard DTMF frequencies are used, measured at GS.
5. All tones of the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 kHz) Gaussian noise.
7. The third tone frequencies are (350 and 440 Hz) ± 2%.
8. Guaranteed by design and characterization.
9. Referenced to lowest level frequency component in DTMF signal.
10. Characterized to assure that acceptance level is measured with specified maximum frequency deviation.
11. Pin designations used are IN+, IN-, and OE.
12. Internal voltage source used to bias V_{REF}.
13. Third tone tolerance also applies to a third tone injected onto the power supply.
14. Refer to Figure 3, input DTMF tone level at -28 dBm.

TYPES SN54154, SN54L154, SN74154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1972–REVISED DECEMBER 1983

- '154 is Ideal for High-Performance Memory Decoding
- 'L154 is Designed for Power-Critical Applications
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL and MSI Circuits

SN54154 . . . J OR W PACKAGE
SN54L154 . . . J PACKAGE
SN74154 . . . J OR N PACKAGE
(TOP VIEW)



TYPE	TYPICAL AVERAGE PROPAGATION DELAY 3 LEVELS OF LOGIC	STROBE	TYPICAL POWER DISSIPATION
54	23 ns	19 ns	170 mW
54	46 ns	38 ns	85 mW

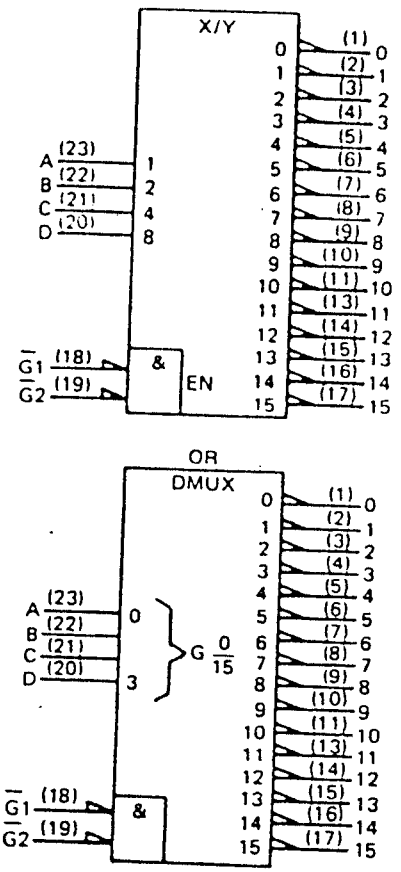
escription

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

The SN54154 and SN54L154 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74154 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown on logic notation are for J or N packages.

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

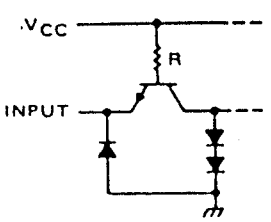
FUNCTION TABLE

INPUTS						OUTPUTS															
$\overline{G}1$	$\overline{G}2$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

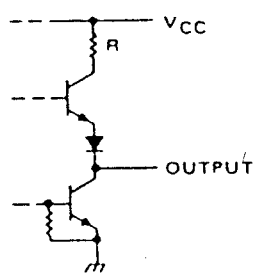
Schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



'154: R = 6 kΩ NOM
'L154: R = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



'154: R = 130 Ω NOM
'L154: R = 260 Ω NOM

bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

OTE 1 Voltage values are with respect to network ground terminal.

commended operating conditions

	SN54154			SN74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
upply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
igh-level output current, I_{OH}			−800			−800	μA
ow-level output current, I_{OL}			16			16	mA
perating free-air temperature, T_A	−55		125	0		70	C

ectrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†	SN54154			SN74154			UNIT
			MIN	TYP	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		34	49		34	56	mA

or conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
All typical values are at V_{CC} = 5 V, T_A = 25°C.
ot more than one output should be shorted at a time.
OTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

vitching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

OTE 3: See General Information Section for load circuits and voltage waveforms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54L154			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54L154			UNIT
		MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
I_{OS}§	V_{CC} = MAX	−9		−29	mA
I_{CC}	V_{CC} = MAX, See Note 2		17	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C, D	Any	R_L = 800 Ω, C_L = 15 pF		48	72	ns
t_{PHL}					44	66	ns
t_{PLH}	Strobe				40	60	ns
t_{PHL}					36	54	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.