DIGITAL FREQUENCY AND SPEED MONITOR

PROJECT REPORT P-69

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF BACHELOR OF ENGINEERING IN ELECTRICAL AND ELECTRONICS ENGINEERING OF THE BHARATHIYAR UNIVERSITY, COIMBATORE-46

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1989-90

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Certificate

This is to certify that the Report entitled

Digital Frequency and Speed Monitor

has been submitted by

Mr _____

in partial fulfilment for the award of Bachelor of Engineering in the Electrical and Electronics Engineering Branch of the Bharathiyar University, Coimbatore-641 046 during the academic year 1989-90

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Guide

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Head of the Dept.

Certified that the candidate was examined by us in the Project Work Viva-Voce Examination held on _____ and the Univerosity Register Number was _____

_____
Internal Examiner

_____
External Examiner

ACKNOWLEDGEMENT

At the outset we would like to place in record our gratitude and appreciation to **Miss. K. RAJESWARI B.E.**, our guide, for her perspicacious guidance counselling and invalvable suggestions without which this project would not have been successful.

We profusely thank **Mr. C. KRISHNASWAMY, B.E.,** (Electronics R & D, Premier instruments & Controls Ltd) who rendered it possible for us to submit this project. He had helped us unfluggingly at all stages of the project, despite a very tight schedule.

Our sincere thanks are due to **Dr. K.A. PALANISWAMY,** Professor & Head of the Department, Department of Electrical and Electronics for having allowed us to use all the facilities in the laboratory for our project. We also thank **Dr. S. PADMANABHAN,** Professor & Head of the Department, and the staff of the Department of Electronics and Communication Engineering for having helped us during the course of the project.

We would be failing in our duty if we don't thank our principal, **Prof. R. PALANIVELU,** for his kind patronage and encouragement.

_ AUTHORS -

CONTENTS

SYNOPSIS

This project work provides a Universal Counter for the measurement of speed, line frequency and external frequencies using digital techniques.

The Project has been designed and fabricated using innovative CMOS ICs. The heart of the system is the versatile, universal, presettable counter, display driver-7217 AIPI. An added advantage of this system is that it has been built with a 5 volt Power Supply which caters to the power needs of the unit.

Another attractive feature of this unit is that mode selection has been simplified by means of toggle switches. External adjustment and complicated fittment modifications have thus been done away with. The readings are digital (on seven segment displays) making them more accurate and easily readable.

INTRODUCTION

This system is extremely useful in labs, industries and power stations, where it is of extreme importance to monitor the mentioned parameters at the same time. Many different meters may be replaced using this single unit.

An important feature of this unit is that a NON CONTACT Proximity switch has been used as a sensor and hence the measurand is not loaded. The pulses from the sensor are shaped and fed to the main counter. A timing signal provided by crystal controlled oscillators has been used to improve accuracy.

The principle behind the measurement of frequency and speed is counting pulses every second and displaying them, hence the value of parameters at every second may be measured. The interface circuits have been designed for correct scaling factor, hence making the readings more accurate.

The present work has been done to develop and test a model using a monolythic IC 7217 AIPI with additional supporting CMOS ICs to optimise circuit flexibility and combine with its economy.

4. DESCRIPTION:

The measurement of the parameter input is performed by the conversion of a square pulse, monitoring it for one second, counting and displaying on an easy to read seven segment numeric display.

This system comprises of the following sections:-

1. Power Supply
2. One second pulse clock
3. Speed sensor
4. Speed pulse interface
5. Line frequency
6. Line frequency interface
7. External frequency interface
8. Counter display driver

A simplified block diagram of this unit has been shown in fig 4-1. In the forthcoming sections circuit diagrams and their design details have been given.

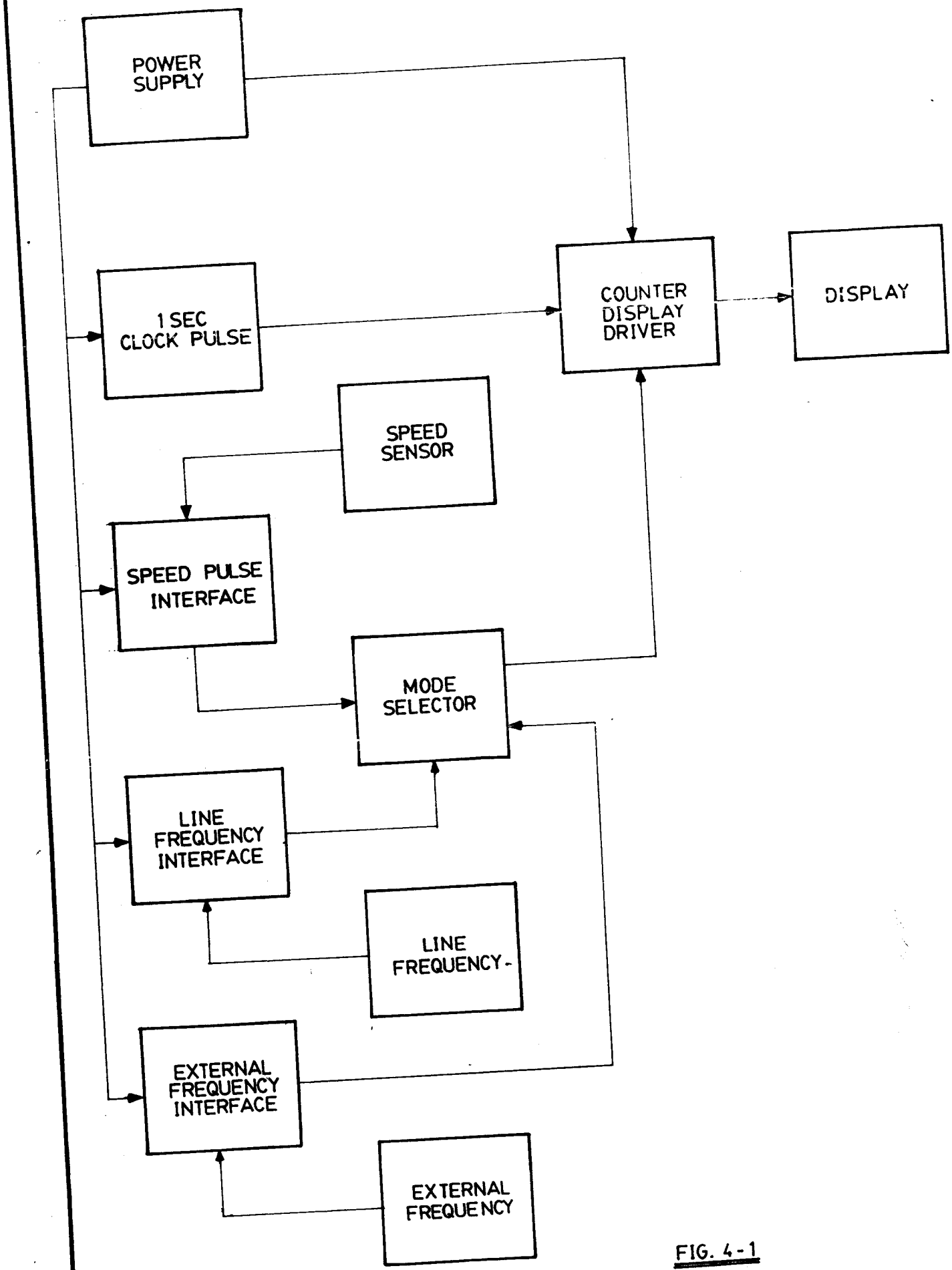

FIG. 4-1

FUNCTIONAL BLOCK DIAGRAM

4-1

DESCRIPTION OF POWER SUPPLY:

The power requirement of this system for normal operation is a regulated 5V DC. The three pin positive voltage regulator 7805 which offers high noise immunity and better regulation has been selected. 230 Volts stepped down to 6 Volts with 500 milliamperes is obtained by means of a suitable transformer. (It is necessary that for proper regulation the input voltage should be 2 Volts higher than the output voltage). A detailed circuit has been shown in fig 4.2.

CIRCUIT OPERATION:

The transformer T1 steps down an AC 230V to 6V. The 6V hence obtained is an AC. It is rectified by a diode bridge which comprises of diodes D1, D2, D3 and D4. The output wave form is smoothened by the capacitor C1, which acts as a filter capacitor . (For wave forms refer chapter 5 - Test Results). Capacitors C2 and C3 are used to suppress high frequency noises and reduce the ripple in the regulated supply.

Unregulated voltage is used for the sensor to reduce the loading on 7805. A red LED has been used in series with R1 to indicate Power ON.

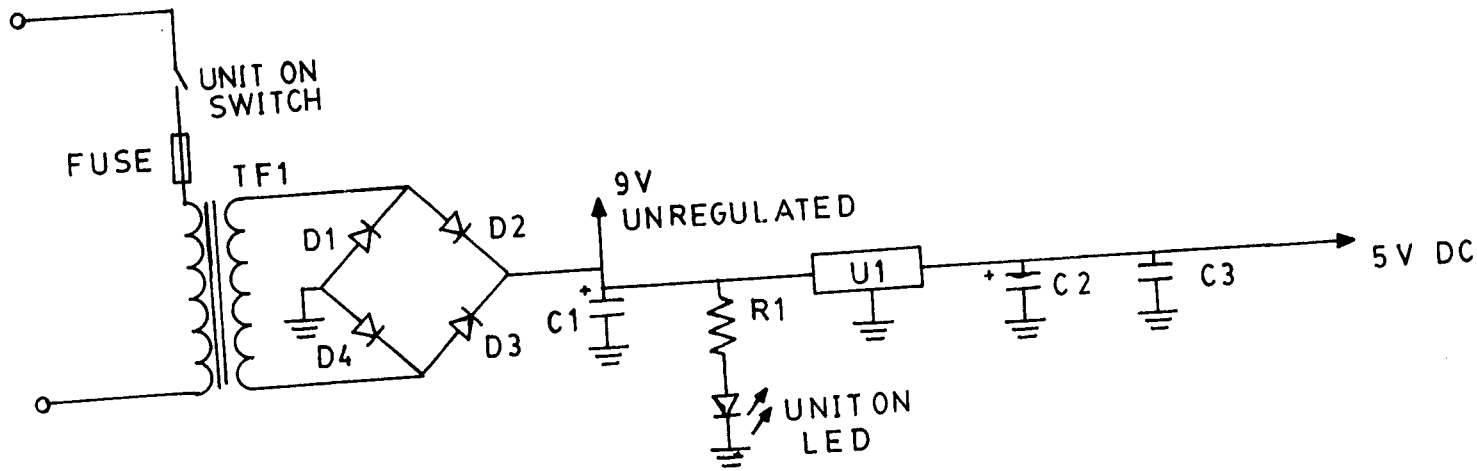

FIG. 4 - 2

POWER SUPPLY

PARTS LIST (FOR POWER SUPPLY)

D1, D2, D3, D4	.....	IN 4001
C1	.....	1000 Mfd ± 20% 25V Radial
C2	.....	10 Mfd ± 20% 16V Radial
C3	.....	0.1 Mfd ± 20% 50V Ceramic
U1	.....	IC 7805
TF1	.....	230V/6V, 500 mA Transformer with CRGO core.
FUSE	.....	250V 200mA

4-2

ONE SECOND CLOCK PULSE:

A crystal controlled oscillator has been used to generate one second clock pulse, to improve reliability and stability. A detailed circuit has been given in fig 4-3.

The IC U2 5369 has a built-in inverter cum divider with feed back resistors R2 and R3. Crystal XL oscillates at a frequency of 3.579 MHz. This frequency is divided to 60 Hz by the IC U2. Further division, 1/6, 1/10 is performed by U3 IC 4518. This gives an output of one second. A stable one second clock pulse is thus obtained.

PARTS LIST FOR ONE SECOND CLOCK PULSE:

R2 - 1K ± 1% MFR , ½ Watt

R3 - 20M ± 1% MFR, ½ Watt

R4 - 10K ± 5% CFR, ¼ Watt

R5 - 100K ± 5% CFR, ¼ Watt

C3 - 22 Pf ± 20% Mica 50 Volts

C4 - 22 Pf ± 20% Mica 50 Volts

C5,C6 - 0.1 Mfd ± 20% Ceramic Disc 50 Volts

U2 - IC 5369 Plastic Dip

U3 - IC 4518 Plastic Dip

XL 3.579 MHz Crystal

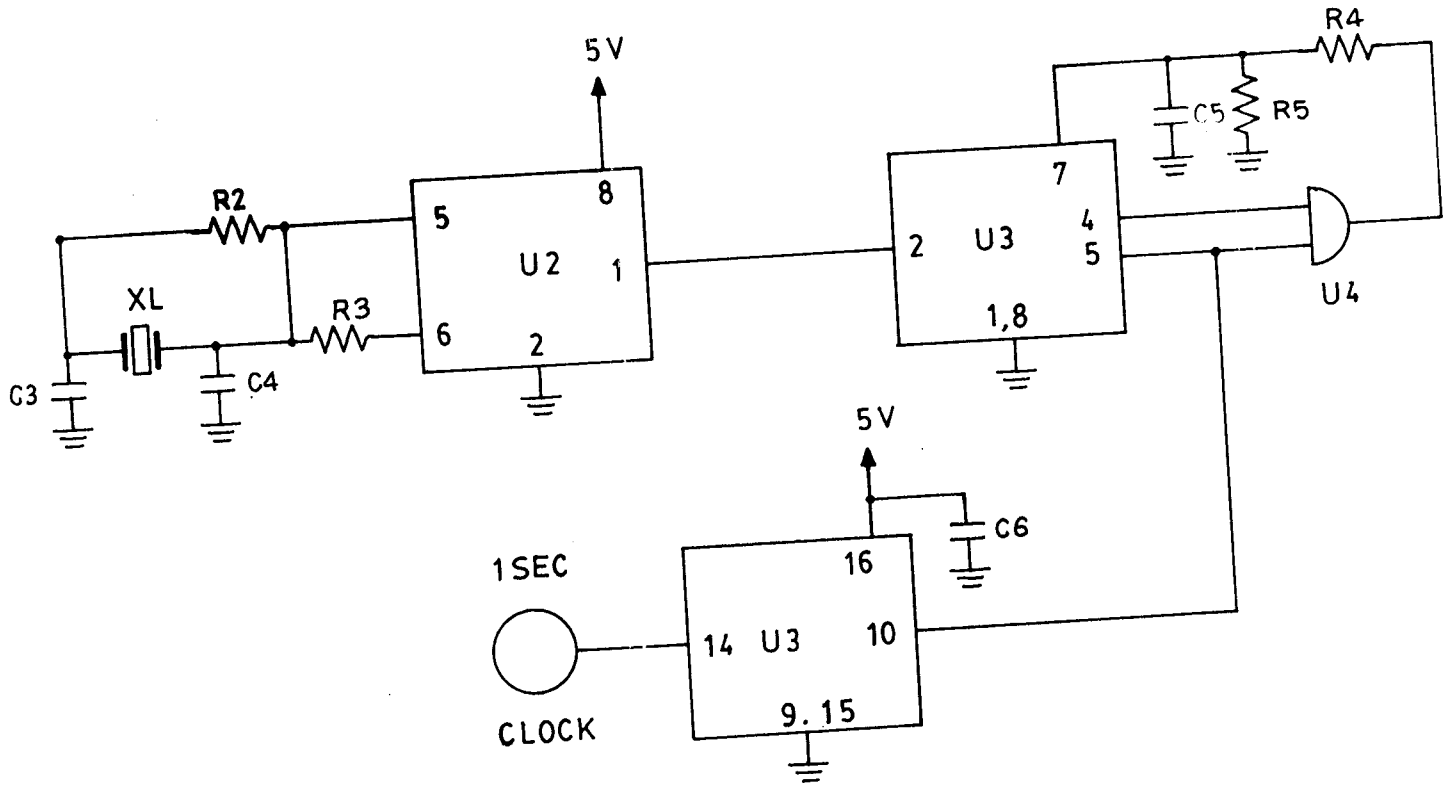

FIG. 4.3
1 SECOND CLOCK PLUSE

4.3

SPEED SENSOR:

The type of sensor used is a non contact type inductive proximity switch. It does not load shaft whose speed is to be measured . It detects the presence of metal upto a distance of 5mm from its face and gives a pulse for each metal crossing. The number of pulses selected is six, so that the pulse per revolution is well within the limitations of the sensor even at maximum speed.

Maximum rpm to be measured = 9999 Hz.

_ 10,000 Hz.

So, rps = $\frac{10,000}{60}$

At maximum rpm , number of pulses per second = $\frac{10,000}{60} \times 6$

= 1,000 Hz.

(that is 1 KHz)

So the sensor has been selected accordingly.

SPEED PULSE INTERFACE:

Pulses from the sensor vary from 0V to unregulated voltage. They are shaped to 0V-5V by transistor T1 and U5 (IC 4093) which acts as a schmitt trigger. A proper RC Combination is selected to shape more than 1KHz frequency at maximum rpm. (Refer Chapter-5 for test results).

R8 = 1Kilo Ohm

Vcc = 5V

Ic = 5/1000

= 5mA

Assume B of T1 = 50.

Minimum IB to saturate T1 = 5/50

= 0.1mA

Sensor output high voltage= $6 \times \sqrt{2}$

= 8.5 Volts

Base resistance of T1 (R7) is selected as 10K to ensure full saturation of T1.

Similarly Time Constant R9 x C10 = 10K x 1KPF

$= 10 \times 10^{3} \times 1 \times 10^{-9}$

$= 10^{-5}$

= 1/100 ms.

Maximum Frequency = 1 KHz

= 1 ms

1 ms x C10

Therefore a proper filtering action is ensured without affecting the input number of pulses. This frequency is once again multiplied by 10 by means of a phase locked loop system and fed to the counter for further process.

Number of pulses per revolution $= 6 \times 10$

$= 60$

Assume an rpm of 'R'

Therefore number of pulses per minute $= R \times 60$

number of pulses per second $= R \times \frac{60}{60}$

$= R$

So sampling time is selected as one second to count and display the input pulse which directly corresponds to rpm.

Fig 4-4 corresponds to the circuit digram for speed pulse interface.

PARTS LIST FOR SPEED PULSE INTERFACE.

T1 ..... BC 107

R7 ..... 1K CFR ½W ± 5%

R8 ..... 100K CFR ¼W ± 5%

R9 ..... 10K CFR ¼W ± 5%

R10..... 100K CFR ¼W ± 5%

R11..... 1K CFR ¼W ± 5%

R12..... 6.8K CFR ¼W ± 5%

R13..... 4.7K CFR ¼W ± 5%

R14..... 1K CFR ¼W ± 5%

R15..... 1K CFR ¼W ± 5%

R16..... 1K CFR ¼W ± 5%

R17..... 4,7K CFR ¼W ± 5%

R18..... 4.7K CFR ¼W ± 5%

VR1..... 5K PRESET

C10..... 1 KPF DISC 50V

C11..... 0.1 MFD DISC 50V

C12..... 0.5 MFD DISC 50V

C13..... 0.001 MFD DISC 50V

C14..... 0.1 MFD DISC 50V

C15..... 0.5 MFD DISC 50V

C16..... 750 PF DISC 50V

C17..... 0.1 MFD DISC 50V

U5 ..... IC 4093

U6 ..... IC 565

U7 ..... IC 7490

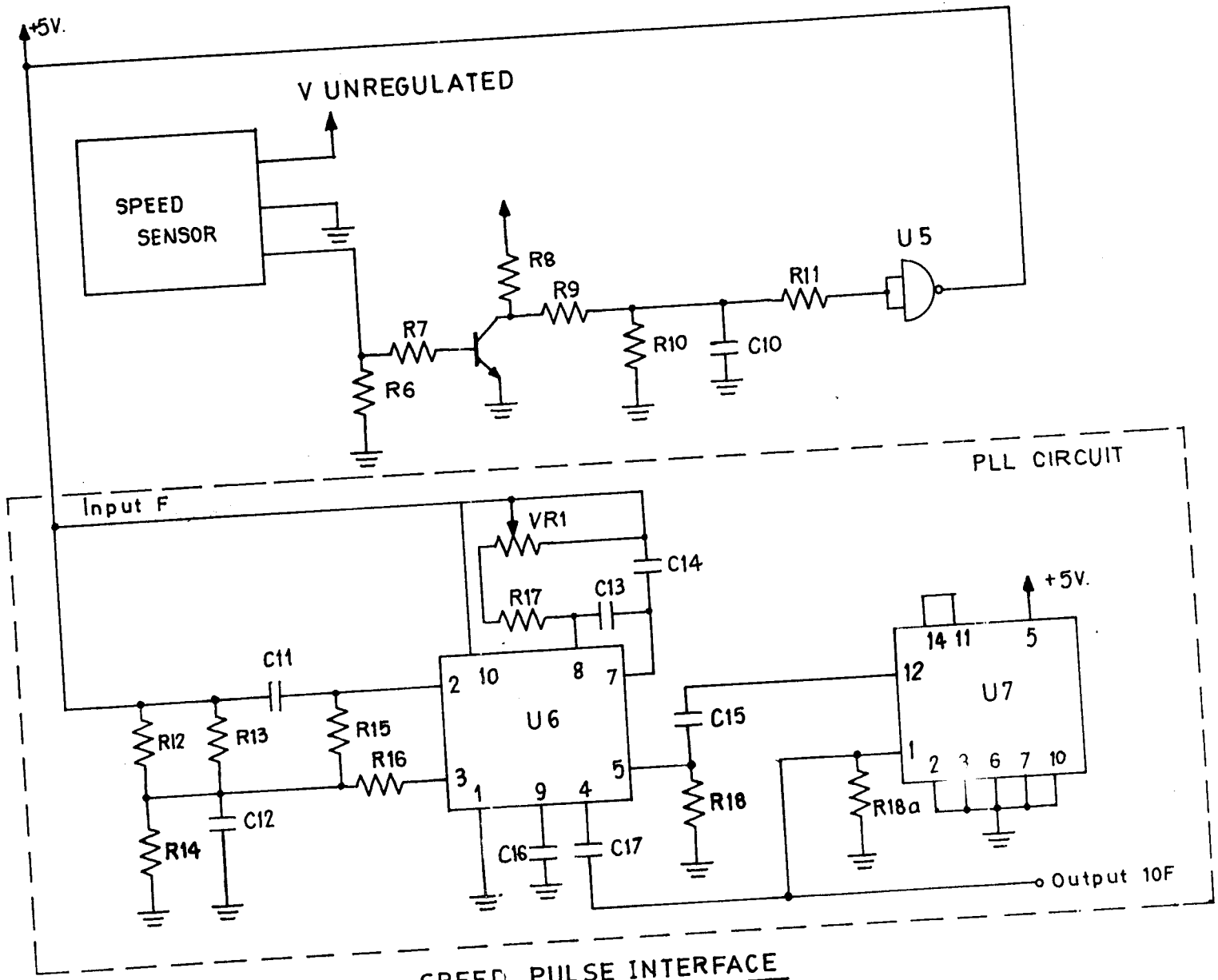

FIG. 4.4 SPEED PULSE INTERFACE

4-5

LINE FREQUENCY AND INTERFACE:

For measurement of line frequency an AC of 6V at line frequency is obtained by stepping down the 230V supply by means of a suitable transformer. A diode D is used to get a half cycle of the line frequency. This half cycle voltage is clipped to 5.1 Volts. It is then shaped by schmitt trigger. Using a phase locked loop, the frequency is again multiplied by 10, so that the resolution of the frequency becomes 0.1 Hz.

The phase locked loop circuit and the interfacing circuit are the same as the circuits used for interfacing the speed sensor. Sampling time is selected as 1 sec, so that the output reading is in Hz.

Detailed circuit diagram for line frequency is shown in fig 4-5.

PART LIST FOR LINE FREQUENCY AND INTERFACE.

TF2	.....	230V AC 50Hz / 6V 200mA.
D5	.....	IN4001
ZD1	.....	5.1V Z 400mV
R19	.....	1K CFR ½W ± 5%
R20	.....	10K CFR ½W ± 5%
C18	.....	0.1 MFD 50V CERAMIC DISC
U5	.....	IC 4093

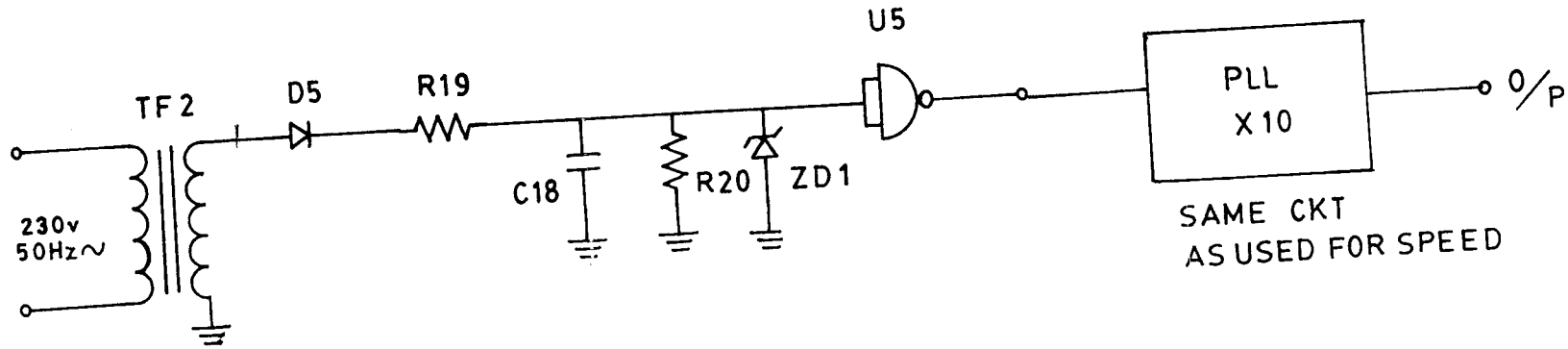

FIG: 4.5

LINE FREQUENCY INTERFACE

4.6

EXTERNAL FREQUENCY INTERFACE:

Any frequency in the range of 0-9999 Hz may be measured by this part of the circuit. The waveform may be of any form (sinusoidal, triangular etc.,). The input pulses are shaped to 0-5V square pulse by transistor T2 and IC 4093 which acts as a schmitt trigger. A proper RC Combination is selected for effective wave shaping.

R 21= 1 Kilo Ohm

Vcc = 5V

Ic = 5/1000

= 5mA

Assume B of T2 = 50

Maximum IB to saturate T2 = 5/50

= 0.1 mA

Sensor output high voltage= $6 \times \sqrt{2}$

= 8.5V

Base resistance of T2 is selected to ensure full saturation of T2.

Similarly, R22x C19 = 10K x 1 KPF

$= 10 \times 10^{3} \times 1 \times 10^{-9}$

$= 10^{-5}$

= 1/100 ms

Maximum frequency = 1 KHz = 1 ms.

1 ms R22x C19

Therefore a proper filtering action is ensured without affecting the input number of pulses. Sampling time is selected as one second to count and display the input pulse which directly corresponds to Hertz.

Fig. 4-6 corresponds to external frequency interface.

PARTS LIST FOR EXTERNAL FREQUENCY INTERFACE

R21	.....	1K CFR ¼W ±5%
R22	.....	10K CFR ¼W ± 5%
R23	.....	100K CFR ¼W ± 5%
R24	.....	4.7K CFR ¼W ± 5%
R25	.....	10K CFR ¼W ± 5%
R26	.....	1K CFR ¼W ± 5%
C19	.....	1 KPF CERAMIC DISC 50V
U5	.....	IC 4093
T2	.....	BC 107

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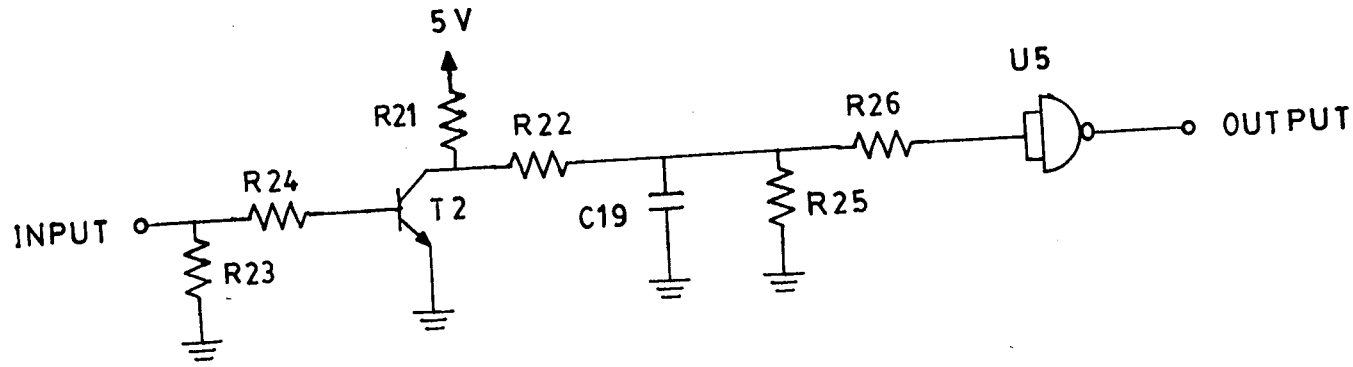


FIG: 4.6

External Frequency Interface.

4-7

COUNTER DISPLAY DRIVER:

This part of the circuit is the most important one and is designed using a 7217 AIPI which is a universal presettable counter and a common cathode display driver. It is a 28 pin IC with a built-in oscillator to operate the four displays in a multiplexed mode so as to minimize the power consumption. the reset and latch pulses are active low. Two monostables (using IC 4093) are connected in series. The 1 Hz clock pulse is fed to the first monostable whose output is connected to the latch pin of 7217 AIPI. During the falling edge of the 1 Hz pulse monostable gets triggered and goes low. Hence the counted output is latched to display and kept there till the next pulse goes to pin 9 of the 7217 AIPI. During the rising edge of this pulse the second monostable gets triggered and resets the counter to zero. The input pulses are once again counted from zero and latched to the display till the next reset pulse reaches pin9. This process is cyclic and the readings are updated for every second. As a result the value of parameters for every second are obtained.

Detailed circuit diagram is shown in fig.4.7.

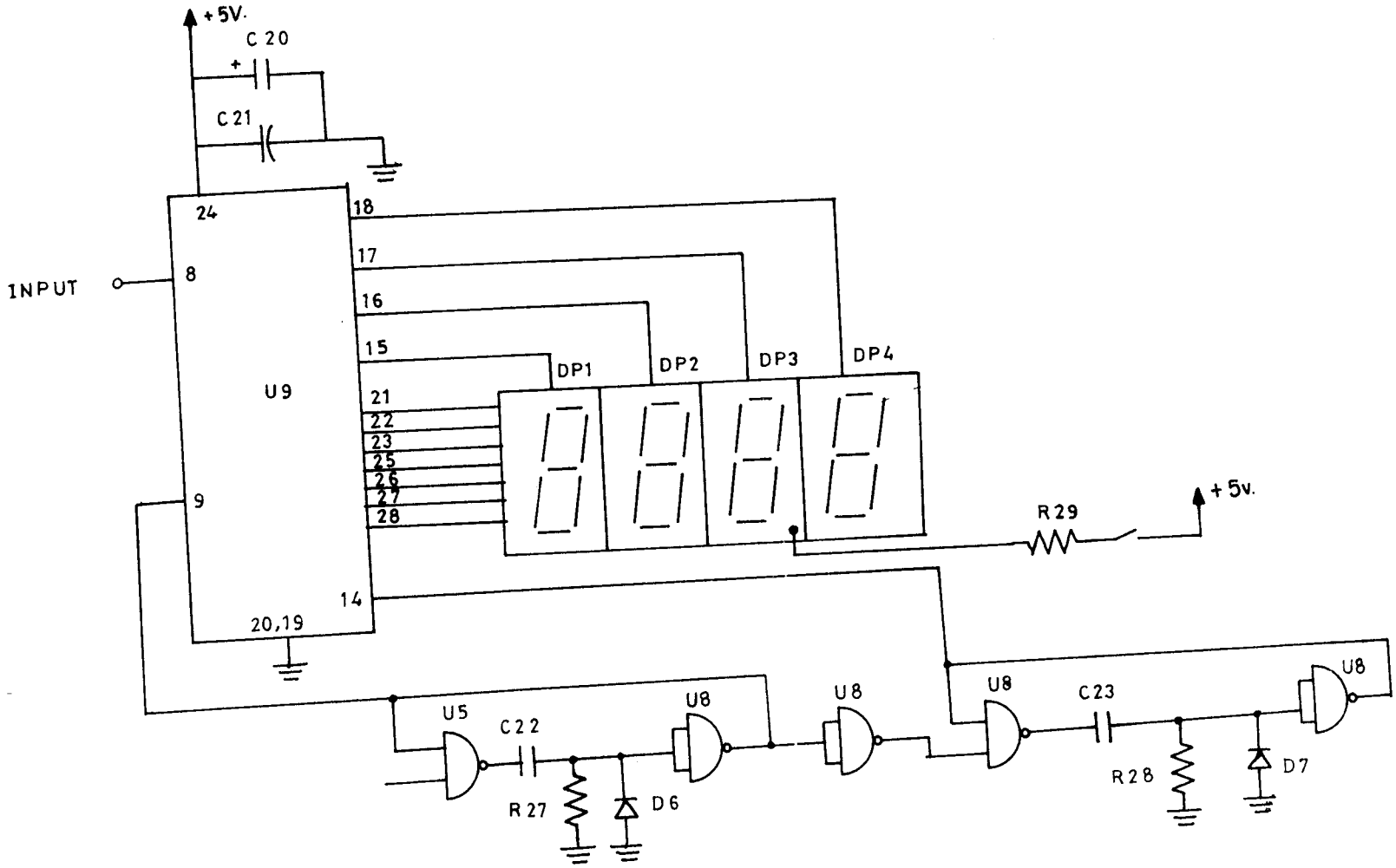


FIG: 4·7 COUNTER DISPLAY DRIVER

PARTS LIST FOR COUNTER DISPLAY DRIVER

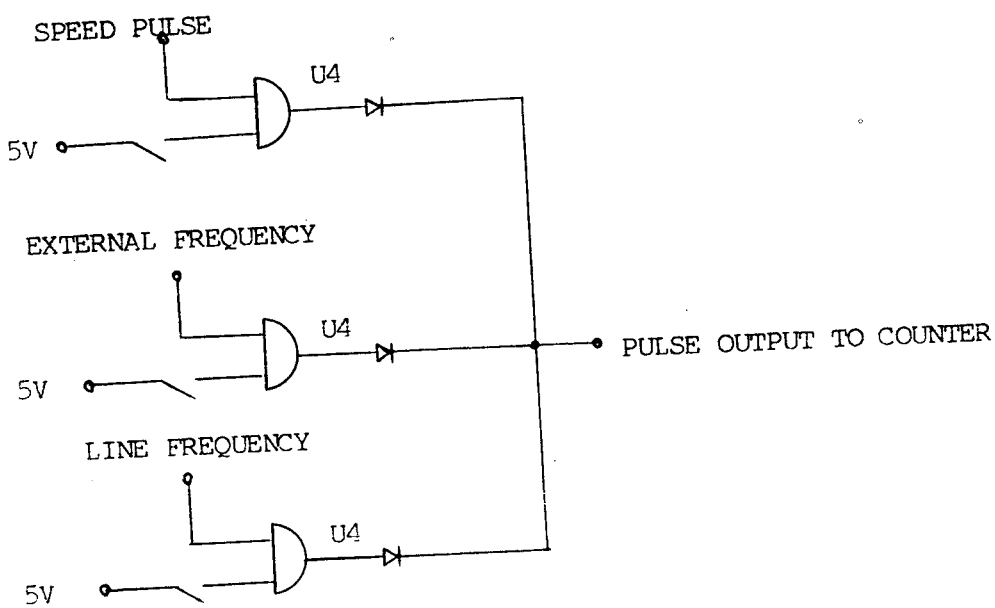
U5	.....	IC 4093
U8	.....	IC 4093
U9	.....	IC 7217 AIPI
C20	.....	10 MFD 25V
C21	.....	0.1 MFD DISC 50V
C22	.....	0.1 MFD DISC 50V
C23	.....	0.1 MFD DISC 50V
R27	.....	22K CFR $\pm$ 5% $\frac{1}{4}$W
R28	.....	22K CFR $\pm$ 5% $\frac{1}{4}$W
R29	.....	560E CFR $\pm$ 5% $\frac{1}{4}$W
D6	.....	IN4001
D7	.....	IN4001
DP1	.....	FND 500
DP2	.....	FND 500
DP3	.....	FND 500
DP4	.....	FND 500

4-8

MODE SELECTION METHOD:

This unit offers easy mode selection which involves the closing of toggle switches corresponding to the circuit of the relevant parameter. the closing of a toggle switch puts the necessary circuit into use. All the three inputs to the switches are permanently connected to the inputs of the AND gate while the switch ends are connected to the other inputs. During selection any one gate is kept in enable position by pulling the respective other input of the gate to high. All the outputs of the gate ORed via diode to the counter inputs. fig 4-8 shows circuit of mode selection.

fig 4-8 MODE SELECTION METHOD



4-9

PRINTED CIRCUIT BOARD DESIGN:

For making the Printed Circuit Board 1.8mm thick hylum based copper sheet was used. The layout was made using computer aided technology. SMART WORK software package supported the computer. Glimpses of some commands are as follows.

F1 - Initiate a line

F2 - Erase a line

F3 - To make a hole

F4 - To erase a hole

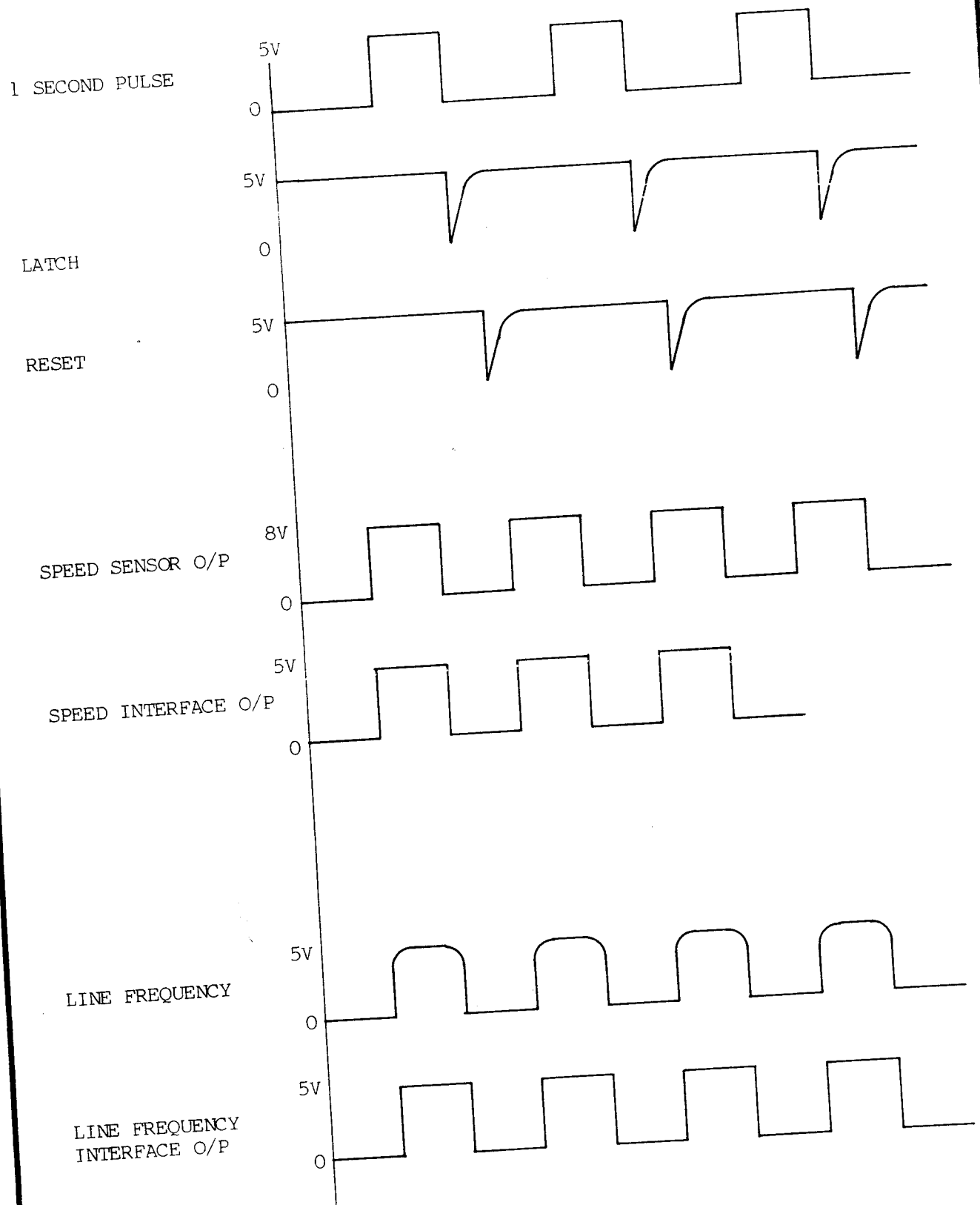
F5 - To thicken a line

F6 - To thin a line

F7 - To make a finish point

The PCB is a single sided one. That is the circuit is on one side and the components are placed on the other. Fig 4-9 depicts the circuit side of the PCB.

5.0 TEST RESULTS AND WAVEFORMS



SPECIFICATIONS

Supply	:	230V AC , 50 Hz.
Maximum measurable speed	:	9999 rpm
Maximum measurable frequency	:	9999 Hz.
Line frequency	:	Minimum 30 Hz Maximum 75 Hz
Resolution	:	0.1 Hz for line frequency/speed
Accuracy	:	±1 %
SENSOR:		
Type of sensor used	:	Inductive type proximity switch
Supply Voltage	:	3V to 30V
Output	:	NC
Maximum driving capacity	:	100 mA
Maximum sensing distance	:	3mm
Size	:	M 15
Sensor wheel	:	Six teeth
Display	:	Seven Segment Common Cathode

7.0 SCOPE FOR IMPROVEMENT:

By cascading another 7217 AIPI with the existing one four more digits may be added to the existing display. Thus the maximum r.p.m and maximum frequency that can be measured may be increased.

The PLL Technology used in our system is X10. Instead of this same technology with component values redesigned can give X100 which inturn increases the resolution of the requirement.

Duty cycle of any square wave form may also be measured. Instead of the to be measured pulse should be fed to the Latch-Reset monostables. For clock external 1ms pulse should be given for counting.

The Universal Counter 7217 AIPI has an in built preset facility also. This preset facility can be used to preset the maximum or minimum values of the counter. This values are constantly compared with the counter contents and equal is given out by the chip which may be used to activate a warning for some other system.

The same circuit with a little bit of modification on the peripheral circuit of the 7217 can be used as a preset counter of the number of events. The scheme for the above is given in fig 7.1.

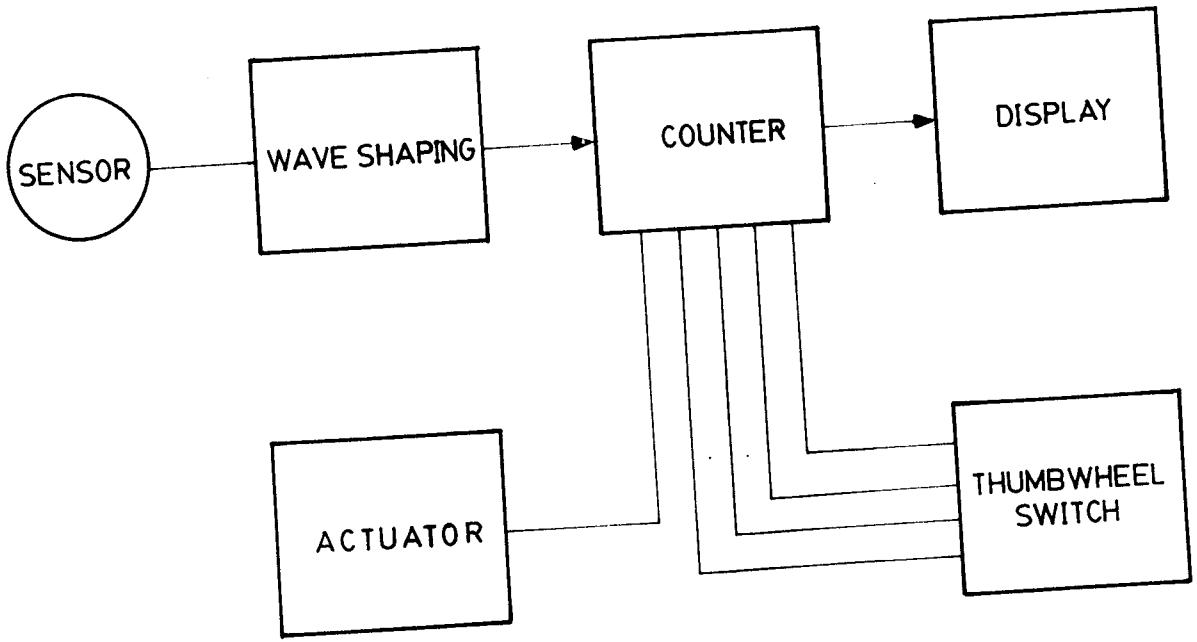

SENSOR
WAVE SHAPING
COUNTER
DISPLAY
ACTUATOR
THUMBWHEEL SWITCH

FIG. 7.1

8. CONCLUSION

The various aspects of the project have been explained in the preceeding chapters. this circuit enables digital measurement of speed, line frequency and an external frequency. As pointed out before (Chapter 7) if a few modifications are made in the existing circuit of the 7217 AIPI, the unit can be used as a warning system if a parameter exceeds preset values. Due to its low power consumptions this unit may be used to monitor parameters for any length of time as designed . The project was fabricated and tested and found working satisfactorily at the time of testing.

¢¢¢¢¢¢¢¢¢

REFERENCES

1. NATIONAL SEMICONDUCTORS DATA BOOK (MM SERIES)
2. CMOS MANUAL
3. TEXAS INSTRUMENTS INCORPORATED MANUAL
4. RCA DATA BOOK
5. SIGNETICS DATA BOOK
6. HOT IDEAS IN CMOS (INTERSIL DATA BOOK)
7. SIEMENS OPTO ELECTRONICS MANUAL
8. JOHN MARKUS' MODERN ELECTRONIC CIRCUITS REFERENCE MANUAL.

****

LIST OF FIGURES

National Semiconductor

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

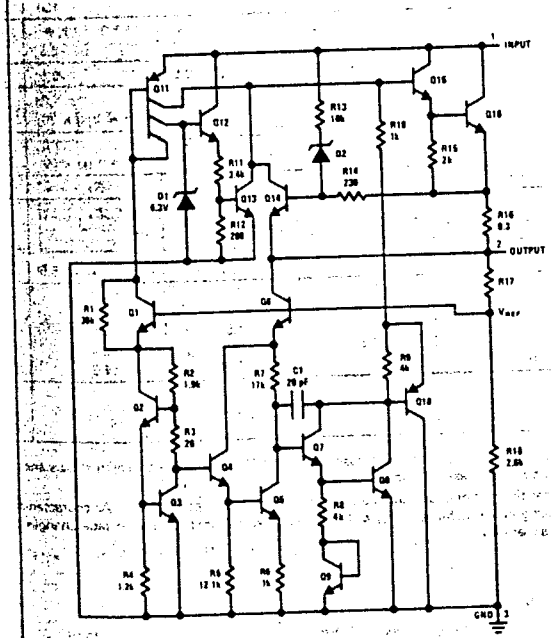
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

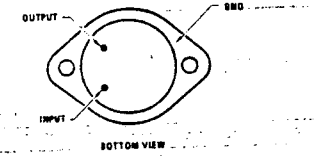
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams

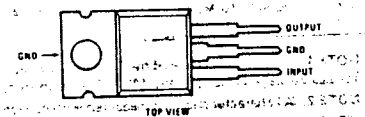


Metal Can Package
TO-3 (K)
Aluminum



Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

Plastic Package
TO-220 (T)



Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

Absolute Maximum Ratings

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

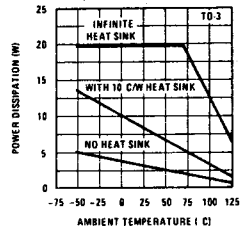
OUTPUT VOLTAGE			5V			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise noted)			10V			19V			23V			
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}	4.75 (7 ≤ V_{IN} ≤ 20)		5.25	11.4 (14.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (17.5 ≤ V_{IN} ≤ 30)		15.75	V V
ΔV_O	Line Regulation	I_O = 500 mA, Tj = 25°C		3	50		4	120		4	150	mV
		I_O = 500 mA, ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
		I_O = 500 mA, 0°C ≤ Tj ≤ +125°C			50			120			150	mV
		I_O = 500 mA, ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A, Tj = 25°C			50			120			150	mV
		I_O ≤ 1A, ΔV_{IN}	(7.3 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A, 0° ≤ Tj ≤ +125°C			25			60			75	mV
		ΔV_{IN}	(8 ≤ $_{IN}$ ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	Tj = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
		Tj = 25°C, 250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C			50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A, Tj = 25°C			8			8			8	mA
		I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5	mA
		Tj = 25°C, I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)		1.0	(14.8 ≤ V_{IN} ≤ 27)		1.0	(17.9 ≤ V_{IN} ≤ 30)		1.0	mA V
		I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C, V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7 ≤ V_{IN} ≤ 25)		1.0	(14.5 ≤ V_{IN} ≤ 30)		1.0	(17.5 ≤ V_{IN} ≤ 30)		1.0	mA V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz, I_O ≤ 1A, Tj = 25°C or I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C	62 62	80		55 55	72		54 54	70		dB dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	Tj = 25°C, I_{OUT} = 1A		2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			18			19		mΩ
	Short-Circuit Current	Tj = 25°C		2.1			1.5			1.2		A
	Peak Output Current	Tj = 25°C		2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ Tj ≤ +125°C, I_O = 5 mA		0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25°C, I_O ≤ 1A	7.3			14.6			17.7			V

NOTE 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

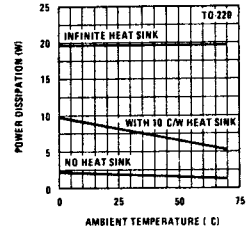
NOTE 2: All characteristics are measured with capacitor across the inut of 0.22 μF, and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

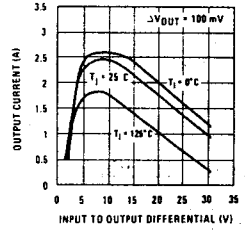
Maximum Average Power Dissipation



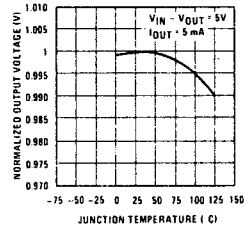
Maximum Average Power Dissipation



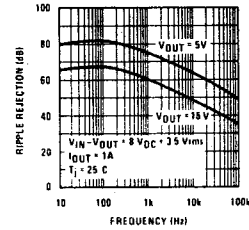
Peak Output Current



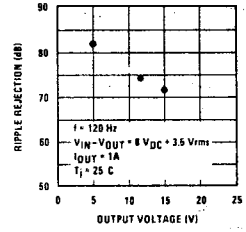
Output Voltage (Normalized to 1V at T_j = 25°C)



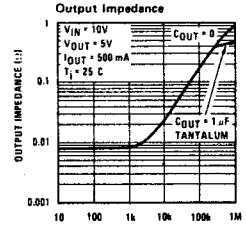
Ripple Rejection



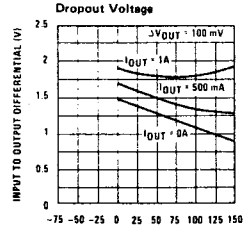
Ripple Rejection



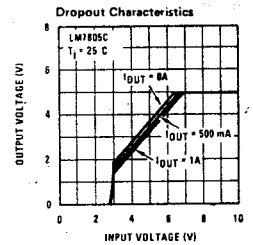
Output Impedance



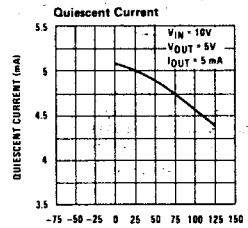
Dropout Voltage



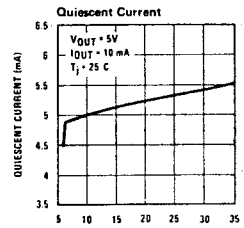
Dropout Characteristics



Quiescent Current



Quiescent Current



National Semiconductor

MM5369 Series 17 Stage Oscillator/Divider

General Description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the crystal frequency for tuning purposes and the 17th stage output. The MM5369 is available in an 8-lead dual-in-line epoxy package.

Features

- Crystal oscillator
- Two buffered outputs
  - Output 1 crystal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10V)
- Wide supply range 3–15V
- Low power
- Fully static operation
- 8 lead dual-in-line package
- Low current

Options

■ MM5369AA	3.58 MHz to 60 Hz
■ MM5369EYR	3.58 MHz to 50 Hz
■ MM5369EST	3.58 MHz to 100 Hz

Connection and Block Diagrams

Dual-In-Line Package

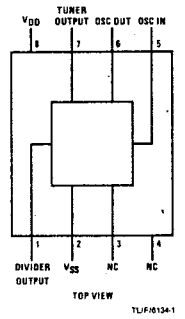


FIGURE 1

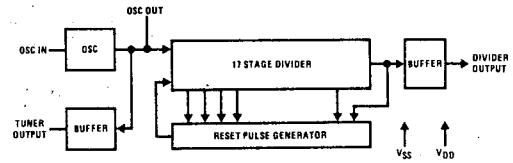


FIGURE 2

Order Number MM5369N
See NS Package N08E

Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{DD} +0.3V	Maximum V_{CC} Voltage	16V
Operating Temperature	0°C to +70°C	Operating V_{CC} Range	3V to 15V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

Electrical Characteristics

T_A within operating temperature range, V_{SS} = GND, 3V ≤ V_{DD} ≤ 15V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 15V			10	μA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V	DC		4.5	MHz
	V_{DD} = 6V	DC		2	MHz
Output Current Levels	V_{DD} = 10V, V_O = 5V				
Logical "1" Source		500			μA
Logical "0" Sink		500			μA
Output Voltage Levels	V_{DD} = 10V, I_O = 10 μA				
Logical "1"		9.0			V
Logical "0"				1.0	V

Note: For 3.58 MHz operation, V_{DD} must be ≥ 10V.

Functional Description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2*.

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

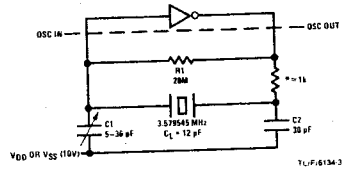
A pulse is generated when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs.

7

Functional Description (Continued)



*To be selected based on xtal used

FIGURE 3. Crystal Oscillator Network

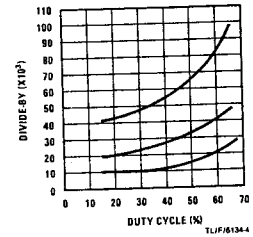


FIGURE 4. Plot of Divide-By vs Duty Cycle

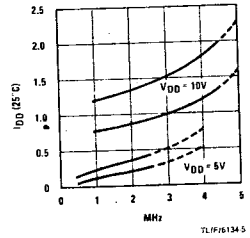


FIGURE 5. Typical Current Drain vs Oscillator Frequency

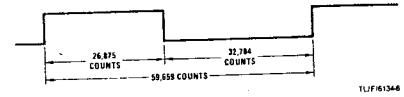
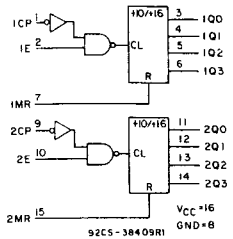


FIGURE 6. Output Waveform for Standard MM5369AA

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

File Number **1665**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Synchronous Counters

CD54/74HC/HCT4518 — BCD
CD54/74HC/HCT4520 — Binary

Type Features:

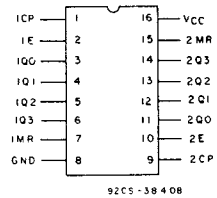
- *Positive or Negative Edge Triggering*
- *Synchronous Internal Carry Propagation*

The RCA CD54/74HC4518 and CD54/74HCT4518 are dual BCD up-counters. The RCA CD54/74HC4520 and CD54/74HCT4520 are dual binary up-counters. Each device consists of two independent internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or the negative-going transition of CLOCK. The counters are cleared by high levels on the MASTER RESET lines. The counter can be cascaded in the ripple mode by connecting Q3 to the ENABLE input of the subsequent counter while the CLOCK input of the latter is held low.

The CD54HC/HCT4518 and CD54HC/HCT4520 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4518 and CD74HC/HCT4520 are supplied in a 16-lead plastic dual-in-line packages (E suffix), and in 16-lead surface mount plastic dual-in-line packages (M suffix). The CD54/74HC/HCT4518/4520 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

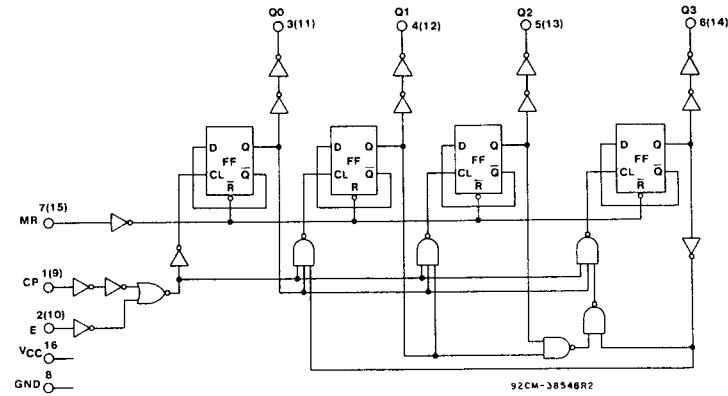


Fig. 1 — CD54/74HC/HCT4518 Logic Diagram

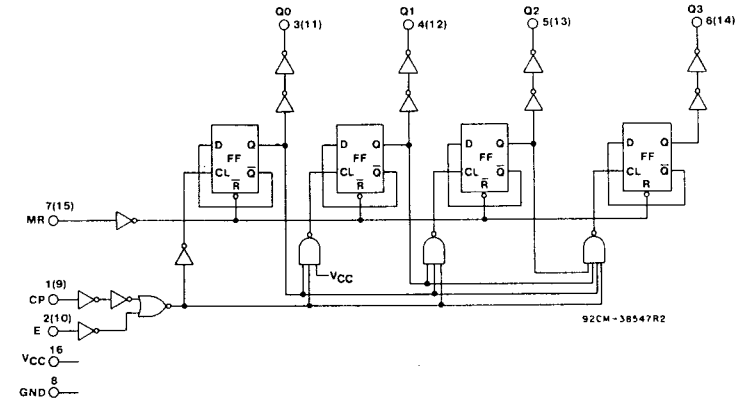


Fig. 2 — CD54/74HC/HCT4520 Logic Diagram

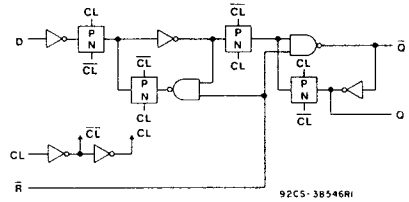


Fig. 3 - Detail of each D Flip-Flop

TRUTH TABLE			
CP	E	MR	ACTION
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q0 thru Q3 = L

X = Don't Care H = High State L = Low State
↑ = low-to-high transition
↓ = high-to-low transition

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}): ..... -0.5 to + 7 V
(Voltages referenced to ground) ..... ±20mA
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V) ..... ±25mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5$V) ..... ±50mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}) ..... 500 mW
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... 500 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... 400 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... -55 to +125° C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -40 to +85° C
PACKAGE TYPE E, M ..... -65 to +150° C
STORAGE TEMPERATURE (T_{stg}) ..... +265° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .....
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CMOS Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

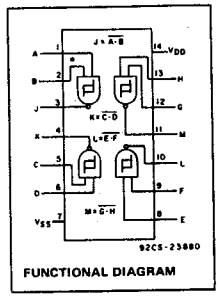
The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



FUNCTIONAL DIAGRAM

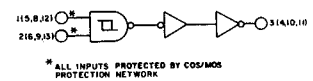
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (T_A = Full Package-Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



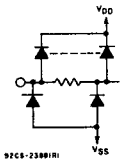
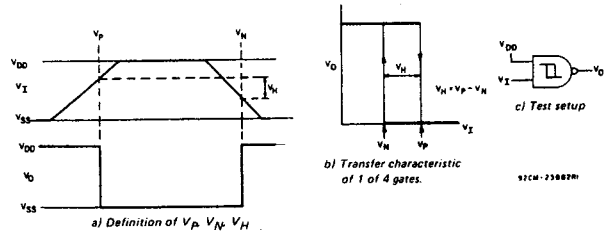


Fig. 1 – Logic diagram—1 of 4 Schmitt triggers.



a) Definition of V_P, V_N, V_H b) Transfer characteristic of 1 of 4 gates. c) Test setup

Fig. 2 – Hysteresis definition, characteristic, and test setup.

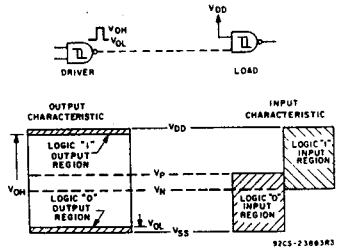


Fig. 3 – Input and output characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	–	a	5	2.2	2.2	2.2	2.2	2.2	2.9	–	V
	–	a	10	4.6	4.6	4.6	4.6	4.6	5.9	–	
	–	a	15	6.8	6.8	6.8	6.8	6.8	8.8	–	
	–	b	5	2.6	2.6	2.6	2.6	2.6	3.3	–	
	–	b	10	5.6	5.6	5.6	5.6	5.6	7	–	
	–	b	15	6.3	6.3	6.3	6.3	6.3	9.4	–	
V_P Max.	–	a	5	3.6	3.6	3.6	3.6	–	2.9	3.6	V
	–	a	10	7.1	7.1	7.1	7.1	–	5.9	7.1	
	–	a	15	10.8	10.8	10.8	10.8	–	8.8	10.8	
	–	b	5	4	4	4	4	–	3.3	4	
	–	b	10	8.2	8.2	8.2	8.2	–	7	8.2	
	–	b	15	12.7	12.7	12.7	12.7	–	9.4	12.7	
Negative Trigger Threshold Voltage V_N Min.	–	a	5	0.9	0.9	0.9	0.9	0.9	1.9	–	V
	–	a	10	2.5	2.5	2.5	2.5	2.5	3.9	–	
	–	a	15	4	4	4	4	4	5.8	–	
	–	b	5	1.4	1.4	1.4	1.4	1.4	2.3	–	
	–	b	10	3.4	3.4	3.4	3.4	3.4	5.1	–	
	–	b	15	4.8	4.8	4.8	4.8	4.8	7.3	–	
V_N Max.	–	a	5	2.8	2.8	2.8	2.8	–	1.9	2.8	V
	–	a	10	5.2	5.2	5.2	5.2	–	3.9	5.2	
	–	a	15	7.4	7.4	7.4	7.4	–	5.8	7.4	
	–	b	5	3.2	3.2	3.2	3.2	–	2.3	3.2	
	–	b	10	6.6	6.6	6.6	6.6	–	5.1	6.6	
	–	b	15	9.6	9.6	9.6	9.6	–	7.3	9.6	
Hysteresis Voltage V_H Min.	–	a	5	0.3	0.3	0.3	0.3	0.3	0.9	–	V
	–	a	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	a	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
	–	b	5	0.3	0.3	0.3	0.3	0.3	0.9	–	
	–	b	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	b	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
V_H Max.	–	a	5	1.6	1.6	1.6	1.6	–	0.9	1.6	V
	–	a	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	a	15	5	5	5	5	–	3.5	5	
	–	b	5	1.6	1.6	1.6	1.6	–	0.9	1.6	
	–	b	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	b	15	5	5	5	5	–	3.5	5	

[a] Input on terminals 1,5,8,12 or 2,6,9,13; other inputs to V_{DD}.
[b] Input on terminals 1 and 2, 5 and 6,8 and 9, or 12 and 13; other inputs to V_{DD}.

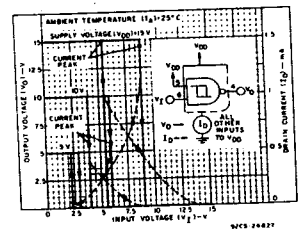


Fig. 4 – Typical current and voltage transfer characteristics.

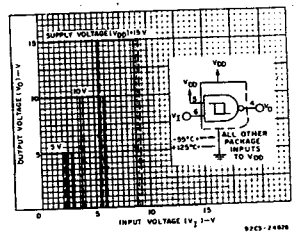


Fig. 5 – Typical voltage transfer characteristics as a function of temperature.

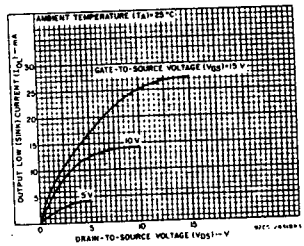


Fig. 6 – Typical output low (sink) current characteristic

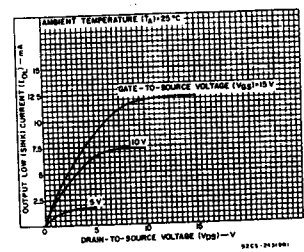


Fig. 7 – Minimum output low (sink) current characteristics.

CMOS AND Gates

High-Voltage Types (20-Volt Rating)

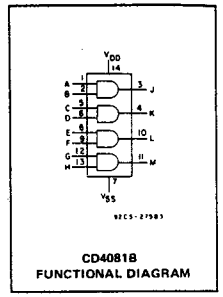
CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

The RCA-CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

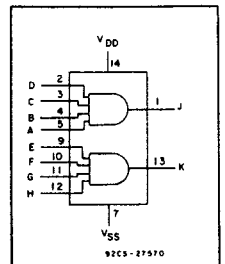
The CD4073B, CD4081B and CD4082B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

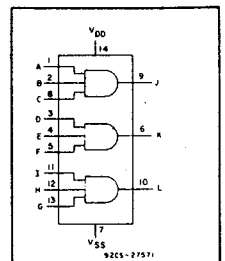
- Medium-Speed Operation – t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4081B
FUNCTIONAL DIAGRAM



CD4082B
FUNCTIONAL DIAGRAM



CD4073B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, K, H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5	–	5	1.5				—	—	1.5	V
	1	–	10	3				—	—	3	
	1.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

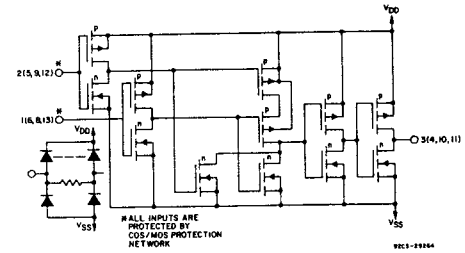


Fig. 1 – Schematic diagram for CD4081B (1 of 4 identical gates).

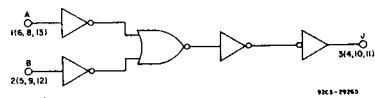


Fig. 2 – Logic diagram for CD4081B (1 of 4 identical gates).

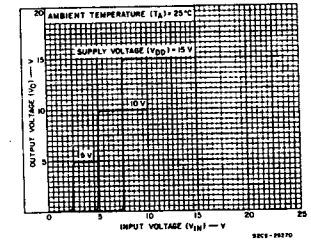


Fig. 3 – Typical voltage transfer characteristics.

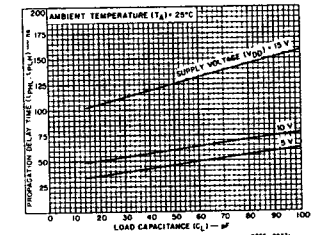


Fig. 4 – Typical propagation delay time as a function of load capacitance.

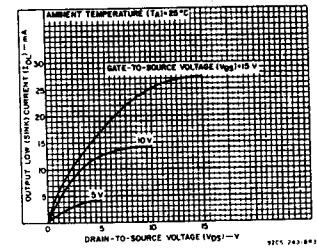


Fig. 5 – Typical output low (sink) current characteristics.

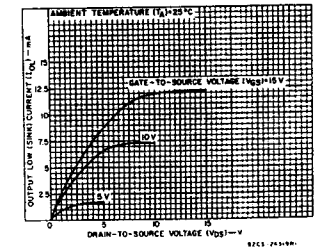


Fig. 6 – Minimum output low (sink) current characteristics.

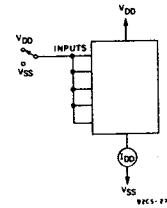


Fig. 15 – Quiescent device current test circuit.

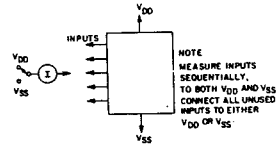


Fig. 16 – Input current test circuit.

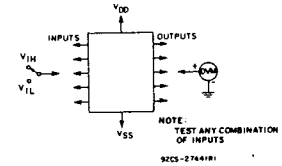
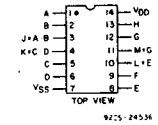
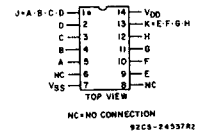


Fig. 17 – Input-voltage test circuit.

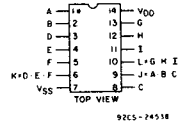
TERMINAL ASSIGNMENTS



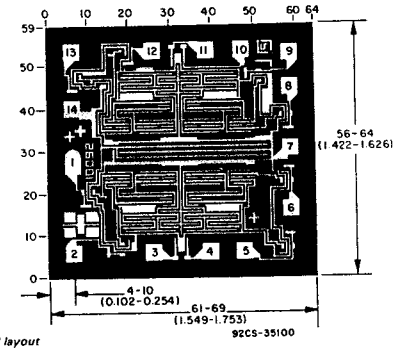
CD4081B



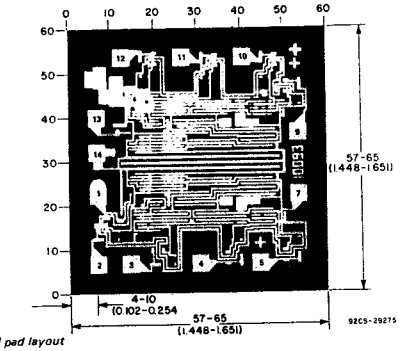
CD4082B



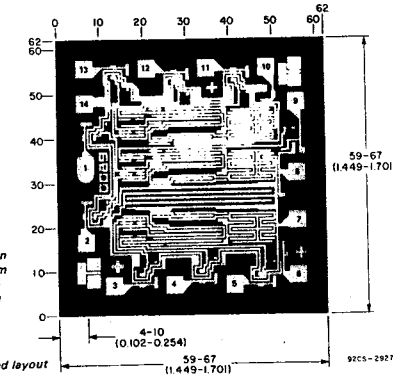
CD4073B



Dimensions and pad layout for CD4081B.



Dimensions and pad layout for CD4082B.



Dimensions and pad layout for CD4073B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

National Semiconductor

Industrial Blocks

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CH and LM565CN are specified for operation over the 0°C to +70°C temperature range.

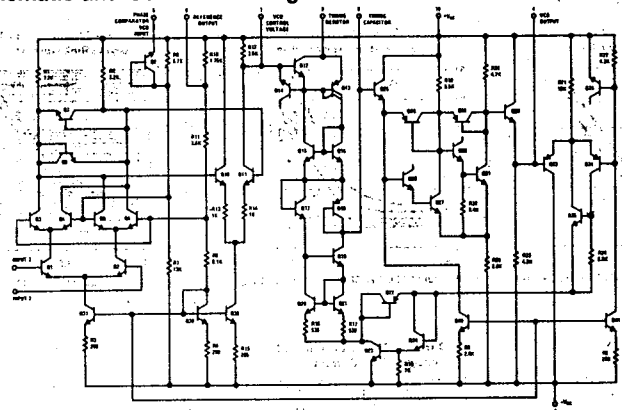
Features

- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%.

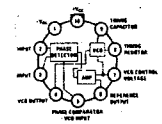
Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators.

Schematic and Connection Diagrams

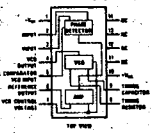


Metal Can Package



Order Number LM565H or LM565CH
See NS Package H10C

Dual-In-Line Package



Order Number LM565CN
See NS Package N14A

Absolute Maximum Ratings

Supply Voltage		±12V
Power Dissipation (Note 1)		300 mW
Differential Input Voltage		±1V
Operating Temperature Range	LM565H	−55°C to +125°C
	LM565CH, LM565CN	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

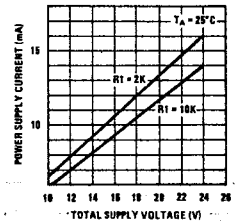
Electrical Characteristics (AC Test Circuit, $T_A = 25°C$, $V_C = ±6V$)

PARAMETER	CONDITIONS	LM565			LM565C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	C_o = 2.7 pF	300	500		250	500		kHz
Operating Frequency Temperature Coefficient			−100	300		−200	500	ppm/°C
Frequency Drift with Supply Voltage			0.01	0.1		0.05	0.2	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2	0.75		0.5	1	%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20	100		20		ns
Square Wave Fall Time			50	200		50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	f_o = 10 kHz	6400	6600	6800	6000	6600	7200	Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	350	200	300	400	mV_{pp}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D		0.6	.68	0.9	0.55	.68	0.95	V/radian

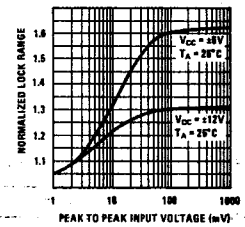
Note 1: The maximum junction temperature of the LM565 is 150°C, while that of the LM565C and LM565CN is 100°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case. Thermal resistance of the dual-in-line package is 100°C/W.

Typical Performance Characteristics

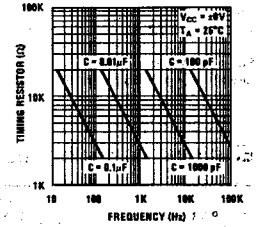
Power Supply Current as a Function of Supply Voltage



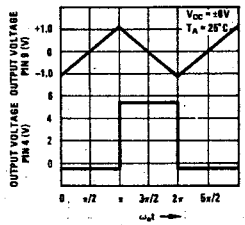
Lock Range as a Function of Input Voltage



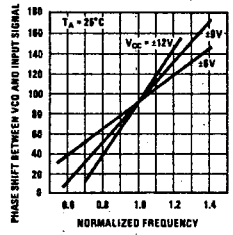
VCO Frequency



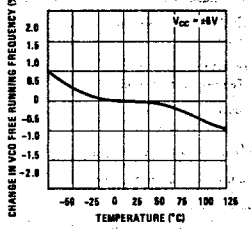
Oscillator Output Waveforms



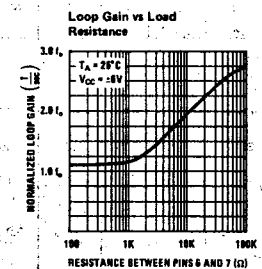
Phase Shift vs Frequency



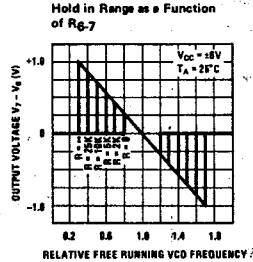
VCO Frequency as a Function of Temperature



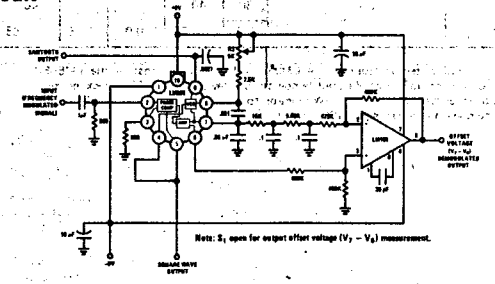
Loop Gain vs Load Resistance



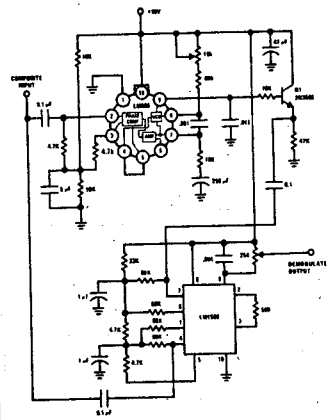
Hold in Range as a Function of R_{6-7}



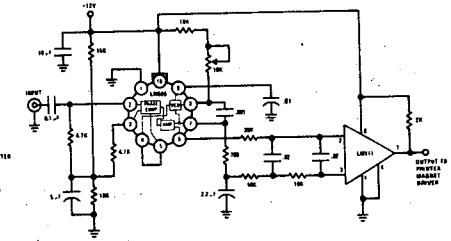
AC Test Circuit



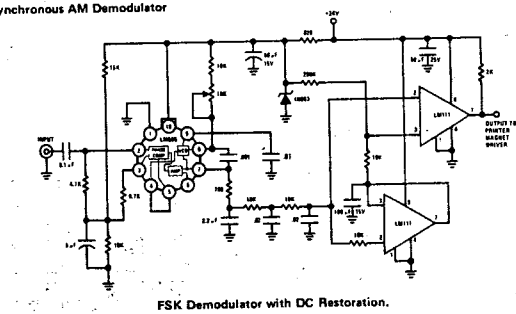
Typical Applications



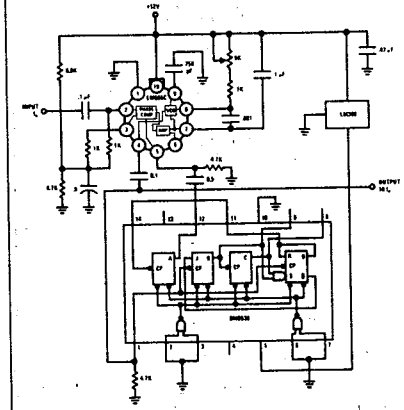
2400 Hz Synchronous AM Demodulator



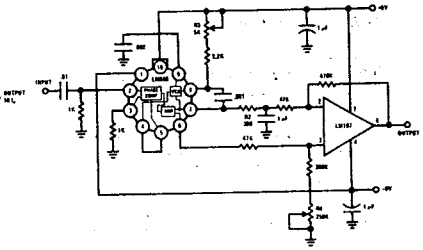
FSK Demodulator (2025-2225 cps)



FSK Demodulator with DC Restoration.



Frequency Multiplier (x10)



IRIG Channel 13 Demodulator

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{1}{3.7\, R_0 C_0}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient".

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

K_o = oscillator sensitivity $\left(\frac{\text{radians/sec}}{\text{volt}}\right)$

K_D = phase detector sensitivity $\left(\frac{\text{volts}}{\text{radian}}\right)$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit.

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

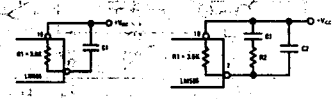
$$f_H = \pm \frac{8\, f_o}{V_c}$$

f_o = free running frequency of VCO

V_c = total supply voltage to the circuit.

THE LOOP FILTER

In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7) this filter may take one of two forms:



Simple Lag Filter | Lag-Lead Filter

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_oK_d$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

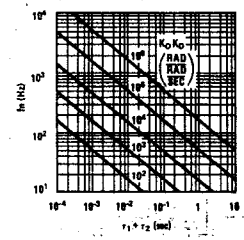
$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1$$

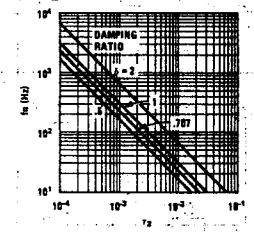
R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \simeq \pi \tau_2 f_n$$

These two equations are plotted for convenience.



Filter Time Constant vs Natural Frequency



Damping Time Constant vs Natural Frequency

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\ C_1$.

7490, LS90
Counters

Decade Counter
Product Specification

Logic Products

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain a divide-by-five operation at the Q_3 output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N7490N, N74LS90N

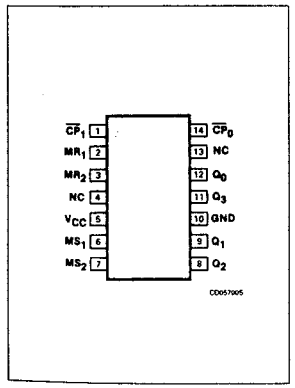
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

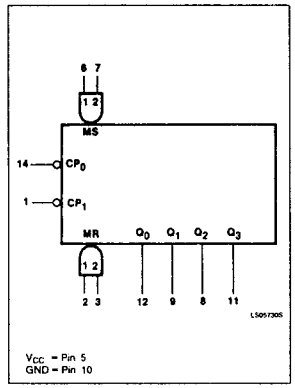
PINS	DESCRIPTION	74	74LS
$\overline{CP}_0$	Input	2ul	6LSul
$\overline{CP}_1$	Input	4ul	8LSul
MR, MS	Inputs		1ul
$Q_0 - Q_3$	Outputs	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

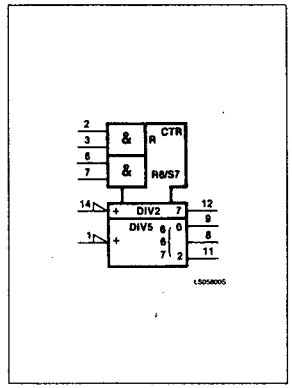
PIN CONFIGURATION



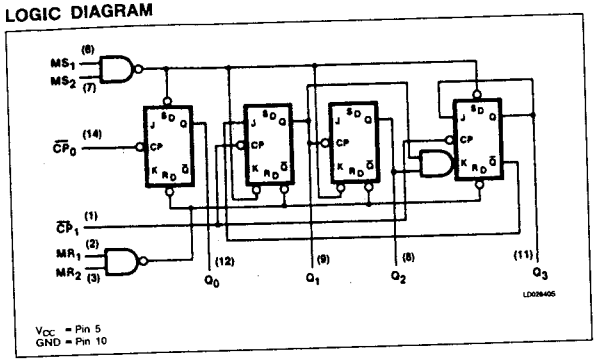
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 5
GND = Pin 10

MODE SELECTION — FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
H	L	L	X	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE — FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE:
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70		°C

NOTE:
V_{IN} is limited to +5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs on the 74LS90 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			−800			−400	μA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			7490			74LS90			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)						0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	All inputs '90			1.0				mA
			V_I = 7.0V	MR, MS inputs						0.1	mA
			V_I = 5.5V	$\overline{CP}_0$ input						0.2	mA
				$\overline{CP}_1$ input						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	MR, MS inputs			40				μA
				$\overline{CP}_0$ input			80				μA
				$\overline{CP}_1$ input			160				μA
			V_I = 2.7V	MR, MS inputs						20	μA
				$\overline{CP}_0$ input[5]						40	μA
				$\overline{CP}_1$ input[5]						80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	MR, MS inputs			−1.6			−0.4	mA
				$\overline{CP}_0$ input			−3.2			−2.4	mA
				$\overline{CP}_1$ input			−6.4			−3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−18		−55	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				30	53		9	15	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS90 only is 80μA for $\overline{CP}_0$ and 160μA for $\overline{CP}_1$ inputs.

5

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

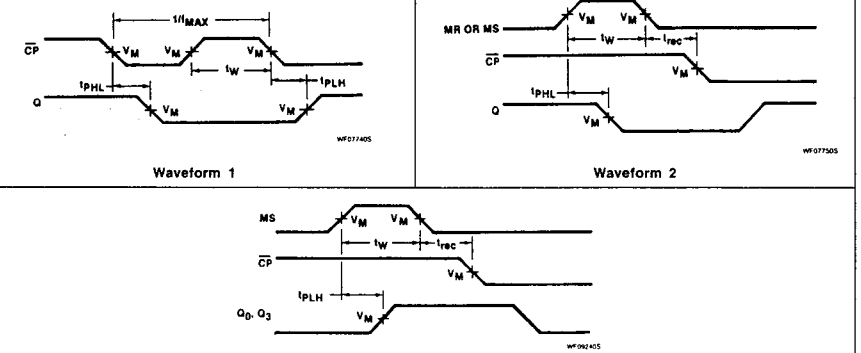
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	Min	Max	
f_{MAX} f_{MAX}	Input count frequency, $\overline{CP}_0$ to Q_0 Input count frequency, $\overline{CP}_1$ to Q_1	Waveform 1	10 10		32 16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1				16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		100 100		48 50	ns
t_{PHL}	MR input to any output	Waveform 2				40	ns
t_{PLH}	MS input to Q_0 and Q_3 outputs	Waveform 3				30	ns
t_{PHL}	MS input to Q_1 and Q_2 outputs	Waveform 2				40	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		30		ns
t_W	MS, MR pulse width	Waveform 2	50		15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2			25		ns
t_{rec}	Recover time, MS to $\overline{CP}$	Waveforms 2 & 3			25		ns

AC WAVEFORMS



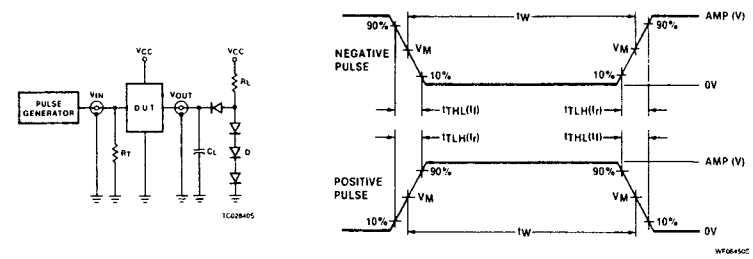
Waveform 1

Waveform 2

For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74 LS
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Function Table.

Waveform 3

TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

5

ICM7217 Series
ICM7227 Series
4-Digit CMOS Up/Down Counter/ Display Driver

FEATURES

- **Four decade, presettable up-down counter with parallel zero detect**
- **Settable register with contents continuously compared to counter**
- **Directly drives multiplexed 7 segment common anode or common cathode LED displays**
- **On-board multiplex scan oscillator**
- **Schmitt trigger on count input**
- **TTL compatible BCD I/O port, carry/borrow, equal, and zero outputs**
- **Display blank control for lower power operation; quiescent power dissipation < 5mW**
- **All terminals fully protected against static discharge**
- **Single 5V supply operation**

DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to .8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

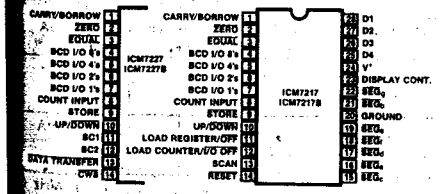
The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

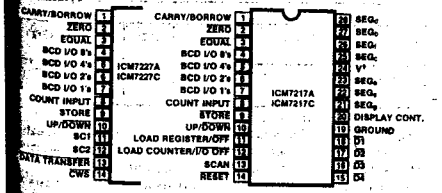
To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2 MHz, although the device will typically run with f_{in} as high as 5 MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750 kHz maximum.

PIN CONFIGURATIONS (outline dwgs JI, PI)



COMMON ANODE



COMMON CATHODE

ORDERING INFORMATION

Display Option	Count Option Max Count	28-LEAD Package	Order Part Number
Common Anode	Decade/9999	CERDIP	ICM7217IJI
Common Cathode	Decade/9999	PLASTIC	ICM7217AIPI
Common Anode	Timer/5959	CERDIP	ICM7217BIJI
Common Cathode	Timer/5959	PLASTIC	ICM7217CIPI
Common Anode	Decade/9999	CERDIP	ICM7227IJI
Common Cathode	Decade/9999	PLASTIC	ICM7227AIPI
Common Anode	Timer/5959	CERDIP	ICM7227BIJI
Common Cathode	Timer/5959	PLASTIC	ICM7227CIPI

6

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (common anode/Cerdip) ..... 1W Note 1
Power Dissipation (common cathode/Plastic) ... 0.5W Note 1
Supply Voltage $V^+ - V^-$ 6V
Input Voltage
(any terminal) ..... V^+ +0.3V, Ground -0.3V Note 2
Operating temperature range ..... -20°C to +85°C
Storage temperature range ..... -55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

OPERATING CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $T_A = 25°C$, Test Circuit, Display Diode Drop 1.7V, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply current (Lowest power mode)	I^+ (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 3)		350	500	µA
Supply current (Lowest power mode)	I^+ (7227)	Display off (Note 3)		300	500	µA
Supply current OPERATING	I_{OP}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver output current	I_{DIG}	Common anode, $V_{OUT} = V^+ - 2.0V$	140	200		mA peak
SEGment driver output current	I_{SEG}	Common anode, $V_{OUT} = +1.3V$	-25	-40		mA peak
Digit Driver output current	I_{DIG}	Common cathode, $V_{OUT} = +1.3V$	-75	-100		mA peak
SEGment driver output current	I_{SEG}	Common cathode $V_{OUT} = V^+ - 2V$	10	12.5		mA peak
$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	I_P	$V_{OUT} = V^+ - 2V$ (See Note 3)	5	25		µA
3 level input impedance	Z_{IN}			100		kΩ
BCD I/O input high voltage	V_{BIH}	ICM7217 common anode (Note 4) ($V^+ = 5.0V$)	1.3			V
		ICM7217 common cathode (Note 4)	$V^+ - 0.8$			V
		ICM7227 with 50pF effective load	3			V
BCD I/O input low voltage	V_{BIL}	ICM7217 common anode (Note 4) ($V^+ = 5.0V$)			0.8	V
		ICM7217 common cathode (Note 4)			$V^+ - 1.8$	V
		ICM7227 with 50pF effective load			1.5	V
BCD I/O input pullup current	I_{BPU}	ICM7217 common cathode $V_{IN} = V^+ - 2V$ (Note 3)	5	25		µA
BCD I/O input pulldown current	I_{BPD}	ICM7217 common anode $V_{IN} = +1.3V$ (Note 3)	5	25		µA
BCD I/O, CARRY/BORROW, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high current	I_{BOH}	$V_{OH} = V^+ - 1.5V$	100			µA
BCD I/O, CARRY/BORROW, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low current	I_{BOL}	$V_{OL} = +0.4V$	-2			mA
Count input frequency (Guaranteed)	f_{in}	$V^+ = 5V \pm 10\%$, $-20°C < T_A < +70°C$	0	5	2	MHz
Count input threshold	V_{TH}	$V^+ = 5V$		2		V
Count input hysteresis	V_{HYS}	$V^+ = 5V$		0.5		V
Display scan oscillator frequency	f_{ds}	Free-running (SCAN terminal open circuit)		2.5		kHz
Operating Temperature Range	T_A	Industrial temperature range	-20		+85	°C

NOTE 1 These limits refer to the package and will not be obtained during normal operation.

NOTE 2 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

NOTE 3 In the ICM7217 the UP/$\overline{DOWN}$, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 µA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.

NOTE 4 These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as the input logic zero for ICM7217 common-cathode versions.

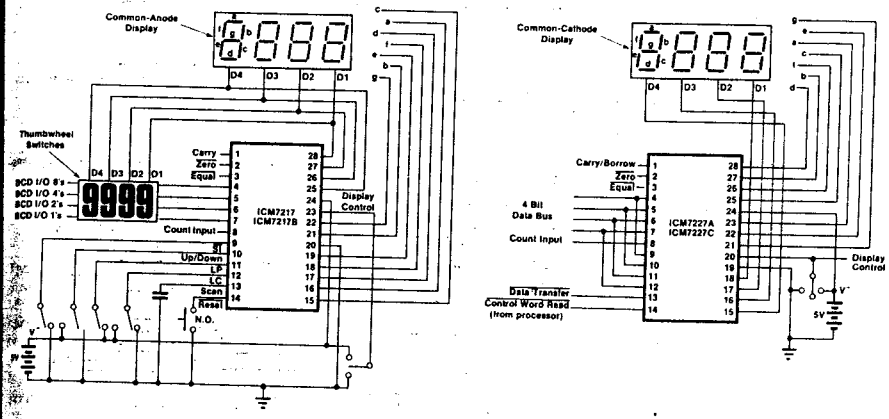


Figure 1: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

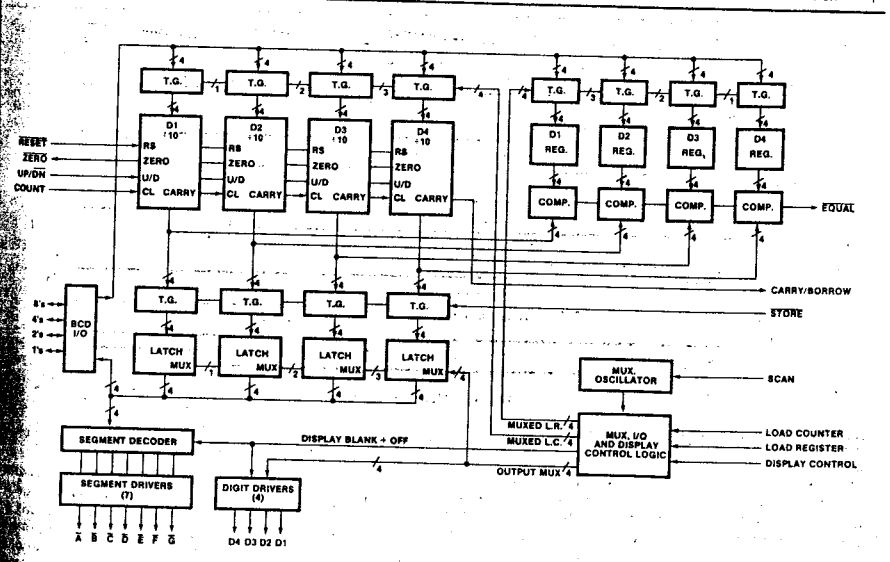


Figure 2: ICM7217 Functional Block Diagram