MICROCONTROLLER BASED ENERGY SAVER FOR MONOBLOCK PUMP

P-210

PROJECT REPORT

Submitted by

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COIMBATORE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE - 641 006

CERTIFICATE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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CERTIFICATE

This is to certify that the project entitled

MICROCONTROLLER BASED ENERGY SAVER FOR MONOBLOCK PUMP

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Date: 15.3.2002

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was examined in Project Work Viva-Voce Examination held on .....

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13.03.2002

CERTIFICATE

This is to certify that the following final year B.E., (E.E.E.) students of Kumaraguru College of Technology, Coimbatore *have carried out a project work in our organization from 01.12.2001 to 04.03.2002.*

1.D.SATISH KUMAR(98EEE46)

2.R.BALU(98EEE08)

3.C.PREMCHAND(98EEE37)

4.N.SUDHAKARAN(98EEE51)

The title of the project was "Micro controller based energy saver for monoblock pump". *During this period their attendance and conduct were found to be* good. *We wish them very best for a prosperous future.*

For DECCAN INDUSTRIES

Partner

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We wish to express our deep sense of gratitude and indebtedness to our project guide Mrs. D. Somasundareswari M.E., Senior Lecturer, department of Electrical and Electronics Engineering, for her invaluable guidance and constructive suggestions, the keen and constant inspiration and interest evinced by her at all stages right from the inception to the completion.

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We are thankful to our industrial guide, Mr. K.K. Veluchamy, Managing Director, Deccan Pumps for his meticulous help rendered to us to complete our project within the stipulated time.

SYNOPSIS

SYNOPSIS

At high voltage levels, power factor related issues are felt as economical impacts, that any small change of improvement reveals itself into significant savings in energy as well as money.

A power factor control scheme for saving energy using switched capacitor is advanced in this project. The load voltage and current are continuously sampled and fed to microcontroller through a comparator. The microcontroller then computes the power factor and gives the signal to energize or de-energize the relays which are used to switch the capacitors. Resolution of the system can be increased by increasing the number of capacitor banks. The system is designed on single phase basis with six capacitors using 89C51 microcontroller.

CONTENTS

CONTENTS

INTRODUCTION

CHAPTER I

INTRODUCTION

Present day rural distribution networks are predominant connected with reactive load having very low lagging power factor contributing for increased current and poor voltage regulation. If the receiving end voltage of the distribution is to be maintained within reasonable limits, the network should have adequate reactive power support.

The method adopted consists of automatic switched capacitor scheme comprising of a bank of L.T., capacitors of rating suitable for maximum KVAR requirement of concerned L.T., distribution with necessary provision of switching a suitable value of capacitor bank, such that, the remaining capacitor bank suits to reactive KVA demand of the system at a particular period of time.

Capacitor across individual consumers gives the benefit of loss reduction and voltage improvement to the maximum extent possible and also acts as automatic switched capacitor without using semi-automatic switch gear.

1.1 Reactive Power

Power and distribution Transformers, Motors and bulk of the other electrical appliances used in industrial agricultural commercial and domestic sectors require magnetic fields for their operations. To establish the magnetic field and sustain it we require reactive power that is power arising from energy which is temporarily stored in the load for part of A.C. cycle and returned to the system at a later stage in the cycle the energy is stored in one of the two ways, first and most commonly inductive i.e. in the magnetic field associated with electric motors i.e. agricultural motors, power looms, fluorescent lights and long over head conductors and secondly capacitive i.e. as a stored charge in the insulation of under ground cables. This characteristics of the load, is described by its power factor which may be expressed as

$$\text{Power Factor} = \frac{\text{Real power}}{\text{Apparent Power}}$$

The two mechanism of energy storage are complementary in that they are time shifted such that they occur at different stages of the AC cycle to the extent that while first one is stored energy, the other is returning its stored energy to the system and vice versa. This time shift is expressed as the sign of the power factor (negative or lagging for inductive loads and positive or leading for capacitive loads)

The reactive power is generated in the grid by (1) Generators (2) EHV Transmission lines (3) Synchronous condensers & (4) HT/LT shunt capacitors. The reactive power is consumed by (a) the inductive loads and (b) transmission and Distribution lines and transformers, as reactive losses. If the available reactive power matches with the reactive power requirement, then the grid voltage profile is good. When there is mismatch, it leads to under/over voltage conditions and the grid experience voltage instability.

1.2 Need for Reactive Compensation

The presence of loads with a large requirement for reactive power is detrimental to the power system. An increase of such loads does not contribute to utilizing the real power, in the sense that the reactive power cannot be extracted as energy by the consumers. It does however lead to very real increase in the current flows on the power system and hence contributes to the system losses. Thus, supply of additional unwanted reactive power, as in the case of highly inductive loads, like arc furnace etc. has to be done at the cost of useful power, which not only is uneconomical but also results into system instability, because of limited capability of generators to supply reactive power for a power system. The power transformers get unnecessarily loaded due to high reactive power requirement and net 'Real Power Availability' for the system gets reduced. Also this leads to excessive voltage regulation and the consequent low voltage at the extremities of the system. These higher current flows for the same 'real power' due to large transfers of reactive power can be ameliorated by the introduction of sources of reactive power close to the load. This is described as 'reactive compensation' and may take the form of

dynamic compensation (i.e.) rotating machines, whose excitation can be varied so that the device may either generate or absorb reactive power ;or static compensation (i.e.) shunt capacitor banks which are in general, only variable in their application by being switched in or out.

In our project, the power factor control is achieved by three units,

1. Power Factor measurement unit
2. Control unit
3. Power Factor Improvement unit

In practice most of distribution circuits catering inductive loads selected for the study, power factor was found to be in the range of 0.6 to 0.75 from this it is inferred that large number of distribution circuits supplying power to inductive consumer have low power factor which can be improved around unity by application of shunt capacitors.

The percent reduction in losses after application of capacitors in terms of losses of a distribution system before application of capacitors can be calculated by:

The saving in line losses expressed as a

Percentage of former value losses = [1-{cos□1/cos□2}]

The general block diagram of the project is shown in Fig.1.

In general, capacitor, by reducing peak load feeder voltage drops, allows greater feeder loads to be carried. Also capacitors by reducing KVA loads, release substation and generation capacity. The application of shunt capacitors to a distribution feeder catering inductive consumers produces a uniform voltage boost per unit length of line, out to its point of application.

The fundamental KVAR and KW relations in a circuit when the power factor is improved are readily portrayed in the Fig.2.

The following relations define some of the properties of the figure, regarding released capacity in inductive equipment which has a current magnitude as the limiting factor.

Capacitor KVAR to go from □1 to □2

CKVA= KVA 1 (sin□1-(cos□1 * sin□2)/cos□2)

Resultant KVA at □2

KVA 2=KVA 1 cos□1/cos□2

The KVA released (KVA)-KVA 1

((KVA/KVA 1 (sin□1-1) + 1- [(KVA 2/KVA1^2] cos^2 □1

Released KW=released KVA cos□1

1.3 Power Factor Measuring Unit

The power factor measuring unit consists of

1. A voltage transformer to measure voltage
2. A current transformer to measure current
3. A comparator for both voltage and current, for converting the analog signal to the corresponding pulses (positive)

1.4 Control Unit

The control unit consists of

1. A microcontroller unit in which the microcontroller reads the phase angle pulse and finds out the corresponding power factor and displays it and takes decision to either connect or disconnect the relays.
2. Relay unit to send the control signal to the contractor to either connect or disconnect the capacitor bank connected to it corresponding from the microcontroller.

1.5 Power Factor Improvement Unit

Power factor improvement unit consists of capacitor banks which leading KVAR to the supply voltage and improves the corresponding voltage.

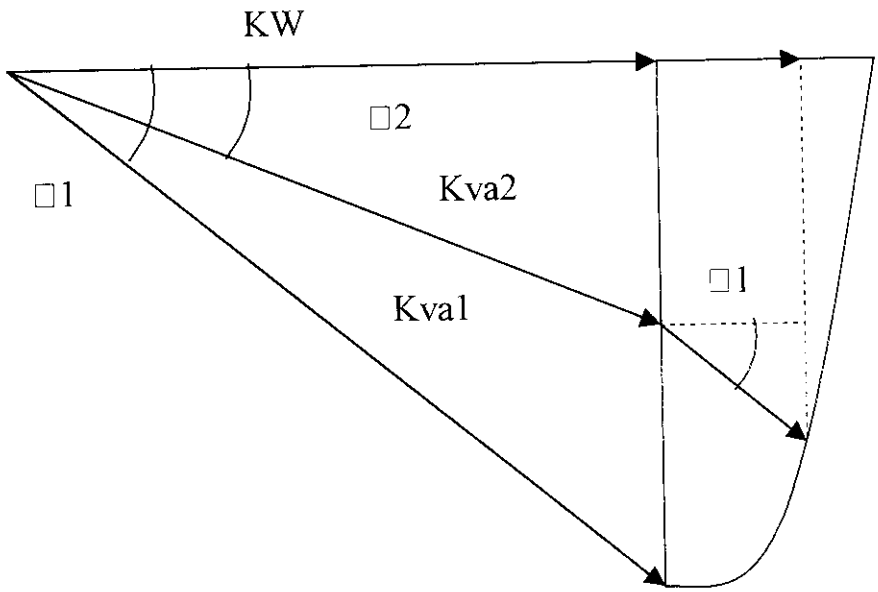


Fig.2 Phasor Diagram

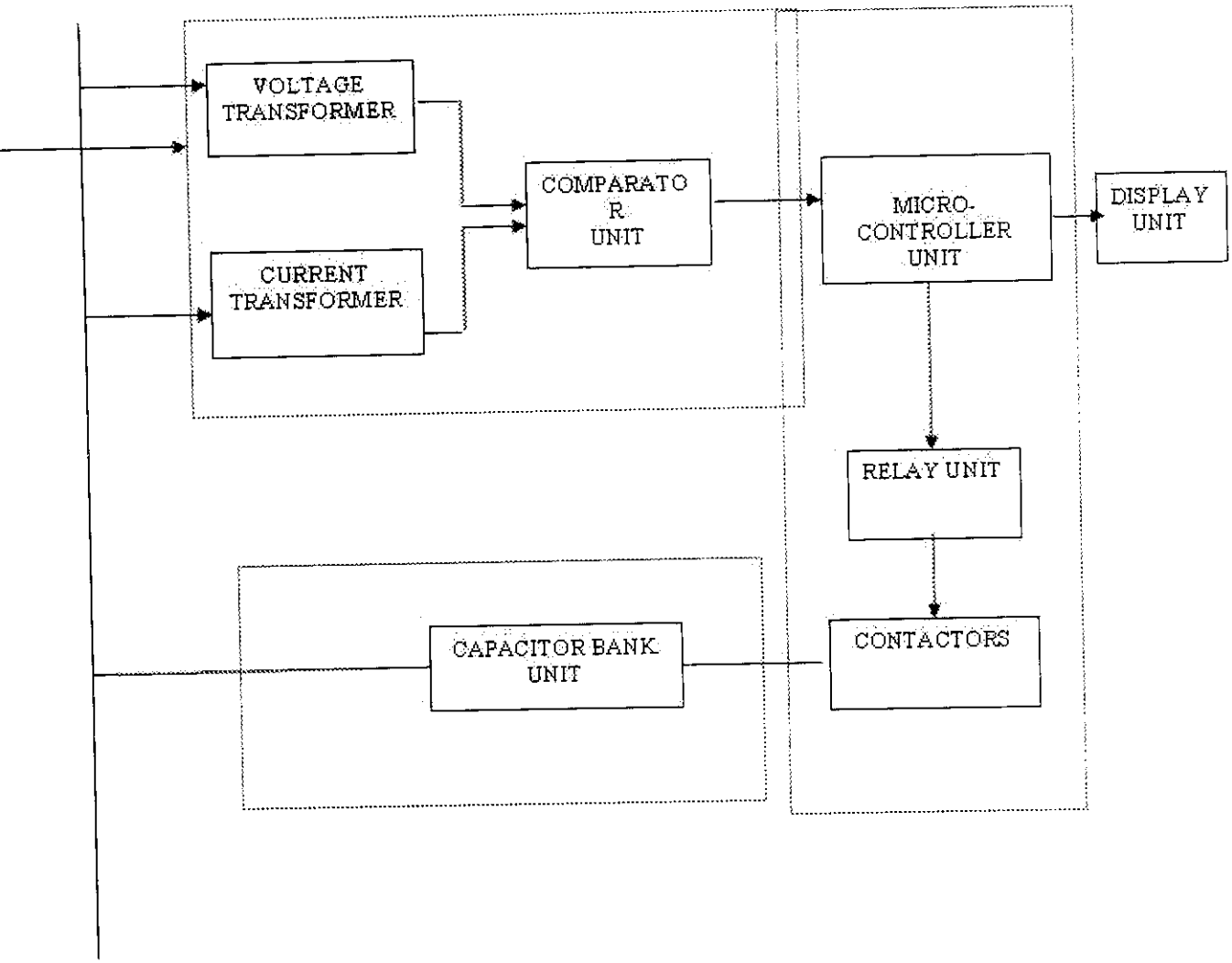


Fig.1 General Block Diagram

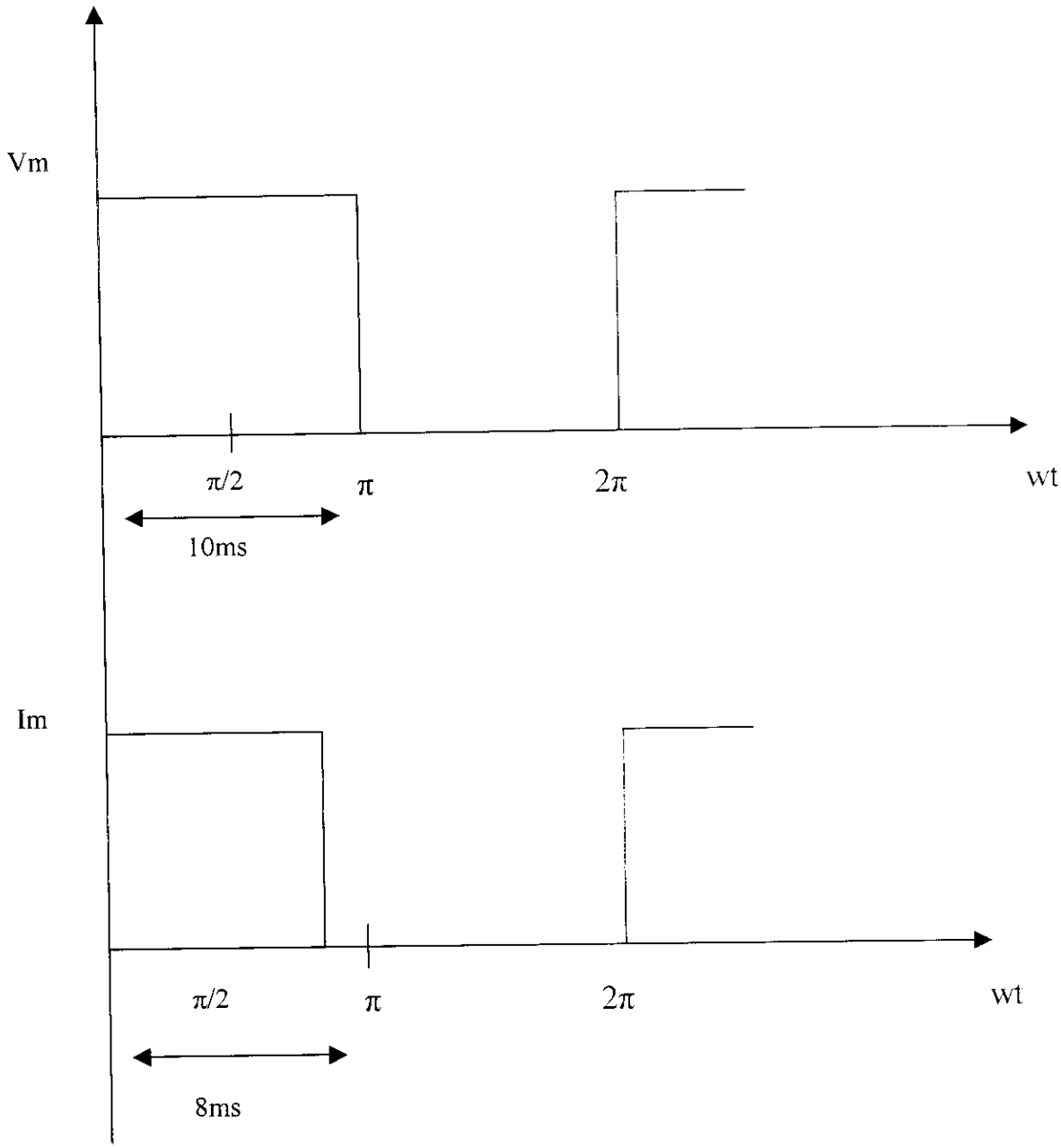


Fig.3 Comparator Output Waveforms

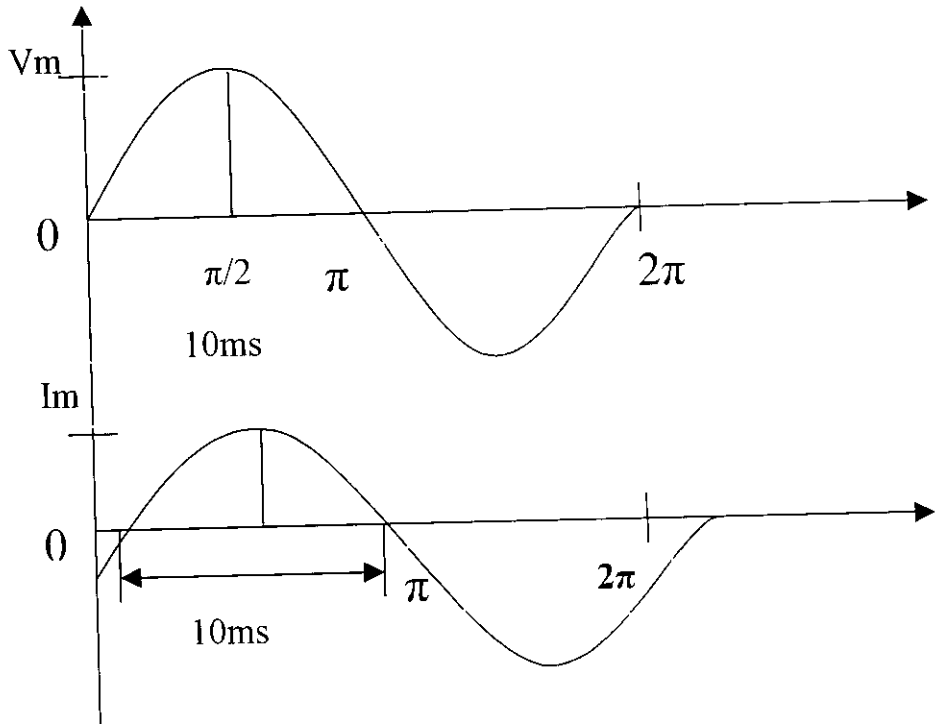


Fig.4 Voltage and Current Waveforms

HARDWARE

CHAPTER II

HARDWARE

2.1 Power Factor Measuring Unit

a) Potential Transformer

Specifications:

Primary→ 230V AC

Secondary→ 0-2V AC, 50mA
0-12.5V AC, 1.5A

It measures the circuit voltage and the 2V input is used for the input to comparator circuit

b) Current Transformer

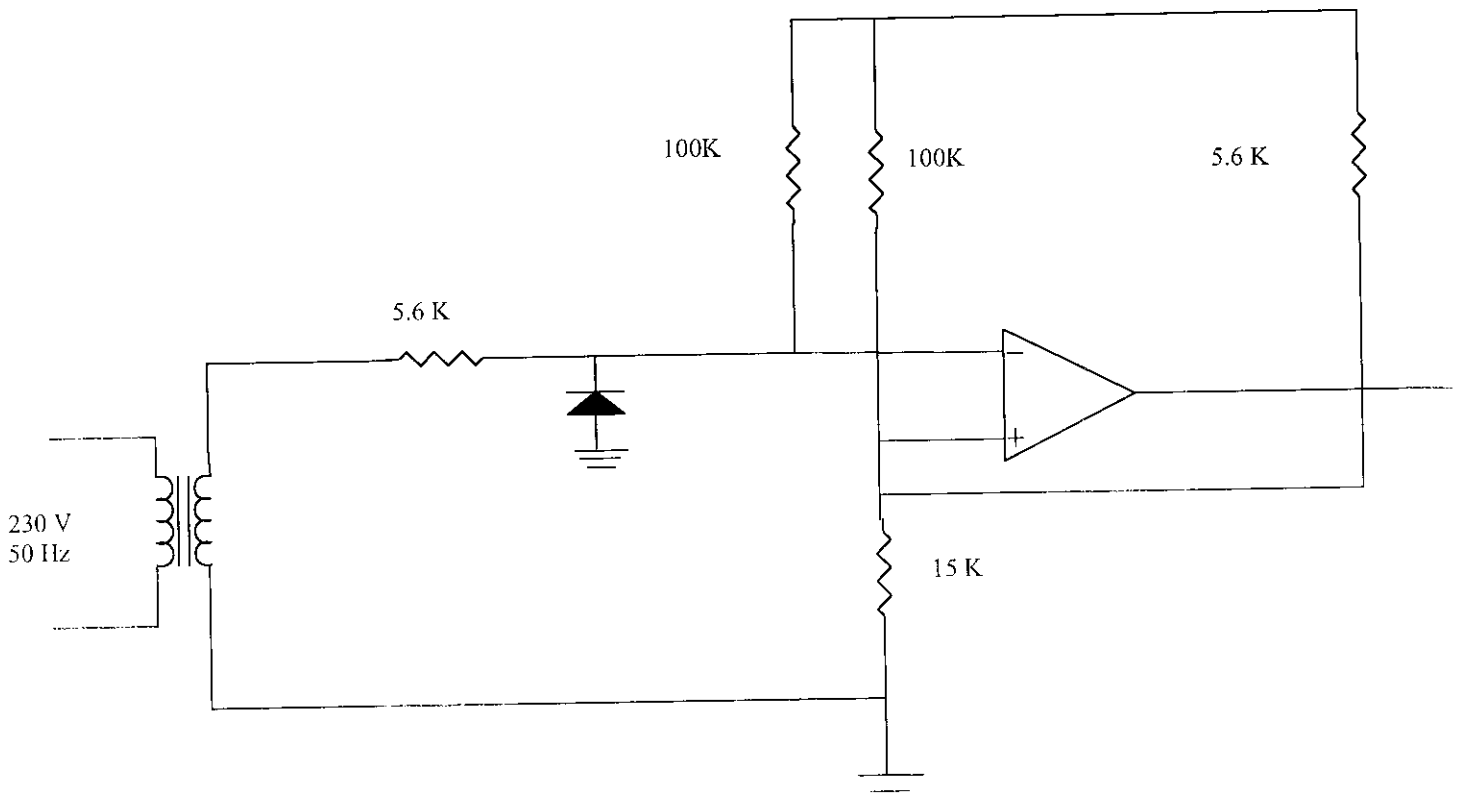
Specifications:

Primary→ 10A

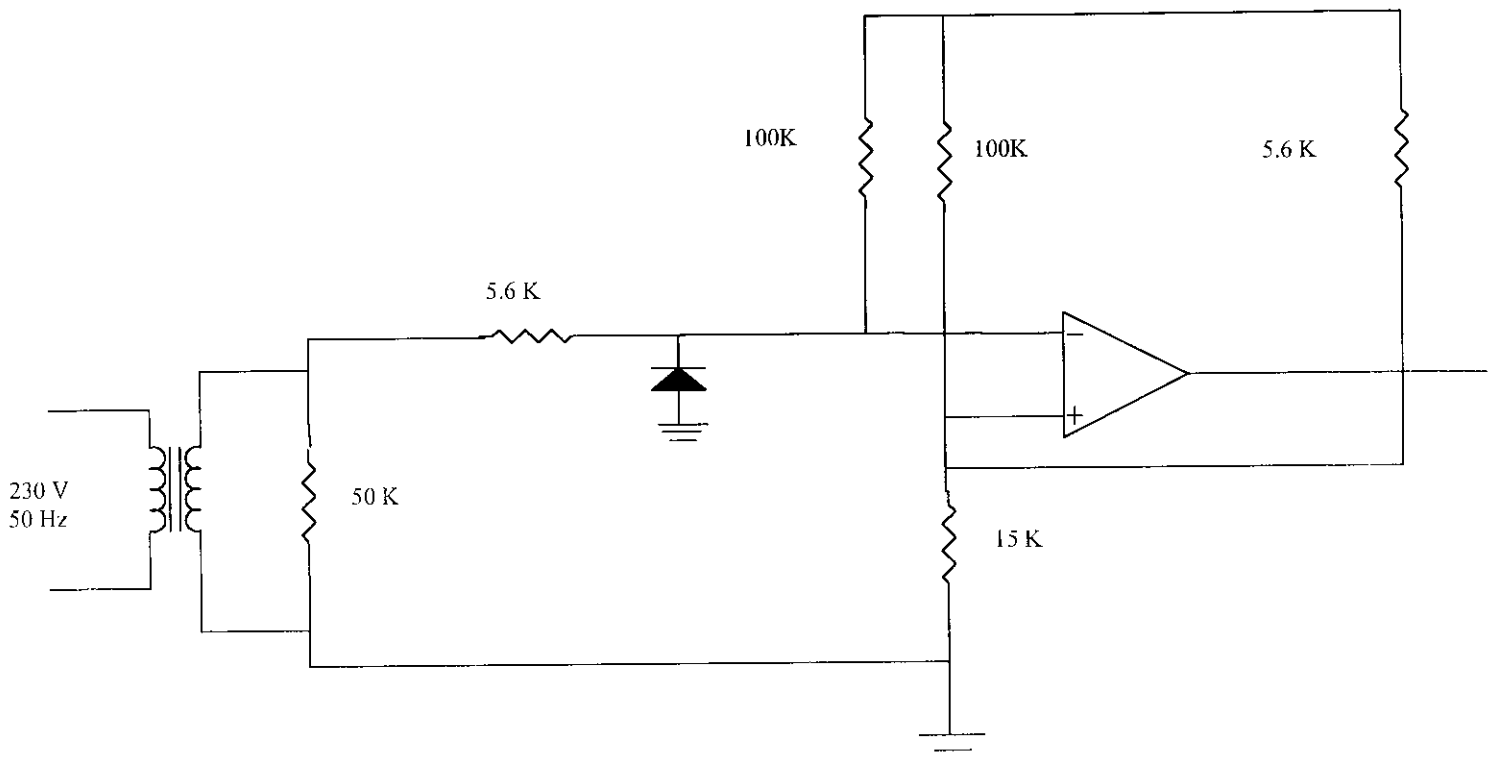
Secondary→ 1A

It measures the current on the mains and the reactive current is fed to the comparator circuit. For heavy loads the C.T. can be replaced by suitable ratios.

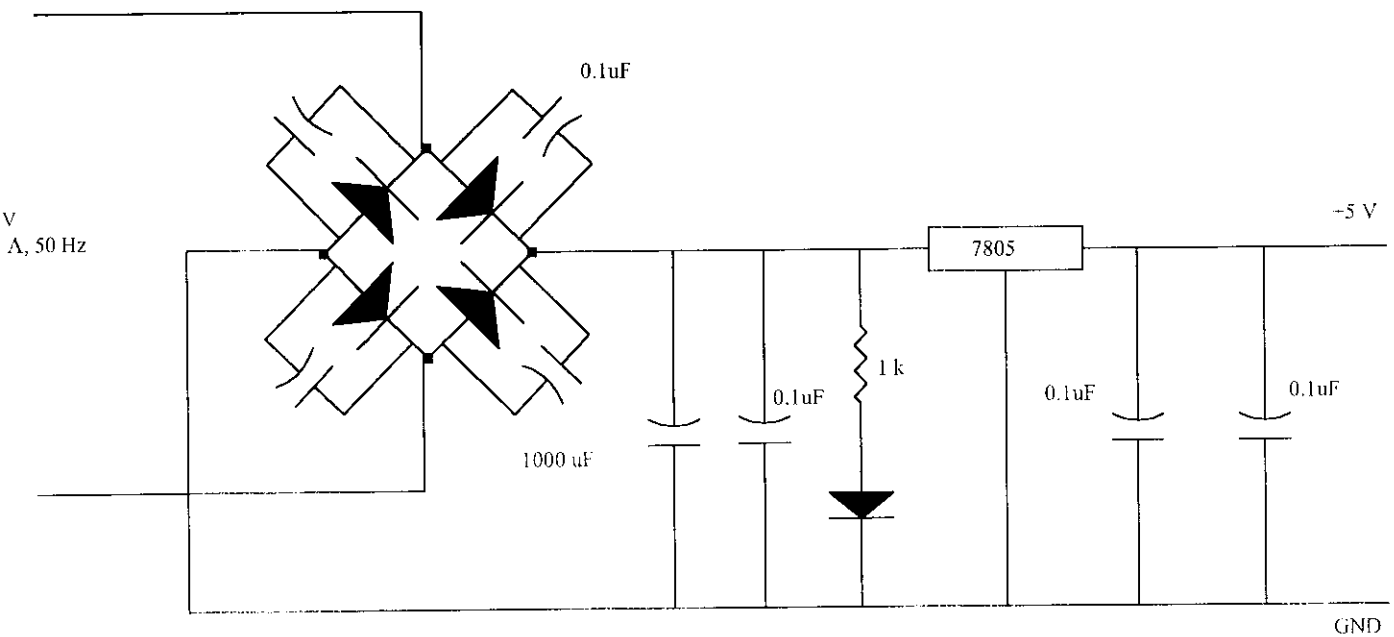
VOLTAGE COMPARATOR CIRCUIT



CURRENT COMPARATOR CIRCUIT



POWER SUPPLY CIRCUIT



c) Comparator

Specifications:

IC LM339 (16 PIN)
Supply- +5V and GND

It has 4 comparators of which two are utilized each one for voltage input and reactive current input. The C/K setting for the comparator is set. The C/K setting is set manually by the formula

Transformer ratios: It/5 = K

Reactive current adjustments, C/K = Ic/K

Where It = rated transformer current

Ic = current of the first capacitor

Example:

Transformer ratio: K = 500/5A = 100

First capacitor = 60 KVAR, 400 V
= 86.7 A

C/K setting control = Ic/K = 86.7/100 = 0.867

Thus the voltage and current inputs are transformed into positive pulses as shown in the fig.4

2.2 Control Unit

The control unit is based on the micro electronic technology, a well proven single board micro controller unit which uses an 89C51 micro controller to get the input, process the data and make complex decisions to either connect or disconnect the capacitor bank and to provide signals to display the power factor value.

The control unit consists of:

1. 89C51 controller
2. Relay unit

2.2.1 Microcontroller Unit [89C51]

Microcontroller is a general-purpose device meant to read data and perform limited calculations on that data and control its environment based on those calculations. The prime use of microcontroller is to control the operation of

a machine using a fixed program that is stored in ROM and that does not change over the lifetime of the system.

The microcontroller design uses a much more limited set of single-and double-byte instructions that are used to move code and data from internal memory to the ALU. The microcontroller is concerned with getting data from and to its own pins; the architecture and instruction set are optimized to handle data in bit and byte size.

a) Features Unique to Microcontrollers

Internal ROM and RAM

I/O ports with programmable pins

Timers and counters

Serial data communication

b) Specific features of 89C51 Architecture

- Eight-bit CPU with registers A(the accumulator) and B
- Sixteen-bit program counter(PC) and data pointer (DPTR)
- Eight-bit program status word (PSW)
- Eight-bit stack pointer (SP)

- Internal ROM or EEPROM
- Internal RAM of 128 bytes:
    - Four register banks, each containing eight registers
    - Sixteen bytes, which may be addressed at the bit level
    - Eighty bytes of general-purpose data memory

- Thirty-two input/output pins arranged as four 8-bit ports: P0-P3
- Two 16-bit timer/counters: T0 and T1
- Full duplex serial data receiver/transmitter: SBUF
- Control registers: TCON, TMOD, SCON, PCON, IP, AND IE
- Two external and three internal interrupt sources
- Oscillator and clock circuits

c) 89C51 Oscillator and Clock

The heart of the 89C51 is the circuitry that generates the clock pulses by which all internal operations are synchronized. Microcontroller can run at specified maximum and minimum frequencies, typically 1 megahertz to 16 megahertz.

d) Program Counter and Data pointer

The 89C51 contains two 16-bit registers: the program counter (PC) and the data pointer (DPTR). Each is used to hold the address of a byte in memory. The PC is automatically incremented after every instruction byte is fetched. The PC is the only register that does not have an internal address.

The DPTR register is made up of two 8-bit registers, named DPH and DPL, which are used to furnish memory address for internal and external code access and external data access.

e) A and B CPU registers

The 89C51 contains 34 general-purpose, or working, registers. Two of these, registers A and B, hold results of many instructions, particularly math and logical operations, of the 89C51 central processing unit. The A register is the most versatile of the two CPU registers and is used for all data transfers between the 89C51 and any external memory. The B registers is used with A register for multiplication and division.

f) Flags and the Program Status Word (PSW)

The 89C51 has 4 math flags that respond automatically to the out comes of math operations and 3 general purpose flags that can be set to 1 or cleared to 0 by the programmer as desired. User flags are named F0, GF0, and GF1. The PSW contains the math flags, user program flag F0, and the register select bits that identify which of the 4 general-purpose register banks is currently in use by the program.

g) Internal RAM

The 128-byte internal RAM is organized into three distinct areas:

1. 32 Bytes from address 00H to 1FH that make up 32 working registers organized as 3 banks of 8 registers each.
2. A bit- addressable area of 16 bytes occupies RAM byte addresses 20H to 2FH, forming a total of 128 addressable bits.
3. A genera purpose RAM area above the bit area, from 30H to 7FH, addressable as bytes.

h) The Stack and the Stack Pointer

The stack refers an area of internal RAM that is used in conjunction with certain op-codes to store and retrieve data quickly. The 8 bit stack pointer (SP) register is used by the 89C51 to hold an internal RAM address that is called the top of the stack. The address held in the SP register is the location in internal RAM where the last byte of data was stored by a stack operation.

i) Special function Registers

The 89C51 operations that do not use the internal 128-byte RAM addresses from 00H to 7FH are done by these special function registers (SFR). Some SFRs are also bit addressable, as is the case for the bit area of RAM. This feature allows the programmer to change only what needs to be altered, leaving the remaining bits in the SFR unchanged.

j) Internal ROM

The internal ROM occupies code address space 0000H to 0FFFH. The PC is ordinarily used to address program code bytes from addresses 0000H to

0FFFH. The program addresses higher than 0FFFH, which exceed the internal ROM capacity, will cause the Microcontroller to automatically fetch code bytes from external program memory.

2.3 Power Factor Improvement Unit

a) Relay Unit

Specification

Type : Single Contact (Normally Open)

Operating Voltage : 12 V DC (Unregulated)

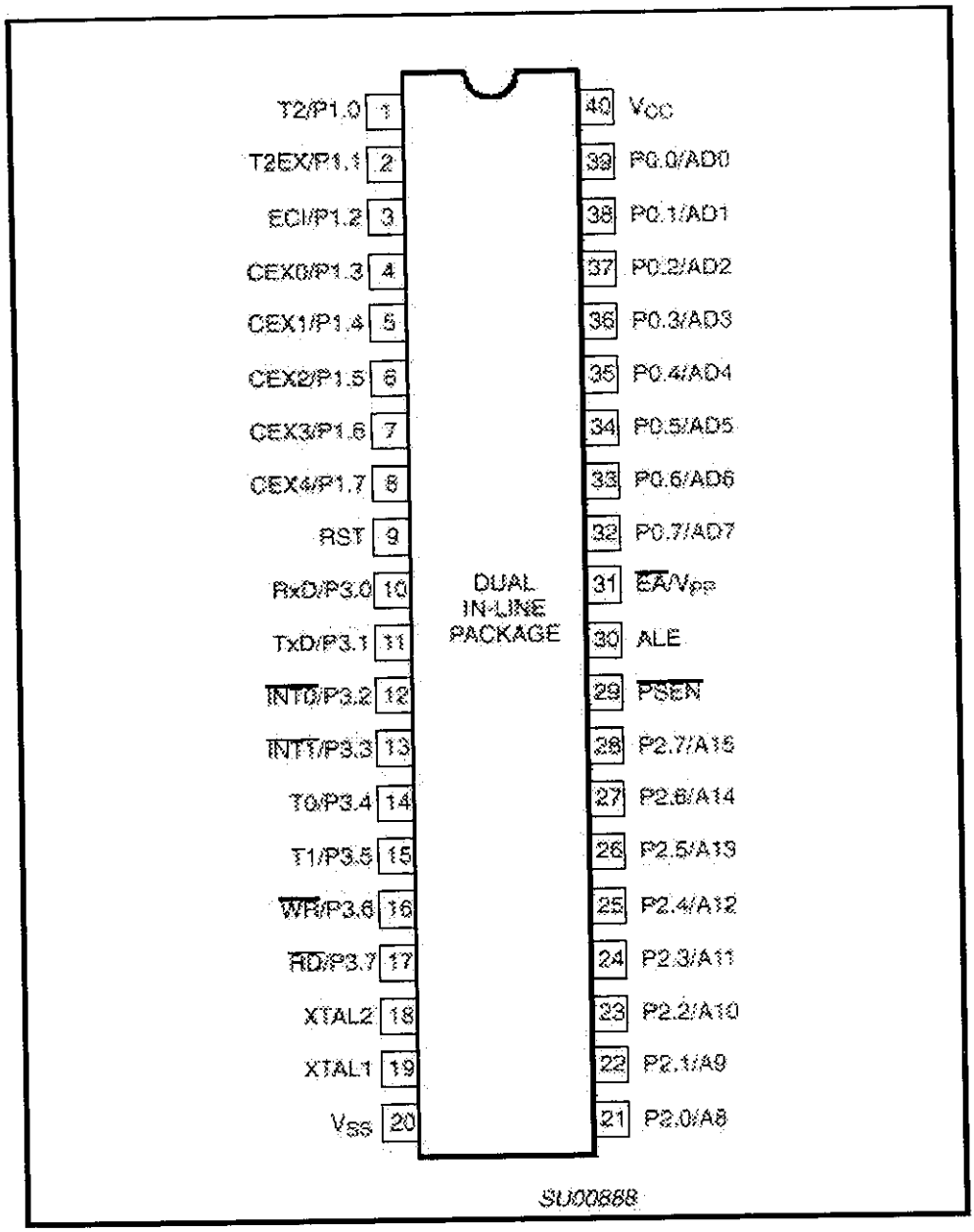
Current : 500 mA

The relay unit is actuated from the signals at the port. It is closed and the contact coil connects the capacitor bank. When it is open, the contactor coil disconnects the capacitor bank.

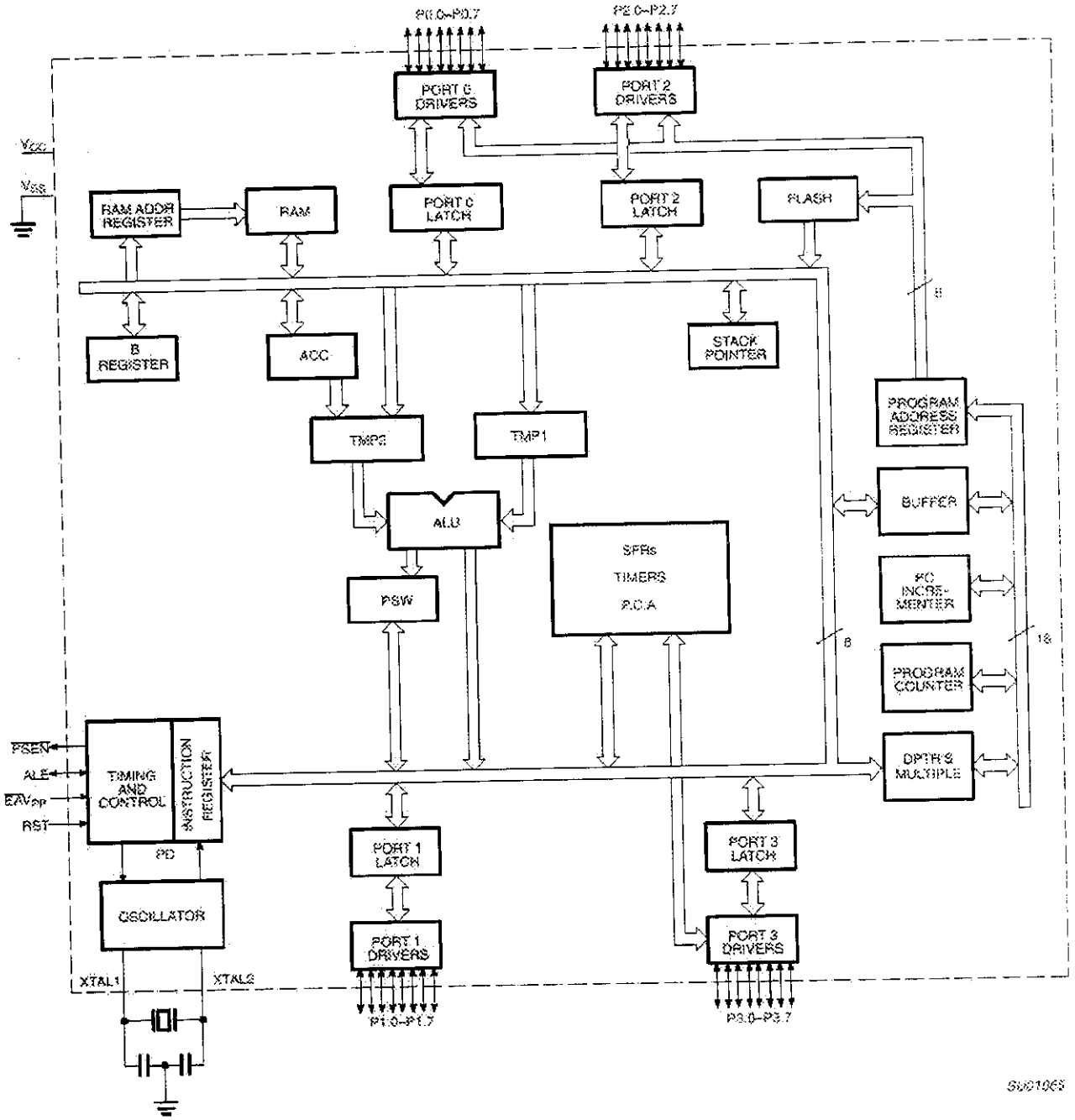
b) Capacitor Banks

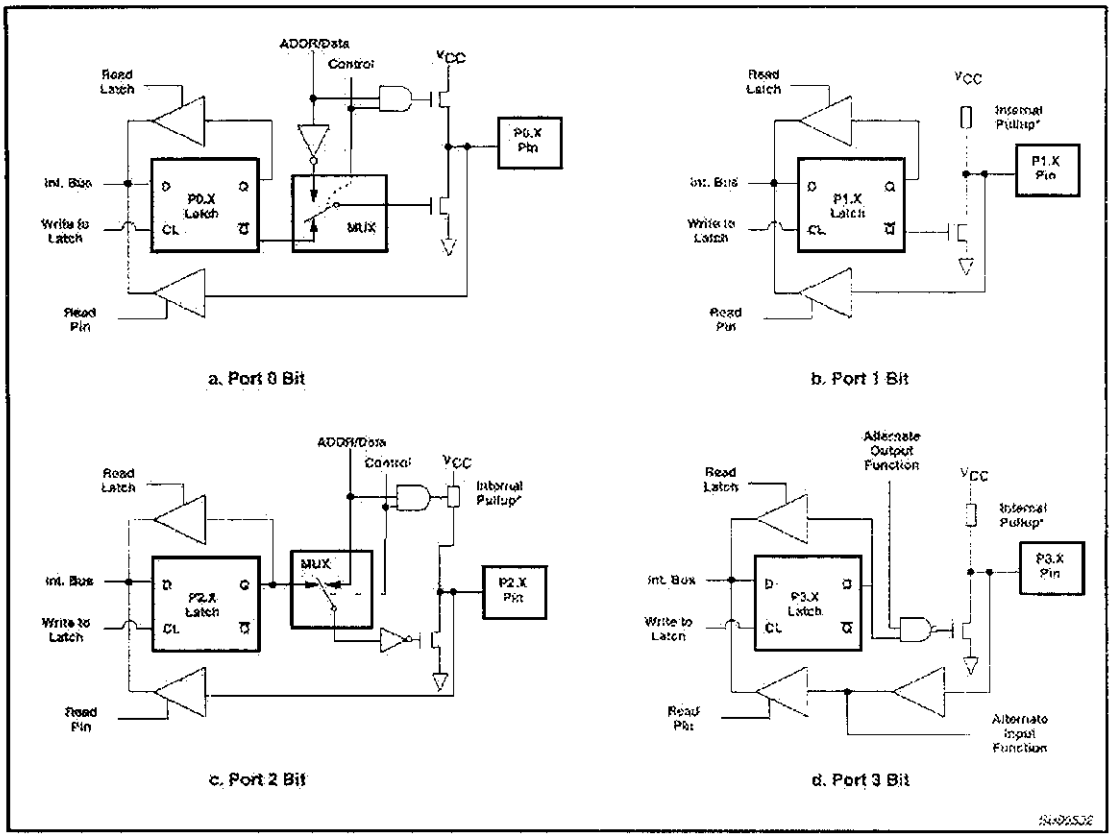
The capacitor banks are connected to the relay unit. When the relay unit operates, the connector coil includes the capacitor bank and when it disconnects, it allows a delay to make the capacitor discharge.

DUAL IN-LINE PACKAGE PIN FUNCTIONS



OCK DIAGRAM


P0.0–P0.7
P2.0–P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
VCC
VSS
RAM ADDR REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
8
TMP2
TMP1
PROGRAM ADDRESS REGISTER
ALU
BUFFER
SFRs
TIMERS
P.C.A
PSW
PC INCRE-MENTER
8
16
PROGRAM COUNTER
PSEN
ALE
EA/VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR'S MULTIPLE
PD
PORT 1 LATCH
PORT 3 LATCH
OSCILLATOR
PORT 1 DRIVERS
PORT 3 DRIVERS
XTAL1
XTAL2
P1.0–P1.7
P3.0–P3.7
SU01065



*See Figure 5 for details of the internal pullup.

Figure 4. 80C51 Port Bit Latches and I/O Buffers

SOFTWARE

CHAPTER III

SOFTWARE

```
; This is a Systronix generated Main file
;  Put your include statements in this file

                ;P1 POWER FACTOR DISPLAY
                ;P1.4 DISPLAY ENABLE
                ;P1.5
                ;P1.6
                ;
                ;

                ;P2.0 RELAY1
                ;P2.1 RELAY2
                ;P2.2 RELAY3
                ;P2.3 RELAY4
                ;P2.4 RELAY5
                ;P2.5 RELAY6

clear     equ 00h

                org 0000h
                mov p1,#clear
                mov p2,#clear
                mov p3,#clear


l1      mov p1,#00h
                mov r5,#00h
                mov p2,#00h
                mov r7,#00h
                ;setb p1.4
                ;setb p1.5
                ;setb p1.6
                mov dptr,#0000h
```

```
        mov r7,p3
    cjne r7,#01h,l1      ;voltage pulse

        anl tcon,#0cfh
        anl tmod,#0f0h
        orl tmod,#01h        ;initialise timer as counter
        mov tl0,#00h
        mov th0,#00h
        orl tcon,#10h        ;start timer



l2      mov r7,p3
    cjne r7,#02h,l2      ;voltage and current pulse

        anl tcon,#0efh       ;stop timer


        mov dpl,tl0
        mov dph ,th0

l

        mov 30h,dpl
        mov 31h,dph

        mov r0,#30h
        mov r1,#31h


        cjne @r1,#00h,n

n       cjne @r0,#00h,n0
    mov r5,#32h
    ljmp a10

n0      cjne @r1,#00h,n1
```

```
n1          cjne @r0,#0fah,n2
            mov r5,#32h
        ljmp a10

n2          cjne @r1,#01h,n3

n3          cjne @r0,#0f4h,n4
        mov r5,#32h
            ljmp a10

n4          cjne @r1,#02h,n5

n5          cjne @r0,#0eeh,n6
        mov r5,#32h
            ljmp a10

n6          cjne @r1,#03h,n7

n7          cjne @r0,#0e8h,n8
        mov r5,#32h
            ljmp a10

n8          cjne @r1,#04h,n9

n9          cjne @r0,#0e2h,n10
        mov r5,#32h
            ljmp a10

n10         cjne @r1,#05h,n11

n11         cjne @r0,#0dch,n12
        mov r5,#32h
            ljmp a10

n12         cjne @r1,#06h,n13

n13         cjne @r0,#0dch,n14
        mov r5,#32h
            ljmp a10
```

```
n14         cjne @r1,#07h,n15

n15         cjne @r0,#0d0h,n16
        mov r5,#32h
            ljmp a10

n16         cjne @r1,#08h,n17

n17         cjne @r0,#0cah,n18
        mov r5,#32h
            ljmp a10

n18         cjne @r1,#09h,n19

n19         cjne @r0,#0c4h,n20
        mov r5,#32h
            ljmp a10

n20         cjne @r1,#0ah,n21

n21         cjne @r0,#0beh,n22
        mov r5,#32h
            ljmp a9

n22         cjne @r1,#0bh,n23

n23         cjne @r0,#0b8h,n24
        mov r5,#32h
            ljmp a8

n24         cjne @r1,#0ch,n25

n25         cjne @r0,#0b2h,n26
        mov r5,#32h
            ljmp a7

n26         cjne @r1,#0dh,n27
```

```
n27         cjne @r0,#0ach,n28
        mov r5,#32h
            ljmp a6

n28         cjne @r1,#0eh,n29

n29         cjne @r0,#0a6h,n30
        mov r5,#32h
            ljmp a5

n30         cjne @r1,#0fh,n31

n31         cjne @r0,#0a0h,n32
        mov r5,#32h
            ljmp a4

n32         cjne @r1,#10h,n33

n33         cjne @r0,#9ah,n34
        mov r5,#32h
            ljmp a3

n34         cjne @r1,#11h,n35

n35         cjne @r0,#94h,n36
        mov r5,#32h
            ljmp a2

n36         cjne @r1,#12h,n37

n37         cjne @r0,#8eh,n38
        mov r5,#32h
            ljmp a1

n38         cjne @r1,#13h,n39

n39         cjne @r0,#88h,increment
        mov r5,#32h
            ljmp a1
```

```
increment inc dptr

        ljmp l



a0
                mov p2,#02h                     ;display0
                mov p2,#02h
                mov p2,#02h
                mov p2,#02h
                mov p2,#02h

                mov p1,#01h
                setb p1.4
                lcall delay

                mov p1,#06h
                setb p1.5
                lcall delay

                mov p1,#09h
                setb p1.6
                lcall delay

                mov p1,#00h
                setb p1.7
                lcall delay

                djnz r5,a0
                ljmp l1
```

```
a1      mov p2,#02h          ;display1
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h

        mov p1,#09h
        setb p1.4
        lcall delay

        mov p1,#07h
        setb p1.5
        lcall delay

        mov p1,#06h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay

        djnz r5,a1
        ljmp l1


a2      mov p2,#02h          ;display2
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p1,#09h
        setb p1.4
        lcall delay

        mov p1,#06h
        setb p1.5
```

```
        lcall delay

        mov p1,#07h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a2
        ljmp l1

a3      mov p2,#02h             ;display3
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h
        mov p2,#02h

        mov p1,#09h
        setb p1.4
        lcall delay

        mov p1,#06h
        setb p1.5
        lcall delay

        mov p1,#02h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a3
```

```
        ljmp l1

a4      mov p2,#06h         ;display4
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h

        mov p1,#09h
        setb p1.4
        lcall delay

        mov p1,#05h
        setb p1.5
        lcall delay

        mov p1,#01h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a4
        ljmp l1

a5      mov p2,#06h         ;display5
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h

        mov p1,#09h
```

```
        setb p1.4
        lcall delay

        mov p1,#02h
        setb p1.5
        lcall delay

        mov p1,#03h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a5
        ljmp l1

a6      mov p2,#06h             ;display6
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h
        mov p2,#06h

        mov p1,#08h
        setb p1.4
        lcall delay

        mov p1,#09h
        setb p1.5
        lcall delay

        mov p1,#01h
        setb p1.6
        lcall delay
```

```
        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a6
        ljmp l1

a7      mov p2,#0eh             ;display7
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh

        mov p1,#08h
        setb p1.4
        lcall delay

        mov p1,#05h
        setb p1.5
        lcall delay

        mov p1,#02h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a7
        ljmp l1

a8      mov p2,#0eh             ;display8
        mov p2,#0eh
        mov p2,#0eh
```

```
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh

        mov p1,#08h
        setb p1.4
        lcall delay

        mov p1,#00h
        setb p1.5
        lcall delay

        mov p1,#09h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a8
        ljmp l1

a9      mov p2,#0eh             ;display9
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh
        mov p2,#0eh

        mov p1,#07h
        setb p1.4
        lcall delay

        mov p1,#06h
```

```
        setb p1.5
        lcall delay

        mov p1,#00h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a9
        ljmp l1

a10     mov p2,#01h             ;display10
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h

        mov p1,#07h
        setb p1.4
        lcall delay

        mov p1,#00h
        setb p1.5
        lcall delay

        mov p1,#07h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay
```

```
        djnz r5,a10
        ljmp l1

a11     mov p2,#01h             ;display11
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h

        mov p1,#06h
        setb p1.4
        lcall delay

        mov p1,#04h
        setb p1.5
        lcall delay

        mov p1,#09h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a11
        ljmp l1

a12     mov p2,#01h             ;display12
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
        mov p2,#01h
```

```
        mov p2,#01h

        mov p1,#05h
        setb p1.4
        lcall delay

        mov p1,#08h
        setb p1.5
        lcall delay

        mov p1,#07h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a12
        ljmp l1

a13     mov p2,#03h             ;display13
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h

        mov p1,#05h
        setb p1.4
        lcall delay

        mov p1,#02h
        setb p1.5
        lcall delay

        mov p1,#02h
```

```
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a13
        ljmp l1

a14     mov p2,#03h             ;display14
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h

        mov p1,#04h
        setb p1.4
        lcall delay

        mov p1,#05h
        setb p1.5
        lcall delay

        mov p1,#03h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a14
        ljmp l1
```

```
a15     mov p2,#03h         ;display15
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h
        mov p2,#03h

        mov p1,#03h
        setb p1.4
        lcall delay

        mov p1,#08h
        setb p1.5
        lcall delay

        mov p1,#02h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a15
        ljmp l1

a16     mov p2,#07h         ;display16
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h

        mov p1,#03h
```

```
        setb p1.4
        lcall delay

        mov p1,#00h
        setb p1.5
        lcall delay

        mov p1,#09h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a16
        ljmp l1

a17     mov p2,#07h             ;display17
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h

        mov p1,#02h
        setb p1.4
        lcall delay

        mov p1,#03h
        setb p1.5
        lcall delay

        mov p1,#03h
        setb p1.6
        lcall delay
```

```
        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a17
        ljmp l1

a18     mov p2,#07h             ;display18
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h

        mov p1,#01h
        setb p1.4
        lcall delay

        mov p1,#05h
        setb p1.5
        lcall delay

        mov p1,#06h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a18
        ljmp l1

a19     mov p2,#07h             ;display19
        mov p2,#07h
```

```
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h
        mov p2,#07h

        mov p1,#00h
        setb p1.4
        lcall delay

        mov p1,#07h
        setb p1.5
        lcall delay

        mov p1,#08h
        setb p1.6
        lcall delay

        mov p1,#00h
        setb p1.7
        lcall delay


        djnz r5,a19
        ljmp l1

;a20    mov p2,#07h          ;display20

        mov p1,#00h
        setb p1.4
        lcall delay

        mov p1,#00h
        setb p1.5
        lcall delay

        mov p1,#00h
        setb p1.6
```

```
            lcall delay

            mov p1,#00h
            setb p1.7
            lcall delay


            ;djnz r5,a20
            ljmp l1



delay   mov r3,#15h         ;08
in          mov r4,#00h     ;00
wait        djnz r4,wait
            djnz r3,in
            ret
```

TEST RESULTS

CHAPTER IV

TABULATION

Voltage	Without Capacitor				With Capacitor			
	Current	P.F.	Volt ampere	Power	Current	P.F.	Volt ampere	Power
Volts	amps	-	VA	Watts	amps	-	VA	watts
219	0.13	0.707	28.47	20.12829	0.095	0.967	20.805	20.118435
219	0.21	0.733	45.99	33.71065	0.16	0.953	35.04	33.39312
219	0.26	0.765	56.94	43.5591	0.204	0.971	44.626	43.380396
219	0.33	0.792	72.27	57.2378	0.275	0.947	50.225	57.033075
219	0.41	0.808	89.79	72.55032	0.346	0.957	75.774	72.515718
219	0.52	0.853	113.88	97.13964	0.461	0.961	100.95	97.021599

COMPARISON TABLE

Energy Consumed without Capacitor	Energy Consumed with Capacitor	Percentage Saving in Energy
28.47	20.805	26.92 %
45.99	35.04	23.86 %
56.94	44.67	21.50 %
72.27	50.225	16.67 %
89.79	75.774	15.61 %
113.88	100.95	11.34 %

MODEL CALCULATION

Without Capacitor

Operating Voltage = 219 volts

Operating Current = 0.13 amps

Operating Power factor = 0.707

Operating VA = 219*0.13 = 28.47 VA

Operating Power = 219*0.13*0.707 = 20.12829 watts

With Capacitor

Operating Voltage = 219 volts

Operating Current = 0.095 amps

Operating Power factor = 0.967

Operating VA = 219*0.095 = 20.805 VA

Operating Power = 219*0.095*0.967 = 20.118435 watts

Percentage volt amps saved = [(28.47-20.805)/28.47]*100 = 26.92 %

CHAPTER V

CONCLUSION

The Microcontroller based Energy Saver has been designed, fabricated and tested on monoblock pump and its operation is found to be satisfactory. In practice, the L.T. consumers use manual switching and may lead to loss in energy. With the adaptation of microcontroller to control the power factor, the new generation of controllers is developed with high performance and capability to save a considerable amount of energy.

The Power factor without the capacitor bank was found to be 0.707 and after the inclusion of capacitors, we obtained an improved Power factor of 0.967.

As a result, a net energy saving of 27 % is obtained.

The advantages of this controller over manual switching system is that,

1. Automatic switching using complex logical decision.
2. Time delay for the disconnecting of capacitor banks is inbuilt.
3. Errors in human readings can be avoided.

FURTHER DEVELOPMENTS

Further developments can be made on this product,

1. Necessary changes can be made in the program to display the number of capacitor banks connected.
2. The ratio of capacitor banks to be made 1:2:4 or 1:2:2 can also be developed.
3. Over voltage and under voltage indication.
4. By replacing the single phase relays and capacitors with three phase relays and capacitors, our product can be implemented for three phase higher rating motors.

REFERENCES

CONCLUSION

REFERENCES

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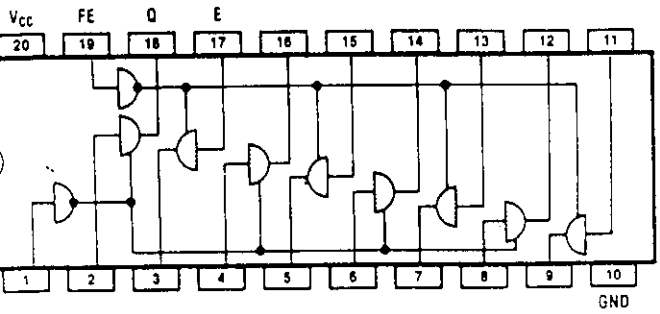
APPENDIX

44
TS

8-Bit Bustreiber
8-bit bus driver
Transceiver à 8 bits
Eccitatore di 8 bit
Excitador de bus de 8 bits



E	Q
	Z
	L
	H

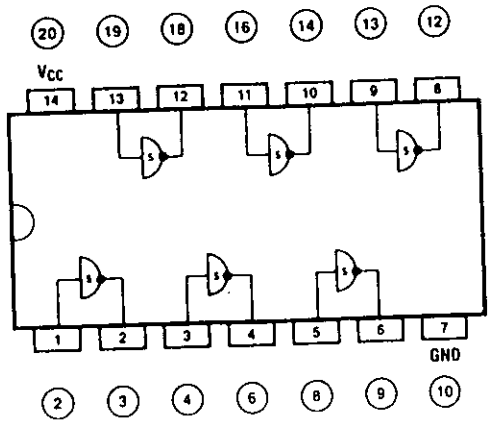
74244	Typ - Type - Tipo		Hersteller Production Fabricants Produttori Fabricantes	Bild Sec. 3 Pins-Art-Nr.	5 $\&I_R$ mA
0...70°C §0...75°C	-40...85°C §-25...85°C	-55...125°C			
		54AC244D	Fch,Nsc	20-dil-4	&(8μ
	74AC244D		Fch,Nsc	20-dil-4	&(8μ
		54AC244F	Fch,Nsc	20-flat-2	&(8μ
		54AC244L	Fch,Nsc	20-chip-2	&(8μ
	74AC244P		Fch,Nsc	20-dil-1	&(8μ
	74AC244S		Fch,Nsc	20-smd-2	&(8μ
ACT		CD54ACT244E	Rca	20-dil-1	&(8μ
	CD74ACT244E		Rca	20-dil-1	&(8μ
		CD54ACT244H	Rca	chip	&(8μ
		CD54ACT244M	Rca	20-smd-2	&(8μ
	CD74ACT244M		Rca	20-smd-2	&(8μ
	HD74AC244		Hit	20-dil	&(8μ
		54ACT244D	Fch,Nsc	20-dil-4	&(8μ
	74ACT244D		Fch,Nsc	20-dil-4	&(8μ
		54ACT244F	Fch,Nsc	20-flat-2	&(8μ
		54ACT244L	Fch,Nsc	20-chip-2	&(8μ
	74ACT244P		Fch,Nsc	20-dil-1	&(8μ
	74ACT244S		Fch,Nsc	20-smd-2	&(8μ
C		MM54C244D	Nsc	20-dil-4	5(2
	MM74C244J	MM54C244J	Nsc	20-dil-4	5(2
	MM74C244N		Nsc	20-dil-1	5(2
HC					
	CD74HC244E		Rca	20-dil-1	&(8μ
		CD54HC244F	Rca	20-dil-4	&(8μ
		CD54HC244H	Rca	chip	&(8μ
	CD74HC244M		Rca	20-smd-2	&(8μ
HD74HC244			Hit	20-dil	&(8μ
LC74HC244			Sa.	20-dil	&(8μ
M74HC244			Mit	20-dil	&(8μ
MB74HC244			Fuj	20-dil	&(8μ
		MC54HC244J	Mot	20-dil-4	&(8μ
		MC74HC244N	Mot	20-dil-1	&(8μ
		MC54HC244AJ	Mot	20-dil-4	&(8μ
		MC74HC244AN	Mot	20-dil-1	&(8μ
	MM74HC244J	MM54HC244J	Nsc	20-dil-4	&(8μ
	MM74HC244N		Nsc	20-dil-1	&(8μ
	MN74HC244		Mit	20-dil-1	&(8μ
	MN74HC244S		Mit	20-smd-2	&(8μ
	PC74HC244P		Philips	20-dil-1	&(8μ
	PC74HC244T		Philips	20-smd-2	&(8μ
SN74HC244DW			Tex	20-smd-2	&(8μ
		SN54HC244FH	Tex	20-chip-2	&(8μ
	SN74HC244FH		Tex	20-chip-2	&(8μ

4	Typ - Type - Tipo		Hersteller Production Fabricants Produttori Fabricantes	Bild Sec. 3 Pins-Art-Nr.	I_S $\&I_R$ mA	t_{PD} E-Q ns_{typ}	t_{PD} E-Q ns_{max}	Bemerk. Note f_T $\S f_Z$ $\&I_E$ MHz
C	-40...85°C	-55...125°C						
C	§-25...85°C							
		CD54AC244E	Rca	20-dil-1	&(8μ		8.2 8.2	
	CD74AC244E		Rca	20-dil-1	&(8μ		7.5 7.5	
		CD54AC244H	Rca	chip	&(8μ		8.2 8.2	
		CD54AC244M	Rca	20-smd-2	&(8μ		8.2 8.2	
	CD74AC244M		Rca	20-smd-2	&(8μ		7.5 7.5	
	HD74AC244		Hit	20-dil	&(8μ		9.5 10.5	

7414

Output: TP

Montages trigger de Schmitt inverseurs
Sganciatori invertenti Schmitt
Disparadores de Schmitt inversores



Logiktabelle siehe Section 1
Function table see section 1
Tableau logique voir section 1
Per tavola di logica vedi sez. 1
Tabla de verdad, ver sección 1

7414	Typ · Type · Tipo		Hersteller Production Fabricants Produttori Fabricantes	Bild Sec. 3 Pins- Art-Nr.	I_S &I_R	t_{PD} E ·Q ns_{typ}		t_{PD} E ·Q ns_{max}		Bemerk. Note I_T f_Z &f_E
0...70°C §0...75°C	–40...85°C §–25...85°C	–55...125°C			mA	↓	↑	↓	↑	MHz
AC										
	CD74AC14E	CD54AC14E	Rca	14-dil-1	&(4µ			10.5	10.5	
			Rca	14-dil-1	&(4µ			9.5	9.5	
		CD54AC14H	Rca	chip	&(4µ			10.5	10.5	
		CD54AC14M	Rca	14-smd-1	&(4µ			10.5	10.5	
	CD74AC14M		Rca	14-smd-1	&(4µ			9.5	9.5	
	HD74AC14		Hit	14-dil	&(4µ			9.5	11	
		54AC14D	Fch,Nsc	14-dil-4	&(4µ	6	7	10	12	
	74AC14D		Fch,Nsc	14-dil-4	&(4µ	6	7	9.5	11	
		54AC14F	Fch,Nsc	14-flat-1	&(4µ	6	7	10	12	
		54AC14L	Fch,Nsc	20-chip-2	&(4µ	6	7	10	12	
	74AC14P		Fch,Nsc	14-dil-1	&(4µ	6	7	9.5	11	
	74AC14S		Fch,Nsc	14-smd-1	&(4µ	6	7	9.5	11	
ACT										
	CD74ACT14E	CD54ACT14E	Rca	14-dil-1	&(4µ			9.5	14.5	
			Rca	14-dil-1	&(4µ			8.6	13.2	

7414	Typ · Type · Tipo		Hersteller Production Fabricants Produttori Fabricantes	Bild Sec. 3 Pins- Art-Nr.	I_S &I_R	t_{PD} E ·Q ns_{typ}		t_{PD} E ·Q ns_{max}		Bemerk. Note I_T f_Z &f_E
0...70°C §0...75°C	–40...85°C §–25...85°C	–55...125°C			mA	↓	↑	↓	↑	MHz
C										
	MM74C14J	MM54C14J	Nsc	14-dil-4	50n	220	220	400	400	
	MM74C14N		Nsc	14-dil-1	50n	220	220	400	400	
		MM54C14W	Nsc	14-flat-1	50n	220	220	400	400	
HC										
	CD74HC14E		Rca	14-dil-1		12	12			
		CD54HC14F	Rca	14-dil-4		12	12			
		CD54HC14H	Rca	chip		12	12			
	CD74HC14M		Rca	14-smd-1		12	12			
	HD74HC14		Hit	14-dil	&(2µ			31	31	
	M74HC14		Mit	14-dil	&(2µ			31	31	
		MC54HC14J	Mot	14-dil-4	&(2µ	11	11	21	21	
		MC74HC14N	Mot	14-dil-1	&(2µ	11	11	21	21	
		MC74HC14AD	Mot	14-smd-1	&1µ			29	29	
		MC54HC14AJ	Mot	14-dil-4	&1µ			29	29	
		MC74HC14AN	Mot	14-dil-1	&1µ			29	29	
	MM74HC14J	MM54HC14J	Nsc	14-dil-4	&(2µ	11	11	21	21	
	MM74HC14N		Nsc	14-dil-1	&(2µ	11	11	21	21	
	MN74HC14		Mat	14-dil-1	&(2µ			31	31	
	MN74HC14S		Mat	14-smd-1	&(2µ			31	31	
			Oki	14-dil	&(2µ			31	31	
MSM74HC14			Phi,Val	14-dil-1	&(2µ	15	15	31	31	
	PC74HC14P		Phi,Val	14-smd-1	&(2µ	15	15	31	31	
	PC74HC14T		Tix	14-smd-1	&(2µ	12	12	31	31	
SN74HC14D			Tix	20-chip-3	&(2µ	12	12	31	31	
		SN54HC14FH	Tix	20-chip-3	&(2µ	12	12	38	38	
	SN74HC14FH		Tix	20-chip-2	&(2µ	12	12	31	31	
		SN54HC14FK	Tix	20-chip-2	&(2µ	12	12	38	38	
	SN74HC14FN		Tix	20-chip-1	&(2µ	12	12	31	31	
		SN54HC14J	Tix	14-dil-4	&(2µ	12	12	38	38	
	SN74HC14J		Tix	14-dil-4	&(2µ	12	12	31	31	
	SN74HC14N		Tix	14-dil-1	&(2µ	12	12	31	31	
T74HC14			Sgs	14-dil	&(2µ			31	31	
TD74HC14			Tos	14-dil	&(2µ			31	31	
µPB74HC14			Nec	14-dil	&(2µ			31	31	
HCT										
	CD74HCT14E		Rca	14-dil-1		12	12			
		CD54HCT14F	Rca	14-dil-4		12	12			
		CD54HCT14H	Rca	chip		12	12			
	CD74HCT14M		Rca	14-smd-1		12	12			
	PC74HCT14P		Phi,Val	14-dil-1	&(2µ	20	20	43	43	
	PC74HCT14T		Phi,Val	14-smd-1	&(2µ	20	20	43	43	