ECONOMIC VERSION OF OVERHEAD CLEANER CONTROLLER

PROJECT REPORT

SUBMITTED BY

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DEPARTMENT OF MECHATRONICS ENGINEERING

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DEPARTMENT OF MECHATRONICS ENGINEERING

CERTIFICATE

This is to certify that this project entitled

ECONOMIC VERSION OF OVERHEAD CLEANER CONTROLLER

has been submitted by

Ms/Mr. ....

In partial fulfillment of the requirements for the award of the degree of

Bachelor of Engineering in Mechatronics Engineering

Branch of Bharathiar University, Coimbatore – 641 046 during the

Academic year 2002-2003

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(Guide)

....
(Head of the Department)

Certified that the candidate was examined by us in the project work.

Viva-Voce examination held on ....

University Register Number

....

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(Internal Examiner)

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12/03/2003

PROJECT COMPLETION CERTIFICATE

is to certify that Ms P.Bharathi, Mr.N.Kathiresh Kumar, Mr.P.G.Magendran
Mr.V.Rajesh of IV B.E. Mechatronics Engineering, Kumaraguru College Of
nology has successfully completed the project titled **"Economic Version**
Overhead Cleaner Controller" as part of their curriculum from 29th
2002 to 20th February 2003.

conduct was good and performance was upto our satisfaction during their
ure.We wish them all the best for a prosperous future.

M.ESWARASAMY
Sr.MANAGER-WORKS

OTE:

Due to technical reasons and contract regulations we are not in a
sition to offer the software in executable form or the coding.

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

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Finally we also thank all the staff members and non teaching staff members who have readily rendered their helping hand towards the project .

SYNOPSIS

SYNOPSIS

The main objective of this project is to design and implement a microcontroller based **'Economic Version Of Overhead Cleaner Controller'**.

Overhead travelling cleaners are widely used in textile spinning & weaving units to collect the waste cotton called as fluff, which not removed properly may affect the quality of thread weaved & also creates an unpleasant environment for the workers .

In the current scenario , overhead cleaners are provided with an electronic control to ensure high reliability and better rated performance when compared to the traditional cleaning systems , but the disadvantage being the cost involved which may not be affordable for small - scale units .

With rapid development in the field of electronics , this economic version of overhead cleaner controller opts in making a compromise on price with acceptable performance . The overhead cleaner controller uses a 20 pin **AT892051** microcontroller to control the operation of the overhead cleaner.

The flash memory microcontroller performs its task efficiently remaining flexible and cost effective . This equipment is versatile and compatible with industrial (real time) requirements and hence to be sought by textile mills . This modified version of overhead cleaner controller is believed to reduce the cost involved in maintaining a dust free environment in textile units.

We are very sure that the execution of this project with so much cost savings to the clients will fetch not only good name to the company but also number of orders and thereby the company can establish a good market in providing cleaning solutions to textile mills .

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INTRODUCTION

CHAPTER 1

INTRODUCTION

In textile industries where cotton is made into thread, unwanted cotton dust called fluff is formed . The so formed fluff disperses out in the surroundings and creates an uncomfortable environment for the people working there . This affects the employee's health, company's productivity and also reduces the performance of the machine . So , some preventive measures become indispensable .

Hence cleaning being an integral part of every textile mill , an over head cleaner offers state – of – the – art solution to cleaning . It is an equipment that moves parallely above the spinning machine on a track , absorbing the cotton dust in the premises .

The over head cleaner can be driven by a microcontroller or a microprocessor . This project uses AT892051 microcontroller as the basic controlling element to enhance the working of the over head cleaner , with a simple programming logic .

The overview of the over head cleaner controller and the detailed functional description of the type of control employed , are dealt with in the forth coming chapters .

FUNCTIONAL DESCRIPTION

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1 OVER HEAD CLEANER:

The overhead cleaner is divided into two basic units according to their functions . They are :

- Mobile unit
- Sucking unit

2.1.1 MOBILE UNIT:

This unit is responsible for the circular or translatory motion of the cleaner . It is controlled by a driver motor .

2.1.2 SUCKING UNIT:

This is similar to a vacuum cleaner . It absorbs and accumulates cotton dust to discharge later . The collected cotton can be reused . This unit is controlled by a fan motor.

As there is a need for overhead cleaner , the automation of its working proves to be useful . The over head cleaner is controlled by an electronic logic board called the '*Over head cleaner controller*' .

2.2 OVER HEAD CLEANER CONTROLLER :

The over head cleaner controller has the following functions :

- It drives the cleaner and reverses it at the ends. The controller senses the 'START' signal and operates the over head cleaner. As soon as the OHC reaches the ends of the trail, the controller reverses the direction of motion of the OHC.

- The ends of track are sensed by using sensors.

- In case of endless loop system, the OHCC can stop OHC for discharging, in the middle.

- Sensors are used to recognize the obstacles and OHCC reverses the direction of OHC if any obstacle is detected .

SYSTEM DESCRIPTION

CHAPTER 3

SYSTEM DESCRIPTION

3.1 BASIC BLOCK DIAGRAM OF OHCC :

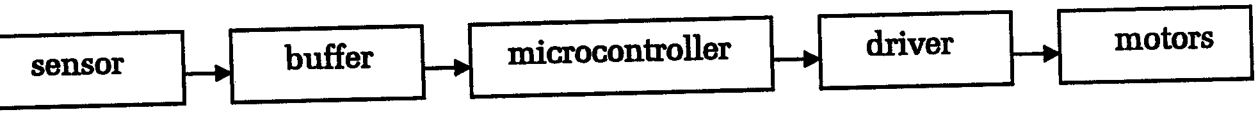


Fig : 3.1

The system working is better understood by having a detailed study of individual components.

3.2 DESCRIPTION :

The OHCC consists of the following blocks:

1. Input signals
2. Buffer
3. Microcontroller
4. Driver
5. Contactor

3.2.1. INPUT SIGNALS :

The OHCC controls the over head cleaner according to the input signals . There are totally five input signals viz .,

- Start
- Stop
- Auto Reverse
- Discharge
- Obstacle 1 & 2

- **START :**

This signal literally starts the OHC. The OHCC energizes the sucking unit first and then the mobile unit later (i.e.) after a small delay.

- **STOP :**

This signal brings the OHC to an *off* condition. As soon as this signal is received, the OHCC disables the sucking unit and mobile unit .

- **AUTO REVERSE :**

When the OHCC receives this signal it allows OHC to stop and wait for a time called ' *reversing delay* '. After this delay the OHC starts to travel in an opposite direction. The sucking unit stays *on* for this delay period.

- **DISCHARGE :**

When the OHCC receives this signal it stops OHC for a pre set time called '*discharge delay*'. After this delay the OHC continues to travel in the same direction.

The sucking unit is disabled during this time and the OHC discharges the collected cotton dust .

- **OBSTACLE 1 :**

This signal indicates the presence of an obstacle in the forward path of the cleaner. This signal is sensed by OHCC and it changes the direction of motion of the OHC .

- **OBSTACLE 2 :**

This signal indicates the presence of an obstacle in the reverse path of the OHC . The OHCC senses this signal and reverses the direction of OHC .

Out of these signals the start and stop signals are generated manually using push button switches , the reverse and discharge signals are generated by proximity sensors and the obstacle signals are given by optical sensors .

These five signals define the basic working of cleaner . Apart from these , a number of other input signals can also be included to make the cleaner perform additional functions .

BLOCK DIAGRAM

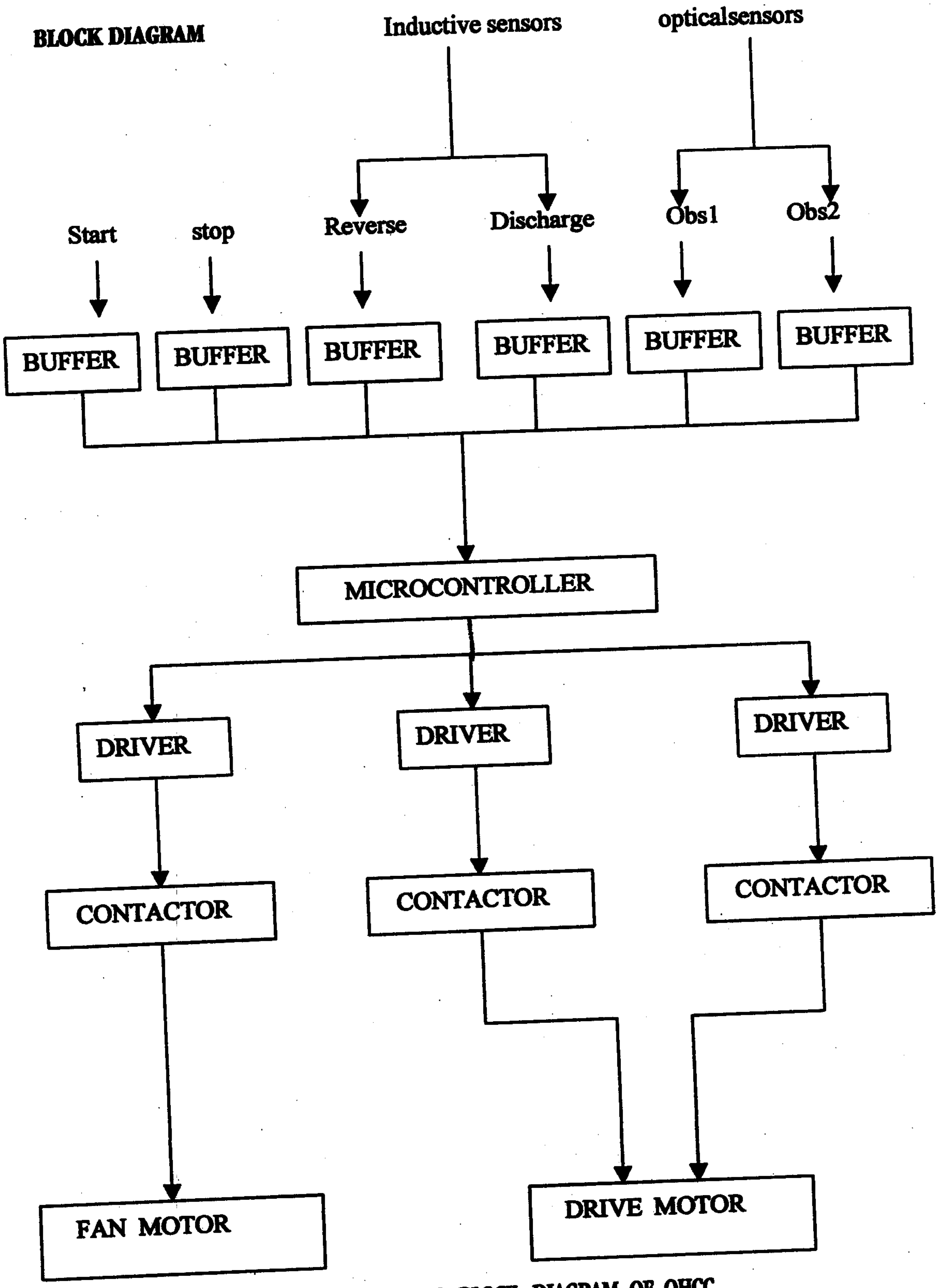


FIG 3.2 DETAILED BLOCK DIAGRAM OF OHCC

3.2.2. BUFFER :

The buffer can be called as a '*matching unit*'. In OHCC the buffer acts as a step down transformer. It couples the sensor outputs with the input of the microcontroller.

As opto coupler acts as a buffer in this case. It couples the sensors working with 24V supply voltage to the microcontroller working with 5V supply.

Each sensor needs a buffer unit to get connected to the microcontroller.

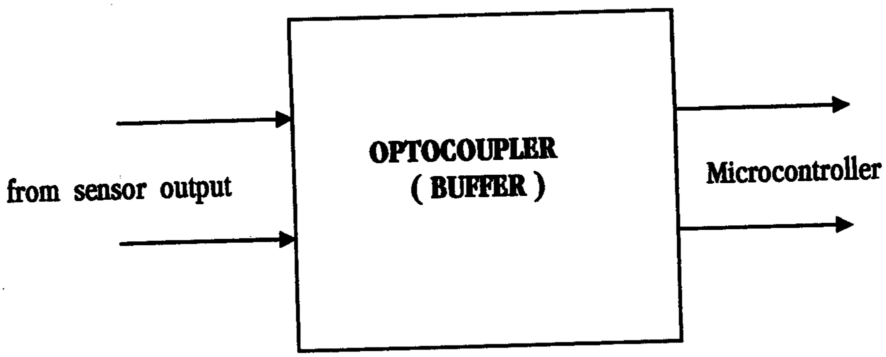


FIG 3.3 BLOCK OF OPTOCOUPLER

3.2.3. MICROCONTROLLER :

The microcontroller controls the entire working of the OHC depending on the signals received. The tasks corresponding to the input signals are stored as programs in the microcontroller. As soon as the OHCC is switched *on* the microcontroller runs the corresponding subroutine of the input signals that gets high. Thus it controls the movement of the cleaner using motors. This mechanism goes on until OHC is switched *off.*

3.2.4. DRIVER :

As the microcontroller cannot drive the motors directly, a drive stage is necessary in between them. The driver can be a transistor, operated as a switch for DC contactors. It couples the microcontroller to the contactor working at 24V supply, (i.e.) it drives the contactors. This project uses a TRIAC as a driver to drive the AC contactors.

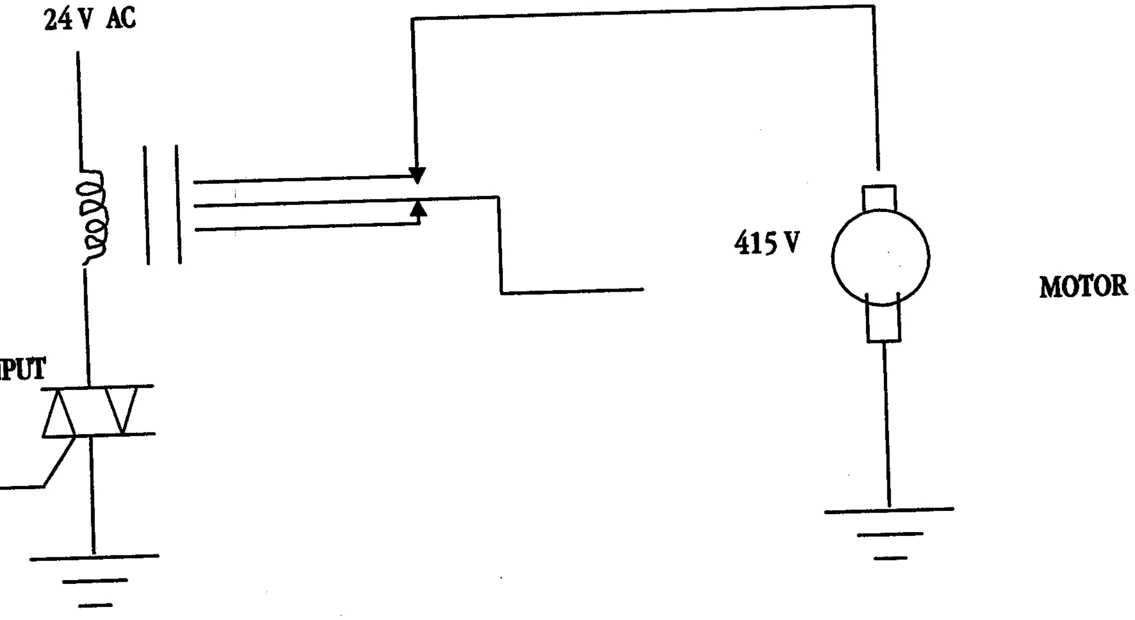
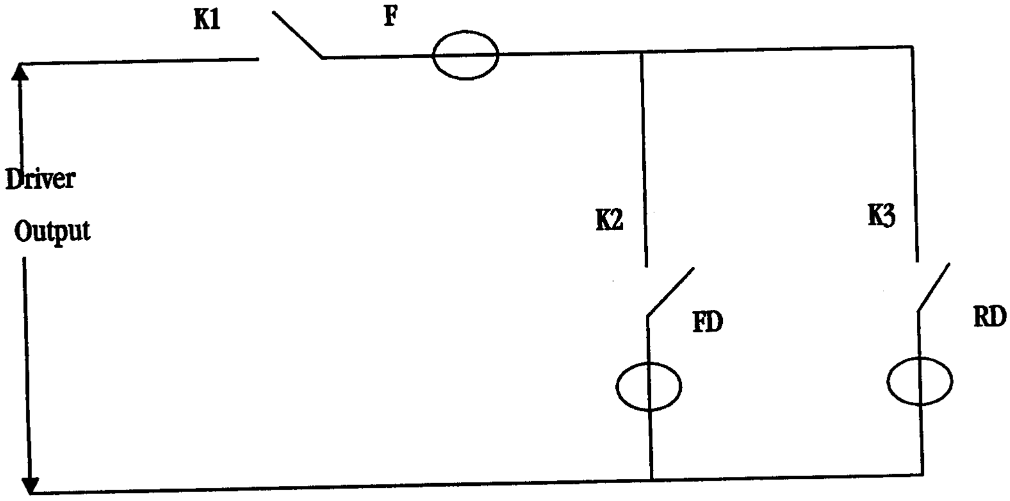


FIG : 3.4 CONTACTOR – DRIVER CONNECTION

5. CONTACTOR :

The contactor runs the fan and drive motors as required. It is actually a relay working at higher voltages. As the contactor is energized, the corresponding motor will run. Depending on which contactor is energized the OHC will move in forward or reverse direction .



K1 – Fan controller

K2 - Forward contactor

K3 - Reverse contractor

F – Fan motor

FD – Forward drive motor

RD – Reverse drive motor

Fig 3.5 Equivalent Circuit for Contactors & Motors switching

SYSTEM LAYOUT:

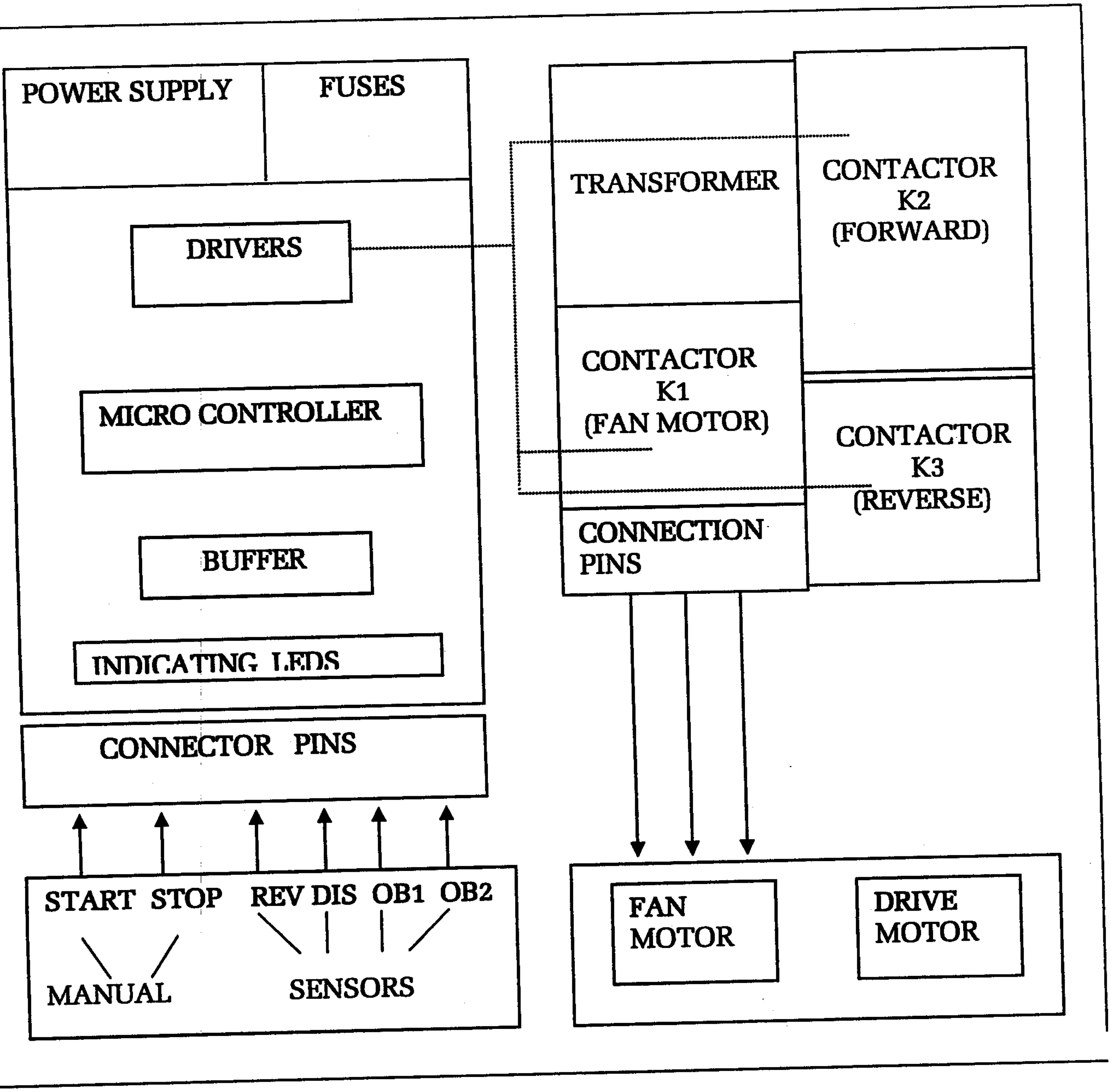


Fig 3.6 Layout of OHCC

The system layout gives an overall idea of the cleaner controller. The LEDS indicate the corresponding input signal from the sensor. The fan & drive motor are controlled by their respective contactors.

HARDWARE DESCRIPTION

CHAPTER 4

HARDWARE DESCRIPTION

The prime use of microcontroller is to control the operation of a machine using a fixed program that is stored in ROM .

The 8051 microcontroller generic part number actually includes a whole family of microcontrollers that have numbers ranging from 8031 to 8751 and are available in an n-channel Metal Oxide Silicon (NMOS) and Complementary Metal Oxide Silicon (CMOS) construction in a variety of package types . As enhanced version of the 8051 , the 8052 also exists with its own family of variations and even includes one member that can be programmed in BASIC .

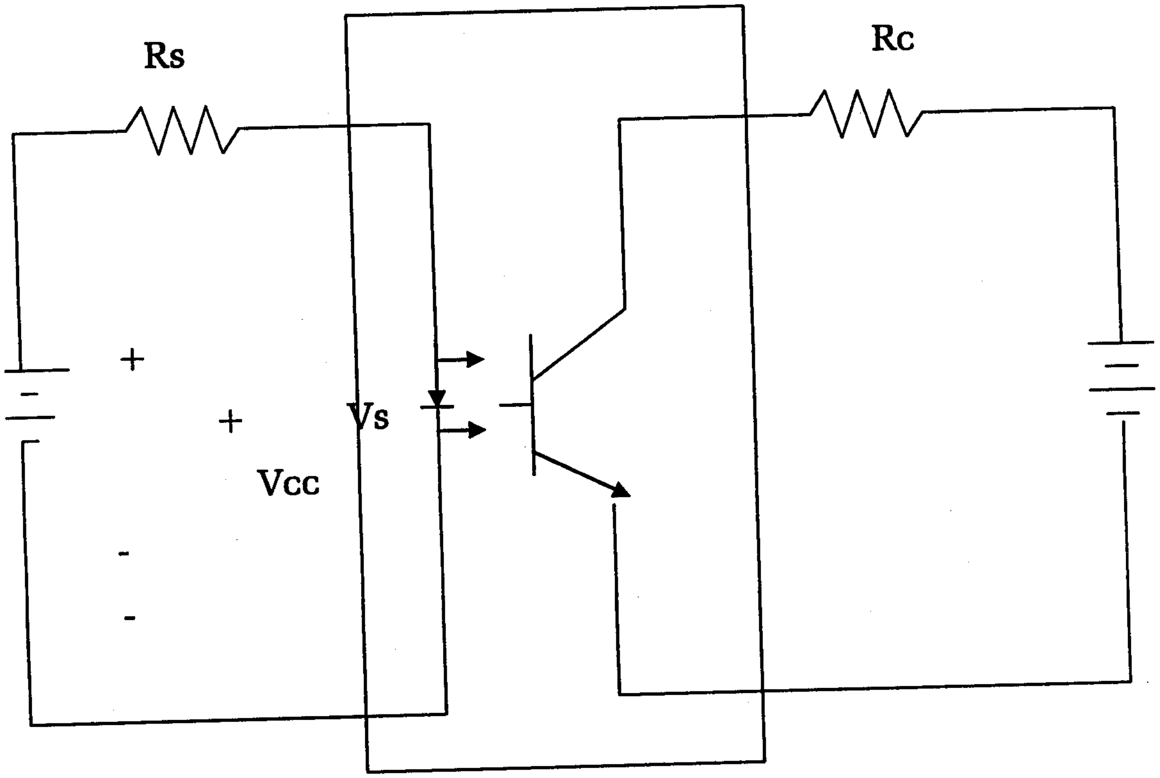
Some members of 8051 family are given below .

				RAM
8031	-	EPROM less	-	128bytes
8032	-	EPROM less	-	256 bytes
87C51	-	with EPROM (4K) (window type)	-	128 bytes
87C52	-	with EPROM (8K)	-	256bytes
87C51	-	with EPROM (4K) (flash memory)	-	128 bytes
89C52	-	with EPROM (8K) (flash memory)	-	256 bytes

A member of the 8051 family AT89C2051 , an 8 – bit microcontroller with 2Kilobytes flash memory has been selected for this project .

4.1 OPTOCOUPLER:

An opto coupler (also called as opto isolator or an optically coupled isolator) combines an LED and a photo transistor in a single package. This opto coupler is used as buffer for coupling the sensor outputs with microcontroller inputs.



This shows an LED driving a photo transistor. This is much more sensitive optocoupler than LED – photodiode. Any change in LED current, changes the current through the photo transistor. In turn, the change in the LED current produces a changing voltage across the Collector – Emitter terminals. Therefore, a signal voltage is coupled from the input circuit to the output circuit. The big advantage of an optocoupler is the electrical isolation, between the input and output circuits. With an optocoupler the only contact between the input and output is a beam of light. Because of this, it is possible to have an insulation resistance between the two circuits in the thousands of megaohms. Isolation like this comes handy in high voltage applications, where the potentials of the two circuits may differ by several thousand voltages.

In this project, the buffer action is carried over by the optocoupler 4N35 .

4.2 TRIAC:

A triac is a device equivalent to an inverse parallel connectd pair of SCRs, during turn – off, its behaviour is not so clear as SCR. The triac is a member of thyristor family .

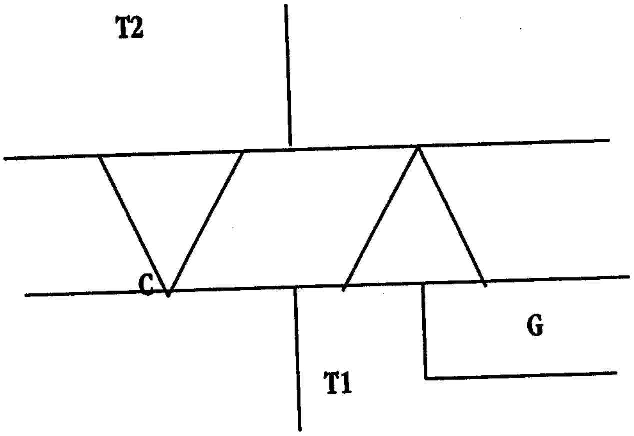


Fig 4.2 Triac

Triac has three terminals , G is the control terminal . The main terminal connected electrically to the envelope is called ' *anode* ' by some manufacturers due to its resemblance with the anode lead of a reverse blocking triode thyristor .

The difference between the operation of a triac and reserve blocking triode thyristor is that triac can conduct when the terminal 2 is positive or negative with respect to T2 . This conduction in either direction can be achieved with either gate positive or negative with respect to the main terminal (ie) T1 .

4.2.1. ADVANTAGES OF TRIAC :

- The triac needs a single heat sink of slightly larger size , but antiparallel thyristor pair needs two heat sinks of slightly smaller sizes but due to the clearance total space required is more for thyristors .
- A triac needs a single fuse for protection , this also simplifies the construction . Triacs can be triggered with positive or negative polarity voltages .
- In some DC applications SCR is required to be fitted with a parallel diode to protect against reverse voltage . A triac used may work without a diode as such breakdown in either direction is possible .
- The triac is preferred due to its low cost and advantages .

The triac BT136 is used in this project, overhead cleaner controller .

4.3. MOTORS :

Two types of motors used are ,

- Fan motor , which is an induction motor .
- Drive motor , which is a stepper motor .

4.3.1. FAN MOTOR :

The fan motor operates a fan for the sucking action . It gets started as soon as the START signal is given .

4.3.2. DRIVE MOTOR :

The drive motor is responsible for the working of mobile unit . This motor can be used for both forward and reverse movements of the OHC , by changing polarity of supply . The driver motor gets started after a delay .

4.4. POWER SUPPLY :

- The OHCC receives its power supply from voltage regulators .
- A multitapped transformer is used to provide the input for voltage regulator .
- Since the microcontroller and the sensors , drivers , etc . , working in different (5V or 24V) voltages , two supplies are provided .
- To avoid overheating of the power components , heat sinks and pre - regulator equipments are used .
- To avoid harmonics or rather noise , capacitors are used at the inputs and the outputs of the regulator .
- An I . C . combination filter can be used to filter out unwanted noise harmonics .

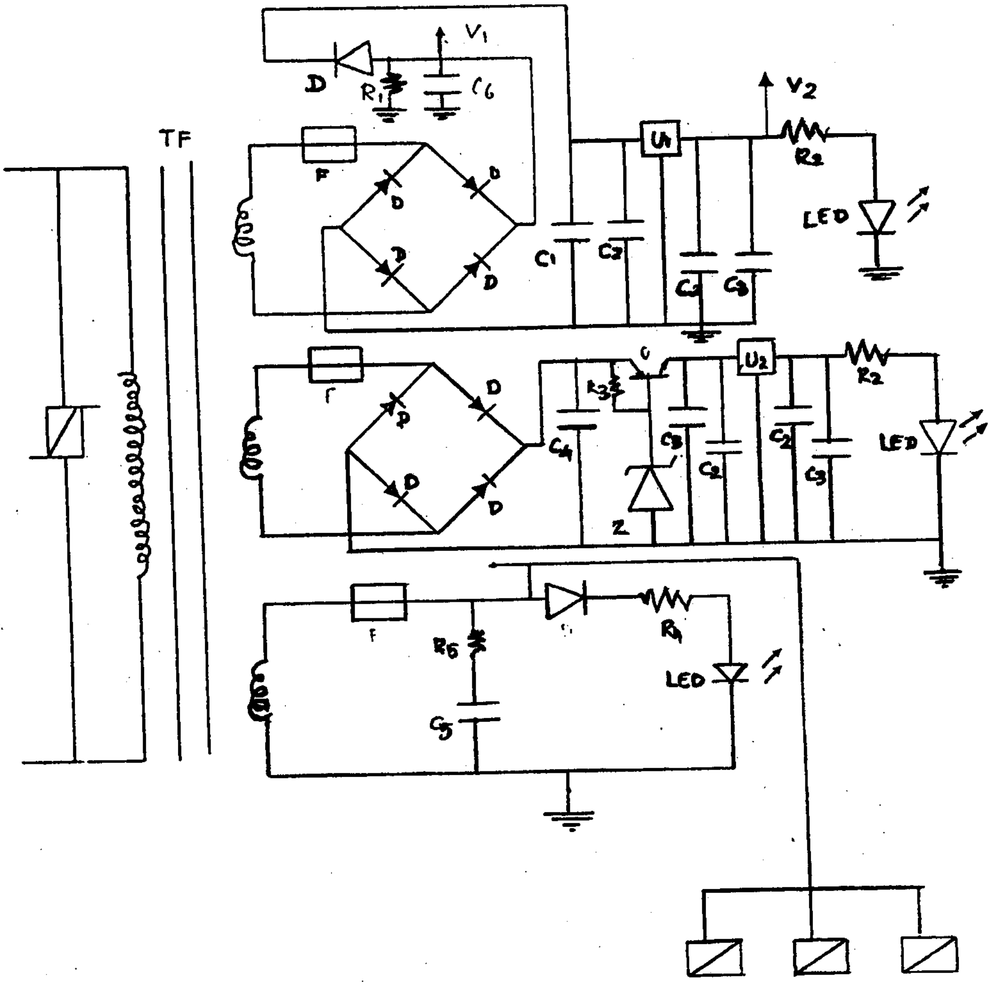


Fig 2.1 POWER SUPPLY

SYSTEM WORKING

CHAPTER 5

SYSTEM WORKING

- The power supply of +5V & +24V is given to the OHCC .
- Now the OHCC is ready for operation .
- The *start* signal is given to the controller using the push button switch .
- The input signal is indicated by LEDs connected to the input port of the OHCC.
- The *start* signal is thus sensed by microcontroller which in turn energizes the contactors K1 and K2 as programmed .
- Now the microcontroller scans for the rest of the input signals .
- The working of the OHCC for the other input signals can be explained as follows .

5.1. RESPONSE OF OHCC TO INPUT SIGNALS :

- **OBSTACLE 1 :**

When the cleaner controller receives this signal from the sensor , it de-energizes the contactor K2 and energizes K3 after a preset delay .

- **OBSTACLE 2 :**

When the cleaner controller receives this signal from the sensor , it de-energizes K3 and energizes K2 after a preset delay .

➢ **AUTO REVERSE :**

Two conditions are possible if ***auto reverse signal*** is received .

1. If K2 is in '*on*' condition and K3 is '*off*' .
   Under this condition, the cleaner controller de - energizes K2 and energizes K3.
2. If K3 is in '*on*' condition and K2 is '*off*' .
   During this condition, the cleaner controller switches *off* K3 and energizes K2 .

➢ **DISCHARGE :**

The two conditions to be considered in this case are,

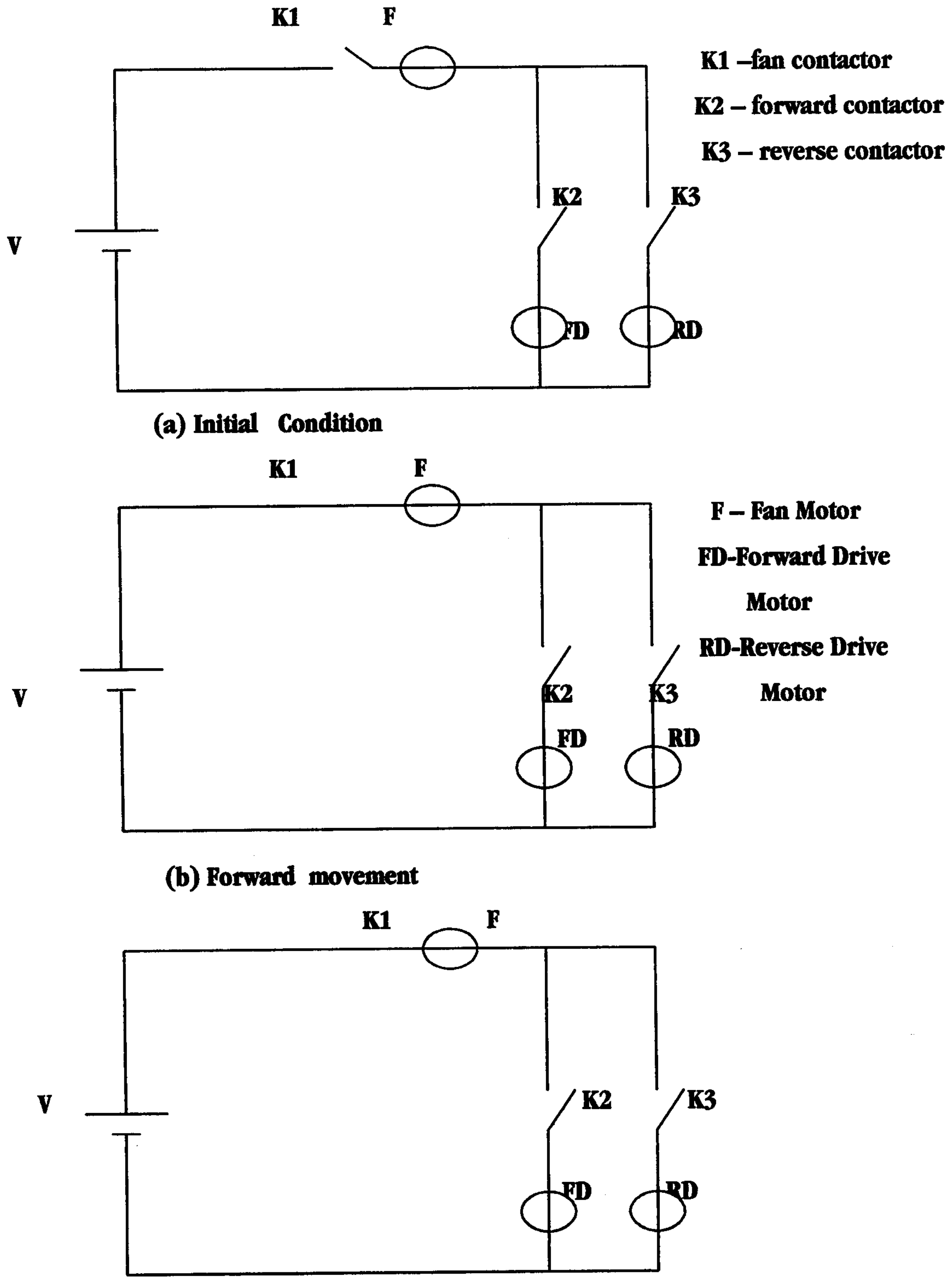
1. When K2 is '*on*' and K3 is '*off*' .
   During this condition, the cleaner controller de - energizes K2 and switches it '*on*' after a preset delay .

2. When K3 is '*on*' and K2 is '*off*' .
   Under this condition, the cleaner controller switches *off* K3 for a preset time and energizes K3 again after the delay .

➢ **STOP :**

When the cleaner controller receives this signal, it de – energizes the driver contactors followed by the fan contactor .

The OHCC works as explained above, until receives the *stop* signal .



(a) Initial Condition

(b) Forward movement

(C) Reverse movement

Fig : 5 . 1. Eqvivalent relay circuits

5.2. FIELD WORKING :

The working of cleaner controller can be very well understood when the OHC operations are studied.

- As soon as the OHCC is energized, the fan motor of the cleaner gets started up followed by the forward drive motor .
- The cleaner moves in the forward direction initially .
- When an obstruction is sensed by the OHCC, the cleaner moves in the reverse direction to avoid the obstacle .
- As the ends of the track are sensed by the controller, the cleaner automatically reverses it 's direction, (i.e.) it stops for a preset time and automatically reverses it 's direction .
- When the discharge bag is sensed by the cleaner, it stops a preset delay and discharges the collected fluff and continues to travel in the same direction .
- The OHC stops when the *stop* switch is pressed .

Thus the OHC works according to the instructions given to the microcontroller of the OHCC .

LOGICAL CONTROL FLOW

CHAPTER 6

LOGICAL CONTROL FLOW

Programming the microcontroller is the important task in this project. The instruction given to the microcontroller coordinates all the accessories connected to the controller.

Programming Steps:

Both the ports of microcontroller (Port 1 & Port 3) are used in the project.

Step 1: Port 1 bits are designed as input and port 3 bits function as output bits.

Step 2: The main loop of the program checks for the start signal.

Step 3: As the microcontroller finds the start bit of port 1 low, the corresponding bits of K1 & K2 (contactors) in port 3 are made low.

Step 4: Now the microcontroller starts to scan the input bits to see if any input signal is received.

Step 5:

- If the input is OBSTACLE 1 then

1. K2 bit is made high (off).
2. A delay loop is executed.
3. K3 bit is made low (on) and control is returned to the main loop.

- If the input is OBSTACLE 2 then

1. K3 bit is made high (off).
2. Delay loop is executed .
3. K2 bit is made low (on) and control is returned to the main loop.

- If the input is AUTO REVERSE then

  1. A check on K3 , K2 bits is performed .

  Condition 1 :

  If K2 bit is low and K3 bit is high then K2 is made high , followed by a delay loop execution and K3 is made low .

  Condition 2 :

  If K3 bit is low and K2 bit is high then K3 is made high , followed by a delay loop execution and K2 is made low .

  2. The control is returned to the main loop.

- If the input is DISCHARGE then

  1. A check on K2 , K3 bits is performed.

  Condition 1 :

  If K2 is low then K2 is made high and a delay loop is executed for preset number of times and K2 is again made low .

  Condition 2 :

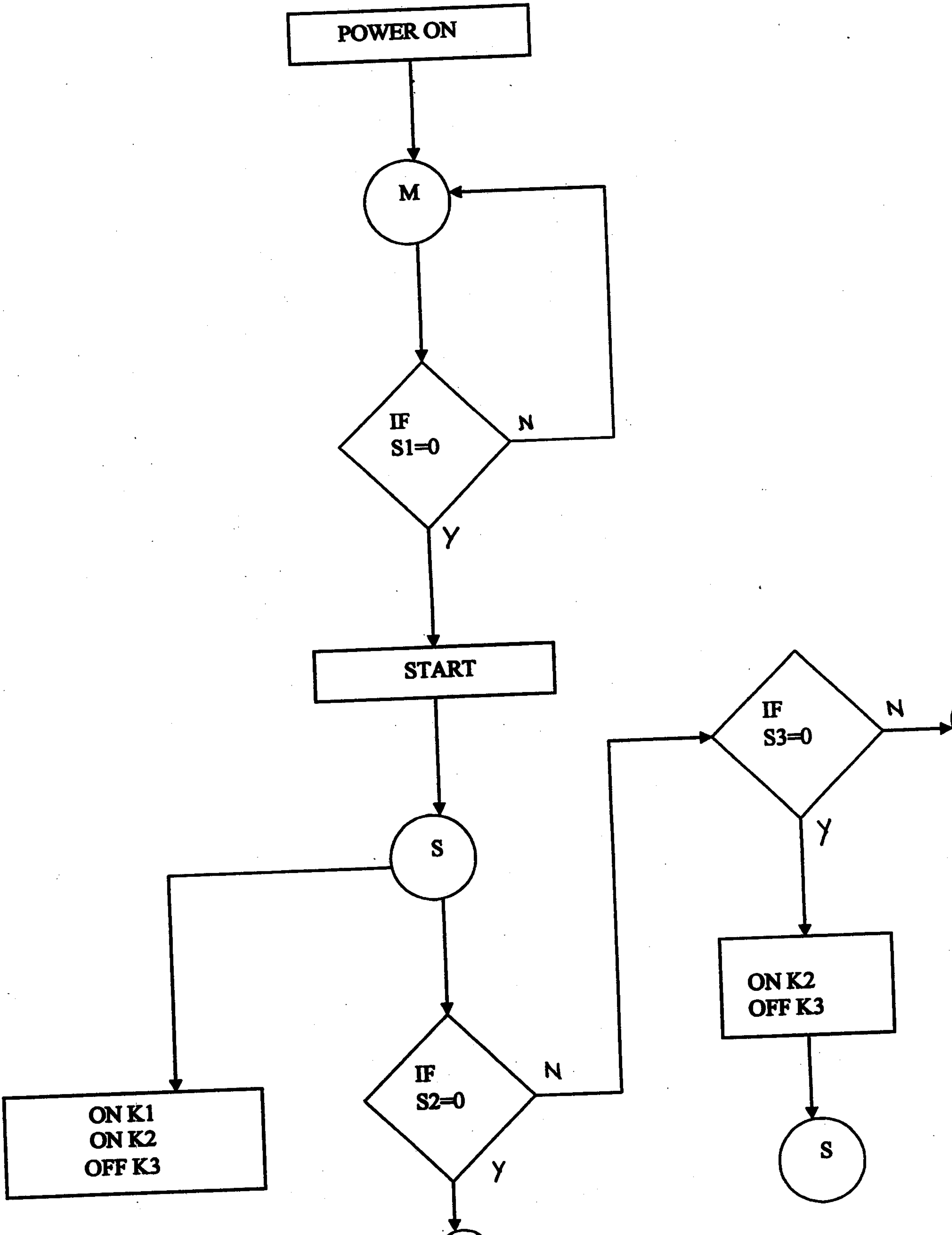
  If K3 is low then K3 is made high and delay loop is executed for a preset number of times and K3 is again made low.

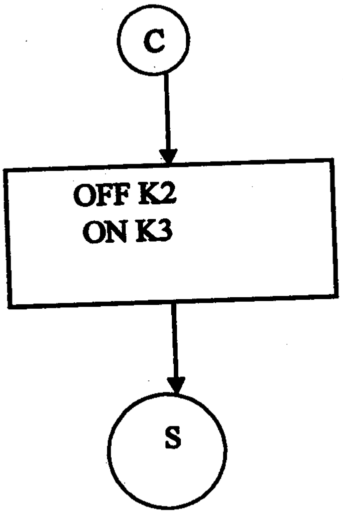
  2. Control is returned to the main loop.

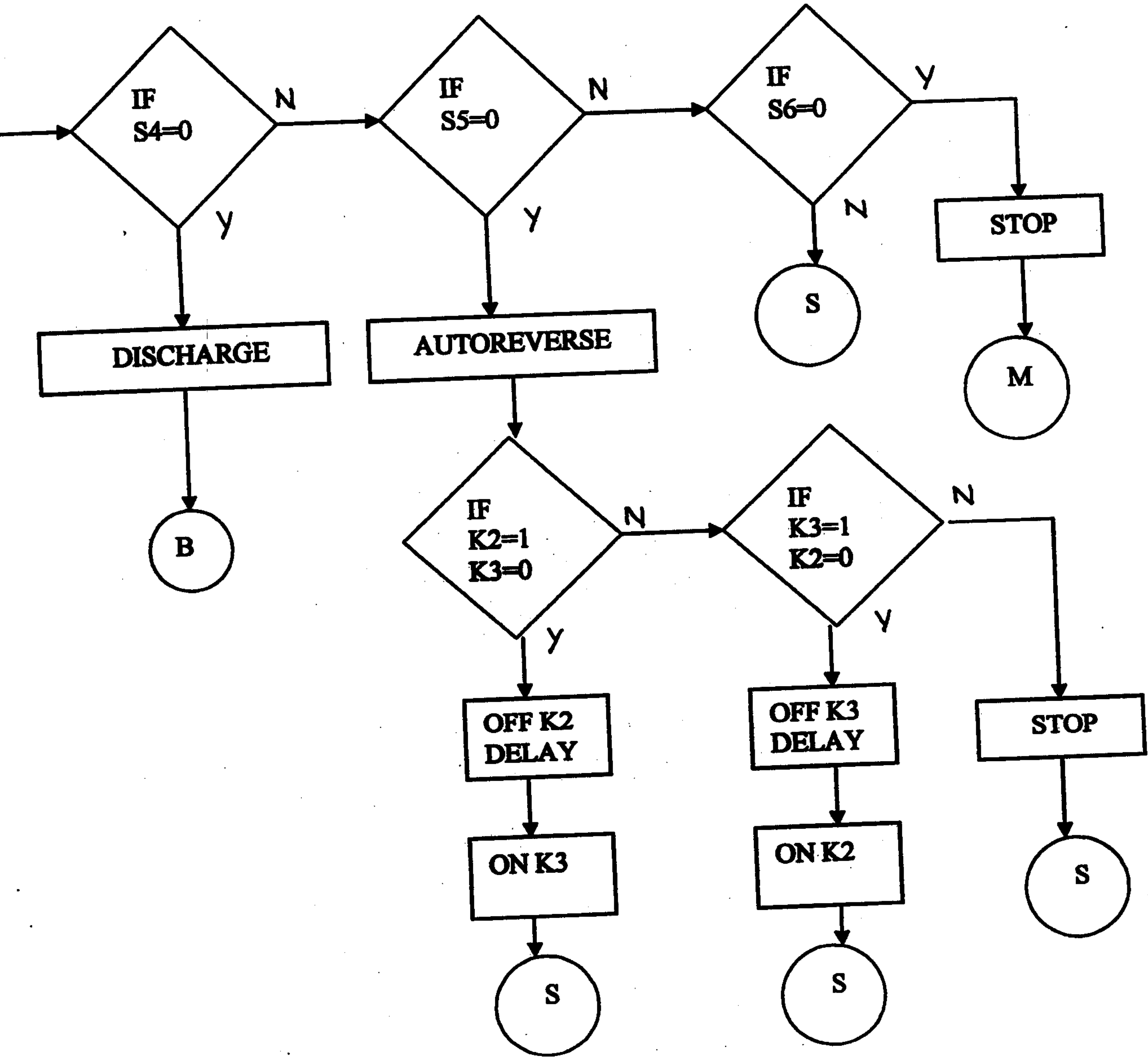
- If the input is STOP then
  1. K2 and K3 bits are made high followed by K1 after a preset delay .

Step 6 : The required subroutine is executed and the control again comes to the main loop .

Step 7: This looping process continues until the microcontroller finds the stop bit of input port to be high .


POWER ON
M
IF
S1=0
N
Y
START
S
IF
S2=0
N
Y
ON K1
ON K2
OFF K3
IF
S3=0
N
Y
ON K2
OFF K3
S


C
OFF K2
ON K3
S


IF
S4=0
N
y
DISCHARGE
B
IF
S5=0
N
y
AUTOREVERSE
IF
S6=0
y
N
S
STOP
M
IF
K2=1
K3=0
N
y
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S
IF
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K2=0
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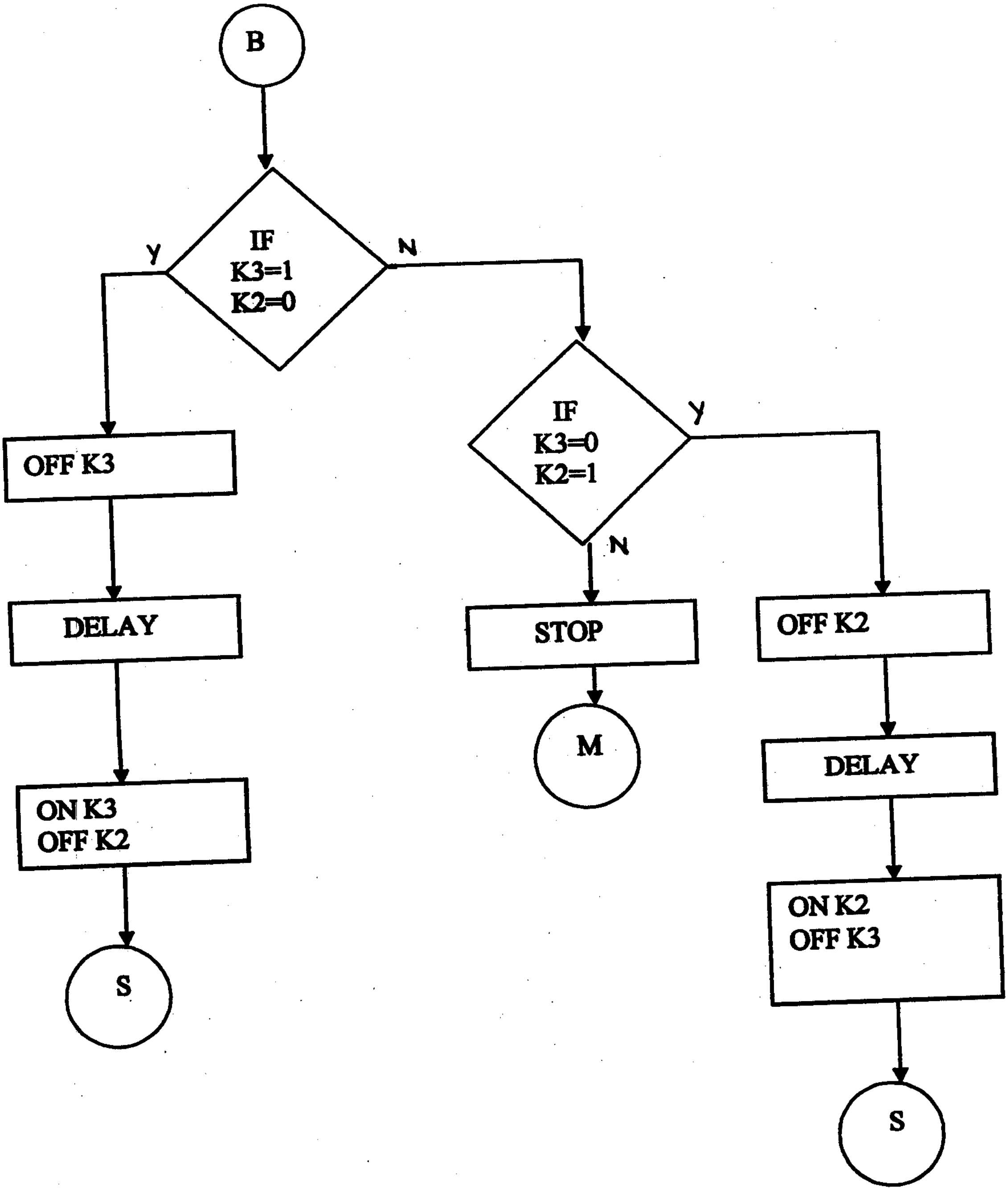
y
OFF K3
DELAY
ON K2
S
STOP
S


B
IF
K3=1
K2=0
Y
N
OFF K3
DELAY
ON K3
OFF K2
S
IF
K3=0
K2=1
Y
N
STOP
M
OFF K2
DELAY
ON K2
OFF K3
S

COMPARATIVE STUDY

CHAPTER 7

COMPARITIVE STUDY

The reason for the usage of microcontroller instead of microprocessor can be best understood from a comparative study using block diagram .

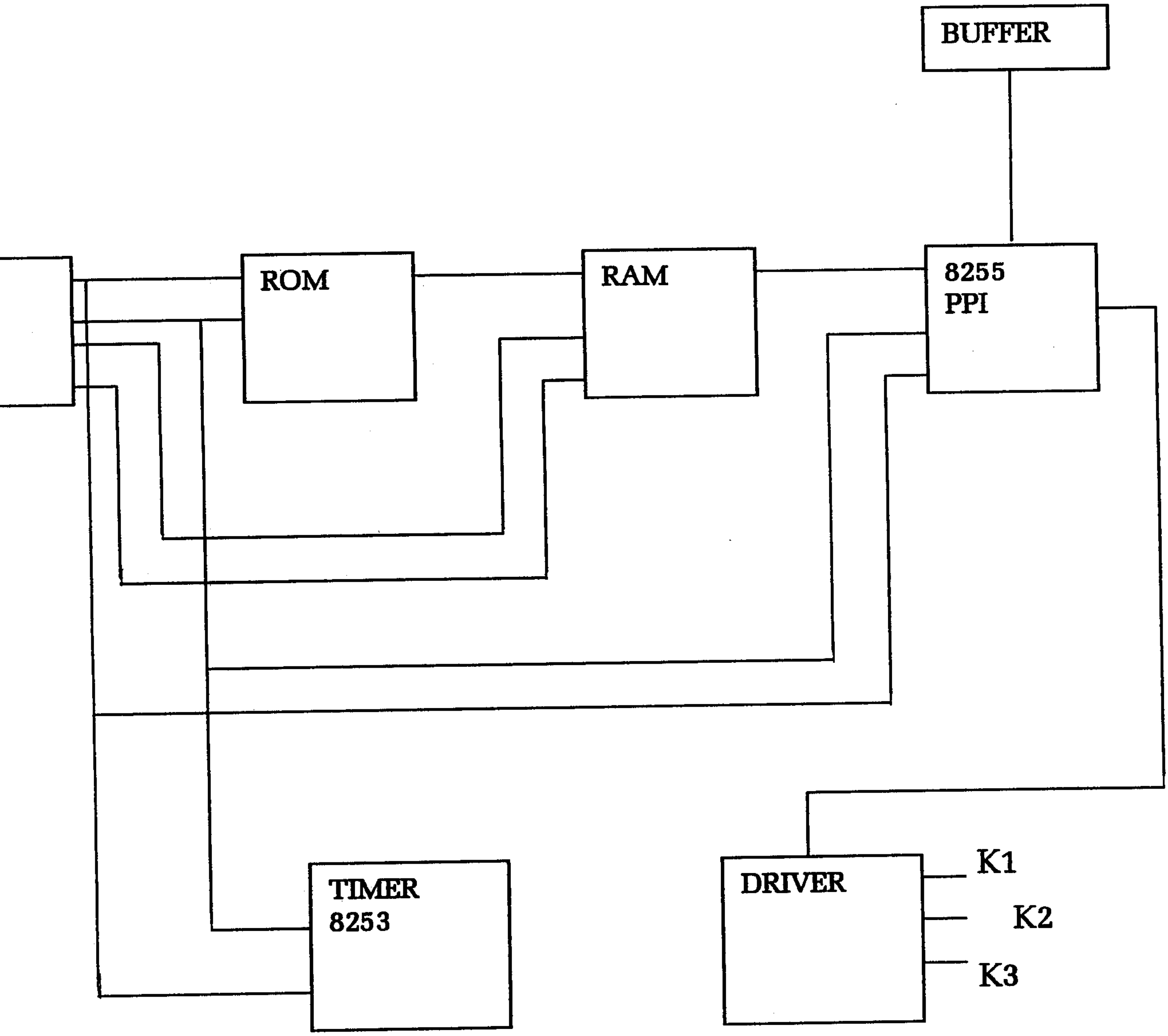


Fig :7.1.Implementation of OHCC using microprocessor

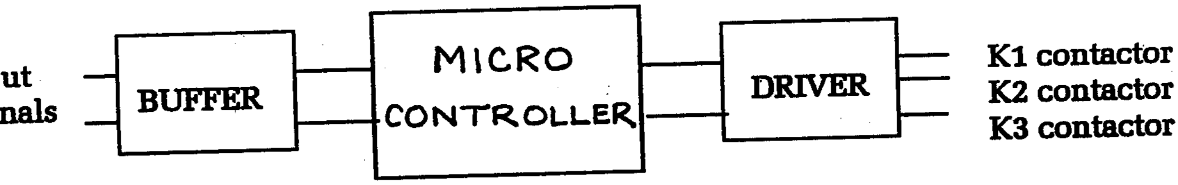


Fig : 7.2. Block diagram of OHCC using microcontroller

By referring to the above blocks it can be inferred that a microprocessor needs a number of external accessories when compared to a microcontroller and thus requiring a lot of space. Hence the cost of the system increases with a trade of in efficiency.

FEATURES

CHAPTER 8

FEATURES

8.1. SPECIAL FEATURES:

- The electronic circuit incorporates microcontroller for low power consumption and high reliability.
- Complete operational status of the electronic system is indicated in the LEDs resulting in easy maintenance and troubleshooting.
- Inductive sensors enable non - contact reversal at the end of every cycle.
- Push button switches on both sides of the system for start and stop make manual control possible.

8.2.OPTIONAL FEATURES:

- Dip switches can be used to select required program from a number of programs of microcontroller to make OHC perform a desired task.
- Programmable timer adjustments can be provided for the reversing discharging etc.,

8.3SAFETY:

- Primary current supply through completely enclosed safety contact rails.
- Power pack with the mechanical and electrical interlock contactors.

CONCLUSION

CHAPTER 9
CONCLUSION

This project was designed and developed using micro controller AT89C2051 and was tested on 'the Cleaner test equipment'. It was found to be efficient and satisfactorily fulfilled the real time requirements without any case of hang over.

The newly developed system is applicable for all sorts of industrial environments and the micro controller can be programmed to include a number of other functions such as intelligent reversal, adjustable delay periods etc.

QUESTIONAIRE

QUESTIONAIRE

NAME : Ramani. N

ADDRESS : EASTMAN FASHIONS
ODAKKADU, TIRUPUR-602

RESPONDENT :

☑ Managing Director

□ Chief Executive

□ Chief Engineer

□ Manager

□ Others

Exisiting cleaning system : ANS 220

Supplier details : ELGI JACOBI

Expectation of customer for the product : Low maintainence,
Cost effective

Rating of features of your product by customer

☑ Quality

□ Savings

□ Price

□ Warranty

☑ Reliability

N. RAMANI M.Tech (Text.)

EASTMAN Fashions

QUESTIONAIRE

NAME : R.Ramasubramanian

ADDRESS : M/S SHIVA TEXTILES
DINDIGUL

RESPONDENT :

- □ Managing Director
- □ Chief Executive
- □ Chief Engineer
- ☑ Manager
- □ Others

Exisiting cleaning system : Rooth haka

Supplier details : y

Expectation of customer for the product : Quality, User friendly

Rating of features of your product by customer

- ☑ Quality
- □ Savings
- ☑ Price
- □ Warranty
- □ Reliability

R. Ramasubramanian
General Manager

Shiva Textiles

QUESTIONAIRE

NAME : G. Raveendran

ADDRESS : Alagendra Textiles Ltd,
Theni-1.

RESPONDENT :

□ Managing Director

□ Chief Executive

□ Chief Engineer

☑ Manager (AGM)

□ Others

Exisiting cleaning system : Pricol XL250

Supplier details : Pricol, Coimbatore

Expectation of customer for the product :

– easy to operate –

Rating of features of your product by customer

□ Quality

□ Savings

□ [✓ Price]

□ Warranty

□ [✓ Reliability]

G. Raveendran
Asst. General Manager (Production)

QUESTIONAIRE

NAME : S. Maruthachalam

ADDRESS : Vanajaa Textiles Limited
Thrissur - 028

RESPONDENT :

☑ Managing Director (VP)

□ Chief Executive

□ Chief Engineer

□ Manager

□ Others

Exisiting cleaning system : elgi jacobi

Supplier details : J engineers, coimbatore

Expectation of customer for the product : automatic type
- low priced

Rating of features of your product by customer

☑ Quality

□ Savings

☑ Price

□ Warranty

□ Reliability

Sathguru Maruthachalam
Vice President

VANAJ
Vanajaa

Kurichikara Post,
Thrissur - 680 028.
Phones : 0487-695521, 695605,

QUESTIONAIRE

NAME : Chellam . S.

ADDRESS : M/s Sivasubramanian Spinning Mills (P) Ltd.
Rasipuram . T-K.

RESPONDENT :

□ Managing Director

□ Chief Executive

□ Chief Engineer

□ Manager

☑ Others (GM)

Exisiting cleaning system : –

Supplier details : –

Expectation of customer for the product : low cost and easy maintainence

Rating of features of your product by customer

☑ Quality

□ Savings

☑ Price

□ Warranty

□ Reliability

S. Chellam, M.Tech
General Manager

**Sivasubramaniam Spinning Mills
Private Limited**

Mills Kurukkapuram, Andagalore Gate (Post) - 637 401,
Rasipuram T.K. India. ✆04287-82-565, 04287-82-523

QUESTIONAIRE

NAME : Nallathambi P.

ADDRESS : K.K.P. Textiles Ltd,
Namakkal-001

RESPONDENT :

☑ Managing Director

□ Chief Executive

□ Chief Engineer

□ Manager

□ Others

Exisiting cleaning system : Rots, Vetal plus

Supplier details : Rots, madras

Expectation of customer for the product : low maintainence and reliability

Rating of features of your product by customer

□ Quality

□ Savings

☑ Price

□ Warranty

☑ Reliability

KKP

P. Nallathambi B.Com.,
Managing Director.

K.K.P. TEXTILES LTD.,
K.K.P. SPINNING MILLS LIMITED

QUESTIONAIRE

NAME : M Sambandam

ADDRESS : TTK Textiles Ltd (SD)
Madras.

RESPONDENT :

□ Managing Director

☑ Chief Executive

□ Chief Engineer

□ Manager

□ Others

Exisiting cleaning system : Stotex, Elgi Jacobi

Supplier details : R.K. Associates, Madras

Expectation of customer for the product : Cost, maintenance

Rating of features of your product by customer

☑ Quality

□ Savings

☑ Price

□ Warranty

☑ Reliability

M. Sambandam
B.Sc., B.Sc., (Tech.). M.B.A., F.I.E.
CHIEF EXECUTIVE

TTK TEXTILES LTD.
SPINNING DIVISION

QUESTIONAIRE

NAME : T. K. Gunasekaran

ADDRESS : M/s Prime Textiles Ltd
Tirupur-603

RESPONDENT :

- □ Managing Director
- □ Chief Executive
- □ Chief Engineer
- □ Manager
- ☑ Others (GM)

Exisiting cleaning system : Elgi-Jacobi

Supplier details : -

Expectation of customer for the product : Cost, Service

Rating of features of your product by customer

- □ Quality
- □ Savings
- ☑ Price
- ☑ Warranty
- ☑ Reliability

ISO 9002
Reg. by
KPMG
The Quality Advantage

PRIME

T.K. GUNASEKARAN
General Manager (Works)

PRIME TEXTILES LIMITED

QUESTIONAIRE

NAME : SUBRAMANIAN. S.G.

ADDRESS : SRI AMBAL TEXTILES,
COIMBATORE-028

RESPONDENT :

- □ Managing Director
- □ Chief Executive
- □ Chief Engineer
- ☑ Manager
- □ Others

Exisiting cleaning system : -(NIL)-

Supplier details : -

Expectation of customer for the product : Price, service

Rating of features of your product by customer

- □ Quality
- □ Savings
- ☑ Price
- ☑ Warranty
- □ Reliability

S. G. SUBRAMANIAN
B TECH. (Textiles)

SRI AMBAL TEXTILES

RESI
OFFICE

QUESTIONAIRE

NAME : K. Arun.

ADDRESS : K.P.R. Mill
Tirupur - 52

RESPONDENT :

- □ Managing Director
- □ Chief Executive
- ☑ Chief Engineer
- □ Manager
- □ Others

Exisiting cleaning system : ROOTS

Supplier details :

Expectation of customer for the product : low cost

Rating of features of your product by customer

- □ Quality
- ☑ Savings
- ☑ Price
- □ Warranty
- □ Reliability

K. ARUN AGM

K.P.R. MILL PRIVATE LIMITED

MILL UNIT :
INDIAMPALAYAM VILLAGE,

ADMN. OFFICE :
252, PERIYAR COLONY,
ANUPPARPALAYAM,

REFERENCE

REFERENCE BOOKS:

1. Kenneth J Ayala, The 8051 Microcontroller Architecture,Programming And Applications, second edition

2. ATMEL handbook

3. M.S. Berde, Thyristor Engineering

4. Albert Paul Malvino, Electronic Principles

ures

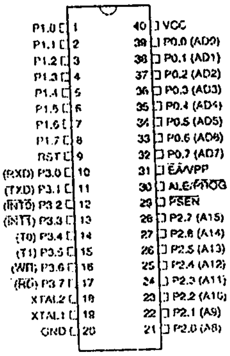
- atible with MCS-51™ Products
- tes of In-System Reprogrammable Flash Memory
- ndurance: 1,000 Write/Erase Cycles
- Static Operation: 0 Hz to 24 MHz
- -level Program Memory Lock
- 8-bit Internal RAM
- ogrammable I/O Lines
- 6-bit Timer/Counters
- terrupt Sources
- rammable Serial Channel
- power Idle and Power-down Modes

cription

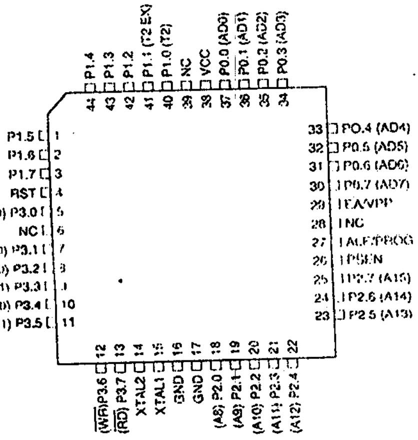
T89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K of Flash programmable and erasable read only memory (PEROM). The device ufactured using Atmel's high-density nonvolatile memory technology and is tible with the industry-standard MCS-51 instruction set and pinout. The on-chip allows the program memory to be reprogrammed in-system or by a conven- nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash onolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ly-flexible and cost-effective solution to many embedded control applications.

Configurations

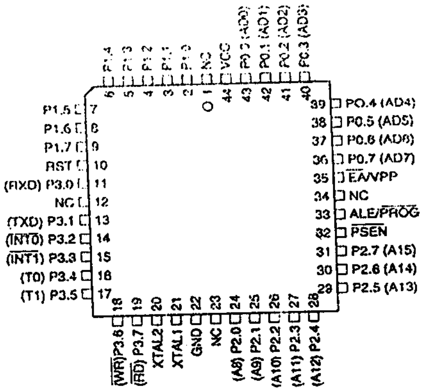
PDIP



PQFP/TQFP



PLCC

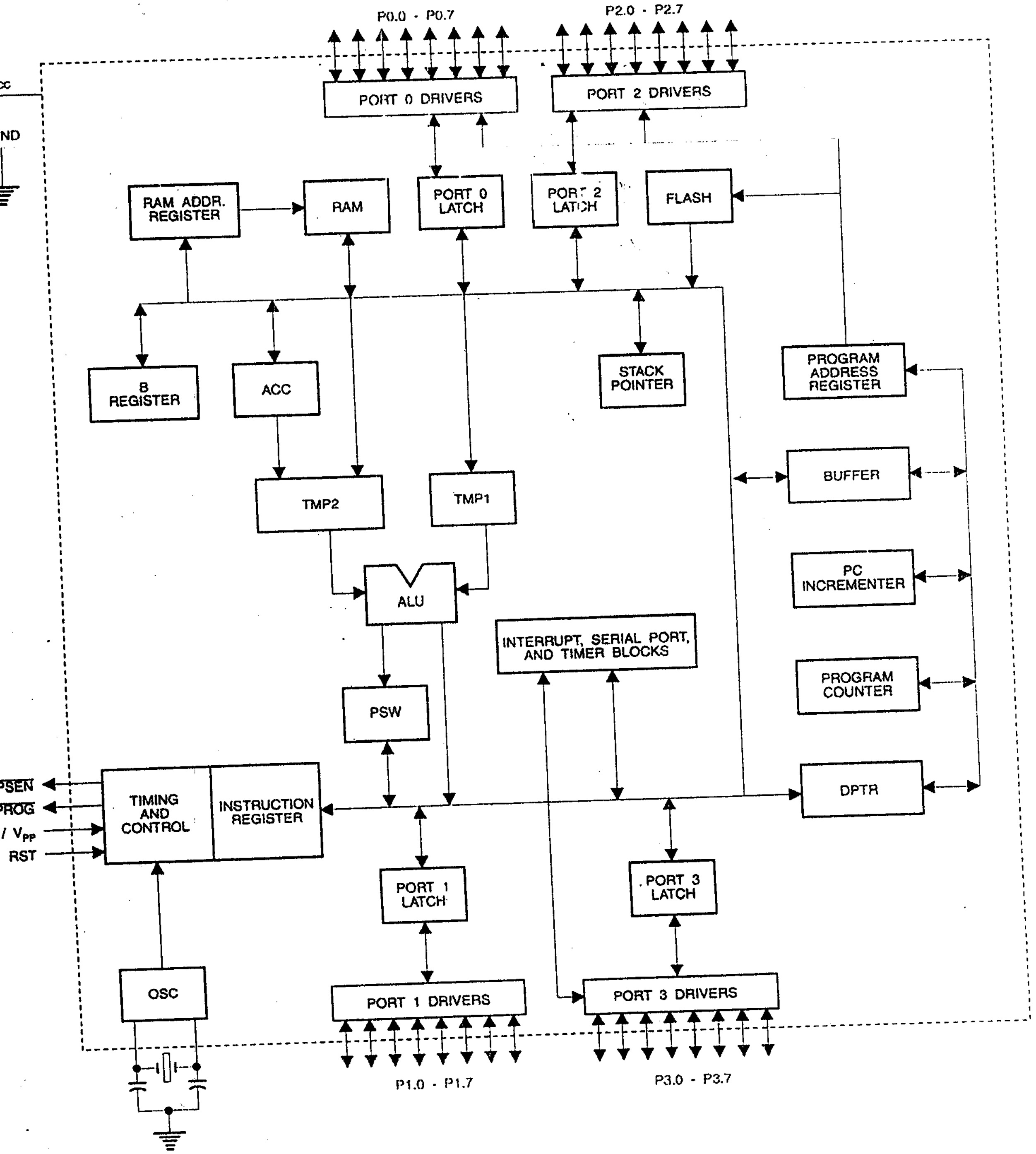


8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

k Diagram


P0.0 - P0.7
P2.0 - P2.7
cc
ND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ V_PP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

sh Programming Modes

de		RST	PSEN	ALE/PROG	EA/V$_{PP}$	P2.6	P2.7	P3.6	P3.7
e Code Data		H	L	‾╲_╱‾	H/12V	L	H	H	H
ad Code Data		H	L	H	H	L	L	H	H
e Lock	Bit - 1	H	L	‾╲_╱‾	H/12V	H	H	H	H
	Bit - 2	H	L	‾╲_╱‾	H/12V	H	H	L	L
	Bit - 3	H	L	‾╲_╱‾	H/12V	H	L	H	L
ip Erase		H	L	‾╲_╱‾ (1)	H/12V	H	L	L	L
ad Signature Byte		H	L	H	H	L	L	L	L

e: 1. Chip Erase requires a 10 ms PROG pulse.

ure 3. Programming the Flash

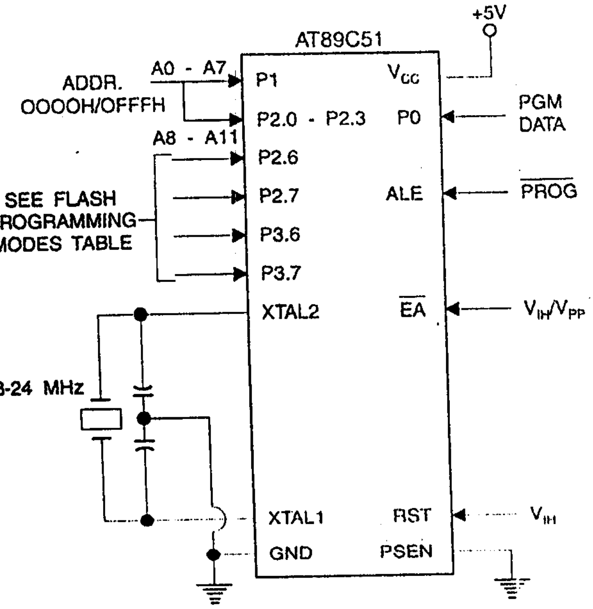
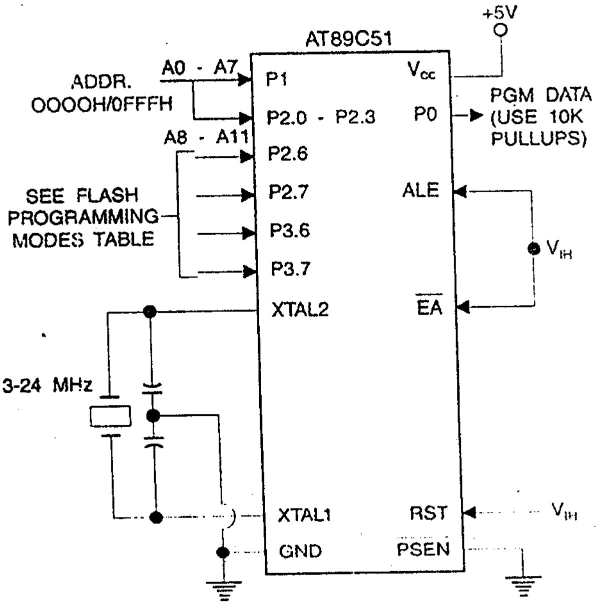
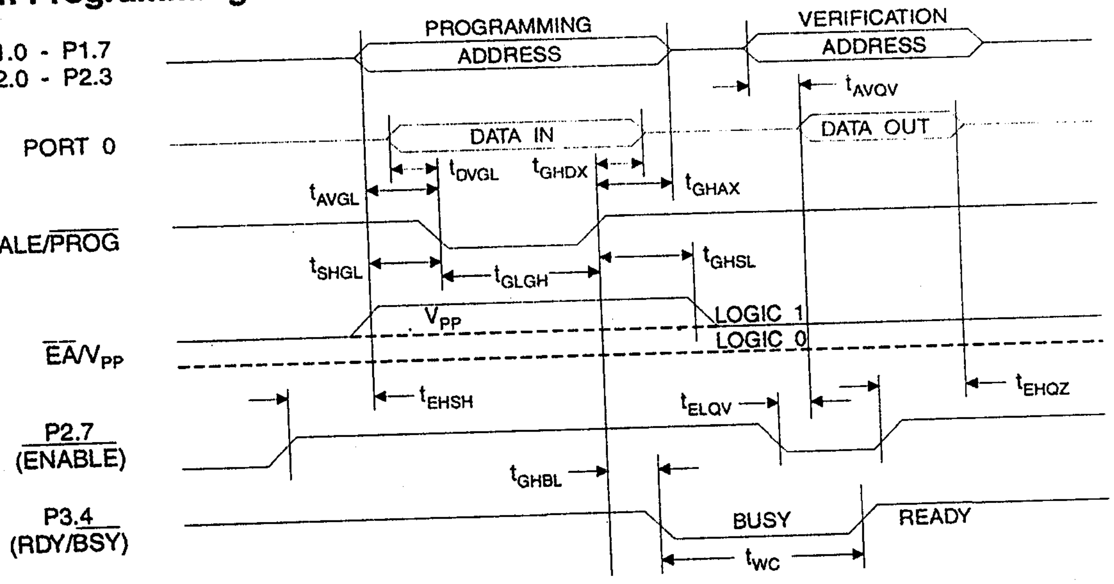


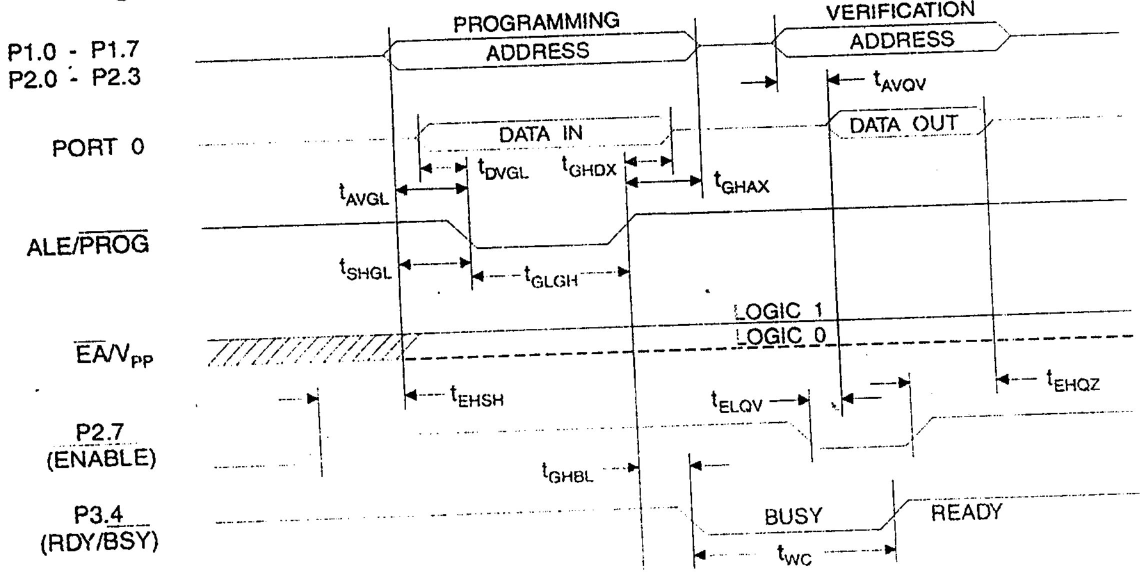
Figure 4. Verifying the Flash



h Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



ash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{\text{ENABLE}}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
t_{GHSL}[1]	V_{PP} Hold After $\overline{\text{PROG}}$	10		μs
t_{GLGH}	$\overline{\text{PROG}}$ Width	1	110	μs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	μs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
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t_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{\text{ENABLE}}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		µs
t_{GHSL}[1]	V_{PP} Hold After $\overline{\text{PROG}}$	10		µs
t_{GLGH}	$\overline{\text{PROG}}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{\text{ENABLE}}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: .1. Only used in 12-volt programming mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greate
   than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

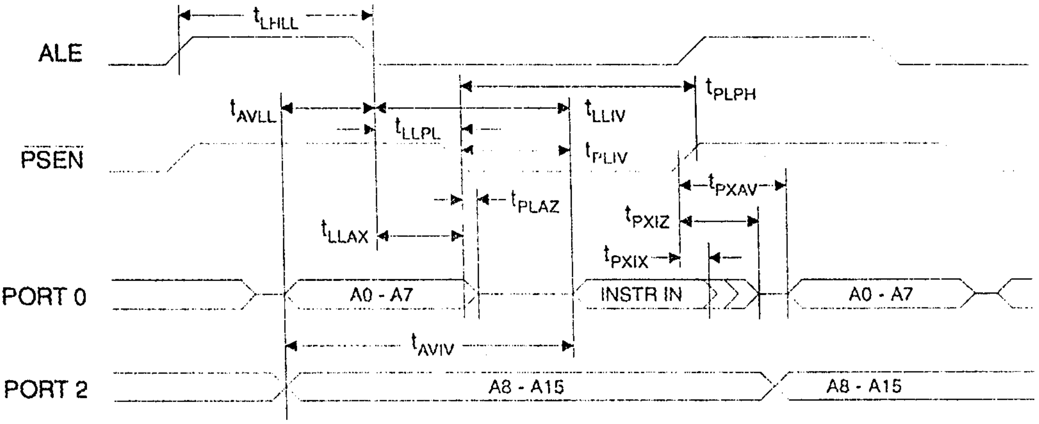
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; load capacitance for all other outputs = 80 pF.

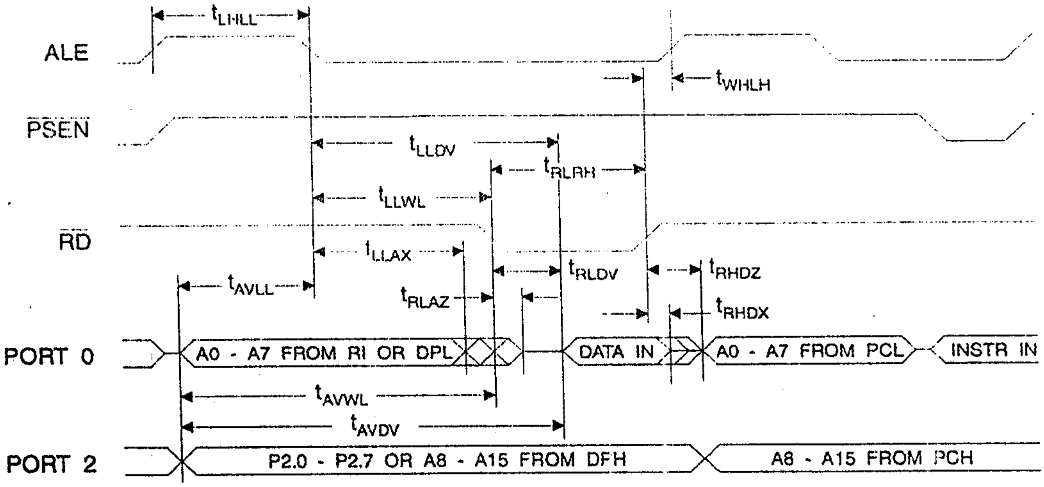
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{\text{PSEN}}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{\text{PSEN}}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{\text{RD}}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{\text{RD}}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{\text{WR}}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{\text{WR}}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{\text{WR}}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

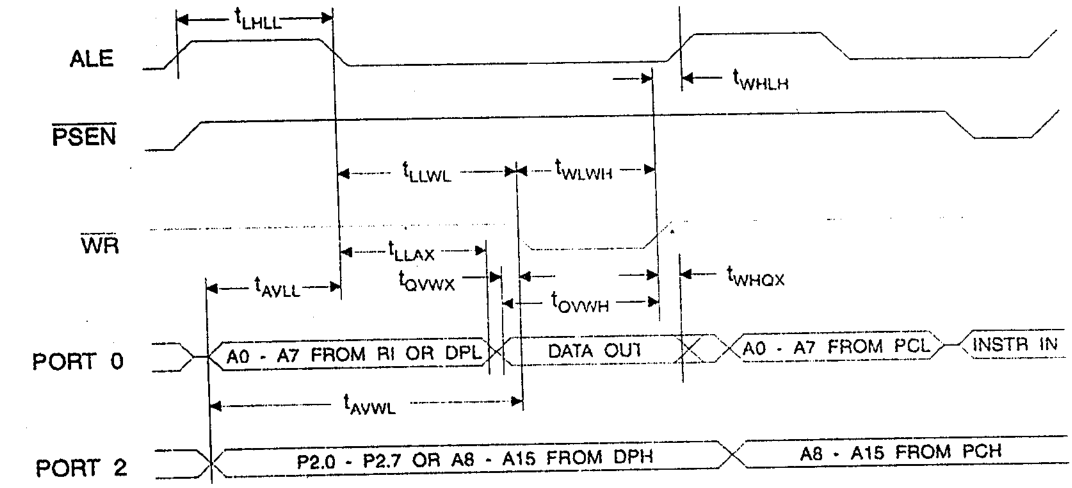
xternal Program Memory Read Cycle



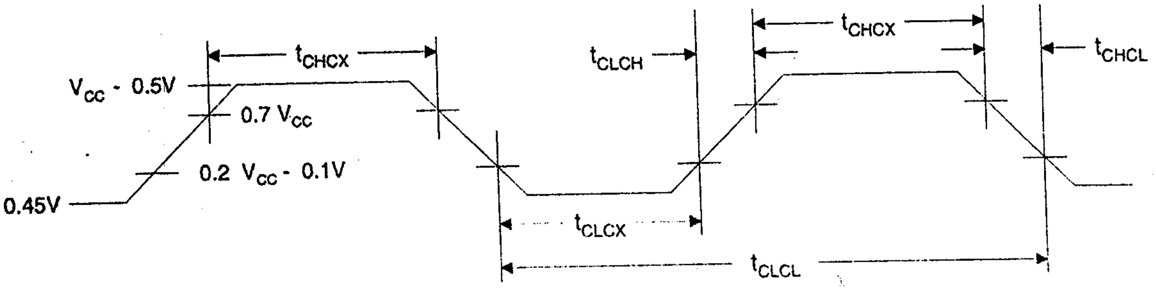
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

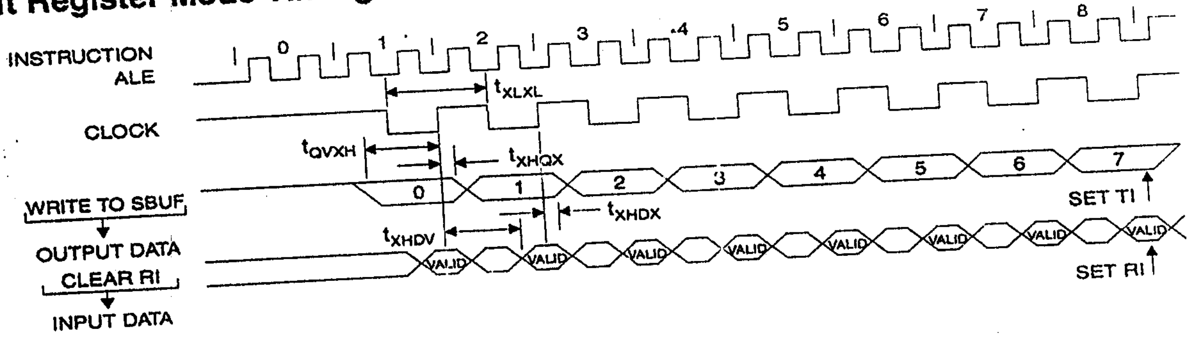
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

erial Port Timing: Shift Register Mode Test Conditions

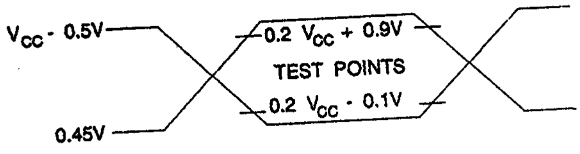
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

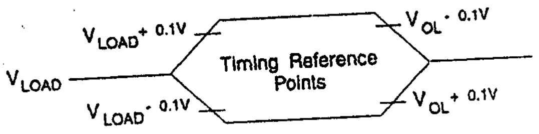


AC Testing Input/Output Waveforms[(1)]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[(1)]

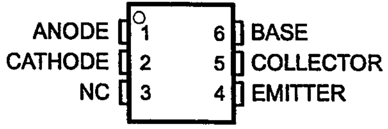


Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

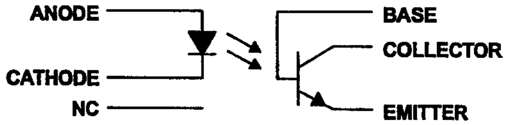
- Gallium-Arsenide-Diode Infrared Source Optically Coupled to a Silicon npn Phototransistor
- High Direct-Current Transfer Ratio
- High-Voltage Electrical Isolation
  1.5-kV, 2.5-kV, or 3.55-kV Rating
- Plastic Dual-In-Line Package
- High-Speed Switching
  t_r = 7 µs, t_f = 7 µs Typical
- Typical Applications Include Remote Terminal Isolation, SCR and Triac Triggers, Mechanical Relays and Pulse Transformers

DCJ, 4N35, 4N36, OR 4N37 PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†‡

Input-to-output peak voltage (8-ms half sine wave): 4N35	3.55 kV
4N36	2.5 kV
4N37	1.5 kV
Input-to-output root-mean-square voltage (8-ms half sine wave): 4N35	2.5 kV
4N36	1.75 kV
4N37	1.05 kV
Collector-base voltage	70 V
Collector-emitter voltage (see Note 1)	30 V
Emitter-base voltage	7 V
Input-diode reverse voltage	6 V
Input-diode forward current: Continuous	60 mA
Peak (1 µs, 300 pps)	3 mA
Phototransistor continuous collector current	100 mA
Continuous total power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	100 mW
Phototransistor (see Note 3)	300 mW
Continuous power dissipation at (or below) 25°C lead temperature:	
Infrared-emitting diode (see Note 4)	100 mW
Phototransistor (see Note 5)	500 mW
Operating temperature range, T_A	–55°C to 100°C
Storage temperature range, T_{stg}	–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

NOTES: 1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100 °C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100 °C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100 °C lead temperature at the rate of 1.33 mW/°C. Lead temperature is measured on the collector lead 0.8 mm (1/32 inch) from the case.
5. Derate linearly to 100°C lead temperature at the rate of 6.7 mW/°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 100 µA, I_E = 0, I_F = 0	70†			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 10 mA, I_B = 0, I_F = 0	30†			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 100 µA, I_C = 0, I_F = 0	7†			V
I_R	Input diode static reverse current	V_R = 6 V			10†	µA
I_{IO}	Input-to-output current	V_{IO} = rated peak value, t = 8 ms			100	mA
$I_{C(on)}$	On-state collector current	V_{CE} = 10 V, I_F = 10 mA, I_B = 0	10†			mA
		V_{CE} = 10 V, I_F = 10 mA, I_B = 0, T_A = –55°C	4†			
		V_{CE} = 10 V, I_F = 10 mA, I_B = 0, T_A = 100°C	4†			
$I_{C(off)}$	Off-state collector current	V_{CE} = 10 V, I_F = 0 I_B = 0		1	50	nA
		V_{CE} = 30 V, I_F = 0, I_B = 0, T_A = 100°C			500†	µA
h_{FE}	Transistor static forward current transfer ratio	V_{CE} = 5 V, I_C = 10 mA, I_F = 0		500		
V_F	Input diode static forward voltage	I_F = 10 mA	0.8†		1.5†	V
		I_F = 10 mA, T_A = –55°C	0.9†		1.7†	
		I_F = 10 mA, T_A = 100°C	0.7†		1.4†	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 0.5 mA, I_F = 10 mA, I_B = 0 mA			0.3†	V
r_{IO}	Input-to-output internal resistance	V_{IO} = 500 V, See Note 6	10^{11}†			Ω
C_{io}	Input-to-output capacitance	V_{IO} = 0, f = 1 MHz, See Note 6		1	2.5†	pF

† JEDEC registered data

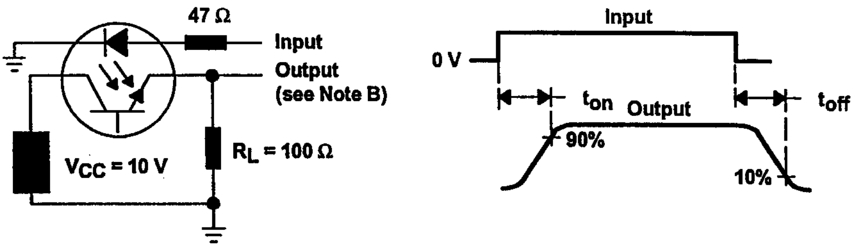
NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Time-on time	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA,			10	µs
t_{off}	Turn-off time	R_L = 100 Ω, See Figure 1			10	

† JEDEC registered data

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1% t_w = 100 µs.

B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

OFF-STATE COLLECTOR CURRENT vs FREE-AIR TEMPERATURE

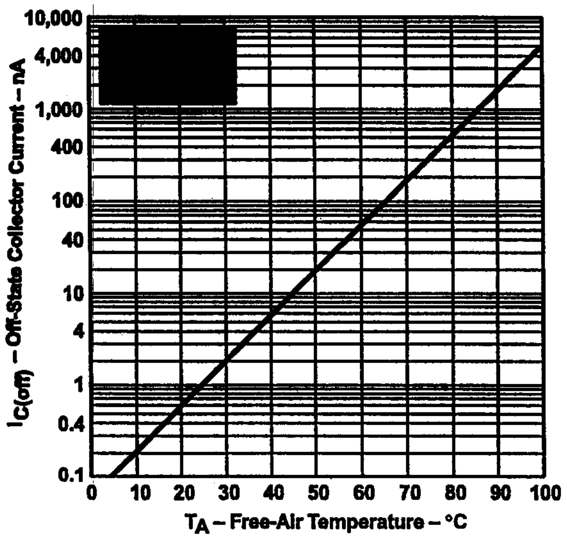


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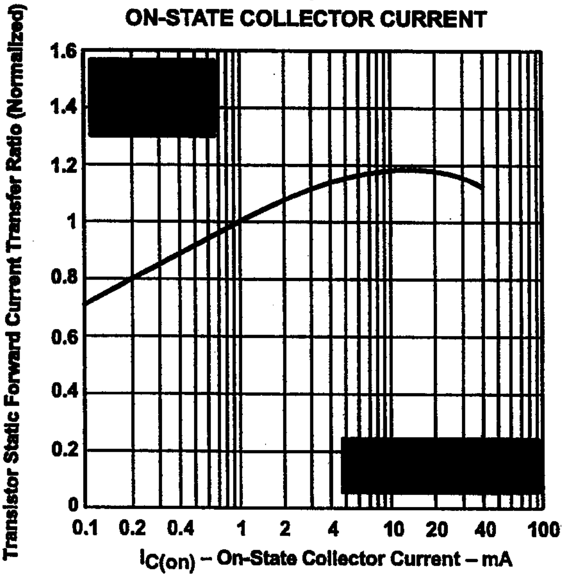
Figure 2

TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO (NORMALIZED) vs ON-STATE COLLECTOR CURRENT



[redacted]

[redacted]

Figure 3

GENERAL DESCRIPTION

Passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

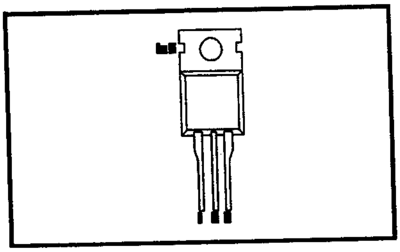
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
	BT136- BT136-	600 600F	
V_{DRM}	Repetitive peak off-state voltages	600	V
$I_{T(RMS)}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	25	A

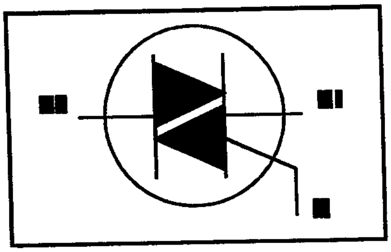
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C	-	4	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge			
		t = 20 ms	-	25	A
		t = 16.7 ms	-	27	A
I^2t	I^2t for fusing	t = 10 ms	-	3.1	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs			
		T2+ G+	-	50	A/µs
		T2+ G-	-	50	A/µs
		T2- G-	-	50	A/µs
		T2- G+	-	10	A/µs
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	°C
T_j	Operating junction temperature		-	125	°C

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.		UNIT
		BT136-			...	...F	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A					
		T2+ G+	-	5	35	25	mA
		T2+ G-	-	8	35	25	mA
		T2- G-	-	11	35	25	mA
		T2- G+	-	30	70	70	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
		T2+ G+	-	7	20	20	mA
		T2+ G-	-	16	30	30	mA
		T2- G-	-	5	20	20	mA
		T2- G+	-	7	30	30	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70		V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5		V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-		V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5		mA

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.		TYP.	MAX.	UNIT
		BT136-	...	...F			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	100	50	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 °C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	2	-	µs

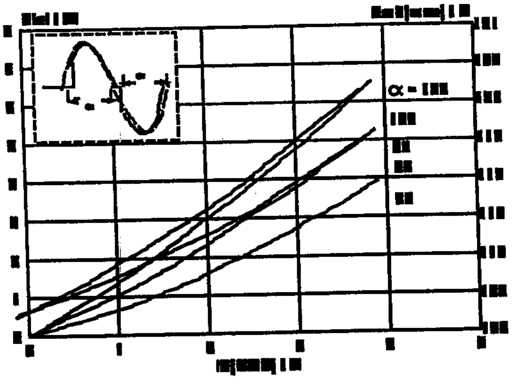


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

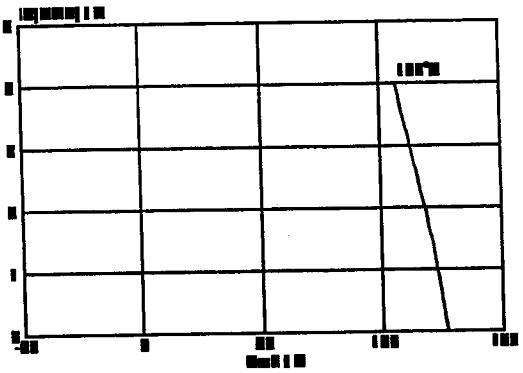


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

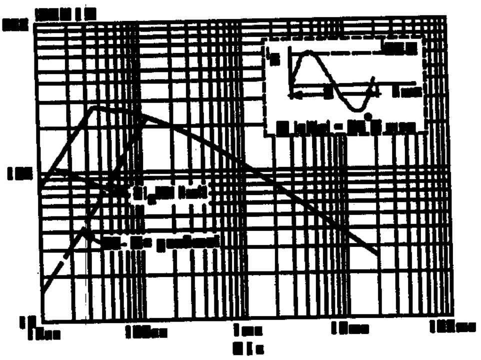


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20$ms.

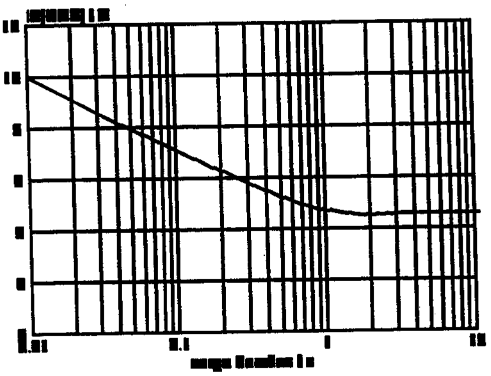


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{mb} \leq 107$°C.

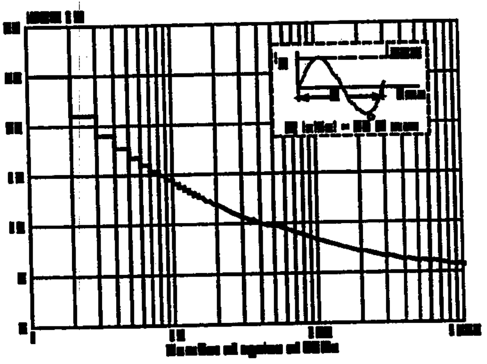


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

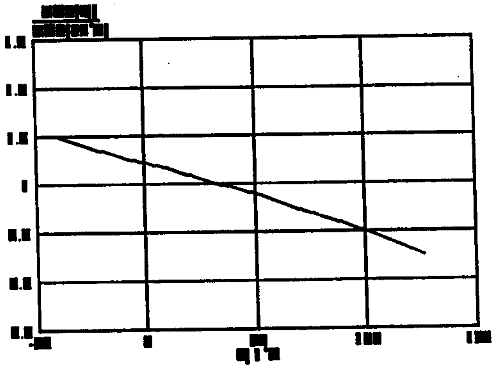


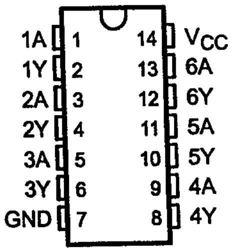
Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

SN5406, SN5416, SN7406, SN7416
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

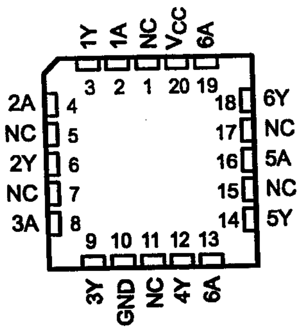
SDLS031A – DECEMBER 1983 – REVISED DECEMBER 2001

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Drivers for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

SN5406, SN5416 . . . J OR W PACKAGE
SN7406 . . . D, N, OR NS PACKAGE
SN7416 . . . D OR N PACKAGE
(TOP VIEW)



SN5406 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays), and also are characterized for use as inverter buffers for driving TTL inputs. The SN5406 and SN7406 have minimum breakdown voltages of 30 V. The SN5416 and SN7416 have minimum breakdown voltages of 15 V. The maximum sink current is 30 mA for the SN5406 and SN5416, and 40 mA for the SN7406 and SN7416.

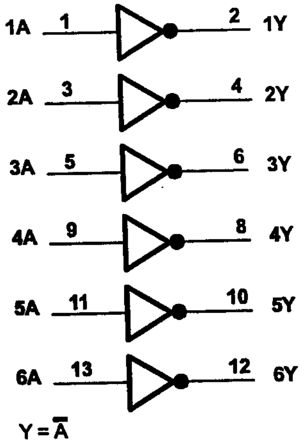
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube	SN7406D	7406
		Tape and reel	SN7406DR	
		Tube	SN7416D	7416
		Tape and reel	SN7416DR	
	PDIP – N	Tube	SN7406N	SN7406N
			SN7416N	SN7416N
	SOP – NS	Tape and reel	SN7406NSR	SN7406
–55°C to 125°C	CDIP – J	Tube	SNJ5406J	SNJ5406J
		Tube	SNJ5416J	SNJ5416J
	CDIP – W	Tube	SNJ5406W	SNJ5406W
		Tube	SNJ5416W	SNJ5416W
	LCCC – FK	Tube	SNJ5406FK	SNJ5406FK

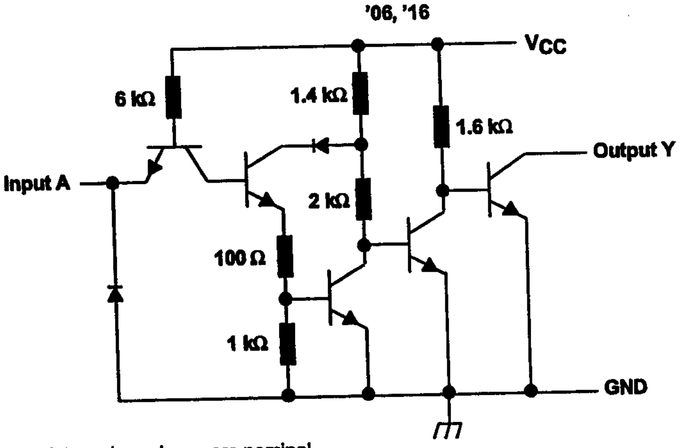
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications o Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram (positive logic)



schematic (each buffer/driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage, V_I (see Note 1)		5.5 V
Output voltage, V_O (see Notes 1 and 2):	SN5406, SN7406	30 V
	SN5416, SN7416	15 V
Package thermal impedance, θ_{JA} (see Note 3):	D package	86°C/W
	N package	80°C/W
	NS package	76°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			SN5406 SN5416			SN7406 SN7416			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	'06			30			30	V
		'16			15			15	
I_{OL}	Low-level output current				30			40	mA
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN5406 SN5416			SN7406 SN7416			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –12 mA				–1.5			–1.5	V
I_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	V_{OH} = §			0.25			0.25	mA
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 16 mA			0.4			0.4	V
			I_{OL} = ¶			0.7			0.7	
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_{IH} = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V				–1.6			–1.6	mA
I_{CCH}	V_{CC} = MAX				30	48		30	48	mA
I_{CCL}	V_{CC} = MAX				32	51		32	51	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ V_{OH} = 30 V for '06 and 15 V for '16.

¶ I_{OL} = 30 mA for SN54' and 40 mA for SN74'.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω, C_L = 15 pF		10	15	ns
t_{PHL}					15	23	

8051 INSTRUCTION SET

DATA TRANSFER INSTRUCTION

MOV Dest byte , src byte

The following 15 instructions are the data transfer instructions.
The data is being transferred between register to register or register to internal data memory .

1) Syntax : **MOV A, Rn**
Description : move the register contents into the accumulator.
Mathematically :(A) ⟵ (Rn)
Bytes : 1
Cycles : 1
Encoding : 1 1 1 0 1 r r r ; r r r bits are the encoded bits corresponding registers R0 to R7. The opcode for this instruction is EB H.
Flags affected : nil
Addressing mode : register addressing

2) Syntax : **MOV A , direct**
description : move the contents of the direct byte into the accumulator.
Mathematically :(A) ⟵ (direct)
Bytes : 1
Cycles :1
Encoding :1 1 1 0 0 1 0 1 direct address byte
Opcodes :E5,direct address byte
Flags affected :nil
Addressing mode :direct memory addressing

3) Syntax : **MOV A,@Ri**
description : move the contents of the internal datamemory indirectly addressed.
Mathematically : (A) ⟵ ((Ri))
Bytes : 1
Cycles : 1
Encoding : 1 1 1 0 0 1 1 1
Opcodes : E6-E7H,direct address byte
Flags affected : nil
Addressing mode : Register indirect addressing

4) Syntax : **MOV A ,# data 8**
description : move the immediate data 8 in the instruction into the accumulator.
Mathematically : (A) ←—— (data 8)
Bytes : 2
Cycles : 1
Encoding : 0 1 1 1 0 1 0 0
Opcodes : 74, immediate data byte(data 8)
Flags affected : nil
Addressing mode : immediate addressing

5) Syntax : **MOV Rn, A**
description : move the accumulator contents into the register
Mathematically : (Rn) ←(A)——
Bytes : 1
Cycles : 1
Encoding : 1 1 1 1 1 r r r
Opcodes : F5 H-FFH
Flags affected : nil
Addressing mode : Register addressing

6) Syntax : **MOV Rn, direct**
description : move the contents of the direct byte into the register
Mathematically : (Rn) ←(direct)
Bytes : 2
Cycles : 1
Encoding : 1 0 1 0 1 r r r ,direct address byte
Opcodes : A8-AFH,direct address byte
Flags affected : nil
Addressing mode : direct memory addressing

7) Syntax : **MOV Rn, #data8**
description : move the contents of the direct byte into the register
Mathematically : (Rn) ←——(data8)
Bytes : 2
Cycles : 1
Encoding : 0 1 1 1 1 r r r ,
Opcodes : 78-7FH,immediate data byte (data 8)
Flags affected : nil
Addressing mode : immediate addressing

8) Syntax : **MOV direct ,A**

description : move the contents of the accumulator into the internal data memory

Mathematically : (direct) ← (A)

Bytes : 2

Cycles : 2

Encoding : 1 1 1 1 0 1 01 ,direct address

Opcodes : F5H,direct address byte

Flags affected : nil

Addressing mode : direct addressing

9) Syntax : **MOV direct,Rn**

description : move the contents of the register into the internal data memory

Mathematically : (direct) ← (Rn)

Bytes : 2

Cycles : 2

Encoding : 1 0 0 0 1 r r r , direct address byte

Opcodes : 88-8FH,direct address byte

Flags affected : nil

Addressing mode : direct memory addressing

10) Syntax : **MOV direct,direct**

description : move the contents of one internal data memory location into another internal data memory location

Mathematically :(direct) ← (direct)

Bytes : 3

Cycles : 2

Encoding : 1 0 0 0 0101 , direct src,direct dst

Opcodes : 85H- direct src,direct dst

Flags affected : nil

Addressing mode : direct addressing

11) Syntax : **MOV direct,@Ri**

description : move the contents of internal data memory indirectly addressed by the Ri into another internal data memory location .

Mathematically :(direct) ← ((Ri))

Bytes : 2

Cycles : 2

Encoding : 1 0 0 0 0111

Opcodes : 86-87H, direct address byte

Flags affected : nil

Addressingmode : register indirect addressing

12) Syntax : **MOV direct,#data8**

description : move the immediate data byte(data8in the instruction) into internal data memory location.

Mathematically : (direct) ← (data8)

Bytes : 3

Cycles : 2

Opcodes : 75H,immediate data byte (data8)
Flags affected : nil
Addressing mode : immediate addressing

13) Syntax : **MOV @Ri,A**
description : move the contents of accumulator into internal data memory locationindirectly addressed by Ri.
Mathematically :((Ri)) ← (A)
Bytes : 1
Cycles : 1
Encoding : 1 1 1 1 0111
Opcodes : F6-F7H,direct address data byte
Flags affected : nil
Addressing mode : register indirect addressing

14) Syntax : **MOV @Ri,direct**
description : move the contents of internal data memory locationspecified in the instruction into another internal data memory location indirectly
Mathematically : ((Ri)) ← (direct)
Bytes : 2
Cycles : 2
Encoding : 1 01 0 0111
Opcodes : A6-A7H,direct address byte
Flags affected : nil
Addressing mode : register indirect addressing

15) Syntax : **MOV @Ri,#data8**
description : move the immediate data byte(data8in the instruction) into internal data memory location, indirectly addressed by the register R0 or R1.
mathematically : ((Ri)) ← (data8)
Bytes : 2
Cycles : 1
Encoding : 00111 0111
Opcodes : 76-77H, immediate data byte (data8)
Flags affected : nil
Addressing mode : indirect immediate addressing

16) Syntax : **MOV DPTR,#data16**
description : move the immediate data word(data16in the instruction) into DPTR .DPTR is a data memory pointer to address either external data or program memory.
mathematically : (DPTR) ← (data16)
Bytes : 3
Cycles : 2
Encoding : 1 001 0000 immediate data 15-8,immediate data 7-0
Opcodes : 90H, immediate data word (data16)
Flags affected : nil

Addressing mode : indirect immediate addressing

DATA BIT TRANSFER INSTRUCTIONS

The following are the bit transfer instructions. The data bits are being transferred between internal or SFR data bits and the carry bits.

17) Syntax : **MOV C,bit**
description : move the bit status of internal data bit specified in the instruction into the carry bit.
mathematically : (C) ⟵ (data bit)
Bytes : 2
Cycles : 1
Encoding : 1010 0010,bit address
Opcodes : A2H, bit address
Flags affected : nil
Addressing mode : bit addressing

18) Syntax : **MOV bit,C**
description : move the carry bit into internal data bit or SFR data bit specified in the instruction .
mathematically :(data bit) ⟵ (C)
Bytes : 2
Cycles :1
Encoding :1001 0010,bit address
Opcodes : 92H, bit address
Flags affected : nil
Addressing mode : bit addressing

19) Syntax : **MOVX A,@DPTR**
description : move the contents of the external data memoryindirectly into the accumulator. The external data memory address is DPTR .
mathematically : (A) ⟵ ((DPTR))
Bytes : 1
Cycles : 2
Encoding : 1110 0000
Opcodes : EOH
Flags affected : nil
Addressing mode : indirect addressing

20) Syntax : **MOVX @DPTR,A**
description : move the contents ofaccumulator into external data memory location pointed by the DPTR.
mathematically : ((DPTR)) ← (A)
Bytes : 1
Cycles : 2
Encoding : 11110000
Opcodes : F0H
Flags affected : nil
Addressing mode : indirect addressing

21) Syntax : **MOVX @Ri,A**
description : move the contents ofaccumulator into external data memory location pointed by the Ri.
mathematically : ((Ri)) ← (A)
Bytes : 1
Cycles : 2
Encoding : 1111 0011
Opcodes : F2H-F3H
Flags affected : nil
Addressing mode : indirect addressing

22) Syntax : **MOVX A, @Ri**
description : move the contents external data memory location pointed by the Ri into the accumulator.
mathematically : (A) ←((Ri))
Bytes : 1
Cycles : 2
Encoding : 1111 0011
Opcodes : E2H-E3H
Flags affected : nil
Addressing mode : indirect addressing

23) Syntax : **MOVC A, @A+DPTR**
description : move the contents program (code) memory into the accumulator .the program(code)memory is formed by adding contents of the base register DPTR and the contents of the accumulator .DPTR points to the program address and the contents of the accumulator is treated as the offset.
mathematically : (A) ←((DPTR)+(A))
Bytes : 1
Cycles : 2
Encoding : 1001 0011
Opcodes : 93H
Flags affected : nil
Addressing mode : index addressing

24) Syntax : **MOVC A, @A+PC**

description : move the contents program (code) memory into the accumulator .the program(code)memory is formed by adding contents of the base register PC and the contents of the accumulator.PC points to the program address and the contents of the accumulator is treated as the offset.

mathematically : (A) ← ((PC)+(A))
Bytes : 1
Cycles : 2
Encoding : 1000 0011
Opcodes : 83H
Flags affected : nil
Addressing mode : index addressing

25) Syntax : **PUSH ,direct**

description : SP the stack pointer is incremented by 1. move or save the contnts of the internal data memory onto the stack.

mathematically : (SP) ← (SP)+1 ; ((SP)) ← (direct)
Bytes : 2
Cycles : 2
Encoding : 1100 0000 ,direct address
Opcodes : COH, direct address
Flags affected : nil
Addressing mode : register addressing

26) Syntax : **POP ,direct**

description : The contents of the top of the SP are moved to popped onto the internal data memory location specified in the instruction and the SP ,the stack pointer is decremented by 1 , after the instruction .

mathematically : (direct) ← ((SP)) ; (SP) ← (SP)-1
Bytes : 2
Cycles : 2
Encoding : 1101 0000 ,direct address
Opcodes : DOH, direct address
Flags affected : nil
Addressing mode : register addressing

27) Syntax : **XCH A, Rn**

description : exchange the register Rn contents with the accumulator .

mathematically : (A) ← (Rn) ;
Bytes : 1
Cycles : 1
Encoding : 1100 1rrr
Opcodes : C8H-CFH

Flags affected : nil
Addressing mode : register addressing

28) Syntax : **XCH A, direct**
description : exchange the contents of the internal data memory with the accumulator
mathematically : (A) ←→ (direct)
Bytes : 2
Cycles : 1
Encoding : 1110 0101,direct address byte
Opcodes : C5 ,direct addres byte
Flags affected : nil
Addressing mode : direct memory addressing

29) Syntax : **XCH A, @Ri**
description : exchange the contents of the internal data memory indirectly addressed by the Ri .
mathematically : (A) ←→ ((Ri))
Bytes : 1
Cycles : 1
Encoding : 1100 0111
Opcodes : C6-C7H,
Flags affected : nil
Addressing mode : indirect register addressing

30) Syntax : **XCHD A, @Ri**
description : exchange the low order nibble of the internal data memory indirectly addressed by the Ri with the low order nibble of the accumulator.
mathematically : (A3-0) ←→ ((Ri) 3-0)
Bytes : 1
Cycles : 1
Encoding : 1101 0111
Opcodes : D6-D7H,
Flags affected : nil
Addressing mode : indirect register addressing

ARITHMETIC INSTRUCTIONS

31) Syntax : **ADD A, Rn**
description : the register contents and the contents of the accumulator are added and returned to the accumulator
mathematically : (A) ← (Rn)+(A)
Bytes : 1
Cycles : 1
Encoding : 0010 1rrr
Opcodes : 28H-2FH
Flags affected : all flags are affected
Addressing mode : register addressing

32) Syntax : **ADD A, direct**
description : the contents of the internal data memory and the contents of the accumulator are added and returned to the accumulator
mathematically : (A) ← (direct)+(A)
Bytes : 2
Cycles : 1
Encoding : 0010 0101,direct address
Opcodes : 25H ,direct address
Flags affected : all flags are affected
Addressing mode : direct addressing

33) Syntax : **ADD A, @Ri**
description : add the contents of the internal data memory indirectly addressed by the Ri to the accumulator and the sum is returned to the accumulator.
mathematically : (A) ← ((Ri)+(A)
Bytes : 1
Cycles : 1
Encoding : 0010 0111
Opcodes : 26H –27H
Flags affected : all flags are affected
Addressing mode : register indirect addressing

34) Syntax : **ADD A, #data8**
description : the immediate data byte(data8) specified in the instruction and the contents of the accumulator are added and the sum is returned to the accumulator.
mathematically : (A) ← data8+(A)
Bytes : 2
Cycles : 1
Encoding : 0010 0100,immediate byte
Opcodes : 24H ,immediate byte
Flags affected : all flags are affected
Addressing mode : immediate addressing

35) Syntax : **ADDC A, Rn**
Description : the register contents and the contents of the accumulator along with the carry status are added and returned to the accumulator.
mathematically : (A) ← data8+(A) +(C)
Bytes : 1
Cycles : 1
Encoding : 0011 1rrr,
Opcodes : 38H-3FH
Flags affected : all flags are affected
Addressing mode : register addressing

36) Syntax : **ADDC A, direct**

Description : the contents of the internal data memory contents and the contents of the accumulator along with the carry status are added and returned to the accumulator.
mathematically : (A) ←—— direct + (A) +(C)
Bytes : 2
Cycles : 1
Encoding : 0011 0101,direct address
Opcodes : 35H
Flags affected : all flags are affected
Addressing mode : direct addressing

37) Syntax : **ADDC A, @Ri**
description : add the contents of the internal data memory indirectly addressed by the Ri to the accumulator along with the status of carry and the sum is returned to the accumulator.
mathematically : (A) ←—— ((Ri) + (A) + (C)
Bytes : 1
Cycles : 1
Encoding : 0011 0111
Opcodes : 36H –37H
Flags affected : all flags are affected
Addressing mode : register indirect addressing

38) Syntax : **ADDC A, #data8**
description : the immediate data byte(data8) specified in the instruction and the contents of the accumulator are added along with the status of carry and the sum is returned to the accumulator.
mathematically : (A) ←—— data8 + (A) + (C)
Bytes : 2
Cycles : 1
Encoding : 0011 0100,immediate byte
Opcodes : 34H ,immediate byte
Flags affected : all flags are affected
Addressing mode : immediate addressing

39) Syntax : **SUBB A, Rn**
description : the register contents and the contents of the accumulator are added and subtracted from the contents of the accumulatorandthe difference is returned to the accumulator.
mathematically : (A) ←—— (A) –{(Rn) + c }
Bytes : 1
Cycles : 1
Encoding : 1001 1rrr
Opcodes : 98H-9FH
Flags affected : all flags are affected
Addressing mode : register addressing

40) Syntax : **SUBB A, direct**
description : the contents of the internal data memory specified in the instruction and the carry status are added and subtracted from the contents of the accumulator and the differnce is returned to the accumulator
mathematically : (A) ← (A)-{(direct) + C}
Bytes : 2
Cycles : 1
Encoding : 1001 0101,direct address
Opcodes : 95H ,direct address
Flags affected : all flags are affected
Addressing mode : direct addressing

41) Syntax : **SUBB A, @Ri**
description : the contents of the internal data memory indirectly addressed by the Ri and the carry status are added and subtracted from the contents of the accumulator and the difference is returned to the accumulator.
mathematically : (A) ← (A)-{((Ri)) + C}
Bytes : 1
Cycles : 1
Encoding : 1001 0111
Opcodes : 96H –97H
Flags affected : all flags are affected
Addressing mode : register indirect addressing

42) Syntax : **SUBB A, #data8**
description : the immediate data byte(data8) specified in the instruction and the carry status are added and subtracted from the contents of the accumulator and the difference is returned to the accumulator.
mathematically : (A) ← (A)-(data 8 + C)
Bytes : 2
Cycles : 1
Encoding : 1001 0100,immediate byte
Opcodes : 94H ,immediate byte
Flags affected : all flags are affected
Addressing mode : immediate addressing

43) Syntax : **INC A**
description : the contents of the accumulator is incremented by 1
mathematically : (A) ← (A) + 1
Bytes : 1
Cycles : 1
Encoding : 0000 0100

Opcodes : 04H
Flags affected : nil
Addressing mode : register addressing

44) Syntax : **INC Rn**
description : the contents of the register is incremented by 1
mathematically : (Rn) ← (Rn) + 1
Bytes : 1
Cycles : 1
Encoding : 0000 1rrr
Opcodes : 08-0FH
Flags affected : nil
Addressing mode : register addressing

45) Syntax : **INC direct**
description : the contents of the internal data memory are incremented by 1
mathematically : (direct) ← (direct) + 1
Bytes : 2
Cycles : 1
Encoding : 0000 0101,direct byte
Opcodes : 05H,direct byte
Flags affected : nil
Addressing mode : direct addressing

46) Syntax : **INC @ Ri**
description : the contents of the internal data memory addressed indirectly by register Ri is incremented by 1
mathematically : ((Ri)) ← ((Ri)) + 1
Bytes : 1
Cycles : 1
Encoding : 0000 0111
Opcodes : 06-07H
Flags affected : nil
Addressing mode : register indirect addressing

47) Syntax : **DEC A**
description : the contents of the accumulator is decremented by 1
mathematically : (A) ← (A) - 1
Bytes : 1
Cycles : 1
Encoding : 0001 0100
Opcodes : 14H
Flags affected : nil
Addressing mode : register addressing

48) Syntax : **DEC Rn**
description : the contents of the register is decremented by 1
mathematically : (Rn) ← (Rn) - 1
Bytes : 1
Cycles : 1
Encoding : 0001 1rrr
Opcodes : 18-1FH
Flags affected : nil
Addressing mode: register addressing

49) Syntax : **DEC direct**
description : the contents of the internal data memory are decremented by 1
mathematically : direct) ← (direct) - 1
Bytes : 2
Cycles : 1
Encoding : 0001 0101,direct byte
Opcodes : 15H,direct byte
Flags affected : nil
Addressing mode : direct addressing

50) Syntax : **DEC @ Ri**
description : the contents of the internal data memory addressed indirectly
by register Ri is decremented by 1
mathematically : ((Ri)) ← ((Ri)) - 1
Bytes : 1
Cycles : 1
Encoding : 0001 0111
Opcodes : 16-17H
Flags affected : nil
Addressing mode : register indirect addressing

51) Syntax : INC DPTR
description : the contents of the 16 bit pointer DPTR is incremented by 1 mathematically
: (DPTR) 16 (DPTR) ← 1
Bytes : 1
Cycles : 2
Encoding : 1010 0011
Opcodes : A3H
Flags affected : nil
Addressing mode : register addressing

52) Syntax : **MUL AB**

description : this is an unsigned 8 bit by 8 bit multiplication instruction.The contents of the accumulator and the SFR B are multiplied and the product is returned to B(MSB) and A (LSB)
Mathematically : (B)(A) ← (B) * (A)
Bytes : 1
Cycles : 4
Encoding : 1010 0100
Opcodes : A4H
Flags affected : carry is cleared after the instruction,O & P are affected
Addressing mode : register addressing

53) Syntax : **DIV AB**
description : this is an unsigned 8 bit by 8 bit division instruction.The contents of the accumulator is the dividend and the content of SFR B is divisor d and the quotient is returned to A and the SFR B contains remainder
Mathematically : (A) ← (A) / (B),(B) ← (A) MOD (B)
Bytes : 1
Cycles : 4
Encoding : 1000 0100
Opcodes : 84H
Flags affected : C & O are cleared.O will be set if the divisor is 00H
Addressing mode : register addressing

54) Syntax : **DAA AB**
description : if the 2 BCD operands are added through ADD or ADDC instructions,the sum in the accumulator may not be a BCD sum. With this instruction after the ADD or ADDC instructions the sum is corrected to BCD value
Mathematically : (A) ← (A) + 06H if A3:0 is > 9 or AC=1 and
(A) ← (A) + 60H if A7:4 is > 9 or C=1
Bytes : 1
Cycles : 1
Encoding : 1101 0100
Opcodes : D4H
Flags affected : all flags are affected
Addressing mode : register addressing

LOGIC INSTRUCTIONS

55) Syntax : **ANL A,Rn**
description : logically AND the contents of the accumulator and the contents of the register Rn and the result is returned to the accumulator
Mathematically : (A) ← (R) ^ (A)
Bytes : 1
Cycles : 1
Encoding : 0101 1rrr
Opcodes : 58H – 5FH

Addressing mode : register addressing

56) Syntax : **ANL A,direct**
description : logically AND the contents of the accumulator and the contents of the internal data memory byte and the result is returned to the accumulator
Mathematically :(A) ←—— (direct) ^ (A)
Bytes : 2
Cycles : 1
Encoding : 0101 0101,direct byte
Opcodes : 55H,direct byte
Flags affected : only parity is affected
Addressing mode : direct addressing

57) Syntax : **ANL A ,@ Ri**
description : logically AND the contents of the accumulator and the contents of the internal data memory indirectly addressed by the Ri and the result is returned to the accumulator
Mathematically : (A) ←—— ((Ri)) ^ (A)
Bytes : 1
Cycles : 1
Encoding : 0101 0111
Opcodes : 56H – 57H
Flags affected : only parity is affected
Addressing mode : register indirect addressing

58) Syntax : **ANL A,#data 8**
description : logically AND the contents of the accumulator and the immediate data byte and the result is returned to the accumulator
Mathematically : (A) ←—— data 8 ^ (A)
Bytes : 2
Cycles : 1
Encoding : 0101 0100,immediate byte
Opcodes : 54H,immediate data byte(data 8)
Flags affected : only parity is affected
Addressing mode : immediate addressing

59) Syntax : **ANL direct,A**
description : logically AND the contents of the accumulator and the contents of the internal data memory byte and the result is returned to the accumulator
Mathematically : (direct) ←——(direct) ^ (A)

Bytes : 2
Cycles : 1
Encoding : 0101 0010,direct byte
Opcodes : 52H,direct byte
Flags affected : only parity is affected
Addressing mode : direct addressing

60) Syntax : **ANL direct,#data 8**
description : logically AND the contents of the internal data memory and the immediate data byte and the result is returned to the internal data memory
Mathematically :(direct) ← data 8 ^ (direct)
Bytes : 2
Cycles : 1
Encoding : 0101 0011,immediate byte
Opcodes : 53H,immediate data byte(data 8)
Flags affected : only parity is affected
Addressing mode : immediate addressing

61) Syntax : **ORL A,Rn**
description : logically OR the contents of the accumulator and the contents of the register Rn and the result is returned to the accumulator
Mathematically : (A) ← (Rn) V (A)
Bytes : 1
Cycles : 1
Encoding : 0100 1rrr
Opcodes : 48H – 4FH
Flags affected : only parity is affected
Addressing mode : register addressing

62) Syntax : **ORL A,direct**
description : logically OR the contents of the accumulator and the contents of the internal data memory byte and the result is returned to the accumulator
Mathematically : (A) ← (direct) V (A)
Bytes : 2
Cycles : 1
Encoding : 0100 0101,direct byte
Opcodes : 45H,direct byte
Flags affected : only parity is affected
Addressing mode : direct addressing

63) Syntax : **ORL A ,@ Ri**

description : logically OR the contents of the accumulator and the contents of the internal data memory indirectly addressed by the Ri and the result is returned to the accumulator
Mathematically : (A) ← ((Ri)) V (A)
Bytes : 1
Cycles : 1
Encoding : 0100 0111
Opcodes : 46H – 47H
Flags affected : only parity is affected
Addressing mode : register indirect addressing

64) Syntax : **ORL A,#data 8**
description : logically OR the contents of the accumulator and
the immediate data byte and the result is returned to the accumulator
Mathematically :(A) ← data 8 V (A)
Bytes : 2
Cycles :1
Encoding : 0100 0100,immediate byte
Opcodes : 44H,immediate data byte(data 8)
Flags affected : only parity is affected
Addressing mode : immediate addressing

65) Syntax : **ORL direct,A**
description : logically OR the contents of the accumulator and
the contents of the internal data memory byte and the result is returned to the accumulator
Mathematically :(direct) ← (direct) V (A)
Bytes : 2
Cycles : 1
Encoding : 0100 0010,direct byte
Opcodes : 42H,direct byte
Flags affected : only parity is affected
Addressing mode : direct addressing

66) Syntax : **ORL direct,#data 8**
description : logically OR the contents of the internal data memory and
the immediate data byte and the result is returned to the internal data memory
Mathematically :(direct) ← data 8 V (direct)
Bytes : 2
Cycles : 1
Encoding : 0100 0011,immediate byte
Opcodes : 43H,immediate data byte(data 8)
Flags affected : only parity is affected
Addressing mode : immediate addressing

67) Syntax : **XRL A,Rn**

description : logically exclusive OR the contents of the accumulator and the contents of the register Rn and the result is returned to the accumulator

Mathematically : (A) ← (Rn) V (A)

Bytes : 1

Cycles : 1

Encoding : 0110 1rrr

Opcodes : 68H – 6FH

Flags affected : only parity is affected

Addressing mode : register addressing

68) Syntax : **XRL A,direct**

description : logically exclusive OR the contents of the accumulator and the contents of the internal data memory byte and the result is returned to the accumulator

Mathematically : (A) ← (direct) V (A)

Bytes : 2

Cycles : 1

Encoding : 0110 0101,direct byte

Opcodes : 65H,direct byte

Flags affected : only parity is affected

Addressing mode : direct addressing

69) Syntax : **XRL A ,@ Ri**

description : logically exclusive OR the contents of the accumulator and the contents of the internal data memory indirectly addressed by the Ri and the result is returned to the accumulator

Mathematically :(A) ← ((Ri)) V (A)

Bytes : 1

Cycles : 1

Encoding : 0110 0111

Opcodes : 66H –67H

Flags affected : only parity is affected

Addressing mode : register indirect addressing

70) Syntax : **XRL A,#data 8**

description : logically exclusive OR the contents of the accumulator and the immediate data byte and the result is returned to the accumulator

Mathematically :(A) ← data 8 V (A)

Bytes : 2

Cycles : 1

Encoding : 0110 0100,immediate byte

Opcodes : 64H,immediate data byte(data 8)

Flags affected : only parity is affected

Addressing mode : immediate addressing

71) Syntax : **XRL direct,A**
description : logically exclusive OR the contents of the accumulator and the contents of the internal data memory byte and the result is returned to the accumulator
Mathematically :(direct) ←(direct) V (A)
Bytes : 2
Cycles : 1
Encoding : 0110 0010,direct byte
Opcodes : 62H,direct byte
Flags affected : only parity is affected
Addressing mode : direct addressing

72) Syntax : **XRL direct,#data 8**
description : logically exclusive OR the contents of the internal data memory and the immediate data byte and the result is returned to the internal data memory
Mathematically : (direct) ← data 8 V (direct)
Bytes : 2
Cycles : 1
Encoding : 0110 0011,immediate byte
Opcodes : 63H,immediate data byte(data 8)
Flags affected : only parity is affected
Addressing mode : immediate addressing

73) Syntax : **CLR A**
description : clear the accumulator
Mathematically : (A) ← 0
Bytes : 1
Cycles : 1
Encoding : 1110 0001
Opcodes : E4H
Flags affected : nil
Addressing mode : register addressing

74) Syntax : **CPL A**
description : complement the accumulator
Mathematically : (A) ← NOT A
Bytes : 1
Cycles : 1
Encoding : 1111 0100
Opcodes : F4H
Flags affected : nil
Addressing mode : register addressing

75) Syntax : **RL A**
description : rotate the accumulator left once
Mathematically : (A) ← rotate left the contents of accumulator
(An+1) ← (An) n=0-6;(A0) ← (A7)
Bytes : 1
Cycles : 1
Encoding : 0010 0011
Opcodes : 23H
Flags affected : nil
Addressing mode : register addressing

76) Syntax : **RLC A**
description : rotate the accumulator left once,through carry
Mathematically : (A) ← rotate left the contents of accumulator through carry
(An+1) ← (An) n=0-6;(A0) ← (carry);
(carry) ← (A7)
Bytes : 1
Cycles : 1
Encoding : 0011 0011
Opcodes : 33H
Flags affected : carry is affected
Addressing mode : register addressing

77) Syntax : **RR A**
description : rotate the accumulator right once
Mathematically : (A) ← rotate right the contents of accumulator
(An) ← (An+1) n=0-6; (A7) ← (A0)
Bytes : 1
Cycles : 1
Encoding : 0000 0011
Opcodes : 03H
Flags affected : nil
Addressing mode : register addressing

78) Syntax : **RRC A**
description : rotate the accumulator right once,through carry
Mathematically : (A) ← rotate right the contents of accumulator through carry
(An) ← (An+1) n=0-6;(A7) ← carry;
carry ← (A0)
Bytes : 1
Cycles : 1
Encoding : 0001 0011
Opcodes : 13H
Flags affected : carry is affected
Addressing mode : register addressing

79) Syntax : **SWAP A**

description : interchange the least significant nibble with the most significant nibble of the accumulator

Mathematically : (A) ← interchange the nibbles of the accumulator

(A3:0) ↔ (A7:4)

Bytes : 1

Cycles : 1

Encoding : 1100 0100

Opcodes : C4H

Flags affected : nil

Addressing mode : register addressing

BIT LOGICAL INSTRUCTIONS

80) Syntax : **ANL C,bit**

description : logically AND the bit (whose address is specified in the instruction)and the carry and the result is returned to the carry

Mathematically :(C) ← (direct bit) ^ (C)

Bytes : 2

Cycles : 2

Encoding : 1000 0010,direct bit

Opcodes : 82H,direct bit

Flags affected : carry is affected

Addressing mode : direct bit addressing

81) Syntax : **ANL C,/ bit**

description : logically AND the complement of bit (whose address is specified in the instruction)and the carry and the result is returned to the carry

Mathematically :(C) ← NOT (direct bit) ^ (C)

Bytes : 2

Cycles : 2

Encoding : 1011 0000,direct bit

Opcodes : B0H,direct bit

Flags affected : carry is affected

Addressing mode : direct bit addressing

82) Syntax : **ORL C,bit**

description : logically OR the bit (whose address is specified in the instruction)and the carry and the result is returned to the carry

Mathematically : (C) ← (direct bit) V (C)

Bytes : 2

Cycles : 2

Encoding : 0111 0010,direct bit

Opcodes : 72H,direct bit

Flags affected : carry is affected
Addressing mode : direct bit addressing

83) Syntax : **ORL C, / bit**
description : logically OR thecomplement of the bit (whose address is specified in the instruction)and the carry and the result is returned to the carry
Mathematically : (C) ← NOT (direct bit) V (C)
Bytes : 2
Cycles : 2
Encoding : 1010 0000,direct bit
Opcodes : A0H,direct bit
Flags affected : carry is affected
Addressing mode : direct bit addressing

84) Syntax : **CLR C**
description : clear the carry
Mathematically : (C) ← 0
Bytes : 1
Cycles : 1
Encoding : 1100 0011
Opcodes : C3H
Flags affected : C
Addressing mode : register addressing

85) Syntax : **CLR bit**
Bytes : 2
Cycles : 1
Encoding : 1100 0010,direct bit
Opcodes : C2H,direct bit
Flags affected : nil
Addressing mode : direct bit addressing

86) Syntax : **SETB C**
description : set the carry bit
Mathematically :(C) ← 1
Bytes : 1
Cycles : 1
Encoding : 1101 0011
Opcodes : D3H
Flags affected : carry is affected

87) Syntax : **SETB bit**
description : set the bit (whose address is specified in the instruction)
Mathematically : (bit) ← 1
Bytes : 2
Cycles : 1

Bytes : 3
Cycles : 2
Encoding : 0000 0010
Opcodes : 02H
Flags affected : nil
Addressing mode : direct addressing

92) Syntax : **SJMP Reladdr8**
description : after this unconditional branch instruction PC jumps to the location labeled as reladdr8,which is within 127/129 locations
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 1000 0000
Opcodes : 80H
Flags affected : nil
Addressing mode : relative addressing

93) Syntax : JMP @A+DPTR
description : after this unconditional indirect branch instruction PC jumps to the location whose address is at (A) + (DPTR)
Mathematically : (PC) ← (A) + (DPTR)
Bytes : 1
Cycles : 2
Encoding : 0111 0011
Opcodes : 73H
Flags affected : nil
Addressing mode : indirect addressing

94) Syntax : **JZ Reladdr8**
description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction if all the bits of accumulator are 0
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0110 0000
Opcodes : 60H
Flags affected : nil
Addressing mode : relative addressing

95) Syntax : **JNZ Reladdr8**

description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction if any of the bits of accumulator are nonzero
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0111 0000
Opcodes : 70H
Flags affected : nil
Addressing mode : relative addressing

96) Syntax : **JC Reladdr8**
description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction, if CY= 1
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0100 0000
Opcodes : 40H
Flags affected : nil
Addressing mode : relative addressing

97) Syntax : **JNC Reladdr8**
description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction, if CY= 0
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0101 0000
Opcodes : 50H
Flags affected : nil
Addressing mode : relative addressing

98) Syntax : **JB Bit addr, Reladdr8**
description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction, if the bit is set.
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0010 0000
Opcodes : 20H
Flags affected : nil
Addressing mode : relative addressing

99) Syntax : **JNB Bit addr, Reladdr8**
description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction, if the bit is not set.
Mathematically : (PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0011 0000
Opcodes : 30H
Flags affected : nil
Addressing mode : relative addressing

100) Syntax : **JBC Bitaddr, Reladdr8**
description : after this conditional relative branch instruction PC jumps relatively to the address location mentioned in the instruction, if the bit is setAfter which the bit is cleared
Mathematically :(PC) ← reladdr8
Bytes : 2
Cycles : 2
Encoding : 0001 0000
Opcodes : 10H
Flags affected : C is cleared after instruction
Addressing mode : relative addressing

101) Syntax : **DJNZ Rn, Reladdr8**
description : after this conditional relative and iterative branch instruction PC jumps relatively to the address location mentioned in the instruction,
Mathematically : Rn ← Rn-1;
if Rn is not zero,then (PC) ← reladdr8,
else PC =PC + 2
Bytes : 3
Cycles : 2
Encoding : 1101 1bbb
Opcodes : D8-DFH
Flags affected : z is affected and Rn register becomes zero
Addressing mode : iterative relative addressing

102) Syntax : **DJNZ direct byte, Reladdr8**
description : after this conditional, relative and iterative branch instruction PC jumps relatively to the address location mentioned in the instruction,
Mathematically : (direct byte) ← (direct byte) - 1
if direct byte is not zero,then (PC) ← reladdr8
else PC =PC + 2
Bytes : 3
Cycles : 2
Encoding : 1101 0101
Opcodes : D5H
Flags affected : z is affected and direct byte becomes zero

103) Syntax : **CJNE A,direct byte, Reladdr8**
description : If the contents of accumulator with that of the direct byte are not equal,then PC jumps relatively to the address location mentioned in the instruction
Mathematically :
PC ← reladdr8 , if the contents of accumulator and the ontents of the direct byte is not equal
then PC ← reladdr8
else PC =PC + 2

Bytes :3
Cycles :2
Encoding :1011 0101
Opcodes :B5H
Flags affected :nil
Addressing mode : conditional and relative addressing

104) Syntax : **CJNE A,#data8, Reladdr8**
description : If the contents of accumulator with that of the immediate byte are not equal,then PC jumps relatively to the address location mentioned in the instruction
Mathematically :
PC ← reladdr8 , if the contents of accumulator and the contents of the immediatebyte are not equal
then PC ← reladdr8
else PC =PC + 2

Bytes :3
Cycles :2
Encoding :1011 0100
Opcodes :B4H
Flags affected :nil
Addressing mode : conditional and relative addressing

105) Syntax : **CJNE Rn,#data8, Reladdr8**
description : If the contents of Rn with that of the immediate byte are not equal,then PC jumps relatively to the address location mentioned in the instruction

Mathematically :
PC ← reladdr8 , if the contents of Rn and the contents of the immediatebyte are not equal
then PC ← reladdr8
else PC =PC + 2

Bytes :3
Cycles :2
Encoding :1011 1bbb
Opcodes :B8-BFH
Flags affected :nil
Addressing mode : conditional and relative addressing

106) Syntax : **CJNE @Ri,#data8, Reladdr8**

description : If the contents of memory location pointed by Ri with that of the immediate byte are not equal,then PC jumps relatively to the address location mentioned in the instruction

Mathematically :

PC ← reladdr8 , if the contents of memory location pointed by Ri and immediate byte are not equal

then PC ← reladdr8

else PC =PC + 2

Bytes : 3
Cycles : 2
Encoding : 1011 011b
Opcodes : B6-B7H
Flags affected : nil
Addressing mode : conditional and relative addressing

107) Syntax : **ACALL Addr11**

description : after this unconditional SUBROUTINE branch instruction PC jumps to the location labeled as Addr11,which is within 2K locations

Mathematically : SP ← SP + 2;((SP)) ← (PC);
(PC) ← Addr11

Bytes : 2
Cycles : 2
Encoding : a10 a9 a8 1 0 0 0 1 a7 a6 a5 a4 a3 a2 a1 a0
Opcodes : 11H, depends on the 2K page addresses
Flags affected : nil
Addressing mode : direct addressing

108) Syntax : **LCALL Addr16**

description : after this unconditional branch instruction PC jumps to the location labeled as Addr16,which is within 64K locations

Mathematically : SP ← SP + 2;((SP)) ← (PC);
(PC) ← Addr16

Bytes : 3
Cycles : 2
Encoding : 0001 0010
Opcodes : 12H
Flags affected : nil
Addressing mode : direct addressing

109) Syntax : **RET**

description : after this unconditional branch instruction PC jumps back to the address stored in the top of the stack.

Mathematically : PC ← (SP) ; SP ← SP - 2

Bytes : 1
Cycles : 2
Encoding : 0010 0010
Opcodes : 22H
Flags affected : nil
Addressing mode : direct addressing

110) Syntax : RETI
description : after this unconditional branch instruction PC jumps back to the address stored in the top of the stack and restores the interrupt logic to accept additional interrupts at the same priority level as the one just processed .this instruction is to be used in the interrupt service routines
Mathematically : PC ← (SP) ; SP ← SP - 2
Bytes : 1
Cycles : 2
Encoding : 0011 0010
Opcodes : 32H
Flags affected : nil
Addressing mode : direct addressing

MISCELLANEOUS INSTRUCTIONS

111) Syntax : NOP
description : It is a no operation instruction
Bytes : 1
Cycles : 1
Encoding : 0000 0000
Opcodes : 00H
Flags affected : nil