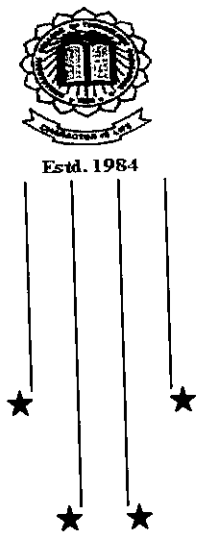
AUTOMATIC PETROLEUM PURITY INDICATOR



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UNDER THE GUIDANCE OF,

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2002 – 2003

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF BE DEGREE IN ELECTRICAL & ELECTRONICS ENGINEERING UNDER BHARATHIAR UNIVERSITY

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
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Estd. 1984

ISO 9001:2000

CERTIFICATE

This is to certify that the Project Report entitled

"AUTOMATIC PETROLEUM PURITY DETECTOR"

has been submitted by

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in partial fulfillment of the requirements for the award of the degree of Bachelor of Engineering in Electrical and Electronics branch of Bharathiar University, Coimbatore during the academic year 2002 - 2003

Project Guide

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20.3.2003

CONTENTS

I. ACKNOWLEDGEMENT

We are highly privileged to thank **Dr.K.K.PADMANABHAN, B.Sc.,(Engg).,M.Tech.,Ph.D.,** Principal, Kumaraguru college of Technology for allowing us to do this project.

We are highly indebted to **Prof.V.Duraiswamy** who encouraged us and kindly agreed to our request for using the various college facilities.

With deep sense of gratitude we thank our project guide Senior Lecturer **Mrs.Rani Thottungal,** whose valuable guidance and enthusiastic encouragement for the successful completion of this project.

We shall be failing in our duty if we do not thank all the department staffs , lab technicians and our friends for having encouraged us and supported us morally while doing the project

Finally we thank one and all who co-operated with us in bringing out this project successfully.

II. SYNOPSIS

" Microcontroller based petrol purity detector " as the title goes detects the percentage purity of petrol in different samples. The purity is detected based on capacitance of the fuel which according to our theory varies with addition of impurities. To determine capacitance we have adopted shcerings bridge circuit. The imbalance voltage across the bridge is the converted into digital value and serially transmitted to the PC. The PIC microcontroller is the controlling device for the whole set up. The output will give the percentage purity of the given sample.

The main intention behind developing this idea is to bring about an awareness among all vehicle users. They can definitely make out a very wide disparity in the amount they have been spending for their vehicle maintenance and what they will be spending in future on adopting this technology.

CHAPTER ONE
Fuel Properties

1. INTRODUCTION

Petroleum fuels are generally obtained from crude oil after various refining processes. The petroleum fuels which draw our concern are petrol and diesel which are generally used in automobiles. It is necessary for us to study their composition and as far as possible use them in their purest form.

1.1 COMPOSITION OF FUEL

The three main groups found in the fuel are:

1. Aromatics-organic compounds based on the benzene ring, a 6-carbon ring with 3 delocalized double bonds, e.g., benzene, toluene, xylene, etc.

2. Olefines-organic compounds which have double bonds. After combustion, one critical by-product is 1,3 - butadiene.

3. Oxygenates-organic compounds containing oxygen molecules such as methane, ethane or MTBE (methyl-tertiary-butyl ether).

Otherwise petrol can be generally differentiated as leaded and unleaded petrol. in regular unleaded petrol, the total aromatic content was 27.7%, and

benzene level at 2.0%. But, for leaded petrol, the total aromatic content was 29.2%, and the benzene level at 2.1%.These compounds may give rise to carcinogens.Hence it is necessary to check the pollutant levels.

Here petroleum fuel is our main concern hence we'll make a detailed study of petrol.

1.2 PROPERTIES OF PETROL

1.2.1 CONDUCTIVITY

Petrol generally has very low electrical conductivity. . Insufficient conductivity is a potential safety risk because it can lead to a build-up of static charge during bulk transfer of fuel (filling bulk storage tanks and road tankers).

1.2.2 DENSITY

Variations in fuel density can result in variations in the energy content of the fuel injected into an engine. Consequently, engine power,

emissions and fuel consumption may be affected. A narrower density range allows more efficient fuel consumption, better engine performance and reduced emissions

1.2.3 VISCOSITY:

Viscosity is a measure of the fuel's resistance to flow. High viscosity can reduce fuel flow rates resulting in insufficient fuel flow. Low viscosity will increase leakage from fuel pumps, can increase engine wear and may result in hot starting difficulties.

1.2.4 COLD FLOW PROPERTIES

Cold flow properties influence the way vehicles start and operate in cold weather.Especially diesel which crystallizes under cold conditions and the wax crystals block fuel filters and interrupt fuel supply.

1.2.5 SULPHUR LEVEL

Sulphur occurs naturally in crude oils and must be removed to an acceptable level during the refining process. Sulphur in the fuel contributes to

the formation of particulate matter, a component of engine exhaust that is linked to health problems. Sulphur also degrades the performance of vehicle emissions-control equipment.

1.2.6 FLASH POINT

Flash point is the lowest temperature at which enough vapour has combined in the air above a liquid that it will ignite when exposed to a flame. Flash point is a measure of both volatility and flammability. It is important primarily from the standpoint of safe handling and storage of fuel. The flash point is used to classify flammable liquids and therefore affects the design of equipment and the control of potential ignition sources.

1.2.7 OXIDATION STABILITY

If excess oxidation occurs it results in the formation of residues and gums,affecting whether engines run reliably and effectively and give years of good service.

1.2.8 VOLATILITY AND DISTILLATION PARAMETERS

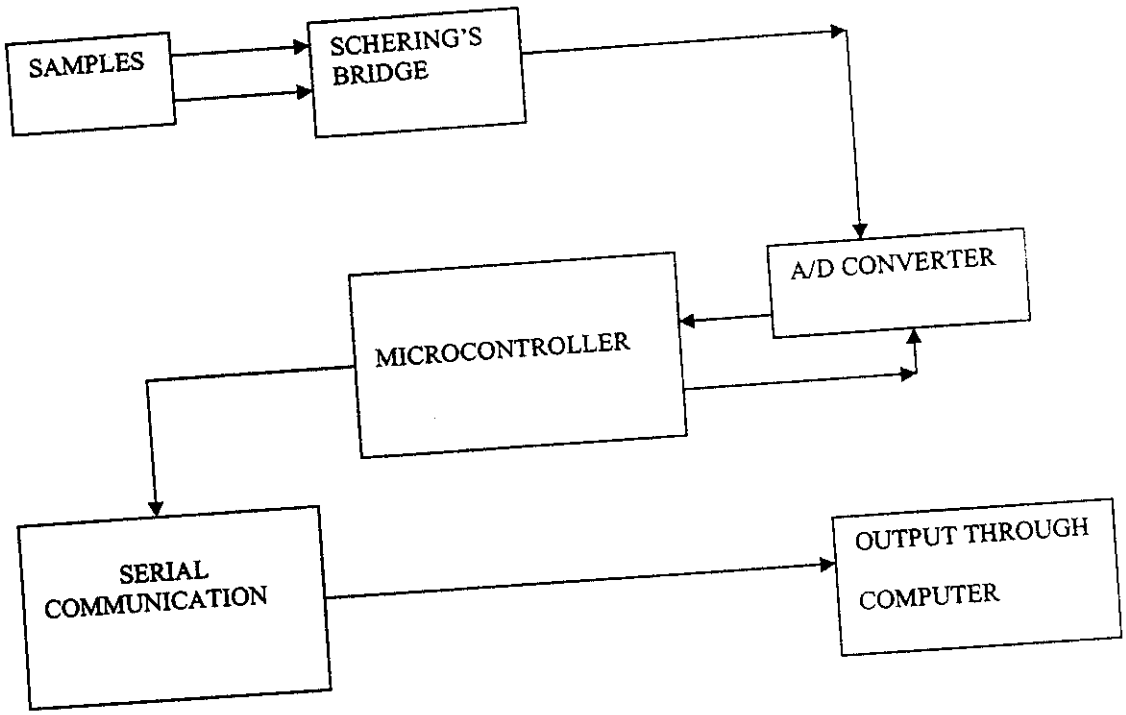
Volatility is an important property to control

It affects:

1. engine performance
2. cold weather starting
3. Evaporative and exhaust emissive

The distillation curve (temperature versus percent volume evaporated) characterises the volatility of a fuel. Distillation is related to density, because heavier fuel components tend to evaporate at high temperatures. Heavy components have more potential for incomplete combustion than lighter components and may increase smoke or soot emissions.Changes to distillation will reduce carbon monoxide , hydrocarbon and particulate emissions.

CHAPTER TWO
BLOCK DIAGRAM


SAMPLES
SCHERING'S BRIDGE
A/D CONVERTER
MICROCONTROLLER
SERIAL COMMUNICATION
OUTPUT THROUGH COMPUTER

CHAPTER THREE
CAPACITANCE MEASUREMENT USING SCHERING BRIDGE

3. BRIDGES:

There are a variety of bridges used for measurement of capacitances.Certain commonly used bridges are as follows

* De Sauty,s bridge:

This bridge is the simplest method for the comparison of two capacitance values.In this bridge it is impossible to obtain balance if both the capacitors are not free from dielectric losses.

* Scherings bridge:

This bridge is very well suited for small value of capacitances and it is generally supplied from normal 50 hz frequency and normal voltage supply. This bridge has been selected for this project to measure the capacitance value of the petroleum fuels whose permittivity is very low.The advantage of this bridge being the possibility of extension of the system for higher voltages and also higher frequencies as the capacitance value increases with frequency.

3.1 SCHERINGS BRIDGE:

3.1.1 GENERAL FEATURES:

The Scherings bridge is widely used for capacitor and dissipation factor measurements. In fact Scherings bridge is one of the most important AC bridges. It is extensively being used for the measurement of capacitances in general, and in particular in the measurement of properties of insulators, condenser, bushings, insulating oil, and other insulating materials. This bridge is particularly used for small capacitances, and is Then usually supplied from a high voltage or high frequency source. The measurements done on small capacitances suffer from many disadvantages if carried out at low voltages. High voltage scherings bridge is certainly preferable for such measurements.

Scherings bridge is very useful in the measurement of relative permittivity of dielectric materials. The determination of the relative permittivity involves measurement of capacitance of small capacitor, with the specimen as dielectric. The capacitor with specimen as dielectric is formed by using either a parallel plate or a concentric cylinder configuration for the electrodes. Guard circuits are used in order to make the plate area definite.

Many different techniques are used , both in type of specimen capacitor used and in the measuring circuit. The normal arrangement for solid materials is to use a disc specimen with metal electrodes. The electrodes may consist of thin metal foil attached to the specimen by petroleum jelly or thin films of silver or aluminium applied by evaporation (both these arrangements normally have solid metal backing electrodes), or mercury. Mercury electrodes are obtained by floating or supporting the specimen on the surface of the mercury pool , the upper electrodes consisting of smaller mercury pool held in place by a metal containing ring. Liquid specimens fill the space between the concentric cylindrical electrodes of a test cell.

3.1.2 CONSTRUCTION:

The figure gives the connections of scherings bridge.The capacitors C1and C2 are standard capacitors with fixed resistance values connected in parallel.Of the other two arms one arm has got a single value of capacitance connected and the other arm has got a same value of capacitance connected in series with the sample whose capacitance is to be measured.The

bridge is balanced without the sample and then with the sample and the difference between of capacitances obtained in the variable arm gives the capacitance value of the sample.

In this context we have not determined the value of capacitance of petrol but have found out the imbalance voltage for different samples .***Thus theory has been implemented which proves that the capacitance of petrol varies with the addition of impurities.*** Thus these different imbalance voltages indicate the presence of impurities in the sample.although sophisticated techniques are not adopted we have maintained the success behind the theory.

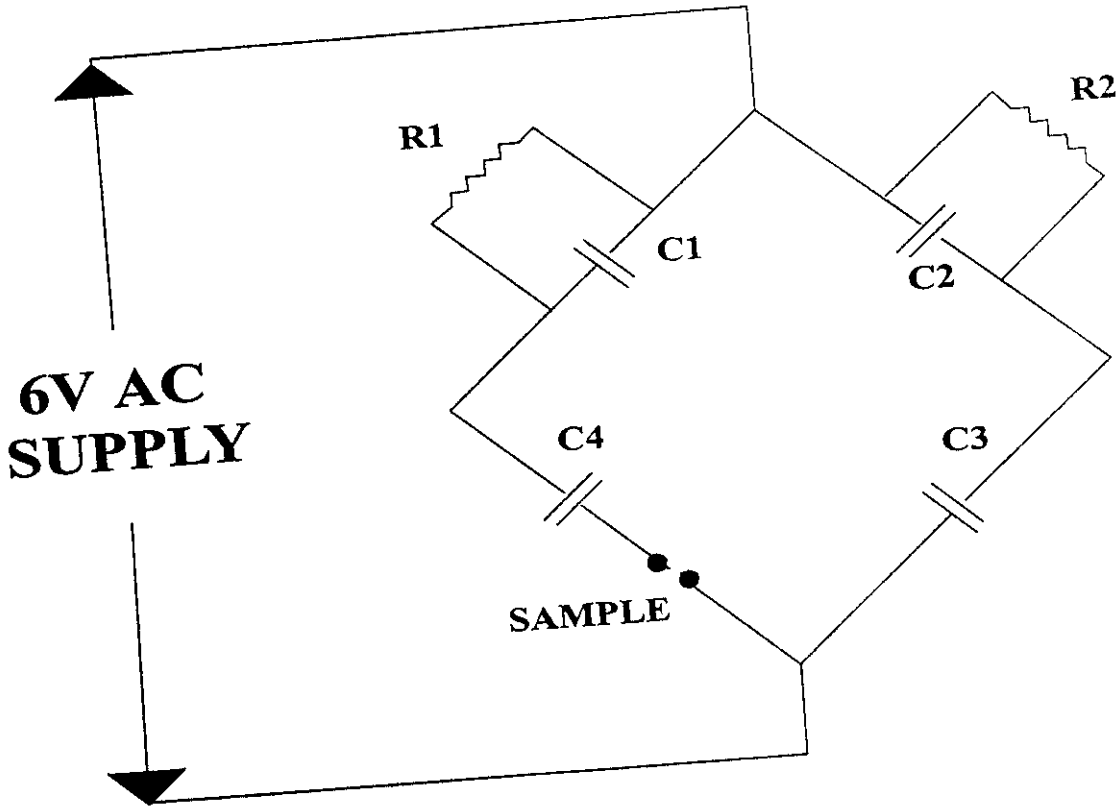
The relation between capacitance and voltage is as follows

$$C=Q/V \text{ Farads}$$

3.2 ADVANTAGES:

This method has got a very high current sensitivity and so it involves a very low power loss.

3.3 SCHERING'S BRIDGE CIRICUIT DIAGRAM:



Design values: R1=R2= 1KOHMS
C1=C2=C3=C4=47μF

3.4 CAPACITANCE BETWEEN TWO CONDUCTING PLATES:

Consider two equal conducting plates ,placed parallel to one another and at a distance D meters apart ,this being small compared with the dimensions of the plates,so that the fringing effect at the edges of the plates is given by the equation

$$\frac{\text{Density of the charge}}{\text{Permittivity of the dielectric}}$$

Then the Potential difference between the plates is

V=Integration (Q/(E*A))=(QD)/(EA)

Where

Q=charge in the plates

E=permittivity of the dielectric

D=Distance between the plates

A=Area of the plates

Thus

$$C=(E*A)/D$$

The relative Permittivity of petrol is between 1.8-2

4.1 GENERAL DESCRIPTION:

All PICmiro™ microcontrollers employ an advanced RISC architecture.PIC16F84 has enhanced core features, eight–level deep stack, and multiple internal and external interrupt sources. The instruction and data buses of the Harvard structure allow a 14 bit wide instruction word with a separate 8-bit wide databus. The two stage instruction pipeline allows all instruction s to execute in a single cycle, except for program branches,which require two cycles. A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set is used to achieve a very high performance level.

PIC16F84 microcontrollers typically achieve a 2:1 code compression and upto a 4:1 speed improvement (at 20 MHz)over other 8-bit microcontrollers in their class. It has upto 68 bytes of RAM ,64 bytes of data EEPROM,and 13 I/O pins . A timer/counter is also available.

The PIC family has special features to reduce external components thus reducing cost enhancing system reliability and reducing power consumption.

There are four oscillator options,of which the single Rc pin oscillator minimizes power consumption.

A highly reliable Watch Dog Timer with its own on chip RC oscillator provides protection against software lock-up.

The devices with Flash memory allow the same device to be used for prototyping and production.In-circuit reprogrammability allows the code to be updated without the device from being removed from the end application , where the device may not be easily accessible,but the prototypes may require code updates.

The PIC16F84 fits perfectly in applications ranging from high speed automotive and application motor control to low power remote sensors, electronic locks, security devices and smart cards. The Flash/EEPROM technology makes customization of application programs extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, high-performance , ease-of-use and I/O flexibility make the 16F84 very versatile even in areas where no microcontroller has been considered before. The serial in system programming feature offers flexibility of customizing the product after complete assembly and testing.This feature can be used to serialize a product,store calibration data or program the device with the current firmware

High performance RISC CPU features:

- Only 35 single word instructions to learn
- All instructions single cycle except for program branches which are two cycle
- Operating speed-DC-10MHZ clock input
  DC-400ns instruction cycle
- 14 bit wide instructions
- 8 bit wide data pattern
- 15 special function registers
- 8 level deep hardware stack
- Four interrupt sources:External RB0/INT pin,TMR0 overflow ,Port B interrupt on change,Data EEPROM write complete

4.1.1 PERIPHERAL FEATURES:

- High current sink/source for direct LED drive-25mA sink max per pin
  20mA source max per pin
- TMR0:8 bit timer/counter with 8 bit programmable prescalar
- Watch dog timer with its own on chip RC oscillator for reliable operation

4.1.2 FLASH DEVICES:

These devices are offered in the lower cost plastic package even though the device to be used for prototype development and pilot programs are well as production.A further advantage of the electrically erasable Flash version is that it can be erased and reprogrammed in circuit or by the device programmers such as microchips PIC start plus or promote 2 programmers.

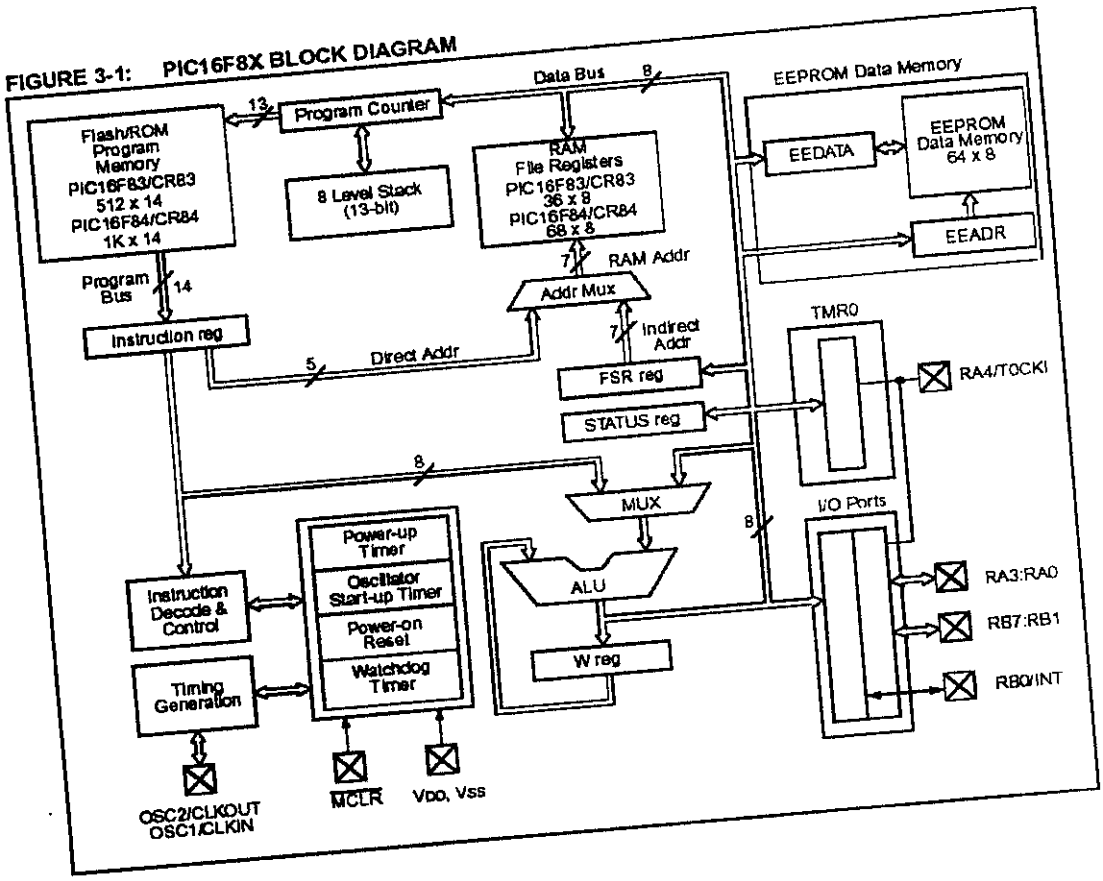
4.2 ARCHITECTURAL OVERVIEW:

To begin with, the PIC16F84 uses a Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC16CXX opcodes are 14-bits wide, enabling single word instructions. The full 14-bit wide program memory bus fetches a 14-bit instruction in a single cycle. A two stage pipeline overlaps fetch and execution

of instructions. Consequently, all instructions execute in a single cycle except for program branches. The PIC16F83 and PIC16CR83 address 512 x 14 of program memory, and the PIC16F84 and PIC16CR84 address 1K x 14 program memory. All program memory is internal. The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. An orthogonal (symmetrical) instruction set makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16F84 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file. The ALU is 8-bits wide and capable of addition, Subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), and the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register. The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

FIGURE 3-1: PIC16F8X BLOCK DIAGRAM



4.3 MEMORY ORGANIZATION:

There are two memory blocks in the PIC16F84. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle. The data memory can further be broken down into the general purpose RAM and the Special Function Registers.The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described

in the section discussing each individual peripheral module.The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped.That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of this memory have the address range 0h-3Fh..

4.3.1 PROGRAM MEMORY ORGANIZATION:

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F83 and PIC16CR83, the first 512 x 14 (0000h-01FFh) are physically implemented . For the PIC16F84 and PIC16CR84, the first 1K x 14 (0000h-03FFh) are physically implemented.Accessing a location above the physically implemented address will cause a wraparound. For example, for the PIC16F84 locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction. The reset vector is at 0000h and the interrupt vector is at 0004h.

4.3.2 DATA MEMORY ORGANIZATION:

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device. Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register.Instructions MOVWF and MOVF can move values from the W register to any location in the register file and vice-versa. The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR). Indirect addressing uses the present value of the RP1:RP0 bitsfor access into the banked areas of data memory. Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to

7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

4.3.3 GENERAL PURPOSE REGISTER FILE :

All devices have some amount of General Purpose Register (GPR) area. Each GPR is 8 bits wide and is accessed either directly or indirectly through the FSR . The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

4.3.4 SPECIAL FUNCTION REGISTERS:

The Special Function Registers are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM. The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in

the section for that specific feature.

4.4 I/O PORTS:

The PIC16F84 has two ports, PORTA and PORTB. Some port pins are multiplexed with an alternate function for other features on the device.

4.4.1 PORTA AND TRISA REGISTERS:

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin. Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-

modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch. The RA4 pin is multiplexed with the TMR0 clock input.

Note: Similar performance is seen in the PORT B and TRIS B register

4.4.2 PRESCALAR:

An 8 bit counter is available as a prescalar for the timer module or as a post scalar for the watchdog timer.The prescalar is fully under software control ie it can be changed during program execution.It can be set to any ratio such that once prescalar is full the timer increments by one the prescalar becoming full depends on the ratio set by the user.

4.4.3 OSCILLATOR:

The PIC can operate in four oscillator modes.In the mode that we area adopting ie the XT mode a crystal is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation.

4.4.4 OSCILLATOR:

The PIC can operate in four oscillator modes.In the mode that we area adopting ie the XT mode a crystal is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation.

4.4.4 RESET:

Of the different Reset options available in PIC family the option that we adopt is the POWER-ON -RESET mode of reset.

4.4.4.1 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected .To take advantage of the POR, just tie the MCLR pin directly to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. When the device starts normal operation device operating parameters, must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met., " Power-up Trouble Shooting." The POR circuit does not produce an internal reset when VDD declines.

4.5 INTERRUPTS:

The PIC16F84 has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits. The global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on reset. The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit, which re-enable interrupts. The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register. When an interrupt is responded to; the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the

interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs . The latency is the same for both one and two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

4.5.1 INT INTERRUPT:

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION_REG<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

4.5.2 TMR0 INTERRUPT:

An overflow (FFh ® 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>).

4.5.3 PORT B INTERRUPT :

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) .

4.5.4 CONTEXT SAVING DURING INTERRUPTS:

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software. The User defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example does the following:

a) Stores the W register.

b) Stores the STATUS register in STATUS_TEMP.

c) Executes the Interrupt Service Routine code

d) Restores the STATUS (and bank select bit) register.

e) Restores the W register.

4.6 ROLE OF PIC IN THE PROJECT:

The PIC microcontroller acts as the complete controlling unit of the whole set up.It gets the output from the scherings bridge and does the following formatting with the data.

- ***It sends the control signal for the conversion of the analog imbalance voltage across the bridge into digital value with reference set based on the look up table values obtained for different samples.***
- ***The ADC is clocked by means of pulses which are generated by the controller and again gets the converted data into it for further processing.***
- ***The controller transmits the digital data that it has stored,serially into the serial port of the PC for getting the percentage impurity .***

5. ADC0808

8-Bit µP Compatible A/D Converters with 8-Channel-Multiplexer

5.1 GENERAL DESCRIPTION:

The ADC0808 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter,*8-channel multiplexer* and microprocessor compatible control logic. The 8-bit A/D converter uses *successive approximation* as the conversion technique. The converter features a high impedance *chopper stabilized comparator*, a *256R voltage divider* with *analog switch tree and a successive approximation register*. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The ADC0808 offers

- High speed
- high accuracy

- minimal temperature dependence
- excellent long-term accuracy and repeatability
- consumes minimal power

The above advantages of this particular converter makes it the most efficient .

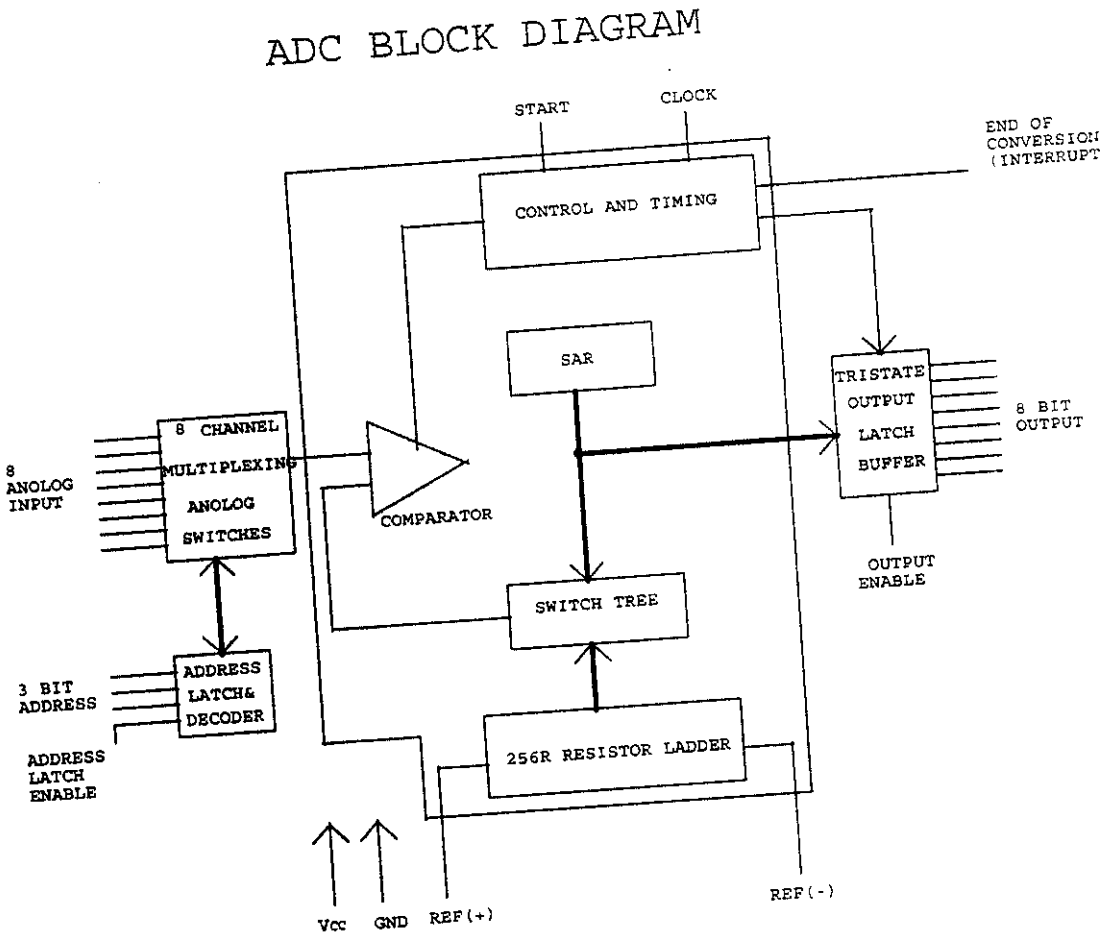
5.2 FEATURES:

1. Easy interface to all microprocessors
2. Operates ratiometrically or with 5 VDC or analog span
3. adjusted voltage reference
4. No zero or full-scale adjust required
5. 8-channel multiplexer with address logic
6. 0V to 5V input range with single 5V power supply
7. Outputs meet TTL voltage level specifications

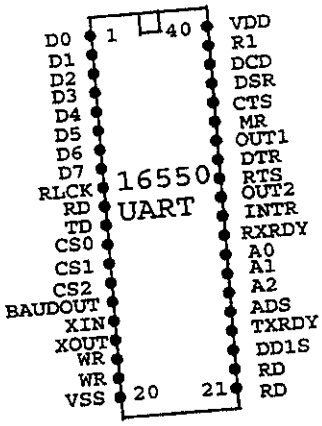
5.3 KEY SPECIFICATIONS:

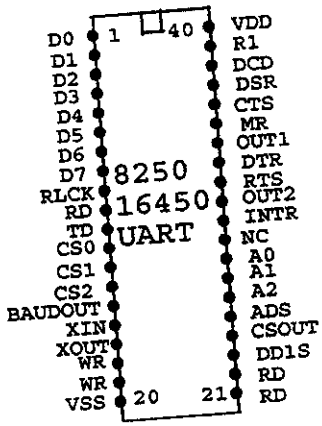
1. Resolution	8 Bits
2. Total Unadjusted Error	± 1 /2 LSB and ±1 LSB
3. Single Supply	5 VDC
4. Low Power	15 mW
5. Conversion Time	100 μs

5.4 BLOCK DIAGRAM:



PIN CONFIGURATION





5.6 FUNCTIONAL DESCRIPTION:

5.6.1 MULTIPLEXER:

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder.*Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

Table:1

SELECTED ADDRESS LINE	ANALOG CHANNEL		
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

5.6.2 THE CONVERTER:

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections:

- The 256R ladder network
- The successive approximation register
- The comparator

The converter's digital outputs are positive true.

5.6.2.1 THE 256R LADDER NETWORK:

The 256R ladder network approach was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally,the 256R network does not cause load variations on the reference voltage.The bottom resistor and the top resistor of the ladder net-work in are not the same value as

the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transi-tion occurs when the analog signal has reached + 1 /2 LSB and succeeding output transitions occur every 1 LSB later upto full-scale.

5.6.2.2 SUCCESSIVE APPROXIMATION REGISTER:

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter The A/D converter's successive approximation register(SAR) is reset on the positive edge of the start conversion start pulse. The conversion is begun on the falling edge ofthe start conversion pulse. A conversion in process will beinterrupted by receipt of a new start conversion pulse. Con-tinuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

5.6.2.3 COMPARATOR:

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the com-parator drift which has the greatest influence on the repeat-ability of the device. A chopper-stabilized comparator pro-vides the most effective method of satisfying all the converter requirements. The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

5.6.2.4 OPERATION:

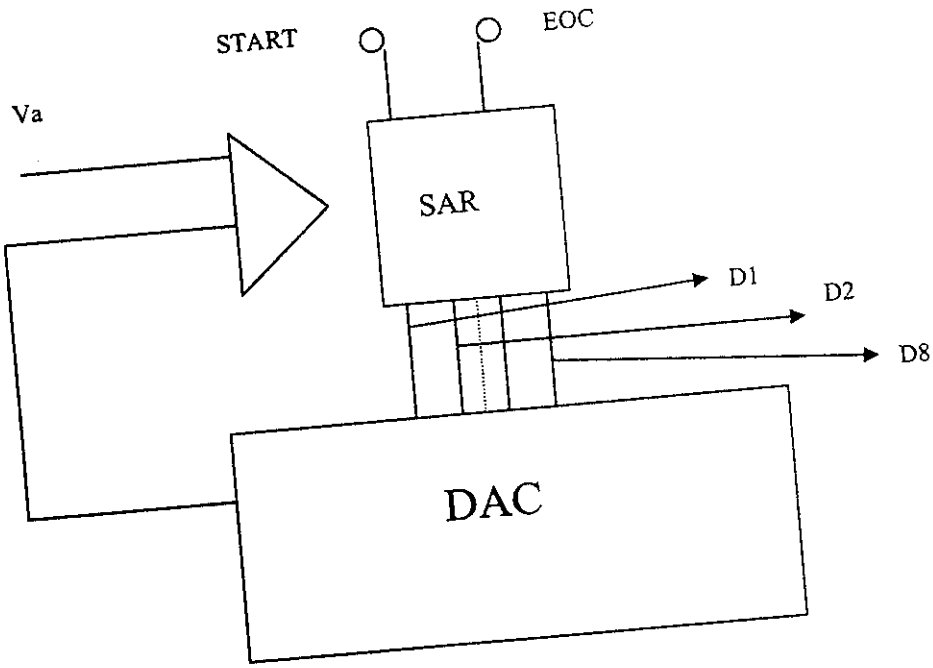
With the arrival of the start command the SAR sets the MSB d1=1with all other bits zero so thst the trial code is 10000000. The output Vd of the DAC is now compared with the analog input Va.If Va is greater than the DAC output Vd is less than the correct digital representation.The MSB is left at 1 and the next lower significant bit is made 1 and further tested.

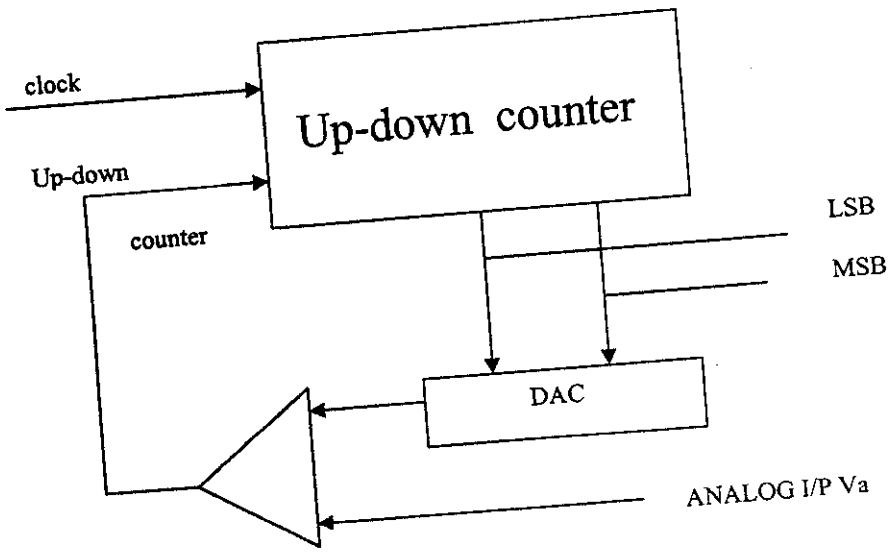
However ,if Va is less than the DAC output, then 10000000 is greater than the correct digital representation.So reset the MSB to 0 and go to the next lowersignificant bit.This procedure is repeated for all the subsequent bits ,one at a time,until all the bit positions have been tested. Whenever the DAC output crosses VA, the comparator changes state and this can be taken as the end of conversion.The table-2 shows a particular sequence.However one additional clock pulse is required is used to latch at the outputs and reinitialize the circuit.

Table:2

Correct digital representation	**Successive approximation register output Vd across the different stages**	**Comparator output**
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	0

5.6.2.5 DIAGRAMS:





5.7 INTEGRATION OF THE ADC AND PIC:

5.7.1 HANDSHAKE WITH PIC:

The PIC acts as a controlling device for the ADC0808. The control signals for the ADC to do its conversion is given by the controller and once it receives similar handshake signal(EOC) from the ADC, the controller handles with the output further processing.

The following I/O lines of the controller are being used for the specified operations

PORT	PORT PIN	SIGNAL	PIN STATUS
PORTA	RA4(3)	EOC	INPUT
PORTA	RA3(2)	OE	OUTPUT
PORTA	RA2(1)	SOC	OUTPUT
PORTA	RA1(18)	DATA OUT	OUTPUT
PORTA	RA0(17)	CLOCK	OUTPUT
PORTB	RBO-RB7 (6-13)	DATA IN	INPUT

SOC:-Start of conversion

OE :-Output Enable

EOC:-End of conversion

Thus the output from the 8 data lines of the ADC are received by the portb pins and then stored in a register from where it is to be transmitted serially.

Accordingly the TRIS values of both the ports are set as follows

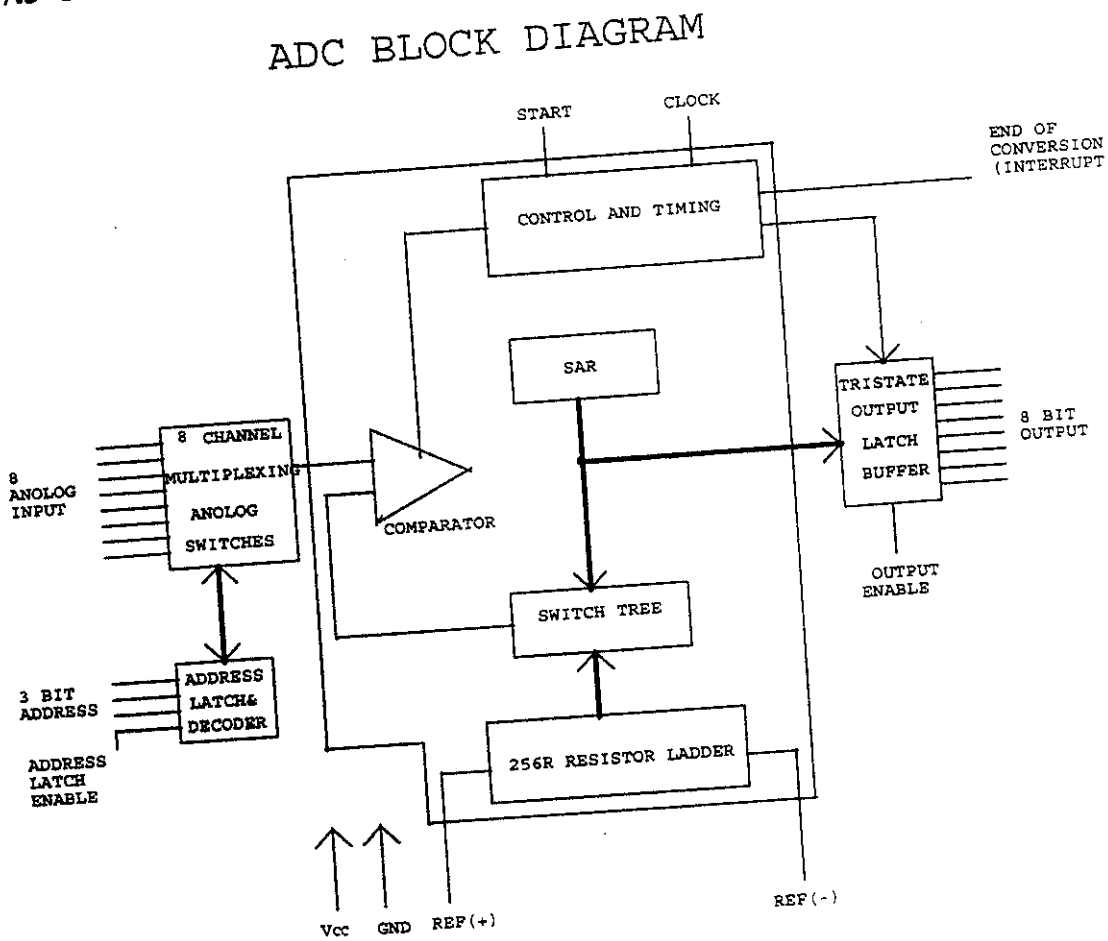
TRIS A ='00010000'

TRIS B ='11111111'

The start pulse given from the controller is also a remarkable feature. The pulse given to the start pin is by making the SOC pin high,then callig a delay and then making the pin low again.

The SOC and the ALE pin of the ADC are shorted and given a single pulse so that the input is taken across latch and reaches the actual input terminal of the internal ADC circuitry .At the same time the EOC pin is continuously being sensed and once the EOC is reached the controller sends a pulse to the output enable pin of the ADC to get the output at the ADC data lines.

5.7.3 CIRCUIT DIAGRAM:



5.7.4 ALGORITHM:

i. Ensure if input signal is given to the input pin of the ADC(here the IN7 input pin is chosen and accordingly the selection pins are also given signals).

ii. Give Start pulse and ALE pulse to the ADC

    1. Make SOC pin high
    2. Call a delay routine
    3. Make the SOC pin low

iii. Check for the EOC pin

    1. If the EOC has been reached goto step (iv)
    2. If the EOC has not been reached the goto step (iii)

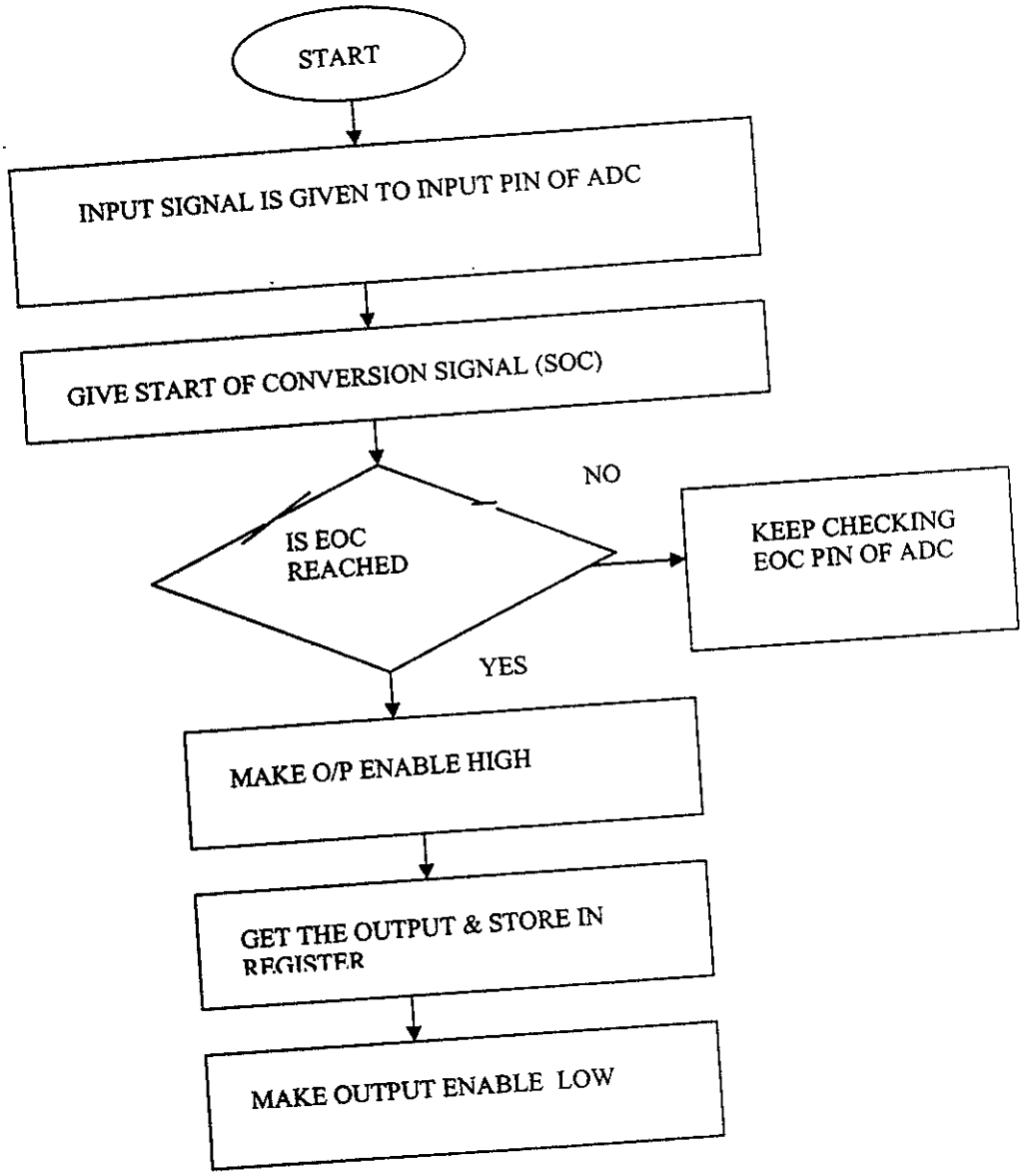
iv. Make the OE pin high

v. Transfer the data into a register

vi. Make the OE pin low.

vii. Goto step (i)

4.7.5 FLOW CHART:



5.7.6 CLOCK PULSE:

One very interesting feature of our project being the clock pulse for the ADC.We have programmed the PIC in such a way that the ADC receives clock pulses for its conversion from the controller itself.For this Interrupt techniques of PIC have been adopted.The PIC generates clock of 54 microseconds time period.

The Time period of the clock pulse is decided by the time the TIMERO special function register takes to overflow and accordingly the Timer overflow generates an internal interrupt to the controller.Each time the register overflows the pin is set to toggle.The internal prescalar is set to a ratio 1:1 so that each time the prescalar increments the timer also increments.All these settings are made in the OPTION register and for enabling Timer interrupt the INTCON register values are changed.

The Interrupts are already enabled at the beginning of the conversion and the disabled after the EOC command is received. The interrups that are being enabled are

a) Global interrupt enable

b) Timer interrupt enable

5.7.6.1 ALGORITHM:

INTERRUPT SERVICE ROUTINE:

i. Disable Interrupt Enable

ii. Check for the clock pin

iii. If high make it low else make it high

iv. Return

6.1 INTRODUCTION

The Serial Port is harder to interface than the Parallel Port. In most cases, any device we connect to the serial port will need the serial transmission converted back to parallel so that it can be used. This can be done using a UART.

The advantages of using serial data transfer rather than parallel

1. The serial port transmits a '1' as -3 to -25 volts and a '0' as +3 to +25 volts where as a parallel port transmits a '0' as 0v and a '1' as 5v.
2. In case of parallel transmission wire requirement is more whereas in serial transmission we require only one wire.Therefore it is cheaper.
3. Serial transmission is used where one bit is sent at a time. IrDA-1 was capable of 115.2k baud and was interfaced into a UART. The pulse length however was cut down to 3/16th of a RS232 bit length to conserve power considering these devices are mainly used on diaries, laptops .
4. Serial Communication reduces the pin count of these MPU's. Only two pins are commonly used, Transmit Data (TXD) and Receive Data (RXD) compared with at least 8 pins if you use a 8 bit Parallel method

6.2 HARDWARE PROPERTIES

The electrical specifications of the serial port is contained in the EIA (Electronics Industry Association) RS232C standard. It states many parameters such as –

1. A "Space" (logic 0) will be between +3 and +25 Volts.
2. A "Mark" (Logic 1) will be between -3 and -25 Volts.
3. The region between +3 and -3 volts is undefined.
4. An open circuit voltage should never exceed 25 volts. (In Reference to GND)
5. A short circuit current should not exceed 500mA. The driver should be handle this without damage.

6.3 SERIAL PINOUTS (D25 AND D9 CONNECTORS)

Serial Ports come in two "sizes", There are the D-Type 25 pin connector and the D-Type 9 pin connector both of which are male on the back of the PC, thus you will require a female connector on your device. Below is a table of pin connections for the 9 pin and 25 pin D-Type connectors. Now we consider D-Type 9 pin for our study.

D-Type-9 Pin No.	**Abbreviation**	**Full Name**
Pin 3	TD	Transmit Data
Pin 2	RD	Receive Data
Pin 7	RTS	Request To Send
Pin 8	CTS	Clear To Send
Pin 6	DSR	Data Set Ready
Pin 5	SG	Signal Ground
Pin 1	CD	Carrier Detect
Pin 4	DTR	Data Terminal Ready
Pin 9	RI	Ring Indicator

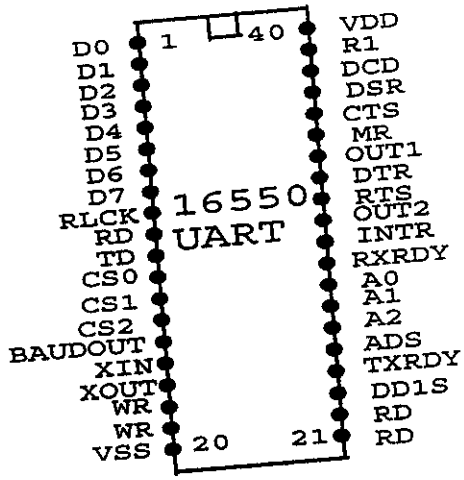
6.3.1 LOOPBACK PLUG

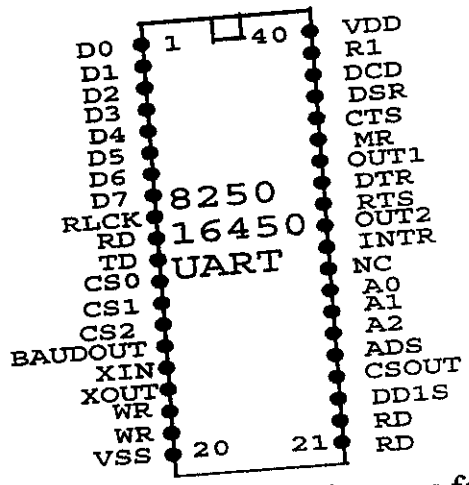
This loopback plug can come in extremely handy when writing Serial / RS232 Communications Programs. It has the receive and transmit lines connected together, so that anything transmitted out of the Serial Port is immediately received by the same port. If you connect this to a Serial Port an load a Terminal Program, anything you type will be immediately displayed on the screen

6.4 THE UART (8250 AND COMPATIBLES)

UART stands for Universal Asynchronous Receiver / Transmitter. Its the little box of tricks found on your serial card which plays the little games with your modem or other connected devices. Most cards will have the UART's integrated into other chips which may also control your parallel port, games port, floppy or hard disk drives and are typically surface mount devices. The 8250 series, which includes the 16450, 16550, 16650, & 16750 UARTS are the most commonly found type in your PC. Later we will look at other types which can be used in your homemade devices and projects.

PIN CONFIGURATION

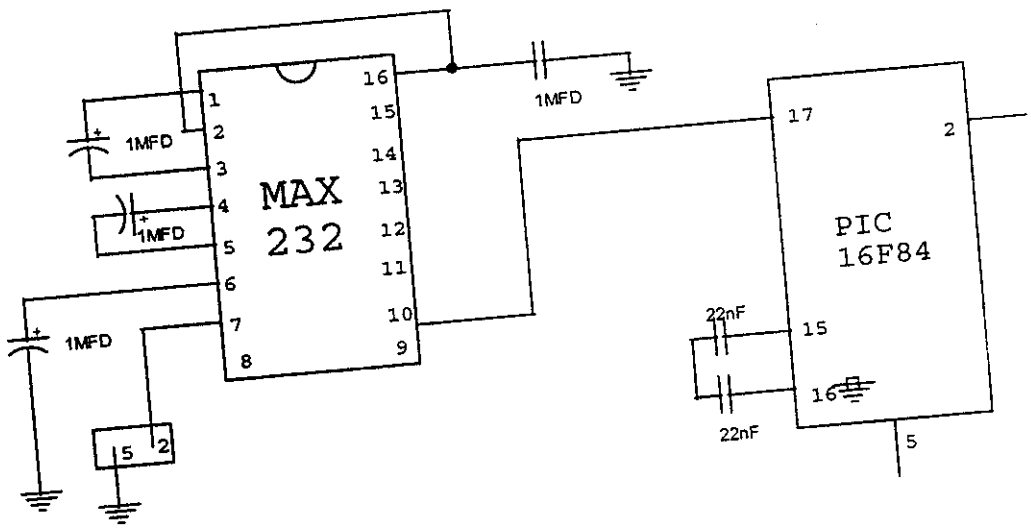




Pin Diagrams for 16550, 16450 & 8250 UARTs

6.4.3 CIRCUIT DIAGRAM

MAX 232 CIRCUIT CONNECTION



The 16550 is chip compatible with the 8250 & 16450. The only two differences are pins 24 & 29. On the 8250 Pin 24 was chip select out which functioned only as a indicator to if the chip was active or not. Pin 29 was not connected on the 8250/16450 UARTs. The 16550 introduced two new pins in their place. These are Transmit Ready and Receive Ready which can be impleSmented with DMA (Direct Memory Access). These Pins have two different modes of operation. Mode 0 supports single transfer DMA where as Mode 1 supports Multi-transfer DMA.

Mode 0 is also called the 16450 mode. This mode is selected when the FIFO buffers are disabled via Bit 0 of the FIFO Control Register or When the FIFO buffers are enabled but DMA Mode Select = 0. (Bit 3 of FCR) In this mode RXRDY is active low when at least one character (Byte) is present in the Receiver Buffer. RXRDY will go inactive high when no more characters are left in the Receiver Buffer. TXRDY will be active low when there are no characters in the Transmit Buffer. It will go inactive high after the first character / byte is loaded into the Transmit Buffer.

Mode 1 is when the FIFO buffers are active and the DMA Mode Select = 1. In Mode 1, RXRDY will go active low when the trigger level is reached or when 16550 Time Out occurs and will return to inactive state when no more characters are left in the FIFO. TXRDY will be active when no characters are present in the Transmit Buffer and will go inactive when the FIFO Transmit Buffer is completely Full.

All the UARTs pins are TTL compatible. That includes TD, RD, RI, DCD, DSR, CTS, DTR and RTS which all interface into your serial plug, typically a D-type connector. Therefore RS232 Level Converters (which we talk about in detail later) are used. These are commonly the DS1489 Receiver and the DS1488 as the PC has +12 and -12 volt rails which can be used by these devices. The RS232 Converters will convert the TTL signal into RS232 Logic Levels.

The UART requires a Clock to run. If you look at your serial card a common crystal found is either a 1.8432 MHZ or a 18.432 MHZ Crystal. The crystal in connected to the XIN-XOUT pins of the UART using a few extra components which help the crystal to start oscillating.

This clock will be used for the Programmable Baud Rate Generator which directly interfaces into the transmit timing circuits but not directly into the receiver timing circuits. For this an external connection mast be made from pin 15 (BaudOut) to pin 9 (Receiver clock in.) Note that the clock signal will be at Baudrate * 16.

Types of UARTS (For PC's)

- 8250
- 8250A
- 8250B
- 16550
- 16650
- 6550A
- 16750

6.5 INTERFACING DEVICES TO RS-232 PORTS

6.5.1 RS-232 WAVEFORMS

RS-232 communication is asynchronous. That is a clock signal is not sent with the data. Each word is synchronized using it's start bit, and an internal clock on each side, keeps tabs on the timing.

The diagram above, shows the expected waveform from the UART when using the common 8N1 format. 8N1 signifies 8 Data bits, No Parity and 1 Stop Bit. The RS-232 line, when idle is in the Mark State (Logic 1). A transmission starts with a start bit which is (Logic 0). Then each bit is sent down the line, one at a time.

The LSB (Least Significant Bit) is sent first. A Stop Bit (Logic 1) is then appended to the signal to make up the transmission.

The diagram, shows the next bit after the Stop Bit to be Logic 0. This must mean another word is following, and this is it's Start Bit. If there is no more data coming then the receive line will stay in it's idle state(logic 1). We have encountered something called a "Break" Signal. This is when the data line

is held in a Logic 0 state for a time long enough to send an entire word. Therefore if you don't put the line back into an idle state, then the receiving end will interpret this as a break signal.

The data sent using this method, is said to be *framed*. That is the data is *framed* between a Start and Stop Bit. Should the Stop Bit be received as a Logic 0, then a framing error will occur. This is common, when both sides are communicating at different speeds.

The above diagram is only relevant for the signal immediately at the UART. RS-232 logic levels uses +3 to +25 volts to signify a "Space" (Logic 0) and -3 to -25 volts for a "Mark" (logic 1). Any voltage in between these regions (ie between +3 and -3 Volts) is undefined. Therefore this signal is put through a "RS-232 Level Converter".

The above waveform applies to the Transmit and Receive lines on the RS-232 port. These lines carry serial data, hence the name

Serial Port. There are other lines on the RS-232 port which, in essence are *Parallel* lines. These lines (RTS, CTS, DCD, DSR, DTR, RTS and RI) are also at RS-232 Logic Levels.

6.5.2 RS-232 LEVEL CONVERTERS

Almost all digital devices which we use require either TTL or CMOS logic levels. Therefore the first step to connecting a device to the RS-232 port is to transform the RS-232 levels back into 0 and 5 Volts. As we have already covered, this is done by RS-232 Level Converters. Two common RS-232 Level Converters are the 1488 RS-232 Driver and the 1489 RS-232 Receiver.

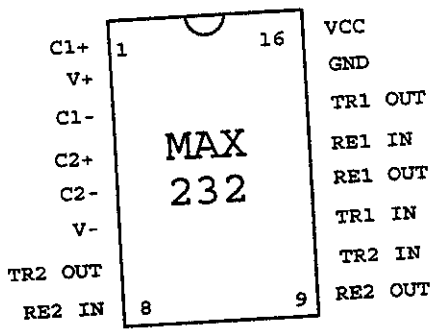
Each package contains 4 inverters of the one type, either Drivers or Receivers. The driver requires two supply rails, +7.5 to +15v and -7.5 to -15v. As you could imagine this may pose a problem in many instances where only a single supply of +5V is present. However the advantages of these I.C's are they are cheap. Another device is the MAX-232. It includes a Charge Pump, which generates +10V and -10V from a single 5v supply. This I.C. also includes two receivers and two transmitters in the same package. This is handy in many cases when you only want to use the Transmit and Receive data Lines. You don't need to use two chips, one for the receive line and one for the transmit. However all this convenience comes at a price, but compared with the price of designing a new power supply it is very cheap.

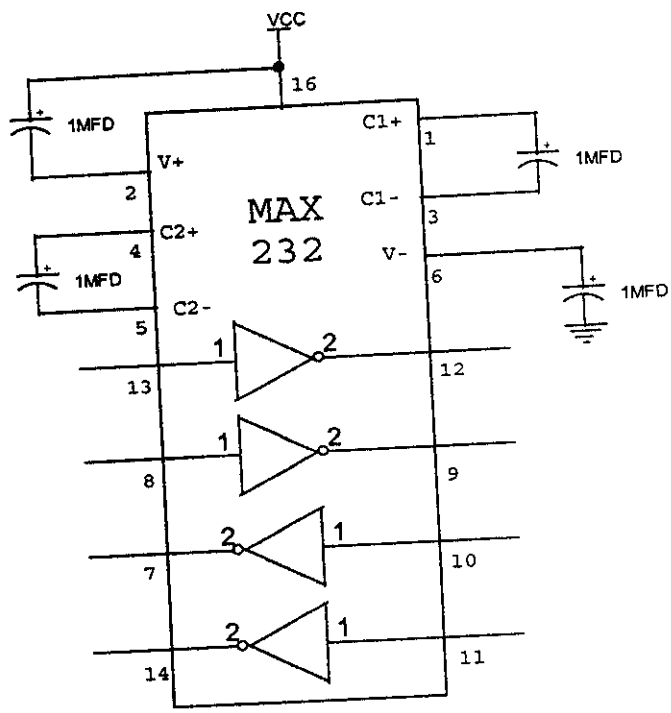
There are also many variations of these devices. The large value of capacitors are not only bulky, but also expensive. Therefore other devices are available which use smaller capacitors and even some with inbuilt capacitors.

(Note : Some MAX-232's can use 1 micro farad Capacitors).

TYPICAL MAX 232 CIRCUIT

PIN CONFIGURATION

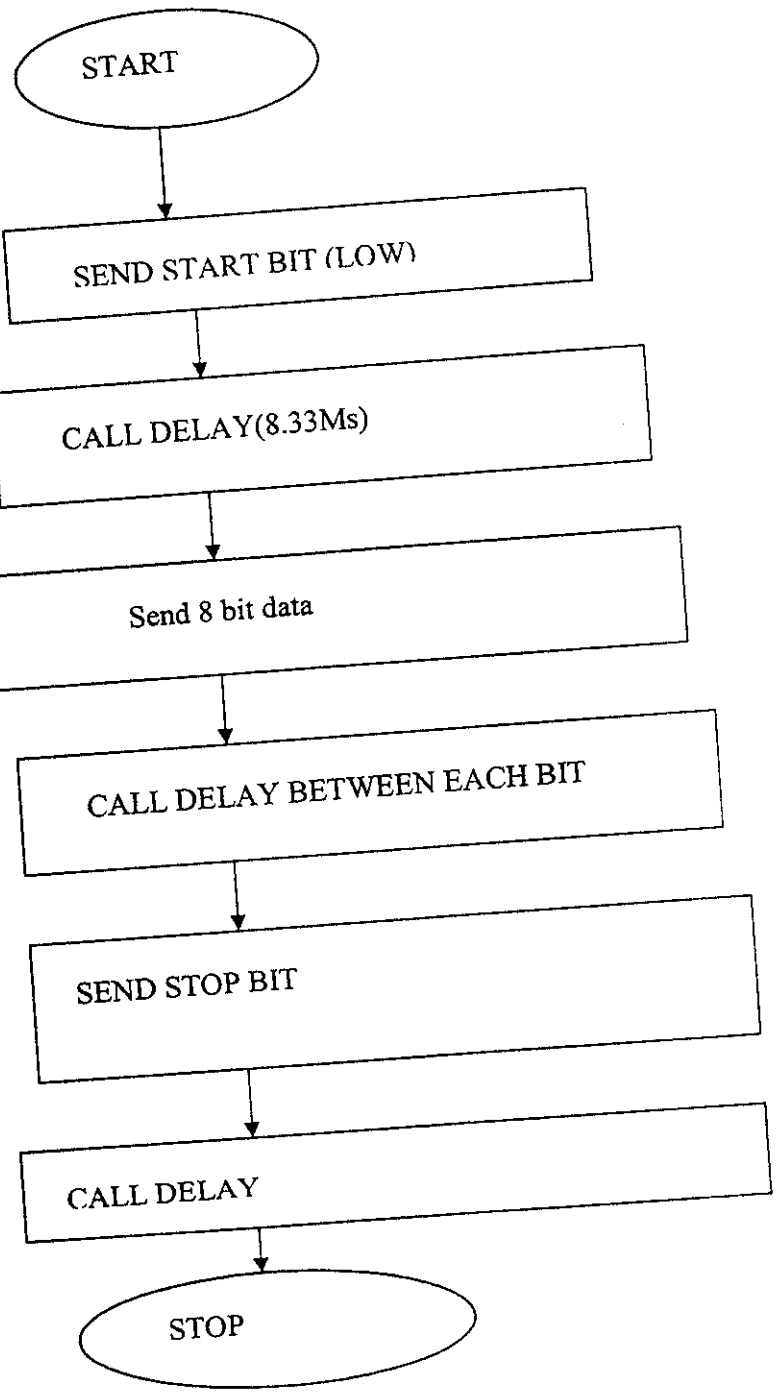


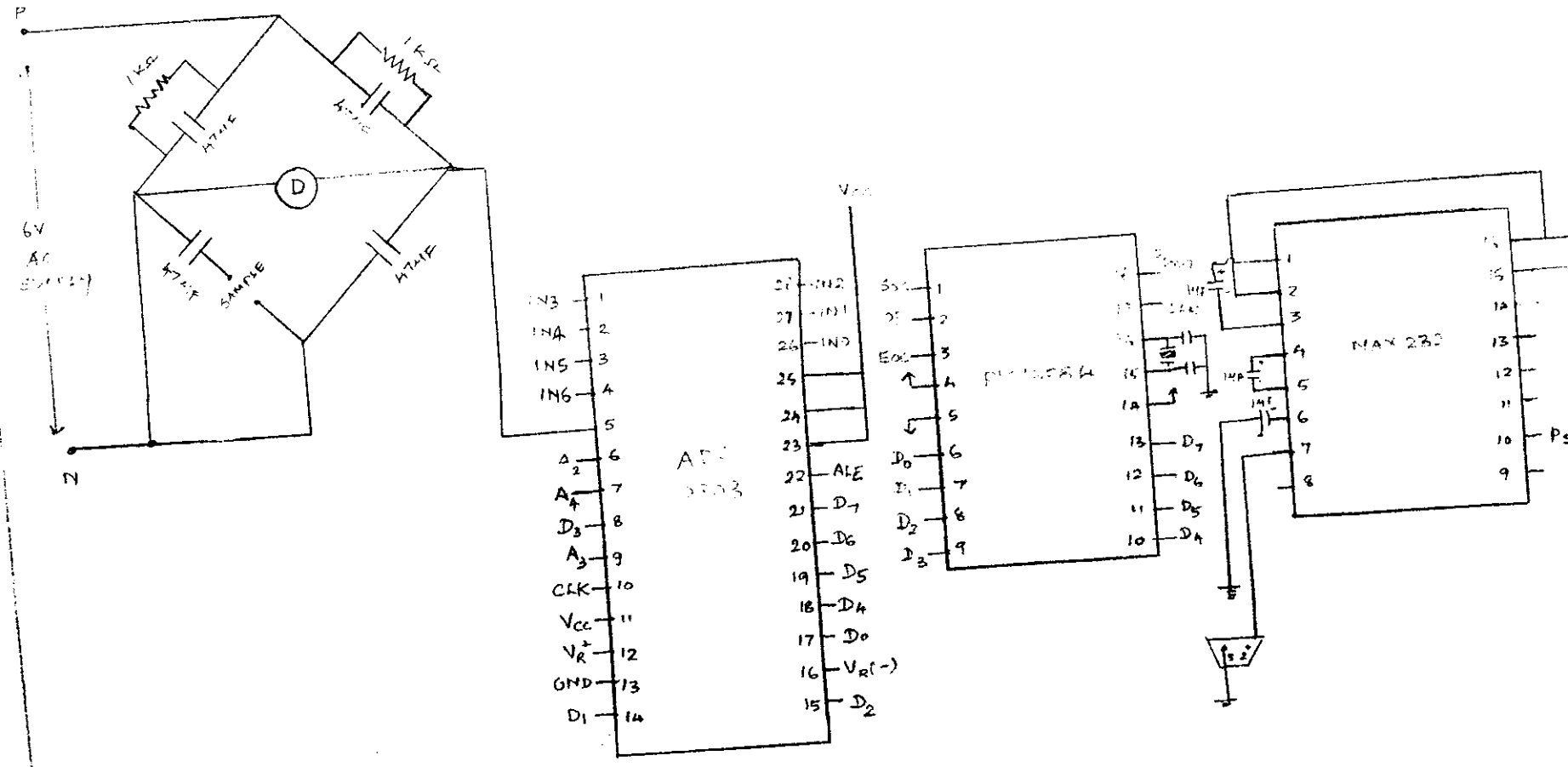


6.4 ALGORITHM

i. Start the program
ii. Send the start bit (Low)
iii. Call delay (833 μs)
iv. SSSend I Data bit
v. Call delay (833 μs)
vi. Send II Data bit
vii. Call delay (833 μs)
viii. Send III Data bit
ix. Call delay (833 μs)
x. Send IV Data bit
xi. Call delay (833 μs)
xii. Send V Data bit
xiii. Call delay (833 μs)
xiv. Send VI Data bit
xv. Call delay (833 μs)
xvi. Send VII Data bit
xvii. Call delay (833 μs)
xviii. Send VIII Data bit
xix. Call delay (833 μs)
xx. Send stop bit
xxi. Call delay (833 μs)
xxii. send stop bit
xxiii. Call delay (833 μs)
xxiv. Stop the program

6.6 FLOWCHART




P
1 KΩ
1 KΩ
470nF
470nF
D
6V
AC
SAMPLE
470nF
470nF
N
IN3
IN4
IN5
IN6
A2
A4
D3
A3
CLK
Vcc
VR+
GND
D1
GND
IN1
IN2
ALE
D7
D6
D5
D4
D0
VR(-)
D2
SOC
OE
EOC
D0
D1
D2
D3
D7
D6
D5
D4
MAX 232
1MF
1MF
1MF
1MF
P

7.2 ALGORITHM

1. Imbalance voltage across the Schering's bridge is determined for the given sample
2. The controller sends signals for the ADC to start conversion
3. The controller polls the EOC pin to check for End Of Conversion signal from the ADC and sends commands foe enabling output device.
4. The digital output stored is transmitted serially to the PC for calculating the percentage purity.
5. Compilation of a C program receives the data from the com1 port, calculates the rms value.
6. Thus from the voltage value the percentage purity is indicated .

CHAPTER EIGHT
RESULTS AND CONCLUSION

8.RESULTS:

8.1 DETAILS ABOUT ELECTRODES:

The electrodes that we have used in the project are normal aluminium sheets of 2 sqcm and they are placed at a distance of 2-3cm. The whole testing is done with the electrodes placed in a beaker.

8.2 DETAILS ABOUT THE SAMPLES:

The samples we have used are petrol and petrol mixed with certain impurities mixed in different proportions .For these samples used as dielectric the voltage across the bridge is obtained and the accordingly the impurity percentage is obtained The following look up table gives the voltage values for different samples.

Pure Petrol	2.5V
Sample2(50% PETROL &50%DIESEL)	1.66V

8.3 CONCLUSION:

Explaining a new concept of using petroleum fuels as dielectric and hence measuring the purity percentage of the sample we have successfully completed the project.Although we have not dealt with the properties of the fuels in depth with the available resources, we have covered the phenomenon to the best possible extent.

Certain difficulties we faced while measuring the voltage values were "sensitivity". In the further expansion of the project it could be dealt with greater precision. The variation of the voltage for the different samples was too small to show its disparity prominently.

The cost of petroleum fuels is getting increased day by day.It is the primal duty of all vehicle owners to check if they get what they pay for.It is essential to test the purity of petroleum fuels in order to abstain from the detrimental effects the impurities can cause to the engine.This indicator can be used by all vehicle owners ,petrol booths ,industries,which make maximum use of petroleum fuels to safeguard and also prolong the effective operation of all the engines.

A. CODING:

```
;program to convert data from scherings bridge to digital and send it serially.

;_____

        list p=16f84

#define      option0x01

#define      porta  0x05

#define      portb  0x06

#define      status 0x03

#define      pstart porta,0x02

#define      peoc   porta,0x04

#define      poe    porta,0x03

#define      Psout porta,0x01

#define      rpo    0x05

#define      f      0x01

#define      w      0x00

#define      pcarrystatus,0x00

#define      zero   0x00

#define      pnext porta,0x00
```

```
#define     tmr0  0x01
#define     pclock      option,0x05
#define     pedge option,0x04
#define     pscaleoption,0x03
#define     ps2   option,0x02
#define     ps1   option,0x01
#define     ps0   option,0x00
#define     intcon0x0b
#define     gie   intcon,0x07
#define     toie  intcon,0x05
#define     toif  intcon,0x02
#define     pin   porta,0x00
;_____________________________________
        org   0x00
        goto  main
;_____________________________________
        cblock 0x10
    varadcdata
```

```
vardlycnt
vardlycnt1
vardlycnt2
varflag
        endc
;_____________________________________
        org    0x04
;isr
        bcf    toif
        movlw        0xea
        movwf        tmr0
        btfss  varflag,0x00
        goto   $+4
        bcf    varflag,0x00
        bcf    pin
        retfie
        bsf    varflag,0x00
        bsf    pin
```

```
        retfie
;_____________________________________

        org 0x20

main
        call    fninitio
        call    fninitram
        call    fngetadcdata
        call    fnstartbitsend
        call    delay1
        call    fnpsenddata
        call    delay1
        call    fnpsenddata
        call    delay1
        call    fnpsenddata
        call    delay1
        call    fnpsenddata
        call    delay1
        call    fnpsenddata
```

```
call    delay1
call    fnpsenddata
call    delay1
call    fnpsenddata
call    delay1
call    fnpsenddata
call    delay1
call    fnstopsendbit
call    delay1
call    delay1
call    delay2
goto    $+1
goto    main
;_____________________________________
fninitio
        bsf     toie
        bsf     status,rpo
        movlw       b'11110000'
        movwf       porta
```

```
    movlw       b'11111111'
    movwf       portb
    bcf    pclock
    bcf    status,rpo
    bcf    pstart
    bcf    poe
    bsf    Psout
    return
;_____________________________________
fninitram
        clrf    varadcdata
        clrf    varflag
        clrf    vardlycnt1
        clrf    vardlycnt2
        clrf    vardlycnt
        return
  ;_____________________________________
```

```
fngetadcdata
        bsf     gie
        bsf     pstart
        call    fndelay
        bcf     pstart
        btfss   peoc
        goto    $-1
        bcf     gie
        bsf     poe
        movf    portb,w
        movwf       varadcdata
        bcf     poe
        return
;_____________________________________
fndelay
        movlw       .31
        movwf       vardlycnt
        decfszvardlycnt,f
        goto    $-1
```

```
        return
;_____________________________________
fnpsenddata
        btfss  varadcdata,0x00
        goto   psoutclear
        goto   psoutset
  psoutclear
        nop
        goto   $+1
        bcf    Psout
        rrf    varadcdata,f
        return
    psoutset
        nop
        nop
        bsf    Psout
        rrf    varadcdata,f
        return
```

```
fnstartbitsend
        bcf    Psout
        nop
        return
;-----------------------------------------
fnstopsendbit
        goto   $+1
        goto   $+1
        goto   $+1
        bsf    Psout
        return
;-----------------------------------------
delay1
        movlw       .163
        movwf       vardlycnt1
        nop
        goto   $+1
        decfszvardlycnt1,f
```

```
        goto   $-2
        return
;-----------------------------------------
delay2
        movlw       .5
        movwf       vardlycnt2
        decfszvardlycnt2,f
        goto   $-1
        return
;-----------------------------------------
        end
```

B.TERMINOLOGY:

REGISTERS AND PINS:

Option	:-	Option register(SFR)
Porta	:-	PortA register
Portb	:-	PortB register
Status	:-	Status register
Pstart	:-	SOC pin
Peoc	:-	EOC pin
Poe	:-	OE pin
Psout	:-	Serial out data pin
Gie	:-	Global Interrupt Enable bit
Toie	:-	Timer Interrupt Enable bit
Pin	:-	Clock pulse pin
Varadcdata	:-	A user defined register to store the digital data
Vardlycnt	:-	A user defined register used in the delay routine
vardlycnt1	:-	A user defined register used in the delay routine
vardlycnt2	:-	A user defined register used in the delay routine
varflag	:-	A user defined register to store the toggling data of isr

FUNCTIONS:

Fninitio	:-	to set initial values
Fninitram	:-	to clear user defined registers initially
Fngetadcdata	:-	to get analog and send and receive signals to ADC0808
Fnstartbitsend	:-	to send low start bit in serial transmission
Fnpsenddata	:-	to send the eight bit data each
Fnstopbitsend	:-	to send high stop bit pulse

BOOKS:

MEASUREMENTS AND INSTRUMENTATION

-A.K.SHAWNEY

MEASUREMENTS AND INSTRUMENTATION

-GOLDING

ENGINEERING CHEMISTRY

-JAIN & JAIN

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