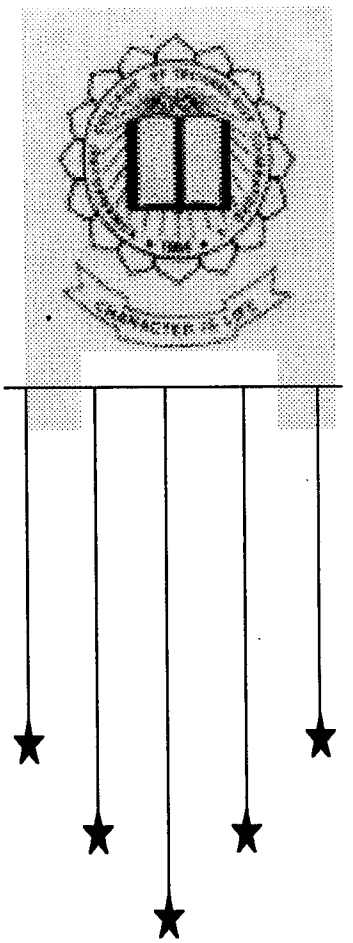
AN INTELLIGENT POWER FACTOR CONTROL SYSTEM USING MICROCONTROLLER FOR EFFICIENT OPERATION OF INDUCTION MOTOR



SUBMITTED BY

M.KIRUTHIGA

K.MARILAKSHMI

B.SUBACHANDAR

K.ARAVIND KUMAR

UNDER THE GUIDANCE OF,

Mr.R.K.Pongiannan,B.E.,M.E,
MISTE,MSST,AMIE

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF BE DEGREE IN ELECTRICAL & ELECTRONICS ENGINEERING UNDER BHARATHIAR UNIVERSITY

Department Of Electrical& Electronics Engineering

Kumaraguru College Of Technology

Coimbatore-641006.

CERTIFICATE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE – 641 006

ISO 9001:2000

CERTIFICATE

This is to certify that the Project Report entitled

"AN INTELLIGENT POWER FACTOR CONTROL SYSTEM USING MICROCONTROLLER FOR EFFICIENT OPERATION OF INDUCTION MOTOR "

has been submitted by

KIRUTHIGA. M	99EEE22
MARILAKSHMI. K	99EEE27
SUBACHANDAR. B	99EEE54
ARAVIND KUMAR. K	99EEE05

in partial fulfillment of the requirements for the award of the degree of Bachelor of Engineering in Electrical and Electronics branch of Bharathiar University, Coimbatore during the academic year 2002 - 2003

Project Guide

Head of Department

Certified that the candidate with University Register No. _____
was examined in project work Viva – Voce Examination on _____

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We wish to express our deep sense of gratitude and indebtedness to our project guide Mr. R. K. Pongiannan, B.E.,M.E,MISTE,MSSI,AMIE. Senior Lecturer, Department of Electrical and Electronics Engineering, for his invaluable guidance and constructive suggestions, the keen and constant inspiration and interest evinced by him at all stages right from the inception to the completion.

We are highly grateful to Prof. T.M. Kameswaran,B.E.,M.Sc.,(Engg)Ph.d., MISTE, Sr.M.I.E.E.E., F.I.E., Head of the Department, Electrical and Electronics Engineering, for his enthusiasm and encouragement which has been instrumental in the success of the project.

We express our heartfelt gratitude to our principal Dr. K. K. Padmanabhan, B.Sc.,(Engg), M.Tech., Ph.D., F.I.E., for providing the necessary facilities for the successful completion of the project.

We are also indebted to the staff members of Electrical and Electronics Department for their cooperation. We are thankful to our student friends for their encouragement and help during the course of the project.

SYNOPSIS

Synopsis

In our country, industrial, commercial and domestic sectors, the utilization of inductive loads is increasing day by day due to new installations. In industrial sectors, the most power consuming load is induction motor drive and lighting loads. The agricultural sector consists of mono set pumps, submersible pumps, open well submersible pumps and bore well compressor pumps which are driven by induction motors. The commercial and domestic sector consists of single phase jet centrifugal pumps, mono set pumps and bore well compressor pumps. Some of the pumps used in domestic and commercial uses are driven by capacitor start capacitor run motors which operate at better power factor during rated supply conditions and their power factor is reduced due to a single value capacitor and also due to the variations in load and supply parameters. The applications like mini mono set pumps, jet centrifugal pump combination, open well mono set and submersible pumps employing single phase capacitor start capacitor run motors with a permanent single value capacitor may leads to leading power factor. The applications like compressors, small machine tool application, and wet grinders which require high starting torque are employed with capacitor start induction motors. Since the normal operating power factor of capacitor start induction motors is poor, it is necessary to improve the power factor.

In our project entitled "**An intelligent power factor control system using microcontroller for efficient operation of induction motor**" is designed and implemented with hardware and software

program in assembly language. The system consists of an intelligent power controller section which measures the real time power factor of the single phase load and improves the power factor to a desired value. The control section of the system has micro controller and relays. The power section has the capacitor bank with different values of capacitors. The display unit displays the improved power factor of the load under a specified range of operating voltage and load condition..

The system has been working satisfactorily and the operating power factor is maintained around unity for varying supply voltage of 150volts to 260 volts at different load conditions.

CONTENTS

CONTENTS

INTRODUCTION

1. Introduction

1.1.Power Factor Defined

Power factor is defined as the ratio of the actual power of an alternating current to the apparent power, or the ratio of the resistance to impedance. Power factor is calculated by determining the cosine of the phase angle between the voltage applied to a load and the current passing through the load.

1.2. Power factor correction

Power factor correction is the process of installing reactive power supplying components that bring the power factor of a branch or circuit closer to "unity power factor" or a power factor of 1.0.Unity power factor is obtained only when current and voltage are in phase. Loads that are inductive in nature require the installation of elements with capacitive terminal characteristics which have the primary function of improving power factor. In an application, power factor correction is accomplished by the installation of capacitors to a normally inductive circuit. As a result, power factor is increased and the total current through the circuit is closer in phase with the applied voltage. Power-factor correction is used in the design of systems that are very sensitive to unusually high currents passing through the load. Generally, a power factor as close to a value of one as possible is the most desirable because most of the power generated from the power source to the load is useful or true power.

1.3. Determining Additional Output Power

When determining the amount of output power available after applying PFC, an analysis using the following equation is required:

Pout = Vin (RMS) * Iin (RMS) * PF * Efficiency

For example, if the power-factor is increased from 0.55 to 0.90, the resulting computation yields an overall increase in output power (Pout).

1.4 Increasing Power Factor

Solving the problem of high harmonics within an application is accomplished by the use of power-factor correctors or Power factor correctors. Power-factor correctors are electronic devices that reshape the non-sinusoidal alternating current waveforms propagating through the circuits and thereby improve the power factor value for the circuit. Two types of Power factor correctors are in common use today: active and passive. Active Power factor correctors are more effective in improving power factor but they are more expensive. Active Power factor correctors can be installed as a part of an off-line switching unit. Passive Power factor correctors are more reliable and less expensive, and can be designed as a stand-alone unit.

The power factor of the transmission lines and the loads like transformers, induction motors and arc lamps is varying with respect to operating conditions. In load side, most of the loads are induction motor drives which are operating at low power factor. Hence a necessary step has been taken to improve the operating power factor of these loads to a desired value usually unity by using switched capacitor banks, synchronous condensers and thyristorised switching capacitors.

2. *Need for Intelligent power factor correction*

The operating power factor of three phase and single phase capacitor start induction run motor is too low during no load and light load conditions. The power factor is around 0.8 during rated conditions depends on the design. the application like mini mono set pumps, jet centrifugal pump combination, open well mono set and submersible pumps employing single phase capacitor start capacitor run motors with the permanent single value capacitor leads to leading power factor under light load conditions and lagging power factor during abnormal operating conditions.

The low power factor operation leads to increased line current, hence the losses and the conductor size is increased and the system efficiency is decreased. To achieve energy efficient operation of single phase and three phase induction motors it is necessary to operate them at unity power factor. Thus the over all efficiency of the power system is increased. The considerable energy conservation is achieved by the improved power factor operation.

3. System architecture

The intelligent power factor correction system is shown in the figure -1.It consists of power supply unit, an intelligent power factor sensing and correction unit, capacitor switching unit and the display unit.

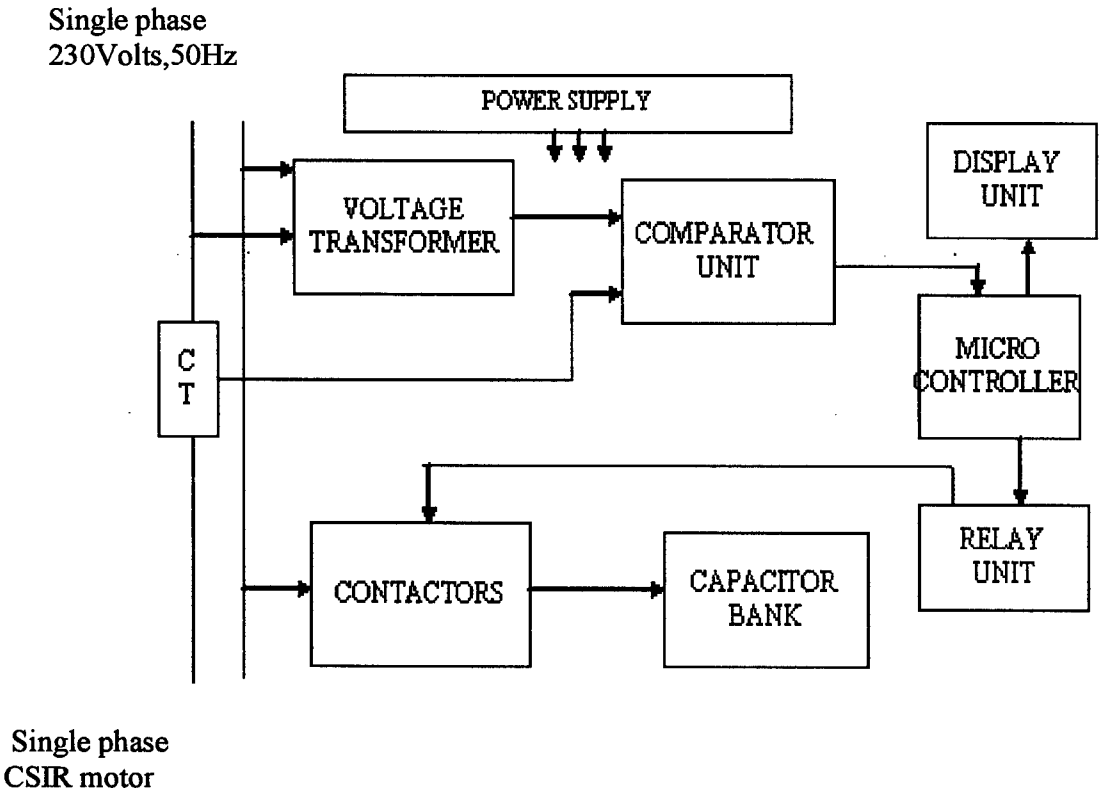


Figure – 1 : Block diagram of the Intelligent power factor correction system

Block diagram consists of:

- The potential transformer.
- The current transformer.
- Comparator.
- Logic circuit.
- Micro controller.
- Control circuit.
- Capacitor bank.

The input voltage is applied to primary winding of potential transformer. And the input current is applied to the current transformer. In this two outputs from the transformer are converted into square wave form in the comparator. The output of the comparators is applied to the logic circuit. The logic circuits are used to allow the positive half cycle from the voltage and negative half cycle of the current wave forms, the negative half cycle current wave will be converted into positive half cycle by the NOT gate.

The two voltage and current wave forms are applied to the AND gate. Whenever the AND gate output is one the timer of the micro controller will count the timing pulses from the crystal oscillator. The micro controller senses the micro controller.

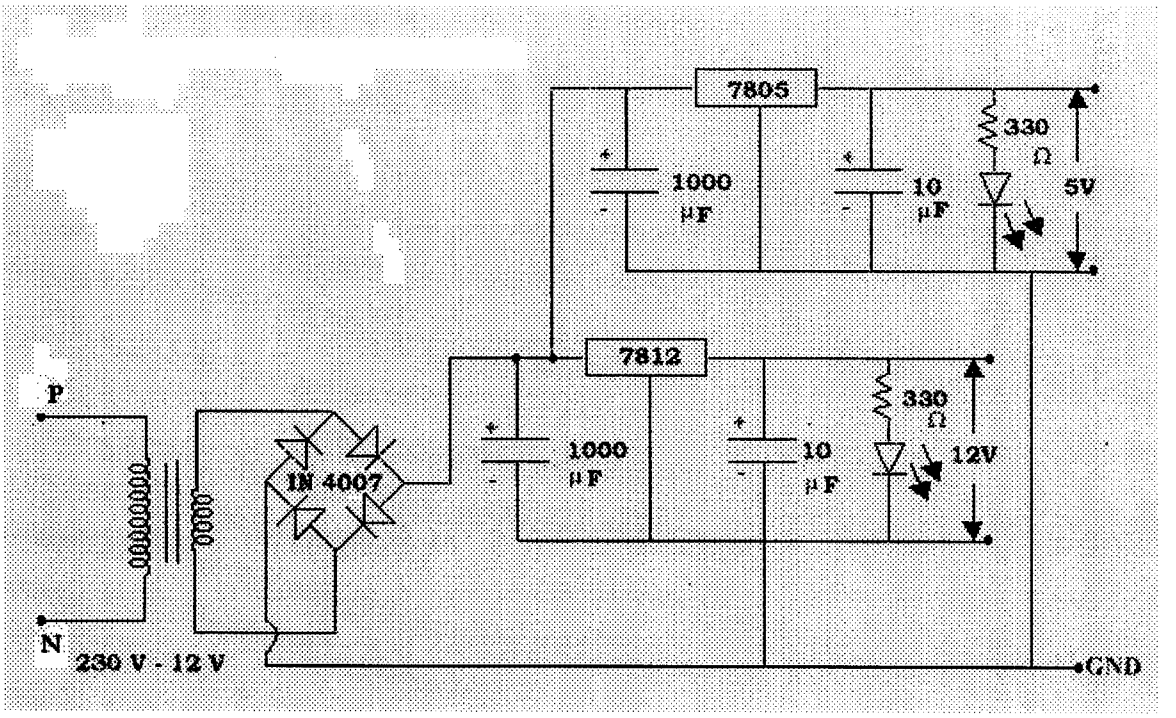
If it is low as compare to reference value, it will drive or energize the required number of relays. The control circuit consists of relays. The capacitor bank is connected across the load through a relay N.O. contact. If the relay coils are energized the N.O. contact of the relays will be closed. Hence the capacitors are added to the load in parallel. Now the power factor will be improved automatically.

HARDWARE

3.1 Hardware Description of the System

3.1.1 Power Supply Module

The power supply module is shown in figure and has 5 volts and 12 volts sources.



3.1.2. Power factor sensing module

The power factor-sensing module consists of the line voltage sensor, line current sensor, comparator and micro controller.

a. Potential transformer

Specifications:

Primary voltage --- > 230volts AC

Secondary voltage --- > 0-6volts AC

It senses the line voltage and the output of potential transformer are fed as one of the input to the Zero crossing detector circuit.

b. Current transformer

Specifications:

Primary current --- > 2A

Secondary current --- > 100mA

It senses the line current and the current transformer output is fed to the zero crossing detector circuit. This system can used for heavy loads with the suitable ratio of Current Transformer.

c. Zero crossing detector

Specifications

IC741 (8 pin)

Supply --------> +5v & gnd

It converts two sinusoidal signals in to square wave from the current transformer and potential transformer signals.

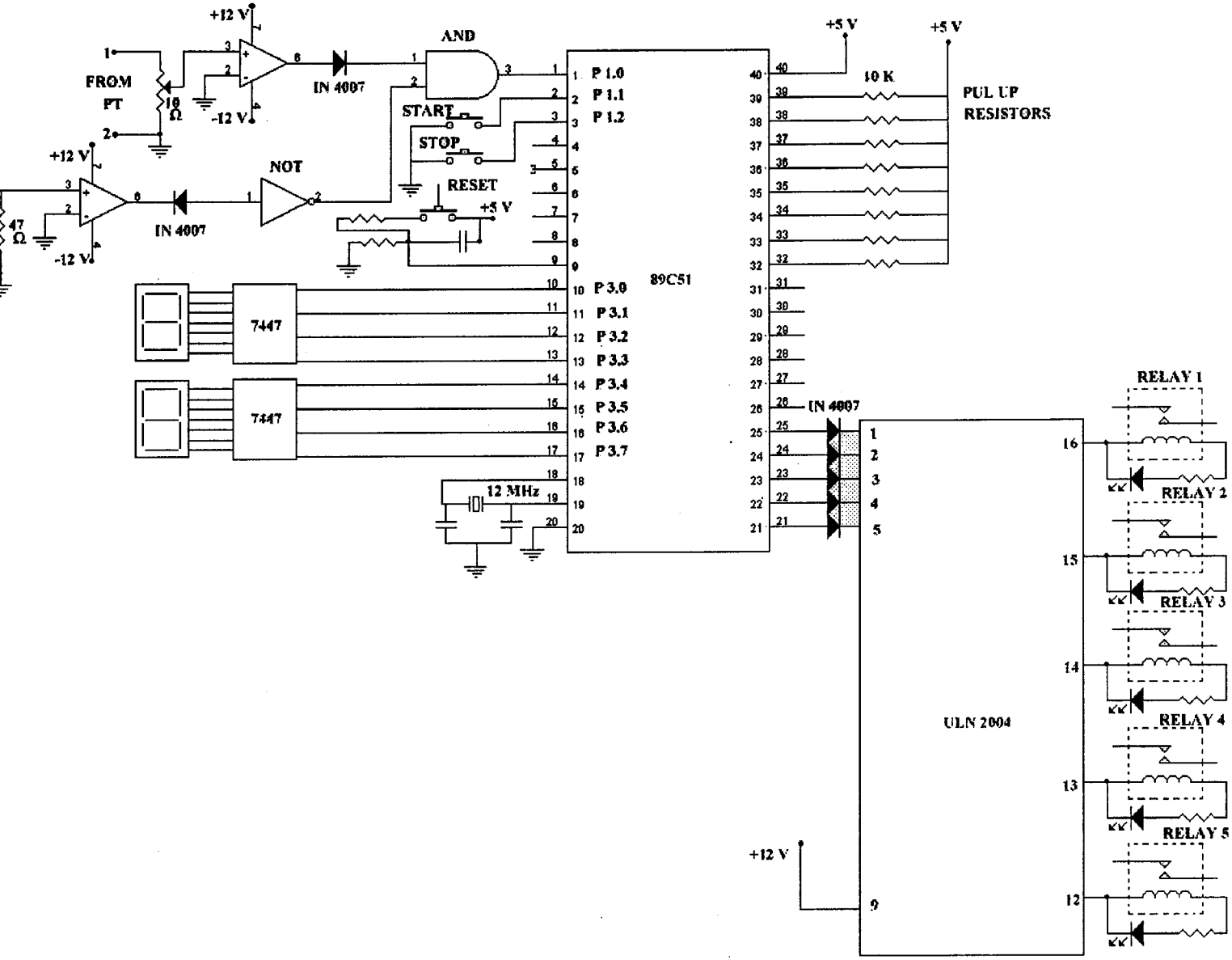
3.1.3.Intelligent power factor correction module

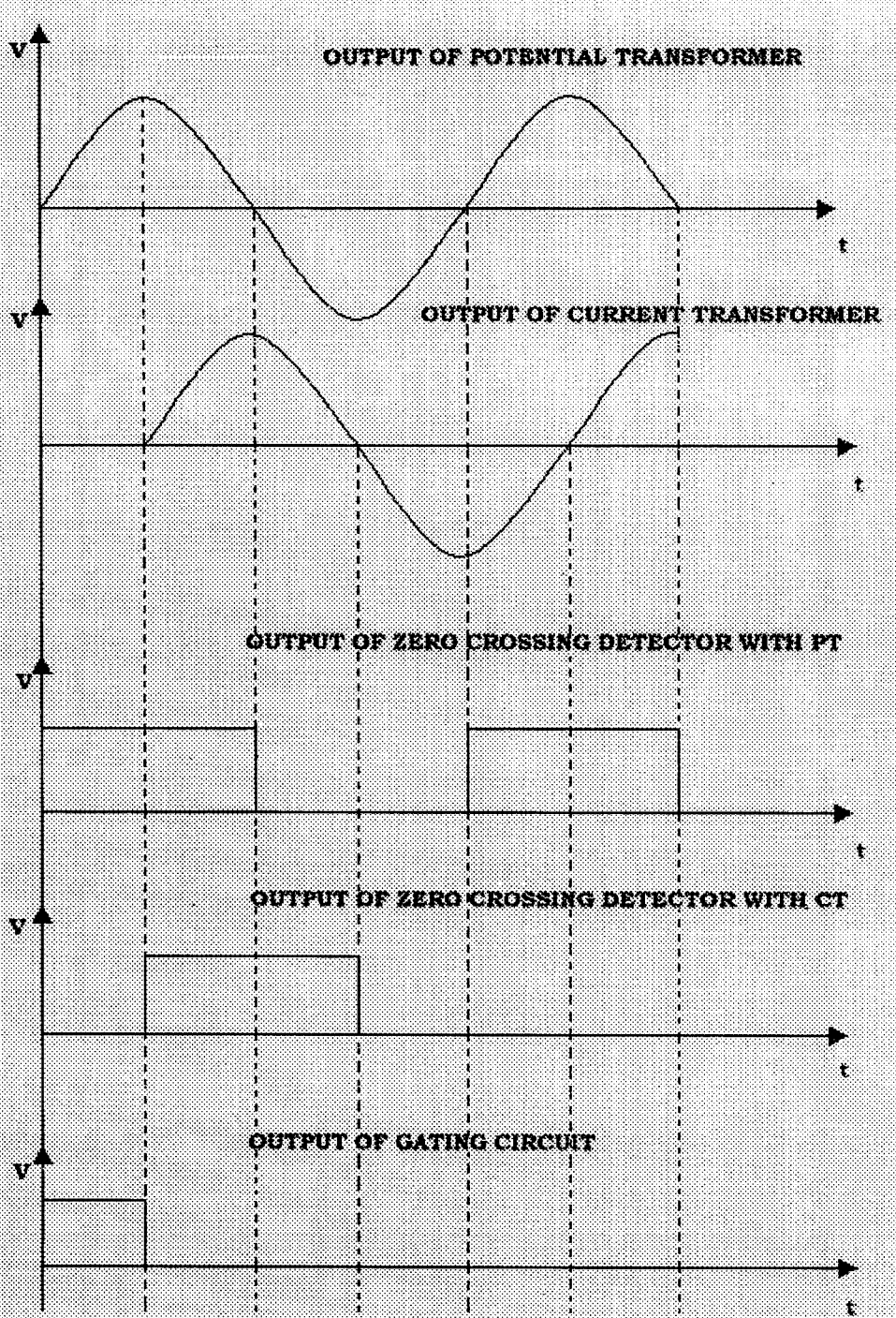
The Intelligent power factor correction module is shown in figure – 3.The control unit is based on the microelectronic technology, a well proven single board microcomputer unit which uses a microcontroller control circuit to get the input, process the data and make complex decisions to either connect or disconnect the capacitor bank and to provide signals to display the power factor value.

The control unit consists of a

- Microcontroller unit - 89C51
- Relay unit

NTROL CIRCUIT:




V
OUTPUT OF POTENTIAL TRANSFORMER
t
V
OUTPUT OF CURRENT TRANSFORMER
t
V
OUTPUT OF ZERO CROSSING DETECTOR WITH PT
t
V
OUTPUT OF ZERO CROSSING DETECTOR WITH CT
t
V
OUTPUT OF GATING CIRCUIT
t

OPERATION:

The potential transformer is connected across the input supply. The 230 voltage is applied to the primary winding. The secondary is designed for 6 volts. Hence the output of the 6 volts from the secondary winding is applied to the square wave converter.

The square wave converter converts the sine wave into square wave. The width of the square wave will depend on the reference voltage to the IC 741.

The current transformer is connected in series with the phase through a shunt resistance. The output of the secondary winding of the current transformer is applied to the square wave converters (I C 741). The output of the square wave converter is a square wave in the I C 741, the reference voltage is applied by through an regulator IC 7805.

The forward biased diode is connected to the output of the voltage square wave converter so the positive cycles are allowed by the diode to the AND gate (IC 7400)

Similarly reverse biased diode is connected to the output of the current square wave converter. So the negative cycles are allowed to the NOT gate. The NOT gate will convert the negative cycle into positive half cycle. The two output of the positive voltage and positive current from the logic gates are applied to the AND gate.

The output of the AND gate is one, when two inputs are high if the voltage and current are high the output is high. The AND gate output is high the microcontroller timer will starts to count the timing pulses from the crystal oscillator (12MHz). the micro controller calculate the load power factor according to the timing pulses.

If it is low compare to the reference value .the required number of capacitors will be added parallel to the load through a relay contactor. The output of the micro controller is not sufficient to drive or energize the relay coil, so the output of the micro controller is

amplified by the driver transistor (ULN 2004). The output of 2004 is applied to the relay coil.

The five numbers of LEDs connected across the relay coil. If the relay coils are energized the LEDs are glows, it is an indication of power factor improvement or the capacitor added in parallel to the load. Now the power factor will be improved automatically.

In our project, we are sensing the voltage and current through the potential transformer and current transformer. The signals taken from the potential transformer and current transformer is given as the inputs of the zero crossing detectors as shown in the circuit diagram.From the output of the zero crossing detector we have received the square wave signal according to the sine wave outputs of the potential transformer and current transformer.If the power factor is lagging ,the square wave form of current is lagging from the voltage square wave,the lagging angle is denoted by alpha . So to get the angle alpha we are introducing a gating circuit we have received resultant waveform of alpha. This wave form is directly connected

with the input and output port of the microcontroller 89C51.By the microcontrollers program routine we have calculated the length of the value alpha by using the internal software counter. The counter register value is compare with the look up table and according to the counter value the power factor is displayed.The display is connected with one port of the 89C51.To display the value we are sending the BCD value to the particular port. External to the microcontroller, a 7 segment driver is connected .This converts the BCD value is to seven segment controls.

In the AP controller section after getting the counter register value that value is compared with the lookup table 1.This will give the exact power factor value. After that the power factor value is compared with the lookup table 2.This lookup table gives the actual leading KVAR value according to the value the respective capacitors will be connected with the load.

The relays cannot be directly connected to the ports of the microcontroller because the driving capacity is very low (say 28mA per port) so to drive the relays darlington array(ULN2004) is used.The output of darlington array is connected with relays.

The start and stop push buttons are also sensible by a microcontroller after sensing the push button the microcontroller gives the signal to the relay 1 to turn ON the load or to turn-off.

For the operation of the automatic powerfactor control circuit needed the regulated power supply of +5v and +12v. These two regulated voltages can be obtained from the regulated ICs 7805 and 7812 respectively.

3.1.4. BENEFITS OF MICROCONTROLLER UNIT

The benefits of the high-speed microcontrollers that reduce power consumption can be summarized as follows:

- A high performance CPU allows the processor clock to be slowed, resulting in the same level of performance at less power. Alternatively, the performance of an existing system can be increased without increasing power consumption.

- The high-speed microcontroller incorporates features such as watchdog timers, additional UARTs, and precision reset circuits. External components consume more power.

- The introduction of two new low-power modes provides a low-power alternative to the idle mode. In addition to reducing current consumption, power management modes such as those used in the DS87C520 allow the processor to perform tasks such as polling while in a low state. Conventional 8051 architectures require the processor to operate at the maximum clock rate, even if only minimal processing power is required.

- The benefits of a programmable clock rate and high-performance core can be combined with the Stop mode to greatly reduce power consumption. Examples have been presented that show how energy consumption can be reduced by matching the clock rate of the device to the desired performance level.

3.1.5.AT89C51 Architecture

The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bittimer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external pro-gram and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups

and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I IL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source

current (I IL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I IL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51 as listed below: Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes.

Note, however, that one ALE pulse is skipped during each access to external Data Memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Port Pin Alternate Functions

P3.0 RXD (serial input port)

P3.1 TXD (serial output port)

P3.2 INT0 (external interrupt 0)

P3.3 INT1 (external interrupt 1)

P3.4 T0 (timer 0 external input)

P3.5 T1 (timer 1 external input)

P3.6 WR (external data memory write strobe)

P3.7 RD (external data memory read strobe)

PSEN

Program Store Enable is the read strobe to external pro-gram memory.

When the AT89C51 is executing code from external pro-gram memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external pro-gram memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to V CC for internal program executions. This pin also receives the 12-volt programming enable volt-age (VPP) during Flash programming, for parts that require
12-volt VPP .

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left

unconnected while XTAL1 is driven as shown in Figure 2.There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maxi-mum voltage high and low time specifications must be

observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this

can be terminated by any enabled interrupt or by a hardware reset. It

should be noted that when idle is terminated by a hardware reset , the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power-down Mode

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode isterminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V CC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with

the current logic level at that pin in order for the device to function properly.

3.1.6.Features of Micro controller

- Compatible with MCS-51 ™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM

- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

3.1.7.Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

Absolute Maximum Ratings

Operating Temperature..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

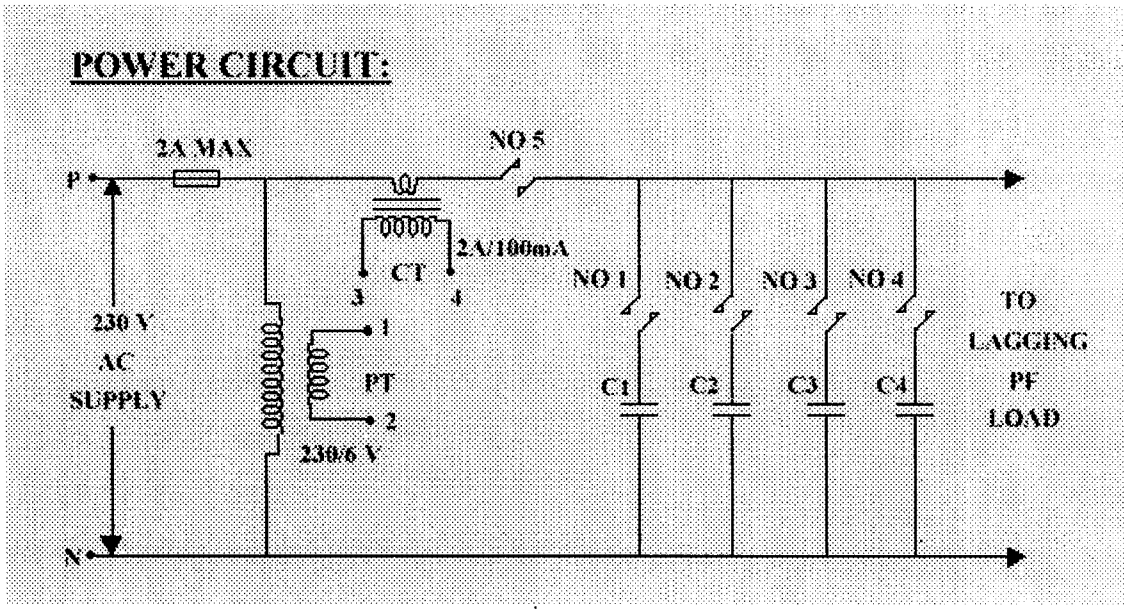
Voltage on Any Pin

with Respect to Ground .....-1.0V to +7.0V

Maximum Operating Voltage 6.6V

DC Output Current..... 15.0 Ma

3.2.Power Module



The power module shown in figure consists of the capacitor banks with switching devices. The suitable value of capacitor in the bank is switched ON depending upon signal from the controller.

SOFTWARE

3.1.9.Software

```
 org 0000h

start:  mov p0,#0ffh
        mov p1,#0ffh
        mov p2,#00h
        mov p3,#00h
        jnb p1.0,motstt
        sjmp start


motstt: setb p2.4
        jnb p1.1,start
        acall delay2
        mov p3,#066h
        setb p2.3
        setb p2.2
        setb p2.1
        setb p2.0
        jnb p1.1,start
        acall delay3
        mov p3,#07h
        clr p2.0
```

```
run:   jnb p1.1,start
       acall delay2
       mov p3,#07fh
       clr p2.1
       clr p2.2
       jnb p1.1,start
       acall delay2
       mov p3,#067h
       setb p2.1
       clr p2.3
       jnb p1.1,start
       acall delay2
       mov p3,#067h
       clr p2.0
       clr p2.1
       clr p2.2
       clr p2.3
       setb p2.0
       setb p2.2
       jnb p1.1,start
       acall delay3
       mov p3,#07fh
       clr p2.0
       clr p2.1
       clr p2.2
```

```
 clr p2.3
setb p2.0
setb p2.2
setb p2.3
jnb p1.1,start
acall delay4
mov p3,#067h
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.2
setb p2.3

acall delay2
mov p3,#067h
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.0
setb p2.1
acall delay3
mov p3,#067h
clr p2.0
```

```
 clr p2.1
clr p2.2
clr p2.3

setb p2.1
setb p2.2
setb p2.0
acall delay4
mov p3,#07fh
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.1
setb p2.3
acall delay2
mov p3,#067h
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.1
setb p2.2
setb p2.3
acall delay4
```

```
mov p3,#07fh
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.0
acall delay2
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.1
setb p2.0
acall delay3
mov p3,#067h
clr p2.0
clr p2.1
clr p2.2
clr p2.3
setb p2.0
setb p2.1
setb p2.2
mov p3,#07fh
acall delay2
ljmp run
```

```
delay2: mov r0,#82h
        mov r1,#02h
        acall timer
        mov r0,#05h
        mov r1,#01h
        acall timer
        ret
delay3: mov r0,#82h
        mov r1,#03h
        acall timer
        mov r0,#05h
        mov r1,#01h
        acall timer
        ret
delay4: mov r0,#82h
        mov r1,#04h
        acall timer
        mov r0,#05h
        mov r1,#01h
        acall timer
        ret
timer:  anl tcon,#0cfh
        anl tmod,#0f2h
        mov th0,#010h
        setb tcon.4
```

```
        jbc tf0,count
count:  clr tcon.4
        djnz r0,timer
        mov r0,#82h
        djnz r1,timer
        ret

        end
```

4. System operation

The line voltage and the line current are sensed by the potential transformer and the current transformer respectively. In this two outputs from the transformer are converted into square wave form in the comparator. The output of the comparators is applied to the logic circuit. The logic circuits are used to allow the positive half cycle from the voltage and negative half cycle of the current wave forms, the negative half cycle current wave will be converted into positive half cycle by the NOT gate. The two voltage and current wave forms are applied to the AND gate. Whenever the AND gate output is one the timer of the micro controller will count the timing pulses from the crystal oscillator. The micro controller senses the micro controller.

If it is low as compare to reference value, it will drive or energize the required number of relays. The control circuit consists of relays. The capacitor bank is connected across the load through a relay N.O. contact. If the relay coils are energized the N.O. contact

of the relays will be closed. Hence the capacitors are added to the load in parallel. Now the power factor will be improved automatically.

5.Conclusion

In this project ,89C51 has been used for the power factor control of the single phase induction motor by hardware implementation and software program to improve the operating power factor at unity by proper switching of the capacitors.The controller board designed cannot used only for this project but also for later other research.

REFERENCE

REFERENCES

1. E.Muljadi and Y.Zhao," Adjustable Ac capacitor for a single phase Induction motor",IEEE(Industrial appln society)/IAS annual meeting, October 1991.

2. T.A.Latent Maier,"Single phase Induction motor with an electronically controlled capacitors",IEEE(Industrial appln society) Volume 27 , Jan 1991.

3. R.K.Pongiannan et.al,"A High frequency energy efficient single phase open well motor pump system using efficient controller"in the national conference proceeding conducted by N.S.S college of engg Palakkad, Jan 2003.

4. R.K.Pongiannan and V.R.Ravi, AICTE-TAPTEC project report titled "computerised test rig for monoblock and submersible pumps".

5. T.J.E.Miller,"Reactive power control in electric systems",1982.

6. M.G.Say ,"The Performance and design of alternating current machines",edition 1983.

7. Roy Choudary," Linear Integrated Circuits ", NewDelhi 1994.

8. A.K.Shawney ,"Measurements and instrumentation".

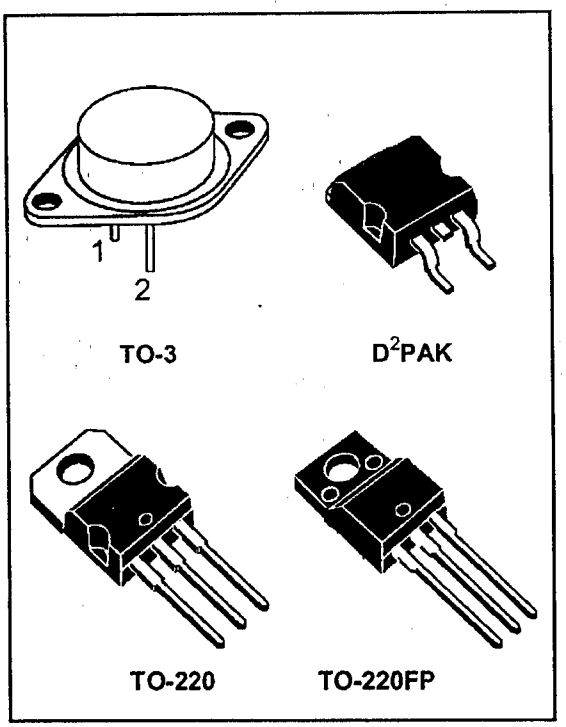
9. www.atmel.com

APPENDIX

L7800 SERIES

POSITIVE VOLTAGE REGULATORS

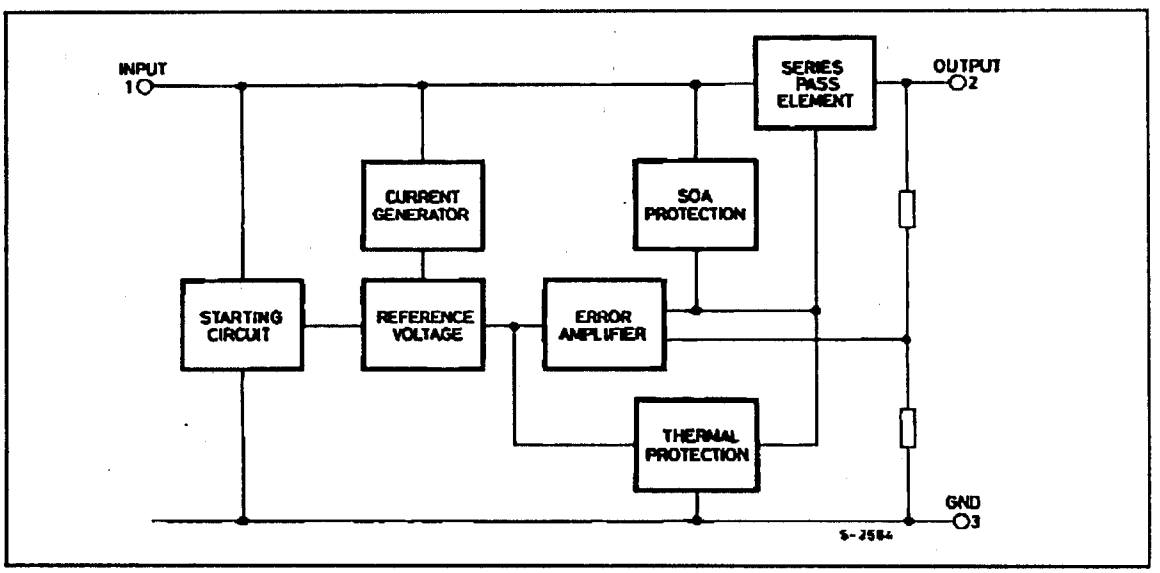
- OUTPUT CURRENT UP TO 1.5 A
- OUTPUT VOLTAGES OF 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSITION SOA PROTECTION



DESCRIPTION

The L7800 series of three-terminal positive regulators is available in TO-220 TO-220FP TO-3 and D^2PAK packages and several fixed output voltages, making it useful in a wide range of applications.These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



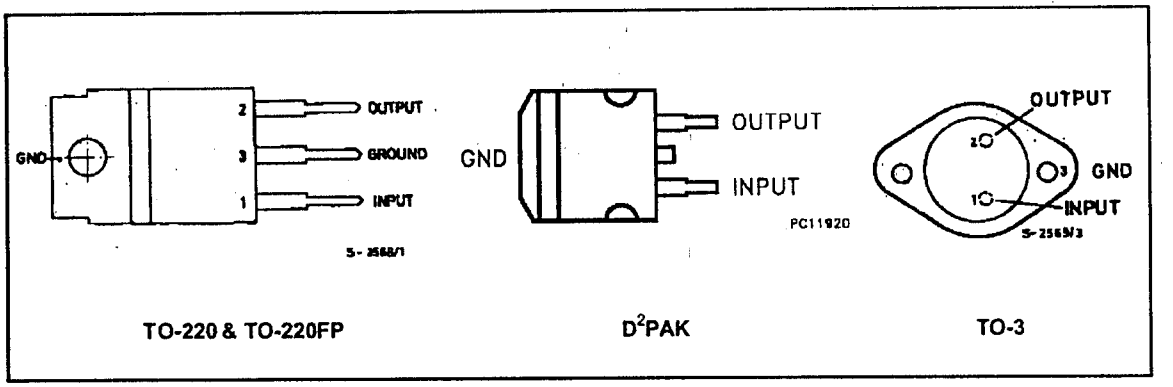
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_O = 5 to 18V) (for V_O = 20, 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature Range (for **L7800**) (for **L7800C**)	-55 to 150 0 to 150	°C °C
T_{stg}	Storage Temperature Range	-65 to 150	°C

THERMAL DATA

Symbol	Parameter	D^2PAK	TO-220	TO-220FP	TO-3	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	3	3	5	4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	62.5	50	60	35	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

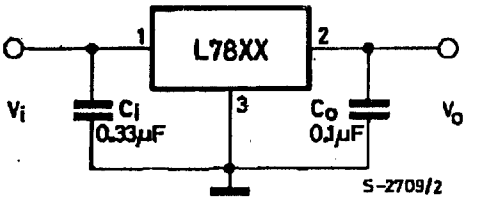


TO-220 & TO-220FP | D^2PAK | TO-3

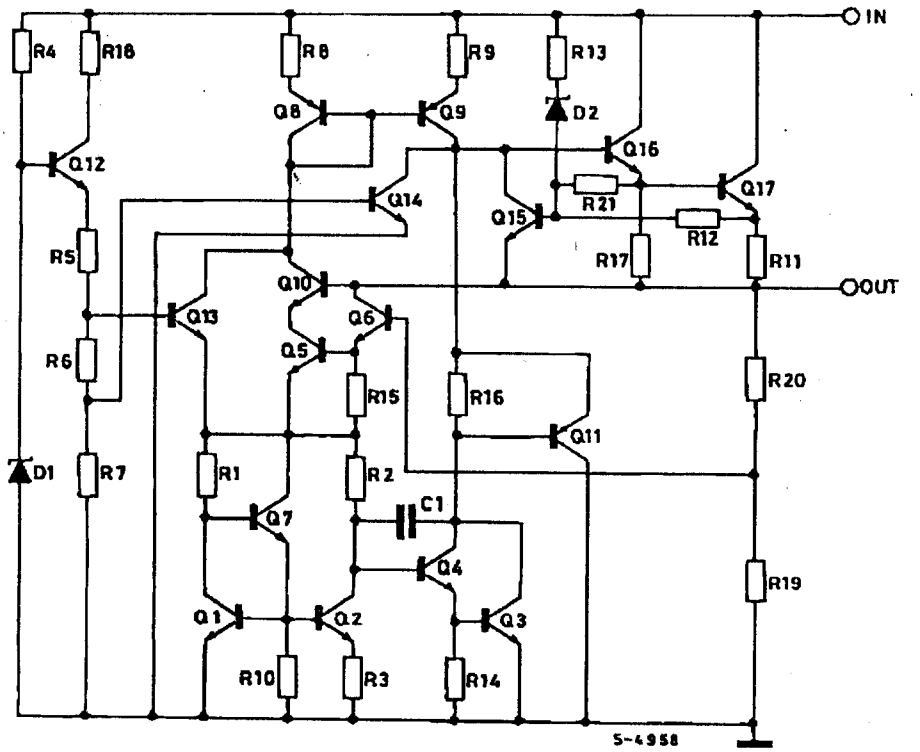
Type	TO-220	D^2PAK (*)	TO-220FP	TO-3	Output Voltage
L7805				L7805T	5V
L7805C	L7805CV	L7805CD2T	L7805CP	L7805CT	5V
L7852C	L7852CV	L7852CD2T	L7852CP	L7852CT	5.2V
L7806				L7806T	6V
L7806C	L7806CV	L7806CD2T	L7806CP	L7806CT	6V
L7808				L7808T	8V
L7808C	L7808CV	L7808CD2T	L7808CP	L7808CT	8V
L7885C	L7885CV	L7885CD2T	L7885CP	L7885CT	8.5V
L7809C	L7809CV	L7809CD2T	L7809CP	L7809CT	9V
L7812				L7812T	12V
L7812C	L7812CV	L7812CD2T	L7812CP	L7812CT	12V
L7815				L7815T	15V
L7815C	L7815CV	L7815CD2T	L7815CP	L7815CT	15V
L7818				L7818T	18V
L7818C	L7818CV	L7818CD2T	L7818CP	L7818CT	18V
L7820				L7820T	20V
L7820C	L7820CV	L7820CD2T	L7820CP	L7820CT	20V
L7824				L7824T	24V
L7824C	L7824CV	L7824CD2T	L7824CP	L7824CT	24V

(*) AVAILABLE IN TAPE AND REEL WITH "-TR" SUFFIX

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameter

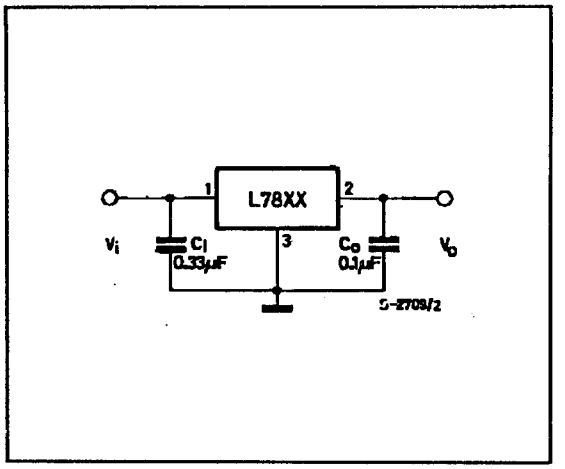


Figure 2 : Load Regulation.

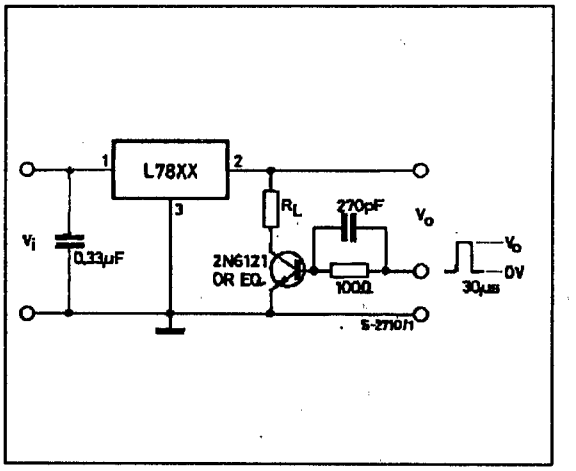
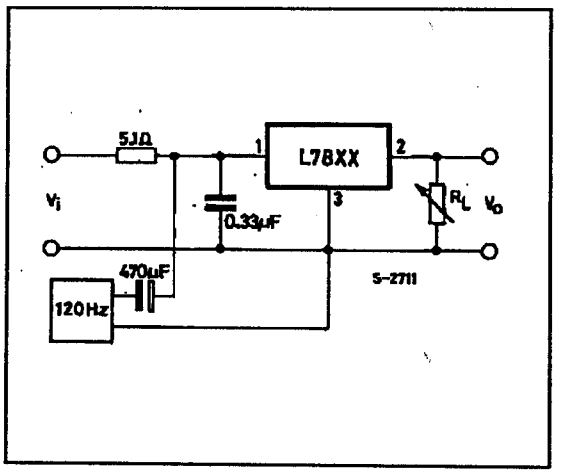


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS FOR L7805 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.8	5	5.2	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 20 V	4.65	5	5.35	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	50 25	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 25	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.6		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	68			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7806 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 15V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.75	6	6.25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 9 to 21 V	5.65	6	6.35	V
ΔV_o*	Line Regulation	V_i = 8 to 25 V T_j = 25 °C V_i = 9 to 13 V T_j = 25 °C			60 30	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 30	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 9 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.7		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 9 to 19 V f = 120 Hz	65			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7815 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 23V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	14.4	15	15.6	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 18.5 to 30 V	14.25	15	15.75	V
ΔV_o*	Line Regulation	V_i = 17.5 to 30 V T_j = 25 °C V_i = 20 to 26 V T_j = 25 °C			150 75	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			150 75	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 18.5 to 30 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		1.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 18.5 to 28.5 V f = 120 Hz	60			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7818 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 26V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	17.3	18	18.7	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 22 to 33 V	17.1	18	18.9	V
ΔV_o*	Line Regulation	V_i = 21 to 33 V T_j = 25 °C V_i = 24 to 30 V T_j = 25 °C			180 90	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			180 90	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 22 to 33 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		2.3		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 22 to 32 V f = 120 Hz	59			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		22		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7820 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 28V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	19.2	20	20.8	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 24 to 35 V	19	20	21	V
ΔV_o*	Line Regulation	V_i = 22.5 to 35 V T_j = 25 °C V_i = 26 to 32 V T_j = 25 °C			200 100	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			200 100	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 24 to 35 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		2.5		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 24 to 35 V f= 120 Hz	58			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		24		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7824 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 33V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	23	24	25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 28 to 38 V	22.8	24	25.2	V
ΔV_o*	Line Regulation	V_i = 27 to 38 V T_j = 25 °C V_i = 30 to 36 V T_j = 25 °C			240 120	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			240 120	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 28 to 38 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		3		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_o
SVR	Supply Voltage Rejection	V_i = 28 to 38 V f= 120 Hz	56			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		28		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7805C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.8	5	5.2	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 7 to 20 V	4.75	5	5.25	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	100 50	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 50	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 7 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1.1		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		40		µV
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	62			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		750		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7852C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.0	5.2	5.4	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 20 V	4.95	5.2	5.45	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	105 52	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			105 52	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 7 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-1.0		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		42		µV
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	61			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		750		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7806C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 11V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.75	6	6.25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 21 V	5.7	6	6.3	V
ΔV_o*	Line Regulation	V_i = 8 to 25 V T_j = 25 °C V_i = 9 to 13 V T_j = 25 °C			120 60	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			120 60	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-0.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		45		µV
SVR	Supply Voltage Rejection	V_i = 9 to 19 V f = 120 Hz	59			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		550		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

ELECTRICAL CHARACTERISTICS FOR L7808C (refer to the test circuits, T_j = 0 to 125 °C, V_i = 14V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	7.7	8	8.3	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 10.5 to 25 V	7.6	8	8.4	V
ΔV_o*	Line Regulation	V_i = 10.5 to 25 V T_j = 25 °C V_i = 11 to 17 V T_j = 25 °C			160 80	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			160 80	mV mV
I_d	Quiescent Current	T_j = 25 °C			8	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 10.5 to 25 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		-0.8		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		52		µV
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5 V f = 120 Hz	56			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
R_o	Output Resistance	f = 1 KHz		16		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		450		mA
I_{scp}	Short Circuit Peak Current	T_j = 25 °C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulce testing with low duty cycle is used.

eatures

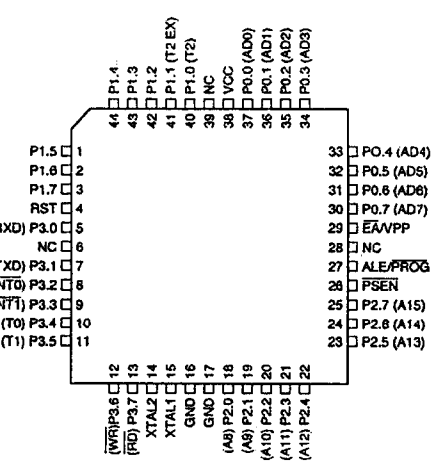
- Compatible with MCS-51™ Products
- K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- ully Static Operation: 0 Hz to 24 MHz
- hree-level Program Memory Lock
- 28 x 8-bit Internal RAM
- 2 Programmable I/O Lines
- wo 16-bit Timer/Counters
- ix Interrupt Sources
- rogrammable Serial Channel
- ow-power Idle and Power-down Modes

escription

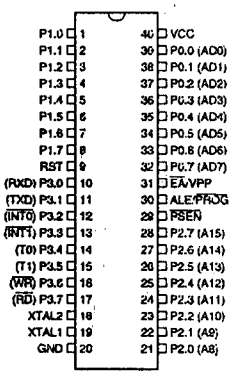
e AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K tes of Flash programmable and erasable read only memory (PEROM). The device manufactured using Atmel's high-density nonvolatile memory technology and is mpatible with the industry-standard MCS-51 instruction set and pinout. The on-chip ash allows the program memory to be reprogrammed in-system or by a conven- nal nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ighly-flexible and cost-effective solution to many embedded control applications.

n Configurations

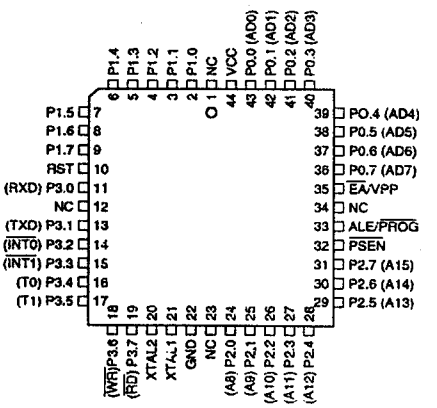
PQFP/TQFP



PDIP



PLCC

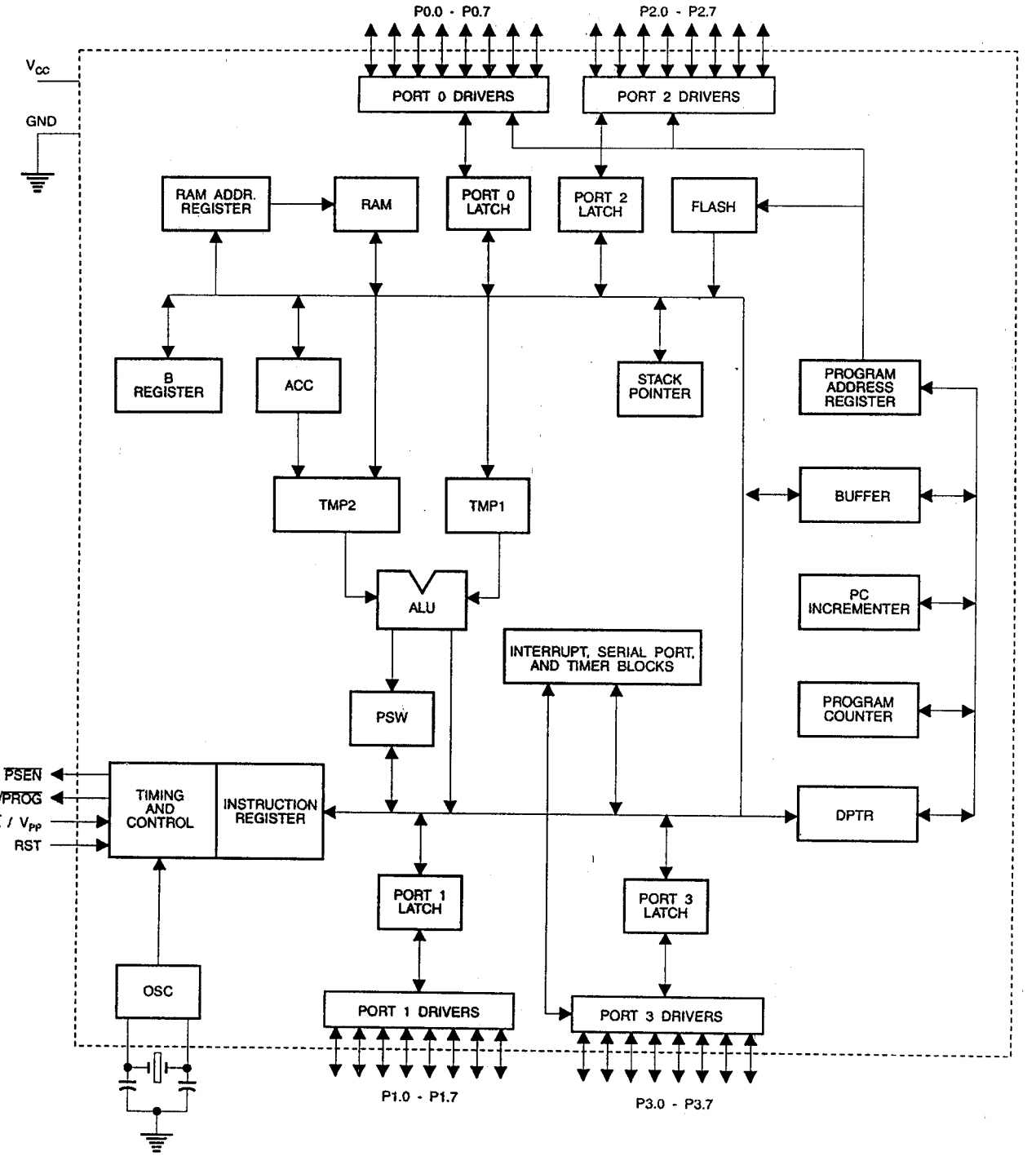


8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
/PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

e AT89C51 provides the following standard features: 4K es of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit er/counters, a five vector two-level interrupt architecture, ull duplex serial port, on-chip oscillator and clock cir- try. In addition, the AT89C51 is designed with static logic operation down to zero frequency and supports two ftware selectable power saving modes. The Idle Mode ops the CPU while allowing the RAM, timer/counters, rial port and interrupt system to continue functioning. The ower-down Mode saves the RAM contents but freezes e oscillator disabling all other chip functions until the next rdware reset.

in Description

CC

upply voltage.

ND

round.

ort 0

ort 0 is an 8-bit open-drain bi-directional I/O port. As an utput port, each pin can sink eight TTL inputs. When 1s re written to port 0 pins, the pins can be used as high- npedance inputs.

ort 0 may also be configured to be the multiplexed low- rder address/data bus during accesses to external pro- ram and data memory. In this mode P0 has internal ullups.

ort 0 also receives the code bytes during Flash program- ing, and outputs the code bytes during program erification. External pullups are required during program erification.

ort 1

ort 1 is an 8-bit bi-directional I/O port with internal pullups. he Port 1 output buffers can sink/source four TTL inputs. Vhen 1s are written to Port 1 pins they are pulled high by ne internal pullups and can be used as inputs. As inputs, ort 1 pins that are externally being pulled low will source urrent (I_{IL}) because of the internal pullups.

ort 1 also receives the low-order address bytes during lash programming and verification.

ort 2

ort 2 is an 8-bit bi-directional I/O port with internal pullups. he Port 2 output buffers can sink/source four TTL inputs. Vhen 1s are written to Port 2 pins they are pulled high by ne internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

ılse is skipped during each access to external Data emory.

desired, ALE operation can be disabled by setting bit 0 of FR location 8EH. With the bit set, ALE is active only dur- g a MOVX or MOVC instruction. Otherwise, the pin is eakly pulled high. Setting the ALE-disable bit has no fect if the microcontroller is in external execution mode.

SEN

ogram Store Enable is the read strobe to external pro- am memory.

hen the AT89C51 is executing code from external pro- am memory, $\overline{PSEN}$ is activated twice each machine cle, except that two $\overline{PSEN}$ activations are skipped during ch access to external data memory.

/VPP

ternal Access Enable. $\overline{EA}$ must be strapped to GND in der to enable the device to fetch code from external pro- am memory locations starting at 0000H up to FFFFH. te, however, that if lock bit 1 is programmed, $\overline{EA}$ will be ernally latched on reset.

$\overline{A}$ should be strapped to V_{CC} for internal program ecutions.

is pin also receives the 12-volt programming enable volt- e (V_{PP}) during Flash programming, for parts that require -volt V_{PP}.

AL1

ut to the inverting oscillator amplifier and input to the ernal clock operating circuit.

AL2

tput from the inverting oscillator amplifier.

scillator Characteristics

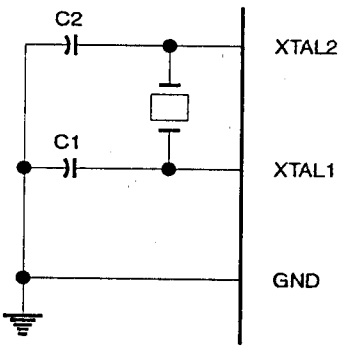
AL1 and XTAL2 are the input and output, respectively, an inverting amplifier which can be configured for use as on-chip oscillator, as shown in Figure 1. Either a quartz stal or ceramic resonator may be used. To drive the vice from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

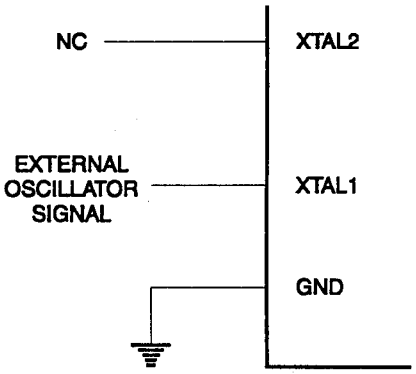


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

tatus of External Pins During Idle and Power-down Modes

ode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
le	Internal	1	1	Data	Data	Data	Data
le	External	1	1	Float	Data	Address	Data
ower-down	Internal	0	0	Data	Data	Data	Data
ower-down	External	0	0	Float	Data	Data	Data

gure 2. External Clock Drive Configuration



ower-down Mode

the power-down mode, the oscillator is stopped, and the struction that invokes power-down is the last instruction ecuted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ock Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled