MICROCONTROLLER BASED HIGH FREQUENCY INVERTER

Project Report
2002-2003

Submitted by

Sundararajan.N
Sathish.R
Prakash.P
Arulnandhisivam.V

Guided by

Mr.K.Rajan,M.E.,
Assistant Professor,
Department of EEE.

2002-2003

In partial fulfillment of the requirements for the award of the degree of **Bachelor of Engineering** in **Electrical and Electronics Engineering** branch Of Bharathiar University, Coimbatore.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
Kumaraguru College of Technology
COIMBATORE-641006.

Estd. 1984

ISO 9001:20

ACKNOWLEDGEMENT

We are very fortunate to have an affectionate, eminent and friendly guide in Asst. Professor K.Rajan M.E in Electrical and Electronics Engineering Department. We are immensely pleased by the valuable suggestions and excellent guidance given by him. We are highly thankful to him for all the help and cooperation rendered by him.

We are highly grateful to Dr.T.M.Kameswaran B.E., M.Sc(Engg.), the professor and head of Electrical and Electronics engineering department for his encouragement and support. We also express our sincere thanks to our beloved Asst. Professor V.Duraisamy for his continued support for our efforts.

We are lucky to be the students of Kumaraguru College of Technology and our distinguished Principal Dr.K.K. Padmanaban BSc(Engg)., M.Tech.,Ph.D., under his able guidance we were also able to acquire good knowledge and experience in this great institution. We express our sincere thanks and gratitude to our great leader who gave us an opportunity to carry out this project.

We also thank our faculty members for their kind co-operation and great help. A very special thanks to all our friends who helped us complete the project successfully. Lastly we thank god almighty for giving us strength and blessings throughout this endeavor.

Synopsis

The demand for control of electric power for motor drive systems and industrial applications has existed for many years. With the use of power electronic devices control of many applications has become easier.

An inverter is a power electronic system that converts a variable or fixed DC supply into a variable ac output. Inverters find wide applications in areas such as variable speed ac motor drives, induction heating, standby power supplies etc.

In our project we have implemented the basic inverter in a high frequency configuration. High frequency power has several advantages over the conventional power system in the fact that it helps to improve overall system efficiency, speed of operation and reducing the power elements used. Currently a maximum frequency of 250 Hz is can be generated using our hardware. Further improvements like increasing the maximum frequency can be easily done by minimal changes in hardware.

Contents

Chapter 1 - Introduction

Introduction

Inverters are power electronic systems that convert a variable or fixed dc supply into a variable ac output. Inverters can be widely classified into two types :

(i) Single phase inverters.

(ii) Three phase inverters.

Each type can use controlled turn-on and turn-off switches likeBJTs, MOSFETs, IGBTs, MCTs, or GTOs. An inverter is called a voltage source inverter if the input voltage remains constant and a current source inverter if the input current is maintained constant.

The high frequency inverter consists of five basic segments. They are:

(i) Power supply segment

(ii) AC-DC converter

(iii) Inverter segment with gate drive

(iv) Microcontroller with isolation segment

(v) Display segment

1.1 Power supply :

The power supply requirements for all the segments has been considered and the power supply suitably designed. There are a total of six separate DC regulated power supplies in this segment supplying the MOSFET gate drive circuit, the microcontroller and the display segment. The power supply uses a standard diode rectifier configuration along with a voltage regulator IC(LM 78xx) to produce a ripple free output.

1.2 AC-DC converter :

The input for an inverter can be variable or fixed dc supply. Here a fixed dc supply is obtained by using a diode rectifier and s filtering capacitor to provide a constant voltage source.

1.3 Inverter segment with gate drive :

The inverter configuration is achieved by using a MOSFET H-Bridge. The MOSFETs used are standard N-Channel power MOSFETs. The MOSFETs are provided with separate floating grounds from separate sources to avoid 'Cross Conduction'. The gate drive is a simple, low impedance 'Totem Pole' TTL drive. The gate pulses to the MOSFETs are Pulse width modulated signals used to eliminate harmonics in the output stage.

1.4 Microcontroller with Isolation :

The control circuitry utilizes the services of the RISC microcontroller. The controller used here is the PIC 16F877 manufactured by microchip. The microcontroller is isolated from the power devices by using opto isolators. These provide excellent protection for the controller from the high voltages developed in the inverter stage.

1.5 Display segment :

The frequency set by the user is displayed using standard seven seven segment displays. The drive for these display segments is obtained from a BCD to Seven Segment display decoder/driver(74LS47). The decoder IC accepts bcd data and decodes them to be displayed in the display segments.

1.6 About High Frequency Power :

With the advent of power semiconductors many different frequency changers, namely static frequency changers have increasingly been employed in most industry and recently in homes and offices.Especially high frequency power can find applications such as motor drives,induction heating and fluorescent lighting.

By operating power systems at high frequency, the system can be made compact because of the large reduction in the size and weight of the transformers, reactors, capacitors and circuit breakers. Use of high frequency also speeds up system speed and provides high quality power. Moreover newly developed materials like amorphous metal and low dielectric loss materials can be more effectively than in a 50/60Hz power system.

It is important to select a proper frequency,which must take into account not only the requirements for much higher frequency from utilities but also the limits of the power elements. The following are the significant advantages to the utilization equipment that a high frequency system provides over a conventional 50/60Hz system.

- ✓ Large reduction in the size of transformers, reactors and electric machines, consequently resulting in improved efficiency and reduced cost of the electrical apparatus.

- ✓ Iron losses can be significantly reduced if amorphous materials are used for construction of reactors and transformer cores.
- ✓ Saving dielectric materials of capacitors, which make the capacitors compact and lower cost. Therefore loads with lower power factors can be economically used.
- ✓ The power source can offer an uninterrupted power supply by connecting some energy storage units to the power converter.
- ✓ Because the frequency is several times the conventional frequency the speed of electrical systems can be improved.

1.7 APPLICATIONS OF HIGH FREQUENCY POWER :

(a) High Speed Motors :

High speed motors find applications in various high power applications such as turbine compressors, and blowers for pipelines. Most of these high speed motors will have to use high frequency power to operate at such a large scale. These motors are compact and maintenance free.

(b)Induction Heating :

In Iron and Steel industry, high frequency power has been widely used for melting of cast steel and alloy in induction furnace, heating of steel bars and heat treatment of steel tubing and pipes by offering advantages of high efficiency, cleanliness, compactness of equipment and ease of control.

(c)Lighting Apparatus :

The use of high frequency supply to fluorescent and mercury lighting systems will result in dramatic reduction in size of size and improve system stability and efficiency. Moreover dimming of the lighting system becomes more easier and economical.

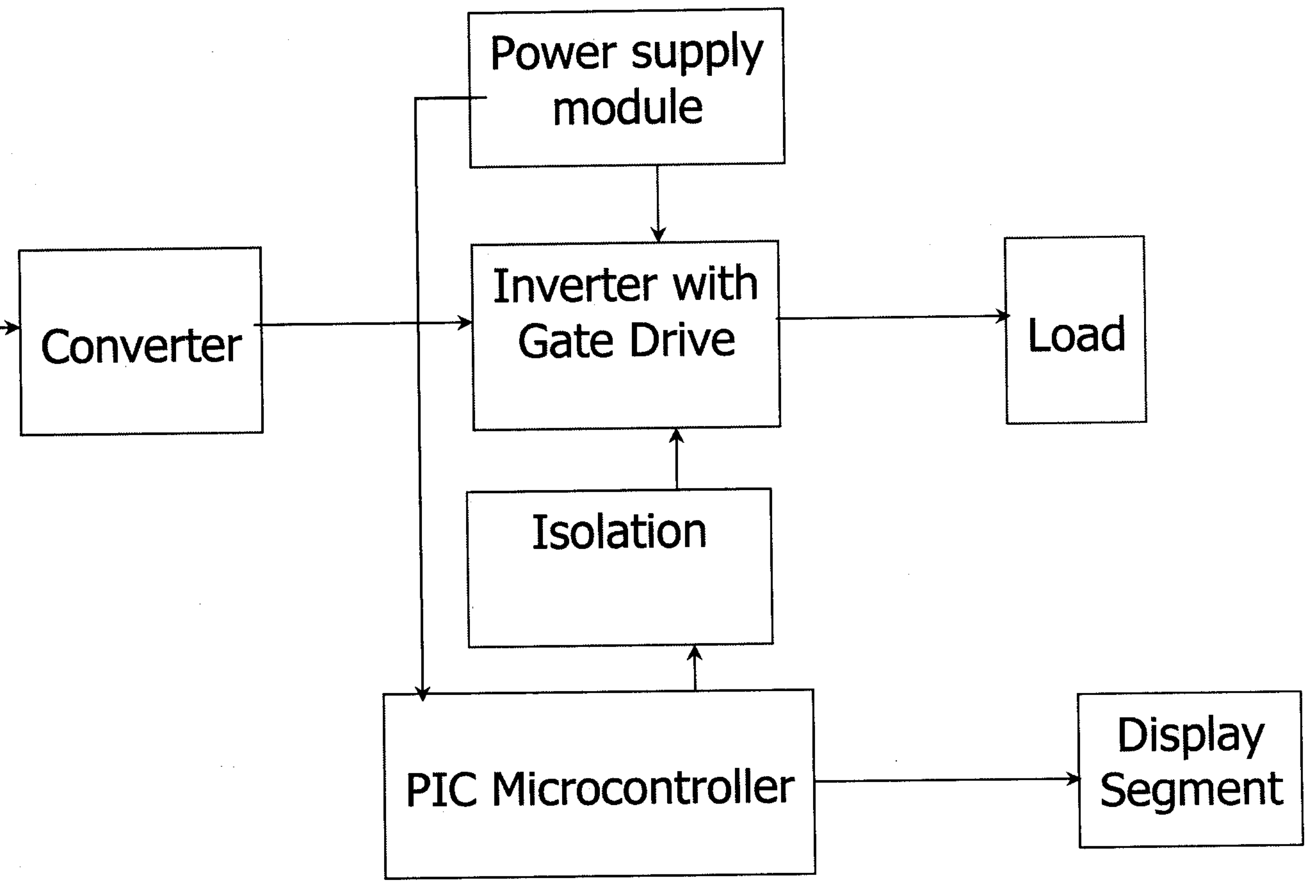
(d)Quick Response DC Power Supply :

It is clear that high power and quick response dc power supply using thyristor converter is available only in high frequency power. Particularly quick response control of dc power supply is more easier.

Chapter 2 – General Block Diagram

Basic Block Diagram

Fig 1



Chapter 3 – Power Supply

3.1 Overview :

The power supply segment consists of six separate regulated power supplies. The design of six separate supplies was necessitated by the fact that the gate drives to the MOSFETs required separate floating grounds and that the microcontroller requires a different value of dc voltage for its operation.

The regulated power supply consists of the following key components:

(i) Diode rectifier

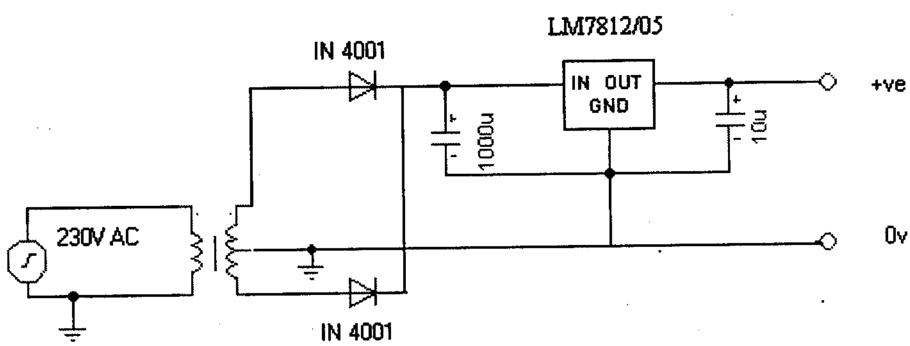
(ii) Capacitive filter at the input stage of the regulator

(iii) Regulator IC(LM 78xx series)

(iv) Capacitive filter at the output stage to reduce ripples.

The schematic of the individual power supplies in the module is shown below :

Fig 2



3.2 Features of LM78XX :

One of the critical components used in the circuit is the LM 78xx series regulator IC. Some of the key features of the IC are:

- Effective improvement in output impedance of two orders of magnitude.
- Output current of over 1.5A.
- Voltage tolerance of 5%.
- Internal thermal overload protection.
- Internal short circuit current limitation.
- Linear positive regulator.

Chapter 4 – Power Devices

The choice of the power element used in the inverter is done under the following constraints :

(i) High switching must be possible.

(ii) Ease of gate drive.

Various choices are available for the power element to be used among which are SCRs, GTOs, IGBTs, SITs, BJTs , MOSFETs etc.. Among these options the thyristor family of devices is not suited for high switching speeds due to their commutation and device protection constraints. Among the power transistor family MOSFETs(Metal Oxide Semiconductor Field Effect Transistor) and IGBTs(Insulated Gate Bipolar transistors) are the best possible options. MOSFETs among the two are the ideal choice for high frequency inverters.

4.1 MOSFET Specifications :

A power MOSFET is a voltage contolled device and requires only a small amount of input current. The switching speed is very high and the switching times are in the order of nanoseconds. MOSFETs are of two types, p-channel and n-channel. Either of these types can be used in the inverter but p-channel type is not preferable due to its considerable switching and conduction losses which is much higher than that of the n-channel type at high frequencies. The following requirements are essential for a switching device such as a MOSFET used in an inverter:

❖ Dynamic dv/dt rating.

- Repetitive avalanche rating.
- Fast switching.
- Ease of gate drive.
- Ease of paralleling.
- Low ON resistance.
- Low thermal resistance.
- Rugged device design.

4.2 MOSFET Parameters:

(i) Breakdown Voltage :

Breakdown voltage is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together.

(ii) Transconductance :

Transconductance, gfs, is a measure of the sensitivity of drain current to changes in gate-source bias. This parameter is normally quoted for a Vgs that gives a drain current equal to about one half of the maximum current rating value and for a VDS that ensures operation in the constant current region. Transconductance is influenced by gate width, which increases in proportion to the active area as cell density increases.

(iii) Threshold Voltage :

Threshold voltage, Vth, is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions. Vth is usually measured at a drain-source current of 250μA.

(iv) Diode Forward Voltage :

The diode forward voltage, VF, is the guaranteed maximum forward drop ofthe body-drain diode at a specified value of source current.

(v) Power Dissipation :

The maximum allowable power dissipation that will raise the die allowable when the case temperature is held at 250C is important. It is give by Pd where:

$$P_d = \frac{T_{jmax-25}}{R_{thJC}}$$

(vi) dv/dt Capability :

Peak diode recovery is defined as the maximum rate of rise of drain-source voltage allowed, i.e., dv/dt capability. If this rate is exceeded then the voltage across the gate-source terminals may become higher than the threshold voltage of the device, forcing the device into current conduction mode, and under certain conditions a catastrophic failure may occur.

Chapter 5 – Gate Drives

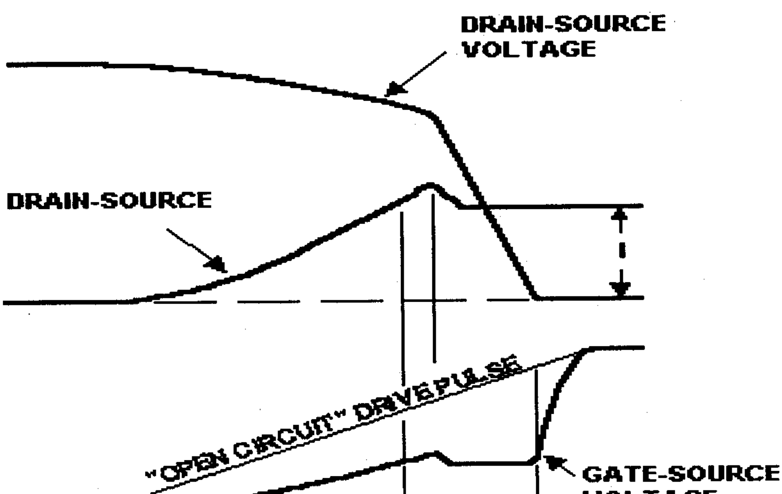
5.1 Requirements :

To turn on a power MOSFET a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the "saturation" (fully enhanced) region. The best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses.

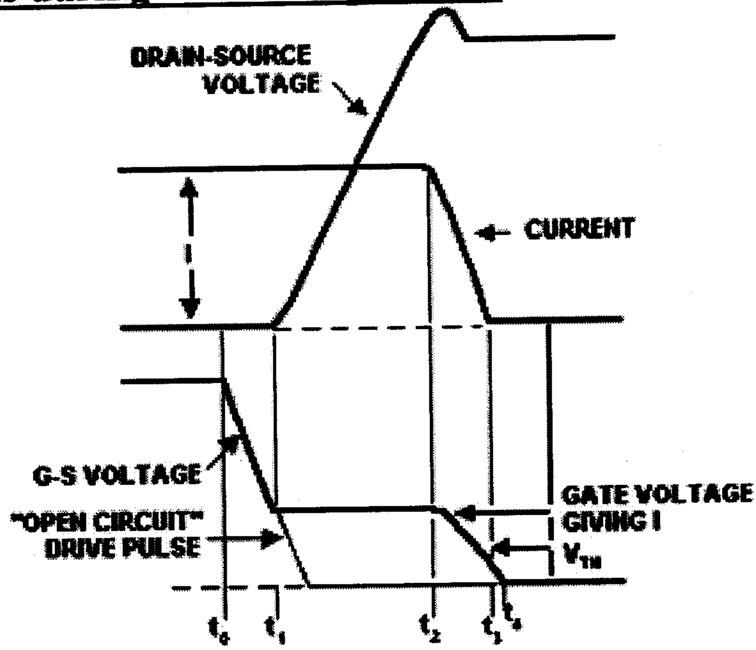
On the other hand, if the device is operated in the linear mode, a large current from the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion. The above considerations are more clearly understood by analyzing the MOSFET's ON-OFF waveforms shown below :

Waveforms during turn-ON process :

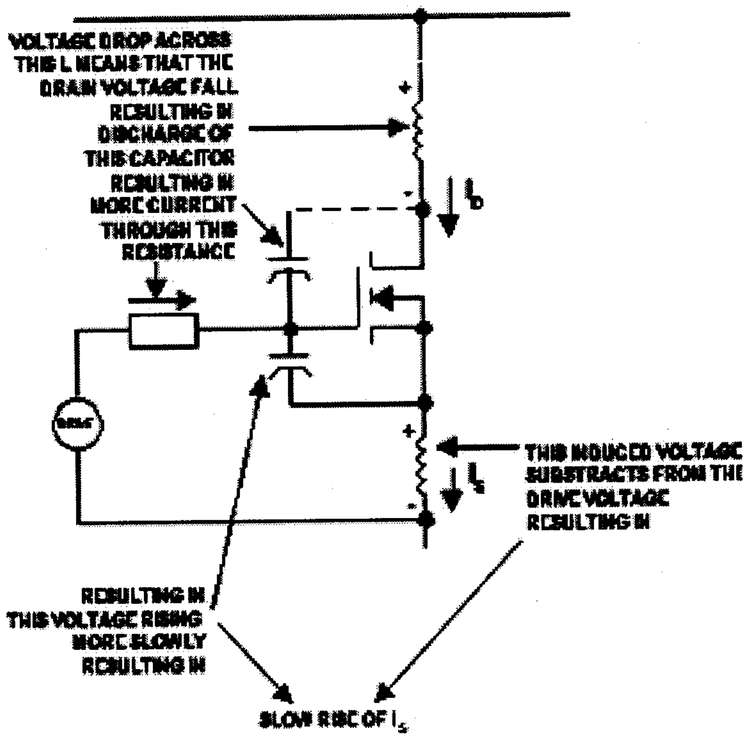
Fig 3



Waveforms during turn-OFF process :



Model of MOSFET during ON-OFF process :



Care should be exercised not to exceed the gate-to-source maximum voltage rating. Even if the applied gate voltage is kept below the maximum rated gate voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. A gate drive circuit with very low impedance insures that the gate voltage is not exceeded in normal operation.

From the model of the MOSFET during switching shown above, it is clear that 'Miller Effect' has an influence in the MOSFET switching process. It is explained as follows: During the period t1 to t2 some voltage is dropped across "unclamped" stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit.

This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be.

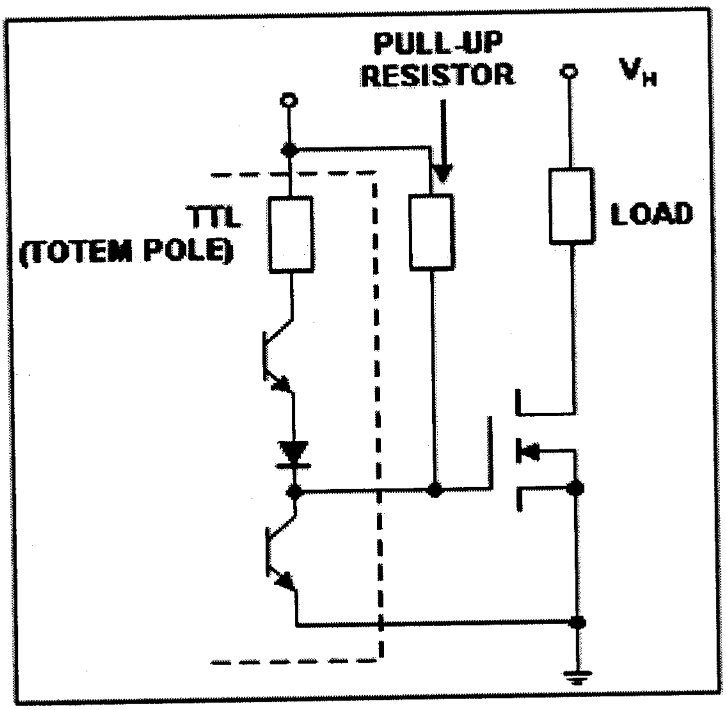
Similar considerations affect the turn-OFF process in MOSFETs, therefore it is critical to have low output impedance drive circuit, not only to reduce switching Losses, but also to clamp down unwanted transients from entering the gate.

5.2 Selection of gate drive :

Considering the factors mentioned in the previous chapter a TTL (Transistor Transistor Logic) 'totem pole' drive is suited because of its simplicity and low output impedance and high input impedance. The schematic is as shown below:

TTL Totem Pole Drive :

Fig 6



With a gate charge of 60 nC and at a switching frequency is 100kHz, the power lost in the gate drive circuit is approximately:

$$P = VGS \text{ x } QG \text{ x } f = 12 \text{ x } 60 \text{ x } 10\text{-}9 \text{ x } 100 \text{ x } 103 = 72mW$$

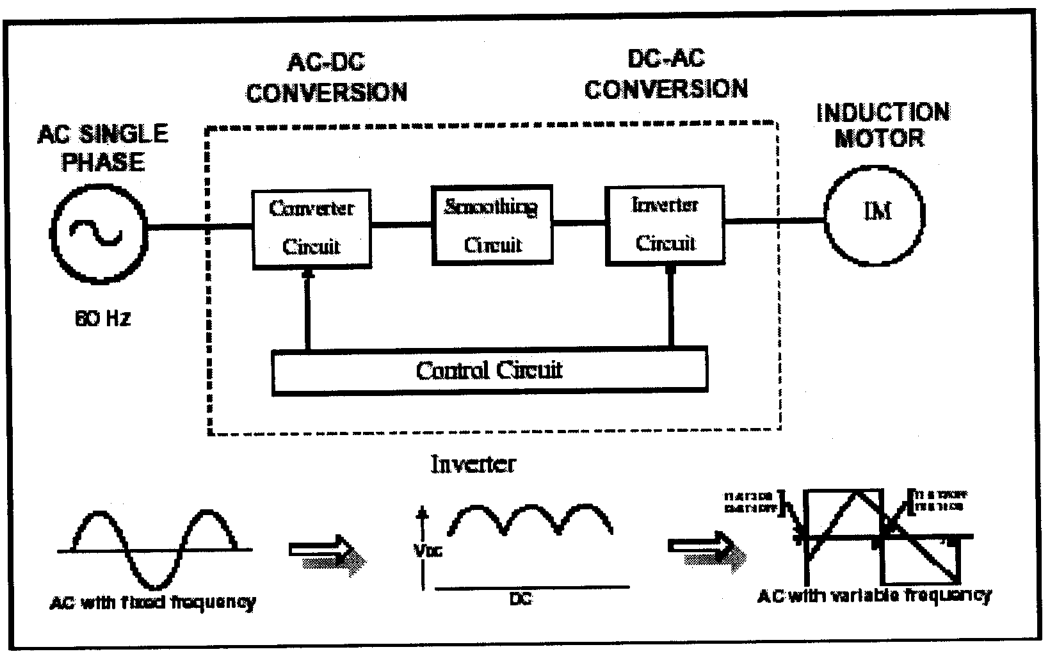
The driver devices must be capable of supplying 1A without significant voltage drop, but hardly any power is dissipated in them. Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances.

Chapter 6 – Inverters

6.1 Overview :

An inverter is the name given to a device that produces an AC, signal usually from a DC supply. Inverters are now commonplace in industry; their uses include, variable speed drives, induction heaters and uninterruptible power supply (UPS) systems. The basic block diagram is as shown :

Fig 7

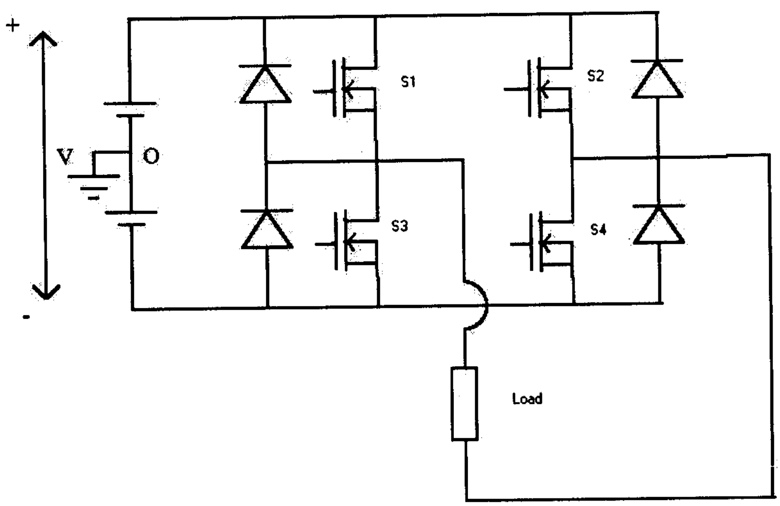


There are four main types of inverter; voltage source, current source, pulse width modulation (PWM) and the cycloconverter. Inverters can be broadly classified into two types, namely, single and three phase inverters.

6.2 Single phase inverters :

The basic single phase inverter schematic is as shown :

Fig 8



In a single phase inverter two power electronic switches are conducting at any particular instant. In the schematic shown above, switches s1 and s4 are turned ON together while s2 and s3 are OFF. In one complete cycle s1 and s4 are ON for a specified duty cycle and s2 and s3 are ON for the remaining period in the same cycle. When the above method of operation is followed the output is as shown below :

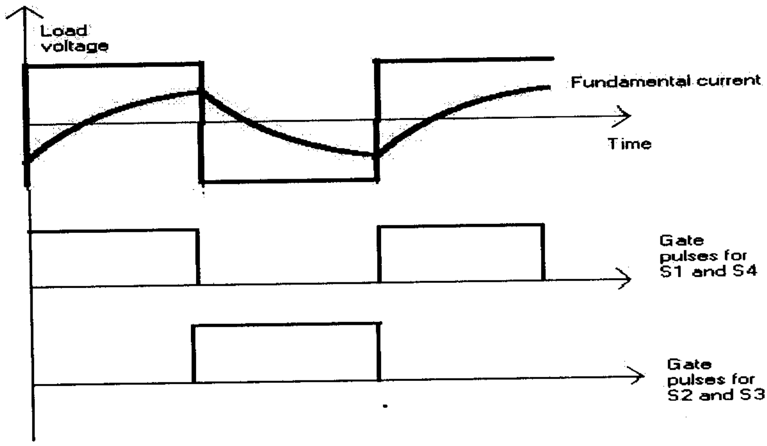


Fig 9

6.3 Three phase inverters :

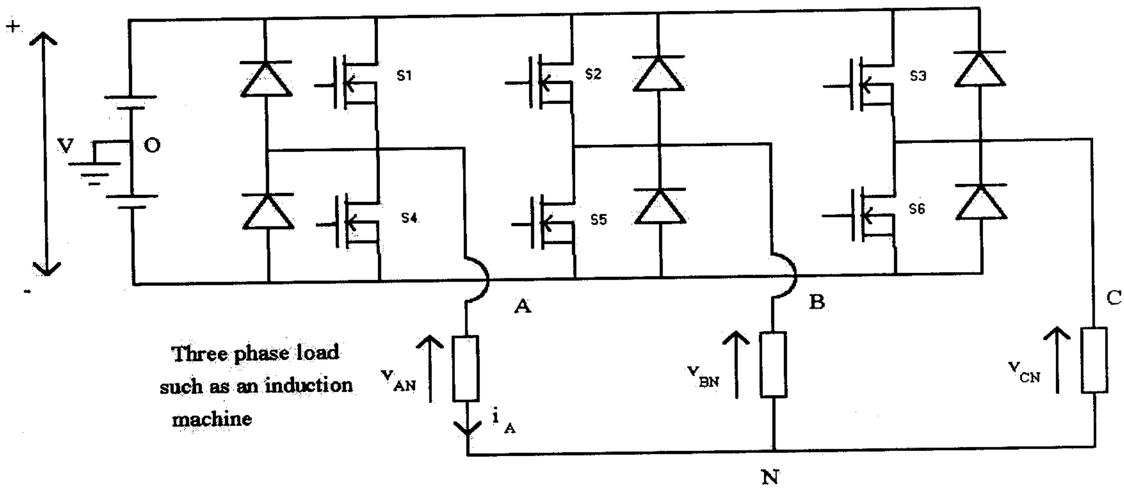
Three phase inverters are more common in industrial applications due to their superior power capabilities. There are usually six power switches used in these inverters. There are two ways in which a 3 phase ac output can be produced from this inverter,

(i) 180° Conduction of power elements

(ii) 120° Conduction of power elements

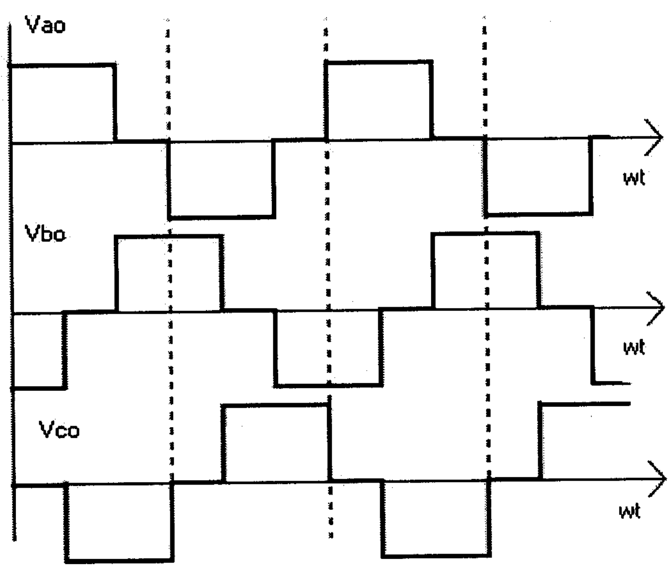
In the first case three power elements are ON at any instant and they each conduct for half a cycle. In the second case only two power elements are ON at any instant and they conduct for one third of the cycle. In both cases the gating signals of the power elements' are delayed by 60° mutually with respect to one another. The following diagram shows the 3 phase inverter :

Fig 10



In 120° degree conduction mode two power elements are ON at any instant of time, remaining ON for one thirds of a cycle and separated from each other by 60°. The gating signals follow a similar pattern, the sequence for the schematic shown above:(1,5),(1,6),(6,2),(2,4),(4,3),(3,5) before the sequence repeats again. The output of the inverter for the above operation is as shown :

Fig 11



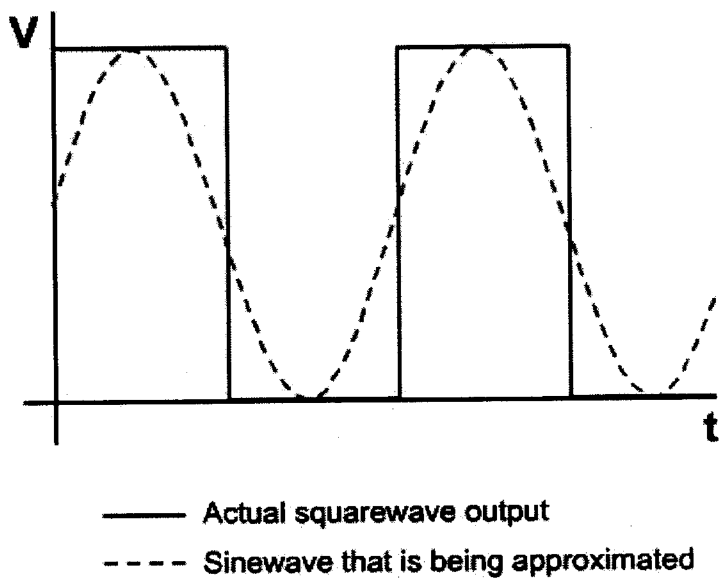
In both the inverters mentioned above the output is a coarse approximation of a sine wave with a large amount of harmonics still present. This can be avoided by the use of Pulse Width Modulation(PWM) wherein a series of pulses are fed as the gating signals instead of a single pulse per element per cycle. On filtering the output the output shown above using an L-C filter a smooth sinusoidal output can be obtained.

Chapter 7 – Pulse Width Modulation

7.1 Overview :

In previous methods all the devices were switched with the same frequency of singular pulses, this provides an output that is a poor approximation of the sine wave. Pwm uses a train of pulses of varying duty cycle to control the output of the inverter to a close sine wave approximation. The following illustration shows the concept :

Fig 12



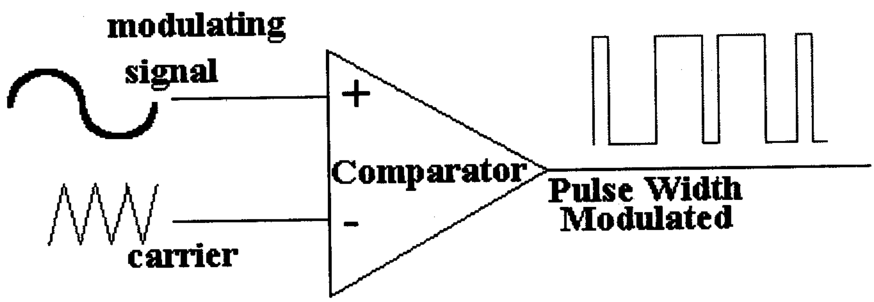
There are many ways of generating a pwm output including

- Single pulse width modulation
- Multiple pulse width modulation
- Sinusoidal pulse width modulation
- Modified pulse width modulation
- Phase displacement control

7.2 Sinusoidal Pulse Width Modulation :

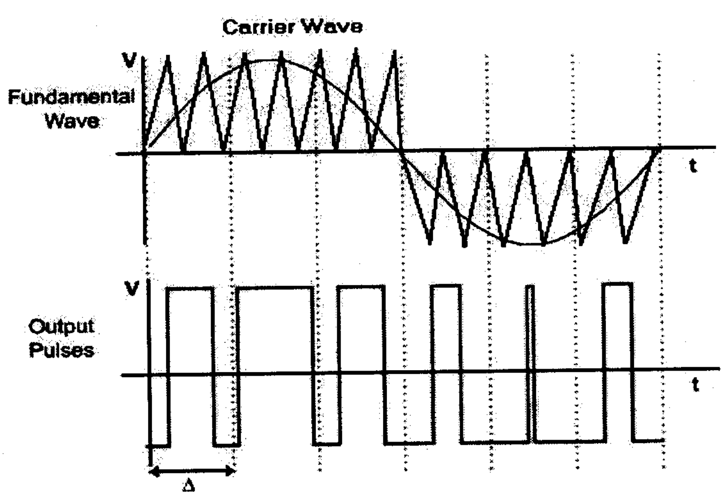
Although these are different ways of generating a pwm wave they differ only in the carrier circuit used fot modulating the input signal. The following illustration shows the principle behind generating these pwm waves.

Fig 13



Since the inverter must produce an output that is a close approximation of a sine wave the pwm signals used in an inverter must follow a sinusoidal modulation. The following illustration shows the pwm output after a sinusoidal modulation :

Fig 14



As shown in the diagram, the gating pulses to the MOSFETs are varying the duty cycle of the MOSFET according to a sinusoidal wave. Thus a close approximation to a sie wave can be obtained as an output. After sufficient filtering a perfect sinusoidal wave can be obtained.

Chapter 8 – Frequency Display

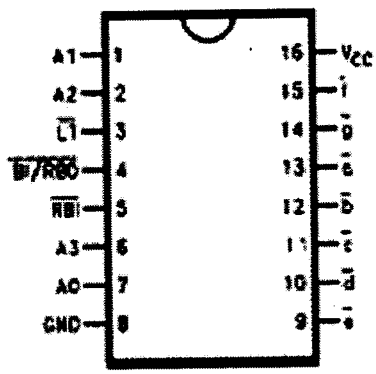
The frequency set by the user is displayed as asset value using the display segment. The segment consists of standard seven segment displays and BCD to seven segment decoder/driver IC(74LS47).

The BCD to seven segment decoder/driver IC is primary controller of the sdisplay, has the following key features :

- The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly.
- Auxiliary inputs provided for lamp test, blanking, cascadable zero suppression.

The illustration below shows the pin diagram and the pin description:

Fig 15



Pin Descriptions

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$–$\overline{g}$	Segment Outputs (Active LOW) (Note 1)

A total of three BCD to seven segment decoder/driver Ics have been used in the display segment and the inputs to the drivers are obtained from separate microcontroller ports. The following table shows the truth table of the driver :

Fig 16

Truth Table

Decimal or Function	Inputs							Outputs						
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L

Chapter 9 – Switching and Isolation

The microcontroller needs to protected or isolated from the power element or the inverter segment. Furthermore the microcontroller provides a PWM output only in one of its output ports and in particular only one pin. To effectively isolate and also efficiently switch multiple power elements simultaneously, the switching and isolation segment is essential. This segment consists of two basic components :

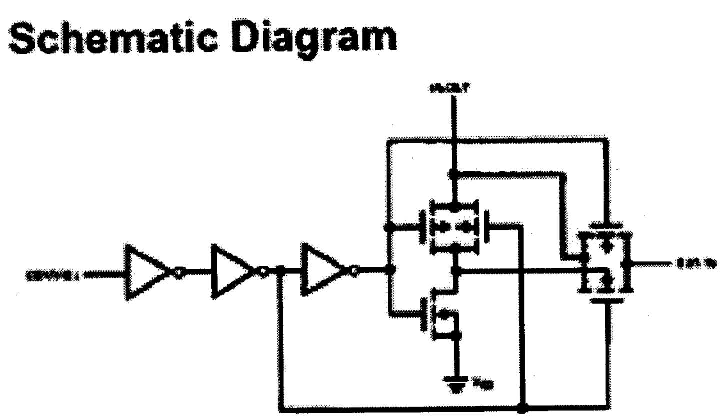
(i) Digital/Analog switches

(ii) Optical Isolators

9.1 Digital/Analog switches :

The switching of multiple power elements is achieved by the usage of the Quad Bilateral Switch provided in the CD4066 integrated circuit. The afore mentioned IC has the following internal schematic :

Fig 17



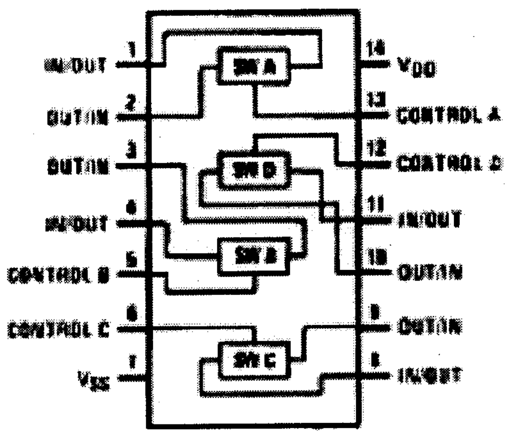
The typical features of this analog/digital switch are :

- High noise immunity.
- Wide range of digital and analog switching.
- ON resistance flat over peak to peak signal range.
- High ON/OFF output voltage ratio.
- Extremely high control input impedance.
- Frequency range of over 40 MHz.
- High degree linearity.

The internal connection diagram of the analog/digital switch package is shown below :

Fig 17

Connection Diagram

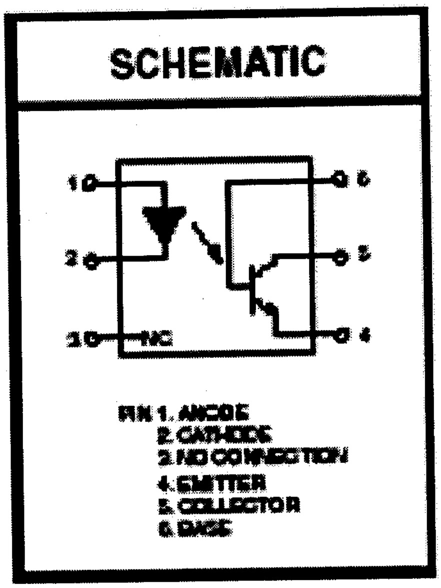


The typical applications include signal gating, chopper, commutating switch, multiplexing etc.

9.2 Optical Isolators :

The optoisolators act as buffers between the microcontroller and the high voltage side thus shielding the microcontroller from damage. The optoisolators used employ light emitting diodes in one side and photo transistors on the other side to effectively act as a buffer between two different voltage levels. The schematic used is as shown :

Fig 18



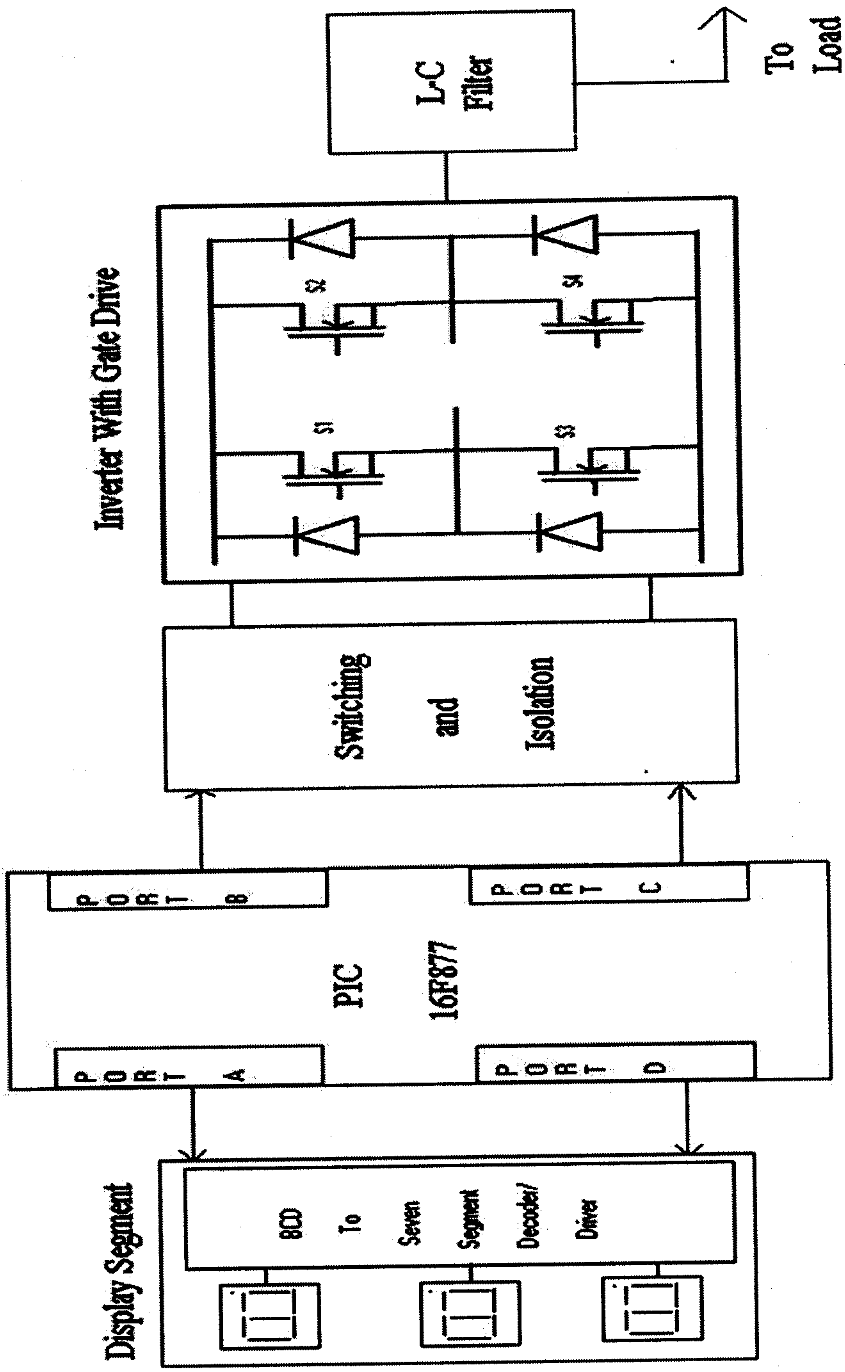
Chapter10 – Control Segment

The control segment primarily consists of the PIC 16F877 microcontroller and its related components. The microcontroller is the heart of the whole project, directing various activities simultaneously. The activities of the microcontroller include :

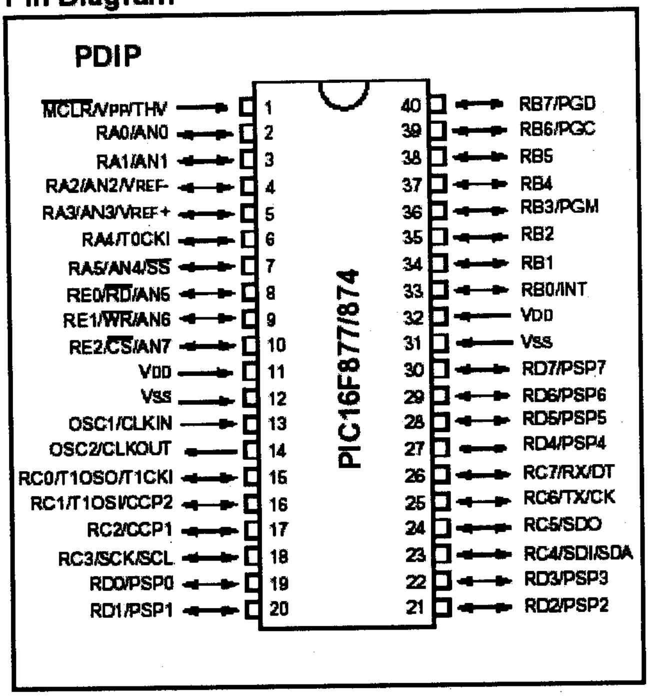
- Generating PWM output for various sine frequencies specified by the user.
- Scanning for user input from interrupt sources.
- Constantly updating PWM duty cycle and period.
- Converting analog inputs into digital data for further processing and display.
- Monitoring and discriminating interrupts and analog inputs.

The following illustration shows the functional blocks of the control segment along with the peripheral segments :

Functional Block Diagram



Pin Diagram



Microcontroller Core Features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program

branches which are two cycle

- Operating speed: DC - 20 MHz clock input

DC - 200 ns instruction cycle

- Up to 8K x 14 words of FLASH Program Memory,

Up to 368 x 8 bytes of Data Memory (RAM)

Up to 256 x 8 bytes of EEPROM data memory

- Interrupt capability (up to 14 sources)
- Direct, indirect and relative addressing modes

• Power-on Reset (POR)
• Power-up Timer (PWRT)
• Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
• Fully static design
• In-Circuit Serial Programming□ (ICSP) via two pins
• Processor read/write access to program memory
• Wide operating voltage range: 2.0V to 5.5V
• Commercial and Industrial temperature ranges
• Low-power consumption:
- < 2 mA typical @ 5V, 4 MHz
- 20 □A typical @ 3V, 32 kHz
- < 1 □A typical standby current

Peripheral Features:

• Timer0: 8-bit timer/counter with 8-bit prescaler
• Timer1: 16-bit timer/counter with prescaler, can be incremented during sleep via external crystal/clock
• Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
• Two Capture, Compare, PWM modules
- Capture is 16-bit, max. resolution is 12.5 ns
- Compare is 16-bit, max. resolution is 200 ns
- PWM max. resolution is 10-bit

• 10-bit multi-channel Analog-to-Digital converter

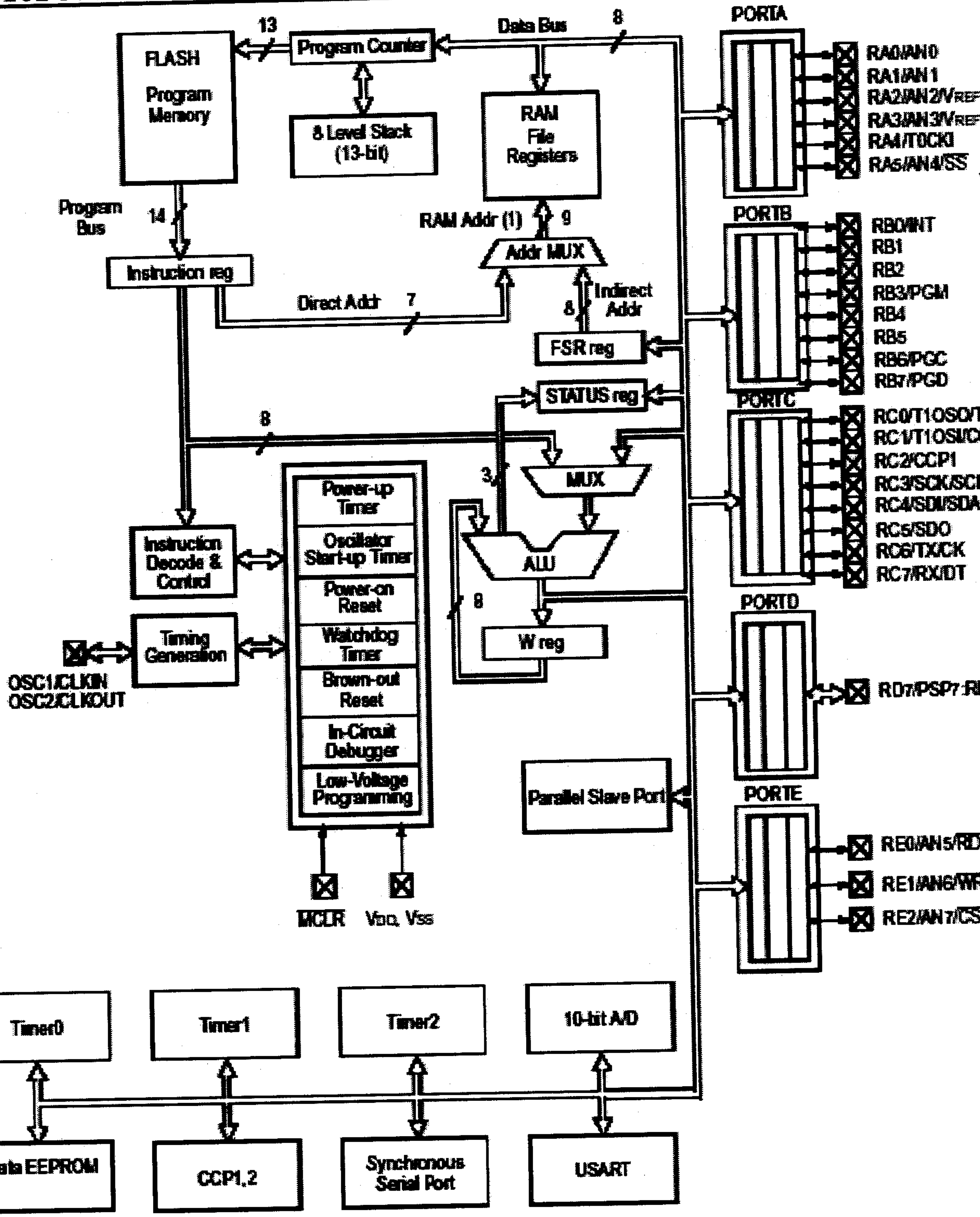
• Synchronous Serial Port (SSP) with SPI□(Master Mode) and I2C□ (Master/Slave)

• Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection

• Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)

• Brown-out detection circuitry for Brown-out Reset (BOR)

PIC 16F877 ARCHITECTURE :



Program Memory Organization :

The PIC16F87X devices have a 13-bit program countercapable of addressing an 8K x 14 program memory space. The PIC16F877/876 devices have 8K x 14words of FLASH program memory and the PIC16F873/874 devices have 4K x 14. Accessing a location above the physically implemented address will cause a wrap around. The reset vector is at 0000h and the interrupt vector is at 0004h.

Special Function Registers :

STATUS Register :

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n= Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
(for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

INTCON Register :

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n= Value at POR reset

bit 7: **GIE**: Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

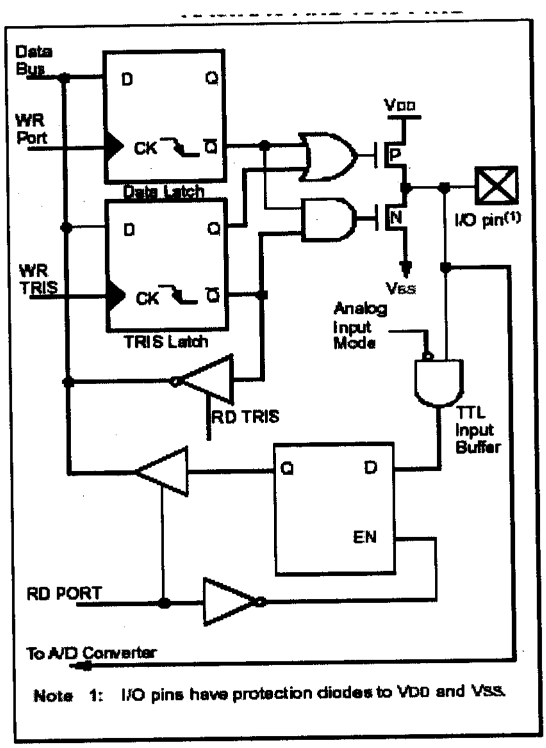
I/O Ports :

Most of the pins for I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register:

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch.

Structure Of I/O Port Pins :



PORTB and the TRISB Register :

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the Low Voltage Programming function; RB3/PGM, RB6/PGC and RB7/PGD. Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>).

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison).

PORTC and the TRISC Register

PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). PORTC is multiplexed with several peripheral functions . PORTC pins have Schmitt Trigger input buffers. When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input.

TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device reset. The input clock (FOSC/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>). The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset. The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)). Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Timer2 Prescaler and Postscaler

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register

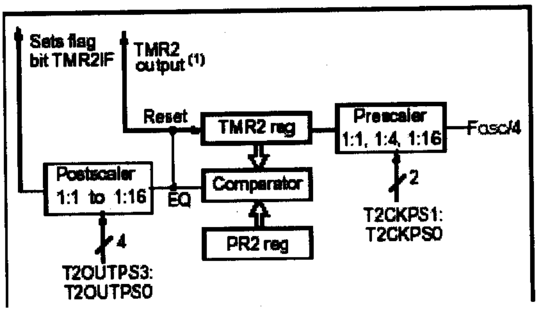
• any device reset (POR, MCLR reset, WDT reset or BOR)

TMR2 is not cleared when T2CON is written.

Output of TMR2

The output of TMR2 (before the postscaler) is fed to the SSPort module, which optionally uses it to generate shift clock.

TIMER 2 BLOCK DIAGRAM :



T2CON REGISTER :

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **Unimplemented:** Read as '0'

bit 6-3: **TOUTPS3:TOUTPS0:** Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2: **TMR2ON:** Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0: **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

CAPTURE/COMPARE/PWM MODULES

Each Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM master/slave Duty Cycle register

Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger.

CCP1 Module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

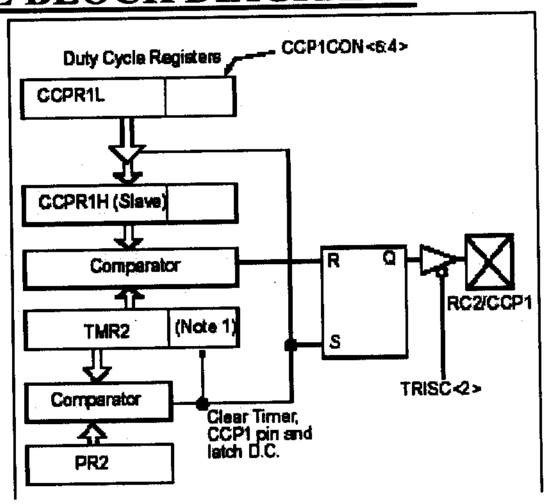
CCP2 Module:

Capture/Compare/PWM Register1 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

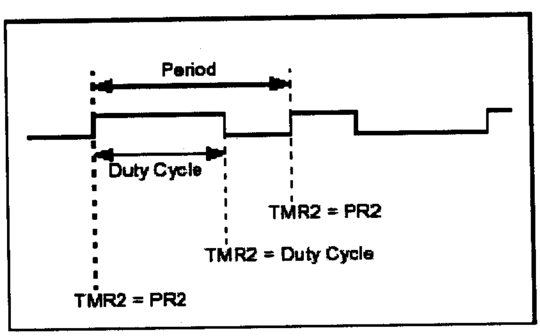
PWM Mode (PWM)

In pulse width modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

PWM MODULE BLOCK DIAGRAM :



SAMPLE PWM WAVE FORM :



PWM PERIOD :

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period]. When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

PWM DUTY CYCLE :

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (\text{CCPR1L:CCP1CON}<5:4>) \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

Maximum PWM resolution (bits) for a given PWM frequency:

$$\text{Resolution} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE :

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the other devices. The analog input charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation. The A/D conversion of the analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low voltage reference input that is software selectable to some combination of VDD, VSS, RA2 or RA3. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The ADCON0 register, shown in Register , controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

ADCON0 REGISTER :

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
\- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0**: A/D Conversion Clock Select bits
- 00 = Fosc/2
- 01 = Fosc/8
- 10 = Fosc/32
- 11 = FRC (clock derived from an RC oscillation)

bit 5-3: **CHS2:CHS0**: Analog Channel Select bits
- 000 = channel 0, (RA0/AN0)
- 001 = channel 1, (RA1/AN1)
- 010 = channel 2, (RA2/AN2)
- 011 = channel 3, (RA3/AN3)
- 100 = channel 4, (RA5/AN4)
- 101 = channel 5, (RE0/AN5)(1)
- 110 = channel 6, (RE1/AN6)(1)
- 111 = channel 7, (RE2/AN7)(1)

bit 2: **GO/DONE**: A/D Conversion Status bit
If ADON = 1
- 1 = A/D conversion in progress (setting this bit starts the A/D conversion)
- 0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

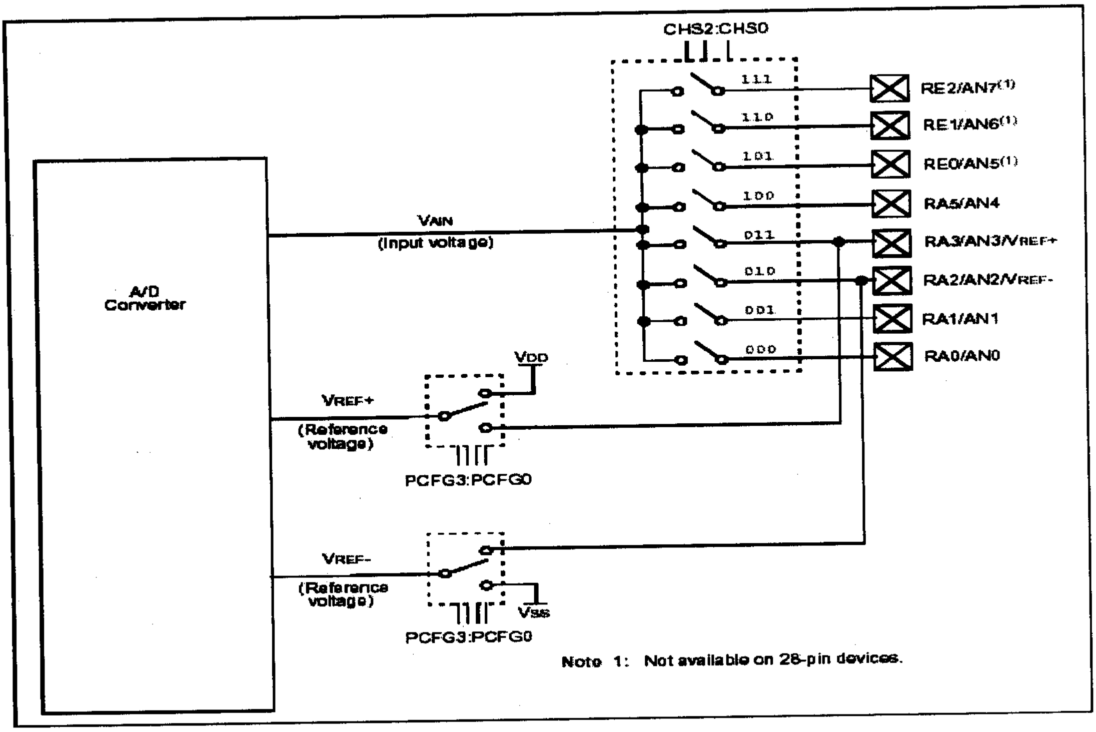
bit 1: **Unimplemented**: Read as '0'

bit 0: **ADON**: A/D On bit
- 1 = A/D converter module is operating
- 0 = A/D converter module is shutoff and consumes no operating current

Note 1: These channels are not available on the 28-pin devices.

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. After this acquisition time has elapsed, the A/D conversion can be started.

A/D Converter Block Diagram :



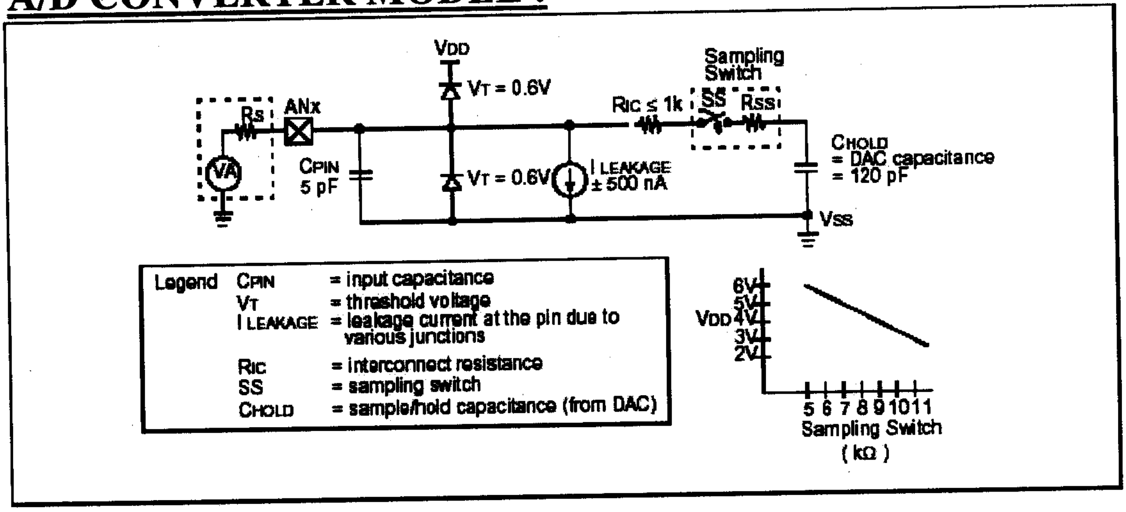
A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure .

To calculate the minimum acquisition time, the following equation is used.

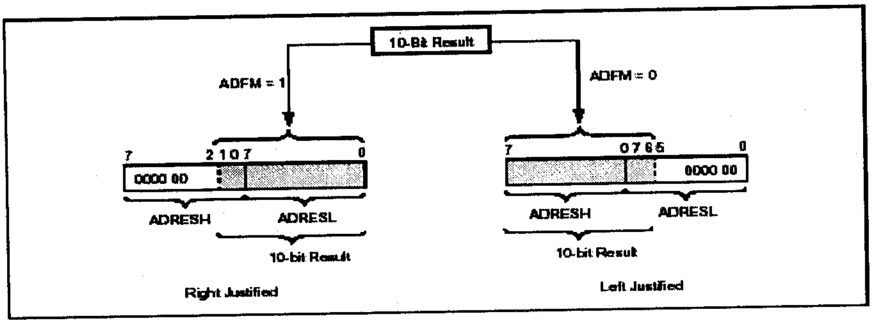
$$
\begin{aligned}
T_{ACQ} &= \text{Amplifier Settling Time} + \\
&\quad \text{Hold Capacitor Charging Time} + \\
&\quad \text{Temperature Coefficient} \\
&= T_{AMP} + T_C + T_{COFF} \\
&= 2\mu S + T_C + [(\text{Temperature} - 25^\circ C)(0.05\mu S/^\circ C)] \\
T_C &= C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047) \\
&= -120pF\ (1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885) \\
&= 16.47\mu S \\
T_{ACQ} &= 2\mu S + 16.47\mu S + [(50^\circ C - 25\times C)(0.05\mu S/\times C) \\
&= 19.72\mu S
\end{aligned}
$$

A/D CONVERTER MODEL :



A/D RESULT REGISTERS

The ADRESH:ADRESL register pair is the location where the 10-bit A/D result is loaded at the completion of the A/D conversion. This register pair is 16-bits wide. The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register. The A/D Format Select bit (ADFM) controls this justification. The figure shown below shows the operation of the A/D result justification. The extra bits are loaded with '0's'. When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.



10-Bit Result
ADFM = 1
ADFM = 0
7
2 1 0 7
0
0000 00
ADRESH
ADRESL
10-bit Result
Right Justified
7
0 7 6 5
0
0000 00
ADRESH
ADRESL
10-bit Result
Left Justified

Chapter11 – Software

Software Routines

The software used in the project has been divided into two major modules,

(i) A/D conversion, display and interrupt service module.

(ii) PWM duty cycle and period update module.

The A/D conversion and interrupt service module constantly scans for new user inputs and converts them to BCD values for display. It also services the various user interrupts and internal software interrupts.

The PWM module updates the duty cycles of the gating signals by using a sine wave lookup table stored by the programmer, it also updates the PWM period by accepting new frequencies from the user.

The following pages show the source codes used and their respective control flow.

11.1 Analog to Digital conversion, interrupt service and display routine:

Source code :

```
;=============A/D Conversion with display routine=====
list p=16f877
include <p16f877.inc>
;=============sfr addresses initialisation==========
status equ 03h
portb equu 06h
trisb equ 86h
portd equ 08h
trisd equ 88h
intcon equ 0bh
pir1 equ 0ch
pie1 equ 8ch
adresh equ 1eh
adcon0 equ 1fh
adcon1 equ 9fh
portc equ 07h
trisc equ 87h
porta equ 05h
trisa equ 85h
;===========Define vector locations=======
org 0x000
```

```
goto start
org 0x004
goto introutine
;============Define user variables================
cblock 20h
index
var
digit0
digit1
digit2
temp1
temp2
temp3
endc
;============Interrupt service routine===============

introutine
      bcf status,5            ;clear interrupt flag bits
      btfsc pir1,6
      call adover
      movf portb,0
      clrf intcon
      bsf intcon,7
      bsf intcon,3
      goto adstart
;============main routine============
adinitialise                    ;initialize a/d converter
```

```
    bsf status,5
    clrf pie1
    bsf pie1,6
    movlw B'11110000'
    movwf trisa
    clrf trisc
    movlw B'00000000'
    movwf trisc
    movlw B'00001110'
    movwf adcon1
    bcf status,5
    bcf pir1,6
    clrf portc
    movlw B'00000000'
    movwf adcon0
    clrf adresh

    clrf var                    ;initialize user variables
    clrf digit0
    clrf digit1
    clrf digit2
return

adstart                         ;start a/d conversion
    bsf adcon0,0
    call adcdelay
    bsf adcon0,2
```

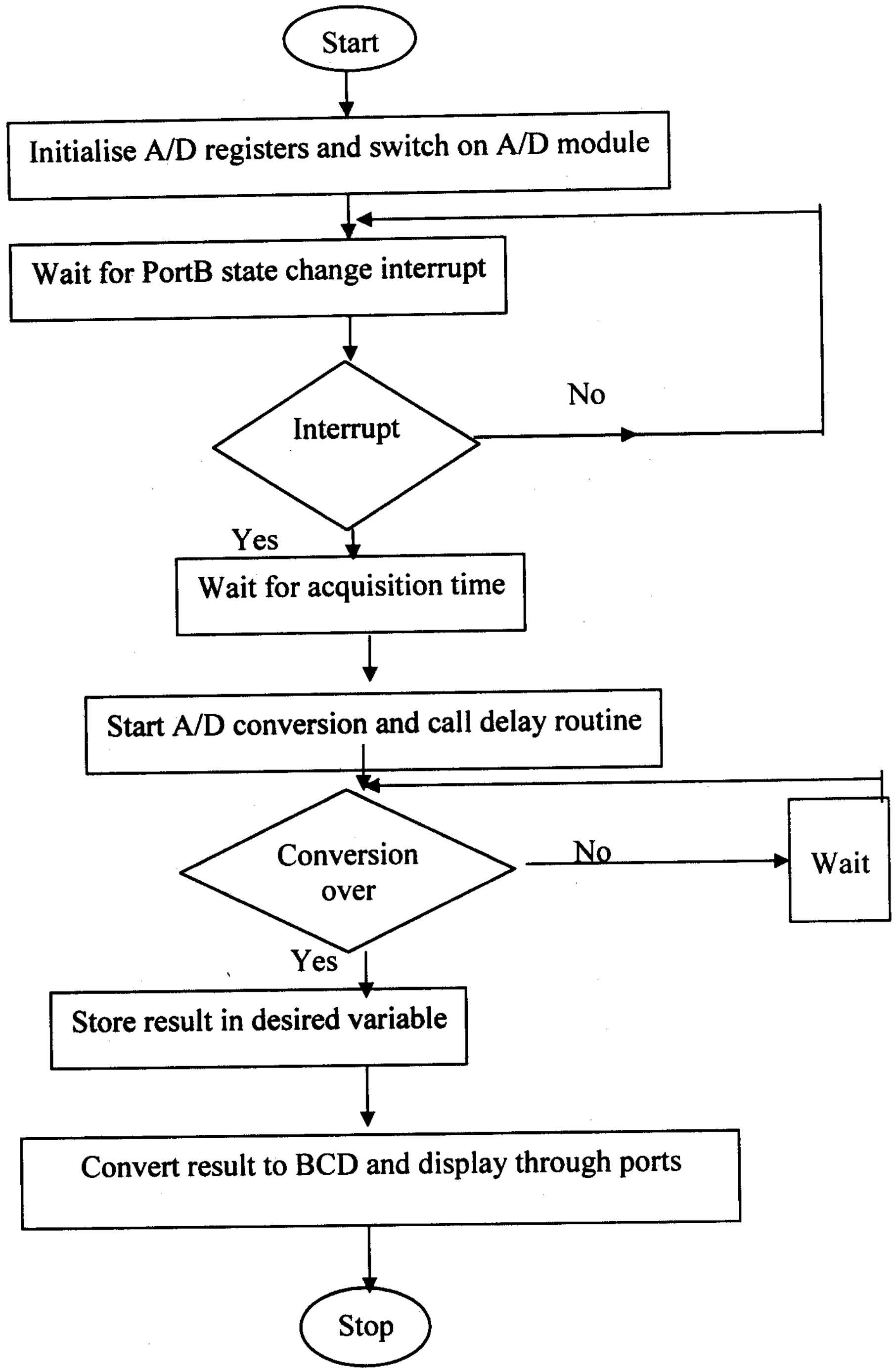
```
      call adcdelay

adcdelay                        ;acquisition delay for a/d conversion
      loop1
       movlw d'1'
      movwf temp1
  loop2
      movlw d'30'
      movwf temp2
  loop3
      clrwdt
      decfsz temp2,1
      goto loop3
      decfsz temp1,1
      goto loop2
       return

 adover
      bsf pie1,6
      bsf intcon,7
      bcf pir1,6
      movf adresh,0
      movwf var
  bin2bcd                        ;binary to bcd conversion
  loophun
      movlw .100
      subwf var,w
```

```
      btfss status,0
      goto huover
      incf digit2,1
      movwf var
      goto loophun
huover
      movlw .0
loopten
      movlw .10
      subwf var,w
      btfss status,0
      goto teover
      incf digit1,1
      movwf var
      goto loopten
teover
      movf var,0
      movwf digit0
      swapf digit0,1                ;display procedure
      movf digit0,0
      movwf porta
      swapf digit2,1
      movf digit2,0
      addwf digit1,0
      movwf portd
      goto wait
```

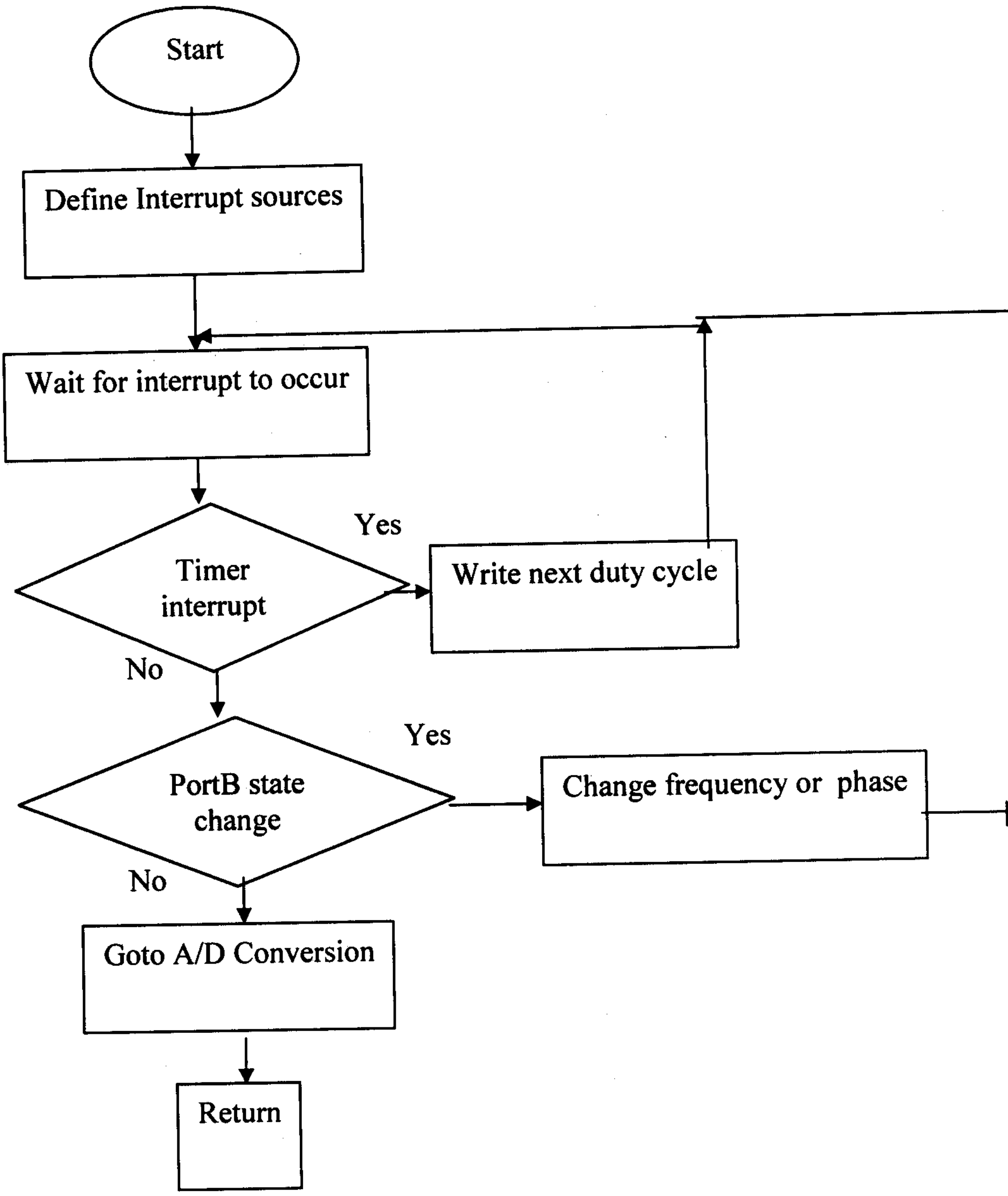
```
start                                   ;program starts
      call adinitialise
      clrf status
      clrf portb
      clrf intcon
      bsf intcon,7
      bsf intcon,3
      clrf portd
      bsf status,5
      clrf trisb
      movlw b'11110000'
      movwf trisb
      movlw b'00000000'
      movwf trisd
      movlw b'11111111'
      movwf portd
      wait
      goto wait
 end
```

Flowcharts :

11.2 Analog to Digital conversion :



Interrupt Service :



11.3 PWM Duty cycle and period update routine :

Source Code :

```
;===============pwm routine=============

list p=16f877
include <p16f877.inc>
;===============sfr address initialisation============
intcon equ 0bh
adresh equ 1eh
adcon0 equ 1fh
adcon1 equ 9fh
portd equ 08h
trisd equ 88h
portb equ 06h
trisb equ 86h
portc equ 07h
trisc equ 87h
status equ 03h
tmr2 equ 11h
t2con equ 12h
pr2 equ 92h
pir1 equ 0ch
ccpr1l equ 15h
ccpr1h equ 16h
```

```
ccp1con equ 17h
pcl equ 02h
pie1 equ 8ch
;==============user variables definition=========
cblock 20h
index
endc
;=============define vector locations==================
org 0x000
goto start
org 0x004
goto introutine
;==============interrupt service routine=======
introutine
        bcf status,5          ;clear interrupt flag bits
        bcf pir1,1
        bsf intcon,7
        bsf status,5
        bsf pie1,2
        goto dcroutine

;==============main routine============
start
        clrf portb
        clrf portc
        clrf status           ;set up status reg
        clrf tmr2
```

```
clrf t2con
clrf pir1
bsf status,5
clrf pr2                    ;clear pwm period
clrf trisc
clrf trisb
clrf pie1
bsf pie1,1
movlw .255
movwf pr2                   ;setup pwm period
bcf status,5
bsf intcon,7
bsf intcon,6
clrf ccp1con                ;clear pwm control register
clrf ccpr1l                 ;clear pwm duty cycle register
bsf ccp1con,2               ;configure ccp register
bsf ccp1con,3
movlw .0
movwf ccpr1l
repeat
bsf portb,4
bsf portb,5
bcf portb,1
bcf portb,3
movlw .3
movwf index
bsf t2con,2                 ;switch timer2 on
```

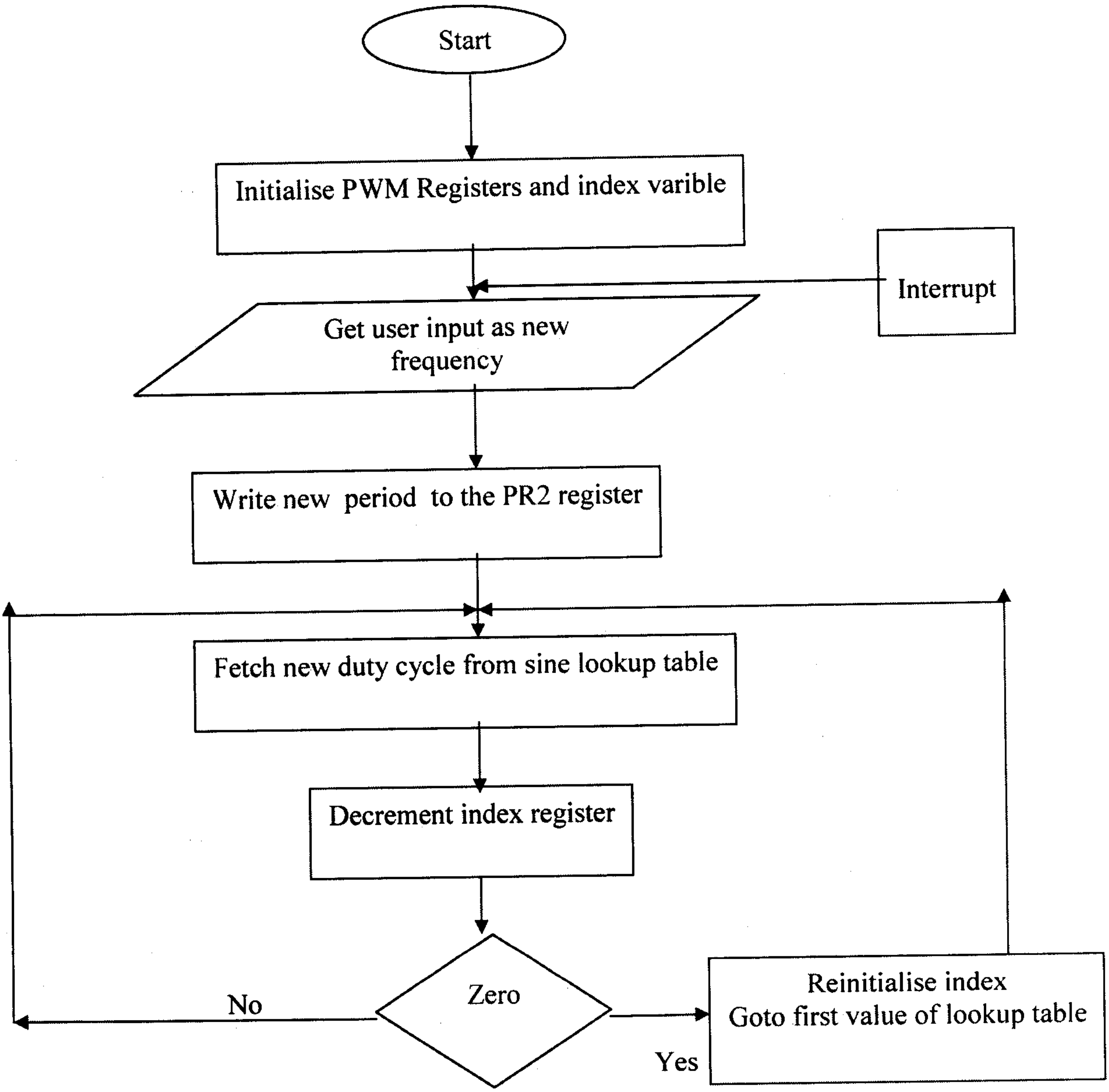
```
      goto pinchange
;===============timer poll=============
dcroutine                              ;duty cycle routine
      bcf pir1,1
      bcf t2con,2
      clrf tmr2
      call sinetable                   ;call duty cycle lookup table
      incf index,1
      movwf ccpr11
      bsf t2con,2
;============port pin change==========
pinchange
t2polli
      btfsc portc,2
       goto t2polli
      bcf portb,4
      bcf portb,5
      nop nop nop
      nop nop nop
      bsf portb,1
      bsf portb,2
wait
      goto wait
;===================look up table=====
sinetable
      movf pcl,0
      addwf index,0
```

```
movwf pcl
retlw .128          ;0 degree, 2.5 volts
retlw .148
retlw .167
retlw .185
retlw .200
retlw .213
retlw .222
retlw .228
retlw .230          ;90 degree, 4.5 volts
retlw .228
retlw .222
retlw .213
retlw .200
retlw .185
retlw .167
retlw .148
retlw .128          ;180 degree, 2.5 volts
retlw .108
retlw .89
retlw .71
retlw .56
retlw .43
retlw .34
retlw .28
retlw .26           ;270 degree, 0.5 volts
retlw .28
```

```
    retlw .34
    retlw .43
    retlw .56
    retlw .71
    retlw .89
    retlw .108
    movlw .0
    movwf index
    goto repeat
end
```

Flowchart :

11.4 PWM Routine :



Chapter12 – Testing

Test Results

Chapter13 – Conclusion

Conclusion

The emerging trends in high frequency power would certainly prove to be beneficial for the consumer. The cost and size of almost all electrical applications would be reduced. Our project can generate frequencies of up to 255 Hz. with the current hardware. With simple hardware modifications frequencies of 500 Hz or more can be generated.

The microcontroller used in the project enables us to generate 'harmonics free' outputs that can be used for sensitive and common applications. The project can be further developed to generate high voltage ac with improved hardware. The prospect of using high frequency power alone in the future provides the basis for further development of the project.

Bibliography

References and Bibliography

- **Modern Power Electronics- Evolution, Technology and Applications** by B.K.Bose.
- **A 500 Hz Power System -Power converters**, by I.Takahashi and G.J.Su- IEEE Transactions on Industrial Applications 1999.]
- **Power Electronics, circuits, devices and applications** by Muhammed.H.Rashid, 12th editon – 2000
- **Power Electronics** by Dr.P.S.Bhimbra, 5th edition- 2001
- **Power Electronics and motor Control** by W.Shepherd and D.T.W.Liang, 2nd edition-2001
- WWW.irf.com
- WWW.microchip.com

Appendix A: PIC 16F877

Special Function Rgisters(SFR) :

ADCON1 Register :

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: ADFM: A/D Result format select
1 = Right Justified. 6 most significant bits of ADRESH are read as '0'.
0 = Left Justified. 6 least significant bits of ADRESL are read as '0'.

bit 6-4: Unimplemented: Read as '0'

bit 3-0: PCFG3:PCFG0: A/D Port Configuration Control bits

PCFG3: PCFG0	AN7[1] RE2	AN6[1] RE1	AN5[1] RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN / Refs[2]
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog Input
D = Digital I/O

Note 1: These channels are not available on the 28-pin devices.
2: This column indicates the number of analog channels available as A/D inputs and the numer of analog channels used as voltage reference inputs.

Interaction between CCP modules :

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base.
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1.
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1.
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt).
PWM	Capture	None.
PWM	Compare	None.

CCP1CON/CCP2CON Registers :

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented**: Read as '0'

bit 5-4: **CCPxX:CCPxY**: PWM Least Significant bits
Capture Mode: Unused
Compare Mode: Unused
PWM Mode: These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0: **CCPxM3:CCPxM0**: CCPx Mode Select bits
0000 = Capture/Compare/PWM off (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
11xx = PWM mode

Registers associated with PWM operation :

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Registers associated with Analog/Digital conversion :

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	$\overline{MCLR}$, WDT
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	--0- 0000	--0- 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
89h[1]	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111
09h[1]	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu

Instruction Set Summary :

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Field Description :

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

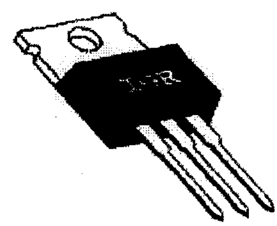
Appendix B: Datasheets

International
IOR Rectifier

IRF840

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



TO-220AB

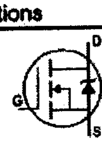
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	5.1	
I_{DM}	Pulsed Drain Current ①	32	
P_D @ T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	510	mJ
I_{AR}	Avalanche Current ①	8.0	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Electrical Characteristics :

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.78	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.85	Ω	V_{GS}=10V, I_D=4.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	4.9	—	—	S	V_{DS}=50V, I_D=4.8A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=500V, V_{GS}=0V
		—	—	250		V_{DS}=400V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	63	nC	I_D=8.0A
Q_{gs}	Gate-to-Source Charge	—	—	9.3		V_{DS}=400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	32		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD}=250V
t_r	Rise Time	—	23	—		I_D=8.0A
$t_{d(off)}$	Turn-Off Delay Time	—	49	—		R_G=9.1Ω
t_f	Fall Time	—	20	—		R_D=31Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	310	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	120	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=8.0A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	460	970	ns	T_J=25°C, I_F=8.0A
Q_{rr}	Reverse Recovery Charge	—	4.2	8.9	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

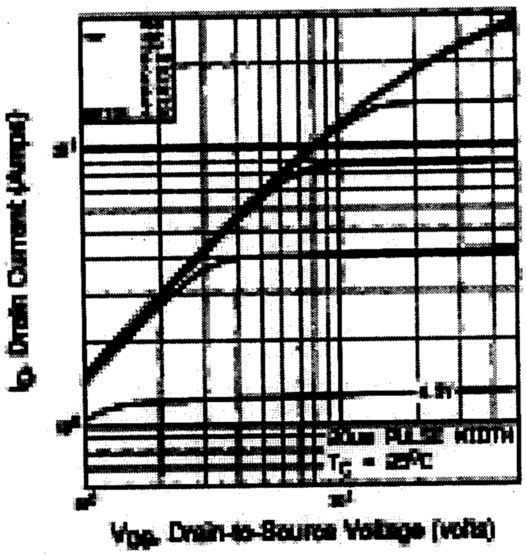


Fig 1. Typical Output Characteristics, T_C=25°C

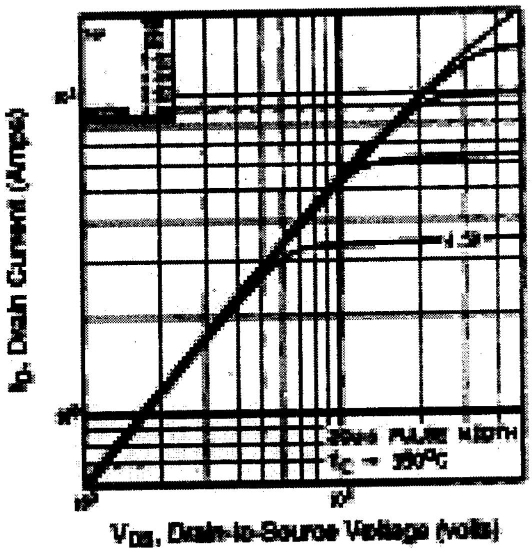


Fig 2. Typical Output Characteristics, T_C=150°C

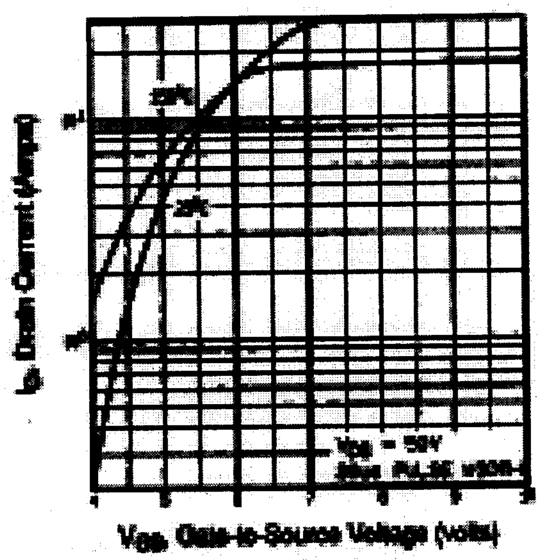


Fig 3. Typical Transfer Characteristics

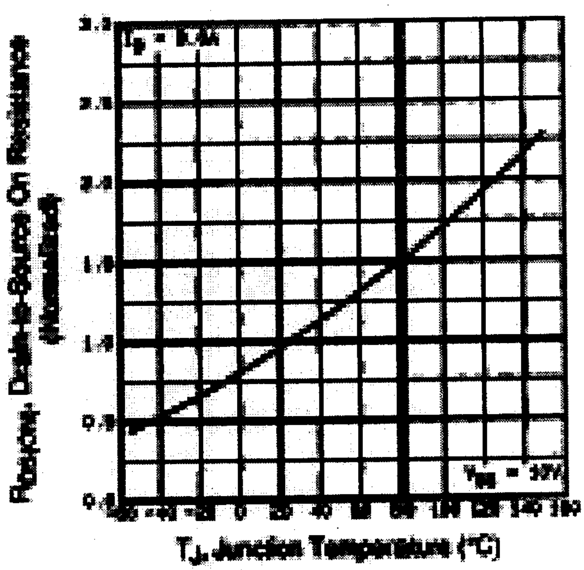


Fig 4. Normalized On-Resistance Vs. Temperature

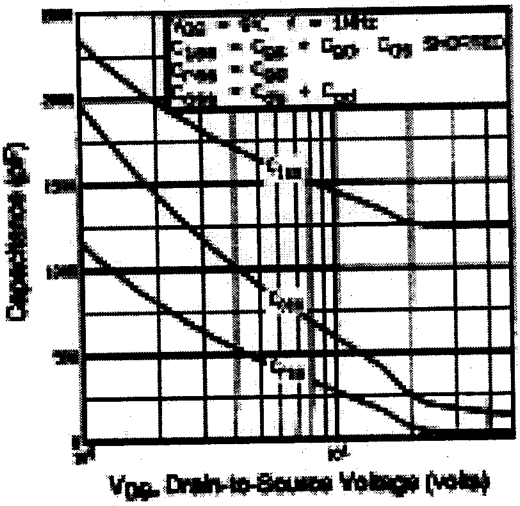


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

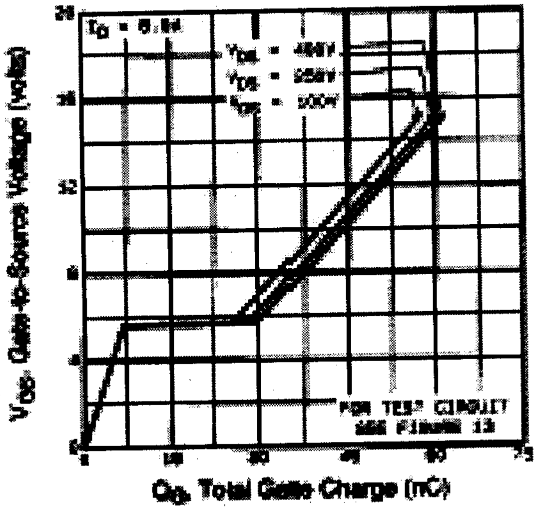


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

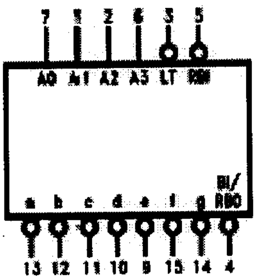
FAIRCHILD
SEMICONDUCTOR™

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

Features

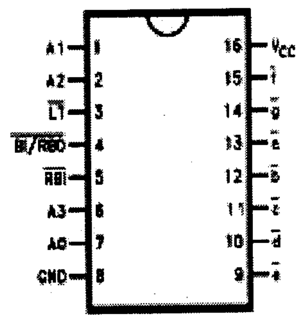
Open-collector outputs
Drive indicator segments directly
Cascadable zero-suppression capability
Lamp test input

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram

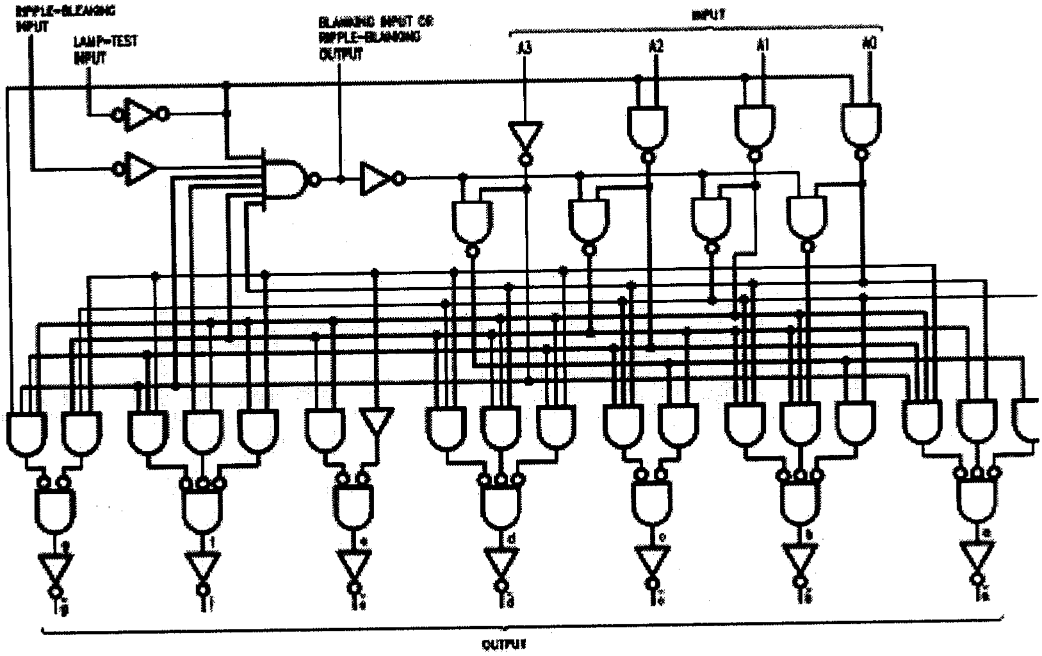


Pin Descriptions

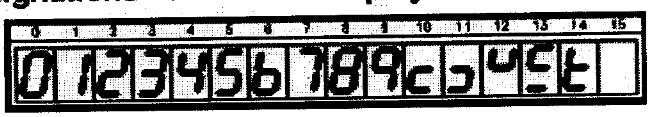
Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$–$\overline{g}$	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

Logic Diagram



Numerical Designations—Resultant Displays



Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current $\overline{a}-\overline{g}$ @ 15V = V_{OH} (Note 7)			−250	μA
I_{OH}	HIGH Level Output Current $\overline{BI}/\overline{RBO}$			−50	μA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Note 7: OFF-State at $\overline{a}-\overline{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 8)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, $\overline{BI}/\overline{RBO}$	2.7	3.4		V
I_{OFF}	Output HIGH Current Segment Outputs	V_{CC} = 5.5V, V_O = 15V $\overline{a}-\overline{g}$			250	µA
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, $\overline{a}-\overline{g}$		0.35	0.5	V
		I_{OL} = 3.2 mA, $\overline{BI}/\overline{RBO}$			0.5	
		I_{OL} = 12 mA, $\overline{a}-\overline{g}$		0.25	0.4	
		I_{OL} = 1.6 mA, $\overline{BI}/\overline{RBO}$			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			100	µA
		V_{CC} = Max, V_I = 10V				
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 9), I_{OS} at $\overline{BI}/\overline{RBO}$	−0.3		−2.0	mA
I_{CC}	Supply Current	V_{CC} = Max			13	mA

Note 8: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	Conditions	R_L = 665Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	An to $\overline{a}-\overline{g}$			100	
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	$\overline{RBI}$ to $\overline{a}-\overline{g}$ (Note 10)			100	

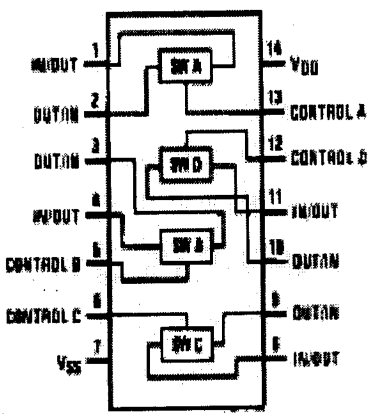
Note 10: $\overline{LT}$ = HIGH, A0–A3 = LOW

FAIRCHILD SEMICONDUCTOR™

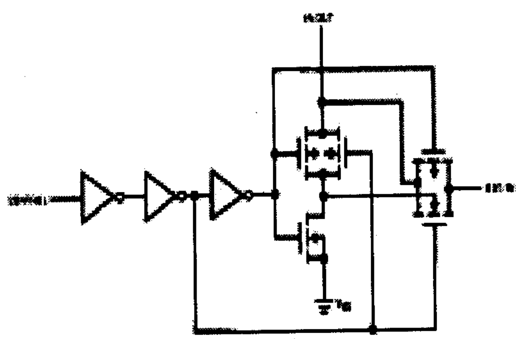
CD4066BC
Quad Bilateral Switch

Features
- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 VDD (typ.)
- Wide range of digital and ±7.5 VPEAK analog switching
- "ON" resistance for 15V operation 80.
- Matched "ON" resistance .RON = 5. (typ.) over 15V signal input
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" 65 dB (typ.) output voltage ratio @ fis = 10 kHz, RL = 10 k.

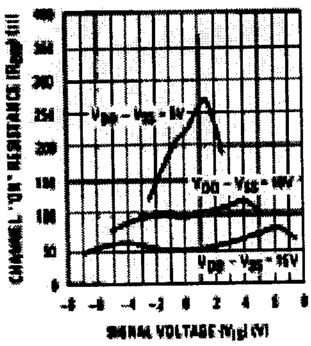
Connection Diagram



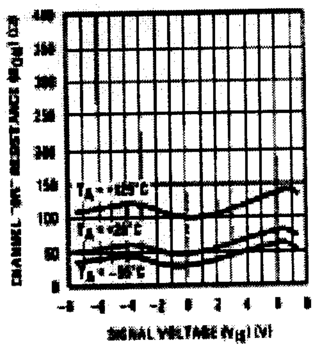
Schematic Diagram



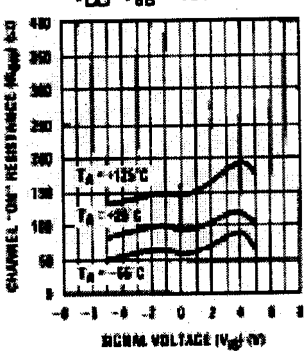
Typical Performance Characteristics



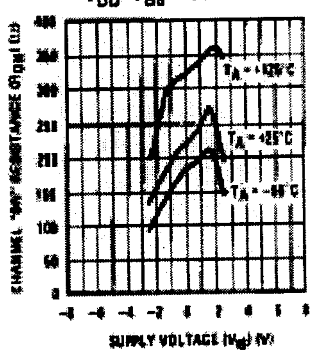
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



"ON" Resistance as a Function of Temperature for $V_{DD}-V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD}-V_{SS} = 10V$



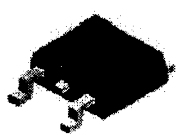
"ON" Resistance as a Function of Temperature for $V_{DD}-V_{SS} = 5V$

LM78XX 1.5A Positive Voltage Regulator

Features

- Output Current of 1.5A
- Output Voltage Tolerance of 5%
- Internal thermal overload protection
- Internal Short-Circuit Limited
- No External Component
- Output Voltage 5.0V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 24V
- Offer in plastic TO-252, TO-220 & TO-263
- Direct Replacement for LM78XX

Packaging Information



Top View

1. Input
2. GND
3. Output

Absolute Maximum Rating

Parameter		LM78--	Unit
Input Voltage	LM7824, LM7827	40	V
	All Others	35	
Operating Free-Air, Case, Virtual Junction Temp.		0 to 150	°C
Storage Temperature Range		-65 to 150	
Lead temperature 1.6 mm from case for sec.		260	

Electrical Characteristics (LM7805)

(V_I=10V, I_O=500mA, 0°C ≤T_J≤125 °C, unless otherwise specified. (Note 1)

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Output Voltage	V_O	T_J= 25 °C	4.8	5.0	5.2	V
Line Regulation	ΔV_O	V_I = 7V to 25V T_J= 25 °C		3	100	mV
		V_I = 8V to 12V T_J= 25 °C		1	50	
Load Regulation	ΔV_O	I_O = 5mA to 1.5A, 25 °C		15	100	mV
		I_O = 250mA to 750mA, 25 °C		5	50	
Ripple Rejection	RR	V_I = 8V to 18V, f=120Hz	62	78		dB
Output Noise Voltage	V_N	F= 10Hz to 100Hz T_J= 25 °C		40		µV
Dropout Voltage	V_D	T_J= 25 °C		2.0		V
Quiescent Current		T_J= 25 °C		4.2	8	mA
Quiescent Current Change	ΔI_Q	V_I = 7V to 25V, T_J= 25 °C			1.3	mA
		I_O = 5mA to 1A, T_J= 25 °C			0.5	

Electrical Characteristics (LM7812)

(V_I=19V, I_O=500mA, 0°C ≤T_J≤125 °C, unless otherwise specified. (Note 1)

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
Output Voltage	V_O	T_J= 25 °C	11.50	12	12.5	V
Line Regulation	ΔV_O	V_I = 14.5V to 30V T_J= 25 °C		10	240	mV
		V_I = 16V to 22V T_J= 25 °C		3.0	120	
Load Regulation	ΔV_O	I_O = 5mA to 1.5A, 25 °C		12	240	mV
		I_O = 250mA to 750mA, 25 °C		4	120	
Ripple Rejection	RR	V_I = 15V to 25V, f=120Hz	55	71		dB
Output Noise Voltage	V_N	F= 10Hz to 100Hz TJ= 25 °C		75		µV
Dropout Voltage	V_D	T_J= 25 °C		2.0		V
Quiescent Current		T_J= 25 °C		4.3	8.0	mA
Quiescent Current Change	ΔI_Q	V_I = 14.5V to 30V, T_J= 25 °C			1.0	mA
		I_O = 5mA to 1A, T_J= 25 °C			0.5	