MICROCONRTOLLER BASED UNINTERRUPTIBLE POWER SUPPLY

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PROJECT REPORT

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CERTIFICATE

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II.SYNOPSIS

The Microcontroller based UPS system has been developed to provide continuos high quality sine wave power supply to vulnerable electronic equipments.The basic concept of UPS is to store energy during normal operation (through battery charge) and release energy (through DC to AC conversion) during a power failure.

It is very difficult if the operation is stopped in the middle due to the failure of supply. So by UPS system this problem can be eliminated upto an extent which depends on the ampere hours (AH) of the battery used in the system.

UPS systems are traditionally designed using analog components. Microcontroller has been integrated to control some important parameters such as inverter control ,low voltage control ,over voltage control and short circuit voltage protection etc...

By using Microcontroller the main advantages are the reduction of the hardware Units, core control features and operations can be changed by the software.

Battery voltage and the load voltage are displayed by using the 7 segment display unit.

CHAPTER-1

INTRODUCTION TO UPS

1.INTRODUCTION TO UPS

1.1. INTRODUCTION

At times, power from a wall socket is neither clean nor uninterruptible. Many abnormalities such as blackouts, brownouts, spikes, surges, and noise can occur. Under the best conditions, power interruptions can be an inconvenience. At their worst, they can cause loss of data in computer systems or damage to electronic equipment. It is the function of an Uninterruptible Power Supply (UPS) to act as a buffer and provide clean, reliable power to vulnerable electronic equipment. The basic concept of a UPS is to store energy during normal operation (through battery charging) and release energy (through DC to AC conversion) during a power failure.

For continuous power supply for critical loads even in the event of commercial power failure for a considerable period. UPS is only the solution.A proper UPS can provide good quality power to the load at all conditions of supply power . Uninterruptible power supplies (UPS) are designed to protect electronic equipment like computers and phone systems against problems stemming from a temporary failure in the power supply. By providing a constant source of electricity, a UPS can help prevent damage or data loss that can occur with the unexpected shutdown of computers, phone systems, and other sensitive equipment.

UPS systems work by detecting decreases in the amount of electricity coming from the wall circuit, and boosting power to maintain a constant flow of electricity to connected equipment. This power boost is provided either by a transformer that enhances a weak electrical flow, or from an internal battery that substitutes for the normal power source in the event of failure.

All UPS systems are not alike. There are three basic types of UPS available.

1.2.TYPES OF UPS

1.Line preferred
2.Line interactive
3.Inverter preferred

Standby, or off-line, units switch from the regular power source to an internal battery when they sense a power disturbance. There is a brief lag time before the internal battery comes on-line. This downtime should be brief enough, however, to avoid causing a computer to shut down.

Line-interactive UPS systems add a transformer to minimize the need to use an internal battery with every power fluctuation. These units monitor the line voltage at all times, activating the power transformer when the voltage falls below certain parameters. The battery is activated when even lower voltages are recorded.

On-line UPS units constantly supply power to connected equipment from an internal battery, with battery recharging occurring on an ongoing basis. There is no lag time when power failures occur since these units serve as the primary source of power to equipment. In the case of a blackout, the UPS will continue to generate power, but will be unable to recharge.

1.2.1.OFF-LINE LINE PREFERRED SYSTEMS:

This system includes a storage battery, a battery charger, a static inverter and a static automatic change-over switch. In this system the power is normally passed directly to the load via the static switch S_1 while S2 is off The battery charger is a stabilized one which maintains the battery on float at fully charged condition and at the same time provides stabilized power to the inverter .So long the utility supply is present the load is supplied by it and the inverter runs on no load .The inverter is phase-synchronized with utility supply.

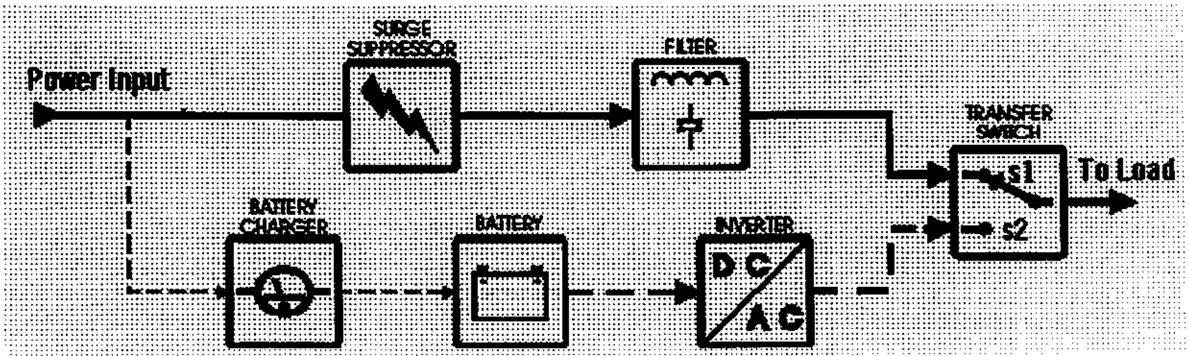
In case of utility power failure the load is transferred to the inverter power through static switch S2.At this condition the inverter runs from the battery which is capable to supply the total demand of power.The total transfer operation should be complete within ¼ cycle so that the operation of critical equipment is not disturbed.

During the outage period the battery has to supply full load and discharges quickly .The back-up time depends upon the ampere-hour capacity of the battery.The battery should be shed off the load when it discharges to a minimum voltage recommended by the manufacturer .

After the restoration of supply power ,the load is transferred to the line through S1 and S2 is switched off.The battery charger now charges the battery in constant current mode during which the battery voltage rises slowly.After the battery reaches the specified voltage,the charging mode automatically changes from constant current mode to constant voltage mode and begins boost charging so that the battery gets fully charged.

This system can not provide complete power protection and mode of operation has to be changed on power failure ,so its application is restricted to small systems where the operation is not highly critical.

In this type of UPS, the primary power source is line power from the utility, and the secondary power source is the battery. It is called a *standby* UPS because the battery and inverter are normally not supplying power to the equipment. The battery charger is using line power to charge the battery, and the battery and inverter are waiting "on standby" until they are needed. When the AC power goes out, the transfer switch changes to the secondary power source. When line power is restored, the UPS switches back.



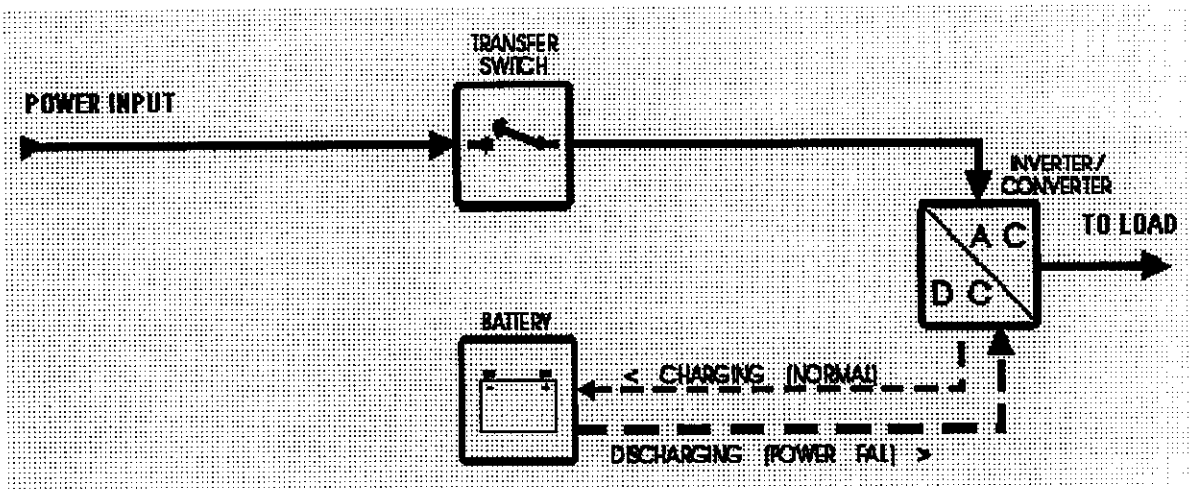
Block schematic of a standby UPS.

While the least desirable type of UPS, a standby unit is still a UPS and will serve well for most users. After all, if standby UPSes didn't work, they wouldn't sell. For a very critical function, however, such as an important server, they are not generally used. The issue with a standby UPS is that when the line power goes out, the switch to battery power happens very quickly, but not instantly. There is a delay of a fraction of a second while the switch occurs, which is called the switch time or transfer time of the UPS. While rare, it is possible for the UPS to not make the switch fast enough for the PC's power supply to continue operation uninterrupted. Again, in practice this does not normally occur or nobody would bother to buy these units. Still, we should compare the unit's transfer time to the hold time of our power supply unit, which tells us how much time the power supply can handle having its input cut off before being interrupted. If the transfer time is much less than the hold time, the UPS will probably work for us.Standby UPSes are usually available in a size range of up to about 1000 VA.

1.2.2.LINE-INTERACTIVE UPS

Essentially, this is still an Off-line UPS. The difference being that the filtering system is often better and that most of these types of UPS 's has a full sine wave output. These can be used with computer file servers and is still not recommended for major applications as it does not offer complete isolation from mains power problems. In areas with known bad power and where generator sets are used, these UPS's should be avoided as they are basically still Off-line UPS's.

The *line-interactive UPS* uses a totally different design than any type of standby UPS. In this type of unit, the separate battery charger, inverter and source selection switch have all been replaced by a combination *inverter/converter*, which both charges the battery and converts its energy to AC for the output as required. AC line power is still the primary power source, and the battery is the secondary. When the line power is operating, the inverter/converter charges the battery; when the power fails, it operates in reverse.



Block schematic of a line-interactive UPS.

The main advantage of this design is that the inverter/converter unit is always connected to the output, powering the equipment. This design allows for faster response to a power failure than a standby UPS. The inverter/converter is also normally fitted with circuitry to filter out noise and spikes, and to *regulate* the power output, providing additional power during brownouts and curtailing output during surges.

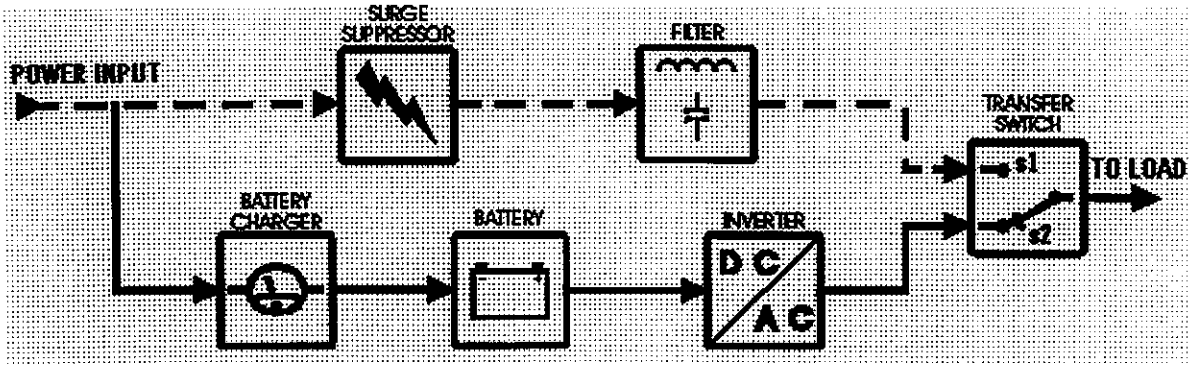
The line-interactive UPS is an improved design that is commonly used in units for home and business use, available in sizes up to 3,000 VA or so. It is superior to the standby UPS, but it still has a transfer time, and thus does not provide protection as good as the On-Line UPS.

1.2.3. ON LINE UPS:

By definition, this is the only real UPS as it can offer complete protection and isolation from bad mains power conditions. Make sure that you get TRUE On-line UPS's (double conversion topology) as there are many instances where UPS's are sold as On-line when they are definitely NOT.Its On-line structure is constantly regulating and filtering the output power when mains is present - thus continuously providing conditioned power!

As these UPS's have full sine wave output and offer the best protection they are the UPS's of choice when it comes to sensitive electronic equipment and critical applications - even in areas with bad power and where generators sets are used routinely !

The *online UPS*, sometimes called a *true UPS*, is the best type you can buy. Paradoxically, it is both very similar to, and totally opposite to, the least-expensive type, the standby UPS. It is very similar to it in that it has the same two power sources, and a transfer switch that selects between them. It is the exact opposite from the standby UPS because it has reversed its sources: in the online UPS the primary power source is the UPS's battery, and utility power is the *secondary* power source!



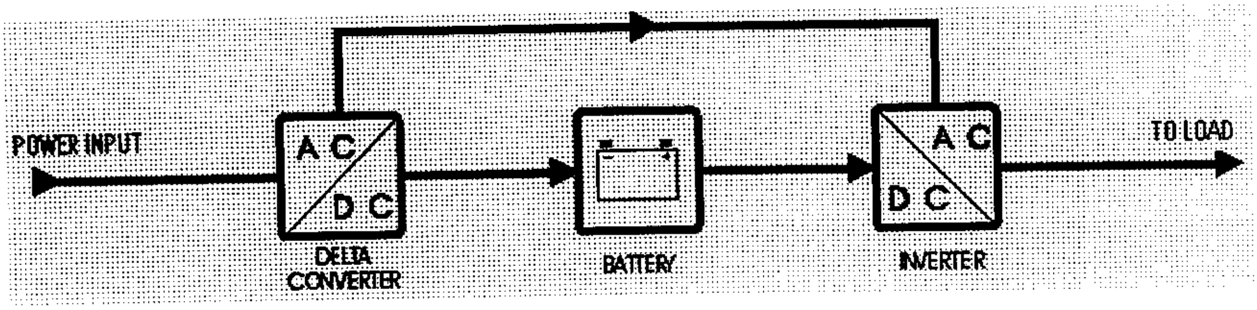
Block schematic of an online ("true") UPS.

Of course, while seeming small, this change is a very significant one. Under normal operation the online UPS is always running off the battery, using its inverter, while the line power runs the battery charger. For this reason, this type of UPS is sometimes also called a *double-conversion* or *double-conversion online* UPS. This design means that there is *no transfer time* in the event of a power failure--if the power goes out, the inverter (and its load) keeps chugging along and only the battery charger fails. A computer powered by an online UPS responds to a power failure in the same way that a plugged-in laptop PC does: it keeps running without interruption, and all that happens is that the battery starts to run down because there is no line power to charge it.

There is another key advantage to having the equipment running off the battery most of the time: the double-conversion process totally isolates the output power from the input power. Any nasty surprises coming from the wall affect only the battery charger, and not the output loads.

Even though it may appear from the schematic diagrams that the online UPS and standby UPS have the same components inside, this is not the case. The distinction is that there is a *big* difference between designing chargers and inverters that are normally sitting around doing nothing and only run say once a month for a few minutes, and designing ones that are running 24 hours a day for weeks on end. The additional engineering and the increased size and quality of the components combine to make online UPSes much more expensive than lesser designs. They are typically used only for large servers, and for backing up multiple pieces of equipment in data centers. They are available in sizes from about 5,000 VA up to hundreds of thousands of VA and even larger.

Aside from the cost, a disadvantage of the online UPS is its inefficiency. All the power going to the loads is converted from AC to DC and back to AC, which means much of the power is dissipated as heat. Furthermore, this is happening all the time, not just during a power failure, and while running equipment that draws a lot of power. To combat this shortcoming, a new design called a *delta-conversion online UPS* was created. "Delta" is the scientific term often used to refer to the *differential* between two quantities. In this design, the battery charger is replaced with a *delta converter*. Instead of providing all of the output from the battery under normal circumstances, some of it is provided directly by the delta converter from the input line power. In the event of a power failure, the delta converter stops operating and the unit acts like a regular double-conversion online UPS, since the inverter is also running off the battery all the time.

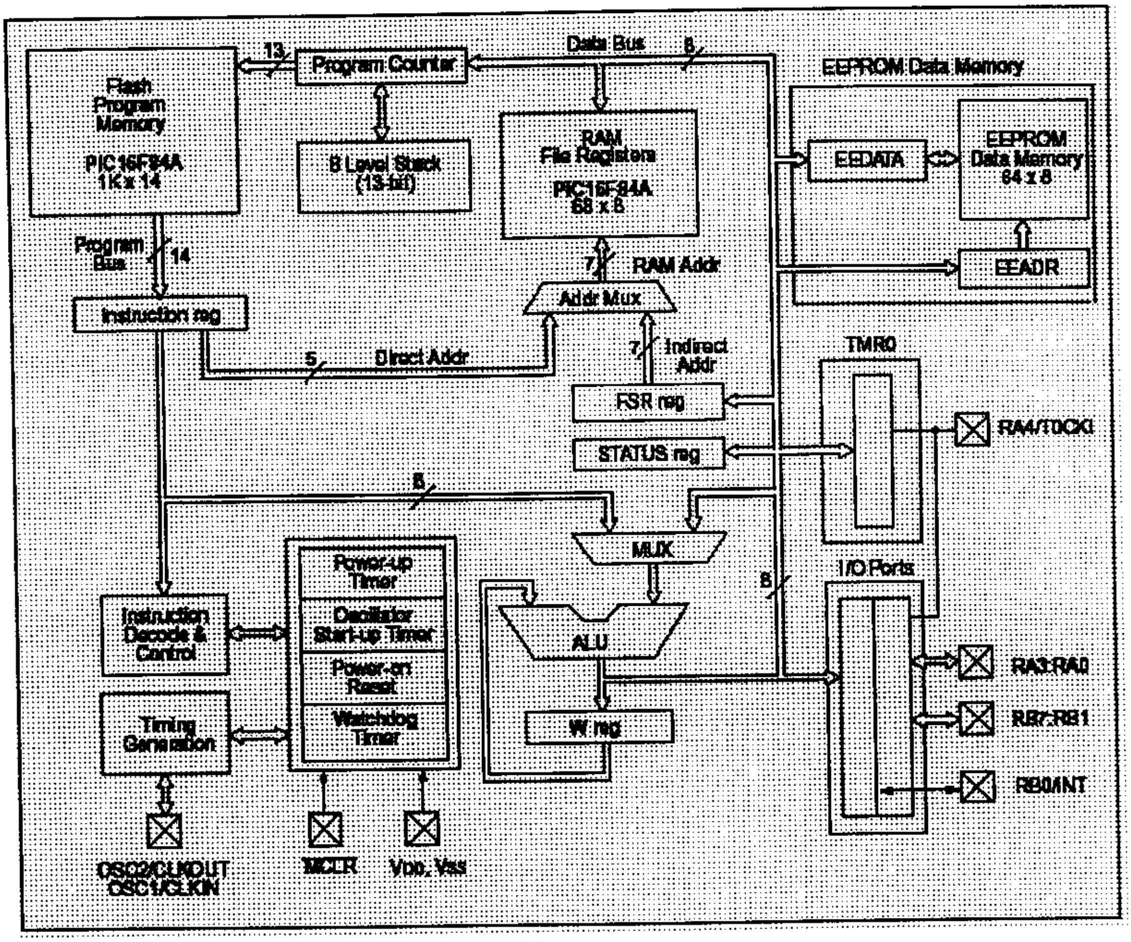


Simplified block schematic of a delta-conversion online UPS.

CHAPTER-2

ARCHITECTURE OF PIC16F84A

2.ARCHITECTURE OF PIC 16F84A



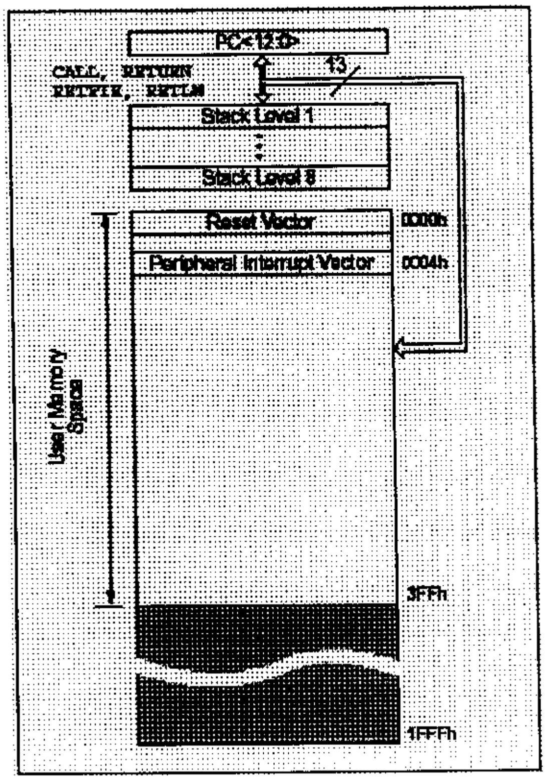
2.1MEMORY ORGANIZATION:

There are two memory blocks in PIC16F84A.These are program memory and the data Memory. The data memory consists of special function registers and general purpose RAM. The data memory also consists of Data EEPROM memory which has 64 bytes of address have 0H-3FH.

2.1.1.PROGRAM MEMORY ORGANIZATION:

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F84A, the first 1K x 14 (0000h-03FFh)are physically Implemented Reset vector is at 0000h and the interrupt

Program Memory Map& stack

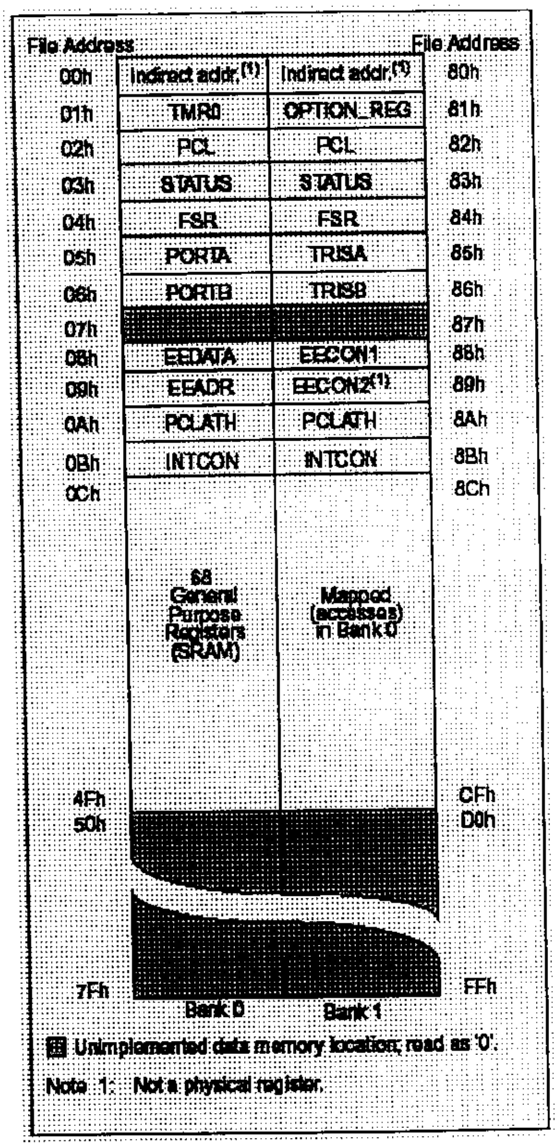


2.1.2.DATA MEMORY ORGANIZATION:

The data memory is partitioned into two areas. The first s the Special Function Registers (SFR) area, while the Second the General Purpose Registers (GPR) area. The SFR control the operation of the device. The GPR area is banked to allow greater than 116 bytes of general purpose RAM.

The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa. The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.4). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory. Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

REGISTER FILE MAP



File Address			File Address
00h	Indirect addr.[1]	Indirect addr.[1]	80h
01h	TMR0	OPTION_REG	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	▨	▨	87h
08h	EEDATA	EECON1	88h
09h	EEADR	EECON2[1]	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch 4Fh	68 General Purpose Registers (SRAM)	Mapped (accesses) in Bank 0	8Ch CFh
50h 7Fh	▨	▨	D0h FFh
	Bank 0	Bank 1	

▨ Unimplemented data memory location; read as '0'.

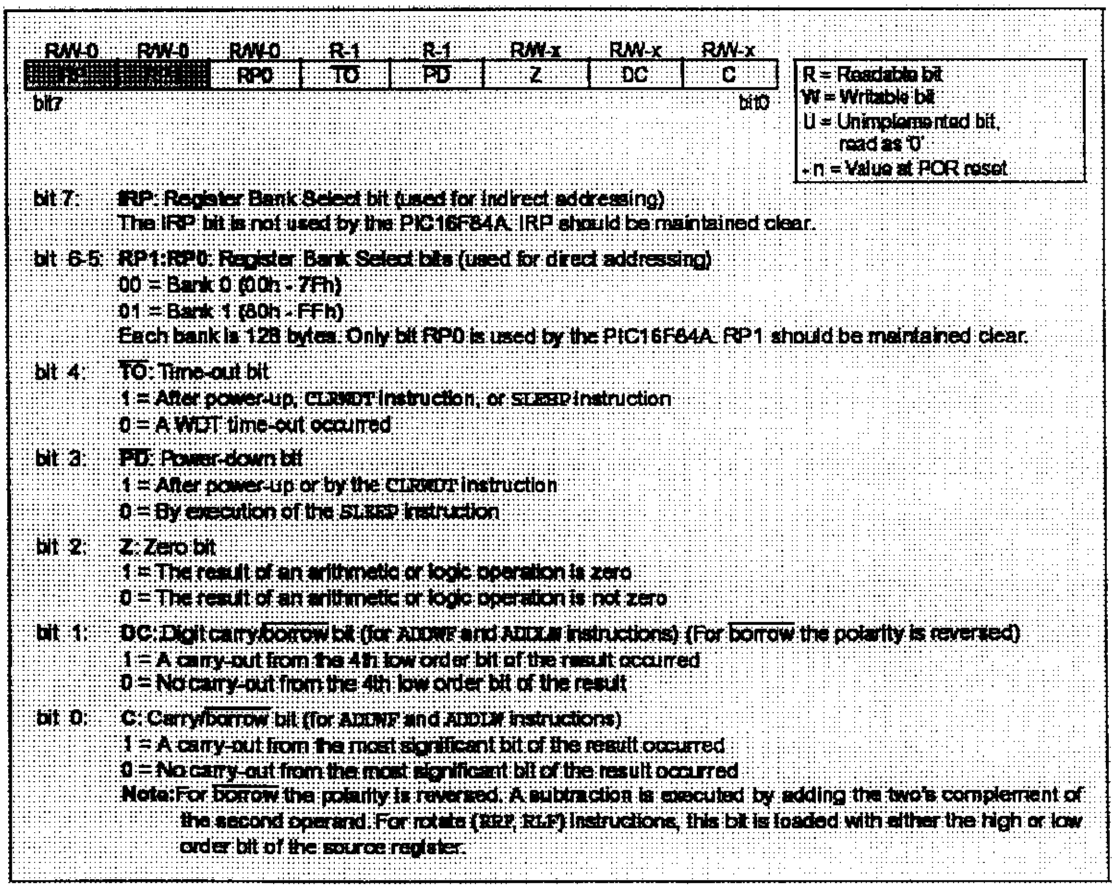
Note 1: Not a physical register.

2.2.REGISTERS

2.2.1.SPECIAL FUNCTION REGISTERS

The Special Function Registers are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM. The special function registers can be classified into two sets, core and peripheral.

STATUS REGISTER



R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit,
read as '0'
- n = Value at POR reset

bit 7: IRP: Register Bank Select bit (used for indirect addressing)
The IRP bit is not used by the PIC16F84A. IRP should be maintained clear.

bit 6-5: RP1:RP0: Register Bank Select bits (used for direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
Each bank is 128 bytes. Only bit RP0 is used by the PIC16F84A. RP1 should be maintained clear.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2: Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: DC: Digit carry/$\overline{borrow}$ bit (for ADDWF and ADDLW instructions) (For $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: C: Carry/$\overline{borrow}$ bit (for ADDWF and ADDLW instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory. As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended. For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged). Only the BCF, BSF, SWAPF and MOVWF instructions should be used to alter the STATUS register because these instructions do not affect any status bit.

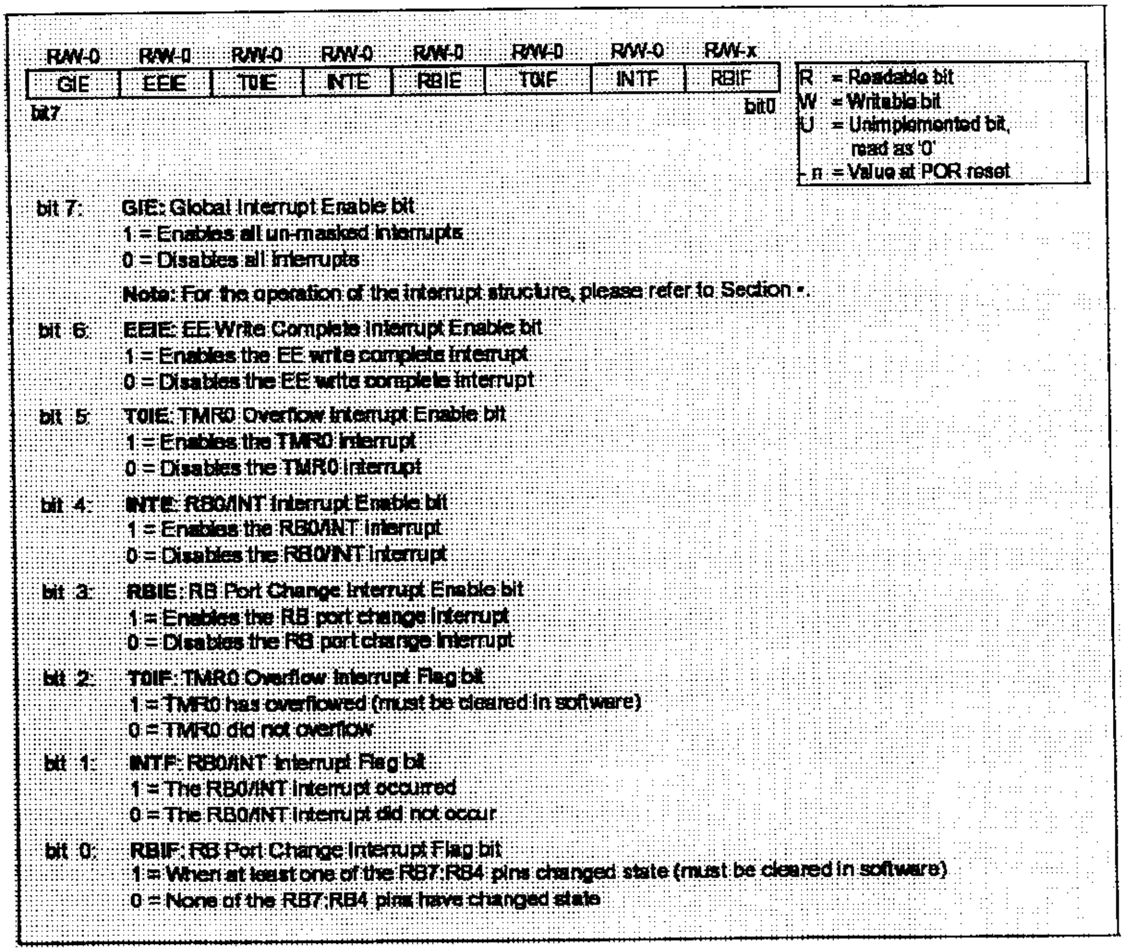
2.2.2.PCL AND PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

2.2.3.STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.Midrange devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed. After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

INTCON REGISTER



R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: GIE: Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts
Note: For the operation of the interrupt structure, please refer to Section •.

bit 6: EEIE: EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 5: T0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: INTE: RB0/INT Interrupt Enable bit
1 = Enables the RB0/INT interrupt
0 = Disables the RB0/INT interrupt

bit 3: RBIE: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: T0IF: TMR0 Overflow Interrupt Flag bit
1 = TMR0 has overflowed (must be cleared in software)
0 = TMR0 did not overflow

bit 1: INTF: RB0/INT Interrupt Flag bit
1 = The RB0/INT interrupt occurred
0 = The RB0/INT interrupt did not occur

bit 0: RBIF: RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

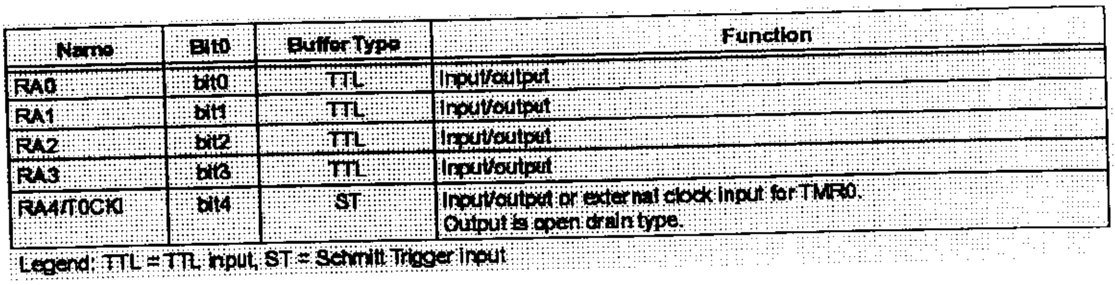
2.3.INPUT AND OUTPUT PORTS:

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

2.3.1.PORTA AND TRISA REGISTERS

PORTA is a 5-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin. Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

PORT A FUNCTIONS:

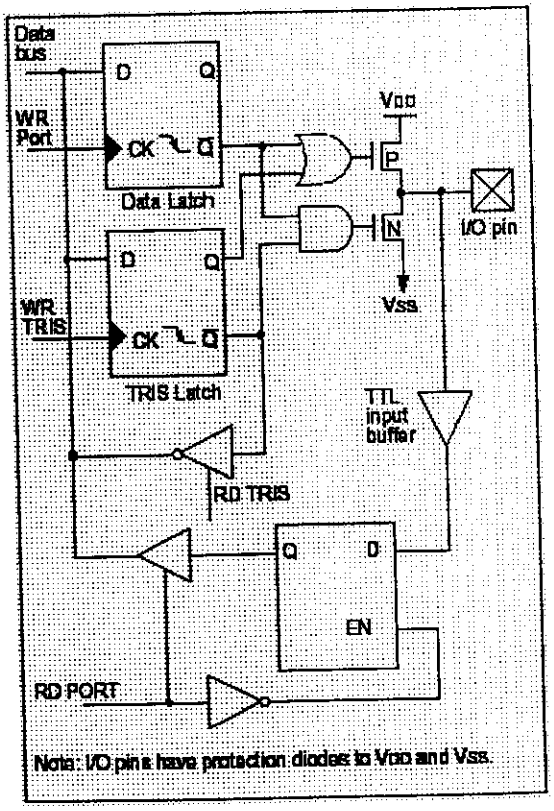


Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

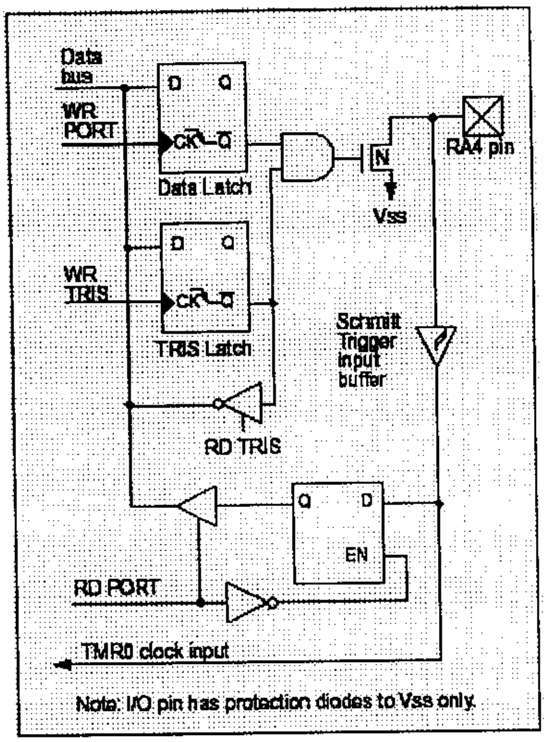
2.3.2.BLOCK DIAGRAM OF PORT A OF 16F84A

BLOCK DIAGRAM OF PINS RA3/RA0



Note: I/O pins have protection diodes to VDD and VSS.

BLOCK DIAGRAM OF PIN RA4



INITIALIZING PORTA

```
BCF STATUS, RP0 ;
CLRF PORTA ; Initialize PORTA by
; clearing output
; data latches
BSF STATUS, RP0 ; Select Bank 1
MOVLW 0x0F ; Value used to
; initialize data
; direction
MOVWF TRISA ; Set RA<3:0> as inputs
; RA4 as output
; TRISA<7:5> are always read as '0'.
```

2.4.PORTB AND TRISB REGISTERS

PORTB is an 8-bit wide bi-directional port. The corresponding data direction egister is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin.

INITIALIZING PORTB

```
BCF STATUS, RP0 ;
CLRF PORTB ; Initialize PORTB by
; clearing output
; data latches
BSF STATUS, RP0 ; Select Bank 1
MOVLW 0xCF ; Value used to
; initialize data
; direction
MOVWF TRISB ; Set RB<3:0> as inputs
; RB<5:4> as outputs
; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin con-figured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>). This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner: a) Any read or write of PORTB. This will end the mismatch condition. b) Clear flag bit RBIF. A mismatch condition will continue to set flag bit RBIF.Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared. The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

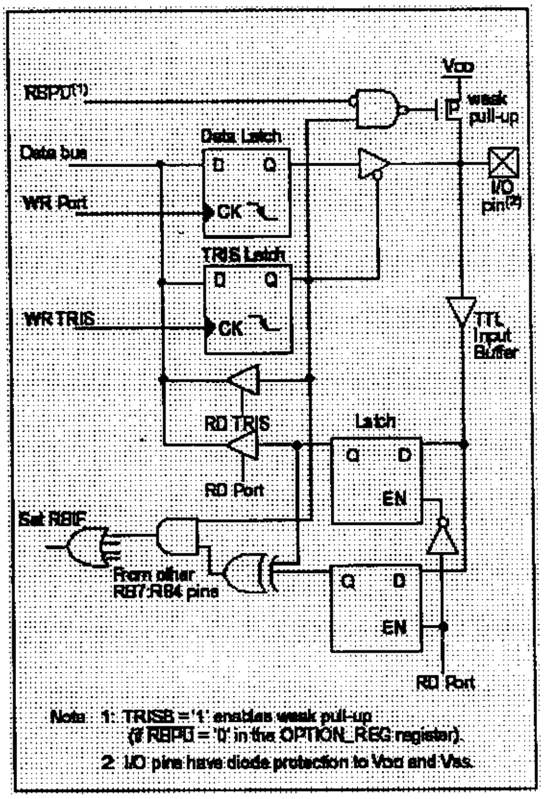
PORT B FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.

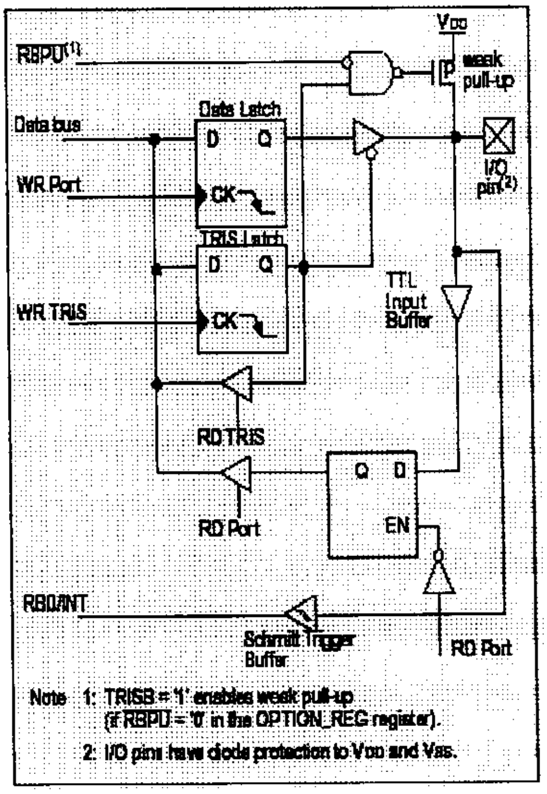
BLOCK DIAGRAM OF PORT B

BLOCK DIAGRAM OF PIN RB7&RB4



Note: 1: TRISB = '1' enables weak pull-up
(if $\overline{\text{RBPU}}$ = '0' in the OPTION_REG register).
2: I/O pins have diode protection to Vdd and Vss.

BLOCK DIAGRAM OF RB3&RB0



Note 1: TRISB = '1' enables weak pull-up
(if $\overline{\text{RBPU}}$ = '0' in the OPTION_REG register).
2: I/O pins have diode protection to Vdd and Vss.

2.5.TIMER 0

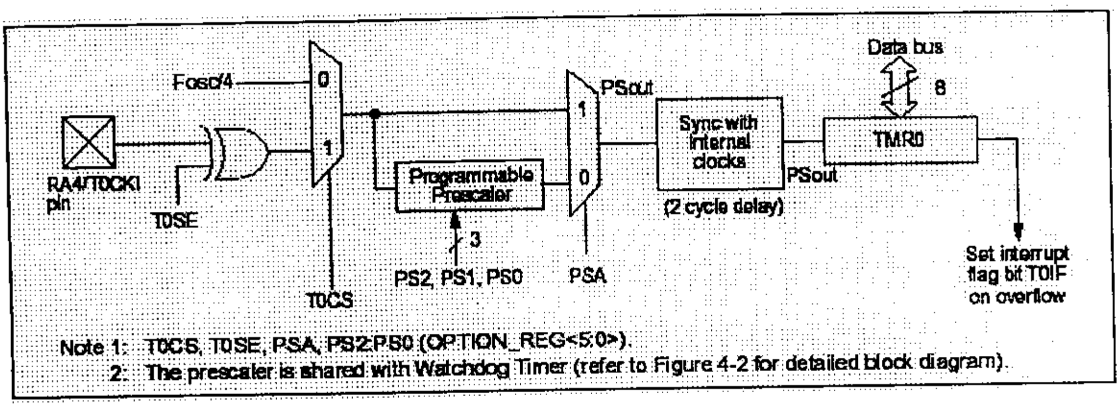
The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

2.5.1.TIMER0 OPERATION

Timer0 can operate as a timer or as a counter. Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register. Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below. When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

BLOCK DIAGRAM OF TIMER0



Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 4-2 for detailed block diagram).

CHAPTER-3

INSTRUCTION SET SUMMARY

3.INSTRUCTION SET SUMMARY

3.1. TYPES OF INSTRUCTION

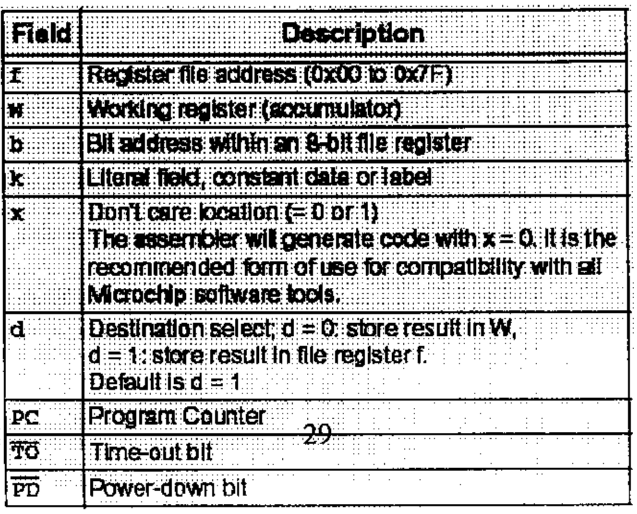
Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

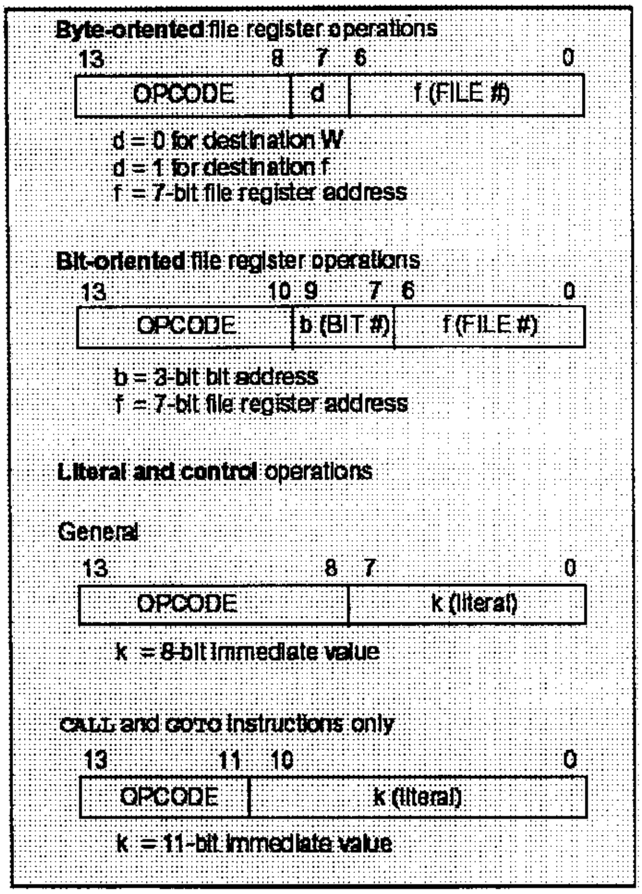
For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

OP CODE FIELD DESCRIPTIONS:



Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit

GENERAL FORMAT FOR INSTRUCTIONS



Byte-oriented file register operations

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

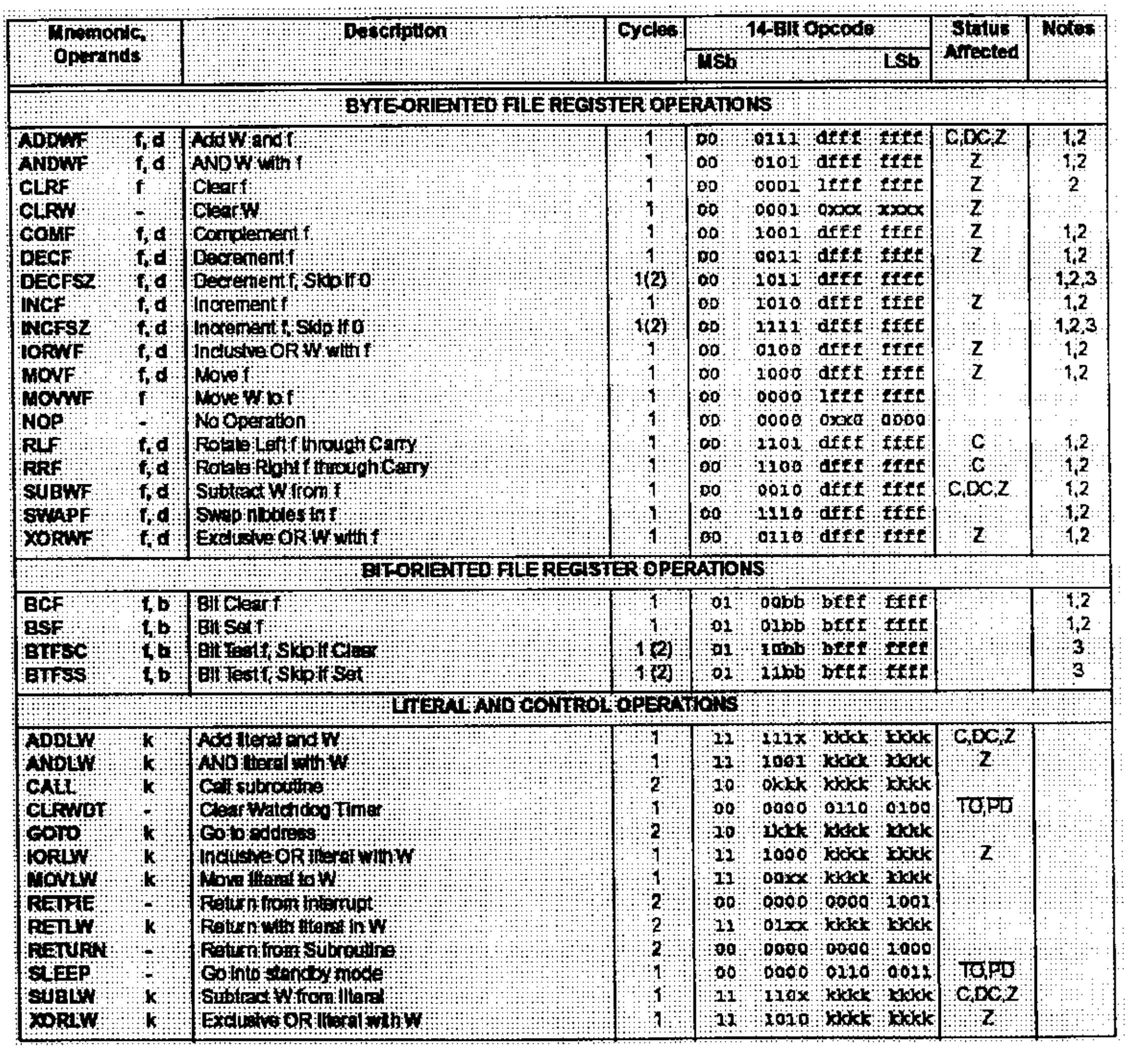
General

k = 8-bit immediate value

CALL and GOTO instructions only

k = 11-bit immediate value

INSTRUCTIONS SET :



Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

3.2.I/O PROGRAMMING CONSIDERATIONS

3.2.1. BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch is unknown. Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e., BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch. A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

3.2.2.SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port. Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

3.2.3.SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F8X has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These features are:

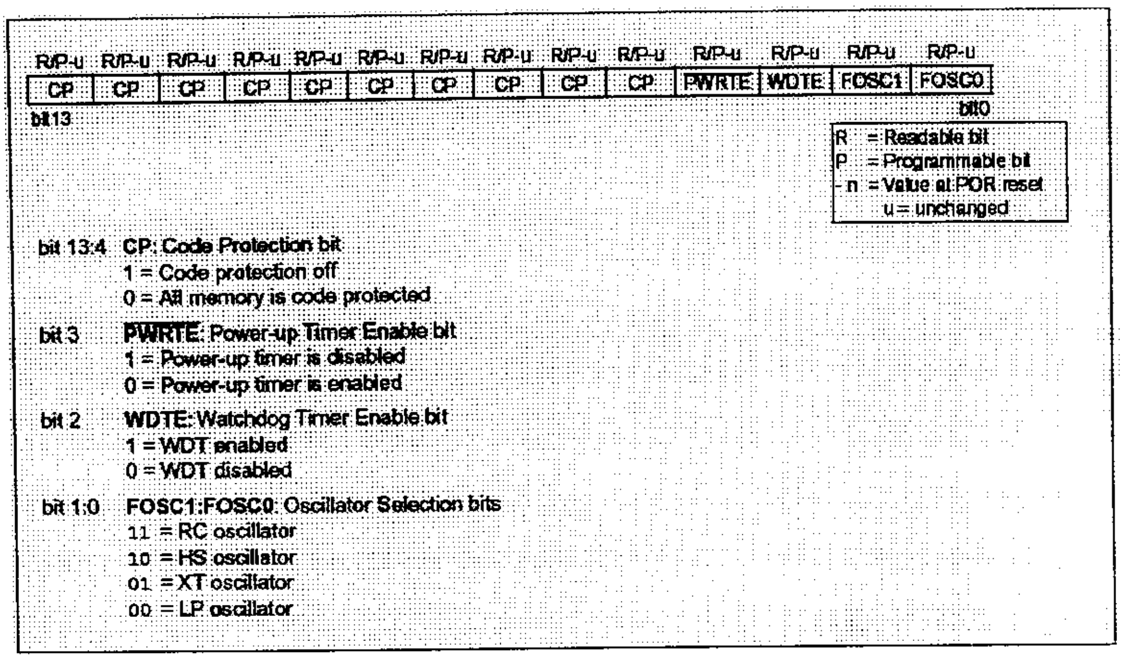
- OSC Selection
- Reset - Power-on Reset (POR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16F8X has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added eliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry. SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

3.2.4.CONFIGURATION BITS

The configuration bits can be programmed (read as '0') or left un programmed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h. Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming. To find out how to program the PIC16C84, refer to PIC16C84 EEPROM Memory Programming Specification (DS30189).

CONFIGURATION WORD -16F84A



R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	PWRTE	WDTE	FOSC1	FOSC0
bit13													bit0

R = Readable bit
P = Programmable bit
- n = Value at POR reset
u = unchanged

bit 13:4 **CP: Code Protection bit**
1 = Code protection off
0 = All memory is code protected

bit 3 **PWRTE**: Power-up Timer Enable bit
1 = Power-up timer is disabled
0 = Power-up timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1:0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

3.3.OSCILLATOR CONFIGURATIONS

3.3.1.OSCILLATOR TYPES

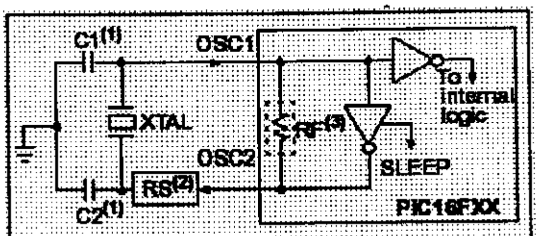
The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

(i) CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation .

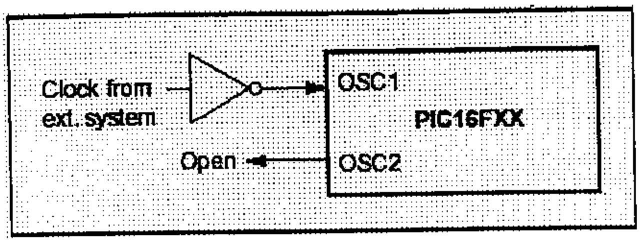
Crystal /Ceramic Resonator Operation



Note1: See Table 6-1 for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen.

The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin

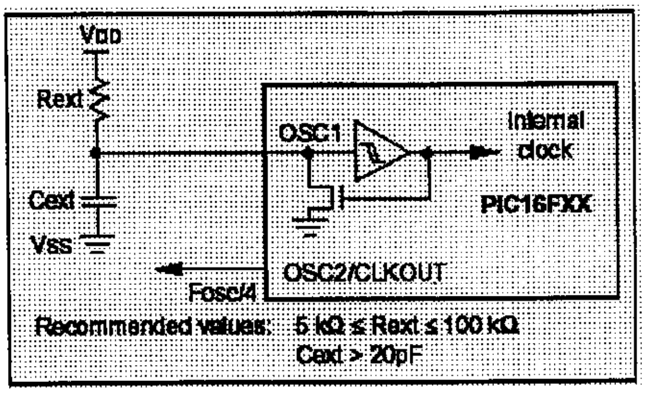
EXTERNAL CLOCK I/P OPERATION



(ii) RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) values, capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low Cext values. The user needs to take into account variation due to tolerance of the external R and C components.

RC OSCILLATOR

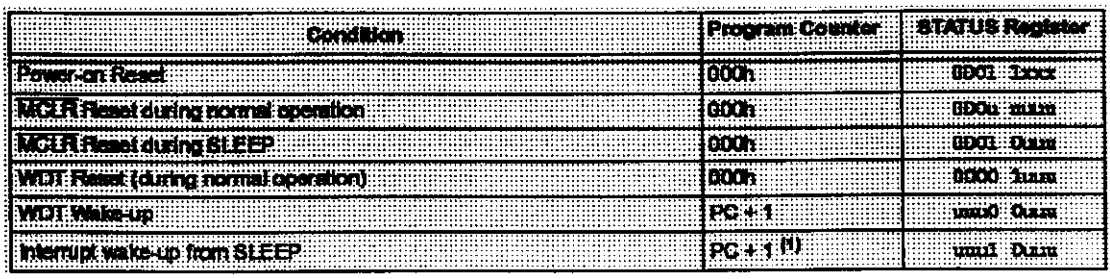


3.4.RESET

The PIC16F84A differentiates between various kinds of reset:

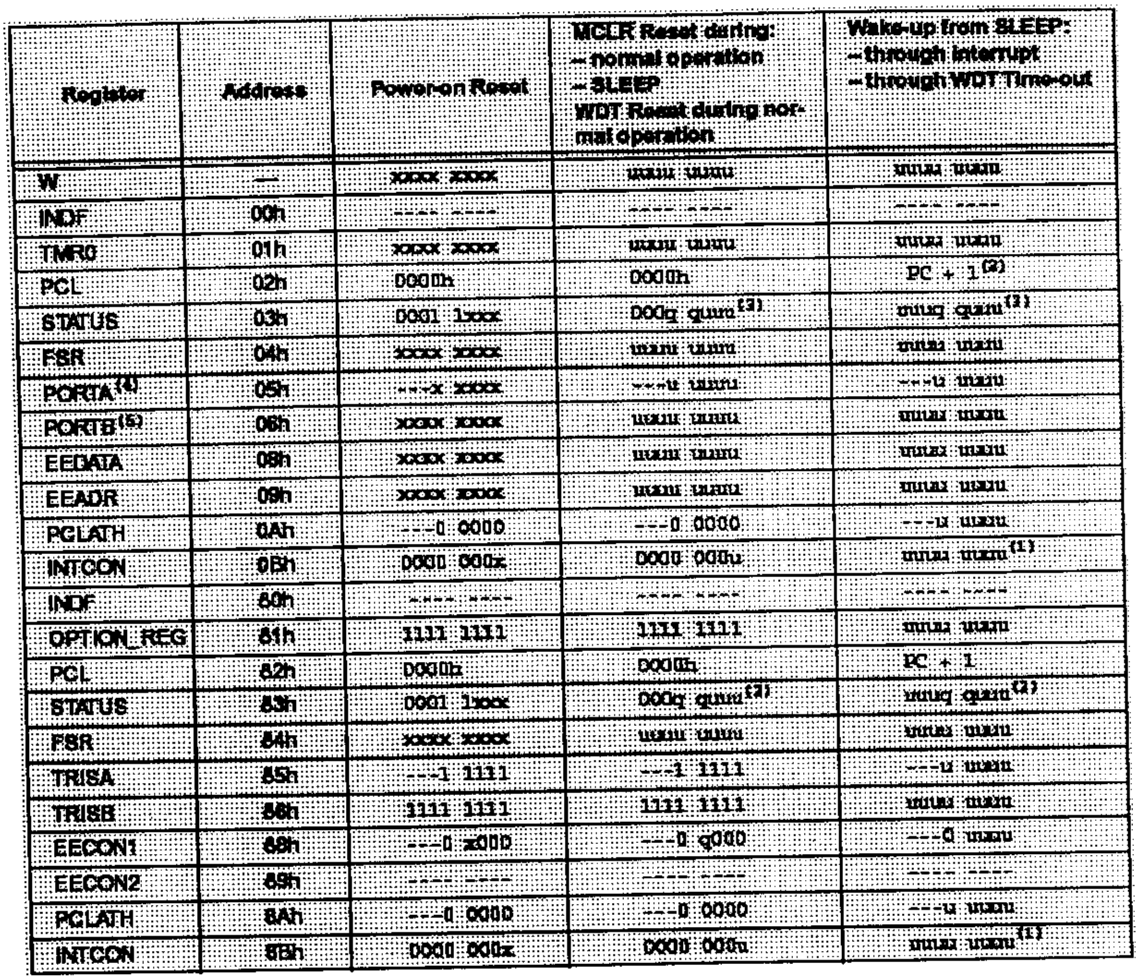
- Power-on Reset (POR)
- MCLR reset during normal operation
- MCLR reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

RESET CONDITION FOR PC AND SR



Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 [1]	uuu1 0uuu

RESET CONDITIONS FOR ALL REGISTERS



Register	Address	Power-on Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1[2]
STATUS	03h	0001 1xxx	000q quuu[3]	uuuq quuu[3]
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA[4]	05h	---x xxxx	---u uuuu	---u uuuu
PORTB[5]	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu[1]
INDF	80h	---- ----	---- ----	---- ----
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000q quuu[3]	uuuq quuu[3]
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu[1]

3.4.1.POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details. When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. For additional information, refer to Application Note AN607, " Power-up Trouble Shooting." The POR circuit does not produce an internal reset when VDD declines.

3.4.2.POWER-UP TIMER (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 msnominal time-out (TPWRT) from POR . The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level .A configuration bit, PWRTE, can enable/disable the PWRT.The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation.

3.4.3.OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends . This ensures the crystal oscillator or resonator has started and stabilized. The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP. When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case, an external power-on reset circuit may be necessary .

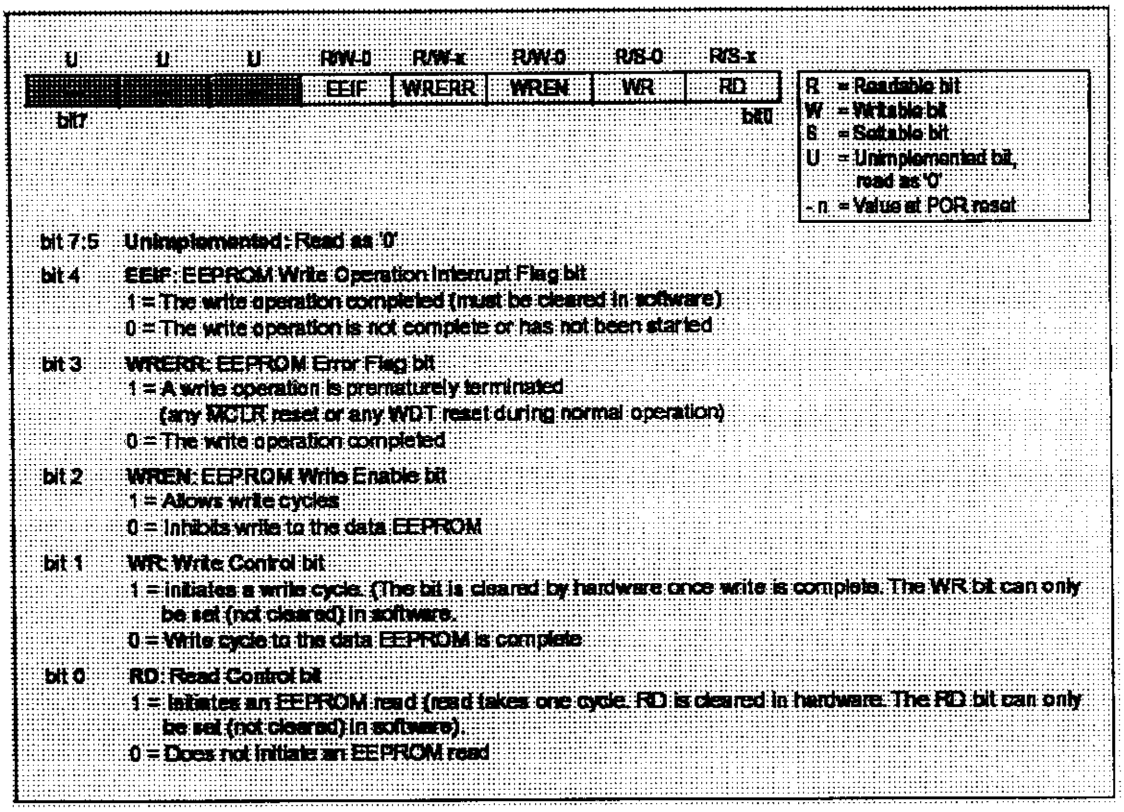
3.5.DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2 (Not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F84A devices have 64 bytes of data. EPROM with an address range from 0h to 3Fh. The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits. When the device is code protected, the CPU may continue to read and write the data EEPROM memory.The device programmer can no longer access this memory.

EECON 1 REGISTER(Address 88H)



U	U	U	R/W-0	R/W-x	R/W-0	R/S-0	R/S-x
▨	▨	▨	EEIF	WRERR	WREN	WR	RD
bit7							bit0

R = Readable bit
W = Writable bit
S = Settable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7:5 Unimplemented: Read as '0'

bit 4 EEIF: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 WRERR: EEPROM Error Flag bit
1 = A write operation is prematurely terminated
(any $\overline{MCLR}$ reset or any WDT reset during normal operation)
0 = The write operation completed

bit 2 WREN: EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 WR: Write Control bit
1 = initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
0 = Write cycle to the data EEPROM is complete

bit 0 RD: Read Control bit
1 = Initiates an EEPROM read (read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software).
0 = Does not initiate an EEPROM read

3.5.1.READING THE EEPROM DATA MEMORY

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation)

3.5.2.WRITING TO THE EEPROM DATA MEMORY

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

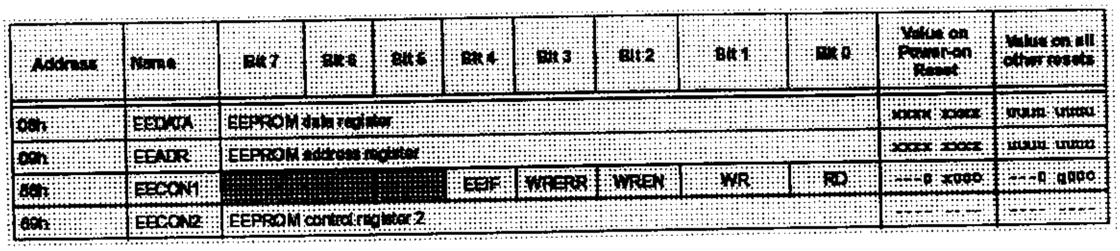
The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set. At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can eitherenable this interrupt or poll this bit. EEIF must be cleared by software.

3.5.3.WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit. The Total Endurance disk will help determine your comfort level. Generally the EEPROM write failure will be a bit which was written as a '0', but reads back as a '1' (due to leakage off the bit).

REGISTER/BITS ASSOCIATED WITH DATA EEPROM



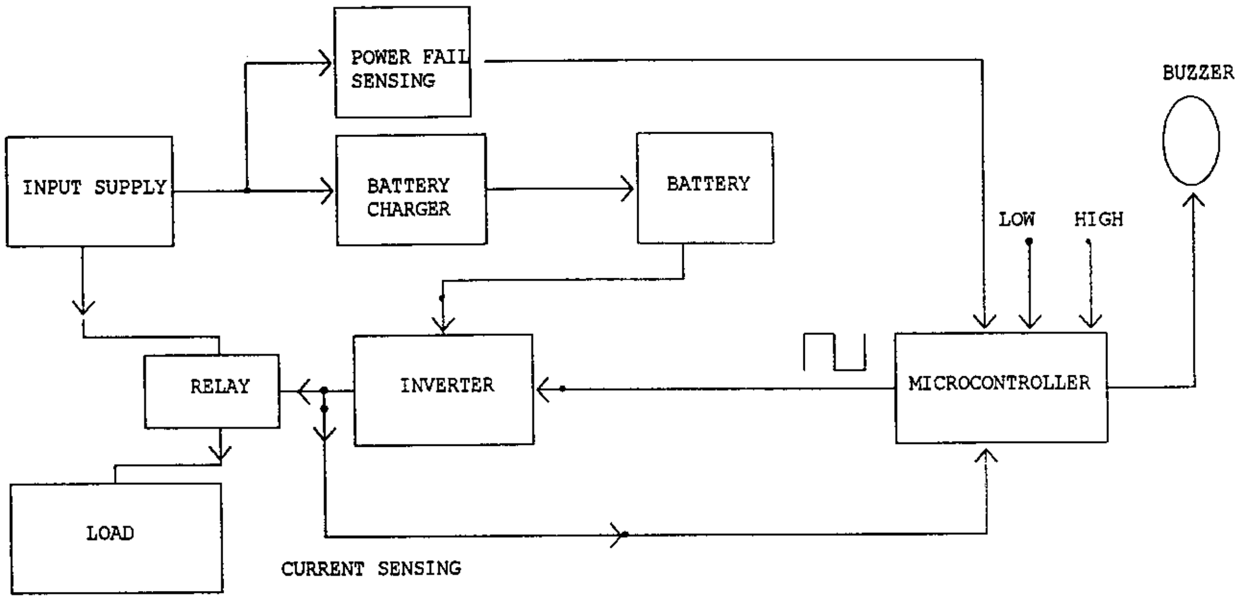
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
88h	EECON1				EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2								---- ----	---- ----

CHAPTER-4

HARDWARE IMPLIMENTATION

4.HARDWARE IMPLEMENTATION :

BLOCK DIAGRAM:



The following are the essential parts of the Microcontroller Based UPS

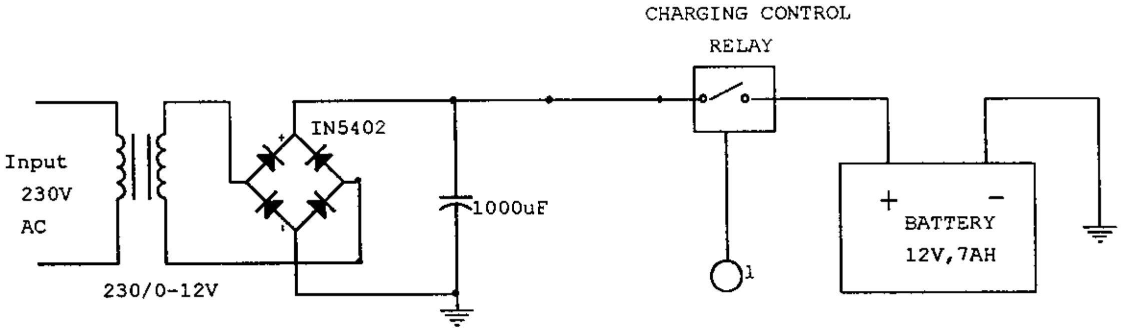
- Battery Charger
- Battery
- Inverter
- Power supply
- Microcontroller(16F84A)
- Transformer
- Current sensor
- Voltage sensor
- Display

4.1.BATTERY CHARGER:

The battery charger consist the following

- Step-down Transformer
- Bridge rectifier
- Filter
- Regulator
- Charging control relay

BATTERY CHARGER CIRCUIT:

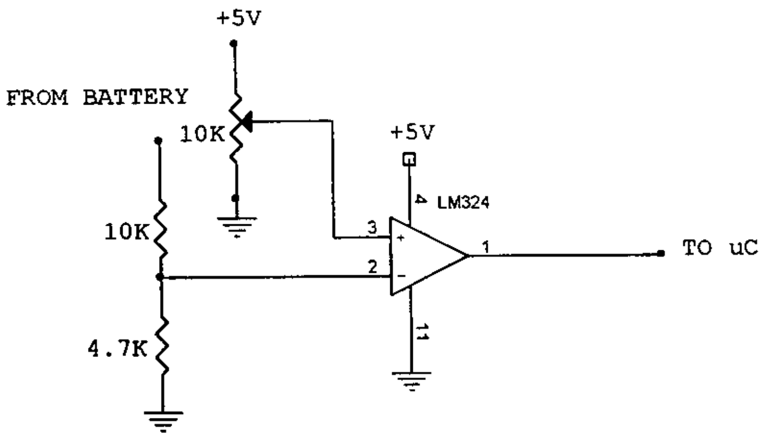


The 230/0-12V step-down transformer is used to step down the voltage from 230V a.c to 12V a.c.The bridge rectifier circuit coverts 12v AC to 12v DC.The filtering circuit consist of a capacitor of 1000uF which filters the ripple contents in the rectifier output. The relay is used to prevent the reverse flow of battery voltage to the supply.The relay coil is activated and controlled by DC when the power supply is cut off.

4.2. BATTERY

A 12v 7AH battery is used to store the DC power.The backup time of the battery depends upon the battery AH's.To charge the battery it recquires 12 to 13.5v DC,750milliAmps current .300 milliAmps per hour is required for the trickle charging.

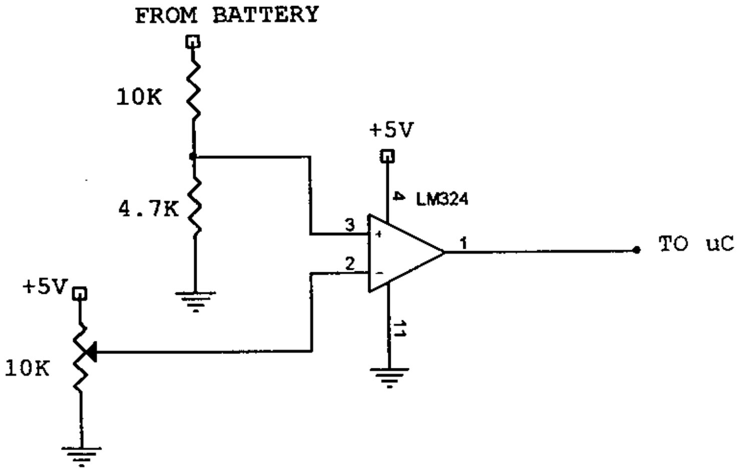
4.3.LOW VOLTAGE CUT-OFF:



BATTERY LOW VOLTAGE CUT-OFF

An Op-amp (LM324) is used as the comparator to detect the low voltage.The non-inverting mode input is set to a preset value of 10.5.The battery output to the inverting input of Op-amp.When the voltage goes below the set value the op-amps sends signal to uC and cut off the supply.

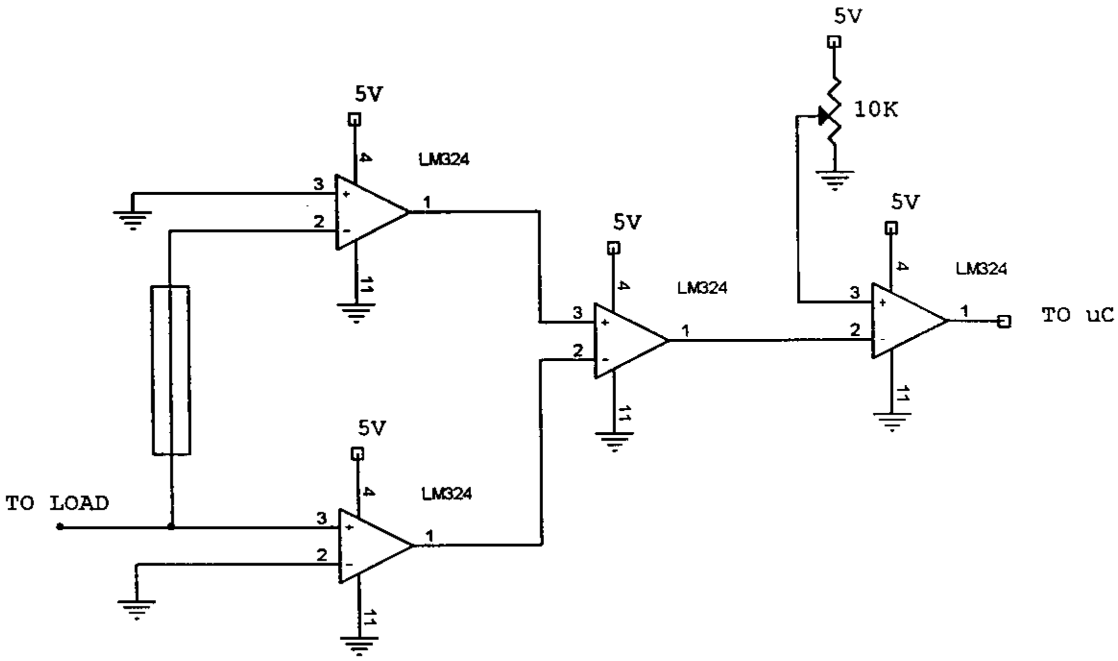
4.4.OVER VOLTAGE CUT-OFF:



BATTERY OVER CHARGE CUT-OFF

An Op-amp (LM324) is used as the comparator to detect the over voltage.The inverting mode input is set to a preset value of 13.5.The battery output to the non-inverting input of Op-amp.When the voltage goes above the set value the op-amps sends signal to microcontroller and the microcontroller cut off the supply to the battery by sending signal to energize the coil of charging control relay.

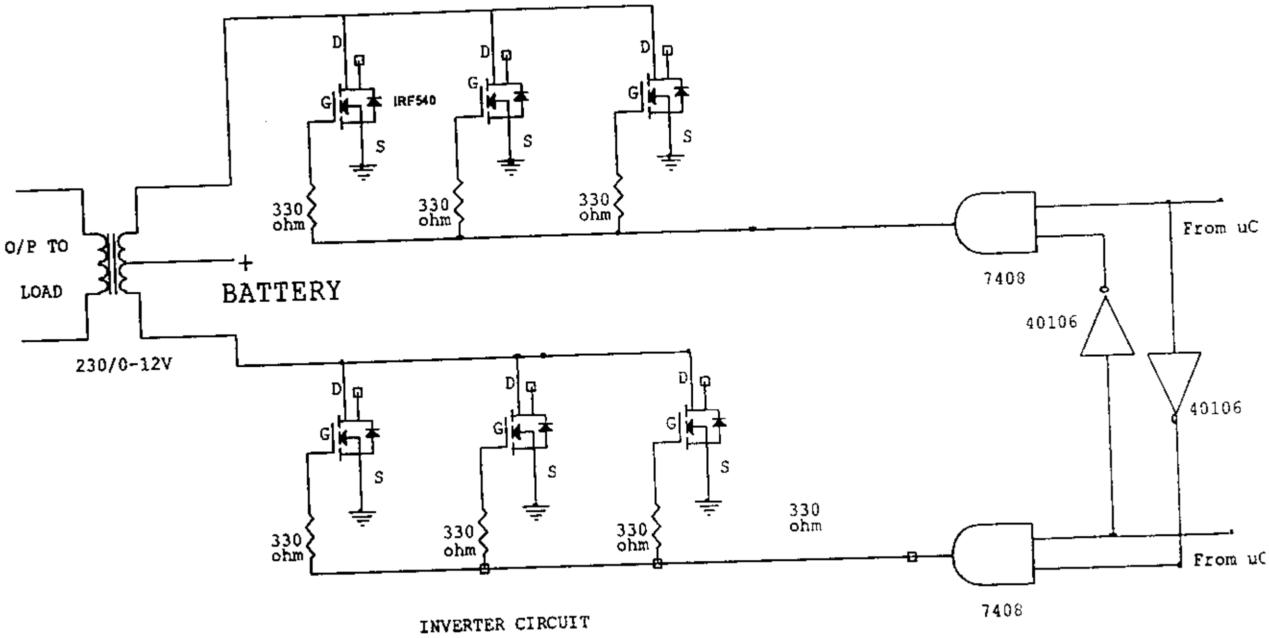
4.5.SHORT CIRCUIT PROTECTION:



SHORT CIRCUIT PREVENTER

A shunt is provided to measure the current flow and to prevent the circuit from short circuit.The output from the shunt is given to Op-amp and is compared with the set value and output of the Op-amp is given to Micro-controller.

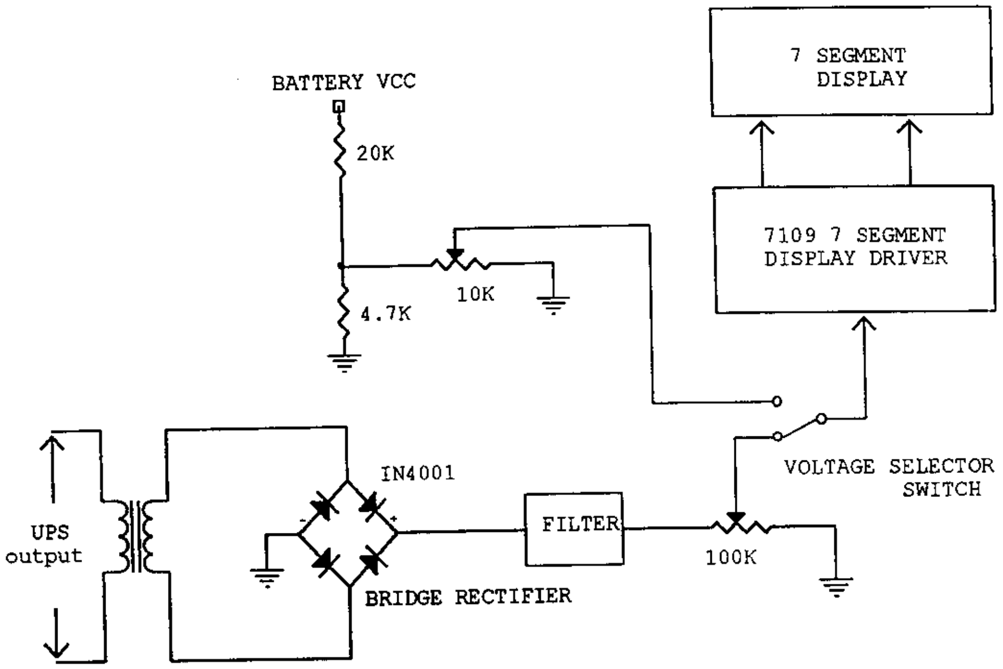
4.6.INVERTER:



INVERTER CIRCUIT

The inverter circuit is used to convert d.c to a.c. MOSFETs are used in inverters. The trigger signal to the inverter is given by microcontroller. IRF 540(MOSFET) is used in this circuit. The AND and NOT logics are used to avoid the MOSFETs trigger at the same time. The control signal to the gate of the inverter is given from the microcontroller.

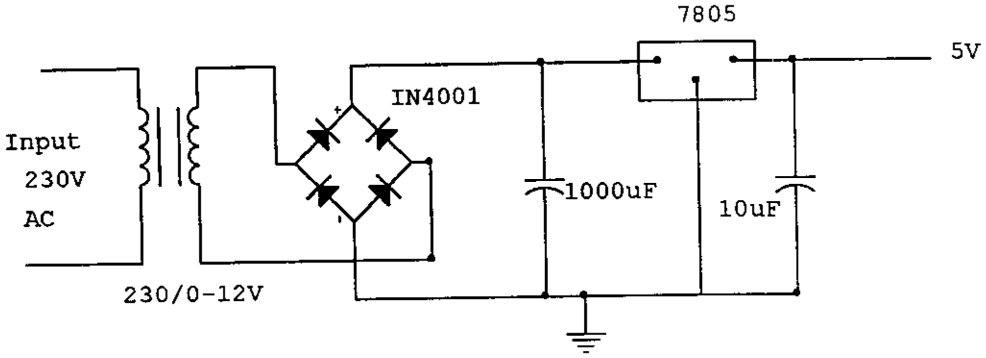
4.7.DISPLAY:



7 SEGMENT DISPLAY

The seven segment LED display is used to display the output voltage and the battery voltage.The output from the inverter is given to the step-down transformer and is step-downed to 12V.Then it is filtered and given to the switch.The battery voltage also given to one end of the voltage selector switch.The switch is placed in any one of the position to get the corresponding voltage.Ic 7109 isused to drive the seven segment LED display.

4.8.POWER SUPPLY:



POWER SUPPLY

To give supply to the microcontroller and other ICs power supplies are used. The 230/0-12V step-down transformer is used to step down the voltage from 230V a.c to 12V a.c.The bridge rectifier circuit coverts 12v ac to 12v ac.bridge rectifier circuit coverts 12v ac to 12 v dc.The filtering circuit consist of a capacitor of 1000uF which filters the ripple contents in the rectifier output. The regulator IC7805 is used to get regulator 5v dc output and used to give power to the ICs.

CHAPTER-5

SOFTWARE CODING

5.SOFTWARE CODING

```
     list p=16F84A
     #include p16F84A.inc

   org 0x00h
   goto start

   org 0x04h

;*************************INT_VEC_ADD  FLAG CHECK******************

   bcf STATUS,6
   bcf STATUS,5

   btfsc PIR1,0
   goto timer1

;** *************************** MAIN LOOP ****************************

    org 0x50h

start  bcf STATUS,6
       bsf STATUS,5
       clrf TRISb
       movlw h'ff'
       movwf ADCON1
       bsf PIE1,0

       bcf STATUS,5
       movlw h'3c'
     movwf 63
    movwf ADCON0
    movlw h'20'
    movwf 67
    movlw h'12'
    movwf 60
    bcf PIR1,0
    movlw h'00'
    movwf TMR1L
    movlw h'00'
    movwf TMR1H
    bsf INTCON,7
    bsf INTCON,6
    bsf INTCON,5
    bcf 22,6
    bsf 22,5

;************************** 50 HZ GENERATION *************************

timer1  bcf STATUS,5
        bcf PIR1,0
        decfsz 49,1
        goto step
        movlw h'23'
        movwf 49

step    decfsz 60,1
       goto end1
       movlw h'12'
       movwf 60
       btfsc 22,7
```

```
        goto t_on
        bsf 22,7
        movlw 0x00
        movwf PORTB
        goto end1

t_on    bcf 22,7
        movlw 0xff
        movwf PORTB
        goto end1

end1    decfsz 30,1
        goto stop
        movlw h'09'
        movwf 30
        decfsz 23,1
        goto led
        goto v_offl

led     btfss 22,6
        goto v_offl
        btfsc 22,0
        goto off
        bsf 22,0
        bsf PORTA,5
        goto stop

off     bcf 22,0
        bcf PORTA,5
        goto stop
```

```
 stop   retfie

;*************************** ADC ROUTINE ***************************

adc    bsf STATUS,5
       movlw h'8e'
       movwf ADCON1
       bcf STATUS,5
       movlw h'01'
       movwf ADCON0
       call dis_delay
       bsf ADCON0,2
       nop
       nop

 loopadc  btfsc ADCON0,2
        goto loopadc
        movf ADRESH,0
        movwf 31
        bsf STATUS,5
        movf ADRESL,0
        bcf STATUS,5
        movwf 32


 ;***************************VOLTAGE CHECK ***************************

 v_check  bcf STATUS,5
          bsf PORTA,5
 h_off   movlw h'b2'
        xorf 32,0
        btfsc STATUS,1
       goto low_off
       goto s_down

low_off  movlw h'93'
       xorf 32,0
       btfsc STATUS,1
       goto s_down
       goto adc

s_down   clrf PORTB
       bcf INTCON,7
Y        goto Y

delay_200  movlw h'45'
           movwf 20
s4         movlw h'ff'
         movwf 21
s3       nop
         nop
         nop
         nop
         nop
         nop
         nop
         nop
         decfsz 21,1
         goto s3
         decfsz 20,1
         goto s4
         return
```

```
dis_delay
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        return

;*****************************************************************************
end
```

CHAPTER-6

CONCLUSION

6.CONCLUSION

The Microcontroller based uninterruptible power supply system was designed, fabricated, assembled and tested. The set up can be tested for its high quality sine wave output.

We would like to state that our efforts towards successful completion of this project has helped us gain a lot of knowledge and practical experience.

SCOPE OF FUTURE WORK

Rectifier Unit can be replaced with control rectifier unit to achieve affective battery charging control using Microcontroller.

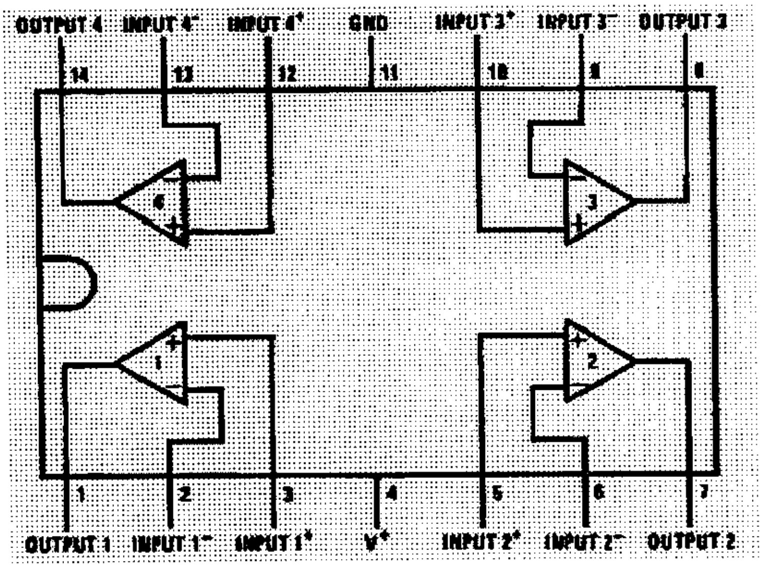
LCD can be interfaced with microcontroller to display battery voltage and output voltage.Back up time of the system can also be displayed with the help of microcontroller.

An ac-ac step up chopper can be used instead of the output transformer to get the a high frequency output.

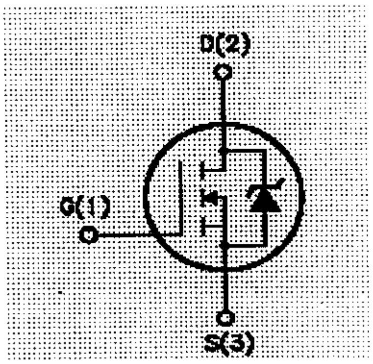
APPENDIX

APPENDIX

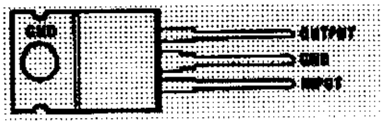
PIN DIAGRAM OF LM324(OP-AMP)



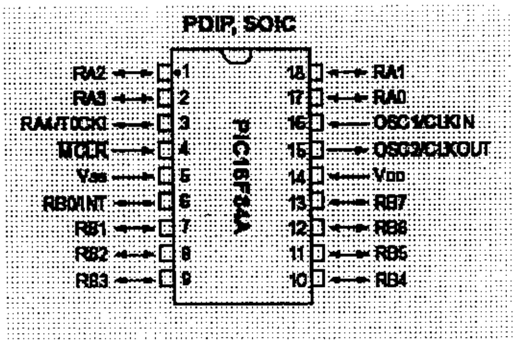
INTERNAL SCHEMATIC DIAGRAM OF IRF 540

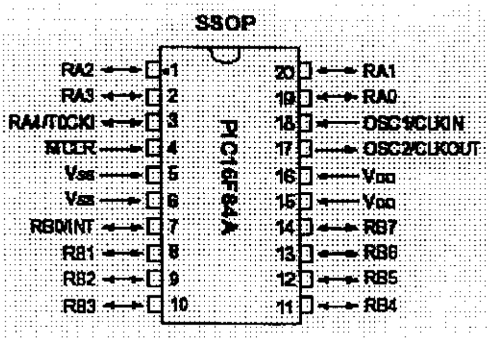


PIN DIAGRAM OF 7805

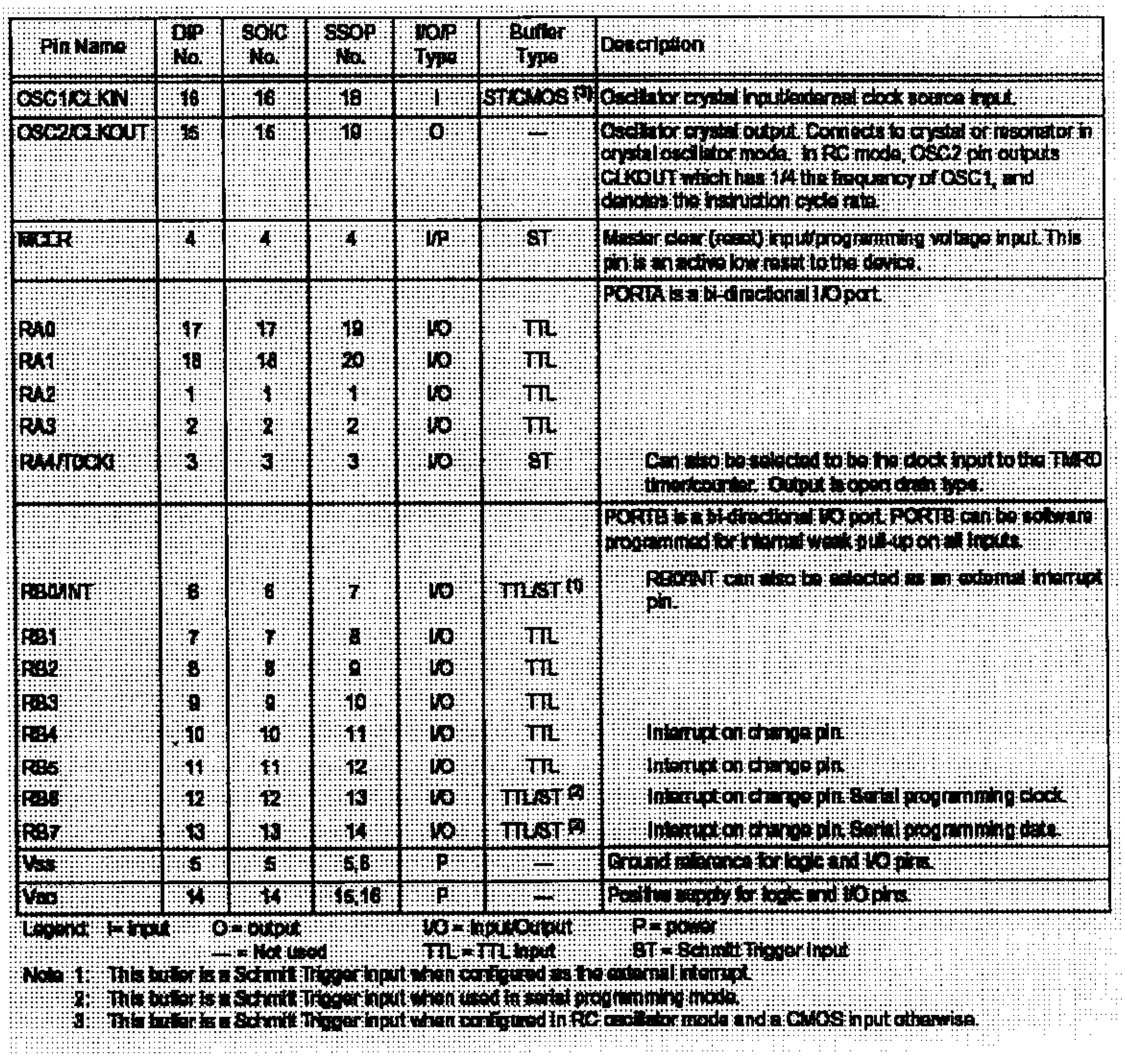


PIN DIAGRAM OF PIC 16F84A





PIN DISCREPTION OF PIC16F84A



Pin Name	DIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS[3]	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	17	17	19	I/O	TTL	
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	7	I/O	TTL/ST[1]	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupt on change pin.
RB5	11	11	12	I/O	TTL	Interrupt on change pin.
RB6	12	12	13	I/O	TTL/ST[2]	Interrupt on change pin. Serial programming clock.
RB7	13	13	14	I/O	TTL/ST[2]	Interrupt on change pin. Serial programming data.
Vss	5	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = Input/Output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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BIBLIOGRAPHY

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-ROY CHOWDHRY

WEBSITES:

*WWW.MICROCHIP.COM