Register Number:……..

KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2022

(Regulation 2018)

Third Semester

INFORMATION TECHNOLOGY

U18ITT3001 Computer Architecture

COURSE OUTCOMES

CO1: **Explain micro level operations of computer using the concepts of hardware and software coordination.**

CO2: **Compare different types of memories and their performances.**

CO3: **Apply the knowledge of binary arithmetic operations to understand the design of hardware components**

CO4: **Enumerate various control methodologies using programming and their effect on the hardware components**

CO5: **Describe the performance enhancement techniques for data handling and I/O handling**

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

1.	Given the CPU clock rate is 1 MHz and the program takes 55 million cycles to execute. What's the CPU time?	CO1	[K_2]
2.	State the purpose of Stacks and Queues.	CO1	[K_2]
3.	Distinguish between singe bus and multi bus organization.	CO2	[K_2]
4.	State the purpose of control store.	CO2	[K_2]
5.	Discuss the various methods used for removing guard bits.	CO2	[K_2]
6.	Calculate the value of A - B using 2's compliment arithmetic for the given two 16-bit binary numbers A= 1001 1011 1101 and B =1001 0111 1001	CO2	[K_2]
7.	Define Hit and Miss in cache .	CO2	[K_2]
8.	Compare between primary memory and Secondary memory	CO2	[K_2]
9.	An instruction pipeline consists of 4 stages – Fetch (F), Decode field (D), Execute (E) and Result Write (W). The four instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below	CO2	[K_3]

No. of cycles needed for

Instruction	F	D	E	W
1	1	2	2	1
2	1	3	2	1
3	1	2	2	2
4	2	3	1	1

Find the number of clock cycles needed to perform the 4 instructions in pipelined execution.

10. When data hazard occurs? Give an example CO2 [K_2]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11. a) Assume a two address instruction format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and the operation done in every instruction. 8 CO1 [K_3]
    i. Move (R5)+ , R1
    ii. ADD (R5)+, R1
    iii. Move 100(R_5), R_3
    iv. Add #100, R_5

    b) Explain the components of a computer system with a neat block diagram. 8 CO1 [K_2]

12. a) Explain about the hardwired control method of generating control signals with a neat diagram. 10 CO2 [K_2]

    b) Write the control sequence for the instruction Sub (R1), R2. 6 CO2 [K_3]

13. a) Explain floating point addition and multiply rules with a suitable example. 8 CO3 [K_2]

    b) Multiply -11* -15 using Booth multiplication algorithm 8 CO3 [K_3]

14. a) Describe how virtual address is translated into physical address with the help of a block diagram 8 CO4 [K_2]

    b) A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the block –set-associative manner, with 4 blocks per set and 64 words per block. 8 CO4 [K_3]

i. Calculate the number of bits in each of the TAG,SET and WORD firelds of the main memory address format.

ii. Assume that the cache is initially empty, suppose that the processor fetches 4352 words from locations 0,1,2,3,…,4351, in that order. It then repeats this fetch sequence nine more times. If the cache is 10 times faster than the main memory , estimate the improvement factor resulting from the use of the cache. Assume that the LRU algorithm is used for block replacement.

15.	a)	With a neat diagram explain the working principle of DMA.	8	CO5	[K_2]
	b)	What are the various situations where an instruction pipeline cans stalls? Illustrate with a suitable example.	8	CO5	[K_2]
16.	a)	Given Dividend= 1000 and Divisor = 011. Perform division operation using restoring algorithm.	6	CO2	[K_3]
	b)	Define cache memory. Explain any two mapping techniques associated with cache Memories.	10	CO4	[K_2]

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