KUMARAGURU college of technology
character is life

Register Number:……

M.E/PHD DEGREE EXAMINATIONS: APRIL / MAY 2024

(Regulation 2018)

Second Semester

EMBEDDED SYSTEM TECHNOLOGIES

P18ESE2002: CMOS VLSI Design

COURSE OUTCOMES

CO1: Understand the fundamental concepts of VLSI design process and CMOS fabrication process.

CO2: Study the electrical properties of MOS devices and characteristics of CMOS logic.

CO3: Interpret the CMOS design rules and circuit characteristics

CO4: Design simple digital modules using CMOS logic

CO5: Apply verilog HDL on design of simple digital circuits

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Find the sequence of steps in VLSI fabrication process CO1 [K2]

   a) dielectric and polysilicon layer deposition, oxidation, lithography, and dry etching
   b) Lithography, dielectric and polysilicon layer deposition, oxidation and dry etching
   c) Lithography, oxidation, dielectric and polysilicon layer deposition and dry etching
   d) dielectric and polysilicon layer deposition, oxidation, Lithography, and dry etching

2. In basic inverter circuit _____ is connected to ground. CO1 [K_2]

   a) source
   b) gates
   c) drain
   d) resistance

3. Pass transistors are transistors used as _____ CO2 [K_1]

   a) switches connected in parallel
   b) switches connected in series
   c) inverters used in series
   d) inverter used in parallel

4. Match the following CO2 [K_2]

List I	List II
A. Noise Margin is	i. V_{IH} and V_{IL}

B. The Lower Noise Margin is given by	ii. Amount of noise the logic circuit can withstand
C. The Uncertain or transition region is between	iii. V_{IL}-V_{OL}
D. The Higher Noise Margin is given by	iv. $V_{OH} - V_{IH}$

a) ii, iii, i, iv b) iv, iii, i, ii

c) i, ii, iii, iv d) iii, ii, i, iv

5. Stick diagrams are those which convey layer information through? COL [K_2]

a) thickness b) shapes

c) layers d) color

6. For 5 micron technology, What is the sheet resistance Rs value for a metal? COL [K_5]

a) 0.03 b) 0.02

c) 0.04 d) 0.01

7. Assertion (A): Power dissipation is small in switch logic COL [K_5]

Reason (R): Switch logic approach takes no static current from the supply rails

a) A is true; R is false b) A is false; R is true

c) Both A and R are false d) Both A and R are true

8. When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is: COL [K_3]

a) 1 b) 0

c) High impedance d) Low impedance

9. What are the blocks present in Behavioral modeling COL [K_2]

a) Initial block b) Always block

c) Begin block d) End module

10. _____ modeling describes the usage of logic gates and specifies the way they are wired or connected. COL [K_1]

a) Data flow b) Gate level

c) Behavioral d) Gate and data flow modeling

PART B (10 x 2 = 20 Marks)

11. Differentiate full custom over semi-custom VLSI Design. CO1 [K_2]

12.	Identify the importance of silicon on insulator.	CO1	[K_2]
13.	Which transistor can be used in enhancement mode?	CO2	[K_1]
14.	Sketch the pass transistor AND gate logic.	CO2	[K_3]
15.	What is the importance of CMOS layout design rules?	CO3	[K_1]
16.	Define sheet resistance.	CO3	[K_2]
17.	Name few circuits for switch logic and mention its importance.	CO4	[K_2]
18.	Define clocked sequential circuit.	CO4	[K_1]
19.	Write the Verilog code for Ex-OR gate in data flow modeling.	CO5	[K_5]
20.	What is test bench in Verilog?	CO5	[K_2]

PART C (6 x 5 = 30 Marks)

21.	Discuss the difference between logical design and physical design in VLSI.	CO1	[K_2]
22.	Calculate the threshold voltage V_{TO} at V_{SB}=0, for a polysilicon gate n-channel MOS transistor with the following parameters: substrate doping density N_A= 10^{16} cm^{-3} polysilicon gate doping density N_D=2x10^{20} cm^{-3} gate oxide thickness t_{ox}=500 Å and oxide interface fixed charge density N_{ox}=4x$10^{10}$$cm^{-2}$	CO2	[K_5]
23.	Draw and discuss the CMOS inverter DC transfer characteristics.	CO2	[K_2]
24.	Define latch up and briefly explain the ways to prevent it.	CO3	[K_2]
25.	Discuss the general architecture of pre-charged domino CMOS logic.	CO4	[K_2]
26.	Write a Verilog code for 4:1 Mux in behavioral modeling.	CO5	[K_5]

Answer any FOUR Questions

PART D (4 x 10 = 40 Marks)

27.	Elaborate the wafer processing methodology in detail.	CO1	[K_2]
28.	Explain the different second order effects in CMOS transistor.	CO2	[K_2]
29.	Draw the circuit diagram of one bit dynamic shift register and explain its functionality.	CO3	[K_3]

30. Implement the given Boolean expression in static CMOS logic CO4 [K_5]

$Y = \overline{(A+B)\cdot(C+D)\cdot(E+F+(G\cdot H)}$

31. Write the Verilog code for Verilog code for 4 to 2 line Encoder and JK flip flop in behavioral modeling. CO5 [K_5]

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