KUMARAGURU
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Register Number:…….

M.E. DEGREE EXAMINATIONS: APRIL/MAY 2024

(Regulation 2018)

Second Semester

EMBEDDED SYSTEM TECHNOLOGIES

P18EST2002: Embedded Processors

COURSE OUTCOMES

CO1: Describe the functional requirements of the hardware and software components of ARM processor Families.

CO2: Apply instruction set to program ARM processor.

CO3: Dramatize DSP Application using ARM processor.

CO4: Outline the Black fin processor in all aspects.

CO5: Implement practical DSP applications using Blackfin processor.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Assertion (A): The operand can be modified before it is used in certain ARM instructions. CO2 [K_2]

   Reason (R): One operand to ALU is routed through the Barrel shifter.

   a) Both A and R are false
   b) A is true but R is false
   c) R is true but A is not related with R
   d) Both A and R are true and R is correct explanation of A

2. ARM instructions are all ____bit long CO2 [K_2]

   a) 8
   b) 16
   c) 32
   d) 64

3. Digitizing an analogue signal is carried out by _____ CO3 [K_2]

   a) Modulation
   b) demodulation
   c) sampling
   d) Clipping

4. Match the list I items with list II for ARM registers in user mode. CO1 [K_2]

List I	List II
A. r0	i. stack pointer
B.r13	ii. general purpose register
C.r14	iii. program counter
D.r15	iv. link register

	A	B	C	D
a)	ii	i	iv	iii
b)	iv	iii	ii	i
c)	i	iii	iv	ii
d)	iii	i	ii	iv

5. cpsr stands for _____ CO1 [K_2]

a) Current Program Status Register
b) Current Program Stack Register
c) Carry Program Status Register
d) Carry Program Stack Register

6. ISR stands for_____ CO3 [K_2]

a) Interrupt Server Routine
b) Interrupt Service Register
c) Instruction Service Routine
d) Interrupt Service Routine

7. The Blackfin processor provides both the functionalities of a micro-controller unit & _____within a single processor by allowing flexibility. CO4 [K_2]

a) microprocessor
b) counter
c) digital signal processor
d) ports

8. Assertion (A): The Blackfin processor includes two dual-channel synchronous serial ports SPORT0 & SPORT1 used for serial & multiprocessor communications.
Reason (R): High-speed and synchronous serial port that supports I^2S, TDM & various other configurable framing modes for connecting DACs, ADCs, FPGAs & other processors. CO4 [K3]

a) Both A and R are false
b) A is true but R is false
c) R is true but A is not related with R
d) Both A and R are true and R is correct explanation of A

9. CODEC units contains_____ CO5 [K_2]

a) ADC
b) DAC
c) LPF
d) all of the above

10.	Blackfin processor is more suitable for_____.	CO5	[K_2]
	a) real time processing b) non-real time processing c) digital counting d) multiplexing		

PART B (10 x 2 = 20 Marks)

11.	What is AMBA bus?	CO1	[K_2]
12.	Mention the role of memory controller.	CO1	[K_3]
13.	What is thumb instruction set?	CO2	[K_2]
14.	Identify the function of instruction MOVS R1, #10.	CO2	[K_2]
15.	Mention any two guidelines for Writing DSP Code for ARM.	CO3	[K_3]
16.	What is an exception?	CO3	[K_2]
17.	List few features of blackfin processor	CO4	[K_2]
18.	Justify the need for DMA operation in blackfin processor.	CO4	[K_2]
19.	What is real time processing?	CO5	[K_2]
20.	Mention two functions of graphic equalizer.	CO5	[K_2]

PART C (10 x 5 = 50 Marks)

21.	Discuss on RISC design philosophy.	CO1	[K_2]
22.	Describe the data flow model of ARM with flow chart.	CO1	[K_3]
23.	Illustrate the types of addressing used in ARM instruction set with examples.	CO2	[K_3]
24.	Write embedded c code for ARM to find sum of n numbers.	CO2	[K_3]
25.	Discuss the guidelines for writing DSP Code for the ARM7TDM with suitable example coding.	CO3	[K_3]
26.	Write a note on Interrupt assigning and latency.	CO3	[K_2]
27.	Discuss the concept and working of scratchpad memory.	CO4	[K_2]
28.	Describe the concept of DMA used in blackfin processor.	CO4	[K_2]
29.	Write note on Digital Image Processing with suitable block diagram.	CO5	[K_2]
30.	Discuss the features of embedded audio CODEC with neat sketch.	CO5	[K_2]

Answer any TWO Questions
PART D (2 x 10 = 20 Marks)

31.	Illustrate the working of ARM core dataflow model with suitable flow diagram.	CO1	[K_2]
32.	Illustrate the arithmetic instruction set of ARM with suitable examples for each.	CO2	[K_3]

33. Describe the micro signal architecture of Blackfin processor with neat sketch. CO4 [K_2]

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