Register Number:……..

KUMARAGURU
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B.E. DEGREE EXAMINATIONS: NOV/DEC 2023

(Regulation 2018)

Third Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECI3203**:** Digital System Design

COURSE OUTCOMES

CO1: Apply Boolean algebra, Karnaugh map and Tabulation method to design combinational logic circuits.

CO2: Design and verify sequential logic circuits using flipflops.

CO3: Apply state machine models to design sequential logic circuits.

CO4: Explain different logic families based on performance.

CO5: Design combinational circuits using programmable logic devices.

Time: Three Hours **Maximum Marks: 100**

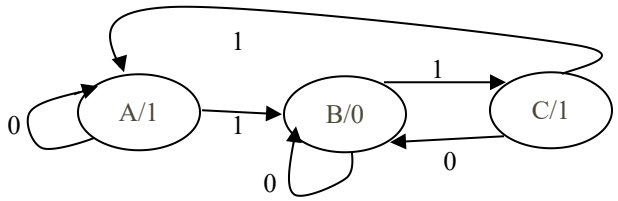
Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

1.	Subtract the number $(1101)_B$ from $(0011)_B$ using 2's complement arithmetic.	CO1	[K_3]
2.	State and prove absorption law.	CO1	[K_2]
3.	How does a carry look-ahead adder reduce propagation delay?	CO1	[K_2]
4.	For 4-bit binary data, draw the logic diagram of odd parity checker.	CO1	[K_2]
5.	Why is a master-slave flipflop required?	CO2	[K_2]
6.	How many unique states are there for a 4-bit Johnson counter?	CO2	[K_2]
7.	Distinguish between Mealy and Moore models.	CO3	[K_3]
8.	What causes races in asynchronous sequential circuits?	CO3	[K_2]
9.	Which logic family has (i) highest speed (ii) least power dissipation?	CO4	[K_2]
10.	Draw the general block diagram of PAL.	CO5	[K_2]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Express the given function in canonical form (SoP) and obtain the truth table: $f(x,y,z) = x'(y'+z)+z'$	8	CO1	[K_3]
	b)	Simplify the given function using K-map and give the expression in PoS form: $f(w,x,y,z) = \sum m(0,1,2,4,5,7,9,12)$	8	CO1	[K_3]
12.	a)	Design and implement a 3-bit magnitude comparator.	8	CO1	[K_3]
	b)	Implement the given function using multiplexer: $f(w,x,y,z) = \sum m(0,1,2,3,7,9,11,12,15)$	8	CO1	[K_3]
13.	a)	Design and implement a 3-bit binary ripple counter using JK flipflops.	8	CO2	[K_3]
	b)	Implement a 4-bit ring counter using schematics and give the state table.	8	CO2	[K_3]
14.	a)	Draw the ASM chart for the state diagram given below: 	8	CO3	[K_2]
	b)	Obtain the primitive flow table for a fundamental mode asynchronous sequential network to meet the following specifications: (i) There are two inputs x_1 and x_2 and one output z (ii) The inputs x_1 and x_2 do not change simultaneously (iii) The output z is to be zero whenever x_1 is zero, independent of the value of x_2 (iv) The output z is to become one if x_2 changes, while x_1 is one and is to remain one until x_1 becomes zero again	8	CO3	[K_3]
15.	a)	With neat schematics, analyze the working of a two-input TTL NAND gate.	8	CO4	[K_2]
	b)	Implement the given functions using PLA: $f_1(x,y,z) = \sum m(0,1,3,4)$ $f_2(x,y,z) = \sum m(1,2,3,4,5)$	8	CO5	[K_3]
16.		Simplify the given function using Tabulation method and implement using logic gates: $f(w,x,y,z) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$	16	CO1	[K_3]

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