

B.E/B.TECH. DEGREE EXAMINATIONS: APRIL/MAY 2010

Third Semester

UO7CS302: COMPUTER ARCHITECTURE

(Common to B.E-Computer Science and Engineering and B.Tech-Information Technology)

Time: Three Hours**Maximum Marks: 100****Answer ALL Questions:****PART A (10 x 1 = 10 Marks)**

1. Pseudo instructions are
 - a. Instructions in any program that have no corresponding m/c code instruction
 - b. instruction that are partially executed
 - c. Instructions for caching
 - d. assembler directives
2. In which addressing mode the address of the location of the operand is given explicitly as a part of the instruction
 - a. absolute mode
 - b. immediate mode
 - c. Indirect mode
 - d. index mode
3. The purpose of denormal numbers is for
 - a. gradual underflow
 - b. gradual overflow
 - c. underflow
 - d. overflow
4. Removing guard bits without changes in the retained bits is called as
 - a. chopping
 - b. Neumann rounding
 - c. rounding
 - d. truncating
5. Bit OR-ing technique is used for modifying
 - a. branch addresses
 - b. micro instructions
 - c. Floating point operations
 - d. Logic instructions
6. If an exception occurs during an instruction execution, all subsequent instructions that may have been partially executed are discarded, called as
 - a. precise exception
 - b. imprecise exception
 - c. inorder exception
 - d. pipelining
7. Data Striping is
 - a. storing identical copies of data on two discs
 - b. a large file is stored in different disks by treating the file into number of smaller pieces
 - c. parity based recovery scheme
 - d. parity checking scheme, without requiring a full duplication of disks
8. Look-up tree is
 - a. Support multiple outstanding misses
 - b. Support multiple misses

- c. Support multiple outstanding hits d. Supports multiple single hits
9. Full handshake provides
- a. highest degree of flexibility and reliability b. only flexibility
c. only reliability d. efficiency
10. Which instructions executed only while the processor is in the supervisor mode are called?
- a. privileged instructions b. vectored instructions c. interrupt nesting d. interrupt enable

PART B (10 x 2 = 20 Marks)

11. Give the concept of pipelining
12. What is use of loader?
13. What are the main features of Booth's algorithm?
14. What are the ways to truncate the guard bits?
15. Differentiate Micro programmed control from hardwired control.
16. What are the types of pipeline hazards?
17. What is the mapping procedures adopted in the organization of a cache memory?
18. Define data stripping?
19. What is polling?
20. What is a privileged instruction?

PART C (5 x 14 = 70 Marks)

21. (a) Describe the different classes of instruction format with example and different addressing modes.

(OR)

(b) (i) Explain the basic input operations with suitable examples. (12)

(ii) What are condition code flags? (2)

22. (a) (i) Explain the organization of a sequential binary multiplier with example. (12)
(ii) How bit pair recoding of multiplier speeds up the multiplication process? (2)

(OR)

(b) Explain the Integer division techniques with suitable example.

23. (a) Explain the multiple bus organization structure with neat diagram.

(OR)

(b) Give the organization of the internal data path of a processor that supports a 4-stage pipeline for instructions and uses a 3-bus structure and discuss the same.

24. (a) Discuss the virtual memory management technique in detail.

(OR)

(b) What is memory interleaving? Explain with neat diagram

25. (a) Explain about the interrupts in detail.

(OR)

(b) Explain in detail the various standard I/O interfaces.
