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B.E. DEGREE EXAMINATIONS: APRIL / MAY 2010

Fourth Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

U07EI403: Digital Logic Circuits

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (10 x 1 = 10 Marks)

1) The output of a logic gate is '1' when all its input are at logic'0' the gate is either ,

A) a NAND or an EX-OR gate B) a NOR or an EX-OR gate

C) a AND or an EX-NOR gate D) a NOR or an EX-NOR gate

2) The number of comparisons carried out in a 4 bit flash type A/D converter is

A) 16 B) 15 C) 4 D) 2

3) If $\bar{x}x\bar{y} = 0$, then which one of the following is true

A) $\bar{x}\bar{y} + \bar{y}x + xz = x\bar{y} + yz$ B) $\bar{x}\bar{y}\bar{z} + xyz = xy\bar{z} + \bar{x}yz$

C) $\bar{x}y + \bar{y}x = xy + \bar{x}\bar{y}$ D) $\bar{x}yx = 1$

4) Assuming that only the X and Y logic inputs are available their complements $\bar{x}$ and $\bar{y}$ are not available, what is the maximum number of two-injput NAND gates are require to implement $X \oplus Y$?

A) 2 B) 3 C) 4 D) 5

5) The digital multiplexer is basically a combination logic circuit to perform the operation

A) AND-AND B) OR-OR C) AND-OR D) OR-AND

6) An R-S Latch is a

A) combinational circuit B) synchronous sequencial circuit

C) one bit memory element D) one clock delay element

7) A mod 2 counter followed by mod 5 counter is

A) same as mod 5 counter followed by mod 2 counter B) a decade counter

C) a mod 7 counter D) mod 5 counter

8) The minimum number of NAND gates required to implement $A + A\bar{B} + A\bar{B}C$ is equal to

A) zero B)1 C) 4 D) 7

9) The decimal equivalent of the hexadecimal number E5 is

A) 279 B) 229 C) 427 D) 3000

10) How many FFs are required to build a binary counter circuit to count from 0 to 1023?

A) 1 B) 6 C) 10 D) 24

PART B (10 x 2 = 20 Marks)

11. Convert an octal number 372 to its decimal equivalent.
12. Write the truth table for universal gates.
13. Explain Full adder.
14. Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method. Also subtract by direct method and compare.
15. Write down the applications of FF.
16. Define Moore machine and Mealy machine.
17. Write down the characteristic equation of S-R FF.
18. Simplify the expression $AB + \overline{AC} + A\overline{B}C(AB + C)$.
19. How many 16K x 4 RAMs are required to achieve a memory with a capacity of 64K and word length of 8 bits.
20. What is Noise Margin?

Part –C 5 x 14 =70 marks

21. (a) (i) Simplify the expression $\overline{\overline{A\overline{B}} + ABC + A(B + A\overline{B}}$.

(ii) Express the function $Y = A + \overline{B}C$ in (a) Canonical SOP and (b) Canonical POS.

(OR)

(b) (i) Simplify the expression $Y = \overline{A}C\left[\overline{\overline{A}BD}\right] + \overline{A}B\overline{C}\,\overline{D} + A\overline{B}C$.

(ii) Simplify the expression $Y = \sum_m(7,9,10,11,12,13,14,15)$ using the K-map method.

22. (a) (i) Draw and explain 4 to 1 multiplexer.

(ii) Implement the following function using a multiplexer $F(A, B, C) = \sum(1,3,5,6)$.

(OR)

(b) Draw and explain about 4 to 16 decoder Circuit.

23. (a) Explain in detail the realization of J.K FF using R.S FF.

(OR)

(b) Explain about the three Bit up counter implementation and application.

24. (a) Design an asynchronous circuit that will output only the second pulse received whenever a control input is asserted from LOW to HIGH state and will ignore any other pulse. Assume necessary conditions.

(OR)

(b) Explain in details of the problems in Asynchronous circuits.

25. (a) Construct 512 x 4 bit memory using two 256 x 4 bit PROM.

(OR)

(b) Explain Open collector output condition of T^2L with a suitable example.

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