Register Number: .....

B.E DEGREE EXAMINATIONS: APRIL / MAY 2010

Third Semester

MECHATRONICS ENGINEERING

U07MH303: Digital Electronics

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions: -

PART A (10 x 1 = 10 Marks)

1. A K-map of five Variable will have_____ cells.

   a) 64 b) 28 c) 32 d) 31

2. Gray code is _____ code.

   a) Weighted code b) Non Weighted code c) Reflective d) Sequential

3. A decoder with 64 output line has _____ select lines.

   a) 5 b) 6 c) 4 d) 8

4. In a 4 bit parallel adder each full adder is considered to have a propagation delay of 30 ns then S_3 (MSB) will reach _____ time.

   a) 120 ns b) 120 ps c) 120 hs d) 120ms.

5. Refresh circuit is required for _____ RAM

   a) Dynamic b) Static c) Volatile d) Non-Volatile

6. In which flip-flop race around condition will take place?

   a) SR b) D c) T d) JK.

7. Hazard may occur in _____ circuits

   a) Synchronous Sequential b) Asynchronous sequential

   c) Combinational Circuit d) Transistor Circuit

8. A _____ occurs when an asynchronous circuit makes a transition through a series of unstable states.

   a) Non-critical race b) Critical race c) Cycles d) Races

9. The programmable array logic has programmable _____ gates and fixed_____ gates.

   a) NAND, NOR b) OR, AND c) AND, OR d) NOR,NAND

10. The output of the Moore model is a function of

    a) Both the present state & input b) Only present state

    c) Both the next state & input d) Only next state

PART B (10 x 2 = 20 Marks)

11. Define redundancy theorem.
12. What are the drawbacks of K-map method?
13. Implement the logic function $f = AB + \overline{A}\,\overline{B}$ using a suitable multiplexer.
14. What is meant by an "Essential-Prime-Implicant"?
15. Derive the characteristics of a D-flip flop.
16. What is a binary counter?
17. What is meant by critical race?
18. What are static 1 and static 0 hazards?
19. Define ASM chart.
20. Draw the block diagram of Mealy and Moore model of FSM.

PART C (5 x 14 = 70 Marks)

21.a) (i) Simplify the boolean function F (A,B,C,D)= $\Sigma m(1,3,7,11,15)+\sum d\ (0,2,5)$. If don't care conditions are not taken care, what is the simplified boolean function? What are your comments on it? Implement both circuits.

(ii) Implement $Y=(A+C)(A+\overline{D})(A+B+\overline{C})$ using NOR gates only.

(OR)

b) What is the advantage of using tabulation method? Determine the prime implicants of the following function using tabulation method.

$F(w,x,y,z) = \Sigma(1,4,6,7,8,9,10,11,15)$.

22. a) (i) Implement the following function using with a (8:1) multiplexer.

$F(a,b,c,d)= \Sigma(0,1,5,7,10,14,15)$ (8)

(ii) Design a full Subtractor. (6)

(OR)

b) Design a network to convert 8421 BCD code to EX-3 code.

23. a) (i) Draw and explain 4-bit parallel in serial out shift register. (8)

(ii) Design and explain the working of a synchronous mod-3 counter. (6)

(OR)

b) Design a synchronous counter for 4 → 6 →7 → 3 → 1 → 4 ..... avoid lockout condition. Use JK type design.

24. a) Using truth-table, simplify and implement the following function using NAND and NOR gates.

$$F(a, b, c, d) = \Sigma m(1, 5, 7, 14, 15)$$

(OR)

b) Describe the different types of hazards in digital circuits with illustrative examples.

25. a) (i) Compare Moore and Mealy models for digital design. Use block diagrams. (7)

(ii) Also, show how one model could be transformed from the other. Use your own example. (7)

(OR)

b) Draw the state transistor diagram for a sequence detector described below:

A system receives a binary stream bit by bit from left. The system generates an output Y=1 when it receives the combination '011'. Otherwise, the output Y=0.

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