Register Number: ……

M.E DEGREE EXAMINATIONS: APRIL/ MAY 2010

Second Semester

APPLIED ELECTRONICS

ANE505: Computer Architecture and Parallel Processing

Time: Three Hours. **Maximum Marks: 100**

Answer ALL Questions

PART A (10 x 2 = 20 Marks)

1. Name the shared memory multiprocessor models.
2. Compare control flow and data flow mechanisms.
3. Mention the various four phases of instruction pipe line operations.
4. Define Hit ratio.
5. What are the internal data forwarding operations?
6. State significance of local and backplane buses.
7. Mention the various instruction types.
8. What are the broadcasting schemes used to implement replication through the control network?
9. What are the requirements of control section (CS) operation?
10. Compare multiprocessing and multi tasking.

PART B (5 x 16 = 80 Marks)

11. a) Explain in detail the shared memory multiprocessors

(OR)

b) (i) Discuss in detail data dependence with example. (12)

(ii) Compare hardware and software parallelism. (4)

12. a) (i) Compare RISC and CISC architectures . (8)

ii.Discuss how pipe lining is achieved in super scalar processors. (8)

(OR)

b) (i) Explain the architecture of VLIW processor. (10)

(ii) Compare physical address and virtual address caches (6)

13. a) Explain in detail the various issues related to instruction pipeline design.

(OR)

b) (i) Explain various cache events and actions. (8)

(ii) With suitable diagrams and illustration discuss about adaptive routing. (8)

14. a) (i) Discuss in detail the various vector access memory schemes. (12)

(ii) Write a short note on multi - threading. (4)

(OR)

b) Explain in detail about the SIMD computer organization.

15. a) What is shared variable communication? Discuss the related issues in detail for establishing such a communication.

(OR)

b) (i) Compare functional Programming and logic programming models. (6)

(ii) Discuss in detail global and local optimization techniques. (10)

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